## **Features**

- □ Improved PSRR at 217 Hz & 1 KHz 60 dB
- **D** Power output at 5.0V, 10% THD+N, 4 $\Omega$  2.0 W (typ.)
- $\label{eq:constraint} \square \quad \mbox{Power output at 5.0V, 1% THD+N, 8} \Omega \qquad 1.5 \ \mbox{W (typ.)}$
- $\Box$  2.2V 5.5V operation
- □ Improved circuitry eliminates pop-click noise during turn-on and turn-off transitions
- □ No output coupling capacitors, snubber networks or bootstrap capacitors required
- □ Unity-gain stable
- □ External gain configuration capability
- Packages: SOP8

#### **General Description**

The 8002 is a Class-AB audio power amplifier. It is capable of delivering 2.0 watts of continuous average power to an 4 $\Omega$  BTL load with less than 10% distortion (THD+N) from a 5V<sub>DC</sub> power supply, or 1.5 watts continuous average power to an 8  $\Omega$  BTL load with less than 1% distortion.

The 8002 is designed specifically to provide high quality output power with a minimal amount of external components. It does not require output coupling capacitors or bootstrap capacitors. The 8002 is ideally suited for audio speakers and other low voltage applications.

With special pop-click eliminating circuit, the 8002 provides perfect pop-click characteristic during turn-on and turn-off transitions.

The 8002 is unity-gain stable and can be configured by external gain-setting resistors.

## Applications

- Audio speakers
- Desktop computers
- Low voltage audio systems

## **Pin Diagrams**

#### Mini Small Outline Package ( SOP8) (Top View) 1 8 SHD - Vout2 2 7 BP GND 3 6 INP VDD 4 5 INN Vout1

## **<u>Pin Description</u>**

No.	Pin Name	I/O	Description		
1	SHD	Ι	Shut-down Logical Control, '1' is active.		
2	BP	I/O	Analog ground for inner OPAs. It's about a half of VDD.		
3	INP	Ι	Positive Input		
4	INN	Ι	Negative Input		
5	Vout1	0	Negative BTL Output		
6	VDD	I/O	Power Supply $(2.2 - 5.5 \text{ V})$		
7	GND	I/O	Ground		
8	Vout2	0	Positive BTL Output		

## **Typical Application Circuit**



FIGURE 1. 8002 Typical Application Circuit



FIGURE 2. 8002 Differential Amplifier Configuration

## **External Components Description**

Components	Functional Description
Ri	Inverting input resistance which sets the closed-loop gain in conjunction with
	Rf. This resistor also forms a high pass filter with Ci at $fc = 1/(2\pi Ri^*Ci)$ .
Ci	Input coupling capacitor which blocks the DC voltage at the amplifiers input
	terminates. Also creates a high-pass filter with Ri at $fc = 1/(2\pi Ri^*Ci)$ .
Rf	Feedback resistance which sets the closed-loop gain in conjunction with Ri. The
	gain is A <sub>VD</sub> =2*(Rf/Ri).
Cs	Supply bypass capacitor which provides power supply filtering.
Cb	Bypass pin capacitor which provides half-supply filtering. Refer to the section.

Absolute Maximu	<u>m Ratings</u>	<b>Operating Ratings</b>				
Supply Voltage	-0.3V to 6V	Temperature Range	$-40^{\circ}\mathrm{C} \leq T_{\mathrm{A}} \leq 85^{\circ}\mathrm{C}$			
Input Voltage	-0.3V to VDD+0.3V	Supply Voltage	$2.2V \le V_{DD} \le 5.5V$			
Power Dissipation						
See Di	ssipation Rating Table					
Junction Temperature	-40°C to $+150$ °C	NOTE: Absolute Maximum Ratings indicate limits				
Storage Temperature	-65℃ to +150℃	beond which damage to the device may occur.				
Thermal Resistance		Operating Rating indicate	conditions for which the			
$\theta_{\rm JC}(\rm MSOP8)$ 56°C/V		device is functional, but do not guarantee specific				
$\theta_{JA}(MSOP8)$	190°C/W	performance limits.				
$\theta_{JA}(SOP8)$ 184°C/W						

## **Electrical Characteristics**

The following specifications apply for the circuit shown in Figure 1, unless otherwise specified. Limits apply for  $T_A = 25$  °C.

$V_{DD} = 5V$	

Symbol	Parameter	Conditions	Spec			Units
	r ar anneter	Conditions	Min.	Тур.	Max.	Units
т	Our Supply Current	$V_{IN} = 0V$ , $8\Omega$ Load		3.0	8	mA
I <sub>DD</sub>	Quiescent Power Supply Current	$V_{IN} = 0V$ , No Load		2.5	7	mA
I <sub>SD</sub>	Shutdown Current	V <sub>IN</sub> =0V, V <sub>SHD</sub> =GND, No Load		0.5		uA

V <sub>SDIH</sub>	Shutdown Voltage Input High		1.2			V
V <sub>SDIL</sub>	Shutdown Voltage Input Low				0.9	V
V <sub>OS</sub>	Output Offset Voltage		-50	6	50	mV
THD+N	Total Harmonic Distortion+Noise	Po=0.5Wrms, f=1KHz,		0.07		%
Po	Output Power	THD+N<=1%, f=1KHz, 8Ω Load		1.5		W
Po	Output Power	THD+N<=10%, f=1KHz, 4Ω Load		2.0		W
PSRR	Power Supply Rejection Ratio	Input terminated with 10Ω, V <sub>DDRIPPLE</sub> =0.2V <sub>P-P</sub> , f=217Hz		60		dB
		Input terminated with 10Ω, V <sub>DDRIPPLE</sub> =0.2V <sub>P-P</sub> , f=1KHz		61		dB
$\mathrm{T}_{\mathrm{WU}}$	Wake-up time			100		ms

# $\Box \quad V_{DD} = 3V$

Sympol	Parameter	Conditions	Spec			I.I.n.ita
Symbol			Min.	Тур.	Max.	Units
т	Quiescent Power Supply Current	$V_{IN} = 0V$ , $8\Omega$ Load		2	7	mA
I <sub>DD</sub>	Quiescent Power Supply Current	$V_{IN} = 0V$ , No Load		1.5	6	mA
I <sub>SD</sub>	Shutdown Current	V <sub>IN</sub> =0V, V <sub>SHD</sub> =GND, No Load		0.5		uA
V <sub>SDIH</sub>	Shutdown Voltage Input High		1.0			V
V <sub>SDIL</sub>	Shutdown Voltage Input Low				0.7	V
V <sub>OS</sub>	Output Offset Voltage		-50	6	50	mV
THD+N	Total Harmonic Distortion+Noise	Po=0.25Wrms, f=1KHz,		0.08		%
Po	Output Power	THD+N<=1%, f=1KHz,		350		mW
10		8Ω Load				
	Power Supply Rejection Ratio	Input terminated with $10\Omega$ ,		57		dB
PSRR		V <sub>DDRIPPLE</sub> =0.2V <sub>P-P</sub> , f=217Hz				
		Input terminated with $10\Omega$ ,		58		dB
		V <sub>DDRIPPLE</sub> =0.2V <sub>P-P</sub> , f=1KHz				
T <sub>WU</sub>	Wake-up time			75		ms



SOP8

MILLIMETER

0.18

1.40

0.65 0.75

0.41 0.43

0.20

4.90

6.00

3.90

1.27BSC

1.05BSC

0.65 0.80

NOM MAX

1.77

0.28

1.60

0.48

0.26

0.21

5.10

6.20

4.10

8°

MIN

0.68

1.20

0.55

6.39

6.38

0.21

0.19

4.70

5.80

3.70

0.50

0