600/1200 MHz, Arm® Cortex®-A55 Dual/Single MPCore, 400/800 MHz, Dual Arm® Cortex®-R52 on-chip FPU and NEON™, 2.0 MB of on-chip SRAM, LPDDR4-1600 with 16-bit, Ethernet MAC, EtherCAT, USB 2.0 high-speed, PCI Express Gen3, SD card host interface, NAND Flash controller, CAN/CANFD, various communications interfaces such as an xSPI and ΔΣ interface, encoder interfaces, and security functions

Features

On-chip 64-bit Arm Cortex-A55 processor

- Dual/Single MPCore cores
- Maximum operating frequency:
  - Core: 600/1200 MHz
  - DSU: 500/1000 MHz
- 64-bit Arm Cortex-A55 Dual/Single MPCore cores (revision r2p0)
- Address space: 32 Gbytes
- L1 cache:
  - I-cache: 32 Kbytes (with parity)
  - D-cache: 32 Kbytes (with ECC)
- L2 cache: 128 Kbytes (with ECC)
- L3 cache: 256 Kbytes (with ECC)
- NEON/FPU supported
- Cryptographic extension supported (Security product only)
- Arm V8.2-A architecture

On-chip 32-bit Arm Cortex-R52 processor

- High-speed realtime control with operating frequency of 400/800 MHz
- On-chip Dual 32-bit Arm Cortex-R52 (revision r1p4)
- Tightly coupled memory (TCM) with ECC
  - CPU0, CPU1: 512 KB/64 KB
- Instruction cache/data cache with ECC
  - CPU0, CPU1: 16 KB per cache
- High-speed interrupt
- NEON/FPU supported
- Harvard architecture with 8-stage pipeline
- Supports the memory protection unit (MPU)
- Arm CoreSight architecture, includes support for debugging through JTAG and SWD interfaces.
- No DCLS (Dual Core Lock Step) support

Low power consumption

- Standby mode and module stop function

On-chip SRAM

- 2.0 MB of the on-chip SRAM with ECC
- 200 MHz

LPDDR4 SDRAM Memory Interface

- Data transfer: 1.6 Gbps
- Bus width: 16-bit
- Rank: 1
- Size: up to 16 Gb

Data transfer

- DMAC: 16 channels × 3 units

Event link controller

- Module operations can be started by event signals rather than by interrupt handlers.
- Linked operation of modules is available even while the CPU is in the standby state.

Reset and power supply voltage control

- Ten reset sources including a pin reset

Clock functions

- External clock/oscillator input frequency: 25 MHz
- CPU clock frequency: 600/1200 MHz (Cortex-A55), 400/800 MHz (Cortex-R52)
- System clock frequency: 400 MHz (A-Bus), 200 MHz (R-Bus)
- Low-speed on-chip oscillator (LOCO): 240 kHz

Safety functions

- Register write protection, input clock oscillation stop detection and CRC
- Master Memory Protection Unit (MPU)

Security functions (optional)

- Boot mode with security through encryption
- JTAG authentication
- Cryptologic accelerator
- TRNG
- Cortex-A55 Crypto Extension
- TrustZone

Encoder interfaces

- 8 or 4 channels
- EnDat 2.2, BiSS-C, A-format, HIPERFACE DSL, EnDat 3, and BiSS-Line-compliant interfaces
- Frequency-divided output from an encoder

Various communications interfaces

- Ethernet
  - EtherCAT slave Controller: 3 ports
  - Ethernet switch: 3 ports
  - Ethernet MAC: 1 port × 3 units
  - HSR/PRP switch: 2 ports
- USB 2.0 high-speed host/functions: 1 channel
- CAN/CANFD (compliant with ISO11898-1): 2 channels
- SCI with 16-byte transmission and reception FIFOs: 6 channels + 8 channels (for encoder)
- I2C bus interface: 3 channel for transfer at up to 400 kbps
- SPI: 4 channels
- xSPI: 2 channels
- PCI Express Gen2: 1 lane × 1 ports
- SD card host interface: 2 channels
- NAND Flash controller

External host interface

- Serial host interface
- Parallel host interface

External address space

- Buses for high-speed data transfer at up to 100 MHz
- Support for up to 4 CS areas
- 8-, 16- or 32-bit bus space is selectable per area

Up to 48 extended-function timers

- 16-bit × 8 + 32-bit MTU3 (9 channels), 32-bit GPT (31 channels)
- 16-bit CMT (6 channels), 32-bit CMTW (2 channels)

ΔΣ interface

- Up to 15 ΔΣ modulators are connectable externally.

Trigonometric function unit

- 2 units
- Simultaneous calculation of sine and cosine
- Simultaneous calculation of arctangent and hypot_k

12-bit A/D converter

- 12 bits × 3 unit (4 channels for unit 0, 1, 8 channels for unit 2)

Temperature sensor for measuring temperature within the chip

General-purpose I/O ports

- Input pull-up/pull-down
- The locations of input/output functions for peripheral modules are selectable from among multiple pins.

Operating temperature range

- Tj = -40 to +125°C

1. Overview

1.1 Outline of Specifications

The MPU is a high-performance ASSP that has Arm® Cortex®-A55 dual MPCore and dual Arm® Cortex®-R52 processor with Floating-Point Unit (FPU) and NEON™. It incorporates integrated peripheral functions necessary for system configuration.

Table 1.1 CPU

Feature	Functional description
Arm® Cortex®-A55	• One processor which consists of a dual/single MPCore cores • Operating frequency – Core: 600 MHz/1200 MHz – DSU: 500 MHz/1000 MHz • 64-bit CPU Cortex-A55 designed by Arm (core revision r2p0) • Address space: 32 GB • L1 cache – I-cache: 32 KB (with parity) each core – D-cache: 32 KB (with ECC) each core • L2 cache: 128 KB (with ECC) • L3 cache: 256 KB (with ECC) • Arm V8.2-A architecture • NEON/FPU supported • Cryptographic extension supported (security product only)
Arm® Cortex®-R52	• Two processors which consist of single core • Operating frequency – Each CPU0 and CPU1: 400 MHz/800 MHz • 32-bit CPU Cortex-R52 designed by Arm (core revision r1p4) • Address space: 4 GB • Instruction cache – Each CPU0 and CPU1: 16 KB (with ECC) • Data cache – Each CPU0 and CPU1: 16 KB (with ECC) • Tightly coupled memory (TCM) – Each CPU0 and CPU1 ATCM: 512 KB (with ECC) 0 wait (400 MHz) / 1 wait (800 MHz) BTCM: 64 KB (with ECC) 0 wait CTCM: 0 KB • Instruction set: ARMv8-R architecture, so support includes Thumb® and Thumb-2 • 2-stage memory protection unit (MPU) • NEON/FPU supported

Table 1.2 Memory

Feature	Functional description
System SRAM with ECC	• Capacity: 2.0 MB (512 KB × 4 units) (with ECC) • Operating frequency: 200 MHz • SEC-DED (single error correction/double error detection) Error injection supported
One-time programmable memory	• Overwrite protection • Redundancy support • Available information – Unique ID – Authentication settings – Trimming data – Boot mode setting – User area
LPDDR4 SDRAM memory interface	• Data transfer: 1.6 Gbps • Bus width: 16 bits • Rank: 1 • Size: up to 16 Gb • Inline ECC • No support of LPDDR4X • Support on-the-fly decryption/encryption*1

Note 1. This function is supported for security product only.

Table 1.3 System

Feature	Functional description
Operating modes	The operating mode can be selected from the following seven boot modes: ● xSPI0 boot mode (CS0 × 1 boot Serial Flash) ● xSPI0 boot mode (CS0 × 8 boot Serial Flash) ● eMMC boot mode ● SD boot mode ● xSPI1 boot mode (CS0 × 1 boot Serial Flash) ● SCI boot mode ● USB boot mode
Clock generation circuit	● The input clock can be selected from an external clock or external resonator. ● Detection of input clock oscillation stopping ● The following clocks are generated: – Cortex-A55 clock: 600 or 1200 MHz (selectable each core) – Cortex-R52 clock: 400 or 800 MHz (selectable each unit) – A-Bus clock: 400 MHz – R-Bus clock: 200 MHz – High-speed peripheral module clock A (PCLKAH): 400 MHz – Middle-speed peripheral module clock A (PCLKAM): 200 MHz – Low-speed peripheral module clock A (PCLKAL): 100 MHz – High-speed peripheral module clock R (PCLKH): 200 MHz – Middle-speed peripheral module clock R (PCLKM): 100 MHz – Low-speed peripheral module clock R (PCLKL): 50 MHz – ADC clock in the 12-bit A/D converter: 25 MHz – External bus clock 100 MHz (max.) – Low-speed on-chip oscillator: 240 kHz (fixed)
Reset	RES# pin reset, software reset, error reset, Cortex-A55 cluster software reset, Cortex-A55 core0 software reset, Cortex-A55 core1 software reset, Cortex-R52 CPU0 software reset, Cortex-R52 CPU1 software reset
Low-power consumption function	● Standby mode (Cortex-A55, Cortex-R52) ● Module stop function
Interrupt controller (ICU)	● Connect an interrupt to the GIC600 for Cortex-A55 ● Connect an interrupt to the GIC (Generic Interrupt Controller) for Cortex-R52 CPU0 and CPU1 ● Connect an activating trigger to the DMAC and ELC ● Peripheral function interrupts: 589 sources ● External interrupts: 16 sources (IRQ0 to IRQ15 pins) ● Software interrupts: 16 sources ● System error interrupts: 1 source ● 32 levels specifiable for the order of priority in the GIC
Bus state controller (BSC)	● The external address space is divided into four areas (CS0, CS2, CS3, and CS5) for management. ● The following features are configurable for each area independently: Bus size (8, 16, or 32 bits): Available sizes depend on the area. Number of access wait cycles (different wait cycles can be specified for read and write access cycles in some areas). Idle wait cycle insertion (between same area access cycles or different area access cycles). Specifying the memory to be connected to each area enables direct connection to SRAM, SRAM with byte selection, and burst ROM (clocked synchronous or asynchronous). The address/data multiplexed I/O (MPX) interface is also available. ● Outputs a chip select signal (CS0# to CS5#) according to the target area (CS assert or negate timing can be selected by software).

Table 1.4 Direct memory access

Feature	Functional description
Direct memory access controller (DMAC)	● 3 units (16 channels each unit) ● Transfer modes: Single transfer mode and block transfer mode ● Transfer size – Unit 0: 1/2/4/8/16/32/64 bytes – Unit 1, 2: 1/2/4/8/16/32 bytes ● Activation sources: Software trigger, external DMA requests (DREQ), external interrupts, and interrupt requests from peripheral functions

Table 1.5 I/O Ports

Feature	Functional description
General-purpose I/O ports	● 537-pin FBGA – I/O pins: 200 – Input pins: 1 – Pull-up/pull-down resistors: 201 ● 489-pin FBGA – I/O pins: 160 – Input pins: 1 – Pull-up/pull-down resistors: 161 ● The locations of input/output functions are selectable from among multiple pins.

Table 1.6 Event link

Feature	Functional description
Event link controller (ELC)	● Up to 413 event signals can be interlinked with the operation of modules. ● In particular, the operation of timer modules can be started by input event signals. ● Event-linked operation of signals of ports 09 and port 14 is to be possible.

Table 1.7 Timers (1 of 2)

Feature	Functional description
Multi-function timer pulse unit 3 (MTU3)	● 9 channels (16 bits × 8 channels, 32 bits × 1 channel) ● Maximum of 28 pulse-input/output and 3 pulse-input possible ● Select from among 10, 11, 12, or 14 counter-input clock signals for each channel (with maximum operating frequency of 250 MHz) ● Input capture function ● 39 output compare/input capture registers ● Counter clear operation (synchronous clearing by compare match/input capture) ● Simultaneous writing to multiple timer counters (TCNT) ● Simultaneous register input/output by synchronous counter operation ● Buffered operation ● Support for cascade-connected operation ● Automatic transfer of register data ● Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM ● Complementary PWM output mode – Outputs non-overlapping waveforms for controlling 3-phase inverters – Automatic specification of dead times – PWM duty cycle: Selectable as any value from 0% to 100% – Delay can be applied to requests for A/D conversion. – Non-generation of interrupt requests at peak or trough values of counters can be selected. – Double buffer configuration ● Reset synchronous PWM mode Six phases of positive and negative PWM waveforms can be output with desired duty cycles. ● Phase-counting mode: 16-bit mode (channels 1 and 2), 32-bit mode (channels 1 and 2 in cascade connection) ● Counter functionality for dead-time compensation ● Generation of triggers for A/D converter conversion ● A/D converter start triggers can be skipped ● Digital noise filter function for signals on the input capture and external counter clock pins ● Event linking by the ELC

Table 1.7 Timers (2 of 2)

Feature	Functional description
General PWM timer (GPT)	• 32 bits × 31 channels (5 channels × 4 units + 7 channels × 1 unit + 4 channels × 1 unit) • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 500 MHz for LLPP) • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of 3 counters, generation of automatic 3-phase PWM waveforms incorporating dead times • Starting, clearing, stopping, switching, up/down counters, and input capture in response to external or internal triggers • Starting, clearing, stopping, switching, up/down counters, and input capture in response to input level comparison • Internal trigger sources: software and compare-match • Generation of triggers for A/D converter conversion • Digital noise filter function for signals on the input capture and external trigger pins • Event linking by the ELC • Function of output duty 0% and 100% is selectable from troughs or crests/troughs. • Period count function • The buffer transfer operation by counter clearing and compare match • External pulse width measuring function
Compare match timer (CMT)	• (16 bits × 2 channels) × 3 units • Select from among four counter-input clock signals for each channel
Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four counter-input clock signals for each channel • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events.
Watchdog timer (WDT)	• 14 bits × 4 channels • Select from among six counter-input clock signals for each channel
Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 waveform output pins • 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11# • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by input clock oscillation-stoppage detection, PLL oscillation anomaly detection, two types of DSMIF error detection, or software • Additional programming of output control target pins is enabled
Port output enable for GPT (POEG)	• Controlling the output disable for GPT waveform output • Initiation by input level detection of GTETRG pins • Initiation by output disable request from GPT • Initiation by detection of oscillation stop, two types of DSMIF error detection, or by software
Real time clock (RTC)	• A 100-year calendar from 2000 to 2099 • BCD code display • Clock source is division of main oscillator. • Automatic adjustment function for leap years

Table 1.8 Communication interfaces (1 of 3)

Feature	Functional description
Ethernet MAC (GMAC)	• 1 port × 3 units • IEEE802.3 • IEEE1588-2008 • IEEE802.3-az-2010 for EEE • Support for 10/100/1000 Mbps data transfer • Full duplex and half duplex are supported • Programmable frame length to support both standard and jumbo frames up to 16 KB • 32 MAC address registers for the address filter block • Variety of flexible addresses filtering modes are supported • Advanced IEEE 1588-2002 & 2008 Ethernet frame time-stamping supported • MII/RMII/RGMII interface is supported by RMII/RGMII converter • TSN features (IEEE802.1Qbv, IEEE802.1Qbu/802.3br) • Multiple queues support up to 8 RX and 8 TX queues • DMA channels: 8 RX and 8 TX channels • VLAN Filtering, L3 and L4 Filtering
Ethernet switch (ETHSW)	• 3-port PHY interfaces • IEEE802.3 • Support for 10/100/1000 Mbps data transfer • Full and half duplex (1000 Mbps supports full-duplex only) • Hardware switching, lookup, and filtering • QoS with frame prioritization • Priority control based on VLAN Priority (IEEE802.1q), which enables priority reassignment • Classification and priority assignment based on IPv4 DiffServ Code Point Field, IPv6 Class of Service • Queue with eight priority levels • Multi-casting and broadcasting • VLAN frame • IEEE 1588-2008 compatible • Programmable addition, removal and manipulation of ingress and egress VLAN tags, supporting single and double-tagged VLAN frames on each port • Cut-through and hub features • Device level ring (DLR) • Programmable egress rate limit per port • Ingress Configurable broadcast/multi-cast storm protection per port • IEEE802.1X source address authentication supported • IEEE802.1X guest VLAN supported • PRP functionality (IEC 62439-3 edition 2.0- 2012) • Configurable Time Multiplexed (TDMA) output queue scheduler supporting real-time network infrastructures using time slots for bandwidth reservation enabling deterministic delays • Frame preemption • Cyclic queuing and forwarding • Forwarding rule for the TSN-IA profile • A MAC source address filtering • Pattern match 12 channels • Independent two timer modules are available for time-stamping and time for TDMA. • Remote monitoring through SNMP • Power-link capable hub • Ingress filtering and frame header manipulation (active stream identification, flow metering) with Enhanced Frame Parser • 4 additional PTP timer pulse generators • MII/RMII/RGMII interface is supported by RMII/RGMII converter • IEEE1588 UDP/IPv4 1-step end-to-end transparent clock
EtherCAT slave controller (ESC)*1	• One channel (3 ports) • EtherCAT Slave Controller IP core (made by Beckhoff Automation GmbH) implemented • MII interface is supported. RMII/RGMII interface is supported by RGMII converter in Ethernet Subsystem.
Layer3 Ethernet switch module (ESWM)	• The Layer 3 Ethernet Switch Module (ESWM) consists of an Ethernet switch with higher level routing capability and multi-protocol interface support. It allows autonomous frame routing within same and between different network interfaces protocols (for now only Ethernet) for optimized gateway applications.
HSR/PRP switch (HPSW)	• 2-port PHY interfaces • High-availability Seamless Redundancy/Parallel Redundancy Protocol (HSR/PRP) • Transparent clock • Ordinary clock

Table 1.8 Communication interfaces (2 of 3)

Feature	Functional description
USB 2.0 HS host/function module	• One port • Compliance with the USB 2.0 specification • OTG support • Transfer rate High speed (480 Mbps), full speed (12 Mbps), low speed (1.5 Mbps, host only) • Communications buffer – Incorporates 1 KB of RAM for host mode – Incorporates 8 KB of RAM for function mode • DMAC (2 channels) incorporated
Serial communication interface (SCI)	• 6 channels + 8 channels (for encoder) • Six communication modes – Asynchronous interfaces – 8-bit clock synchronous interface – Simple I^2C (master-only) – Simple SPI – Smart card interface – Manchester mode (For channel for encoder, Simple I^2C, Simple SPI, and Smart card interface mode are not supported.) • Clock source is select from among four internal clock signals • Bit rate specifiable with the on-chip baud rate generator • Full-duplex and half-duplex communication • Data length: 7 to 9 bits (Asynchronous mode) • Bit rate modulation • Double speed mode (Asynchronous, Clock Synchronous, Simple SPI mode, Manchester mode) • RS-485 driver control function (Asynchronous mode) • Loopback function to enable self-diagnosis (Asynchronous, Clock synchronous mode)
I^2C bus interface (IIC)	• Three channels • Communication formats: I^2C bus format or SMBus format • Master or slave mode selectable • Supports the multi-master • Maximum transfer rate: 400 kbps (Standard mode and Fast mode)
CAN-FD module (CANFD)	• Two channels • Comply with CAN-FD ISO 11898-1 (2015) • Communication speed – Classical CAN mode: 1 Mbps – CAN FD mode: Nominal bit rate: max. 1 Mbps Data bit rate: max. 8 Mbps • Total 192 message buffers (in case frame size is 76 bytes) – Individual buffers: 64 for TX – Shared buffers: 128 for TX and RX including FIFO • Selectable ID type with 11-bit Standard and 18-bit Extended • Selectable Frame type: Data Frame and Remote Frame • Up to 256 receive rules
Serial peripheral interface (SPI)	• Four channels • SPI transfer facility Using the MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (SPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) capable of handling serial transfer as a master or slave • Data formats – Switching between MSB first and LSB first – Transfer bit length selectable from 4 to 32 bits – 32 bits × 4-stage FIFO transmit and receive buffers – Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • RSPCK can be stopped automatically with the reception buffer full for master reception

Table 1.8 Communication interfaces (3 of 3)

Feature	Functional description
Expanded serial peripheral interface (xSPI)	• Two channels • Comply with JESD251 • Multiple slave up to 2 slaves • Protocol mode: 1/4/8pin with SDR/DDR 1S-1S-1S, 4S-4D-4D, 8D-8D-8D • Support OctaFlash, OctaRAM, HyperFlash and HyperRAM • Protocol mode: 2/4pin with SDR compatible with QSPI 1S-2S-2S, 2S-2S-2S 1S-4S-4S, 4S-4S-4S 1S-1S-4S • Configurable address length • Configurable initial access latency cycle • Support XiP mode • Support up to 256 MB address space • Prefetch function for burst-read with low latency • Outstanding buffer for burst-write with high throughput • Manual command configurable up to 4 commands • Output clock/input strobe port timing shift • Automatic command after released reset: up to 4 commands • Support on-the-fly decryption (decryption read only)*2
SD/MMC Host Interface (SDHI)	• 2 channels (up to 8-bits for channel 0 and 4-bits for channel 1) • SD memory/IO card interface (1-bit/4-bit SD bus) • SD, SDHC, and SDXC SD memory card access supported • Default, high-speed, UHS-I/SDR12, SDR25, SDR50, SDR104, and DDR50 transfer modes supported • Error check function: CRC7 (for command/response), CRC16 (for data) • Card detect function • Write protect supported • MMC interface (1-/4-/8-bit MMC bus) • eMMC device access supported • Backward-compatible, high-speed (SDR/DDR), and HS200 transfer modes supported • High-priority interrupt (HPI) supported
PCI Express Gen2 (PCIE)	• PCI Express Gen1 (2.5 [GT/s]) / Gen2 (5.0 [GT/s]) • Root Complex / Endpoint Applications, Type 0/1 Configuration Register • Lane/Port: 1 lanes × 1 port • Support Polarity inversion • Maximum data payload of 256 bytes, Maximum read request size 512 bytes • Number of outstanding 1-8 • Dynamic control of speed/width up/down configuration • Power Management (not support ASPM L1-Substate) • Error handling/logging (AER Support) • Replay FIFO with ECC • Number of Support Functions 2
NAND Flash controller (NANDC)	• NAND interface with 8-bit bus width • Compatible with ONFI 1.x and 2.x standards • Only support Asynchronous mode (SDR) • DMAC support • Support pages size from 256 B to 16 KB • Number of chip select: 4

Note 1. EtherCAT is a registered trademark of Beckhoff Automation GmbH, Germany.
Note 2. This function is supported for security product only.

Table 1.9 Analog

Feature	Functional description
12-bit A/D converter (ADC12)	• 12 bits × 3 units (unit 0, 1: 4 channels, unit 2: 8 channels) • 12-bit resolution • Conversion time 0.84 µs per channel • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group priority control • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (3 channels: in all units) included • Sampling variable Sampling time can be set up for each channel • Double trigger mode (A/D conversion data duplicated) • Three ways to start A/D conversion Software trigger, timer (MTU3, ELC) trigger, external trigger • Event linking by the ELC
Temperature sensor unit (TSU)	• One channel • Relative precision: ±1°C (typ)

Table 1.10 Hardware accelerator for industrial interfaces

Feature	Functional description
ΔΣ interface (DSMIF)	• 3 channels × 5 units • Selectable 2 inputs (U/V) or 3 inputs (U/V/W) • Up to 6 ΔΣ modulators are externally connectable • Sinc filter can be selected as first, second or third order • Direct error connection to POE3 and POEG • Enhancement of current error detection • Core clock: 200 MHz
Trigonometric function unit (TFU)	• Two units • Calculation of sine, cosine, arctangent, hypot_k ($\sqrt{x^2+y^2}/k$) • Simultaneous calculation of sine and cosine • Simultaneous calculation of arctangent and hypot_k
Encoder interfaces	• EnDat 2.2 (8 units) • EnDat 3.0 (4 units) • BiSS-C (8 units) • BiSS-Line (4 units) • A-format (8 units) • HIPERFACE DSL (8 units) • ENCOUT (1 unit)

Table 1.11 Safety (1 of 2)

Feature	Functional description
Memory protection unit (MPU)	• Cortex-R52 MPU Two stages MPUs (EL2 and EL1) 24 regions each MPU • Master MPU Memory protection for masters including Cortex-A55 and Cortex-R52 (DMAC, USB, Ethernet MAC, Ethernet TSN switch, CoreSight, SHOSTIF, PHOSTIF, SDHI, PCIE, NANDC)
Register write protection function	Protects important registers from being overwritten for in case a program runs out of control.
CRC calculator (CRC)	• Two channels • CRC code generation for arbitrary amounts of data in 8-, 16-, or 32-bit units • Select any of five generating polynomials: – $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (32-Ethernet) – $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C) – $X^{16} + X^{15} + X^2 + 1$ (CRC-16) – $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT) – $X^8 + X^2 + X + 1$ (CRC-8)

Table 1.11 Safety (2 of 2)

Feature	Functional description
Clock monitor circuit (CLMA)	• Monitors the abnormal output clock frequency from the input clock (main clock oscillator), PLL circuit, or low-speed on-chip oscillator. • Input clock oscillation stop detection: Available
Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
Isolated peripherals	• Safety dedicated peripherals are available: – GPT: 4 ch – SCI: 1 ch – IIC: 1 ch – SPI: 1 ch – CRC: 1 unit – RTC: 1 unit – GPIO: Sharable with normal GPIO – On-chip system SRAM with ECC • They are mapped independently from normal peripherals so that access protection can be done by EL2 MPU.

Table 1.12 Security

Feature	Functional description
Security*1	• Secure boot • JTAG authentication*2 • SCI/USB boot authentication*2 • Cryptographic accelerators – Symmetric Cipher: AES 128/192/256 bits with CBC/ECB/CTR/GCM/XTS – Asymmetric Cipher: ECC 256 bits, RSA 1024/2048/3072 bits, RSAES-OAEP – Hash: SHA-1, SHA-2 – Message authentication: HMAC, CMAC, GMAC – Signature algorithms: ECDSA with NIST P-256, RSASSA-PSS, RSASSA-PKCS1 • TRNG • Cortex-A55 Crypto Extension • TrustZone

Note 1. For details, contact our sales representative.
Note 2. Authentication by plaintext is available in non-security support product.

Table 1.13 Debug

Feature	Functional description
Debugging interface	• CoreSight architecture designed by Arm • Debugging function by the JTAG/SWD interface, and trace function by ETF and system bus by ETR

Table 1.14 External host interface (1 of 2)

Feature	Functional description
Serial host interface (SHOSTIF)	• Serial communication is possible in slave mode. • Supported interface – Motorola Serial Peripheral Interface (4-wire SPI) – Enhanced SPI Modes with Dual, Quad, or Octal SPI • Serial clock polarity switching • Serial clock phase switching • Single Data Transfer • Data size is up to 32 bits × 64 burst
Parallel host interface (PHOSTIF)	• Synchronous/Asynchronous SRAM interface mode • Synchronous burst SRAM type transfer mode • Bus width: 8, 16 and 32 bits • Synchronous relations – HCKIO synchronous • Write buffer • Read buffer • Multiplexing of addresses and data (Synchronous burst SRAM type only)

Table 1.14 External host interface (2 of 2)

Feature	Functional description
Mailbox and semaphore (MBXSEM)	• Eight semaphores for external host CPU and Cortex-A55/Cortex-R52 • Four 32-bit mailboxes for both external host CPU to Cortex-A55/Cortex-R52 and Cortex-A55/Cortex-R52 to external host CPU • Interrupts can be generated and cleared from both external host CPU and Cortex-A55/Cortex-R52 • Semaphores and Mailboxes with exclusive access among Cortex-A55, Cortex-R52 CPU0 and CPU1.

Table 1.15 Others

Feature	Functional description
Power supply voltage	1.1 V: Core (Digital and Analog (PLL, TSU, OTP, USB, PCIE, ADC)) 1.1 V: DDR 1.8 V: PLL, OSC, USB, ADC, TSU, OTP, PCIE, DDR, RGMII 3.3 V: GPIO, USB, OSC, RMII/MII, other peripherals 1.8 V/3.3 V selectable: xSPI, SDHI
Operating temperature	Tj = −40 to +125°C
Packages	537 pins FBGA 21 × 21 mm, 0.8-mm pitch 489 pins FBGA 16 × 16 mm, 0.65-mm pitch

1.2 Function Comparison

Table 1.16 Function comparison (1 of 2)

Module/Function		537-pin FBGA	489-pin FBGA
CPU	ARM Cortex-A55	Dual/Single	
	ARM Cortex-R52	Dual	
Memory	System SRAM	2.0 MB	
External bus	External bus width	32 bits	16 bits
Interrupt	External interrupt	SEI, IRQ0 to IRQ15	
DMA	DMA controller (DMAC)	3 units (16 channels each unit)	
Timer	Multi-function timer pulse unit 3 (MTU3)	1 unit (9 channels)	
	General PWM timer (GPT)	6 units (31 channels)	
	Compare match timer (CMT)	3 units (6 channels)	
	Compare match timer W (CMTW)	2 channels	
	Watchdog timer	4 channels	
	Port output enable 3 (POE3)	1 unit	
	Port output enable for GPT (POEG)	3 units	
	Real time clock (RTC)	1 unit	
Communication function	Ethernet MAC (GMAC)	3 units	
	Ethernet switch (ETHSW)	1 unit (3 external ports)	
	EtherCAT slave controller (ESC)	1 unit (3 external ports)	
	Layer3 Ethernet switch module (ESWM)	1 unit (2 external ports)	
	HSR/PRP switch (HPSW)	1 unit (2 external ports)	
	USB 2.0 HS host/function module (USB)	1 unit (1 port)	
	Serial communication interface (SCI)	6 channels + 8 channels	
	I2C bus interface (IIC)	3 channels	
	CANFD module (CANFD)	2 channels	
	Serial peripheral interface (SPI)	4 channels	
	Expanded serial peripheral interface (xSPI)	2 channels	
	SD/eMMC Host interface (SDHI)	2 channels	
	PCI Express Gen2 (PCIE)	1 unit (1 lane × 1 port)	
	NAND Flash controller (NANDC)	1 unit	
12-bit A/D converter (ADC12)		3 units (4 channels for unit 0 and unit 1, 8 channels for unit 2)	
Temperature sensor unit (TSU)		1 unit	
ΔΣ interface (DSMIF)		5 units (15 channels)	5 units (13 channels)
Trigonometric function unit (TFU)		2 units	
Encoder I/F	EnDat 2.2 (ENDAT22)	8 units	
	EnDat 3.0 (ENDAT3)	4 units	
	BiSS-C (BISS)	8 units	
	BiSS-Line (BISSL)	4 units	
	A-format (AFMT)	8 units	
	Hiperface DSL (HDSL)	8 units	
	ENCOUT	1 unit	
CRC calculator (CRC)		2 channels	

Table 1.16 Function comparison (2 of 2)

Module/Function	537-pin FBGA	489-pin FBGA
Clock monitor circuit (CLMA)	7 units	
Data operation circuit (DOC)	1 unit	
Security*1	Optional	
One-time programmable memory (OTP)	Available	
Serial host interface (SHOSTIF)	1 unit	
Parallel host interface (PHOSTIF)	1 unit	
Mailbox and semaphore (MBXSEM)	Available	
Event link controller (ELC)	Available	
LPDDR4 SDRAM Subsystem (DDRSS)	16 bits	

Note 1. For details, contact our sales representative.

1.3 Product Lineup

Table 1.17 shows a product lineup.

Table 1.17 Product lineup

Part Number	Package	Cortex-A55	EtherCAT	HSR/PRP switch	CAN	Security*1
R9A07G076M48GBG	537-pin FBGA	Dual cores	Available	Available	CAN-FD	Available
R9A07G076M47GBG	537-pin FBGA	Dual cores	Available	Not available	CAN-FD	Available
R9A07G076M45GBG	537-pin FBGA	Dual cores	Not available	Not available	Classical CAN	Available
R9A07G076M43GBG	537-pin FBGA	Dual cores	Available	Available	CAN-FD	Not available
R9A07G076M37GBG	537-pin FBGA	Single core	Available	Not available	CAN-FD	Available
R9A07G076M35GBG	537-pin FBGA	Single core	Not available	Not available	Classical CAN	Available
R9A07G076M30GBG	537-pin FBGA	Single core	Not available	Not available	Classical CAN	Not available
R9A07G076M48GBA	489-pin FBGA	Dual cores	Available	Available	CAN-FD	Available
R9A07G076M47GBA	489-pin FBGA	Dual cores	Available	Not available	CAN-FD	Available
R9A07G076M45GBA	489-pin FBGA	Dual cores	Not available	Not available	Classical CAN	Available
R9A07G076M43GBA	489-pin FBGA	Dual cores	Available	Available	CAN-FD	Not available
R9A07G076M37GBA	489-pin FBGA	Single core	Available	Not available	CAN-FD	Available
R9A07G076M35GBA	489-pin FBGA	Single core	Not available	Not available	Classical CAN	Available
R9A07G076M30GBA	489-pin FBGA	Single core	Not available	Not available	Classical CAN	Not available

Note 1. Except for TrustZone. TrustZone is available for all part number.

1.4 Block Diagram

Figure 1.1 shows a block diagram.

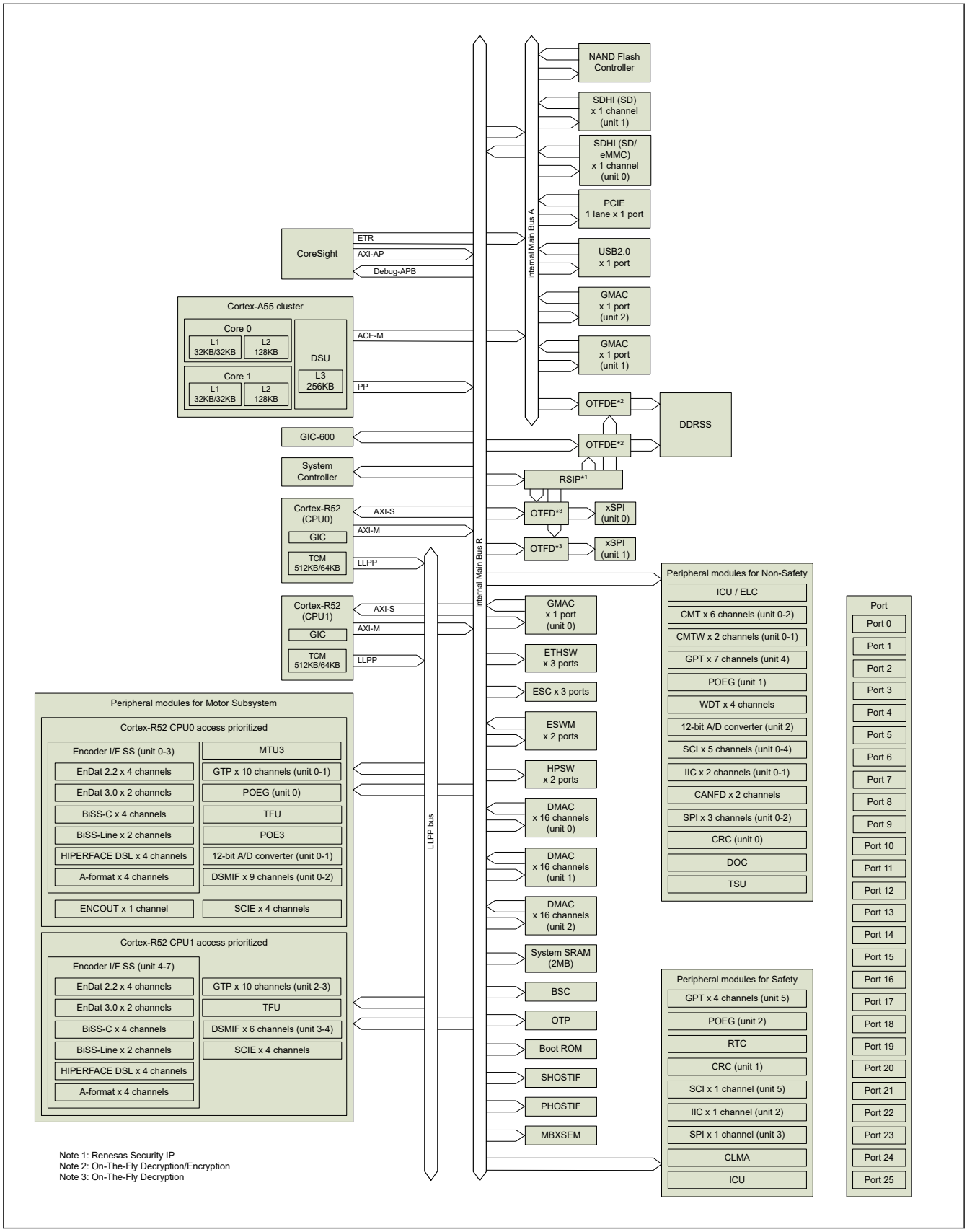


Figure 1.1 Block diagram

Abbreviations denoted in Figure 1.1 are listed in the following table.

1.5 Pin Functions

Table 1.18 lists the pin functions.

Table 1.18 Pin functions (1 of 9)

Classification	Pin name	I/O	Description
Power supply	VDD	Input	1.1 V power supply pin
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
	VCC1833_0 to VCC1833_6	Input	Power supply pins for each I/O domains. (1.8 V or 3.3 V) VCC1833_0: ETH0 and ETH1 domain VCC1833_1: ETH2 domain VCC1833_2: ETH3 and ETH4 domain VCC1833_3: xSPI0 domain VCC1833_4: xSPI1 domain VCC1833_5: SDHI0 domain VCC1833_6: SDHI1 domain
	VCC33	Input	3.3 V power supply pins for I/O
	VCC18_PLL0 to VCC18_PLL4	Input	1.8 V power supply pins for PLL
	AVCC18_TSU	Input	1.8 V power supply pin for Thermal sensor
	VCC18_OTP	Input	1.8 V power supply pin for OTP
Adaptive body bias generator (ABBG)	VDD18ABG	Input	ABBG power supply pin
	NCPOUT	I/O	Analog in-output pin
Clock	XTAL	Output	Connected to a crystal resonator. When external clock signal is used, EXTAL pin should be driven low. XTAL pin should never be driven or loaded by anything other than crystal oscillator. The voltage level of EXTAL must not exceed VDD (1.16V).
	EXTAL	Input	
	EXTCLKIN	Input	Inputs the external clock. When a crystal resonator is connected, it should be driven low.
	CKIO	Output	Outputs the external bus clock for external devices.
	ETH0_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 0
	ETH1_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 1
	ETH2_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 2
	ETH3_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 3
	ETH4_REFCLK	Output	Outputs 25 MHz clock for EtherPHY 4
	RMII0_REFCLK	Output	Outputs 50 MHz clock for RMII0
	RMII1_REFCLK	Output	Outputs 50 MHz clock for RMII1
	RMII2_REFCLK	Output	Outputs 50 MHz clock for RMII2
	RMII3_REFCLK	Output	Outputs 50 MHz clock for RMII3
	RMII4_REFCLK	Output	Outputs 50 MHz clock for RMII4

Table 1.18 Pin functions (2 of 9)

Classification	Pin name	I/O	Description
Operating mode control	MDX	Input	This signal should be driven low.
	MD0 to MD2	Input	Input the operating mode select signal. The signal level on these pins must not be changed during operation mode transition on release from the reset state.
	MDV0 to MDV5	Input	Input the operating voltage select signal. The signal level on these pins must not be changed during operation mode transition on release from the reset state.
	MDW0, MDW1	Input	Input the ATCM wait cycle select signal. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
	MDD	Input	Input the enabling JTAG authentication by hash signal. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
	MDB	Input	Pin for setting the 2nd boot CPU. This signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES#	Input	Inputs the reset signal. This MPU enters the reset state when this signal goes low.
	BSCANP	Input	Inputs the boundary scan enable signal. Boundary scan is enabled when this pin goes high. When boundary scan is not used, this pin should be driven low.
	RSTOUT#	Output	Outputs the reset signal externally
Debugging interface	TRST#	Input	Test reset pin for the on-chip emulator
	TMS	I/O	Test mode select pin for the on-chip emulator Functions as the SWDIO pin in serial wire debug (SWD) mode
	TDI	Input	Test data input pin for the on-chip emulator
	TDO	Output	Test data output pin for the on-chip emulator
	TCK	Input	Test clock pin for the on-chip emulator Functions as the SWCLK pin in serial wire debug (SWD) mode

Table 1.18 Pin functions (3 of 9)

Classification	Pin name	I/O	Description
Bus state controller (BSC)	A25 to A0	Output	Output the address
	D31 to D0	I/O	Input and output the data
	CS0#, CS2#, CS3#, CS5#	Output	Output the chip select signal for the external memory or device.
	RD#	Output	Outputs the strobe signal which indicates a read is in progress.
	RD/WR#	Output	Outputs the strobe signal which indicates a read or write access
	BS#	Output	Outputs the status signal which indicates the start of the bus cycle
	AH#	Output	Outputs the address hold signal for the device that uses the multiplexed I/O interface
	WAIT#	Input	Inputs the external wait control signal which inserts a wait cycle into the bus cycle
	WE0#	Output	Outputs the write strobe signal to D7 to D0
	WE1#	Output	Outputs the write strobe signal to D15 to D8
	WE2#	Output	Outputs the write strobe signal to D23 to D16
	WE3#	Output	Outputs the write strobe signal to D31 to D24
Direct memory access controller (DMAC)	DREQ	Input	Inputs the DMA transfer request signal from the external device
	DACK	Output	Outputs the acknowledge signal which indicates acceptance of the DMA transfer request from the external device
	TEND	Output	Outputs the DMA transfer end signal
Interrupt	IRQ00_0 to IRQ25_0	Input	Input the system error interrupt signal and the external interrupt request signal
Multi-function timer pulse unit 3 (MTU3)	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	TGRA0 to TGRD0 input capture input, output compare output, and PWM output pins
	MTIOC1A, MTIOC1B	I/O	TGRA1 and TGRB1 input capture input, output compare output, and PWM output pins
	MTIOC2A, MTIOC2B	I/O	TGRA2 and TGRB2 input capture input, output compare output, and PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	TGRA3 to TGRD3 input capture input, output compare output, and PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	TGRA4 to TGRD4 input capture input, output compare output, and PWM output pins
	MTIC5U, MTIC5V, MTIC5W	Input	TGRU5, TGRV5, and TGRW5 input capture input and dead time compensation input pins
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	External clock input pins for MTU3
Port output enable 3 (POE3)	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input the request signal to place the MTU3 in the high-impedance state

Table 1.18 Pin functions (4 of 9)

Classification	Pin name	I/O	Description
General PWM timer (GPT)/ Port output enable for GPT (POEG)	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input and output-disable request input pins
	GTETRGSA, GTETRGSB	Input	External trigger input and output-disable request input pins (SAFETY)
	GTIOC0_0A to GTIOC0_4A, GTIOC0_0B to GTIOC0_4B, GTIOC1_0A to GTIOC1_4A, GTIOC1_0B to GTIOC1_4B, GTIOC2_0A to GTIOC2_4A, GTIOC2_0B to GTIOC2_4B, GTIOC3_0A to GTIOC3_4A, GTIOC3_0B to GTIOC3_4B, GTIOC4_0A to GTIOC4_6A, GTIOC4_0B to GTIOC4_6B, GTIOC5_0A to GTIOC5_3A, GTIOC5_0B to GTIOC5_3B	I/O	Input capture input/output compare output/PWM output pins
	GTADSM0_0 to GTADSM0_1, GTADSM1_0 to GTADSM1_1, GTADSM2_0 to GTADSM2_1, GTADSM3_0 to GTADSM3_1, GTADSM4_0 to GTADSM4_1,	Output	Output pins for monitoring A/D conversion start requests
Compare match timer W (CMTW)	CMTW0_TIC0, CMTW0_TIC1, CMTW1_TIC0, CMTW1_TIC1	Input	CMTW input capture input pins
	CMTW0_TOC0, CMTW0_TOC1, CMTW1_TOC0, CMTW1_TOC1	Output	CMTW output compare output pins
Real time clock (RTC)	RTCAT1HZ	Output	RTC 1 Hz output pin
Serial communication interface (SCI)	SCK0 to SCK5	I/O	Clock I/O pins (clock synchronous mode/simple SPI mode/smart card mode)
	RXD0 to RXD5	Input	Input the receive data (asynchronous mode/clock synchronous mode/smart card mode)
	TXD0 to TXD5	Output	Output the transmit data (asynchronous mode/clock synchronous mode/smart card mode)
	CTS0# to CTS5#	Input	Input the start of transmission (asynchronous mode/ clock synchronous mode) active-low
	RTS0# to RTS5#	Output	Output the reception (asynchronous mode/clock synchronous mode) active-low
	SCL0 to SCL5	I/O	Input/output the I2C clocks (simple I2C mode)
	SDA0 to SDA5	I/O	Input/output the I2C data (simple I2C mode)
	MISO0 to MISO5	I/O	Input/output the data for slave transmission (simple SPI mode)
	MOSI0 to MOSI5	I/O	Input/output the data for master transmission (simple SPI mode)
	SS0# to SS5#	Input	Chip-select input pins (simple SPI mode) active-low
	DE0 to DE5	Output	Driver enable output pins (asynchronous mode)
Serial communication interface for Encoder (SCIE)	SCKE0 to SCKE7	Output	Clock I/O pins (clock synchronous mode)
	RXDE0 to RXDE7	Input	Input the receive data (asynchronous mode/clock synchronous mode)
	TXDE0 to TXDE7	Output	Output the transmit data (asynchronous mode/clock synchronous mode)
	DEE0 to DEE7	Output	Driver enable output pins (asynchronous mode)
SCI and SCIE common	SCIEXTCLK	Input	SCI external operation clock input pin

Table 1.18 Pin functions (5 of 9)

Classification	Pin name	I/O	Description
I^2C bus interface (IIC)	IIC_SCL0 to IIC_SCL2	I/O	Clock I/O pins
	IIC_SDA0 to IIC_SDA2	I/O	Data I/O pins
Ethernet	ETH0_TXCLK to ETH4_TXCLK	I/O	TX clock input pins (MII mode) TX clock output pins (RGMII mode)
	ETH0_TXD0 to ETH4_TXD0	Output	TX data 0 pins (RGMII, RMII, and MII modes)
	ETH0_TXD1 to ETH4_TXD1	Output	TX data 1 pins (RGMII, RMII, and MII modes)
	ETH0_TXD2 to ETH4_TXD2	Output	TX data 2 pins (RGMII and MII modes)
	ETH0_TXD3 to ETH4_TXD3	Output	TX data 3 pins (RGMII and MII modes)
	ETH0_TXEN to ETH4_TXEN	Output	TX data enable pins (RMII and MII modes) TX data enable/TX data error (TX_CTL) pins (RGMII mode)
	ETH0_TXER to ETH4_TXER	Output	TX data error pins (MII mode)
	ETH0_RXCLK to ETH4_RXCLK	Input	RX clock pins (RGMII, RMII, and MII modes)
	ETH0_RXD0 to ETH4_RXD0	Input	RX data 0 pins (RGMII, RMII, and MII modes)
	ETH0_RXD1 to ETH4_RXD1	Input	RX data 1 pins (RGMII, RMII, and MII modes)
	ETH0_RXD2 to ETH4_RXD2	Input	RX data 2 pins (RGMII and MII modes)
	ETH0_RXD3 to ETH4_RXD3	Input	RX data 3 pins (RGMII and MII modes)
	ETH0_RXDV to ETH4_RXDV	Input	RX data valid pins (MII mode) Carrier sense/RX data valid (CRS_DV) pins (RMII mode) RX data valid/RX error (RX_CTL) pins (RGMII mode)
	ETH0_RXER to ETH4_RXER	Input	RX data error pins (RMII and MII modes)
	ETH0_CRS to ETH4_CRS	Input	Carrier sense pins (MII mode)
	ETH0_COL to ETH4_COL	Input	Collision detection pins (MII mode)
Ethernet MAC (GMAC)	GMAC0_PTPTRG0 to GMAC2_PTPTRG0	Input	PTP timer trigger external input 0
	GMAC0_PTPTRG1 to GMAC2_PTPTRG1	Input	PTP timer trigger external input 1
	GMAC0_MDC to GMAC2_MDC	Output	Management data clock output pin
	GMAC0_MDIO to GMAC2_MDIO	I/O	Management data I/O pin
Ethernet switch (ETHSW)	ETHSW_LPI0	Output	Port 0 MAC status indicates that it is currently receiving low-power-idle sequences from the PHY
	ETHSW_LPI1	Output	Port 1 MAC status indicates that it is currently receiving low-power-idle sequences from the PHY
	ETHSW_LPI2	Output	Port 2 MAC status indicates that it is currently receiving low-power-idle sequences from the PHY
	ETHSW_PTPOUT0 to ETHSW_PTPOUT3	Output	Ethernet switch timer pulse output pins
	ETHSW_TDMAOUT0 to ETHSW_TDMAOUT3	Output	Ethernet switch TDMA timer output pins
	ETHSW_PHYLINK0 to ETHSW_PHYLINK2	Input	Ethernet switch PHY link status input pins
	ETHSW_MDC	Output	Management data clock output pin
	ETHSW_MDIO	I/O	Management data I/O pin

Table 1.18 Pin functions (6 of 9)

Classification	Pin name	I/O	Description
EtherCAT slave controller (ESC)	ESC_LEDRUN	Output	Outputs the EtherCAT RUN LED signal
	ESC_IRQ	Output	Outputs the EtherCAT IRQ signal
	ESC_LEDSTER	Output	Outputs the EtherCAT Dual-color state LED signal
	ESC_LEDERR	Output	Outputs the EtherCAT error LED signal
	ESC_LINKACT0 to ESC_LINKACT2	Output	Output the EtherCAT link/activity LED signal
	ESC_SYNC0, ESC_SYNC1	Output	Output the EtherCAT SYNC signal
	ESC_LATCH0, ESC_LATCH1	Input	Input the EtherCAT LATCH signal
	ESC_RESETOUT#	Output	Output the EtherCAT reset signal
	ESC_I2CCLK	Output	Outputs the EtherCAT EEPROM I2C clock signal
	ESC_I2CDATA	I/O	Inputs and outputs the EtherCAT EEPROM I2C data signal
	ESC_PHYLINK0 to ESC_PHYLINK2	Input	Inputs the EtherCAT PHY link status signal.
	ESC_MDC	Output	Management data clock output pin
	ESC_MDIO	I/O	Management data I/O pin
Layer3 Ethernet switch module (ESWM)	ESWM_MPINT0, ESWM_MPINT1	Output	Magic Packet interrupt output
	ESWM_PHYLINK0, ESWM_PHYLINK1	Input	TSN switch PHY link status input
	ESWM_MDC	Output	Management data clock output pin
	ESWM_MDIO	I/O	Management data I/O pin
	ESWM_TASGATE0[8:0], ESWM_TASGATE1[8:0]	Output	TAS gate status debug output
HSR/PRP switch (HPSW)	HPSW_PHYLINK0	Input	HSR/PRP switch PHY link status input port 0
	HPSW_PHYLINK1	Input	HSR/PRP switch PHY link status input port 1
USB 2.0 host/function module	VCC33_USB	Input	Power supply input pin for USB
	VCC18_USB	Input	Power supply input pin for USB
	VSS_USB	Input	Ground input pins for USB
	AVCC18_USB	Input	Analog power supply input pin for USB
	USB_RREF	Input	Reference current input pin for USB. Connect this pin to the VSS_USB pin with 1.8 kΩ (±1%).
	USB_DP	I/O	USB bus D+ data I/O pin
	USB_DM	I/O	USB bus D- data I/O pin
	USB_VBUSEN	Output	Outputs the VBUS power enable signal for USB
	USB_OVRCUR	Input	Inputs the overcurrent signal for USB
	USB_VBUSIN	Input	USB cable connection/disconnection detection input pin
	USB_EXICEN	Output	OTG power supply IC control pin
	USB_OTGID	Input	OTG ID pin
CANFD module (CANFD)	CANRX0, CANRX1	Input	Receive data input pins
	CANTX0, CANTX1	Output	Transmit data output pins
	CANRXDP0, CANRXDP1	Output	Receive data phase output pins
	CANTXDP0, CANTXDP1	Output	Transmit data phase output pins

Table 1.18 Pin functions (7 of 9)

Classification	Pin name	I/O	Description
Serial peripheral interface (SPI)	SPI_RSPCK0 to SPI_RSPCK3	I/O	Clock I/O pins
	SPI_MOSI0 to SPI_MOSI3	I/O	Master transmit data I/O pins
	SPI_MISO0 to SPI_MISO3	I/O	Slave transmit data I/O pins
	SPI_SSL00 to SPI_SSL30	I/O	Slave select signal I/O pins
	SPI_SSL01 to SPI_SSL31, SPI_SSL02 to SPI_SSL32, SPI_SSL03 to SPI_SSL33	Output	Slave select signal output pins
Expanded serial peripheral interface (xSPI)	XSPI0_CKP, XSPI1_CKP, XSPI0_CKN	Output	Clock output pins
	XSPI0_CS0#, XSPI0_CS1#, XSPI1_CS0#, XSPI1_CS1#	Output	Chip select output pins
	XSPI0_DS, XSPI1_DS	I/O	Read data strobe/write data mask input/output pin
	XSPI0_IO0 to XSPI0_IO7, XSPI1_IO0 to XSPI1_IO7	I/O	Data0 to Data7 input/output pins
	XSPI0_RESET0#	Output	Master reset status output pins
ΔΣ interface (DSMIF)	MCLK00 to MCLK40, MCLK01 to MCLK41, MCLK02 to MCLK42	I/O	Clock I/O pins
	MDAT00 to MDAT40, MDAT01 to MDAT41, MDAT02 to MDAT42	Input	Data input pins
12-bit A/D converter (ADC12)	AN000 to AN003, AN100 to AN103, AN200 to AN207	Input	Analog input pins for the A/D converter
	ADTRG0# to ADTRG2#	Input	External trigger input pins for the start of A/D conversion
Analog power supply	VCC18_ADC0 to VCC18_ADC2	Input	Analog power supply input pin for the 12-bit A/D converter. Connect this pin to the 1.8 V power supply if the 12-bit A/D converter is not to be used.
	VREFH0 to VREFH2	Input	Reference voltage input pin for the 12-bit A/D converter. Connect this pin to the 1.8 V power supply if the 12-bit A/D converter is not to be used.
Serial host interface (SHOSTIF)	HSPI_CK	Input	Clock input pin
	HSPI_CS#	Input	Chip select input pin
	HSPI_IO0 to HSPI_IO7	I/O	Data0 to Data7 input/output pins
	HSPI_INT#	Output	Interrupt output pin

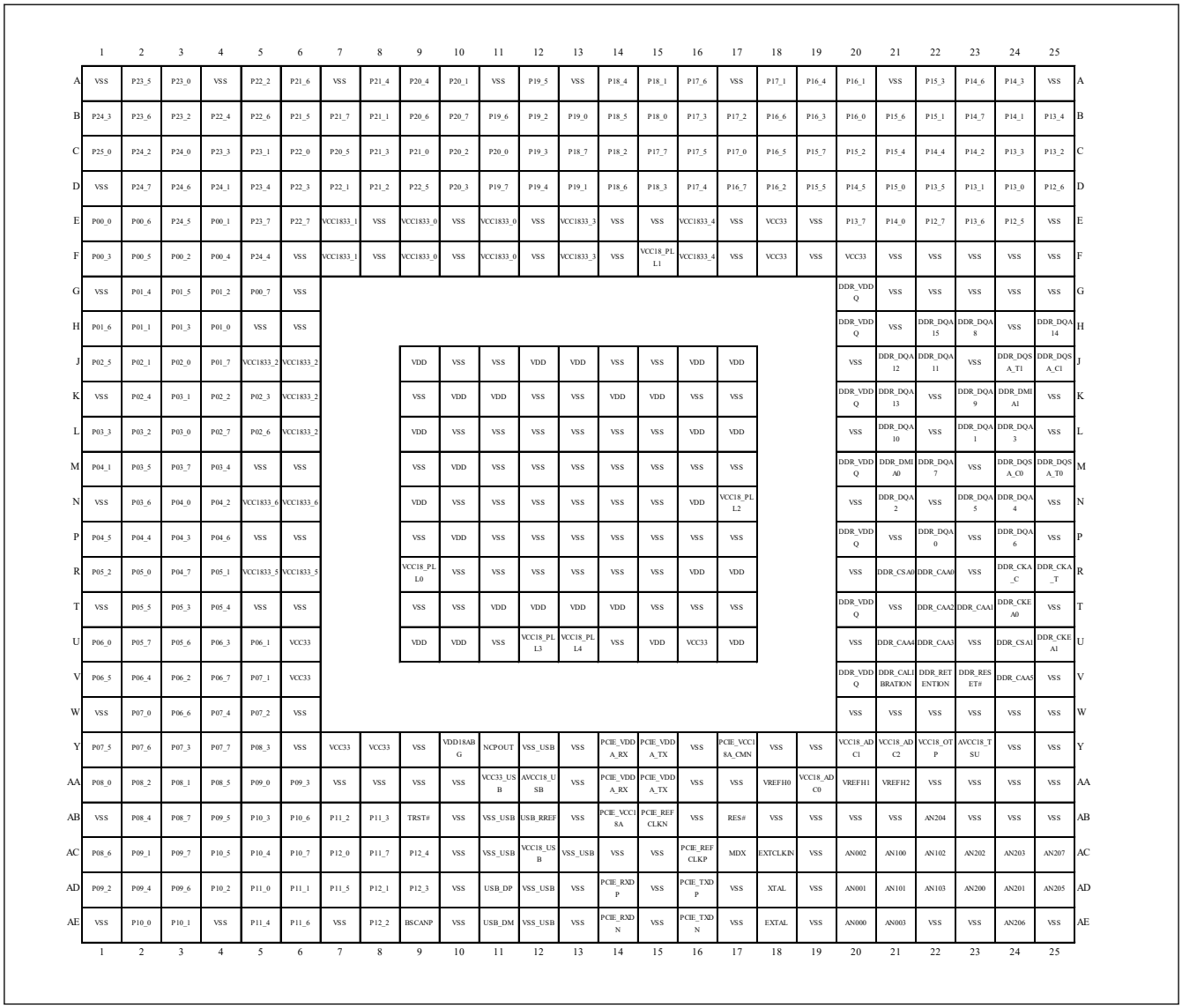
Table 1.18 Pin functions (8 of 9)

Classification	Pin name	I/O	Description
Parallel host interface (PHOSTIF)	HCKIO	Input	Bus clock input pin
	HA0 to HA21	Input	Address input pins
	HD0 to HD31	I/O	Data I/O pins
	HCS0#	Input	Chip select input pin supporting burst transfer
	HCS1#	Input	Chip select input pin supporting BSC ADMUX mode
	HRD#	Input	Strobe input pin indicating a read access
	HWAIT#	Output	Output pin indicating that the bus cycle is in wait state
	HWRSTB#	Input	Strobe input pin indicating a write access
	HWR0#	Input	Write strobe/byte enable input pin to HD7 to HD0
	HWR1#	Input	Write strobe/byte enable input pin to HD15 to HD8
	HWR2#	Input	Write strobe/byte enable input pin to HD23 to HD16
	HWR3#	Input	Write strobe/byte enable input pin to HD31 to HD24
	HERROUT#	Output	Outputs the bus access error interrupt signal
	HBS#	Input	Bus cycle input pin
Mailbox and Semaphore (MBXSEM)	MBX_HINT#	Output	Mailbox (Cortex-A55/Cortex-R52 to Host CPU) interrupt output pin
Encoder I/F common	ENCIFCK0 to ENCIFCK7	Output	Encoder I/F clock output pins
	ENCIFOE0 to ENCIFOE7	Output	Encoder I/F data output enable pins
	ENCIFDO0 to ENCIFDO7	Output	Encoder I/F data output pins
	ENCIFDI0 to ENCIFDI7	Input	Encoder I/F data input pins
EnDat 2.2 (ENDAT)	DUEI0 to DUEI7	Output	EnDat 2.2 Data transfer
	TST_OUT0 to TSTOUT7	Output	EnDat 2.2 Data input after internal synchronization
	SI0# to SI7#	Output	EnDat 2.2 Start pulse
Hiperface DSL (HDSL)	HDSL0_LINK to HDSL7_LINK	Output	HDSL LINK
	HDSL0_SMPL to HDSL7_SMPL	Output	HDSL Test signal line sampler
	HDSL0_CLK1 to HDSL7_CLK1	Input	HDSL SPI clock safe 1
	HDSL0_SEL1 to HDSL7_SEL1	Input	HDSL SPI selection safe 1
	HDSL0_MISO1 to HDSL7_MISO1	Output	HDSL SPI data output safe 1
	HDSL0_MOSI1 to HDSL7_MOSI1	Input	HDSL SPI data input safe 1
	HDSL0_CLK2 to HDSL7_CLK2	Input	HDSL SPI clock safe 2
	HDSL0_SEL2 to HDSL7_SEL2	Input	HDSL SPI selection safe 2
	HDSL0_MISO2 to HDSL7_MISO2	Output	HDSL SPI data output safe 2
	HDSL0_MOSI2 to HDSL7_MOSI2	Input	HDSL SPI data input safe 2
ENCOUT	POUTA	Output	ENCOUT A-phase output pin
	POUTB	Output	ENCOUT B-phase output pin
	POUTZ	Output	ENCOUT Z-phase output pin

Table 1.18 Pin functions (9 of 9)

Classification	Pin name	I/O	Description
SD/eMMC Host Interface (SDHI)	SD0_CLK, SD1_CLK	Output	SD/MMC clock output
	SD0_CMD, SD1_CMD	I/O	SD/MMC command output, response input
	SD0_DATA0 to SD0_DATA7, SD1_DATA0 to SD1_DATA3	I/O	SD/MMC Data
	SD0_CD, SD1_CD	Input	SD card detection
	SD0_WP, SD1_WP	Input	SD write protection
	SD0_RST#	Output	MMC reset
	SD0_PWEN, SD1_PWEN	Output	SD power enable
	SD0_IOVS, SD1_IOVS	Output	SD voltage select
PCI Express Gen2 (PCIE)	PCIE_VCC18A, PCIE_VCC18A_CMN	Input	1.8 V power supply pins for PCIE
	PCIE_VDDA_TX, PCIE_VDDA_RX	Input	1.1 V power supply pins for PCIE
	PCIE_REFCLKP, PCIE_REFCLKN	Input	Reference clock input
	PCIE_RXDP, PCIE_RXDN	Input	Serial data input
	PCIE_TXDP, PCIE_TXDN	Output	Serial data output
	PCIE_RSTOUTB	Output	PCIE Reset output for Root Complex
NAND Flash controller (NAND)	NAND_CE[3:0]#	Output	Chip enable, active low
	NAND_IO[7:0]	I/O	Data
	NAND_CLE	Output	Command latch enable
	NAND_ALE	Output	Address latch enable
	NAND_RE#	Output	Read enable, active low
	NAND_WE#	Output	Write enable, active low
	NAND_WP#	Output	Write protect/reset
	NAND_RY_BY[3:0]#	Input	Ready/Busy (RnB), Ready=High, Busy=Low
LPDDR4 SDRAM Subsystem (DDRSS)	DDR_VDDQ	Input	1.1 V power supply pin for DDRPHY
	DDR_RESET#	Output	DDRSS DRAM reset
	DDR_CKA_T, DDR_CKA_C	I/O	DDRSS DRAM ch A clock
	DDR_CKEA[1:0]	I/O	DDRSS DRAM ch A clock enable
	DDR_CSA[1:0]	I/O	DDRSS DRAM ch A chip select
	DDR_CAA[5:0]	I/O	DDRSS DRAM ch A command/address
	DDR_DQA[15:0]	I/O	DDRSS DRAM ch A data
	DDR_DMIA[1:0]	I/O	DDRSS DRAM ch A data mask inversion
	DDR_DQSA_T[1:0]	I/O	DDRSS DRAM ch A data strobe (positive)
	DDR_DQSA_C[1:0]	I/O	DDRSS DRAM ch A data strobe (negative)
	DDR_CALIBRATION	Input	Impedance Calibration Connect this pin to the DDR_VDDQ with 240 Ω (±1%).
	DDR_RETENTION	Input	Retention input Since retention mode is not supported in this LSI, the pin should be connected to DDR_VDDQ (No need to insert a pull-up resister).
I/O ports	P00_0 to P25_0	I/O	General-purpose input/output pins

1.6 FBGA 537 Pin Assignment



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A	VSS	P23_5	P23_0	VSS	P22_2	P21_6	VSS	P21_4	P20_4	P20_1	VSS	P19_5	VSS	P18_4	P18_1	P17_6	VSS	P17_1	P16_4	P16_1	VSS	P15_3	P14_6	P14_3	VSS	A
B	P24_3	P23_6	P23_2	P22_4	P22_6	P21_5	P21_7	P21_1	P20_6	P20_7	P19_6	P19_2	P19_0	P18_5	P18_0	P17_3	P17_2	P16_6	P16_3	P16_0	P15_6	P15_1	P14_7	P14_1	P13_4	B
C	P25_0	P24_2	P24_0	P23_3	P23_1	P22_0	P20_5	P21_3	P21_0	P20_2	P20_0	P19_3	P18_7	P18_2	P17_7	P17_5	P17_0	P16_5	P15_7	P15_2	P15_4	P14_4	P14_2	P13_3	P13_2	C
D	VSS	P24_7	P24_6	P24_1	P23_4	P22_3	P22_1	P21_2	P22_5	P20_3	P19_7	P19_4	P19_1	P18_6	P18_3	P17_4	P16_7	P16_2	P15_5	P14_5	P15_0	P13_5	P13_1	P13_0	P12_6	D
E	P00_0	P00_6	P24_5	P00_1	P23_7	P22_7	VCC1833_1	VSS	VCC1833_0	VSS	VCC1833_0	VSS	VCC1833_3	VSS	VSS	VCC1833_4	VSS	VCC33	VSS	P13_7	P14_0	P12_7	P13_6	P12_5	VSS	E
F	P00_3	P00_5	P00_2	P00_4	P24_4	VSS	VCC1833_1	VSS	VCC1833_0	VSS	VCC1833_0	VSS	VCC1833_3	VSS	VCC18_PLL1	VCC1833_4	VSS	VCC33	VSS	VCC33	VSS	VSS	VSS	VSS	VSS	F
G	VSS	P01_4	P01_5	P01_2	P00_7	VSS														DDR_VDDQ	VSS	VSS	VSS	VSS	VSS	G
H	P01_6	P01_1	P01_3	P01_0	VSS	VSS														DDR_VDDQ	VSS	DDR_DQA15	DDR_DQA8	VSS	DDR_DQA14	H
J	P02_5	P02_1	P02_0	P01_7	VCC1833_2	VCC1833_2			VDD	VSS	VSS	VDD	VDD	VSS	VSS	VDD	VDD			VSS	DDR_DQA12	DDR_DQA11	VSS	DDR_DQSA_T1	DDR_DQSA_C1	J
K	VSS	P02_4	P03_1	P02_2	P02_3	VCC1833_2			VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS			DDR_VDDQ	DDR_DQA13	VSS	DDR_DQA9	DDR_DMIA1	VSS	K
L	P03_3	P03_2	P03_0	P02_7	P02_6	VCC1833_2			VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDD			VSS	DDR_DQA10	VSS	DDR_DQA1	DDR_DQA3	VSS	L
M	P04_1	P03_5	P03_7	P03_4	VSS	VSS			VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS			DDR_VDDQ	DDR_DMIA0	DDR_DQA7	VSS	DDR_DQSA_C0	DDR_DQSA_T0	M
N	VSS	P03_6	P04_0	P04_2	VCC1833_6	VCC1833_6			VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VCC18_PLL2			VSS	DDR_DQA2	VSS	DDR_DQA5	DDR_DQA4	VSS	N
P	P04_5	P04_4	P04_3	P04_6	VSS	VSS			VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS			DDR_VDDQ	VSS	DDR_DQA0	VSS	DDR_DQA6	VSS	P
R	P05_2	P05_0	P04_7	P05_1	VCC1833_5	VCC1833_5			VCC18_PLL0	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDD			VSS	DDR_CSA0	DDR_CAA0	VSS	DDR_CKA_C	DDR_CKA_T	R
T	VSS	P05_5	P05_3	P05_4	VSS	VSS			VSS	VSS	VDD	VDD	VDD	VDD	VSS	VSS	VSS			DDR_VDDQ	VSS	DDR_CAA2	DDR_CAA1	DDR_CKEA0	VSS	T
U	P06_0	P05_7	P05_6	P06_3	P06_1	VCC33			VDD	VDD	VSS	VCC18_PLL3	VCC18_PLL4	VSS	VDD	VCC33	VDD			VSS	DDR_CAA4	DDR_CAA3	VSS	DDR_CSA1	DDR_CKEA1	U
V	P06_5	P06_4	P06_2	P06_7	P07_1	VCC33														DDR_VDDQ	DDR_CALIBRATION	DDR_RETENTION	DDR_RESET#	DDR_CAA5	VSS	V
W	VSS	P07_0	P06_6	P07_4	P07_2	VSS														VSS	VSS	VSS	VSS	VSS	VSS	W
Y	P07_5	P07_6	P07_3	P07_7	P08_3	VSS	VCC33	VCC33	VSS	VDD18AHG	NCPOUT	VSS_USB	VSS	PCIE_VDDA_RX	PCIE_VDDA_TX	VSS	PCIE_VCC18A_CMN	VSS	VSS	VCC18_ADC1	VCC18_ADC2	VCC18_OTP	AVCC18_TSU	VSS	VSS	Y
AA	P08_0	P08_2	P08_1	P08_5	P09_0	P09_3	VSS	VSS	VSS	VSS	VCC33_USB	AVCC18_USB	VSS	PCIE_VDDA_RX	PCIE_VDDA_TX	VSS	VSS	VREFH0	VCC18_ADC0	VREFH1	VREFH2	VSS	VSS	VSS	VSS	AA
AB	VSS	P08_4	P08_7	P09_5	P10_3	P10_6	P11_2	P11_3	TRST#	VSS	VSS_USB	USB_RREF	VSS	PCIE_VCC18A	PCIE_REFCLKN	VSS	RES#	VSS	VSS	VSS	VSS	AN204	VSS	VSS	VSS	AB
AC	P08_6	P09_1	P09_7	P10_5	P10_4	P10_7	P12_0	P11_7	P12_4	VSS	VSS_USB	VCC18_USB	VSS_USB	VSS	VSS	PCIE_REFCLKP	MDX	EXTCLKIN	VSS	AN002	AN100	AN102	AN202	AN203	AN207	AC
AD	P09_2	P09_4	P09_6	P10_2	P11_0	P11_1	P11_5	P12_1	P12_3	VSS	USB_DP	VSS_USB	VSS	PCIE_RXDP	VSS	PCIE_TXDP	VSS	XTAL	VSS	AN001	AN101	AN103	AN200	AN201	AN205	AD
AE	VSS	P10_0	P10_1	VSS	P11_4	P11_6	VSS	P12_2	BSCANP	VSS	USB_DM	VSS_USB	VSS	PCIE_RXDN	VSS	PCIE_TXDN	VSS	EXTAL	VSS	AN000	AN003	VSS	VSS	AN206	VSS	AE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

Figure 1.2 Pin arrangement (537-pin FBGA) (top view)

Table 1.19 List of pins and pin functions (537-pin FBGA) (1 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
A1	—	VSS	—	—	—	—	—	—	—	—
A2	VCC1833_1	IRQ23_5	P23_5	—	GTIOC4_2B	DE3 / ETH2_TXEN / ESC_LEDERR / SPI_SSL02	MCLK30 / MCLK42	—	—	HDSL7_MOSI1
A3	VCC1833_1	IRQ23_0	P23_0	—	GTIOC3_3A / GTIOC4_0A	RXD3/SCL3/MISO3 / ETH2_TXCLK / SPI_RSPCK0	MDAT01	—	—	HDSL7_LINK
A4	—	VSS	—	—	—	—	—	—	—	—
A5	VCC1833_0	IRQ22_2	P22_2	—	GTIOC0_3A / GTIOC4_5B / GTIOC5_0B	ETH1_RXD2	—	—	—	HDSL6_MISO1
A6	VCC1833_0	IRQ21_6	P21_6	—	—	ETH1_TXEN	—	—	—	HDSL6_LINK
A7	—	VSS	—	—	—	—	—	—	—	—
A8	VCC1833_0	IRQ21_4	P21_4	—	—	ETH1_TXD2	—	—	—	HDSL5_MISO2

Table 1.19 List of pins and pin functions (537-pin FBGA) (2 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
A9	VCC1833_0	MD0 / IRQ20_4	P20_4	—	—	GMAC0_MDC / GMAC1_MDC / GMAC2_MDC / ETHSW_MDC / ESC_MDC / ESWM_MDC / CANTX1	—	—	—	—
A10	VCC1833_0	IRQ20_1	P20_1	—	—	ETH0_RXD2 / CANRXDP0	—	—	—	HDSL4_MISO2
A11	—	VSS	—	—	—	—	—	—	—	—
A12	VCC1833_0	IRQ19_5	P19_5	—	—	ETH0_TXEN	—	—	—	HDSL4_MISO1
A13	—	VSS	—	—	—	—	—	—	—	—
A14	VCC1833_3	IRQ18_4	P18_4	—	GTETRGA	DEE4 / ESWM_TASGATE1_5 / XSPI0_IO5	MDAT21	—	—	ENCIFOE4 / HDSL3_MOSI1
A15	VCC1833_3	IRQ18_1	P18_1	—	—	ESWM_TASGATE1_2 / XSPI0_IO2	MCLK32	—	—	HDSL3_CLK1
A16	VCC1833_3	IRQ17_6	P17_6	—	—	ESWM_TASGATE0_8 / XSPI0_DS	MCLK20	—	—	HDSL2_MOSI2
A17	—	VSS	—	—	—	—	—	—	—	—
A18	VCC1833_4	IRQ17_1	P17_1	—	MTIOC0B / MTIOC6C / GTIOC4_4B	RXDE3 / IIC_SDA1 / ETH2_COL / ETH3_COL / CANTX0 / XSPI1_IO7	MDAT31	—	MBX_HINT#	ENCIFDI3 / HDSL2_MISO1
A19	VCC1833_4	IRQ16_4	P16_4	—	MTIOC7B / GTIOC3_2A / GTIOC4_2A	RXD4/SCL3/MISO3 / SCKE7 / ETH4_CRS, SPI_MISO0 / XSPI1_IO2	MCLK01	—	—	ENCIFCK7 / HDSL1_MOSI2
A20	VCC1833_4	IRQ16_1	P16_1	—	MTIOC6D / GTIOC3_0B / GTIOC4_0B	TXD1/SDA1/MOSI1 / RXDE1 / IIC_SDA2 / ESWM_TASGATE0_3 / XSPI1_DS	MDAT22	—	—	ENCIFDI1 / HDSL1_CLK2
A21	—	VSS	—	—	—	—	—	—	—	—
A22	—	IRQ15_3	P15_3	D10	MTIOC1A / MTIOC3C / GTIOC2_4B / CMTW1_TOC0	RXDE2 / SD1_IOVS	—	ADTRG0#	HD10	ENCIFDI2 / HDSL1_LINK
A23	—	IRQ14_6	P14_6	D5	MTIOC1B / MTIOC4B / GTIOC2_2A / CMTW0_TIC0	SD0_PWEN	—	—	HD5	HDSL0_MOSI1 / POUTA
A24	—	IRQ14_3	P14_3	D2	POE0# / GTIOC0_2A / GTETRGA / RTCAT1HZ	SCIEXTCLK	—	ADTRG0# / USB_EXICEN	HD2 / MBX_HINT#	HDSL0_CLK1
A25	—	VSS	—	—	—	—	—	—	—	—
B1	VCC1833_1	IRQ24_3	P24_3	—	GTIOC4_5B / CMTW0_TIC1	RXD5/SDA5/MOSI5 / IIC_SCL1 / ETH0_RXER / ETH2_RXDV / ESC_I2CCLK / SPI_MOSI1 / SD0_PWEN	MDAT12	—	—	HDSL0_LINK
B2	VCC1833_1	IRQ23_6	P23_6	—	GTIOC4_3A / GTIOC5_3A / RTCAT1HZ	SCK4 / ETH2_RXCLK / ESC_LEDRUN / SD0_CD	MDAT30 / MDAT42	—	—	HDSL7_CLK2
B3	VCC1833_1	IRQ23_2	P23_2	—	GTIOC4_1A	IIC_SDA0 / ETH2_TXD1 / ESC_LINKACT0 / CANTXDP1 / SPI_MOSI0	MDAT21 / MDAT40	—	—	HDSL7_CLK1
B4	VCC1833_0	IRQ22_4	P22_4	—	GTIOC0_2B	ETH1_RXDV	—	—	—	HDSL6_CLK2
B5	VCC1833_0	ETH1_REFCLK / RMII1_REFCLK / IRQ22_6	P22_6	—	—	—	—	—	—	HDSL6_MISO2
B6	VCC1833_0	IRQ21_5	P21_5	—	—	ETH1_TXD3	—	—	—	HDSL5_MOSI2
B7	VCC1833_0	IRQ21_7	P21_7	—	GTIOC4_4A	ETH1_RXCLK	—	—	—	HDSL6_SMPL

Table 1.19 List of pins and pin functions (537-pin FBGA) (3 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
B8	VCC1833_0	IRQ21_1	P21_1	—	—	ETH1_TXCLK	—	—	—	HDSL5_MOSI1
B9	VCC1833_0	IRQ20_6	P20_6	—	—	ETHSW_PHYLINK0 / ESC_PHYLINK0 / ESWM_PHYLINK0 / HPSW_PHYLINK0 / CANRXDP1	—	—	—	HDSL5_CLK1
B10	VCC1833_0	ETH0_REFCLK / RMII0_REFCLK / IRQ20_7	P20_7	—	—	CANTXDP1	—	—	—	HDSL5_SEL1
B11	VCC1833_0	IRQ19_6	P19_6	—	—	ETH0_RXCLK	—	—	—	HDSL4_MOSI1
B12	VCC1833_0	IRQ19_2	P19_2	—	—	ETH0_TXD1	—	—	—	HDSL4_SMPL
B13	VCC1833_0	IRQ19_0	P19_0	—	—	ETH0_TXCLK	—	—	—	HDSL3_MOSI2
B14	VCC1833_3	IRQ18_5	P18_5	—	GTETRGB	RXDE4 / ESWM_TASGATE1_6 / XSPI0_IO6	MCLK20	—	—	ENCIFDI4 / HDSL3_CLK2
B15	VCC1833_3	IRQ18_0	P18_0	—	—	ESWM_TASGATE1_1 / XSPI0_IO1	MCLK02	—	—	HDSL3_SMPL
B16	VCC1833_3	IRQ17_3	P17_3	—	—	DEE7 / ESWM_TASGATE0_5 / XSPI0_CKN	MDAT30	—	—	ENCIFOE7 / HDSL2_CLK2
B17	VCC1833_3	IRQ17_2	P17_2	—	—	SCKE7 / ESWM_TASGATE0_4 / XSPI0_CKP	MCLK30	—	—	ENCIFCK7 / HDSL2_MOSI1
B18	VCC1833_4	IRQ16_6	P16_6	—	MTCLKC / MTIOC0C / GTIOC3_3A	SCKE3 / IIC_SCL0 / ETH2_TXER / ETH3_TXER / CANRXDP0 / SPI_RSPCK0 / XSPI1_IO4	MCLK30	—	—	ENCIFCK3 / HDSL2_SMPL
B19	VCC1833_4	IRQ16_3	P16_3	—	MTIOC7C / GTIOC3_1A / GTIOC4_1B	TXD5/SDA5/MOSI5 / TXDE4 / ETH4_RXER / SPI_SSL02 / XSPI1_IO1	—	—	—	ENCIFDO4 / HDSL1_MISO2
B20	VCC1833_4	IRQ16_0	P16_0	—	MTIOC1B / MTIOC6B / GTIOC3_0A / GTIOC4_0A	RXD1/SCL1/MISO1 / TXDE1 / IIC_SCL2 / ESWM_TASGATE0_2 / XSPI1_CS1#	MCLK22	—	—	ENCIFDO1 / HDSL1_MOSI1
B21	VCC1833_4	IRQ15_6	P15_6	—	GTIOC0_4A	DE1 / TXDE6 / TXDE7 / IIC_SCL1 / ESWM_TASGATE0_0 / XSPI1_CKP	MCLK21	—	—	ENCIFDO6 / ENCIFDO7 / HDSL1_SEL1
B22	—	IRQ15_1	P15_1	D8	MTCLKB / MTIOC8D / GTIOC2_3B / CMTW0_TOC1	DEE2 / SD1_WP	—	—	HD8	ENCIFOE2 / HDSL0_MISO2
B23	—	IRQ14_7	P14_7	D6	MTIOC1A / MTIOC4D / GTIOC2_2B / CMTW0_TOC0	SD0_IOVS	—	—	HD6	HDSL0_CLK2 / POUTB
B24	—	IRQ14_1	P14_1	D0	MTIOC3B / MTIOC8A / GTIOC0_0A / GTIOC2_0A / GTIOC4_6A	SCKE6 / ETH2_TXER / ETH3_TXER	—	USB_VBUSEN	HD0	ENCIFCK6 / HDSL0_LINK
B25	—	IRQ13_4	P13_4	D23	GTADSM3_1 / RTCAT1HZ	ETH1_COL / GMAC0_MDIO / GMAC1_MDIO / GMAC2_MDIO / ETHSW_MDIO / ESC_MDIO / ESWM_MDIO / SD1_IOVS	MDAT42	—	HD23	HDSL7_MOSI1
C1	VCC1833_1	IRQ25_0	P25_0	—	—	RXD1/SCL1/MISO1 / RXD3/SCL3/MISO3 / ETHSW_PHYLINK2 / ESC_PHYLINK2 / CANTX1 / SPI_SSL03	MCLK22	—	—	—

Table 1.19 List of pins and pin functions (537-pin FBGA) (4 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
C2	VCC1833_1	IRQ24_2	P24_2	TEND	POE8# / GTIOC4_5A / CMTW0_TOC0	CTS4# / RXDE0 / ETH2_RXD3 / ESC_RESETOUT# / SPI_SSL11	MDAT11	—	—	ENCIFDI0 / HDSL7_MOSI2
C3	VCC1833_1	IRQ24_0	P24_0	DREQ	POE0# / GTIOC4_4A	DEE0 / IIC_SDA1 / ETH0_CRS / ETH2_RXD1 / ESC_LINKACT2 / SPI_SSL13 / SD1_CD	MDAT10 / MDAT32	—	—	ENCIFOE0 / HDSL7_MISO2
C4	VCC1833_1	IRQ23_3	P23_3	—	GTIOC4_1B / GTIOC4_3A	SS3#/CTS3#/RTS3# / ETH2_TXD2 / ESC_LINKACT1 / SPI_SSL00	MCLK01 / MCLK41	—	—	HDSL7_SEL1
C5	VCC1833_1	IRQ23_1	P23_1	—	GTIOC3_3B / GTIOC4_0B	SCK3 / IIC_SCL0 / ETH2_TXD0 / GMAC0_PTPTRG0 / ESC_LATCH0 / CANRXDP1 / SPI_MISO0	MCLK21 / MCLK40	—	—	HDSL7_SMPL
C6	VCC1833_0	IRQ22_0	P22_0	—	GTIOC4_4B	ETH1_RXD0	—	—	—	HDSL6_CLK1
C7	VCC1833_0	IRQ20_5	P20_5	—	—	GMAC0_MDIO / GMAC1_MDIO / GMAC2_MDIO / ETHSW_MDIO / ESC_MDIO / ESWM_MDIO / CANRX1	—	—	—	HDSL5_SMPL
C8	VCC1833_0	IRQ21_3	P21_3	—	—	ETH1_TXD1	—	—	—	HDSL5_SEL2
C9	VCC1833_0	IRQ21_0	P21_0	—	—	—	—	—	—	HDSL5_MISO1
C10	VCC1833_0	IRQ20_2	P20_2	—	—	ETH0_RXD3 / CANTXDP0	—	—	—	HDSL4_MOSI2
C11	VCC1833_0	IRQ20_0	P20_0	—	—	ETH0_RXD1 / CANTX0	—	—	—	HDSL4_SEL2
C12	VCC1833_0	IRQ19_3	P19_3	—	—	ETH0_TXD2	—	—	—	HDSL4_CLK1
C13	VCC1833_3	IRQ18_7	P18_7	—	—	ESWM_TASGATE1_8 / XSPI0_RESET0#	MCLK30 / MDAT02	—	—	HDSL3_MISO2
C14	VCC1833_3	IRQ18_2	P18_2	—	—	ESWM_TASGATE1_3 / XSPI0_IO3	MDAT32	—	—	HDSL3_SEL1
C15	VCC1833_3	IRQ17_7	P17_7	—	—	ESWM_TASGATE1_0 / XSPI0_IO0	MDAT20	—	—	HDSL3_LINK
C16	VCC1833_3	IRQ17_5	P17_5	—	—	RXDE7 / ESWM_TASGATE0_7 / XSPI0_CS1#	MDAT31	—	—	ENCIFDI7 / HDSL2_MISO2
C17	VCC1833_4	IRQ17_0	P17_0	—	MTIOC0A / MTIOC6A / GTIOC3_4A	TXDE3 / IIC_SCL1 / ETH2_CRS / ETH3_CRS / CANRX0 / XSPI1_IO6	MCLK31	USB_VBUSEN	—	ENCIFDO3 / HDSL2_SEL1
C18	VCC1833_4	IRQ16_5	P16_5	—	MTIOC7D / GTIOC3_2B / GTIOC4_2B	TXD3/SDA3/MOSI3 / DEE7 / ETH4_COL / SPI_MOSI0 / XSPI1_IO3	MDAT01	—	—	ENCIFOE7 / HDSL2_LINK
C19	VCC1833_4	IRQ15_7	P15_7	—	GTIOC0_4B	DE3 / RXDE6 / RXDE7 / IIC_SDA1 / ESWM_TASGATE0_1 / XSPI1_CS0#	MDAT21	—	—	ENCIFDI6 / ENCIFDI7 / HDSL1_MISO1
C20	—	IRQ15_2	P15_2	D9	MTIOC3A / MTIC5W / GTIOC2_4A / CMTW1_TIC0	TXDE2 / SD1_PWEN	—	—	HD9	ENCIFDO2 / HDSL0_MOSI2
C21	—	IRQ15_4	P15_4	D11	GTIOC2_0A / CMTW1_TIC1	SCKE6 / IIC_SCL0 / ESC_I2CCLK	MCLK20	ADTRG1#	HD11	ENCIFCK6 / HDSL1_SMPL
C22	—	IRQ14_4	P14_4	D3	MTIOC4A / MTIC5U / GTIOC0_1B / GTIOC2_1A	TXDE6 / ETH2_CRS / ETH3_CRS	—	ADTRG1#	HD3	ENCIFDO6 / HDSL0_SEL1

Table 1.19 List of pins and pin functions (537-pin FBGA) (5 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
C23	—	IRQ14_2	P14_2	D1	MTIOC3D / MTIOC8B / GTIOC0_0B / GTIOC2_0B / GTIOC4_6B	DEE6 / ETH2_RXER / ETH3_RXER	—	USB_OVRCUR	HD1	ENCIFOE6 / HDSL0_SMPL
C24	—	IRQ13_3	P13_3	D22	GTADSM3_0	ETH1_CRS / GMAC0_MDC / GMAC1_MDC / GAMC2_MDC / ETHSW_MDC / ESC_MDC / ESWM_MDC / SD1_PWEN	MCLK42	—	HD22	HDSL7_MISO1
C25	—	IRQ13_2	P13_2	D21	GTADSM2_1	ESC_EDERR / SD1_IOVS	MDAT10	—	HD21	HDSL7_SEL1
D1	—	VSS	—	—	—	—	—	—	—	—
D2	VCC1833_1	IRQ24_7	P24_7	—	—	TXD3/SDA3/MOSI3 / GMAC0_MDIO / GMAC1_MDIO / GMAC2_MDIO / ETHSW_MDIO / ESC_MDIO / ESWM_MDIO / CANRX1 / SPI_RSPCK1	—	—	—	—
D3	VCC1833_1	MD1 / IRQ24_6	P24_6	—	—	DE5 / GMAC0_MDC / GMAC1_MDC / GMAC2_MDC / ETHSW_MDC / ESC_MDC / ESWM_MDC	—	—	—	—
D4	VCC1833_1	IRQ24_1	P24_1	DACK	POE4# / GTIOC4_4B / CMTW0_TIC0	SS4#/CTS4#/RTS4# / TXDE0 / ETH0_TXER / ETH2_RXD2 / ESC_IRQ / SPI_SSL10 / SD1_WP	MCLK11	—	MBX_HINT#	ENCIFDO0
D5	VCC1833_1	IRQ23_4	P23_4	—	GTIOC4_2A / GTIOC4_3B	CTS3# / ETH2_TXD3 / ETHSW_PTPOUT2 / ESC_SYNC0 / SPI_SSL01	MDAT01 / MDAT41	—	—	HDSL7_MISO1
D6	VCC1833_0	IRQ22_3	P22_3	—	GTIOC0_3B	ETH1_RXD3	—	—	—	HDSL6_MOSI1
D7	VCC1833_0	IRQ22_1	P22_1	—	GTIOC4_5A / GTIOC5_0A	ETH1_RXD1	—	—	—	HDSL6_SEL1
D8	VCC1833_0	IRQ21_2	P21_2	—	—	ETH1_TXD0	—	—	—	HDSL5_CLK2
D9	VCC1833_0	IRQ22_5	P22_5	—	—	ETHSW_PHYLINK1 / ESC_PHYLINK1 / ESWM_PHYLINK1 / HPSW_PHYLINK1	—	—	—	HDSL6_SEL2
D10	VCC1833_0	IRQ20_3	P20_3	—	—	ETH0_RXDV	—	—	—	HDSL5_LINK
D11	VCC1833_0	IRQ19_7	P19_7	—	—	ETH0_RXD0 / CANRX0	—	—	—	HDSL4_CLK2
D12	VCC1833_0	IRQ19_4	P19_4	—	—	ETH0_TXD3	—	—	—	HDSL4_SEL1
D13	VCC1833_0	IRQ19_1	P19_1	—	—	ETH0_TXD0	—	—	—	HDSL4_LINK
D14	VCC1833_3	IRQ18_6	P18_6	—	GTETRGC	TXDE4 / ESWM_TASGATE1_7 / XSPI0_IO7	MDAT20	—	—	ENCIFDO4 / HDSL3_SEL2
D15	VCC1833_3	IRQ18_3	P18_3	—	—	SCKE4 / ESWM_TASGATE1_4 / XSPI0_IO4	MCLK21	—	—	ENCIFCK4 / HDSL3_MISO1
D16	VCC1833_3	IRQ17_4	P17_4	—	—	TXDE7 / ESWM_TASGATE0_6 / XSPI0_CS0#	MCLK31	—	—	ENCIFDO7 / HDSL2_SEL2
D17	VCC1833_4	IRQ16_7	P16_7	—	MTCLKD / MTIOC0D / GTIOC3_3B	DEE3 / IIC_SDA0 / ETH2_RXER / ETH3_RXER / CANTXDP0 / SPI_SSL00 / XSPI1_IO5	MDAT30	—	—	ENCIFOE3 / HDSL2_CLK1

Table 1.19 List of pins and pin functions (537-pin FBGA) (6 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
D18	VCC1833_4	IRQ16_2	P16_2	—	MTIOC7A / GTIOC3_1B / GTIOC4_1A	RXD5/SCL5/MISO5 / RXDE4 / ETH4_TXER / SPI_SSL01 / XSPI1_IO0	—	—	—	ENCIFDI4 / HDSL1_SEL2
D19	—	IRQ15_5	P15_5	D12	GTIOC2_0B / CMTW1_TOC1 / RTCAT1HZ	DEE6 / IIC_SDA0 / ESC_I2CDATA	MDAT20	ADTRG2#	HD12	ENCIFDO6 / HDSL1_CLK1
D20	—	IRQ14_5	P14_5	D4	MTIOC4C / MTIC5V / GTIOC0_1A / GTIOC2_1B	RXDE6 / ETH2_COL / ETH3_COL	—	ADTRG2#	HD4	ENCIFDI6 / HDSL0_MISO1
D21	—	IRQ15_0	P15_0	D7	MTCLKA / MTIOC8C / GTIOC2_3A / CMTW0_TIC1	SCKE2 / SD1_CD	—	—	HD7	ENCIFCK2 / HDSL0_SEL2 / POUTZ
D22	—	IRQ13_5	P13_5	D24	GTADSM4_0	SCKE7 / ESC_LEDSTER	MCLK11	—	HD24	ENCIFCK7 / HDSL7_CLK2
D23	—	IRQ13_1	P13_1	D20 / TEND	GTADSM2_0	ESC_LEDRUN / SD1_PWEN	MCLK10	—	HD20	HDSL7_CLK1
D24	—	IRQ13_0	P13_0	D19	GTADSM1_1 / CMTW1_TOC1	ETHSW_PTPOUT1 / ESC_SYNC1	MDAT41	—	HD19	HDSL7_SMPL
D25	—	IRQ12_6	P12_6	D17 / DACK	GTADSM0_1 / GTETRGC / CMTW1_TOC0	—	MDAT40	—	HD17	HDSL6_MOSI2
E1	VCC1833_2	IRQ00_0	P00_0	A16	MTIOC3B / GTIOC0_0A / GTADSM0_0	SCKE1 / ETH3_TXCLK / SPI_RSPCK2	—	—	HA16	ENCIFCK1 / HDSL0_SEL1
E2	VCC1833_2	IRQ00_6	P00_6	A22	MTCLKA / MTIOC8D / GTIOC0_3A / GTADSM3_0	RXD4/SCL4/MISO4 / SCKE0 / SCKE6 / ETH3_RXCLK / SPI_SSL23	—	—	MBX_HINT#	ENCIFCK0 / ENCIFCK6
E3	VCC1833_1	IRQ24_5	P24_5	—	POE10# / GTIOC4_6B / GTETRGA	TXD4/SDA4/MOSI4 / SCIEXTCLK	MDAT22	PCIE_RSTOUTB	—	HDSL0_CLK1
E4	VCC1833_2	IRQ00_1	P00_1	A17	MTIOC3D / GTIOC0_0B / GTADSM0_1	DEE1 / IIC_SCL2 / ETH3_TXD0 / CANRX0 / SPI_MISO2	—	—	HA17	ENCIFOE1 / HDSL0_MISO1
E5	VCC1833_1	IRQ23_7	P23_7	—	GTIOC4_3B / GTIOC5_3B	SCKE0 / IIC_SCL1 / ETH0_COL / ETH2_RXD0 / SPI_SSL12 / SD0_WP	MCLK10 / MCLK32	—	—	ENCIFCK0 / HDSL7_SEL2
E6	VCC1833_0	IRQ22_7	P22_7	—	—	—	—	—	—	HDSL6_MOSI2
E7	—	VCC1833_1	—	—	—	—	—	—	—	—
E8	—	VSS	—	—	—	—	—	—	—	—
E9	—	VCC1833_0	—	—	—	—	—	—	—	—
E10	—	VSS	—	—	—	—	—	—	—	—
E11	—	VCC1833_0	—	—	—	—	—	—	—	—
E12	—	VSS	—	—	—	—	—	—	—	—
E13	—	VCC1833_3	—	—	—	—	—	—	—	—
E14	—	VSS	—	—	—	—	—	—	—	—
E15	—	VSS	—	—	—	—	—	—	—	—
E16	—	VCC1833_4	—	—	—	—	—	—	—	—
E17	—	VSS	—	—	—	—	—	—	—	—
E18	—	VCC33	—	—	—	—	—	—	—	—
E19	—	VSS	—	—	—	—	—	—	—	—
E20	—	IRQ13_7	P13_7	D26	—	TXDE7	MCLK12	—	HD26	ENCIFDO7 / HDSL7_MISO2
E21	—	IRQ14_0	P14_0	D27	—	RXDE7 / ETHSW_PTPOUT3 / ESC_SYNC1	MDAT12	—	HD27	ENCIFDI7 / HDSL7_MOSI2

Table 1.19 List of pins and pin functions (537-pin FBGA) (7 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
E22	—	IRQ12_7	P12_7	D18	GTADSM1_0 / GTETRGD / CMTW1_TIC1	ETHSW_PTPOUT0 / ESC_SYNC0	MCLK41	—	HD18	HDSL7_LINK
E23	—	IRQ13_6	P13_6	D25	GTADSM4_1	DEE7	MDAT11	—	HD25	ENCIFOE7 / HDSL7_SEL2
E24	—	IRQ12_5	P12_5	D16 / DREQ	GTADSM0_0 / GTETRGB / CMTW1_TIC0	—	MCLK40	—	HD16	HDSL6_MISO2
E25	—	VSS	—	—	—	—	—	—	—	—
F1	VCC1833_2	IRQ00_3	P00_3	A19	MTIOC4C / GTIOC0_1A / GTADSM1_1	RXDE1 / ETH3_TXD2 / CANRXDP0 / SPI_SSL20	MDAT41	—	HA19	ENCIFDI1 / HDSL0_CLK2
F2	VCC1833_2	IRQ00_5	P00_5	A21	MTIOC4D / MTIOC8C / GTIOC0_2B / GTADSM2_1	RXDE6 / ETH3_TXEN / SPI_SSL22	MDAT20	—	HA21	ENCIFDI6 / HDSL0_MISO2
F3	VCC1833_2	IRQ00_2	P00_2	A18	MTIOC4A / GTIOC0_1B / GTADSM1_0	TXDE1 / IIC_SDA2 / ETH3_TXD1 / CANTX0 / SPI_MOSI2	MCLK41	—	HA18	ENCIFDO1 / HDSL0_MOSI1
F4	VCC1833_2	IRQ00_4	P00_4	A20	MITOC4B / GTIOC0_2A / GTADSM2_0	TXDE6 / ETH3_TXD3 / CANTXDP0 / SPI_SSL21	MCLK20	—	HA20	ENCIFDO6 / HDSL0_SEL2
F5	VCC1833_1	ETH2_REFCLK / RMII2_REFCLK / IRQ24_4	P24_4	—	POE11# / GTIOC4_6A / CMTW0_TOC1	RXD5/SCL5/MISO5 / IIC_SDA1 / ETH1_RXER / ESC_I2CDATA / SPI_MISO1 / SD0_IOVS	MCLK12	—	—	HDSL0_SMPL
F6	—	VSS	—	—	—	—	—	—	—	—
F7	—	VCC1833_1	—	—	—	—	—	—	—	—
F8	—	VSS	—	—	—	—	—	—	—	—
F9	—	VCC1833_0	—	—	—	—	—	—	—	—
F10	—	VSS	—	—	—	—	—	—	—	—
F11	—	VCC1833_0	—	—	—	—	—	—	—	—
F12	—	VSS	—	—	—	—	—	—	—	—
F13	—	VCC1833_3	—	—	—	—	—	—	—	—
F14	—	VSS	—	—	—	—	—	—	—	—
F15	—	VCC18_PLL1	—	—	—	—	—	—	—	—
F16	—	VCC1833_4	—	—	—	—	—	—	—	—
F17	—	VSS	—	—	—	—	—	—	—	—
F18	—	VCC33	—	—	—	—	—	—	—	—
F19	—	VSS	—	—	—	—	—	—	—	—
F20	—	VCC33	—	—	—	—	—	—	—	—
F21	—	VSS	—	—	—	—	—	—	—	—
F22	—	VSS	—	—	—	—	—	—	—	—
F23	—	VSS	—	—	—	—	—	—	—	—
F24	—	VSS	—	—	—	—	—	—	—	—
F25	—	VSS	—	—	—	—	—	—	—	—
G1	—	VSS	—	—	—	—	—	—	—	—
G2	VCC1833_2	ETH3_REFCLK / RMII3_REFCLK / IRQ01_4	P01_4	CS5# / TEND	—	TXD1/SDA1/MOSI1 / RXDE4 / IIC_SDA1 / ETH1_RXER / ETH1_CRS / ESC_I2CDATA / SPI_RSPCK2	MCLK01	USB_EXICEN / ADTRG2#	—	ENCIFDI4

Table 1.19 List of pins and pin functions (537-pin FBGA) (8 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
G3	VCC1833_2	IRQ01_5	P01_5	CS2# / DREQ	—	TXDE4 / ETH1_COL / ETH3_TXER / ESC_RESETOUT# / ESWM_PHYLINK0 / HPSW_PHYLINK0 / SPI_SSL20	MDAT01	USB_EXICEN	HCS1#	ENCIFDO4
G4	VCC1833_2	IRQ01_2	P01_2	BS# / DREQ	—	SS5#/CTS5#/RST5# / TXD5/SDA5/MOSI5 / SCKE4 / ETH3_RXD3 / SPI_MOSI2 / SD1_IOVS	MCLK00	ADTRG0#	HBS#	ENCIFCK4
G5	VCC1833_2	IRQ00_7	P00_7	A23	MTCLKB / MTIOC1B / GTIOC0_3B / GTADSM3_1	TXD4/SDA4/MOSI4 / DEE0 / DEE6 / ETH3_RXD0 / SPI_SSL22	—	—	HERROUT#	ENCIFOE0 / ENCIFOE6
G6	—	VSS	—	—	—	—	—	—	—	—
G7	—	—	—	—	—	—	—	—	—	—
G8	—	—	—	—	—	—	—	—	—	—
G9	—	—	—	—	—	—	—	—	—	—
G10	—	—	—	—	—	—	—	—	—	—
G11	—	—	—	—	—	—	—	—	—	—
G12	—	—	—	—	—	—	—	—	—	—
G13	—	—	—	—	—	—	—	—	—	—
G14	—	—	—	—	—	—	—	—	—	—
G15	—	—	—	—	—	—	—	—	—	—
G16	—	—	—	—	—	—	—	—	—	—
G17	—	—	—	—	—	—	—	—	—	—
G18	—	—	—	—	—	—	—	—	—	—
G19	—	—	—	—	—	—	—	—	—	—
G20	—	DDR_VDDQ	—	—	—	—	—	—	—	—
G21	—	VSS	—	—	—	—	—	—	—	—
G22	—	VSS	—	—	—	—	—	—	—	—
G23	—	VSS	—	—	—	—	—	—	—	—
G24	—	VSS	—	—	—	—	—	—	—	—
G25	—	VSS	—	—	—	—	—	—	—	—
H1	VCC1833_2	IRQ01_6	P01_6	D13	MTIOC6B / MTIOC8B / GTIOC1_0A / GTADSM0_0 / GTETRGB / CMTW1_TIC0	SCK1 / ETH0_RXER / ETH4_TXCLK / SPI_RSPCK3 / SD1_CD	MCLK02	—	HD13	—
H2	VCC1833_2	IRQ01_1	P01_1	RD/WR#	MITOC3C / MTIOC8A / GTIOC0_4B / GTADSM4_1	SCK5 / RXD5/SCL5/ MISO5 / RXDE0 / ETH3_RXD2 / SD1_PWEN	—	USB_OVRCUR	HWRSTB#	ENCIFDI0
H3	VCC1833_2	IRQ01_3	P01_3	CS3# / DACK	—	CTS5# / RXD1/ SCL1/MISO1/ DEE4 / IIC_SCL1 / ETH1_TXER / ETH3_RXDV / ESC_I2CCLK / SPI_MISO2	MDAT00	ADTRG1#	MBX_HINT#	ENCIFOE4
H4	VCC1833_2	IRQ01_0	P01_0	A0	MTIOC1A / MTIOC3A / GTIOC0_4A / GTADSM4_0_	DE4 / TXDE0 / ETH3_RXD1 / SPI_SSL21	—	—	HA0	ENCIFDO0
H5	—	VSS	—	—	—	—	—	—	—	—
H6	—	VSS	—	—	—	—	—	—	—	—
H7	—	—	—	—	—	—	—	—	—	—
H8	—	—	—	—	—	—	—	—	—	—

Table 1.19 List of pins and pin functions (537-pin FBGA) (9 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
H9	—	—	—	—	—	—	—	—	—	—
H10	—	—	—	—	—	—	—	—	—	—
H11	—	—	—	—	—	—	—	—	—	—
H12	—	—	—	—	—	—	—	—	—	—
H13	—	—	—	—	—	—	—	—	—	—
H14	—	—	—	—	—	—	—	—	—	—
H15	—	—	—	—	—	—	—	—	—	—
H16	—	—	—	—	—	—	—	—	—	—
H17	—	—	—	—	—	—	—	—	—	—
H18	—	—	—	—	—	—	—	—	—	—
H19	—	—	—	—	—	—	—	—	—	—
H20	—	DDR_VDDQ	—	—	—	—	—	—	—	—
H21	—	VSS	—	—	—	—	—	—	—	—
H22	—	—	—	—	—	—	—	DDR_DQA15	—	—
H23	—	—	—	—	—	—	—	DDR_DQA8	—	—
H24	—	VSS	—	—	—	—	—	—	—	—
H25	—	—	—	—	—	—	—	DDR_DQA14	—	—
J1	VCC1833_2	IRQ02_5	P02_5	A11	MTCLKD / MTIOC0D / GTIOC1_3B / GTADSM3_1	RXD2/SCL2/MISO2 / DEE1 / ETH4_RXD0 / GMAC2_PTPTRG1 / SPI_SSL32	MDAT12/ MDAT40	—	HA11	ENCIFOE1
J2	VCC1833_2	IRQ02_1	P02_1	WE3#/AH#	MTIC5W / MTIOC7C / GTIOC1_1A / GTADSM1_1	SS1#/CTS1#/RTS1# / RXD3/SCL3/MISO3 / TXDE5 / ETH4_TXD2 / GMAC0_PTPTRG0 / ESC_LATCH0 / SPI_SSL30 / SPI_SSL00	—	—	HWR3#	ENCIFDO5
J3	VCC1833_2	IRQ02_0	P02_0	WE2#	MTIC5V / MTIOC7A / GTIOC1_1B / GTADSM1_0 / GTETRGD	TXD1/SDA1/MOSI1 / SCIEXTCLK / ETH4_TXD1 / ETHSW_PTPOUT0 / ESC_SYNC0 / SPI_MOSI3 / SD1_PWEN	—	—	HWR2#	—
J4	VCC1833_2	IRQ01_7	P01_7	D14	MTIC5U / MTIOC6D / GTIOC1_0B / GTADSM0_1 / GTETRGC / CMTW1_TOC0	RXD1/SCL1/MISO1 / ETH1_RXER / ETH4_TXD0 / SPI_MISO3 / SD1_WP	MDAT02	—	HD14	—
J5	—	VCC1833_2	—	—	—	—	—	—	—	—
J6	—	VCC1833_2	—	—	—	—	—	—	—	—
J7	—	—	—	—	—	—	—	—	—	—
J8	—	—	—	—	—	—	—	—	—	—
J9	—	VDD	—	—	—	—	—	—	—	—
J10	—	VSS	—	—	—	—	—	—	—	—
J11	—	VSS	—	—	—	—	—	—	—	—
J12	—	VDD	—	—	—	—	—	—	—	—
J13	—	VDD	—	—	—	—	—	—	—	—
J14	—	VSS	—	—	—	—	—	—	—	—
J15	—	VSS	—	—	—	—	—	—	—	—
J16	—	VDD	—	—	—	—	—	—	—	—
J17	—	VDD	—	—	—	—	—	—	—	—
J18	—	—	—	—	—	—	—	—	—	—
J19	—	—	—	—	—	—	—	—	—	—

Table 1.19 List of pins and pin functions (537-pin FBGA) (10 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
J20	—	VSS	—	—	—	—	—	—	—	—
J21	—	—	—	—	—	—	—	DDR_DQA12	—	—
J22	—	—	—	—	—	—	—	DDR_DQA11	—	—
J23	—	VSS	—	—	—	—	—	—	—	—
J24	—	—	—	—	—	—	—	DDR_DQSA_T1	—	—
J25	—	—	—	—	—	—	—	DDR_DQSA_C1	—	—
K1	—	VSS	—	—	—	—	—	—	—	—
K2	VCC1833_2	IRQ02_4	P02_4	A10	MTCLKC / MTIOC0C / GTIOC1_3A / GTADSM3_0	SCK2/ SCKE1 / ETH4_RXCLK / GMAC1_PTPTRG1 / SPI_SSL03 / SPI_SSL33	MCLK12 / MCLK40	—	HA10	ENCIFCK1
K3	VCC1833_2	IRQ03_1	P03_1	A15	GTIOC3_3B	DE2 / DEE5 / IIC_SDA2 / ETH0_CRS / ETH4_RXDV / ETHSW_PTPOUT3 / ESC_SYNC1 / SPI_MISO3	MDAT10	—	HA15	ENCIFOE5 / SI3# / HDSL1_LINK
K4	VCC1833_2	IRQ02_2	P02_2	D15	MTIOC0A / MTIOC7B / GTIOC1_2A / GTADSM2_0	CTS1# / ETH4_TXD3 / GMAC0_PTPTRG1 / ESC_LEDRUN / ESC_LATCH1 / SPI_SSL01 / SPI_SSL31 / SD1_PWEN	—	—	HD15	—
K5	VCC1833_2	IRQ02_3	P02_3	A9	MTIOC0B / MTIOC7D / GTIOC1_2B / GTADSM2_1	DE1 / ETH4_TXEN / GMAC1_PTPTRG0 / ESC_LEDERR / SPI_SSL02 / SPI_SSL32 / SD1_IOVS	—	—	HA9	—
K6	—	VCC1833_2	—	—	—	—	—	—	—	—
K7	—	—	—	—	—	—	—	—	—	—
K8	—	—	—	—	—	—	—	—	—	—
K9	—	VSS	—	—	—	—	—	—	—	—
K10	—	VDD	—	—	—	—	—	—	—	—
K11	—	VDD	—	—	—	—	—	—	—	—
K12	—	VSS	—	—	—	—	—	—	—	—
K13	—	VSS	—	—	—	—	—	—	—	—
K14	—	VDD	—	—	—	—	—	—	—	—
K15	—	VDD	—	—	—	—	—	—	—	—
K16	—	VSS	—	—	—	—	—	—	—	—
K17	—	VSS	—	—	—	—	—	—	—	—
K18	—	—	—	—	—	—	—	—	—	—
K19	—	—	—	—	—	—	—	—	—	—
K20	—	DDR_VDDQ	—	—	—	—	—	—	—	—
K21	—	—	—	—	—	—	—	DDR_DQA13	—	—
K22	—	VSS	—	—	—	—	—	—	—	—
K23	—	—	—	—	—	—	—	DDR_DQA9	—	—
K24	—	—	—	—	—	—	—	DDR_DMIA1	—	—
K25	—	VSS	—	—	—	—	—	—	—	—

Table 1.19 List of pins and pin functions (537-pin FBGA) (11 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
L1	VCC1833_2	IRQ03_3	P03_3	TEND	CMTW1_TIC1	TXD1/SDA1/MOSI1 / TXD3/SDA3/MOSI3 / GMAC0_MDIO / GMAC1_MDIO / GMAC2_MDIO / ETHSW_MDIO / ESC_MDIO / ESWM_MDIO / ESC_LINKACT0 / SD1_PWEN	—	—	—	—
L2	VCC1833_2	MD2 / IRQ03_2	P03_2	DACK	CMTW1_TOC1 / RTCAT1HZ	DE2 / TXDE4 / ETH0_TXER / GMAC0_MDC / GMAC1_MDC / GMAC2_MDC / ETHSW_MDC / ESC_MDC / ESWM_MDC / SD1_IOVS	—	—	—	ENCIFDO4
L3	VCC1833_2	IRQ03_0	P03_0	A14	GTIOC3_3A	CTS2# / SCKE5 / IIC_SCL2 / ETH0_COL / ETH4_RXD3 / SPI_MOSI3	MCLK10	—	HA14	ENCIFCK5 / TST_OUT3 / HDSL0_MOSI2
L4	VCC1833_2	IRQ02_7	P02_7	A13	MTIOC1B / MTIOC6C / GTIOC1_4B / GTADSM4_1	SS2#/CTS2#/RTS2# / RXDE1 / ETH4_RXD2	MDAT11 / MDAT42	—	HA13	ENCIFDI1 / DUEI3
L5	VCC1833_2	IRQ02_6	P02_6	A12	MTIOC1A / MTIOC6A / GTIOC1_4A / GTADSM4_0	TXD2/SDA2/MOSI2 / TXDE1 / ETH4_RXD1 / GMAC2_PTPTRG0 / ESC_LEDSTER / SPI_SSL31	MCLK11 / MCLK42	—	HA12	ENCIFDO1
L6	—	VCC1833_2	—	—	—	—	—	—	—	—
L7	—	—	—	—	—	—	—	—	—	—
L8	—	—	—	—	—	—	—	—	—	—
L9	—	VDD	—	—	—	—	—	—	—	—
L10	—	VSS	—	—	—	—	—	—	—	—
L11	—	VSS	—	—	—	—	—	—	—	—
L12	—	VSS	—	—	—	—	—	—	—	—
L13	—	VSS	—	—	—	—	—	—	—	—
L14	—	VSS	—	—	—	—	—	—	—	—
L15	—	VSS	—	—	—	—	—	—	—	—
L16	—	VDD	—	—	—	—	—	—	—	—
L17	—	VDD	—	—	—	—	—	—	—	—
L18	—	—	—	—	—	—	—	—	—	—
L19	—	—	—	—	—	—	—	—	—	—
L20	—	VSS	—	—	—	—	—	—	—	—
L21	—	—	—	—	—	—	—	DDR_DQA10	—	—
L22	—	VSS	—	—	—	—	—	—	—	—
L23	—	—	—	—	—	—	—	DDR_DQA1	—	—
L24	—	—	—	—	—	—	—	DDR_DQA3	—	—
L25	—	VSS	—	—	—	—	—	—	—	—
M1	VCC1833_6	IRQ04_1	P04_1	—	GTIOC1_1A	SS0#/CTS0#/RST0# / DEE1 / SD1_DATA1	MDAT00 / MDAT30	—	—	ENCIFOE1 / DUEI5 / HDSL1_MISO1
M2	VCC1833_2	IRQ03_5	P03_5	A25	GTETRGSB	RXD3/SCL3/MISO3 / RXDE5 / ETH4_RXER / ESWM_PHYLINK1 / HPSW_PHYLINK1 / SPI_MISO0 / SPI_SSL30 / SD1_WP	MDAT11 / MCLK30	—	—	ENCIFDI5

Table 1.19 List of pins and pin functions (537-pin FBGA) (12 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
M3	VCC1833_6	IRQ03_7	P03_7	—	GTIOC1_0B	RXD0/SCL0/MISO0 / DEE0 / IIC_SCL0 / SD1_CMD	MDAT02 / MDAT32	—	—	ENCIFOE0 / TST_OUT4 / HDSL1_CLK1
M4	VCC1833_2	ETH4_REFCLK / RMII4_REFCLK / IRQ03_4	P03_4	A24	GTETRGSA	TXDE5 / ESC_RESETOUT# / SPI_MOSI0 / SPI_RSPCK3 / SD1_CD	MCLK11	—	—	ENCIFDO5
M5	—	VSS	—	—	—	—	—	—	—	—
M6	—	VSS	—	—	—	—	—	—	—	—
M7	—	—	—	—	—	—	—	—	—	—
M8	—	—	—	—	—	—	—	—	—	—
M9	—	VSS	—	—	—	—	—	—	—	—
M10	—	VDD	—	—	—	—	—	—	—	—
M11	—	VSS	—	—	—	—	—	—	—	—
M12	—	VSS	—	—	—	—	—	—	—	—
M13	—	VSS	—	—	—	—	—	—	—	—
M14	—	VSS	—	—	—	—	—	—	—	—
M15	—	VSS	—	—	—	—	—	—	—	—
M16	—	VSS	—	—	—	—	—	—	—	—
M17	—	VSS	—	—	—	—	—	—	—	—
M18	—	—	—	—	—	—	—	—	—	—
M19	—	—	—	—	—	—	—	—	—	—
M20	—	DDR_VDDQ	—	—	—	—	—	—	—	—
M21	—	—	—	—	—	—	—	DDR_DMIA0	—	—
M22	—	—	—	—	—	—	—	DDR_DQA7	—	—
M23	—	VSS	—	—	—	—	—	—	—	—
M24	—	—	—	—	—	—	—	DDR_DQSA_C0	—	—
M25	—	—	—	—	—	—	—	DDR_DQSA_T0	—	—
N1	—	VSS	—	—	—	—	—	—	—	—
N2	VCC1833_6	IRQ03_6	P03_6	—	GTIOC1_0A	SCK0 / SCKE0 / SD1_CLK	MCLK02 / MCLK32	—	—	ENCIFCK0 / DUEI4 / HDSL1_SMPL
N3	VCC1833_6	IRQ04_0	P04_0	—	GTIOC1_1B	TXD0/SDA0/MOSI0 / SCKE1 / IIC_SDA0 / SD1_DATA0	MCLK00 / MCLK30	—	—	ENCIFCK1 / SI4# / HDSL1_SEL1
N4	VCC1833_6	IRQ04_2	P04_2	—	GTIOC1_2A	CTS0# / TXDE2 / SD1_DATA2	MCLK01 / MCLK31	—	—	ENCIFDO2 / TST_OUT5 / HDSL1_MOSI1
N5	—	VCC1833_6	—	—	—	—	—	—	—	—
N6	—	VCC1833_6	—	—	—	—	—	—	—	—
N7	—	—	—	—	—	—	—	—	—	—
N8	—	—	—	—	—	—	—	—	—	—
N9	—	VDD	—	—	—	—	—	—	—	—
N10	—	VSS	—	—	—	—	—	—	—	—
N11	—	VSS	—	—	—	—	—	—	—	—
N12	—	VSS	—	—	—	—	—	—	—	—
N13	—	VSS	—	—	—	—	—	—	—	—
N14	—	VSS	—	—	—	—	—	—	—	—
N15	—	VSS	—	—	—	—	—	—	—	—
N16	—	VDD	—	—	—	—	—	—	—	—
N17	—	VCC18_PLL2	—	—	—	—	—	—	—	—

Table 1.19 List of pins and pin functions (537-pin FBGA) (13 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
N18	—	—	—	—	—	—	—	—	—	—
N19	—	—	—	—	—	—	—	—	—	—
N20	—	VSS	—	—	—	—	—	—	—	—
N21	—	—	—	—	—	—	—	DDR_DQA2	—	—
N22	—	VSS	—	—	—	—	—	—	—	—
N23	—	—	—	—	—	—	—	DDR_DQA5	—	—
N24	—	—	—	—	—	—	—	DDR_DQA4	—	—
N25	—	VSS	—	—	—	—	—	—	—	—
P1	VCC1833_5	IRQ04_5	P04_5	—	GTIOC5_1B / CMTW0_TOC0	RXD1/SCL1/MISO1 / ESC_LINKACT0 / CANRX0 / SPI_MISO1 / SD0_CMD / NAND_RE#	—	—	HSPI_CS#	TST_OUT6 / HDSL1_MISO2
P2	VCC1833_5	IRQ04_4	P04_4	—	GTIOC5_1A / CMTW0_TIC0	SCK1 / GMAC0_PTPTRG0 / ESC_LATCH0 / SPI_RSPCK1 / SD0_CLK / NAND_WE#	—	—	HSPI_INT#	DUEI6 / HDSL1_SEL2
P3	VCC1833_6	IRQ04_3	P04_3	—	GTIOC1_2B	DE0 / RXDE2 / SD1_DATA3	MDAT01 / MDAT31	—	—	ENCIFDI2 / SI5# / HDSL1_CLK2
P4	VCC1833_5	IRQ04_6	P04_6	—	GTIOC2_4A / GTIOC5_2A / CMTW0_TIC1	TXD1/SDA1/MOSI1 / ESC_LINKACT1 / CANTX0 / SPI_MOSI1 / SD0_DATA0 / NAND_IO0	—	—	HSPI_IO0	SI6# / HDSL1_MOSI2
P5	—	VSS	—	—	—	—	—	—	—	—
P6	—	VSS	—	—	—	—	—	—	—	—
P7	—	—	—	—	—	—	—	—	—	—
P8	—	—	—	—	—	—	—	—	—	—
P9	—	VSS	—	—	—	—	—	—	—	—
P10	—	VDD	—	—	—	—	—	—	—	—
P11	—	VSS	—	—	—	—	—	—	—	—
P12	—	VSS	—	—	—	—	—	—	—	—
P13	—	VSS	—	—	—	—	—	—	—	—
P14	—	VSS	—	—	—	—	—	—	—	—
P15	—	VSS	—	—	—	—	—	—	—	—
P16	—	VSS	—	—	—	—	—	—	—	—
P17	—	VSS	—	—	—	—	—	—	—	—
P18	—	—	—	—	—	—	—	—	—	—
P19	—	—	—	—	—	—	—	—	—	—
P20	—	DDR_VDDQ	—	—	—	—	—	—	—	—
P21	—	VSS	—	—	—	—	—	—	—	—
P22	—	—	—	—	—	—	—	DDR_DQA0	—	—
P23	—	VSS	—	—	—	—	—	—	—	—
P24	—	—	—	—	—	—	—	DDR_DQA6	—	—
P25	—	VSS	—	—	—	—	—	—	—	—
R1	VCC1833_5	IRQ05_2	P05_2	—	GTIOC1_3B / GTIOC5_0A / CMTW1_TIC1	SCK2 / TXDE5 / ESC_LEDRUN / SPI_RSPCK2 / SD0_DATA4 / NAND_IO4	—	—	HSPI_CK	ENCIFDO5 / HDSL2_CLK1

Table 1.19 List of pins and pin functions (537-pin FBGA) (14 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
R2	VCC1833_5	IRQ05_0	P05_0	—	GTIOC3_4A / GTIOC5_3A / CMTW1_TIC0	CTS1# / SCKE5 / ESC_LEDERR / CANTXDP0 / SPI_SSL11 / SD0_DATA2 / NAND_IO2	—	—	HSPI_IO2	ENCIFCK5 / TST_OUT7 / HDSL2_SMPL
R3	VCC1833_5	IRQ04_7	P04_7	—	GTIOC2_4B / GTIOC5_2B / CMTW0_TOC1	SS1#/CTS1#/RTS1# / ESC_RESETOUT# / CANRXDP0 / SPI_DDL10 / SD0_DATA1 / NAND_IO1	—	—	HSPI_IO1	DUEI7 / HDSL2_LINK
R4	VCC1833_5	IRQ05_1	P05_1	—	GTIOC4_4B / GTIOC5_3B / CMTW1_TOC0	DE1 / DEE5 / ETHSW_PTPOUT0 / ESC_SYNC0 / SPI_SSL12 / SPI_RSPCK0 / SD0_DATA3 / NAND_IO3	—	—	HSPI_IO3	ENCIFOE5 / SI7#
R5	—	VCC1833_5	—	—	—	—	—	—	—	—
R6	—	VCC1833_5	—	—	—	—	—	—	—	—
R7	—	—	—	—	—	—	—	—	—	—
R8	—	—	—	—	—	—	—	—	—	—
R9	—	VCC18_PLL0	—	—	—	—	—	—	—	—
R10	—	VSS	—	—	—	—	—	—	—	—
R11	—	VSS	—	—	—	—	—	—	—	—
R12	—	VSS	—	—	—	—	—	—	—	—
R13	—	VSS	—	—	—	—	—	—	—	—
R14	—	VSS	—	—	—	—	—	—	—	—
R15	—	VSS	—	—	—	—	—	—	—	—
R16	—	VDD	—	—	—	—	—	—	—	—
R17	—	VDD	—	—	—	—	—	—	—	—
R18	—	—	—	—	—	—	—	—	—	—
R19	—	—	—	—	—	—	—	—	—	—
R20	—	VSS	—	—	—	—	—	—	—	—
R21	—	—	—	—	—	—	—	DDR_CSA0	—	—
R22	—	—	—	—	—	—	—	DDR_CAA0	—	—
R23	—	VSS	—	—	—	—	—	—	—	—
R24	—	—	—	—	—	—	—	DDR_CKA_C	—	—
R25	—	—	—	—	—	—	—	DDR_CKA_T	—	—
T1	—	VSS	—	—	—	—	—	—	—	—
T2	VCC1833_5	IRQ05_5	P05_5	—	GTIOC2_3B	SS2#/CTS2#/RTS2# / RXD2/SCL2/MISO2 / ETH0_CRS / SPI_SSL20 / SD0_DATA7 / NAND_IO7	MDAT00	—	HSPI_IO6	HDSL2_MOSI1
T3	VCC1833_5	IRQ05_3	P05_3	—	GTIOC5_0B / CMTW1_TOC1	RXD2/SCL2/MISO2 / RXDE5 / IIC_SCL2 / ETH0_TXER / ETH1_RXER / SPI_MISO2 / SD0_DATA5 / NAND_IO5	—	—	HSPI_IO4	ENCIFDI5 / HDSL2_SEL1
T4	VCC1833_5	IRQ05_4	P05_4	—	GTIOC2_3A	TXD2/SDA2/MOSI2 / IIC_SDA2 / ETH0_RXER / SPI_MOSI2 / SD0_DATA6 / NAND_IO6	MCLK00	—	HSPI_IO5	HDSL2_MISO1
T5	—	VSS	—	—	—	—	—	—	—	—
T6	—	VSS	—	—	—	—	—	—	—	—

Table 1.19 List of pins and pin functions (537-pin FBGA) (15 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
T7	—	—	—	—	—	—	—	—	—	—
T8	—	—	—	—	—	—	—	—	—	—
T9	—	VSS	—	—	—	—	—	—	—	—
T10	—	VSS	—	—	—	—	—	—	—	—
T11	—	VDD	—	—	—	—	—	—	—	—
T12	—	VDD	—	—	—	—	—	—	—	—
T13	—	VDD	—	—	—	—	—	—	—	—
T14	—	VDD	—	—	—	—	—	—	—	—
T15	—	VSS	—	—	—	—	—	—	—	—
T16	—	VSS	—	—	—	—	—	—	—	—
T17	—	VSS	—	—	—	—	—	—	—	—
T18	—	—	—	—	—	—	—	—	—	—
T19	—	—	—	—	—	—	—	—	—	—
T20	—	DDR_VDDQ	—	—	—	—	—	—	—	—
T21	—	VSS	—	—	—	—	—	—	—	—
T22	—	—	—	—	—	—	—	DDR_CAA2	—	—
T23	—	—	—	—	—	—	—	DDR_CAA1	—	—
T24	—	—	—	—	—	—	—	DDR_CKEA0	—	—
T25	—	VSS	—	—	—	—	—	—	—	—
U1	—	IRQ06_0	P06_0	CS3#	GTIOC1_0A	SS3#/CTS3#/RTS3# / ETH1_RXER / ESC_LEDSTER / CANRXDP1 / SPI_SSL00	—	—	—	TST_OUT4 / HDSL2_MISO2
U2	—	IRQ05_7	P05_7	CS2#	GTIOC1_3A	SCK3 / SCKE5 / ETH1_TXER / ESC_RESETOUT# / SPI_RSPCK0	MCLK00	—	—	ENCIFCK5 / DUEI4 / HDSL2_SEL2
U3	VCC1833_5	IRQ05_6	P05_6	—	—	CTS2# / TXD2/SDA2/ MOSI2 / ETH2_COL / SPI_SSL21 / SD0_RST# / NAND_WP#	MCLK01	—	HSPI_IO7	HDSL2_CLK2
U4	—	IRQ06_3	P06_3	D29	GTIOC1_1B / GTIOC2_0B	CTS3# / GMAC1_PTPTRG0 / ESC_LEDERR / CANTXDP1 / SPI_SSL01	—	—	HD29	TST_OUT5 / HDSL3_SMPL
U5	—	IRQ06_1	P06_1	CS5#	GTIOC1_3B	DEE5 / TXD3/SDA3/ MOSI3 / ETH1_CRS / CANTX1 / SPI_MOSI0	MDAT00	—	—	ENCIFOE5 / SI4# / HDSL2_MOSI2
U6	—	VCC33	—	—	—	—	—	—	—	—
U7	—	—	—	—	—	—	—	—	—	—
U8	—	—	—	—	—	—	—	—	—	—
U9	—	VDD	—	—	—	—	—	—	—	—
U10	—	VDD	—	—	—	—	—	—	—	—
U11	—	VSS	—	—	—	—	—	—	—	—
U12	—	VCC18_PLL3	—	—	—	—	—	—	—	—
U13	—	VCC18_PLL4	—	—	—	—	—	—	—	—
U14	—	VSS	—	—	—	—	—	—	—	—
U15	—	VDD	—	—	—	—	—	—	—	—
U16	—	VCC33	—	—	—	—	—	—	—	—
U17	—	VDD	—	—	—	—	—	—	—	—
U18	—	—	—	—	—	—	—	—	—	—
U19	—	—	—	—	—	—	—	—	—	—

Table 1.19 List of pins and pin functions (537-pin FBGA) (16 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
U20	—	VSS	—	—	—	—	—	—	—	—
U21	—	—	—	—	—	—	—	DDR_CAA4	—	—
U22	—	—	—	—	—	—	—	DDR_CAA3	—	—
U23	—	VSS	—	—	—	—	—	—	—	—
U24	—	—	—	—	—	—	—	DDR_CSA1	—	—
U25	—	—	—	—	—	—	—	DDR_CKEA1	—	—
V1	—	IRQ06_5	P06_5	D31	MTIOC2B / GTIOC1_2A / GTIOC2_1B	SCK4 / SPI_SSL03	MCLK30	—	HD31	DUIE6 / HDSL3_SEL1
V2	—	IRQ06_4	P06_4	D30	GTIOC1_1A / GTIOC2_1A	DE3 / GMAC1_PTPTRG1 / SPI_SSL02	MDAT01	—	HD30	SI5# / HDSL3_CLK1
V3	—	IRQ06_2	P06_2	D28	GTIOC1_0B / GITOC02_0A	RXD3/SCL3/MISO3 / ETH1_COL / CANRX1 / SPI_MISO0	MCLK01	—	HD28	DUEI5 / HDSL3_LINK
V4	—	IRQ06_7	P06_7	—	GTIOC1_4B / GITOC02_2B	TXD4/SDA4/MOSI4 / RXDE5 / CANTX0 / SD1_IOVS	MDAT02	—	—	ENCIFDI5 / SI6# / HDCL3_MOSI1
V5	—	IRQ07_1	P07_1	—	POE4#	CTS4# / DEE1 / ETH4_RXER / ETHSW_TDMAOUT1 / ESC_LEDERR / CANRXDP0 / SPI_SSL22	MCLK31	ADTRG0#	—	ENCIFOE1 / TST_OUT7 / HDSL3_SEL2
V6	—	VCC33	—	—	—	—	—	—	—	—
V7	—	—	—	—	—	—	—	—	—	—
V8	—	—	—	—	—	—	—	—	—	—
V9	—	—	—	—	—	—	—	—	—	—
V10	—	—	—	—	—	—	—	—	—	—
V11	—	—	—	—	—	—	—	—	—	—
V12	—	—	—	—	—	—	—	—	—	—
V13	—	—	—	—	—	—	—	—	—	—
V14	—	—	—	—	—	—	—	—	—	—
V15	—	—	—	—	—	—	—	—	—	—
V16	—	—	—	—	—	—	—	—	—	—
V17	—	—	—	—	—	—	—	—	—	—
V18	—	—	—	—	—	—	—	—	—	—
V19	—	—	—	—	—	—	—	—	—	—
V20	—	DDR_VDDQ	—	—	—	—	—	—	—	—
V21	—	—	—	—	—	—	—	DDR_CALIBRATION	—	—
V22	—	—	—	—	—	—	—	DDR_RETENTION	—	—
V23	—	—	—	—	—	—	—	DDR_RESET#	—	—
V24	—	—	—	—	—	—	—	DDR_CAA5	—	—
V25	—	VSS	—	—	—	—	—	—	—	—
W1	—	VSS	—	—	—	—	—	—	—	—
W2	—	IRQ07_0	P07_0	—	POE0# / GTIOC1_2B	SS4#/CTS4#/RTS4# / IIC_SDA1 / ETH4_TXER / ESC_RESETOUT# / SPI_SSL13	MDAT30	ADTRG2#	—	DUEI7 / HDSL3_CLK2 / POUTA
W3	—	IRQ06_6	P06_6	—	GTIOC1_4A / GTIOC2_2A	RXD4/SCL4/MISO4 / TXDE5 / CANRX0 / SD1_PWEN	MCLK02	—	—	ENCIFDO5 / TST_OUT6 / HDSL3_MISO1

Table 1.19 List of pins and pin functions (537-pin FBGA) (17 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
W4	—	IRQ07_4	P07_4	A16	POE11# / GTIOC1_1B	SCKE1 / GMAC2_PTPTRG0 / ETHSW_TDMAOUT0 / ESC_LEDRUN	MDAT22	—	—	ENCIFCK1 / HDSL3_MOSI2
W5	—	IRQ07_2	P07_2	—	POE8#	DE4 / TXDE1 / ETH4_CRS / ETHSW_PTPOUT2 / ESC_SYNC0 / CANTXDP0 / SPI_SSL23	MDAT31	ADTRG1#	—	ENCIFDO1 / SI7# / POUTB
W6	—	VSS	—	—	—	—	—	—	—	—
W7	—	—	—	—	—	—	—	—	—	—
W8	—	—	—	—	—	—	—	—	—	—
W9	—	—	—	—	—	—	—	—	—	—
W10	—	—	—	—	—	—	—	—	—	—
W11	—	—	—	—	—	—	—	—	—	—
W12	—	—	—	—	—	—	—	—	—	—
W13	—	—	—	—	—	—	—	—	—	—
W14	—	—	—	—	—	—	—	—	—	—
W15	—	—	—	—	—	—	—	—	—	—
W16	—	—	—	—	—	—	—	—	—	—
W17	—	—	—	—	—	—	—	—	—	—
W18	—	—	—	—	—	—	—	—	—	—
W19	—	—	—	—	—	—	—	—	—	—
W20	—	VSS	—	—	—	—	—	—	—	—
W21	—	VSS	—	—	—	—	—	—	—	—
W22	—	VSS	—	—	—	—	—	—	—	—
W23	—	VSS	—	—	—	—	—	—	—	—
W24	—	VSS	—	—	—	—	—	—	—	—
W25	—	VSS	—	—	—	—	—	—	—	—
Y1	—	IRQ07_5	P07_5	—	MTCLKC / MTIOC0C / GTETRGA	TXDE6 / IIC_SDA0 / ETH0_TXER / CANTX0 / SPI_MOSI3	MCLK21	—	—	ENCIFDO6 / DUEI0 / HDSL6_LINK
Y2	—	IRQ07_6	P07_6	A23	GTETRGB	ETH0_RXER / CANRXDP0 / SPI_SSL30	—	—	—	TST_OUT0 / HDSL6_SMPL
Y3	—	IRQ07_3	P07_3	—	POE10# / GTIOC1_0A	RXDE1 / IIC_SCL1 / ETH4_COL / GMAC2_PTPTRG1 / ETHSW_PTPOUT3 / ESC_SYNC1	MCLK22	—	—	ENCIFDI1 / HDSL3_MISO2 / POUTZ
Y4	—	IRQ07_7	P07_7	A22	MTCLKD / MTIOC0D / GTIOC0_1B / GTIOC4_0B / GTETRGC	SCK5 / DEE6 / IIC_SCL0 / ETH0_CRS / CANRX0 / SPI_MISO3	MCLK32	—	—	ENCIFOE6
Y5	—	IRQ08_3	P08_3	A18	—	TXD5/SDA5/MOSI5 / ETH1_CRS / ETHSW_TDMAOUT2 / ESC_LINKACT0 / CANRXDP1 / SPI_SSL33	—	—	—	SI0# / HDSL6_CLK2
Y6	—	VSS	—	—	—	—	—	—	—	—
Y7	—	VCC33	—	—	—	—	—	—	—	—
Y8	—	VCC33	—	—	—	—	—	—	—	—
Y9	—	VSS	—	—	—	—	—	—	—	—
Y10	—	VDD18ABG	—	—	—	—	—	—	—	—
Y11	—	NCPOUT	—	—	—	—	—	—	—	—

Table 1.19 List of pins and pin functions (537-pin FBGA) (18 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
Y12	—	VSS_USB	—	—	—	—	—	—	—	—
Y13	—	VSS	—	—	—	—	—	—	—	—
Y14	—	PCIE_VDDA_RX	—	—	—	—	—	—	—	—
Y15	—	PCIE_VDDA_TX	—	—	—	—	—	—	—	—
Y16	—	VSS	—	—	—	—	—	—	—	—
Y17	—	PCIE_VCC18A_CMN	—	—	—	—	—	—	—	—
Y18	—	VSS	—	—	—	—	—	—	—	—
Y19	—	VSS	—	—	—	—	—	—	—	—
Y20	—	VCC18_ADC1	—	—	—	—	—	—	—	—
Y21	—	VCC18_ADC2	—	—	—	—	—	—	—	—
Y22	—	VCC18_OTP	—	—	—	—	—	—	—	—
Y23	—	AVCC18_TSU	—	—	—	—	—	—	—	—
Y24	—	VSS	—	—	—	—	—	—	—	—
Y25	—	VSS	—	—	—	—	—	—	—	—
AA1	—	IRQ08_0	P08_0	A21	MTIOC0A / MTIOC6A / GTIOC4_1A / GTETRGD	SS5#/CTS5#/RTS5# / SCKE6 / ETH0_COL / CANRX1 / SPI_RSPCK3	MDAT32	—	—	ENCIFCK6 / DUEI1 / HDSL6_SEL1
AA2	—	IRQ08_2	P08_2	A19	MTIOC0B / MTIOC6C / GTETRGSB	DE5 / RXDE6 / GMAC0_PTPTRG1 / ESC_LATCH1 / CANTX1 / SPI_SSL32 / SD0_WP	MDAT21	—	—	ENCIFDI6
AA3	—	IRQ08_1	P08_1	A20	GTETRGSA	CTS5# / GMAC0_PTPTRG0 / ESC_LATCH0 / CANTXDP0 / SPI_SSL31 / SD0_CD	—	—	—	TST_OUT1 / HDSL6_MISO1
AA4	—	MDW0 / IRQ08_5	P08_5	A6	—	SCKE3 / SD1_PWEN / NAND_ALE	—	—	HA6	ENCIFCK3 / DUIE0
AA5	—	MDV0 / IRQ09_0	P09_0	WE0#	—	TXDE7 / ETHSW_PTPOUT1 / ESC_SYNC1 / SD0_IOVS	—	—	HWR0#	ENCIFDO7 / DUEI1
AA6	—	IRQ09_3	P09_3	CS0#	MTIOC2A / GTIOC4_3A	SS0#/CTS0#/RST0# / RXDE6 / SCKE4 / ETHSW_LPI0 / ESWM_MPINT0 / SD0_CD / NAND_RY_BY0#	MCLK31	—	HCS0#	ENCIFCK4 / ENCIFDI6 / HDSL6_MOSi1
AA7	—	VSS	—	—	—	—	—	—	—	—
AA8	—	VSS	—	—	—	—	—	—	—	—
AA9	—	VSS	—	—	—	—	—	—	—	—
AA10	—	VSS	—	—	—	—	—	—	—	—
AA11	—	VCC33_USB	—	—	—	—	—	—	—	—
AA12	—	AVCC18_USB	—	—	—	—	—	—	—	—
AA13	—	VSS	—	—	—	—	—	—	—	—
AA14	—	PCIE_VDDA_RX	—	—	—	—	—	—	—	—
AA15	—	PCIE_VDDA_TX	—	—	—	—	—	—	—	—
AA16	—	VSS	—	—	—	—	—	—	—	—
AA17	—	VSS	—	—	—	—	—	—	—	—
AA18	—	VREFH0	—	—	—	—	—	—	—	—
AA19	—	VCC18_ADC0	—	—	—	—	—	—	—	—
AA20	—	VREFH1	—	—	—	—	—	—	—	—
AA21	—	VREFH2	—	—	—	—	—	—	—	—

Table 1.19 List of pins and pin functions (537-pin FBGA) (19 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
AA22	—	VSS	—	—	—	—	—	—	—	—
AA23	—	VSS	—	—	—	—	—	—	—	—
AA24	—	VSS	—	—	—	—	—	—	—	—
AA25	—	VSS	—	—	—	—	—	—	—	—
AB1	—	VSS	—	—	—	—	—	—	—	—
AB2	—	IRQ08_4	P08_4	A17	—	RXD5/SCL5/MISO5 / ETH1_COL / ETHSW_TDMAOUT3 / ESC_LINKACT1 / CANTXDP1	—	—	—	SI1# / HDSL6_SEL2
AB3	—	MDD / IRQ08_7	P08_7	A8	—	DEE7 / SD0_PWEN / NAND_CE0#	—	—	HA8	ENCIFOE7 / SI0#
AB4	—	MDV2 / IRQ09_5	P09_5	A1	—	TXDE3 / TXDE4 / ETHSW_LPI2	—	—	HA1	ENCIFDO3 / ENCIFDO4 / DUEI2
AB5	—	IRQ10_3	P10_3	—	MTIOC6D / GTIOC3_0B	RXD2/SCL2/MISO2	MDAT22	—	—	TST_OUT2
AB6	—	IRQ10_6	P10_6	—	MTIOC7B / GTIOC3_2A / CMTW0_TIC1	CTS2# / SCKE2	—	—	—	ENCIFCK2 / TST_OUT3
AB7	—	IRQ11_2	P11_2	—	GTIOC0_3B	TXD1/SDA1/MOSI1 / IIC_SDA0 / ESC_I2CDATA	—	USB_EXICEN	—	—
AB8	—	IRQ11_3	P11_3	—	POE4# / GTETRGD	RXD0/SCL0/MISO0 / IIC_SCL1	—	—	—	—
AB9	—	TRST#	—	—	—	—	—	—	—	—
AB10	—	VSS	—	—	—	—	—	—	—	—
AB11	—	VSS_USB	—	—	—	—	—	—	—	—
AB12	—	USB_RREF	—	—	—	—	—	—	—	—
AB13	—	VSS	—	—	—	—	—	—	—	—
AB14	—	PCIE_VCC18A	—	—	—	—	—	—	—	—
AB15	—	—	—	—	—	—	—	PCIE_REFCLKN	—	—
AB16	—	VSS	—	—	—	—	—	—	—	—
AB17	—	RES#	—	—	—	—	—	—	—	—
AB18	—	VSS	—	—	—	—	—	—	—	—
AB19	—	VSS	—	—	—	—	—	—	—	—
AB20	—	VSS	—	—	—	—	—	—	—	—
AB21	—	VSS	—	—	—	—	—	—	—	—
AB22	—	—	—	—	—	—	—	AN204	—	—
AB23	—	VSS	—	—	—	—	—	—	—	—
AB24	—	VSS	—	—	—	—	—	—	—	—
AB25	—	VSS	—	—	—	—	—	—	—	—
AC1	—	MDW1 / IRQ08_6	P08_6	A7	—	DEE3 / SD1_IOVS / NAND_CLE	—	—	HA7	ENCIFOE3 / TST_OUT0
AC2	—	MDV1 / IRQ09_1	P09_1	WE1#	—	SCKE7 / NAND_CE1#	—	—	HWR1#	ENCIFCK7 / TST_OUT1
AC3	—	MDV4 / IRQ09_7	P09_7	A3	—	SCKE6 / ETHSW_TDMAOUT1 / ESC_LINKACT1 / ESC_LINKACT2	—	—	HA3	ENCIFCK6 / SI2# / POUTA
AC4	—	IRQ10_5	P10_5	—	MTIOC7C / GTIOC3_1A / GTIOC4_2B / CMTW0_TOC0	SS2#/CTS2#/RTS2# / IIC_SDA2	—	—	—	DUEI3
AC5	—	IRQ10_4	P10_4	—	MTIOC7A / GTIOC3_1B / GTIOC4_2A / CMTW0_TIC0	TXD2/SDA2/MOSI2	—	—	—	SI2#

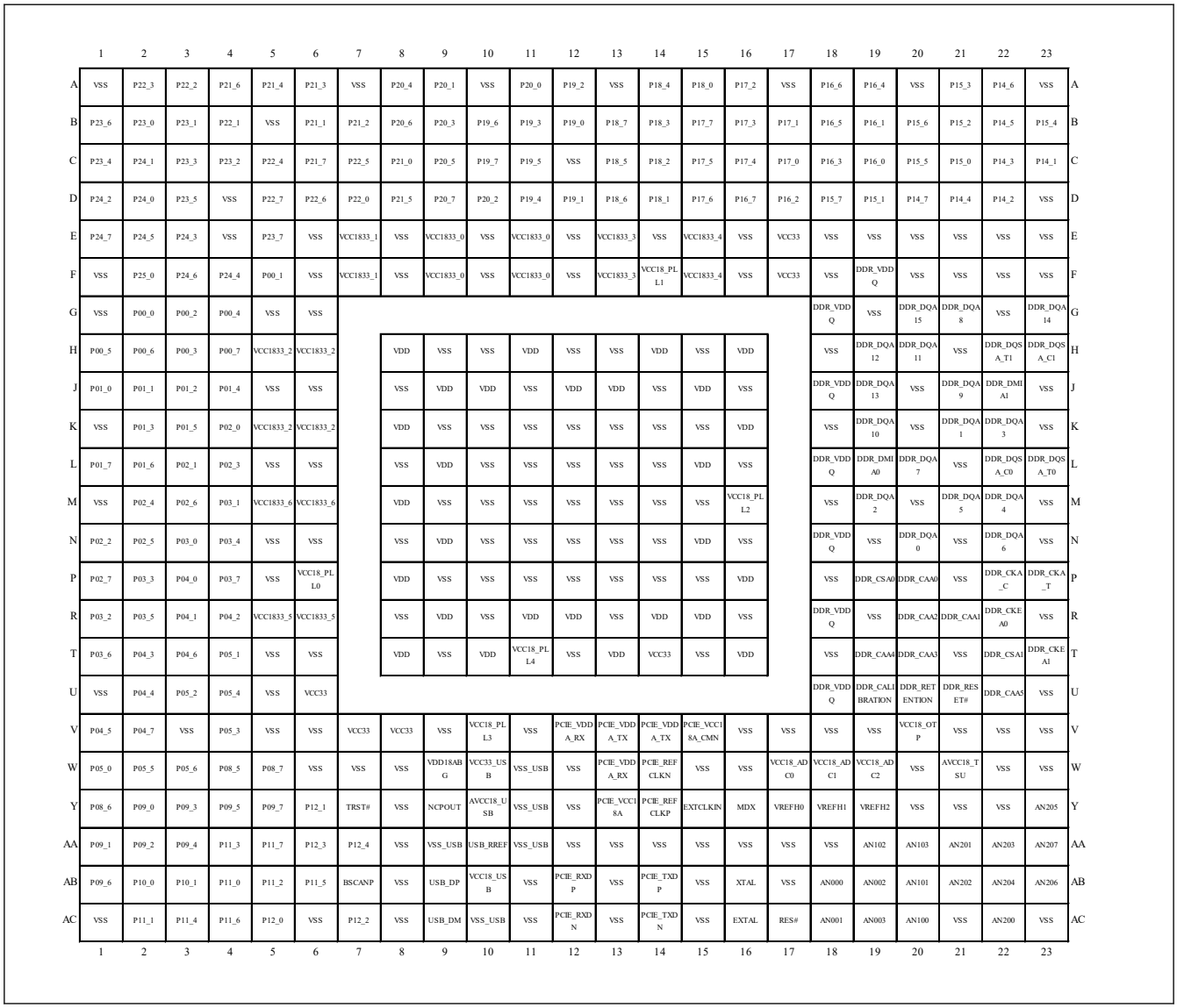
Table 1.19 List of pins and pin functions (537-pin FBGA) (20 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
AC6	—	IRQ10_7	P10_7	—	MTIOC7D / GTIOC3_2B / CMTW0_TOC1	DE2 / DEE2	—	—	—	ENCIFOE2 / SI3#
AC7	—	TMS / IRQ12_0	P12_0	—	—	—	—	—	—	—
AC8	—	IRQ11_7	P11_7	—	POE11# / GTIOC5_2A / GTETRGB / RTCAT1HZ	—	—	USB_OTG_ID	MBX_HINT#	—
AC9	—	IRQ12_4	P12_4	—	—	—	—	USB_VBUSIN	—	—
AC10	—	VSS	—	—	—	—	—	—	—	—
AC11	—	VSS_USB	—	—	—	—	—	—	—	—
AC12	—	VCC18_USB	—	—	—	—	—	—	—	—
AC13	—	VSS_USB	—	—	—	—	—	—	—	—
AC14	—	VSS	—	—	—	—	—	—	—	—
AC15	—	VSS	—	—	—	—	—	—	—	—
AC16	—	—	—	—	—	—	—	PCIE_REFCLKP	—	—
AC17	—	MDX	—	—	—	—	—	—	—	—
AC18	—	EXTCLKIN	—	—	—	—	—	—	—	—
AC19	—	VSS	—	—	—	—	—	—	—	—
AC20	—	—	—	—	—	—	—	AN002	—	—
AC21	—	—	—	—	—	—	—	AN100	—	—
AC22	—	—	—	—	—	—	—	AN102	—	—
AC23	—	—	—	—	—	—	—	AN202	—	—
AC24	—	—	—	—	—	—	—	AN203	—	—
AC25	—	—	—	—	—	—	—	AN207	—	—
AD1	—	IRQ09_2	P09_2	WAIT#	—	SCK0 / RXDE3 / RXDE4 / NAND_RY_BY1#	—	—	HWAIT#	ENCIFDI3 / ENCIFDI4 / SI1# / HDCL6_CLK1
AD2	—	IRQ09_4	P09_4	RD#	MTIOC2B / GTIOC4_3B	CTS0# / RXDE7 / DEE4 / ETHSW_LPI1 / ESWM_MPINT1 / SD0_WP / NAND_RY_BY2#	MDAT31	—	HRD#	ENCIFOE4 / ENCIFDI7
AD3	—	MDV3 / IRQ09_6	P09_6	A2	—	DE0 / TXDE6 / ETHSW_TDMAOUT0 / NAND_CE2#	—	—	HA2	ENCIFDO6 / TST_OUT2
AD4	—	IRQ10_2	P10_2	—	MTIOC1B / MTIOC6B / GTIOC3_0A / GTIOC4_1B	SCK2 / IIC_SCL2	MCLK22	—	—	DUEI2
AD5	—	IRQ11_0	P11_0	—	—	TXDE2	—	USB_VBUSEN	—	ENCIFDO2
AD6	—	IRQ11_1	P11_1	—	GTIOC0_3A	RXD1/SCL1/MISO1 / RXDE2 / IIC_SCL0 / ESC_I2CCLK	—	USB_OVRCUR	—	ENCIFDI2
AD7	—	CKIO / IRQ11_5	P11_5	—	POE0# / GTIOC5_0A / GTETRGA	SCIEXTCLK / IIC_SCL2 / NAND_RY_BY3#	—	—	HCKIO	—
AD8	—	TDI / IRQ12_1	P12_1	—	—	—	—	—	—	—
AD9	—	TDO / IRQ12_3	P12_3	—	—	—	—	—	—	—
AD10	—	VSS	—	—	—	—	—	—	—	—
AD11	—	—	—	—	—	—	—	USB_DP	—	—
AD12	—	VSS_USB	—	—	—	—	—	—	—	—
AD13	—	VSS	—	—	—	—	—	—	—	—
AD14	—	—	—	—	—	—	—	PCIE_RXDP	—	—
AD15	—	VSS	—	—	—	—	—	—	—	—
AD16	—	—	—	—	—	—	—	PCIE_TXDP	—	—

Table 1.19 List of pins and pin functions (537-pin FBGA) (21 of 21)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
AD17	—	VSS	—	—	—	—	—	—	—	—
AD18	—	XTAL	—	—	—	—	—	—	—	—
AD19	—	VSS	—	—	—	—	—	—	—	—
AD20	—	—	—	—	—	—	—	AN001	—	—
AD21	—	—	—	—	—	—	—	AN101	—	—
AD22	—	—	—	—	—	—	—	AN103	—	—
AD23	—	—	—	—	—	—	—	AN200	—	—
AD24	—	—	—	—	—	—	—	AN201	—	—
AD25	—	—	—	—	—	—	—	AN205	—	—
AE1	—	VSS	—	—	—	—	—	—	—	—
AE2	—	MDV5 / IRQ10_0	P10_0	A4	—	DEE6 / ETHSW_TDMAOUT2 / ESC_IRQ / NAND_CE3#	—	—	HA4	ENCIFOE6 / POUTB
AE3	—	MDB / IRQ10_1	P10_1	A5	—	ETHSW_TDMAOUT3 / ESC_RESETOUT# / ESC_LEDRUN	—	—	HA5	POUTZ
AE4	—	VSS	—	—	—	—	—	—	—	—
AE5	—	RSTOUT# / IRQ11_4	P11_4	—	GTETRGSA	TXD0/SDA0/MOSI0 / IIC_SDA1	—	—	—	—
AE6	—	IRQ11_6	P11_6	—	—	IIC_SDA2	—	USB_OVRCUR	—	—
AE7	—	VSS	—	—	—	—	—	—	—	—
AE8	—	TCK / IRQ12_2	P12_2	—	—	—	—	—	—	—
AE9	—	BSCANP	—	—	—	—	—	—	—	—
AE10	—	VSS	—	—	—	—	—	—	—	—
AE11	—	—	—	—	—	—	—	USB_DM	—	—
AE12	—	VSS_USB	—	—	—	—	—	—	—	—
AE13	—	VSS	—	—	—	—	—	—	—	—
AE14	—	—	—	—	—	—	—	PCIE_RXDN	—	—
AE15	—	VSS	—	—	—	—	—	—	—	—
AE16	—	—	—	—	—	—	—	PCIE_TXDN	—	—
AE17	—	VSS	—	—	—	—	—	—	—	—
AE18	—	EXTAL	—	—	—	—	—	—	—	—
AE19	—	VSS	—	—	—	—	—	—	—	—
AE20	—	—	—	—	—	—	—	AN000	—	—
AE21	—	—	—	—	—	—	—	AN003	—	—
AE22	—	VSS	—	—	—	—	—	—	—	—
AE23	—	VSS	—	—	—	—	—	—	—	—
AE24	—	—	—	—	—	—	—	AN206	—	—
AE25	—	VSS	—	—	—	—	—	—	—	—

1.7 FBGA 489 Pin Assignment



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	VSS	P22_3	P22_2	P21_6	P21_4	P21_3	VSS	P20_4	P20_1	VSS	P20_0	P19_2	VSS	P18_4	P18_0	P17_2	VSS	P16_6	P16_4	VSS	P15_3	P14_6	VSS	A
B	P23_6	P23_0	P23_1	P22_1	VSS	P21_1	P21_2	P20_6	P20_3	P19_6	P19_3	P19_0	P18_7	P18_3	P17_7	P17_3	P17_1	P16_5	P16_1	P15_6	P15_2	P14_5	P15_4	B
C	P23_4	P24_1	P23_3	P23_2	P22_4	P21_7	P22_5	P21_0	P20_5	P19_7	P19_5	VSS	P18_5	P18_2	P17_5	P17_4	P17_0	P16_3	P16_0	P15_5	P15_0	P14_3	P14_1	C
D	P24_2	P24_0	P23_5	VSS	P22_7	P22_6	P22_0	P21_5	P20_7	P20_2	P19_4	P19_1	P18_6	P18_1	P17_6	P16_7	P16_2	P15_7	P15_1	P14_7	P14_4	P14_2	VSS	D
E	P24_7	P24_5	P24_3	VSS	P23_7	VSS	VCC1833_1	VSS	VCC1833_0	VSS	VCC1833_0	VSS	VCC1833_3	VSS	VCC1833_4	VSS	VCC33	VSS	VSS	VSS	VSS	VSS	VSS	E
F	VSS	P25_0	P24_6	P24_4	P00_1	VSS	VCC1833_1	VSS	VCC1833_0	VSS	VCC1833_0	VSS	VCC1833_3	VCC18_PLL1	VCC1833_4	VSS	VCC33	VSS	DDR_VDDQ	VSS	VSS	VSS	VSS	F
G	VSS	P00_0	P00_2	P00_4	VSS	VSS												DDR_VDDQ	VSS	DDR_DQA15	DDR_DQA8	VSS	DDR_DQA14	G
H	P00_5	P00_6	P00_3	P00_7	VCC1833_2	VCC1833_2		VDD	VSS	VSS	VDD	VSS	VSS	VDD	VSS	VDD		VSS	DDR_DQA12	DDR_DQA11	VSS	DDR_DQSA_T1	DDR_DQSA_C1	H
J	P01_0	P01_1	P01_2	P01_4	VSS	VSS		VSS	VDD	VDD	VSS	VDD	VDD	VSS	VDD	VSS		DDR_VDDQ	DDR_DQA13	VSS	DDR_DQA9	DDR_DMIA1	VSS	J
K	VSS	P01_3	P01_5	P02_0	VCC1833_2	VCC1833_2		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		VSS	DDR_DQA10	VSS	DDR_DQA1	DDR_DQA3	VSS	K
L	P01_7	P01_6	P02_1	P02_3	VSS	VSS		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		DDR_VDDQ	DDR_DMIA0	DDR_DQA7	VSS	DDR_DQSA_C0	DDR_DQSA_T0	L
M	VSS	P02_4	P02_6	P03_1	VCC1833_6	VCC1833_6		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC18_PLL2		VSS	DDR_DQA2	VSS	DDR_DQA5	DDR_DQA4	VSS	M
N	P02_2	P02_5	P03_0	P03_4	VSS	VSS		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		DDR_VDDQ	VSS	DDR_DQA0	VSS	DDR_DQA6	VSS	N
P	P02_7	P03_3	P04_0	P03_7	VSS	VCC18_PLL0		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		VSS	DDR_CSA0	DDR_CAA0	VSS	DDR_CKA_C	DDR_CKA_T	P
R	P03_2	P03_5	P04_1	P04_2	VCC1833_5	VCC1833_5		VSS	VDD	VSS	VDD	VDD	VSS	VDD	VDD	VSS		DDR_VDDQ	VSS	DDR_CAA2	DDR_CAA1	DDR_CKEA0	VSS	R
T	P03_6	P04_3	P04_6	P05_1	VSS	VSS		VDD	VSS	VDD	VCC18_PLL4	VSS	VDD	VCC33	VSS	VDD		VSS	DDR_CAA4	DDR_CAA3	VSS	DDR_CSA1	DDR_CKEA1	T
U	VSS	P04_4	P05_2	P05_4	VSS	VCC33												DDR_VDDQ	DDR_CALIBRATION	DDR_RETENTION	DDR_RESET#	DDR_CAA5	VSS	U
V	P04_5	P04_7	VSS	P05_3	VSS	VSS	VCC33	VCC33	VSS	VCC18_PLL3	VSS	PCIE_VDDA_RX	PCIE_VDDA_TX	PCIE_VDDA_TX	PCIE_VCC18A_CMN	VSS	VSS	VSS	VSS	VCC18_OTP	VSS	VSS	VSS	V
W	P05_0	P05_5	P05_6	P08_5	P08_7	VSS	VSS	VSS	VDD18ABG	VCC33_USB	VSS_USB	VSS	PCIE_VDDA_RX	PCIE_REFCLKN	VSS	VSS	VCC18_ADC0	VCC18_ADC1	VCC18_ADC2	VSS	AVCC18_TSU	VSS	VSS	W
Y	P08_6	P09_0	P09_3	P09_5	P09_7	P12_1	TRST#	VSS	NCPOUT	AVCC18_USB	VSS_USB	VSS	PCIE_VCC18A	PCIE_REFCLKP	EXTCLKIN	MDX	VREFH0	VREFH1	VREFH2	VSS	VSS	VSS	AN205	Y
AA	P09_1	P09_2	P09_4	P11_3	P11_7	P12_3	P12_4	VSS	VSS_USB	USB_RREF	VSS_USB	VSS	VSS	VSS	VSS	VSS	VSS	VSS	AN102	AN103	AN201	AN203	AN207	AA
AB	P09_6	P10_0	P10_1	P11_0	P11_2	P11_5	BSCANP	VSS	USB_DP	VCC18_USB	VSS	PCIE_RXDP	VSS	PCIE_TXDP	VSS	XTAL	VSS	AN000	AN002	AN101	AN202	AN204	AN206	AB
AC	VSS	P11_1	P11_4	P11_6	P12_0	VSS	P12_2	VSS	USB_DM	VSS_USB	VSS	PCIE_RXDN	VSS	PCIE_TXDN	VSS	EXTAL	RES#	AN001	AN003	AN100	VSS	AN200	VSS	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Figure 1.3 Pin arrangement (489-pin FBGA) (top view)

Table 1.20 List of pins and pin functions (489-pin FBGA) (1 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
A1	—	VSS	—	—	—	—	—	—	—	—
A2	VCC1833_0	IRQ22_3	P22_3	—	GTIOC0_3B	ETH1_RXD3	—	—	—	HDSL6_MOSI1
A3	VCC1833_0	IRQ22_2	P22_2	—	GTIOC0_3A / GTIOC4_5B / GTIOC5_0B	ETH1_RXD2	—	—	—	HDSL6_MISO1
A4	VCC1833_0	IRQ21_6	P21_6	—	—	ETH1_TXEN	—	—	—	HDSL6_LINK
A5	VCC1833_0	IRQ21_4	P21_4	—	—	ETH1_TXD2	—	—	—	HDSL5_MISO2
A6	VCC1833_0	IRQ21_3	P21_3	—	—	ETH1_TXD1	—	—	—	HDSL5_SEL2
A7	—	VSS	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (489-pin FBGA) (2 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
A8	VCC1833_0	MD0 / IRQ20_4	P20_4	—	—	GMAC0_MDC / GMAC1_MDC / GMAC2_MDC / ETHSW_MDC / ESC_MDC / ESWM_MDC / CANTX1	—	—	—	—
A9	VCC1833_0	IRQ20_1	P20_1	—	—	ETH0_RXD2 / CANRXDP0	—	—	—	HDSL4_MISO2
A10	—	VSS	—	—	—	—	—	—	—	—
A11	VCC1833_0	IRQ20_0	P20_0	—	—	ETH0_RXD1 / CANTX0	—	—	—	HDSL4_SEL2
A12	VCC1833_0	IRQ19_2	P19_2	—	—	ETH0_TXD1	—	—	—	HDSL4_SMPL
A13	—	VSS	—	—	—	—	—	—	—	—
A14	VCC1833_3	IRQ18_4	P18_4	—	GTETRGA	DEE4 / ESWM_TASGATE1_5 / XSPI0_IO5	MDAT21	—	—	ENCIFOE4 / HDSL3_MOSI1
A15	VCC1833_3	IRQ18_0	P18_0	—	—	ESWM_TASGATE1_1 / XSPI0_IO1	MCLK02	—	—	HDSL3_SMPL
A16	VCC1833_3	IRQ17_2	P17_2	—	—	SCKE7 / ESWM_TASGATE0_4 / XSPI0_CKP	MCLK30	—	—	ENCIFCK7 / HDSL2_MOSI1
A17	—	VSS	—	—	—	—	—	—	—	—
A18	VCC1833_4	IRQ16_6	P16_6	—	MTCLKC / MTIOC0C / GTIOC3_3A	SCKE3 / IIC_SCL0 / ETH2_TXER / ETH3_TXER / CANRXDP0 / SPI_RSPCK0 / XSPI1_IO4	MCLK30	—	—	ENCIFCK3 / HDSL2_SMPL
A19	VCC1833_4	IRQ16_4	P16_4	—	MTIOC7B / GTIOC3_2A / GTIOC4_2A	RXD4/SCL3/MISO3 / SCKE7 / ETH4_CRS, SPI_MISO0 / XSPI1_IO2	MCLK01	—	—	ENCIFCK7 / HDSL1_MOSI2
A20	—	VSS	—	—	—	—	—	—	—	—
A21	—	IRQ15_3	P15_3	D10	MTIOC1A / MTIOC3C / GTIOC2_4B / CMTW1_TOC0	RXDE2 / SD1_IOVS	—	ADTRG0#	HD10	ENCIFDI2 / HDSL1_LINK
A22	—	IRQ14_6	P14_6	D5	MTIOC1B / MTIOC4B / GTIOC2_2A / CMTW0_TIC0	SD0_PWEN	—	—	HD5	HDSL0_MOSI1 / POUTA
A23	—	VSS	—	—	—	—	—	—	—	—
B1	VCC1833_1	IRQ23_6	P23_6	—	GTIOC4_3A / GTIOC5_3A / RTCAT1HZ	SCK4 / ETH2_RXCLK / ESC_LEDRUN / SD0_CD	MDAT30 / MDAT42	—	—	HDSL7_CLK2
B2	VCC1833_1	IRQ23_0	P23_0	—	GTIOC3_3A / GTIOC4_0A	RXD3/SCL3/MISO3 / ETH2_TXCLK / SPI_RSPCK0	MDAT01	—	—	HDSL7_LINK
B3	VCC1833_1	IRQ23_1	P23_1	—	GTIOC3_3B / GTIOC4_0B	SCK3 / IIC_SCL0 / ETH2_TXD0 / GMAC0_PTPTRG0 / ESC_LATCH0 / CANRXDP1 / SPI_MISO0	MCLK21 / MCLK40	—	—	HDSL7_SMPL
B4	VCC1833_0	IRQ22_1	P22_1	—	GTIOC4_5A / GTIOC5_0A	ETH1_RXD1	—	—	—	HDSL6_SEL1
B5	—	VSS	—	—	—	—	—	—	—	—
B6	VCC1833_0	IRQ21_1	P21_1	—	—	ETH1_TXCLK	—	—	—	HDSL5_MOSI1
B7	VCC1833_0	IRQ21_2	P21_2	—	—	ETH1_TXD0	—	—	—	HDSL5_CLK2
B8	VCC1833_0	IRQ20_6	P20_6	—	—	ETHSW_PHYLINK0 / ESC_PHYLINK0 / ESWM_PHYLINK0 / HPSW_PHYLINK0 / CANRXDP1	—	—	—	HDSL5_CLK1
B9	VCC1833_0	IRQ20_3	P20_3	—	—	ETH0_RXDV	—	—	—	HDSL5_LINK

Table 1.20 List of pins and pin functions (489-pin FBGA) (3 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
B10	VCC1833_0	IRQ19_6	P19_6	—	—	ETH0_RXCLK	—	—	—	HDSL4_MOSI1
B11	VCC1833_0	IRQ19_3	P19_3	—	—	ETH0_TXD2	—	—	—	HDSL4_CLK1
B12	VCC1833_0	IRQ19_0	P19_0	—	—	ETH0_TXCLK	—	—	—	HDSL3_MOSI2
B13	VCC1833_3	IRQ18_7	P18_7	—	—	ESWM_TASGATE1_8 / XSPI0_RESET0#	MCLK30 / MDAT02	—	—	HDSL3_MISO2
B14	VCC1833_3	IRQ18_3	P18_3	—	—	SCKE4 / ESWM_TASGATE1_4 / XSPI0_IO4	MCLK21	—	—	ENCIFCK4 / HDSL3_MISO1
B15	VCC1833_3	IRQ17_7	P17_7	—	—	ESWM_TASGATE1_0 / XSPI0_IO0	MDAT20	—	—	HDSL3_LINK
B16	VCC1833_3	IRQ17_3	P17_3	—	—	DEE7 / ESWM_TASGATE0_5 / XSPI0_CKN	MDAT30	—	—	ENCIFOE7 / HDSL2_CLK2
B17	VCC1833_4	IRQ17_1	P17_1	—	MTIOC0B / MTIOC6C / GTIOC4_4B	RXDE3 / IIC_SDA1 / ETH2_COL / ETH3_COL / CANTX0 / XSPI1_IO7	MDAT31	—	MBX_HINT#	ENCIFDI3 / HDSL2_MISO1
B18	VCC1833_4	IRQ16_5	P16_5	—	MTIOC7D / GTIOC3_2B / GTIOC4_2B	TXD3/SDA3/MOSI3 / DEE7 / ETH4_COL / SPI_MOSI0 / XSPI1_IO3	MDAT01	—	—	ENCIFOE7 / HDSL2_LINK
B19	VCC1833_4	IRQ16_1	P16_1	—	MTIOC6D / GTIOC3_0B / GTIOC4_0B	TXD1/SDA1/MOSI1 / RXDE1 / IIC_SDA2 / ESWM_TASGATE0_3 / XSPI1_DS	MDAT22	—	—	ENCIFDI1 / HDSL1_CLK2
B20	VCC1833_4	IRQ15_6	P15_6	—	GTIOC0_4A	DE1 / TXDE6 / TXDE7 / IIC_SCL1 / ESWM_TASGATE0_0 / XSPI1_CKP	MCLK21	—	—	ENCIFDO6 / ENCIFDO7 / HDSL1_SEL1
B21	—	IRQ15_2	P15_2	D9	MTIOC3A / MTIC5W / GTIOC2_4A / CMTW1_TIC0	TXDE2 / SD1_PWEN	—	—	HD9	ENCIFDO2 / HDSL0_MOSI2
B22	—	IRQ14_5	P14_5	D4	MTIOC4C / MTIC5V / GTIOC0_1A / GTIOC2_1B	RXDE6 / ETH2_COL / ETH3_COL	—	ADTRG2#	HD4	ENCIFDI6 / HDSL0_MISO1
B23	—	IRQ15_4	P15_4	D11	GTIOC2_0A / CMTW1_TIC1	SCKE6 / IIC_SCL0 / ESC_I2CCLK	MCLK20	ADTRG1#	HD11	ENCIFCK6 / HDSL1_SMPL
C1	VCC1833_1	IRQ23_4	P23_4	—	GTIOC4_2A / GTIOC4_3B	CTS3# / ETH2_TXD3 / ETHSW_PTPOUT2 / ESC_SYNC0 / SPI_SSL01	MDAT01 / MDAT41	—	—	HDSL7_MISO1
C2	VCC1833_1	IRQ24_1	P24_1	DACK	POE4# / GTIOC4_4B / CMTW0_TIC0	SS4#/CTS4#/RTS4# / TXDE0 / ETH0_TXER / ETH2_RXD2 / ESC_IRQ / SPI_SSL10 / SD1_WP	MCLK11	—	MBX_HINT#	ENCIFDO0
C3	VCC1833_1	IRQ23_3	P23_3	—	GTIOC4_1B / GTIOC4_3A	SS3#/CTS3#/RTS3# / ETH2_TXD2 / ESC_LINKACT1 / SPI_SSL00	MCLK01 / MCLK41	—	—	HDSL7_SEL1
C4	VCC1833_1	IRQ23_2	P23_2	—	GTIOC4_1A	IIC_SDA0 / ETH2_TXD1 / ESC_LINKACT0 / CANTXDP1 / SPI_MOSI0	MDAT21 / MDAT40	—	—	HDSL7_CLK1
C5	VCC1833_0	IRQ22_4	P22_4	—	GTIOC0_2B	ETH1_RXDV	—	—	—	HDSL6_CLK2
C6	VCC1833_0	IRQ21_7	P21_7	—	GTIOC4_4A	ETH1_RXCLK	—	—	—	HDSL6_SMPL
C7	VCC1833_0	IRQ22_5	P22_5	—	—	ETHSW_PHYLINK1 / ESC_PHYLINK1 / ESWM_PHYLINK1 / HPSW_PHYLINK1	—	—	—	HDSL6_SEL2
C8	VCC1833_0	IRQ21_0	P21_0	—	—	—	—	—	—	HDSL5_MISO1

Table 1.20 List of pins and pin functions (489-pin FBGA) (4 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
C9	VCC1833_0	IRQ20_5	P20_5	—	—	GMAC0_MDIO / GMAC1_MDIO / GMAC2_MDIO / ETHSW_MDIO / ESC_MDIO / ESWM_MDIO / CANRX1	—	—	—	HDSL5_SMPL
C10	VCC1833_0	IRQ19_7	P19_7	—	—	ETH0_RXD0 / CANRX0	—	—	—	HDSL4_CLK2
C11	VCC1833_0	IRQ19_5	P19_5	—	—	ETH0_TXEN	—	—	—	HDSL4_MISO1
C12	—	VSS	—	—	—	—	—	—	—	—
C13	VCC1833_3	IRQ18_5	P18_5	—	GTETRGB	RXDE4 / ESWM_TASGATE1_6 / XSPI0_IO6	MCLK20	—	—	ENCIFDI4 / HDSL3_CLK2
C14	VCC1833_3	IRQ18_2	P18_2	—	—	ESWM_TASGATE1_3 / XSPI0_IO3	MDAT32	—	—	HDSL3_SEL1
C15	VCC1833_3	IRQ17_5	P17_5	—	—	RXDE7 / ESWM_TASGATE0_7 / XSPI0_CS1#	MDAT31	—	—	ENCIFDI7 / HDSL2_MISO2
C16	VCC1833_3	IRQ17_4	P17_4	—	—	TXDE7 / ESWM_TASGATE0_6 / XSPI0_CS0#	MCLK31	—	—	ENCIFDO7 / HDSL2_SEL2
C17	VCC1833_4	IRQ17_0	P17_0	—	MTIOC0A / MTIOC6A / GTIOC3_4A	TXDE3 / IIC_SCL1 / ETH2_CRS / ETH3_CRS / CANRX0 / XSPI1_IO6	MCLK31	USB_VBUSEN	—	ENCIFDO3 / HDSL2_SEL1
C18	VCC1833_4	IRQ16_3	P16_3	—	MTIOC7C / GTIOC3_1A / GTIOC4_1B	TXD5/SDA5/MOSI5 / TXDE4 / ETH4_RXER / SPI_SSL02 / XSPI1_IO1	—	—	—	ENCIFDO4 / HDSL1_MISO2
C19	VCC1833_4	IRQ16_0	P16_0	—	MTIOC1B / MTIOC6B / GTIOC3_0A / GTIOC4_0A	RXD1/SCL1/MISO1 / TXDE1 / IIC_SCL2 / ESWM_TASGATE0_2 / XSPI1_CS1#	MCLK22	—	—	ENCIFDO1 / HDSL1_MOSI1
C20	—	IRQ15_5	P15_5	D12	GTIOC2_0B / CMTW1_TOC1 / RTCAT1HZ	DEE6 / IIC_SDA0 / ESC_I2CDATA	MDAT20	ADTRG2#	HD12	ENCIFDO6 / HDSL1_CLK1
C21	—	IRQ15_0	P15_0	D7	MTCLKA / MTIOC8C / GTIOC2_3A / CMTW0_TIC1	SCKE2 / SD1_CD	—	—	HD7	ENCIFCK2 / HDSL0_SEL2 / POUTZ
C22	—	IRQ14_3	P14_3	D2	POE0# / GTIOC0_2A / GTETRGA / RTCAT1HZ	SCIEXTCLK	—	ADTRG0# / USB_EXICEN	HD2 / MBX_HINT#	HDSL0_CLK1
C23	—	IRQ14_1	P14_1	D0	MTIOC3B / MTIOC8A / GTIOC0_0A / GTIOC2_0A / GTIOC4_6A	SCKE6 / ETH2_TXER / ETH3_TXER	—	USB_VBUSEN	HD0	ENCIFCK6 / HDSL0_LINK
D1	VCC1833_1	IRQ24_2	P24_2	TEND	POE8# / GTIOC4_5A / CMTW0_TOC0	CTS4# / RXDE0 / ETH2_RXD3 / ESC_RESETOUT# / SPI_SSL11	MDAT11	—	—	ENCIFDI0 / HDSL7_MOSI2
D2	VCC1833_1	IRQ24_0	P24_0	DREQ	POE0# / GTIOC4_4A	DEE0 / IIC_SDA1 / ETH0_CRS / ETH2_RXD1 / ESC_LINKACT2 / SPI_SSL13 / SD1_CD	MDAT10 / MDAT32	—	—	ENCIFOE0 / HDSL7_MISO2
D3	VCC1833_1	IRQ23_5	P23_5	—	GTIOC4_2B	DE3 / ETH2_TXEN / ESC_LEDERR / SPI_SSL02	MCLK30 / MCLK42	—	—	HDSL7_MOSI1
D4	—	VSS	—	—	—	—	—	—	—	—
D5	VCC1833_0	IRQ22_7	P22_7	—	—	—	—	—	—	HDSL6_MOSI2
D6	VCC1833_0	ETH1_REFCLK / RMII1_REFCLK / IRQ22_6	P22_6	—	—	—	—	—	—	HDSL6_MISO2
D7	VCC1833_0	IRQ22_0	P22_0	—	GTIOC4_4B	ETH1_RXD0	—	—	—	HDSL6_CLK1
D8	VCC1833_0	IRQ21_5	P21_5	—	—	ETH1_TXD3	—	—	—	HDSL5_MOSI2

Table 1.20 List of pins and pin functions (489-pin FBGA) (5 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
D9	VCC1833_0	ETH0_REFCLK / RMII0_REFCLK / IRQ20_7	P20_7	—	—	CANTXDP1	—	—	—	HDSL5_SEL1
D10	VCC1833_0	IRQ20_2	P20_2	—	—	ETH0_RXD3 / CANTXDP0	—	—	—	HDSL4_MOSI2
D11	VCC1833_0	IRQ19_4	P19_4	—	—	ETH0_TXD3	—	—	—	HDSL4_SEL1
D12	VCC1833_0	IRQ19_1	P19_1	—	—	ETH0_TXD0	—	—	—	HDSL4_LINK
D13	VCC1833_3	IRQ18_6	P18_6	—	GTETRGC	TXDE4 / ESWM_TASGATE1_7 / XSPI0_IO7	MDAT20	—	—	ENCIFDO4 / HDSL3_SEL2
D14	VCC1833_3	IRQ18_1	P18_1	—	—	ESWM_TASGATE1_2 / XSPI0_IO2	MCLK32	—	—	HDSL3_CLK1
D15	VCC1833_3	IRQ17_6	P17_6	—	—	ESWM_TASGATE0_8 / XSPI0_DS	MCLK20	—	—	HDSL2_MOSI2
D16	VCC1833_4	IRQ16_7	P16_7	—	MTCLKD / MTIOC0D / GTIOC3_3B	DEE3 / IIC_SDA0 / ETH2_RXER / ETH3_RXER / CANTXDP0 / SPI_SSL00 / XSPI1_IO5	MDAT30	—	—	ENCIFOE3 / HDSL2_CLK1
D17	VCC1833_4	IRQ16_2	P16_2	—	MTIOC7A / GTIOC3_1B / GTIOC4_1A	RXD5/SCL5/MISO5 / RXDE4 / ETH4_TXER / SPI_SSL01 / XSPI1_IO0	—	—	—	ENCIFDI4 / HDSL1_SEL2
D18	VCC1833_4	IRQ15_7	P15_7	—	GTIOC0_4B	DE3 / RXDE6 / RXDE7 / IIC_SDA1 / ESWM_TASGATE0_1 / XSPI1_CS0#	MDAT21	—	—	ENCIFDI6 / ENCIFDI7 / HDSL1_MISO1
D19	—	IRQ15_1	P15_1	D8	MTCLKB / MTIOC8D / GTIOC2_3B / CMTW0_TOC1	DEE2 / SD1_WP	—	—	HD8	ENCIFOE2 / HDSL0_MISO2
D20	—	IRQ14_7	P14_7	D6	MTIOC1A / MTIOC4D / GTIOC2_2B / CMTW0_TOC0	SD0_IOVS	—	—	HD6	HDSL0_CLK2 / POUTB
D21	—	IRQ14_4	P14_4	D3	MTIOC4A / MTIC5U / GTIOC0_1B / GTIOC2_1A	TXDE6 / ETH2_CRS / ETH3_CRS	—	ADTRG1#	HD3	ENCIFDO6 / HDSL0_SEL1
D22	—	IRQ14_2	P14_2	D1	MTIOC3D / MTIOC8B / GTIOC0_0B / GTIOC2_0B / GTIOC4_6B	DEE6 / ETH2_RXER / ETH3_RXER	—	USB_OVRCUR	HD1	ENCIFOE6 / HDSL0_SMPL
D23	—	VSS	—	—	—	—	—	—	—	—
E1	VCC1833_1	IRQ24_7	P24_7	—	—	TXD3/SDA3/MOSI3 / GMAC0_MDIO / GMAC1_MDIO / GMAC2_MDIO / ETHSW_MDIO / ESC_MDIO / ESWM_MDIO / CANRX1 / SPI_RSPCK1	—	—	—	—
E2	VCC1833_1	IRQ24_5	P24_5	—	POE10# / GTIOC4_6B / GTETRGA	TXD4/SDA4/MOSI4 / SCIEXTCLK	MDAT22	PCIE_RSTOUTB	—	HDSL0_CLK1
E3	VCC1833_1	IRQ24_3	P24_3	—	GTIOC4_5B / CMTW0_TIC1	RXD5/SDA5/MOSI5 / IIC_SCL1 / ETH0_RXER / ETH2_RXDV / ESC_I2CCLK / SPI_MOSI1 / SD0_PWEN	MDAT12	—	—	HDSL0_LINK
E4	—	VSS	—	—	—	—	—	—	—	—
E5	VCC1833_1	IRQ23_7	P23_7	—	GTIOC4_3B / GTIOC5_3B	SCKE0 / IIC_SCL1 / ETH0_COL / ETH2_RXD0 / SPI_SSL12 / SD0_WP	MCLK10 / MCLK32	—	—	ENCIFCK0 / HDSL7_SEL2

Table 1.20 List of pins and pin functions (489-pin FBGA) (6 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
E6	—	VSS	—	—	—	—	—	—	—	—
E7	—	VCC1833_1	—	—	—	—	—	—	—	—
E8	—	VSS	—	—	—	—	—	—	—	—
E9	—	VCC1833_0	—	—	—	—	—	—	—	—
E10	—	VSS	—	—	—	—	—	—	—	—
E11	—	VCC1833_0	—	—	—	—	—	—	—	—
E12	—	VSS	—	—	—	—	—	—	—	—
E13	—	VCC1833_3	—	—	—	—	—	—	—	—
E14	—	VSS	—	—	—	—	—	—	—	—
E15	—	VCC1833_4	—	—	—	—	—	—	—	—
E16	—	VSS	—	—	—	—	—	—	—	—
E17	—	VCC33	—	—	—	—	—	—	—	—
E18	—	VSS	—	—	—	—	—	—	—	—
E19	—	VSS	—	—	—	—	—	—	—	—
E20	—	VSS	—	—	—	—	—	—	—	—
E21	—	VSS	—	—	—	—	—	—	—	—
E22	—	VSS	—	—	—	—	—	—	—	—
E23	—	VSS	—	—	—	—	—	—	—	—
F1	—	VSS	—	—	—	—	—	—	—	—
F2	VCC1833_1	IRQ25_0	P25_0	—	—	RXD1/SCL1/MISO1 / RXD3/SCL3/MISO3 / ETHSW_PHYLINK2 / ESC_PHYLINK2 / CANTX1 / SPI_SSL03	MCLK22	—	—	—
F3	VCC1833_1	MD1 / IRQ24_6	P24_6	—	—	DE5 / GMAC0_MDC / GMAC1_MDC / GMAC2_MDC / ETHSW_MDC / ESC_MDC / ESWM_MDC	—	—	—	—
F4	VCC1833_1	ETH2_REFCLK / RMII2_REFCLK / IRQ24_4	P24_4	—	POE11# / GTIOC4_6A / CMTW0_TOC1	RXD5/SCL5/MISO5 / IIC_SDA1 / ETH1_RXER / ESC_I2CDATA / SPI_MISO1 / SD0_IOVS	MCLK12	—	—	HDSL0_SMPL
F5	VCC1833_2	IRQ00_1	P00_1	A17	MTIOC3D / GTIOC0_0B / GTADSM0_1	DEE1 / IIC_SCL2 / ETH3_TXD0 / CANRX0 / SPI_MISO2	—	—	HA17	ENCIFOE1 / HDSL0_MISO1
F6	—	VSS	—	—	—	—	—	—	—	—
F7	—	VCC1833_1	—	—	—	—	—	—	—	—
F8	—	VSS	—	—	—	—	—	—	—	—
F9	—	VCC1833_0	—	—	—	—	—	—	—	—
F10	—	VSS	—	—	—	—	—	—	—	—
F11	—	VCC1833_0	—	—	—	—	—	—	—	—
F12	—	VSS	—	—	—	—	—	—	—	—
F13	—	VCC1833_3	—	—	—	—	—	—	—	—
F14	—	VCC18_PLL1	—	—	—	—	—	—	—	—
F15	—	VCC1833_4	—	—	—	—	—	—	—	—
F16	—	VSS	—	—	—	—	—	—	—	—
F17	—	VCC33	—	—	—	—	—	—	—	—
F18	—	VSS	—	—	—	—	—	—	—	—
F19	—	DDR_VDDQ	—	—	—	—	—	—	—	—
F20	—	VSS	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (489-pin FBGA) (7 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
F21	—	VSS	—	—	—	—	—	—	—	—
F22	—	VSS	—	—	—	—	—	—	—	—
F23	—	VSS	—	—	—	—	—	—	—	—
G1	—	VSS	—	—	—	—	—	—	—	—
G2	VCC1833_2	IRQ00_0	P00_0	A16	MTIOC3B / GTIOC0_0A / GTADSM0_0	SCKE1 / ETH3_TXCLK / SPI_RSPCK2	—	—	HA16	ENCIFCK1 / HDSL0_SEL1
G3	VCC1833_2	IRQ00_2	P00_2	A18	MTIOC4A / GTIOC0_1B / GTADSM1_0	TXDE1 / IIC_SDA2 / ETH3_TXD1 / CANTX0 / SPI_MOSI2	MCLK41	—	HA18	ENCIFDO1 / HDSL0_MOSI1
G4	VCC1833_2	IRQ00_4	P00_4	A20	MITOC4B / GTIOC0_2A / GTADSM2_0	TXDE6 / ETH3_TXD3 / CANTXDP0 / SPI_SSL21	MCLK20	—	HA20	ENCIFDO6 / HDSL0_SEL2
G5	—	VSS	—	—	—	—	—	—	—	—
G6	—	VSS	—	—	—	—	—	—	—	—
G7	—	—	—	—	—	—	—	—	—	—
G8	—	—	—	—	—	—	—	—	—	—
G9	—	—	—	—	—	—	—	—	—	—
G10	—	—	—	—	—	—	—	—	—	—
G11	—	—	—	—	—	—	—	—	—	—
G12	—	—	—	—	—	—	—	—	—	—
G13	—	—	—	—	—	—	—	—	—	—
G14	—	—	—	—	—	—	—	—	—	—
G15	—	—	—	—	—	—	—	—	—	—
G16	—	—	—	—	—	—	—	—	—	—
G17	—	—	—	—	—	—	—	—	—	—
G18	—	DDR_VDDQ	—	—	—	—	—	—	—	—
G19	—	VSS	—	—	—	—	—	—	—	—
G20	—	—	—	—	—	—	—	DDR_DQA15	—	—
G21	—	—	—	—	—	—	—	DDR_DQA8	—	—
G22	—	VSS	—	—	—	—	—	—	—	—
G23	—	—	—	—	—	—	—	DDR_DQA14	—	—
H1	VCC1833_2	IRQ00_5	P00_5	A21	MTIOC4D / MTIOC8C / GTIOC0_2B / GTADSM2_1	RXDE6 / ETH3_TXEN / SPI_SSL22	MDAT20	—	HA21	ENCIFDI6 / HDSL0_MISO2
H2	VCC1833_2	IRQ00_6	P00_6	A22	MTCLKA / MTIOC8D / GTIOC0_3A / GTADSM3_0	RXD4/SCL4/MISO4 / SCKE0 / SCKE6 / ETH3_RXCLK / SPI_SSL23	—	—	MBX_HINT#	ENCIFCK0 / ENCIFCK6
H3	VCC1833_2	IRQ00_3	P00_3	A19	MTIOC4C / GTIOC0_1A / GTADSM1_1	RXDE1 / ETH3_TXD2 / CANRXDP0 / SPI_SSL20	MDAT41	—	HA19	ENCIFDI1 / HDSL0_CLK2
H4	VCC1833_2	IRQ00_7	P00_7	A23	MTCLKB / MTIOC1B / GTIOC0_3B / GTADSM3_1	TXD4/SDA4/MOSI4 / DEE0 / DEE6 / ETH3_RXD0 / SPI_SSL22	—	—	HERROUT#	ENCIFOE0 / ENCIFOE6
H5	—	VCC1833_2	—	—	—	—	—	—	—	—
H6	—	VCC1833_2	—	—	—	—	—	—	—	—
H7	—	—	—	—	—	—	—	—	—	—
H8	—	VDD	—	—	—	—	—	—	—	—
H9	—	VSS	—	—	—	—	—	—	—	—
H10	—	VSS	—	—	—	—	—	—	—	—
H11	—	VDD	—	—	—	—	—	—	—	—
H12	—	VSS	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (489-pin FBGA) (8 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
H13	—	VSS	—	—	—	—	—	—	—	—
H14	—	VDD	—	—	—	—	—	—	—	—
H15	—	VSS	—	—	—	—	—	—	—	—
H16	—	VDD	—	—	—	—	—	—	—	—
H17	—	—	—	—	—	—	—	—	—	—
H18	—	VSS	—	—	—	—	—	—	—	—
H19	—	—	—	—	—	—	—	DDR_DQA12	—	—
H20	—	—	—	—	—	—	—	DDR_DQA11	—	—
H21	—	VSS	—	—	—	—	—	—	—	—
H22	—	—	—	—	—	—	—	DDR_DQSA_T1	—	—
H23	—	—	—	—	—	—	—	DDR_DQSA_C1	—	—
J1	VCC1833_2	IRQ01_0	P01_0	A0	MTIOC1A / MTIOC3A / GTIOC0_4A / GTADSM4_0_	DE4 / TXDE0 / ETH3_RXD1 / SPI_SSL21	—	—	HA0	ENCIFDO0
J2	VCC1833_2	IRQ01_1	P01_1	RD/WR#	MITOC3C / MTIOC8A / GTIOC0_4B / GTADSM4_1	SCK5 / RXD5/SCL5/ MISO5 / RXDE0 / ETH3_RXD2 / SD1_PWEN	—	USB_OVRCUR	HWRSTB#	ENCIFDI0
J3	VCC1833_2	IRQ01_2	P01_2	BS# / DREQ	—	SS5#/CTS5#/RST5# / TXD5/SDA5/MOSI5 / SCKE4 / ETH3_RXD3 / SPI_MOSI2 / SD1_IOVS	MCLK00	ADTRG0#	HBS#	ENCIFCK4
J4	VCC1833_2	ETH3_REFCLK / RMII3_REFCLK / IRQ01_4	P01_4	CS5# / TEND	—	TXD1/SDA1/MOSI1 / RXDE4 / IIC_SDA1 / ETH1_RXER / ETH1_CRS / ESC_I2CDATA / SPI_RSPCK2	MCLK01	USB_EXICEN / ADTRG2#	—	ENCIFDI4
J5	—	VSS	—	—	—	—	—	—	—	—
J6	—	VSS	—	—	—	—	—	—	—	—
J7	—	—	—	—	—	—	—	—	—	—
J8	—	VSS	—	—	—	—	—	—	—	—
J9	—	VDD	—	—	—	—	—	—	—	—
J10	—	VDD	—	—	—	—	—	—	—	—
J11	—	VSS	—	—	—	—	—	—	—	—
J12	—	VDD	—	—	—	—	—	—	—	—
J13	—	VDD	—	—	—	—	—	—	—	—
J14	—	VSS	—	—	—	—	—	—	—	—
J15	—	VDD	—	—	—	—	—	—	—	—
J16	—	VSS	—	—	—	—	—	—	—	—
J17	—	—	—	—	—	—	—	—	—	—
J18	—	DDR_VDDQ	—	—	—	—	—	—	—	—
J19	—	—	—	—	—	—	—	DDR_DQA13	—	—
J20	—	VSS	—	—	—	—	—	—	—	—
J21	—	—	—	—	—	—	—	DDR_DQA9	—	—
J22	—	—	—	—	—	—	—	DDR_DMIA1	—	—
J23	—	VSS	—	—	—	—	—	—	—	—
K1	—	VSS	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (489-pin FBGA) (9 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
K2	VCC1833_2	IRQ01_3	P01_3	CS3# / DACK	—	CTS5# / RXD1/ SCL1/MISO1/ DEE4 / IIC_SCL1 / ETH1_TXER / ETH3_RXDV / ESC_I2CCLK / SPI_MISO2	MDAT00	ADTRG1#	MBX_HINT#	ENCIFOE4
K3	VCC1833_2	IRQ01_5	P01_5	CS2# / DREQ	—	TXDE4 / ETH1_COL / ETH3_TXER / ESC_RESETOUT# / ESWM_PHYLINK0 / HPSW_PHYLINK0 / SPI_SSL20	MDAT01	USB_EXICEN	HCS1#	ENCIFDO4
K4	VCC1833_2	IRQ02_0	P02_0	WE2#	MTIC5V / MTIOC7A / GTIOC1_1B / GTADSM1_0 / GTETRGD	TXD1/SDA1/MOSI1 / SCIEXTCLK / ETH4_TXD1 / ETHSW_PTPOUT0 / ESC_SYNC0 / SPI_MOSI3 / SD1_PWEN	—	—	HWR2#	—
K5	—	VCC1833_2	—	—	—	—	—	—	—	—
K6	—	VCC1833_2	—	—	—	—	—	—	—	—
K7	—	—	—	—	—	—	—	—	—	—
K8	—	VDD	—	—	—	—	—	—	—	—
K9	—	VSS	—	—	—	—	—	—	—	—
K10	—	VSS	—	—	—	—	—	—	—	—
K11	—	VSS	—	—	—	—	—	—	—	—
K12	—	VSS	—	—	—	—	—	—	—	—
K13	—	VSS	—	—	—	—	—	—	—	—
K14	—	VSS	—	—	—	—	—	—	—	—
K15	—	VSS	—	—	—	—	—	—	—	—
K16	—	VDD	—	—	—	—	—	—	—	—
K17	—	—	—	—	—	—	—	—	—	—
K18	—	VSS	—	—	—	—	—	—	—	—
K19	—	—	—	—	—	—	—	DDR_DQA10	—	—
K20	—	VSS	—	—	—	—	—	—	—	—
K21	—	—	—	—	—	—	—	DDR_DQA1	—	—
K22	—	—	—	—	—	—	—	DDR_DQA3	—	—
K23	—	VSS	—	—	—	—	—	—	—	—
L1	VCC1833_2	IRQ01_7	P01_7	D14	MTIC5U / MTIOC6D / GTIOC1_0B / GTADSM0_1 / GTETRGC / CMTW1_TOC0	RXD1/SCL1/MISO1 / ETH1_RXER / ETH4_TXD0 / SPI_MISO3 / SD1_WP	MDAT02	—	HD14	—
L2	VCC1833_2	IRQ01_6	P01_6	D13	MTIOC6B / MTIOC8B / GTIOC1_0A / GTADSM0_0 / GTETRGB / CMTW1_TIC0	SCK1 / ETH0_RXER / ETH4_TXCLK / SPI_RSPCK3 / SD1_CD	MCLK02	—	HD13	—
L3	VCC1833_2	IRQ02_1	P02_1	WE3#/AH#	MTIC5W / MTIOC7C / GTIOC1_1A / GTADSM1_1	SS1#/CTS1#/RTS1# / RXD3/SCL3/MISO3 / TXDE5 / ETH4_TXD2 / GMAC0_PTPTRG0 / ESC_LATCH0 / SPI_SSL30 / SPI_SSL00	—	—	HWR3#	ENCIFDO5
L4	VCC1833_2	IRQ02_3	P02_3	A9	MTIOC0B / MTIOC7D / GTIOC1_2B / GTADSM2_1	DE1 / ETH4_TXEN / GMAC1_PTPTRG0 / ESC_LEDERR / SPI_SSL02 / SPI_SSL32 / SD1_IOVS	—	—	HA9	—

Table 1.20 List of pins and pin functions (489-pin FBGA) (10 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
L5	—	VSS	—	—	—	—	—	—	—	—
L6	—	VSS	—	—	—	—	—	—	—	—
L7	—	—	—	—	—	—	—	—	—	—
L8	—	VSS	—	—	—	—	—	—	—	—
L9	—	VDD	—	—	—	—	—	—	—	—
L10	—	VSS	—	—	—	—	—	—	—	—
L11	—	VSS	—	—	—	—	—	—	—	—
L12	—	VSS	—	—	—	—	—	—	—	—
L13	—	VSS	—	—	—	—	—	—	—	—
L14	—	VSS	—	—	—	—	—	—	—	—
L15	—	VDD	—	—	—	—	—	—	—	—
L16	—	VSS	—	—	—	—	—	—	—	—
L17	—	—	—	—	—	—	—	—	—	—
L18	—	DDR_VDDQ	—	—	—	—	—	—	—	—
L19	—	—	—	—	—	—	—	DDR_DMIA0	—	—
L20	—	—	—	—	—	—	—	DDR_DQA7	—	—
L21	—	VSS	—	—	—	—	—	—	—	—
L22	—	—	—	—	—	—	—	DDR_DQSA_C0	—	—
L23	—	—	—	—	—	—	—	DDR_DQSA_T0	—	—
M1	—	VSS	—	—	—	—	—	—	—	—
M2	VCC1833_2	IRQ02_4	P02_4	A10	MTCLKC / MTIOC0C / GTIOC1_3A / GTADSM3_0	SCK2/ SCKE1 / ETH4_RXCLK / GMAC1_PTPTRG1 / SPI_SSL03 / SPI_SSL33	MCLK12 / MCLK40	—	HA10	ENCIFCK1
M3	VCC1833_2	IRQ02_6	P02_6	A12	MTIOC1A / MTIOC6A / GTIOC1_4A / GTADSM4_0	TXD2/SDA2/MOSI2 / TXDE1 / ETH4_RXD1 / GMAC2_PTPTRG0 / ESC_LEDSTER / SPI_SSL31	MCLK11 / MCLK42	—	HA12	ENCIFDO1
M4	VCC1833_2	IRQ03_1	P03_1	A15	GTIOC3_3B	DE2 / DEE5 / IIC_SDA2 / ETH0_CRS / ETH4_RXDV / ETHSW_PTPOUT3 / ESC_SYNC1 / SPI_MISO3	MDAT10	—	HA15	ENCIFOE5 / SI3# / HDSL1_LINK
M5	—	VCC1833_6	—	—	—	—	—	—	—	—
M6	—	VCC1833_6	—	—	—	—	—	—	—	—
M7	—	—	—	—	—	—	—	—	—	—
M8	—	VDD	—	—	—	—	—	—	—	—
M9	—	VSS	—	—	—	—	—	—	—	—
M10	—	VSS	—	—	—	—	—	—	—	—
M11	—	VSS	—	—	—	—	—	—	—	—
M12	—	VSS	—	—	—	—	—	—	—	—
M13	—	VSS	—	—	—	—	—	—	—	—
M14	—	VSS	—	—	—	—	—	—	—	—
M15	—	VSS	—	—	—	—	—	—	—	—
M16	—	VCC18_PLL2	—	—	—	—	—	—	—	—
M17	—	—	—	—	—	—	—	—	—	—
M18	—	VSS	—	—	—	—	—	—	—	—
M19	—	—	—	—	—	—	—	DDR_DQA2	—	—
M20	—	VSS	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (489-pin FBGA) (11 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
M21	—	—	—	—	—	—	—	DDR_DQA5	—	—
M22	—	—	—	—	—	—	—	DDR_DQA4	—	—
M23	—	VSS	—	—	—	—	—	—	—	—
N1	VCC1833_2	IRQ02_2	P02_2	D15	MTIOC0A / MTIOC7B / GTIOC1_2A / GTADSM2_0	CTS1# / ETH4_TXD3 / GMAC0_PTPTRG1 / ESC_LEDRUN / ESC_LATCH1 / SPI_SSL01 / SPI_SSL31 / SD1_PWEN	—	—	HD15	—
N2	VCC1833_2	IRQ02_5	P02_5	A11	MTCLKD / MTIOC0D / GTIOC1_3B / GTADSM3_1	RXD2/SCL2/MISO2 / DEE1 / ETH4_RXD0 / GMAC2_PTPTRG1 / SPI_SSL32	MDAT12/ MDAT40	—	HA11	ENCIFOE1
N3	VCC1833_2	IRQ03_0	P03_0	A14	GTIOC3_3A	CTS2# / SCKE5 / IIC_SCL2 / ETH0_COL / ETH4_RXD3 / SPI_MOSI3	MCLK10	—	HA14	ENCIFCK5 / TST_OUT3 / HDSL0_MOSI2
N4	VCC1833_2	ETH4_REFCLK / RMII4_REFCLK / IRQ03_4	P03_4	A24	GTETRGSA	TXDE5 / ESC_RESETOUT# / SPI_MOSI0 / SPI_RSPCK3 / SD1_CD	MCLK11	—	—	ENCIFDO5
N5	—	VSS	—	—	—	—	—	—	—	—
N6	—	VSS	—	—	—	—	—	—	—	—
N7	—	—	—	—	—	—	—	—	—	—
N8	—	VSS	—	—	—	—	—	—	—	—
N9	—	VDD	—	—	—	—	—	—	—	—
N10	—	VSS	—	—	—	—	—	—	—	—
N11	—	VSS	—	—	—	—	—	—	—	—
N12	—	VSS	—	—	—	—	—	—	—	—
N13	—	VSS	—	—	—	—	—	—	—	—
N14	—	VSS	—	—	—	—	—	—	—	—
N15	—	VDD	—	—	—	—	—	—	—	—
N16	—	VSS	—	—	—	—	—	—	—	—
N17	—	—	—	—	—	—	—	—	—	—
N18	—	DDR_VDDQ	—	—	—	—	—	—	—	—
N19	—	VSS	—	—	—	—	—	—	—	—
N20	—	—	—	—	—	—	—	DDR_DQA0	—	—
N21	—	VSS	—	—	—	—	—	—	—	—
N22	—	—	—	—	—	—	—	DDR_DQA6	—	—
N23	—	VSS	—	—	—	—	—	—	—	—
P1	VCC1833_2	IRQ02_7	P02_7	A13	MTIOC1B / MTIOC6C / GTIOC1_4B / GTADSM4_1	SS2#/CTS2#/RTS2# / RXDE1 / ETH4_RXD2	MDAT11 / MDAT42	—	HA13	ENCIFDI1 / DUEI3
P2	VCC1833_2	IRQ03_3	P03_3	TEND	CMTW1_TIC1	TXD1/SDA1/MOSI1 / TXD3/SDA3/MOSI3 / GMAC0_MDIO / GMAC1_MDIO / GMAC2_MDIO / ETHSW_MDIO / ESC_MDIO / ESWM_MDIO / ESC_LINKACT0 / SD1_PWEN	—	—	—	—
P3	VCC1833_6	IRQ04_0	P04_0	—	GTIOC1_1B	TXD0/SDA0/MOSI0 / SCKE1 / IIC_SDA0 / SD1_DATA0	MCLK00 / MCLK30	—	—	ENCIFCK1 / SI4# / HDSL1_SEL1

Table 1.20 List of pins and pin functions (489-pin FBGA) (12 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
P4	VCC1833_6	IRQ03_7	P03_7	—	GTIOC1_0B	RXD0/SCL0/MISO0 / DEE0 / IIC_SCL0 / SD1_CMD	MDAT02 / MDAT32	—	—	ENCIFOE0 / TST_OUT4 / HDSL1_CLK1
P5	—	VSS	—	—	—	—	—	—	—	—
P6	—	VCC18_PLL0	—	—	—	—	—	—	—	—
P7	—	—	—	—	—	—	—	—	—	—
P8	—	VDD	—	—	—	—	—	—	—	—
P9	—	VSS	—	—	—	—	—	—	—	—
P10	—	VSS	—	—	—	—	—	—	—	—
P11	—	VSS	—	—	—	—	—	—	—	—
P12	—	VSS	—	—	—	—	—	—	—	—
P13	—	VSS	—	—	—	—	—	—	—	—
P14	—	VSS	—	—	—	—	—	—	—	—
P15	—	VSS	—	—	—	—	—	—	—	—
P16	—	VDD	—	—	—	—	—	—	—	—
P17	—	—	—	—	—	—	—	—	—	—
P18	—	VSS	—	—	—	—	—	—	—	—
P19	—	—	—	—	—	—	—	DDR_CSA0	—	—
P20	—	—	—	—	—	—	—	DDR_CAA0	—	—
P21	—	VSS	—	—	—	—	—	—	—	—
P22	—	—	—	—	—	—	—	DDR_CKA_C	—	—
P23	—	—	—	—	—	—	—	DDR_CKA_T	—	—
R1	VCC1833_2	MD2 / IRQ03_2	P03_2	DACK	CMTW1_TOC1 / RTCAT1HZ	DE2 / TXDE4 / ETH0_TXER / GMAC0_MDC / GMAC1_MDC / GMAC2_MDC / ETHSW_MDC / ESC_MDC / ESWM_MDC / SD1_IOVS	—	—	—	ENCIFDO4
R2	VCC1833_2	IRQ03_5	P03_5	A25	GTETRGSB	RXD3/SCL3/MISO3 / RXDE5 / ETH4_RXER / ESWM_PHYLINK1 / HPSW_PHYLINK1 / SPI_MISO0 / SPI_SSL30 / SD1_WP	MDAT11 / MCLK30	—	—	ENCIFDI5
R3	VCC1833_6	IRQ04_1	P04_1	—	GTIOC1_1A	SS0#/CTS0#/RST0# / DEE1 / SD1_DATA1	MDAT00 / MDAT30	—	—	ENCIFOE1 / DUEI5 / HDSL1_MISO1
R4	VCC1833_6	IRQ04_2	P04_2	—	GTIOC1_2A	CTS0# / TXDE2 / SD1_DATA2	MCLK01 / MCLK31	—	—	ENCIFDO2 / TST_OUT5 / HDSL1_MOSI1
R5	—	VCC1833_5	—	—	—	—	—	—	—	—
R6	—	VCC1833_5	—	—	—	—	—	—	—	—
R7	—	—	—	—	—	—	—	—	—	—
R8	—	VSS	—	—	—	—	—	—	—	—
R9	—	VDD	—	—	—	—	—	—	—	—
R10	—	VSS	—	—	—	—	—	—	—	—
R11	—	VDD	—	—	—	—	—	—	—	—
R12	—	VDD	—	—	—	—	—	—	—	—
R13	—	VSS	—	—	—	—	—	—	—	—
R14	—	VDD	—	—	—	—	—	—	—	—
R15	—	VDD	—	—	—	—	—	—	—	—
R16	—	VSS	—	—	—	—	—	—	—	—
R17	—	—	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (489-pin FBGA) (13 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
R18	—	DDR_VDDQ	—	—	—	—	—	—	—	—
R19	—	VSS	—	—	—	—	—	—	—	—
R20	—	—	—	—	—	—	—	DDR_CAA2	—	—
R21	—	—	—	—	—	—	—	DDR_CAA1	—	—
R22	—	—	—	—	—	—	—	DDR_CKEA0	—	—
R23	—	VSS	—	—	—	—	—	—	—	—
T1	VCC1833_6	IRQ03_6	P03_6	—	GTIOC1_0A	SCK0 / SCKE0 / SD1_CLK	MCLK02 / MCLK32	—	—	ENCIFCK0 / DUEI4 / HDSL1_SMPL
T2	VCC1833_6	IRQ04_3	P04_3	—	GTIOC1_2B	DE0 / RXDE2 / SD1_DATA3	MDAT01 / MDAT31	—	—	ENCIFDI2 / SI5# / HDSL1_CLK2
T3	VCC1833_5	IRQ04_6	P04_6	—	GTIOC2_4A / GTIOC5_2A / CMTW0_TIC1	TXD1/SDA1/MOSI1 / ESC_LINKACT1 / CANTX0 / SPI_MOSI1 / SD0_DATA0 / NAND_IO0	—	—	HSPI_IO0	SI6# / HDSL1_MOSI2
T4	VCC1833_5	IRQ05_1	P05_1	—	GTIOC4_4B / GTIOC5_3B / CMTW1_TOC0	DE1 / DEE5 / ETHSW_PTPOUT0 / ESC_SYNC0 / SPI_SSL12 / SPI_RSPCK0 / SD0_DATA3 / NAND_IO3	—	—	HSPI_IO3	ENCIFOE5 / SI7#
T5	—	VSS	—	—	—	—	—	—	—	—
T6	—	VSS	—	—	—	—	—	—	—	—
T7	—	—	—	—	—	—	—	—	—	—
T8	—	VDD	—	—	—	—	—	—	—	—
T9	—	VSS	—	—	—	—	—	—	—	—
T10	—	VDD	—	—	—	—	—	—	—	—
T11	—	VCC18_PLL4	—	—	—	—	—	—	—	—
T12	—	VSS	—	—	—	—	—	—	—	—
T13	—	VDD	—	—	—	—	—	—	—	—
T14	—	VCC33	—	—	—	—	—	—	—	—
T15	—	VSS	—	—	—	—	—	—	—	—
T16	—	VDD	—	—	—	—	—	—	—	—
T17	—	—	—	—	—	—	—	—	—	—
T18	—	VSS	—	—	—	—	—	—	—	—
T19	—	—	—	—	—	—	—	DDR_CAA4	—	—
T20	—	—	—	—	—	—	—	DDR_CAA3	—	—
T21	—	VSS	—	—	—	—	—	—	—	—
T22	—	—	—	—	—	—	—	DDR_CSA1	—	—
T23	—	—	—	—	—	—	—	DDR_CKEA1	—	—
U1	—	VSS	—	—	—	—	—	—	—	—
U2	VCC1833_5	IRQ04_4	P04_4	—	GTIOC5_1A / CMTW0_TIC0	SCK1 / GMAC0_PTPTRG0 / ESC_LATCH0 / SPI_RSPCK1 / SD0_CLK / NAND_WE#	—	—	HSPI_INT#	DUEI6 / HDSL1_SEL2
U3	VCC1833_5	IRQ05_2	P05_2	—	GTIOC1_3B / GTIOC5_0A / CMTW1_TIC1	SCK2 / TXDE5 / ESC_LEDRUN / SPI_RSPCK2 / SD0_DATA4 / NAND_IO4	—	—	HSPI_CK	ENCIFDO5 / HDSL2_CLK1

Table 1.20 List of pins and pin functions (489-pin FBGA) (14 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
U4	VCC1833_5	IRQ05_4	P05_4	—	GTIOC2_3A	TXD2/SDA2/MOSI2 / IIC_SDA2 / ETH0_RXER / SPI_MOSI2 / SD0_DATA6 / NAND_IO6	MCLK00	—	HSPI_IO5	HDSL2_MISO1
U5	—	VSS	—	—	—	—	—	—	—	—
U6	—	VCC33	—	—	—	—	—	—	—	—
U7	—	—	—	—	—	—	—	—	—	—
U8	—	—	—	—	—	—	—	—	—	—
U9	—	—	—	—	—	—	—	—	—	—
U10	—	—	—	—	—	—	—	—	—	—
U11	—	—	—	—	—	—	—	—	—	—
U12	—	—	—	—	—	—	—	—	—	—
U13	—	—	—	—	—	—	—	—	—	—
U14	—	—	—	—	—	—	—	—	—	—
U15	—	—	—	—	—	—	—	—	—	—
U16	—	—	—	—	—	—	—	—	—	—
U17	—	—	—	—	—	—	—	—	—	—
U18	—	DDR_VDDQ	—	—	—	—	—	—	—	—
U19	—	—	—	—	—	—	—	DDR_CALIBRATION	—	—
U20	—	—	—	—	—	—	—	DDR_RETENTION	—	—
U21	—	—	—	—	—	—	—	DDR_RESET#	—	—
U22	—	—	—	—	—	—	—	DDR_CAA5	—	—
U23	—	VSS	—	—	—	—	—	—	—	—
V1	VCC1833_5	IRQ04_5	P04_5	—	GTIOC5_1B / CMTW0_TOC0	RXD1/SCL1/MISO1 / ESC_LINKACT0 / CANRX0 / SPI_MISO1 / SD0_CMD / NAND_RE#	—	—	HSPI_CS#	TST_OUT6 / HDSL1_MISO2
V2	VCC1833_5	IRQ04_7	P04_7	—	GTIOC2_4B / GTIOC5_2B / CMTW0_TOC1	SS1#/CTS1#/RTS1# / ESC_RESETOUT# / CANRXDP0 / SPI_DDL10 / SD0_DATA1 / NAND_IO1	—	—	HSPI_IO1	DUEI7 / HDSL2_LINK
V3	—	VSS	—	—	—	—	—	—	—	—
V4	VCC1833_5	IRQ05_3	P05_3	—	GTIOC5_0B / CMTW1_TOC1	RXD2/SCL2/MISO2 / RXDE5 / IIC_SCL2 / ETH0_TXER / ETH1_RXER / SPI_MISO2 / SD0_DATA5 / NAND_IO5	—	—	HSPI_IO4	ENCIFDI5 / HDSL2_SEL1
V5	—	VSS	—	—	—	—	—	—	—	—
V6	—	VSS	—	—	—	—	—	—	—	—
V7	—	VCC33	—	—	—	—	—	—	—	—
V8	—	VCC33	—	—	—	—	—	—	—	—
V9	—	VSS	—	—	—	—	—	—	—	—
V10	—	VCC18_PLL3	—	—	—	—	—	—	—	—
V11	—	VSS	—	—	—	—	—	—	—	—
V12	—	PCIE_VDDA_RX	—	—	—	—	—	—	—	—
V13	—	PCIE_VDDA_TX	—	—	—	—	—	—	—	—
V14	—	PCIE_VDDA_TX	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (489-pin FBGA) (15 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
V15	—	PCIE_VCC18A_CMN	—	—	—	—	—	—	—	—
V16	—	VSS	—	—	—	—	—	—	—	—
V17	—	VSS	—	—	—	—	—	—	—	—
V18	—	VSS	—	—	—	—	—	—	—	—
V19	—	VSS	—	—	—	—	—	—	—	—
V20	—	VCC18_OTP	—	—	—	—	—	—	—	—
V21	—	VSS	—	—	—	—	—	—	—	—
V22	—	VSS	—	—	—	—	—	—	—	—
V23	—	VSS	—	—	—	—	—	—	—	—
W1	VCC1833_5	IRQ05_0	P05_0	—	GTIOC3_4A / GTIOC5_3A / CMTW1_TIC0	CTS1# / SCKE5 / ESC_LEDERR / CANTXDP0 / SPI_SSL11 / SD0_DATA2 / NAND_IO2	—	—	HSPI_IO2	ENCIFCK5 / TST_OUT7 / HDSL2_SMPL
W2	VCC1833_5	IRQ05_5	P05_5	—	GTIOC2_3B	SS2#/CTS2#/RTS2# / RXD2/SCL2/MISO2 / ETH0_CRS / SPI_SSL20 / SD0_DATA7 / NAND_IO7	MDAT00	—	HSPI_IO6	HDSL2_MOSI1
W3	VCC1833_5	IRQ05_6	P05_6	—	—	CTS2# / TXD2/SDA2/ MOSI2 / ETH2_COL / SPI_SSL21 / SD0_RST# / NAND_WP#	MCLK01	—	HSPI_IO7	HDSL2_CLK2
W4	—	MDW0 / IRQ08_5	P08_5	A6	—	SCKE3 / SD1_PWEN / NAND_ALE	—	—	HA6	ENCIFCK3 / DUIE0
W5	—	MDD / IRQ08_7	P08_7	A8	—	DEE7 / SD0_PWEN / NAND_CE0#	—	—	HA8	ENCIFOE7 / SI0#
W6	—	VSS	—	—	—	—	—	—	—	—
W7	—	VSS	—	—	—	—	—	—	—	—
W8	—	VSS	—	—	—	—	—	—	—	—
W9	—	VDD18ABG	—	—	—	—	—	—	—	—
W10	—	VCC33_USB	—	—	—	—	—	—	—	—
W11	—	VSS_USB	—	—	—	—	—	—	—	—
W12	—	VSS	—	—	—	—	—	—	—	—
W13	—	PCIE_VDDA_RX	—	—	—	—	—	—	—	—
W14	—	—	—	—	—	—	—	PCIE_REFCLKN	—	—
W15	—	VSS	—	—	—	—	—	—	—	—
W16	—	VSS	—	—	—	—	—	—	—	—
W17	—	VCC18_ADC0	—	—	—	—	—	—	—	—
W18	—	VCC18_ADC1	—	—	—	—	—	—	—	—
W19	—	VCC18_ADC2	—	—	—	—	—	—	—	—
W20	—	VSS	—	—	—	—	—	—	—	—
W21	—	AVCC18_TSU	—	—	—	—	—	—	—	—
W22	—	VSS	—	—	—	—	—	—	—	—
W23	—	VSS	—	—	—	—	—	—	—	—
Y1	—	MDW1 / IRQ08_6	P08_6	A7	—	DEE3 / SD1_IOVS / NAND_CLE	—	—	HA7	ENCIFOE3 / TST_OUT0
Y2	—	MDV0 / IRQ09_0	P09_0	WE0#	—	TXDE7 / ETHSW_PTPOUT1 / ESC_SYNC1 / SD0_IOVS	—	—	HWR0#	ENCIFDO7 / DUEI1

Table 1.20 List of pins and pin functions (489-pin FBGA) (16 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
Y3	—	IRQ09_3	P09_3	CS0#	MTIOC2A / GTIOC4_3A	SS0#/CTS0#/RST0# / RXDE6 / SCKE4 / ETHSW_LPI0 / ESWM_MPINT0 / SD0_CD / NAND_RY_BY0#	MCLK31	—	HCS0#	ENCIFCK4 / ENCIFDI6 / HDSL6_MOSi1
Y4	—	MDV2 / IRQ09_5	P09_5	A1	—	TXDE3 / TXDE4 / ETHSW_LPI2	—	—	HA1	ENCIFDO3 / ENCIFDO4 / DUEI2
Y5	—	MDV4 / IRQ09_7	P09_7	A3	—	SCKE6 / ETHSW_TDMAOUT1 / ESC_LINKACT1 / ESC_LINKACT2	—	—	HA3	ENCIFCK6 / SI2# / POUTA
Y6	—	TDI / IRQ12_1	P12_1	—	—	—	—	—	—	—
Y7	—	TRST#	—	—	—	—	—	—	—	—
Y8	—	VSS	—	—	—	—	—	—	—	—
Y9	—	NCPOUT	—	—	—	—	—	—	—	—
Y10	—	AVCC18_USB	—	—	—	—	—	—	—	—
Y11	—	VSS_USB	—	—	—	—	—	—	—	—
Y12	—	VSS	—	—	—	—	—	—	—	—
Y13	—	PCIE_VCC18A	—	—	—	—	—	—	—	—
Y14	—	—	—	—	—	—	—	PCIE_REFCLKP	—	—
Y15	—	EXTCLKIN	—	—	—	—	—	—	—	—
Y16	—	MDX	—	—	—	—	—	—	—	—
Y17	—	VREFH0	—	—	—	—	—	—	—	—
Y18	—	VREFH1	—	—	—	—	—	—	—	—
Y19	—	VREFH2	—	—	—	—	—	—	—	—
Y20	—	VSS	—	—	—	—	—	—	—	—
Y21	—	VSS	—	—	—	—	—	—	—	—
Y22	—	VSS	—	—	—	—	—	—	—	—
Y23	—	—	—	—	—	—	—	AN205	—	—
AA1	—	MDV1 / IRQ09_1	P09_1	WE1#	—	SCKE7 / NAND_CE1#	—	—	HWR1#	ENCIFCK7 / TST_OUT1
AA2	—	IRQ09_2	P09_2	WAIT#	—	SCK0 / RXDE3 / RXDE4 / NAND_RY_BY1#	—	—	HWAIT#	ENCIFDI3 / ENCIFDI4 / SI1# / HDCL6_CLK1
AA3	—	IRQ09_4	P09_4	RD#	MTIOC2B / GTIOC4_3B	CTS0# / RXDE7 / DEE4 / ETHSW_LPI1 / ESWM_MPINT1 / SD0_WP / NAND_RY_BY2#	MDAT31	—	HRD#	ENCIFOE4 / ENCIFDI7
AA4	—	IRQ11_3	P11_3	—	POE4# / GTETRGD	RXD0/SCL0/MISO0 / IIC_SCL1	—	—	—	—
AA5	—	IRQ11_7	P11_7	—	POE11# / GTIOC5_2A / GTETRGB / RTCAT1HZ	—	—	USB_OTG_ID	MBX_HINT#	—
AA6	—	TDO / IRQ12_3	P12_3	—	—	—	—	—	—	—
AA7	—	IRQ12_4	P12_4	—	—	—	—	USB_VBUSIN	—	—
AA8	—	VSS	—	—	—	—	—	—	—	—
AA9	—	VSS_USB	—	—	—	—	—	—	—	—
AA10	—	USB_RREF	—	—	—	—	—	—	—	—
AA11	—	VSS_USB	—	—	—	—	—	—	—	—
AA12	—	VSS	—	—	—	—	—	—	—	—
AA13	—	VSS	—	—	—	—	—	—	—	—
AA14	—	VSS	—	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (489-pin FBGA) (17 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
AA15	—	VSS	—	—	—	—	—	—	—	—
AA16	—	VSS	—	—	—	—	—	—	—	—
AA17	—	VSS	—	—	—	—	—	—	—	—
AA18	—	VSS	—	—	—	—	—	—	—	—
AA19	—	—	—	—	—	—	—	AN102	—	—
AA20	—	—	—	—	—	—	—	AN103	—	—
AA21	—	—	—	—	—	—	—	AN201	—	—
AA22	—	—	—	—	—	—	—	AN203	—	—
AA23	—	—	—	—	—	—	—	AN207	—	—
AB1	—	MDV3 / IRQ09_6	P09_6	A2	—	DE0 / TXDE6 / ETHSW_TDMAOUT0 / NAND_CE2#	—	—	HA2	ENCIFDO6 / TST_OUT2
AB2	—	MDV5 / IRQ10_0	P10_0	A4	—	DEE6 / ETHSW_TDMAOUT2 / ESC_IRQ / NAND_CE3#	—	—	HA4	ENCIFOE6 / POUTB
AB3	—	MDB / IRQ10_1	P10_1	A5	—	ETHSW_TDMAOUT3 / ESC_RESETOUT# / ESC_LEDRUN	—	—	HA5	POUTZ
AB4	—	IRQ11_0	P11_0	—	—	TXDE2	—	USB_VBUSEN	—	ENCIFDO2
AB5	—	IRQ11_2	P11_2	—	GTIOC0_3B	TXD1/SDA1/MOSI1 / IIC_SDA0 / ESC_I2CDATA	—	USB_EXICEN	—	—
AB6	—	CKIO / IRQ11_5	P11_5	—	POE0# / GTIOC5_0A / GTETRGA	SCIEXTCLK / IIC_SCL2 / NAND_RY_BY3#	—	—	HCKIO	—
AB7	—	BSCANP	—	—	—	—	—	—	—	—
AB8	—	VSS	—	—	—	—	—	—	—	—
AB9	—	—	—	—	—	—	—	USB_DP	—	—
AB10	—	VCC18_USB	—	—	—	—	—	—	—	—
AB11	—	VSS	—	—	—	—	—	—	—	—
AB12	—	—	—	—	—	—	—	PCIE_RXDP	—	—
AB13	—	VSS	—	—	—	—	—	—	—	—
AB14	—	—	—	—	—	—	—	PCIE_TXDP	—	—
AB15	—	VSS	—	—	—	—	—	—	—	—
AB16	—	XTAL	—	—	—	—	—	—	—	—
AB17	—	VSS	—	—	—	—	—	—	—	—
AB18	—	—	—	—	—	—	—	AN000	—	—
AB19	—	—	—	—	—	—	—	AN002	—	—
AB20	—	—	—	—	—	—	—	AN101	—	—
AB21	—	—	—	—	—	—	—	AN202	—	—
AB22	—	—	—	—	—	—	—	AN204	—	—
AB23	—	—	—	—	—	—	—	AN206	—	—
AC1	—	VSS	—	—	—	—	—	—	—	—
AC2	—	IRQ11_1	P11_1	—	GTIOC0_3A	RXD1/SCL1/MISO1 / RXDE2 / IIC_SCL0 / ESC_I2CCLK	—	USB_OVRCUR	—	ENCIFDI2
AC3	—	RSTOUT# / IRQ11_4	P11_4	—	GTETRGSA	TXD0/SDA0/MOSI0 / IIC_SDA1	—	—	—	—
AC4	—	IRQ11_6	P11_6	—	—	IIC_SDA2	—	USB_OVRCUR	—	—
AC5	—	TMS / IRQ12_0	P12_0	—	—	—	—	—	—	—
AC6	—	VSS	—	—	—	—	—	—	—	—
AC7	—	TCK / IRQ12_2	P12_2	—	—	—	—	—	—	—

Table 1.20 List of pins and pin functions (489-pin FBGA) (18 of 18)

Pin number	IO Port power domain	Power supply clock, system control, interrupt	I/O port	Bus, DMAC	Timer (MTU3, POE3, GPT / POEG, CMTW, RTC)	Communication (SCI, IIC, GMAC, ETHSW, ESC, ESWM, HPSW, CANFD, SPI, xSPI, SDHI, NAND)	DSMIF	Analog / High speed (DDRSS, ADC12, USB, PCIE)	Host interface (SHOST, PHOST, MBXSEM)	Encoder I/F (ENCIF, ENDAT, ENDAT3, HDSL, ENCOUT)
AC8	—	VSS	—	—	—	—	—	—	—	—
AC9	—	—	—	—	—	—	—	USB_DM	—	—
AC10	—	VSS_USB	—	—	—	—	—	—	—	—
AC11	—	VSS	—	—	—	—	—	—	—	—
AC12	—	—	—	—	—	—	—	PCIE_RXDN	—	—
AC13	—	VSS	—	—	—	—	—	—	—	—
AC14	—	—	—	—	—	—	—	PCIE_TXDN	—	—
AC15	—	VSS	—	—	—	—	—	—	—	—
AC16	—	EXTAL	—	—	—	—	—	—	—	—
AC17	—	RES#	—	—	—	—	—	—	—	—
AC18	—	—	—	—	—	—	—	AN001	—	—
AC19	—	—	—	—	—	—	—	AN003	—	—
AC20	—	—	—	—	—	—	—	AN100	—	—
AC21	—	VSS	—	—	—	—	—	—	—	—
AC22	—	—	—	—	—	—	—	AN200	—	—
AC23	—	VSS	—	—	—	—	—	—	—	—

2. Electrical Characteristics

Electrical characteristics of this LSI is defined with the following conditions unless otherwise described.

Conditions:

- Core voltage
  VDD = PCIE_VDDA_TX = PCIE_VDDA_RX = 1.05 to 1.15 V
- LPDDR4 I/O voltage
  DDR_VDDQ = 1.06 to 1.17 V
- 1.8V I/O and analog voltage
  VCC1833_n (n = 0 to 6, 1.8-V mode) = VCC18_PLLn (n = 0 to 4) = AVCC18_TSU = VCC18_OTP = VCC18_USB = AVCC18_USB = VCC18_ADCn (n = 0 to 2) = PCIE_VCC18A = PCIE_VCC18A_CMN = 1.70 to 1.95 V
- 3.3V I/O and analog voltage
  VCC33 = VCC1833_n (n = 0 to 6, 3.3-V mode) = VCC33_USB = 3.135V to 3.465
- Ground
  VSS = VSS_USB = 0 V
- Operating temperature
  Tj = −40 to 125ºC

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter	Symbol	Value	Unit
Power supply voltage (3.3-V mode)	VCC33 VCC1833_0 to VCC1833_6 (3.3-V mode)	-0.3 to +3.8	V
Power supply voltage (1.8-V mode)	(VCC18) VCC1833_0 to VCC1833_6 (1.8-V mode)	-0.3 to +2.5	V
Power supply voltage (Core)	VDD	-0.3 to +1.5	V
Input voltage	Vin (3.3-V logic)	-0.3 to smaller value of VDD33/ VCC1833_n (3.3-V mode) + 0.3 or 3.8	V
Input voltage	Vin (1.8-V logic)	-0.3 to smaller value of VDD33/ VCC1833_n (1.8-V mode) + 0.3 or 2.5	V
ABBG power supply voltage	VDD18ABG	-0.3 to +2.5	V
PLL power supply voltage	VCC18_PLL0 to VCC18_PLL4	-0.3 to +2.5	V
TSU power supply voltage	AVCC18_TSU	-0.3 to +2.5	V
OTP power supply voltage	VCC18_OTP	-0.3 to +2.5	V
USB power supply voltage	VCC33_USB	-0.3 to smaller value of VCC33 + 0.3 or 3.8	V
	VCC18_USB, AVCC18_USB	-0.3 to +2.5	V
ADC12 power supply voltage	VCC18_ADC0 to VCC18_ADC2	-0.3 to +2.5	V
PCI Express power supply voltage	PCIE_VCC18A, PCIE_VCC18A_CMN	-0.3 to +2.5	V
	PCIE_VDDA_TX, PCIE_VDDA_RX	-0.3 to +1.5	V
LPDDR4 power supply voltage	DDR_VDDQ	-0.3 to +1.4	V
Voltage difference between power supply pins	VCC33-VCC18	-2.5 to +2.1	V
ADC12 analog input voltage	VAN	-0.3 to smaller value of VCC18_ADCn + 0.3 or 2.5	V

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter	Symbol	Value	Unit
ADC12 reference voltage	VREFH0 to VREFH2	-0.3 to smaller value of VCC18_ADCn + 0.3 or 2.5	V
Crystal oscillator pins input voltage	XTAL, EXTAL	-0.3 to +1.5	V
Operating temperature (Junction temperature)	Tj	-40 to +125	ºC
Storage temperature	Tstg	-55 to +125	ºC

Caution: Permanent damage to the LSI might result if absolute maximum ratings are exceeded.

2.2 Power Supply

Table 2.2 Power supply

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage (3.3-V I/O)	VCC33 VCC1833_0 to VCC1833_6 (3.3-V mode)	3.135	3.3	3.465	V
Power supply voltage (1.8-V I/O)	(VCC18) VCC1833_0 to VCC1833_6 (1.8-V mode)	1.7	1.8	1.95	V
Power supply voltage (Core)	VDD	1.05	1.1	1.15	V
Ground	VSS	—	0	—	V
ABBG power supply voltage	VDD18ABG	1.7	1.8	1.95	V
PLL power supply voltage	VCC18_PLL0 to VCC18_PLL4	1.7	1.8	1.95	V
TSU power supply voltage	AVCC18_TSU	1.7	1.8	1.95	V
OTP power supply voltage	VCC18_OTP	1.7	1.8	1.95	V
USB power supply voltage	VCC33_USB	3.135	3.3	3.465	V
	VCC18_USB, AVCC18_USB	1.7	1.8	1.95	V
	VSS_USB	—	0	—	V
ADC12 power supply voltage	VCC18_ADC0 to VCC18_ADC2	1.7	1.8	1.95	V
PCI Express power supply voltage	PCIE_VCC18A, PCIE_VCC18A_CMN	1.7	1.8	1.95	V
	PCIE_VDDA_TX, PCIE_VDDA_RX	1.05	1,1	1,15	V
LPDDR4 power supply voltage	DDR_VDDQ	1.06	1.1	1.17	V
ADC12 reference voltage	VREFHn (n = 0 to 2)	VSS	—	VCC18_ADCn	V

Note: The condition of A/D conversion characteristics is VREFHn = VCC18_ADCn (n = 0 to 2). And power-up/down sequence should follow VCC18_ADCn.
Note: Even if there are unused functions, power must be supplied to each power pins.

2.3 Power On/Off Sequence

Power on/off sequence and timing are shown in the figure and table below.

For power-up, 1.1-V power (i.e. VDD) must be supplied first, 1.8-V power (i.e. VCC18, PCIE_VCC18A, and AVCC) must be supplied second, 3.3-V power (i.e. VCC33) must be supplied third, then 1.8-V/3.3-V SDHI, 1.1-V DDR I/O, and 1.1-V PCIe power (i.e. VCC1833_5/6, DDR_VDDQ, and PCIE_VDDA_TX/RX) must be supplied. The power-up sequence must be completed within 100 ms. The reset signal (i.e. RES#) must be held to Low level during the power-up.

For power-down, 1.8-V/3.3-V SDHI, 1.1-V DDR I/O and 1.1-V PCIe power (i.e. VCC1833_5/6, DDR_VDDQ, and PCIE_VDDA_TX/RX) must go down first, 3.3-V power (i.e. VCC33) must go down second, and then 1.1-V and 1.8-V power (i.e. VDD, VCC18, PCIE_VCC18A, and AVCC). The power-down sequence must be completed within 100 ms.

When 1.8-V/3.3-V switching power supply for SDHI is not used, VCC1833_5 can follow the 1.8-V power or 3.3-V power timing according to the voltage mode. VCC1833_6 should follow the 3.3-V power timing because VCC1833_6 is 3.3V fixed at power-on.

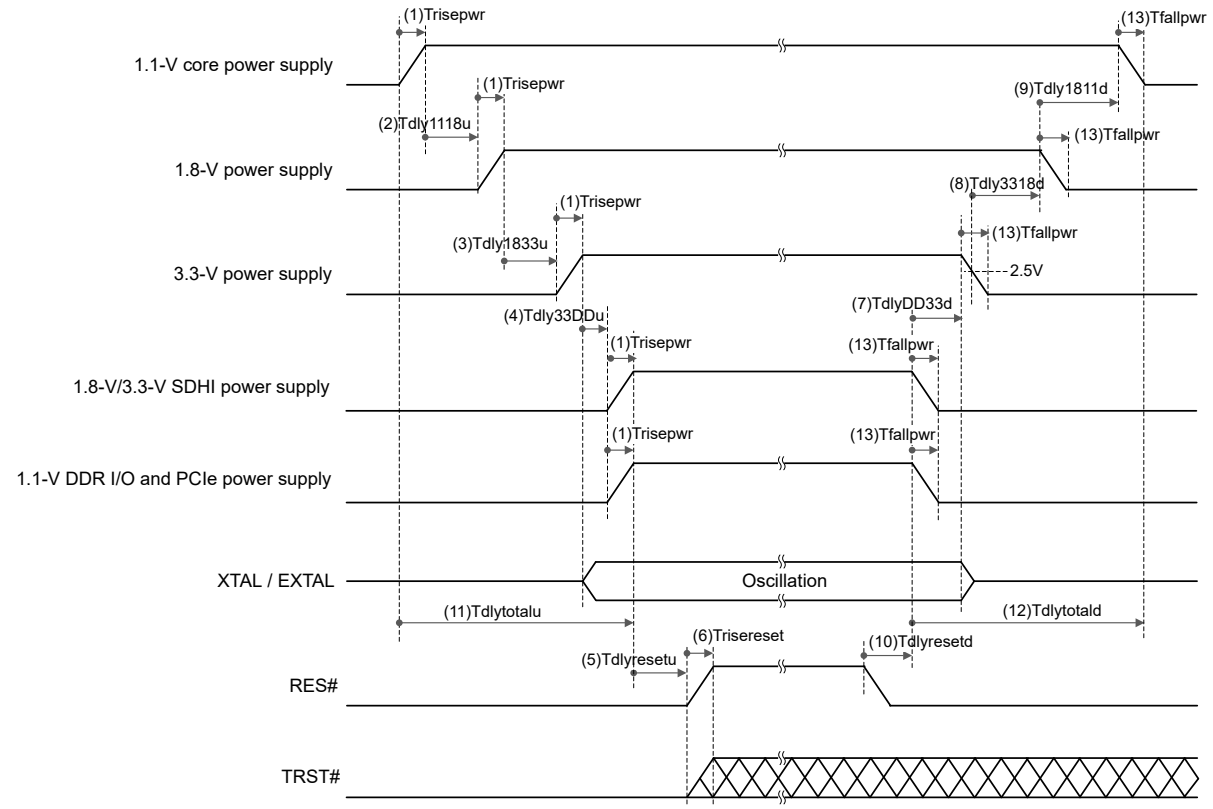
The rise and fall time of each power supply for the power-up and the power-down must be larger than 10 µs.

Power supply voltages and reset signal must be applied with monotonic increase.

Do not apply a negative voltage to power supply voltages.

Do not apply a voltage to any pins except P12_4 (USB_VBUSIN) until the power supply has powered up.

A stable clock must be supplied to EXTAL/XTAL or EXTCLKIN pin when the reset signal (i.e. RES#) is driven high.



Note:
- When 1.8V is supplied to VCC1833_n, should follow the 1.8-V power supply sequence. When 3.3V is supplied to VCC1833_n, should follow the 3.3-V power supply sequence.
- When SDHI used UHS-I mode, VCC1833_5/VCC1833_6 should require 3.3V at power up but separated power supply and sequence from other 3.3V. At power down, either 1.8-V or 3.3-V voltage is available.
- All 3.3-V power supplies except SDHI with UHS-I mode must start up at the same time.

Figure 2.1 Power on/off sequence

Table 2.3 Power on/off sequence timing (1 of 2)

No.	Symbol	Description	Value		
			Min.	Typ.	Max.
(1)	Trisepwr	Rising time of the power supply voltage	10 µs	—	30 ms
(2)	Tdly1118u	Delay time from completion of rising of the 1.1-V core power supply voltage to start of rising of the 1.8-V power supply voltage	0	—	100 ms

Table 2.3 Power on/off sequence timing (2 of 2)

No.	Symbol	Description	Value		
			Min.	Typ.	Max.
(3)	Tdly1833u	Delay time from completion of rising of the 1.8-V power supply voltage to start of rising of the 3.3-V power supply voltage	0	—	100 ms
(4)	Tdly33DDu	Delay time from completion of rising of the 3.3-V power supply voltage to start of rising of the 1.8-V/3.3-V SDHI, and 1.1-V DDR I/O and PCIe power supply voltage	10 µs	—	100 ms
(5)	Tdlyresetu	Delay time from completion of rising of the 1.8-V/3.3-V SDHI, and 1.1-V DDR I/O and PCIe power supply voltage to start of rising of RES# when XTAL/EXTAL is used.	10 ms	—	—
		Delay time from completion of rising of the 1.8-V/3.3-V SDHI, and 1.1-V DDR I/O and PCIe power supply voltage to start of rising of RES# when EXTCLKIN is used.	1 ms	—	—
(6)	Trisereset	Rising time of RES#	—	—	150 µs
(7)	TdlyDD33d	Delay time from start of falling of the 1.8-V/3.3-V SDHI, and 1.1-V DDR I/O and PCIe power supply voltage to start of falling of the 3.3-V power supply voltage	0	—	100 ms
(8)	Tdly3318d	Delay time from the time when the 3.3-V power supply voltage drops below 2.5V to start of falling of the 1.8-V power supply voltage	0	—	100 ms
(9)	Tdly1811d	Delay time from start of falling of the 1.8-V power supply voltage to start of falling of the 1.1-V power supply voltage	0	—	100 ms
(10)	Tdlyresetd	Delay time from start of falling of RES# to start of falling of 1.8-V/3.3-V SDHI, and 1.1-V DDR I/O and PCIe power supply voltage	8 µs	—	—
(11)	Tdlytotalu	Startup time of all power supply voltage	0	—	100 ms
(12)	Tdlytotald	Shut down time of all power supply voltage	0	—	100 ms
(13)	Tfallpwr	Falling time of the power supply voltage	10 µs	—	30 ms

2.4 DC Characteristics

Table 2.4 DC Characteristics (3.3-V mode) (1 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High-level voltage	V_{IH33}	3.3-V mode, Schmitt Trigger Control Disabled, Except P12_4 pin	2.0	—	VCC33 + 0.3	V
Input Low-level voltage	V_{IL33}		−0.3	—	0.8	V
Positive trigger voltage	V_{T33+}	3.3-V mode, Schmitt Trigger Control Enabled, Except P12_4 pin	0.9	—	2.1	V
Negative trigger voltage	V_{T33-}		0.7	—	1.9	V
Hysteresis voltage	ΔV_{T33}		0.2	—	—	V
Input High-level voltage 2	V_{IH33_2}	3.3-V mode, Schmitt Trigger Control Disabled, P12_4 pin ONLY	VCC33 × 0.7	—	VCC33 + 0.3	V
Input Low-level voltage 2	V_{IL33_2}		-0.3	—	VCC33 × 0.3	V
Positive trigger voltage 2	V_{T33+_2}	3.3-V mode, Schmitt Trigger Control Enabled, P12_4 pin ONLY	—	—	VCC33 × 0.72	V
Negative trigger voltage 2	V_{T33-_2}		VCC33 × 0.3	—	—	V
Hysteresis voltage 2	ΔV_{T33_2}		VCC33 × 0.1	—	—	V
Output High-level voltage	V_{OH33}	Low, IOH = −2 mA	VCC33 − 0.4	—	—	V
	V_{OH33}	Middle, IOH = −4 mA	VCC33 − 0.4	—	—	V
	V_{OH33}	High, IOH = −8 mA	VCC33 − 0.4	—	—	V
	V_{OH33}	Ultra High, IOH = −12 mA	VCC33 − 0.4	—	—	V

Table 2.4 DC Characteristics (3.3-V mode) (2 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Low-level voltage	V_{OL33}	Low, IOL = 2 mA	—	—	0.4	V
	V_{OL33}	Middle, IOL = 4 mA	—	—	0.4	V
	V_{OL33}	High, IOL = 8 mA	—	—	0.4	V
	V_{OL33}	Ultra High, IOL = 12 mA	—	—	0.4	V
Input leakage current	|Iin|	Vin = 0 V, Vin = VCC33	—	—	10	µA
Three-State leakage current (off state)	$\|I_{TSI}\|$	Vin = 0 V, Vin = VCC33	—	—	10	µA
Input Pull-up resistors resistance	Rpu	Vin = 0 V	15	—	300	kΩ
Input Pull-up resistors current	Ipu	Vin = 0 V	-220	—	-11	µA
Input Pull-down resistors resistance	Rpd	Vin = VCC33	15	—	300	kΩ
Input Pull-down resistors current	Ipd	Vin = VCC33	11	—	220	µA
Input Capacitance	Cin	All input/output and input pins	—	—	10	pF

Table 2.5 DC Characteristics (1.8-V mode)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input High-level voltage	V_{IH18}	1.8-V mode, Schmitt Trigger Control Disabled	VCC18 × 0.65	—	VCC18 + 0.3	V
Input Low-level voltage	V_{IL18}		−0.3	—	VCC18 × 0.35	V
Positive trigger voltage	V_{T18+}	1.8-V mode, Schmitt Trigger Control Enabled	VCC18 × 0.4	—	VCC18 × 0.7	V
Negative trigger voltage	V_{T18-}		VCC18 × 0.3	—	VCC18 × 0.6	V
Hysteresis voltage	ΔV_{T18}		VCC18 × 0.1	—	—	V
Output High-level voltage	V_{OH18}	Low, IOH = −2 mA	VCC18 − 0.45	—	—	V
	V_{OH18}	Middle, IOH = −4 mA	VCC18 − 0.45	—	—	V
	V_{OH18}	High, IOH = −8 mA	VCC18 − 0.45	—	—	V
	V_{OH18}	Ultra High, IOH = −12 mA	VCC18 − 0.45	—	—	V
Output Low-level voltage	V_{OL18}	Low, IOL = 2 mA	—	—	0.45	V
	V_{OL18}	Middle, IOL = 4 mA	—	—	0.45	V
	V_{OL18}	High, IOL = 8 mA	—	—	0.45	V
	V_{OL18}	Ultra High, IOL = 12 mA	—	—	0.45	V
Input leakage current	|Iin|	Vin = 0 V, Vin = VCC18	—	—	10	µA
Three-State leakage current (off state)	$\|I_{TSI}\|$	Vin = 0 V, Vin = VCC18	—	—	10	µA
Input Pull-up resistors resistance	Rpu	Vin = 0 V	15	—	300	kΩ
Input Pull-up resistors current	Ipu	Vin = 0 V	-120	—	-6	µA
Input Pull-down resistors resistance	Rpd	Vin = VCC18	15	—	300	kΩ
Input Pull-down resistors current	Ipd	Vin = VCC18	6	—	120	µA
Input Capacitance	Cin	All input/output and input pins	—	—	10	pF

Table 2.6 USB2.0 USB_RREF Pin

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reference resistor*1	R_{REF}	—	1.8 (±1%)			kΩ

Note 1. The reference resistor connected to the USB_RREF pin is for external connection to this LSI.

Table 2.7 USB2.0 Pull-Up/Pull-Down Resistors

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
USB_DP pull-up resistor (when the function controller is selected)	R_{PU}	Idle	0.900	—	1.575	kΩ
		Transmission/reception	1.425	—	3.090	kΩ
USB_DP/USB_DM pull-down resistors (when the host controller is selected)	R_{PD}	—	14.25	—	24.80	kΩ

Table 2.8 USB2.0 Host/Function-Related Pins (Low/Full Speed)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input high level voltage	V_{FSIH}	—	2.0	—	—	V
Input low level voltage	V_{FSIL}	—	—	—	0.8	V
Differential input sensitivity	V_{FSDI}	|(USB_DP) − (USB_DM)|	0.2	—	—	V
Differential common mode range	V_{FSCM}	—	0.8	—	2.5	V
Output low level voltage	V_{FSOL}	IFSOL = 2 mA	0.0	—	0.3	V
Output high level voltage	V_{FSOH}	IFSOH = −200 µA	2.8	—	3.6	V
Output signal crossover voltage	V_{FSCRS}	—	1.3	—	2.0	V

Table 2.9 USB2.0 Host/Function-Related Pins (High Speed)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Squelch detection threshold voltage (differential voltage)	V_{HSSQ}	—	100	—	150	mV
Disconnection detection threshold voltage (differential voltage)	V_{HSDSC}	—	525	—	625	mV
Common mode voltage range	V_{HSCM}	—	−50	—	500	mV
Idle state	V_{HSOI}	—	−10.0	—	10.0	mV
Output high level voltage	V_{HSOH}	—	360	—	440	mV
Output low level voltage	V_{HSOL}	—	−10.0	—	10.0	mV
Chirp J output voltage (differential)	V_{CHIRPJ}	—	700	—	1100	mV
Chirp K output voltage (differential)	V_{CHIRPK}	—	−900	—	−500	mV

Table 2.10 Supply Current (1 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Normal operation	I_{vdd}	Cortex-A55 Clock = 1.2 GHz Cortex-R52 Clock = 800 MHz, Tj ≤ 110°C	—	—	2300	mA
	I_{VCC33}	*1	—	27	—	mA
	$I_{VCC1833_0}$	*1	—	18	—	mA
	$I_{VCC1833_1}$	*1	—	9	—	mA
	$I_{VCC1833_2}$	*1	—	18	—	mA
	$I_{VCC1833_3}$	*1	—	9	—	mA
	$I_{VCC1833_4}$	*1	—	9	—	mA
	$I_{VCC1833_5}$	*1	—	9	—	mA
	$I_{VCC1833_6}$	*1	—	9	—	mA
	I_{VCC18_PLL0}	—	—	—	6	mA
	I_{VCC18_PLL1}	—	—	—	6	mA
	I_{VCC18_PLL2}	—	—	—	6	mA
	I_{VCC18_PLL3}	—	—	—	6	mA
	I_{VCC18_PLL4}	—	—	—	6	mA
	I_{VCC18_USB}	—	—	—	39	mA
	I_{VCC18_ADC0}	—	—	—	3	mA
	I_{VCC18_ADC1}	—	—	—	3	mA
	I_{VCC18_ADC2}	—	—	—	3	mA
	I_{VCC18_TSU}	—	—	—	1	mA
	I_{VCC18_OTP}	—	—	—	5	mA
	I_{VCC33_USB}	—	—	—	6	mA
	I_{PCIE_VCC18A}	—	—	—	8	mA
	$I_{PCIE_VCC18A_CMN}$	—	—	—	8	mA
	$I_{PCIE_VDDA_TX}$	—	—	—	18	mA
	$I_{PCIE_VDDA_RX}$	—	—	—	19	mA
	I_{DDR_VDDQ}	—	—	—	260	mA
	I_{VDDABG}	—	—	—	1.1	mA

Table 2.10 Supply Current (2 of 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low power consumption mode*2	I_{vdd}	All modules inactive	—	18	—	mA
	I_{VCC33}	*1	—	13	—	mA
	$I_{VCC1833_0}$	*1	—	4	—	mA
	$I_{VCC1833_1}$	*1	—	2	—	mA
	$I_{VCC1833_2}$	*1	—	4	—	mA
	$I_{VCC1833_3}$	*1	—	2	—	mA
	$I_{VCC1833_4}$	*1	—	2	—	mA
	$I_{VCC1833_5}$	*1	—	2	—	mA
	$I_{VCC1833_6}$	*1	—	1	—	mA
	I_{VCC18_PLL0}	—	—	3.5	—	mA
	I_{VCC18_PLL1}	—	—	3.5	—	mA
	I_{VCC18_PLL2}	—	—	0.1	—	mA
	I_{VCC18_PLL3}	—	—	0.1	—	mA
	I_{VCC18_PLL4}	—	—	0.1	—	mA
	I_{VCC18_USB}	—	—	0.5	—	mA
	I_{VCC18_ADC0}	—	—	0.2	—	mA
	I_{VCC18_ADC1}	—	—	0.2	—	mA
	I_{VCC18_ADC2}	—	—	0.2	—	mA
	I_{VCC18_TSU}	—	—	0.1	—	mA
	I_{VCC18_OTP}	—	—	0.1	—	mA
	I_{VCC33_USB}	—	—	0.3	—	mA
	I_{PCIE_VCC18A}	—	—	0.8	—	mA
	$I_{PCIE_VCC18A_CMN}$	—	—	0.8	—	mA
	$I_{PCIE_VDDA_TX}$	—	—	0.5	—	mA
	$I_{PCIE_VDDA_RX}$	—	—	0.5	—	mA
	I_{DDR_VDDQ}	—	—	0.3	—	mA
	I_{VDDABG}	—	—	0.1	—	mA

Note: These values are reference values. The actual operating current greatly depends on the system (such as unsharpened waveforms due to I/O load and toggle frequency). Be sure to measure these current values in the system.

Note 1. IO supply current (I_{VCC33}, $I_{VCC1833_n\ (n = 0\ to\ 6)}$) should be 80 mA or less. (ΣIOH in Table 2.11)

Note 2. All applicable modules are stopped or standby mode with the lowest clock frequency setting, no pull-up/down or operation for all I/O ports, and room temperature.

Table 2.11 Permissible Output Currents

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Permissible output low current (max. value per pin)	IOL	All output pins	—	—	12	mA
Permissible output low current (total)	ΣIOL	Sum of all output pins	—	—	80	mA
Permissible output high current (max. value per pin)	IOH	All output pins	—	—	-12	mA
Permissible output high current (total)	ΣIOH	Sum of all output pins	—	—	-80	mA

Note: All output current values shall be within the values in this table to ensure the reliability of this LSI.

Table 2.12 Thermal Resistance value (Reference)

Item	Symbol	Package	Max.	Unit
Thermal Resistance	Θja	537 pin FBGA 21 × 21 mm, 0.8-mm pitch	15.0	°C/W
		489 pin FBGA 16 × 16 mm, 0.65-mm pitch	15.0	°C/W
	Ψjt	537 pin FBGA 21 × 21 mm, 0.8-mm pitch	0.13	°C/W
		489 pin FBGA 16 × 16 mm, 0.65-mm pitch	0.13	°C/W

Note: Package thermal resistance values above are based on EIA/JESD51-9 (2s2p) condition and reference only.

2.5 AC Characteristics

Table 2.13 Operating frequency

Parameter		Symbol	Min.	Max.	Unit
Operating frequency	Cortex-A55 Core clock (CA55CnCLK, n = 0, 1)	f	600	1,200	MHz
	Cortex-A55 DSU clock (CA55SCLK)		500	1,000	
	Cortex-R52 Core clock (CR52CnCLK, n = 0, 1)		400	800	
	Peripheral module clock AH (PCLKAH)		400		
	Peripheral module clock AM (PCLKAM)		200		
	Peripheral module clock AL (PCLKAL)		100		
	Peripheral module clock H (PCLKH)		200		
	Peripheral module clock M (PCLKM)		100		
	Peripheral module clock L (PCLKL)		50		
	Peripheral module clock for ADC (PCLKADC)		25		
	Peripheral module clock for SCIn (PCLKSCIn, n = 0 to 5)		75	100	
	Peripheral module clock for SCIEn (PCLKSCIEn, n = 0 to 7)		75	100	
	Peripheral module clock for SPIn (PCLKSPIn, n = 0 to 3)		75	100	
	xSPI serial clock (XSPI_CLKn) (n = 0, 1)		12.5	133	
	DDR controller clock		0.0125	800	
	External bus clock output (CKIO)		25	100	
	Ethernet PHY reference clock (ETHn_REFCLK, n = 0 to 4)		25		
	Ethernet PHY reference clock (RMIIn_REFCLK, n = 0 to 4)		50		

AC Characteristics are defined in condition of the IO setting (DRCTLm register setting) show in Table 2.14.

Table 2.14 IO setting (DRCTLm register setting) condition (1 of 2)

Module	Signal		IO type	Voltage	DRCTLm register		
					DRVn	SRn	SMTn
Bus	CKIO	High drive	—	3.3 V	High	Fast	—
		Other than the above	—	3.3 V	Middle	Fast	—
	Other than the above		Type A	3.3 V	Middle	Slow	Disable
			Type B	3.3 V	Low	Slow	Disable
DMAC, MTU3, IIC, CANFD, DSMIF	All signals		Type A	3.3 V	Middle	Slow	Disable
			Type B	3.3 V	Low	Slow	Disable

Table 2.14 IO setting (DRCTLm register setting) condition (2 of 2)

Module		Signal	IO type	Voltage	DRCTLm register		
					DRVn	SRn	SMTn
GPT (n = 0 to 17) (m = 0, 1)		GTIOCnA, GTIOCnB	Type A	3.3 V	Middle	Slow	Disable
			Type B	3.3 V	Low	Slow	Disable
		GTADSMLm, GTADSMPm	—	3.3 V	Low	Slow	Disable
SCI, SCIE, SPI		All signals	—	3.3 V	High	Fast	Disable
xSPI (n = 0, 1; m = 0, 1)		XSPIn_CKP, XSPIn_CKN, XSPIn_IO [7:0], XSPIn_CSm#, XSPIn_DS	—	1.8 V	High	Fast	Disable
			—	3.3 V	High	Fast	Enable
		Other than the above	—	—	Low	Slow	Disable
Ethernet Interface (n = 0 to 4)		ETHn_TXCLK, ETHn_TXD[3:0]	—	1.8 V/3.3 V	High	Fast	Disable
		ETHn_TXER	—	3.3 V	Middle	Fast	—
		ETHn_RXCLK, ETHn_RXD[3:0]	—	1.8 V/3.3 V	—	—	Disable
		ETHn_RXER, ETHn_COL, ETHn_CRS	—	3.3 V	—	—	Disable
		ETHn_REFCLK, RMIIn_REFCLK	—	3.3 V	High	Fast	—
		Other than the above	—	—	Low	Slow	Disable
SHOSTIF		HSPI_CK, HSPI_CS#, HSPI_IO[7:0]	—	1.8 V/3.3 V	High	Fast	Disable
		HSPI_INT#	—	1.8 V/3.3 V	Low	Slow	Disable
PHOSTIF		All signals	Type A	3.3 V	Middle	Slow	Disable
			Type B	3.3 V	Low	Slow	Disable
SDHI (n = 0, 1)	SDR104, SDR50, HS200	SDn_CLK	—	1.8 V	Ultra-high	Fast	—
		Other than the above	—	1.8 V	High	Fast	Disable
	DDR50, High Speed DDR	All signals	—	1.8 V/3.3 V	High	Fast	Disable
	Other than the above	SDn_CLK	—	1.8 V/3.3 V	High	Fast	—
		Other than the above	—	1.8 V/3.3 V	Middle	Fast	Disable
NANDC		NAND_CEn#, NAND_CLE, NAND_ALE, NAND_WP#	—	3.3 V	Middle	Fast	—
		NAND_IOn	—	3.3 V	High	Fast	Disable
		NAND_RW#, NAND_WE#	—	3.3 V	Middle	Fast	—
		NAND_RY_BYn#	—	3.3 V	—	—	Disable
Debug Interface		TDO, TMS	—	3.3 V	High	Fast	Disable
		Other than the above	—	—	Low	Slow	Disable
Other than the above			—	—	Low	Slow	Disable

2.5.1 Clock Timing

2.5.1.1 CKIO Pin Output Timing

Table 2.15 CKIO pin output timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CKIO pin output cycle time	t_{CKcyc}	Figure 2.2	10	—	40	ns
CKIO pin output high level pulse width	t_{CKH}		t_{CKcyc} / 2 − t_{CKr}	—	—	ns
CKIO pin output low level pulse width	t_{CKL}		t_{CKcyc} / 2 − t_{CKf}	—	—	ns
CKIO pin output rising time 1	t_{CKr}	CKIO: High drive output Setting	—	—	3.8	ns
CKIO pin output falling time 1	t_{CKf}		—	—	3.8	ns
CKIO pin output rising time 2	t_{CKr}	CKIO: Normal output setting	—	—	9	ns
CKIO pin output falling time 2	t_{CKf}		—	—	9	ns

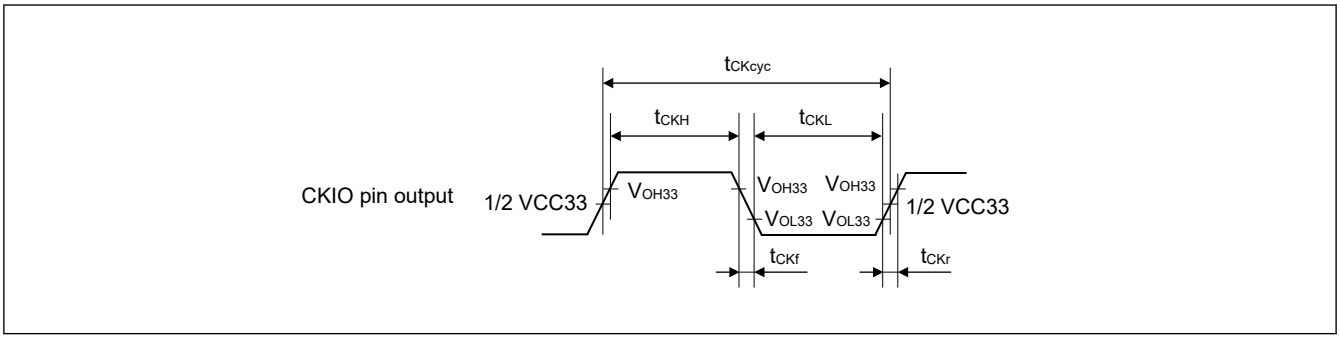


Figure 2.2 CKIO pin output timing

2.5.1.2 Ethernet PHY Reference Clock Output Timing

Conditions:

C = 30 pF (ETHn_REFCLK)

C = 25 pF (RMIIn_REFCLK)

Table 2.16 Ethernet PHY reference clock output timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
ETHn_REFCLK cycle time	t_{CK}	—	40	—	—	ns
ETHn_REFCLK frequency	—	—	25.00 ± 50 ppm			MHz
		EtherCAT in use	25.00 ± 25 ppm			MHz
ETHn_REFCLK duty*1	—	—	47	—	53	%
ETHn_REFCLK rising/falling time	t_{CKr}/t_{CKf}	—	0.5	—	4.2	ns
RMIIn_REFCLK cycle time	t_{CK}	—	20	—	—	ns
RMIIn_REFCLK frequency	—	—	50.00 ± 50 ppm			MHz
RMIIn_REFCLK duty	—	—	45	—	55	%
RMIIn_REFCLK rising/falling time	t_{CKr}/t_{CKf}	—	0.5	—	4.2	ns

Note 1. In the case of SCKCR3.ETHnREFCLKSEL = 0 (n = 0 to 4)

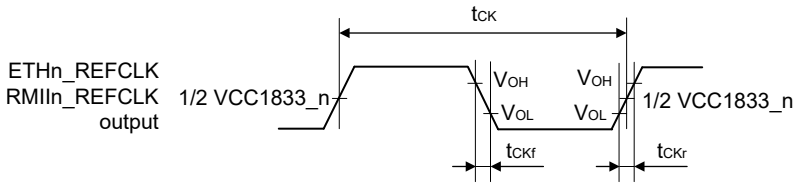


Figure 2.3 Ethernet PHY reference clock output timing

2.5.1.3 EXTCLKIN External Clock Input

Table 2.17 EXTCLKIN clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
EXTCLKIN external clock frequency	$f_{EXTCLKIN}$	—	25.00 ± 50 ppm			MHz
		EtherCAT in use	25.00 ± 25 ppm			MHz
EXTCLKIN duty	$r_{EXTCLKIN}$	—	±5%			—
EXTCLKIN rising time	$t_{rEXTCLKIN}$	—	0	—	5	ns
EXTCLKIN falling time	$t_{fEXTCLKIN}$	—	0	—	5	ns

Note: When using crystal resonator (i.e. EXTAL/XTAL clock is used), EXTCLKIN should be driven low.

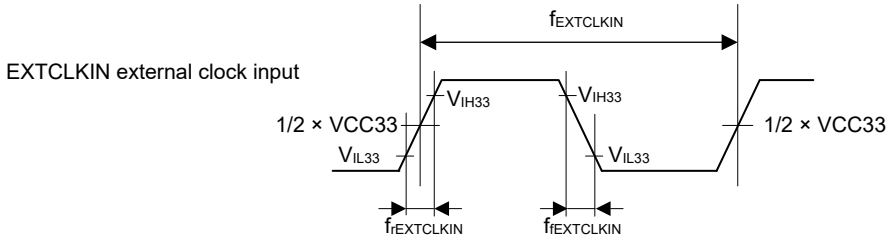


Figure 2.4 EXTCLKIN external clock input timing

2.5.1.4 EXTAL/XTAL Clock Timing

Table 2.18 EXTAL/XTAL clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
EXTAL/XTAL clock frequency*1	f_{XTAL}	—	25.00 ± 50 ppm			MHz
		EtherCAT in use	25.00 ± 25 ppm			MHz

Note: When using an external oscillator, be sure to leave XTAL open-circuit and make sure that EXTAL is driven low.
Note 1. When using the EXTAL/XTAL clock (i.e. crystal resonator), ask the oscillator manufacturer to evaluate oscillation of the oscillator. For the oscillation stabilization time, see the evaluation result provided by the oscillator manufacturer.

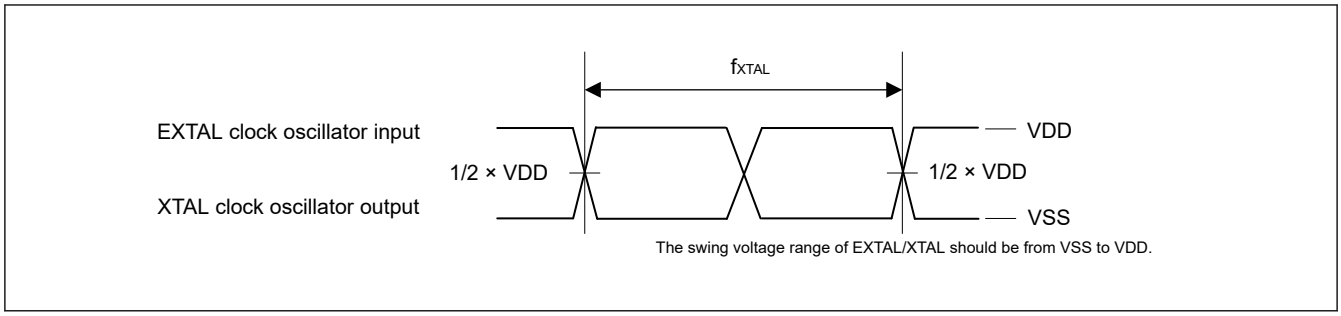


Figure 2.5 EXTAL clock oscillator input and XTAL clock oscillator output timing

2.5.1.5 LOCO Clock Timing

Table 2.19 LOCO clock timing

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
LOCO clock cycle time	t_{Lcyc}	—	4.62	4.17	3.79	µs
LOCO clock oscillation frequency	t_{LOCO}	—	216	240	264	kHz
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	—	40	µs

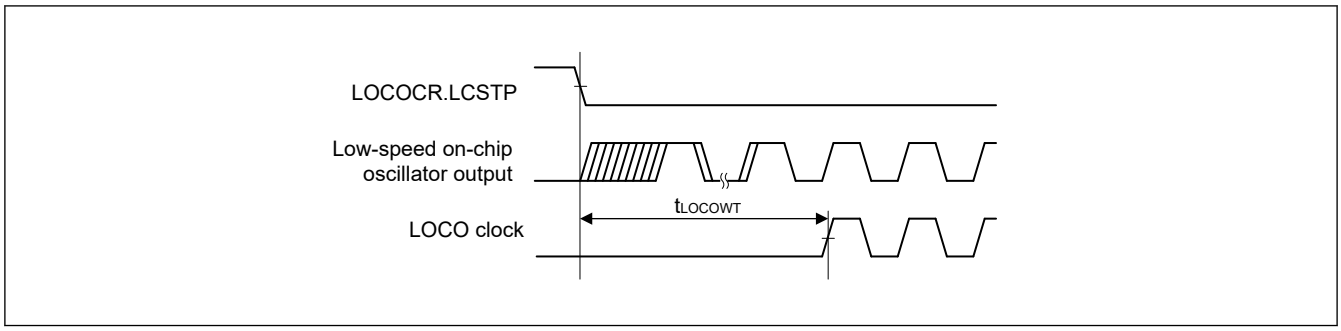


Figure 2.6 LOCO clock oscillation start timing

2.5.2 Reset, Interrupt, and Mode Timing

Table 2.20 Reset, interrupt, and mode timing

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
RES# pulse width	At power on	$t_{dlyreset}$	Figure 2.7	10	—	—	ms
	Other than above	$t_{dlyreset2}$		1	—	—	ms
RES# rising time		$t_{risereset}$		—	—	150	µs
TRST# pulse width	At power on	$t_{dlyreset}$		10	—	—	ms
	Other than above	$t_{dlyreset2}$		1	—	—	ms
TRST# rising time		$t_{risereset}$		—	—	150	µs
SEI pulse width	Level detection	t_{SEIW}	Figure 2.8	t_{PHcyc} × 2.5*1	—	—	ns
	Edge detection			t_{PMcyc} × 3.5*2*3	—	—	ns
IRQ pulse width	Level detection	t_{IRQW}	Figure 2.9	t_{PHcyc} × 2.5*1	—	—	ns
	Edge detection			t_{PMcyc} × 3.5*2*3	—	—	ns
Mode hold time (to RES#)	At power on	t_{MDH}	Figure 2.10	250	—	—	ns

Note 1. t_{PHcyc}: PCLKH cycle
Note 2. t_{PMcyc}: PCLKM cycle
Note 3. This value is when noise filter sampling frequency divided rate is 1. In other cases, it is [clock division rate] × t_{PMcyc} × 3.5.

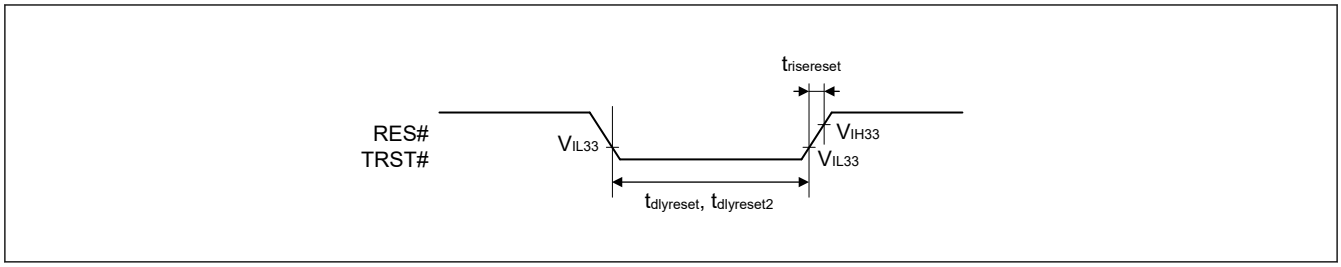


Figure 2.7 Reset input timing

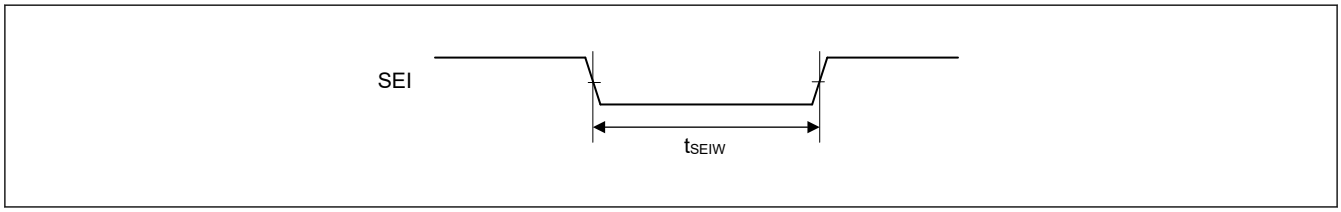


Figure 2.8 SEI interrupt input timing

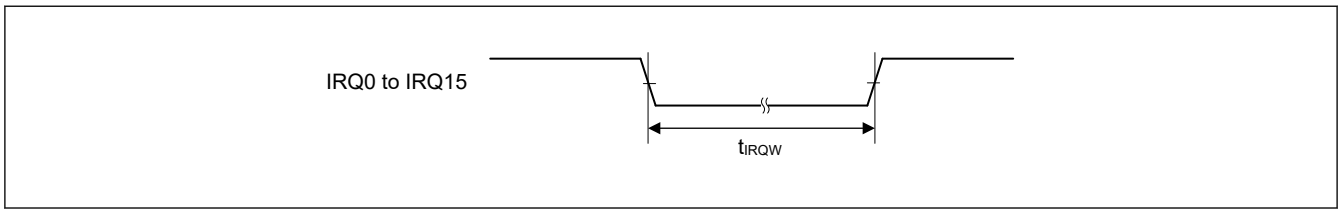


Figure 2.9 IRQ interrupt input timing

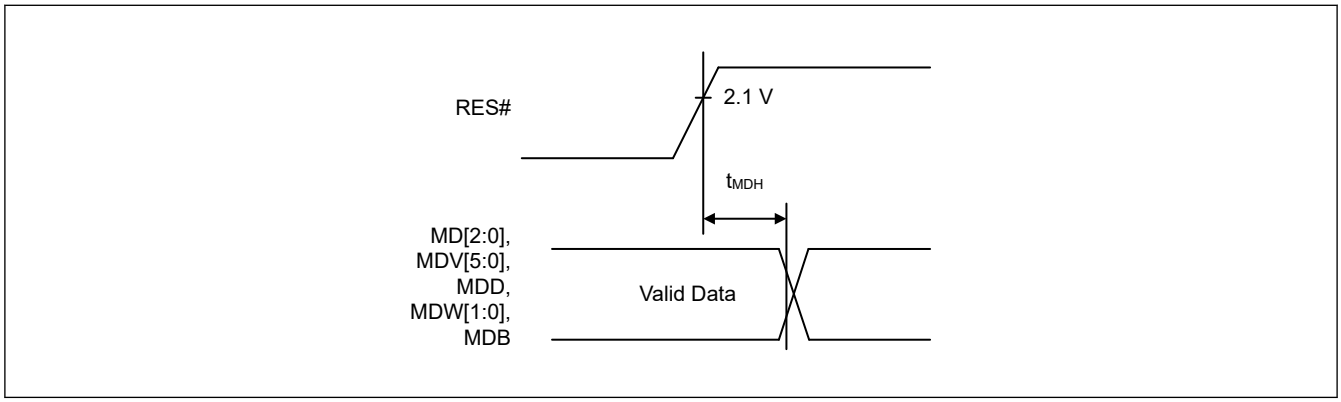


Figure 2.10 Mode input timing

2.5.3 Bus Timing

Table 2.21 Bus timing (1 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (CKIO), 30 pF (others), $T_j$min = −40°C

Parameter	Symbol	CKIO = 1/t_{CKcyc} *1 (Max 66 MHz)		Unit	Reference Figure
		Min.	Max.		
Address delay time 1	t_{AD1}	0	10	ns	Figure 2.11 to Figure 2.18
Address delay time 2	t_{AD2}	1/2t_{CKcyc}	1/2t_{CKcyc} + 10	ns	Figure 2.18
Address setup time	t_{AS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18
Chip enable setup time	t_{CS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18

Table 2.21 Bus timing (2 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (CKIO), 30 pF (others), $T_j$min = −40°C

Parameter		Symbol	CKIO = $1/t_{CKcyc}$ *1 (Max 66 MHz) Min.	Max.	Unit	Reference Figure
Address hold time		t_{AH}	0	—	ns	Figure 2.11 to Figure 2.14
BS delay time		t_{BSD}	—	11	ns	Figure 2.11 to Figure 2.18
CSn# delay time 1		t_{CSD1}	0	10	ns	Figure 2.11 to Figure 2.18
Read/write delay time 1		t_{RWD1}	0	10	ns	Figure 2.11 to Figure 2.18
Read strobe delay time		t_{RSD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 2.11 to Figure 2.18
Read data setup time 1*2	High-drive output	t_{RDS1}	$1/2t_{CKcyc}$ + 4	—	ns	Figure 2.11 to Figure 2.17
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns	
Read data setup time 3*2	High-drive output	t_{RDS3}	$1/2t_{CKcyc}$ + 4	—	ns	Figure 2.18
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns	
Read data hold time 1		t_{RDH1}	0	—	ns	Figure 2.11 to Figure 2.17
Read data hold time 3		t_{RDH3}	0	—	ns	Figure 2.18
Write enable delay time 1		t_{WED1}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 2.11 to Figure 2.16
Write enable delay time 2		t_{WED2}	—	11	ns	Figure 2.17
Write data delay time 1		t_{WDD1}	—	11	ns	Figure 2.11 to Figure 2.17
Write data hold time 1		t_{WDH1}	1	—	ns	Figure 2.11 to Figure 2.17
Write data hold time 4		t_{WDH4}	0	—	ns	Figure 2.11 to Figure 2.15
WAIT# setup time*2	High-drive output	t_{WTS}	$1/2t_{CKcyc}$ + 4.5	—	ns	Figure 2.12 to Figure 2.18
	Normal output		$1/2t_{CKcyc}$ + 8	—	ns	
WAIT# hold time		t_{WTH}	$1/2t_{CKcyc}$ + 3.5	—	ns	Figure 2.12 to Figure 2.18
AH# delay time		t_{AHD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 2.15
Multiplex address delay time		t_{MAD}	—	10	ns	Figure 2.15
Multiplex address hold time		t_{MAH}	1	—	ns	Figure 2.15
Address setup time to AH#		t_{AVVH}	$1/2t_{CKcyc}$ − 2	—	ns	Figure 2.15
DACK/TEND delay time		t_{DACD}	See section 2.5.4. DMAC Timing		ns	Figure 2.11 to Figure 2.18

Note: Notation of $1/2t_{CKcyc}$ in the delay time, setup time, and hold time shows 1/2 cycles from the clock rising edge, that is, the reference of clock falling.

Note 1. Take the number of cycles of waiting that suits the system configuration into consideration with regard to the fmax value for CKIO (the external bus clock). When CKIO is running at 50 MHz or a higher frequency, select high drive output.

Note 2. These are values when high-drive output and normal output are respectively selected for CKIO.

Table 2.22 Bus timing (1 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 12 pF (CKIO), 12 pF (others), $T_j$min = −20°C

Parameter	Symbol	CKIO = $1/t_{CKcyc}$ *1 (Max 100 MHz) Min.	Max.	Unit	Reference Figure
Address delay time 1	t_{AD1}	0	8	ns	Figure 2.11 to Figure 2.18
Address delay time 2	t_{AD2}	$1/2t_{CKcyc}$ - 0.5	$1/2t_{CKcyc}$ + 8	ns	Figure 2.18
Address setup time	t_{AS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18

Table 2.22 Bus timing (2 of 2)

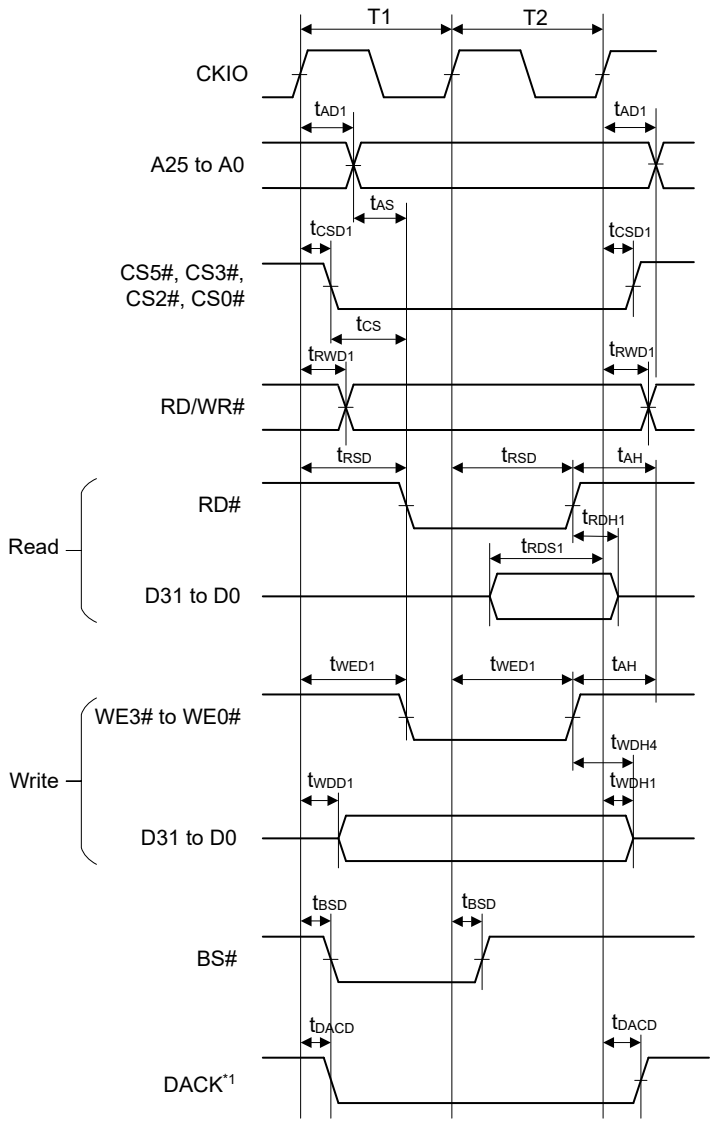
Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 12 pF (CKIO), 12 pF (others), $T_j$min = −20°C

Parameter		Symbol	CKIO = 1/t_{CKcyc} *1 (Max 100 MHz) Min.	Max.	Unit	Reference Figure
Chip enable setup time		t_{CS}	0	—	ns	Figure 2.11 to Figure 2.14, Figure 2.18
Address hold time		t_{AH}	0	—	ns	Figure 2.11 to Figure 2.14
BS delay time		t_{BSD}	—	8	ns	Figure 2.11 to Figure 2.18
CSn# delay time 1		t_{CSD1}	0	8	ns	Figure 2.11 to Figure 2.18
Read/write delay time 1		t_{RWD1}	0	8	ns	Figure 2.11 to Figure 2.18
Read strobe delay time		t_{RSD}	1/2t_{CKcyc}	1/2t_{CKcyc} + 8	ns	Figure 2.11 to Figure 2.18
Read data setup time 1*2	High-drive output	t_{RDS1}	1/2t_{CKcyc} + 4.5	—	ns	Figure 2.11 to Figure 2.17
	Normal output		1/2t_{CKcyc} + 7	—	ns	
Read data setup time 3*2	High-drive output	t_{RDS3}	1/2t_{CKcyc} + 4.5	—	ns	Figure 2.18
	Normal output		1/2t_{CKcyc} + 7	—	ns	
Read data hold time 1		t_{RDH1}	0	—	ns	Figure 2.11 to Figure 2.17
Read data hold time 3		t_{RDH3}	0	—	ns	Figure 2.18
Write enable delay time 1		t_{WED1}	1/2t_{CKcyc}	1/2t_{CKcyc} + 8	ns	Figure 2.11 to Figure 2.16
Write enable delay time 2		t_{WED2}	—	9	ns	Figure 2.17
Write data delay time 1		t_{WDD1}	—	8	ns	Figure 2.11 to Figure 2.17
Write data hold time 1		t_{WDH1}	1	—	ns	Figure 2.11 to Figure 2.17
Write data hold time 4		t_{WDH4}	0	—	ns	Figure 2.11 to Figure 2.15
WAIT# setup time*2	High-drive output	t_{WTS}	1/2t_{CKcyc} + 4.5	—	ns	Figure 2.12 to Figure 2.18
	Normal output		1/2t_{CKcyc} + 8	—	ns	
WAIT# hold time		t_{WTH}	1/2t_{CKcyc} + 3.5	—	ns	Figure 2.12 to Figure 2.18
AH# delay time		t_{AHD}	1/2t_{CKcyc}	1/2t_{CKcyc} + 8	ns	Figure 2.15
Multiplex address delay time		t_{MAD}	—	8	ns	Figure 2.15
Multiplex address hold time		t_{MAH}	1	—	ns	Figure 2.15
Address setup time to AH#		t_{AVVH}	1/2t_{CKcyc} − 2	—	ns	Figure 2.15
DACK/TEND delay time		t_{DACD}	See section 2.5.4. DMAC Timing		ns	Figure 2.11 to Figure 2.18

Note: Notation of 1/2t_{CKcyc} in the delay time, setup time, and hold time shows 1/2 cycles from the clock rising edge, that is, the reference of clock falling.

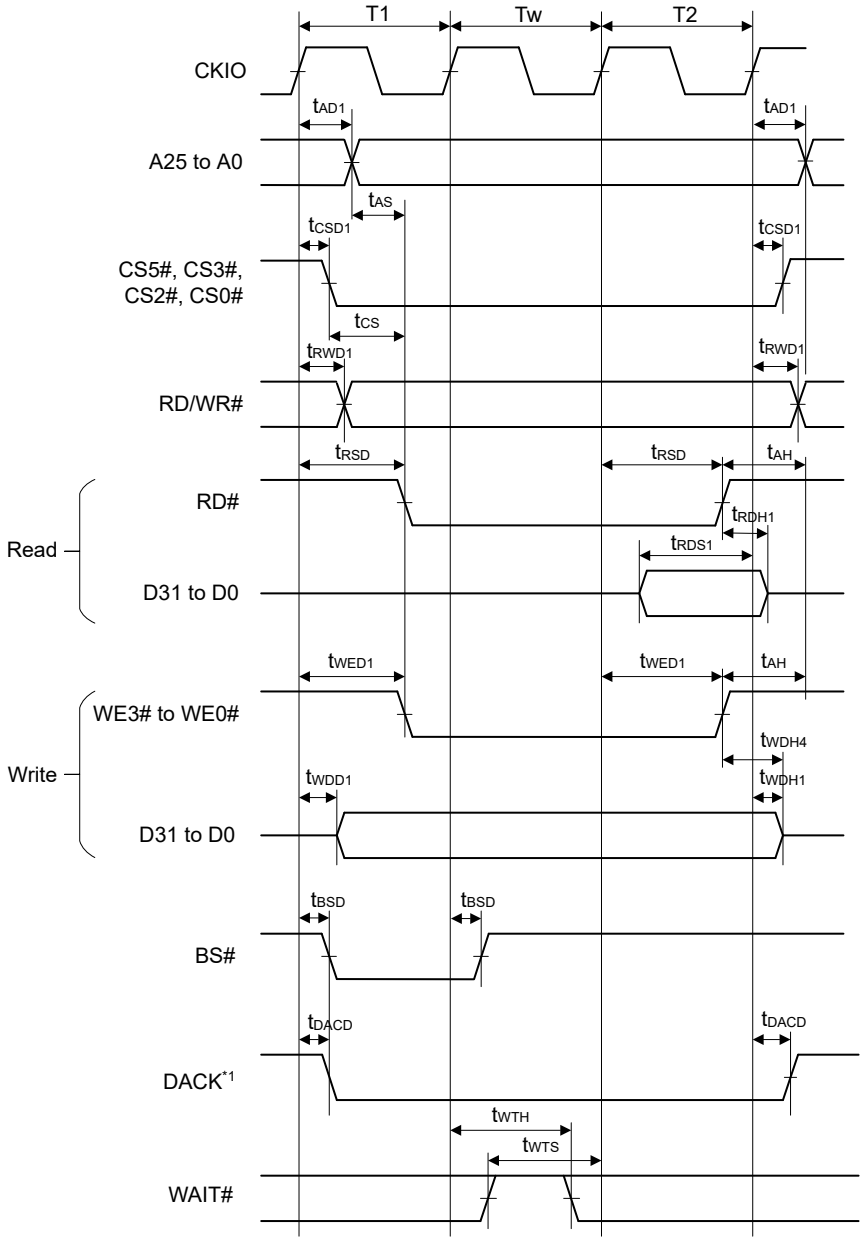
Note 1. Take the number of cycles of waiting that suits the system configuration into consideration with regard to the fmax value for CKIO (the external bus clock). When CKIO is running at 50 MHz or a higher frequency, select high drive output.

Note 2. These are values when high-drive output and normal output are respectively selected for CKIO.



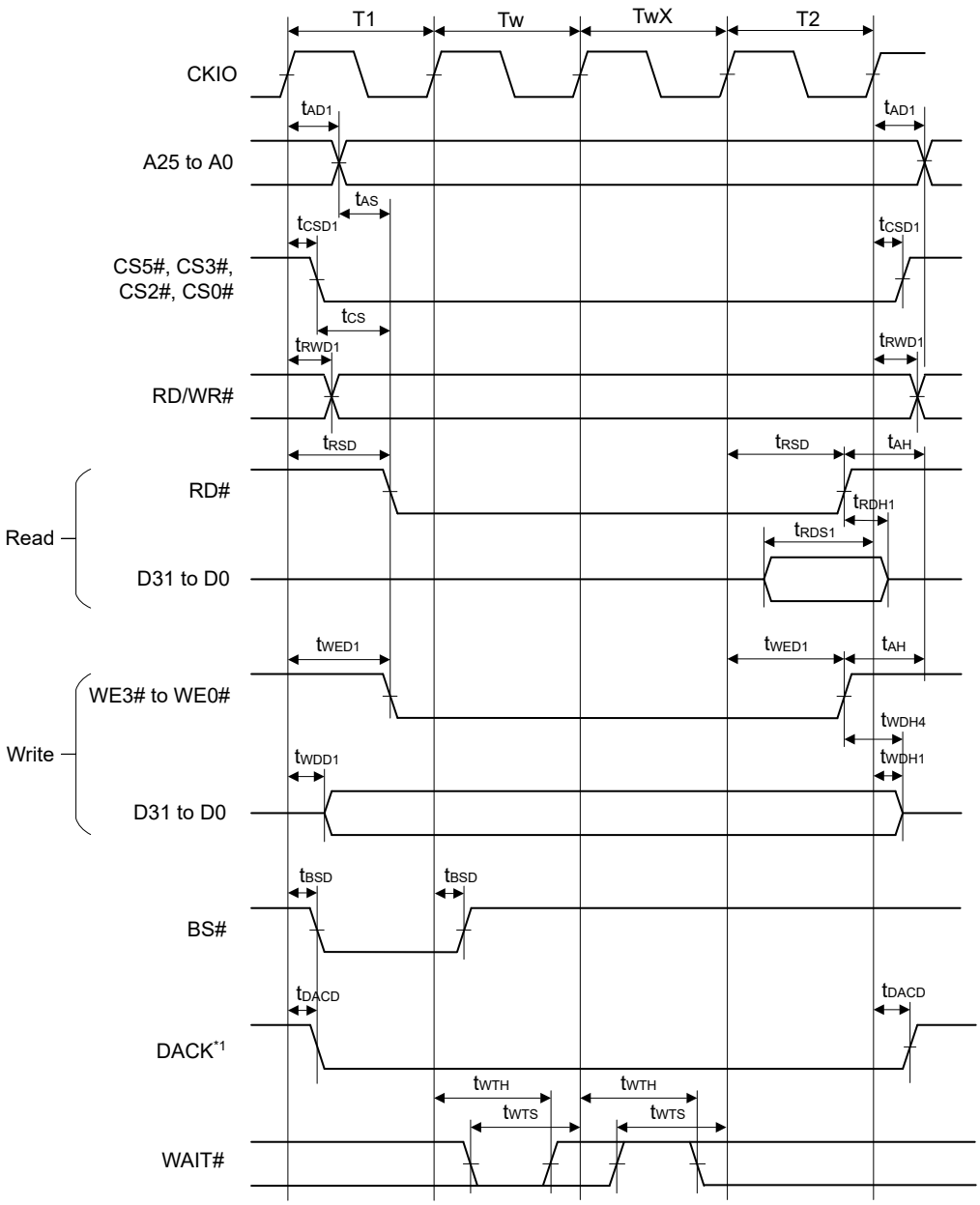
Note 1. DACK is waveform when active-low is specified.

Figure 2.11 SRAM interface basic bus cycle (no wait)



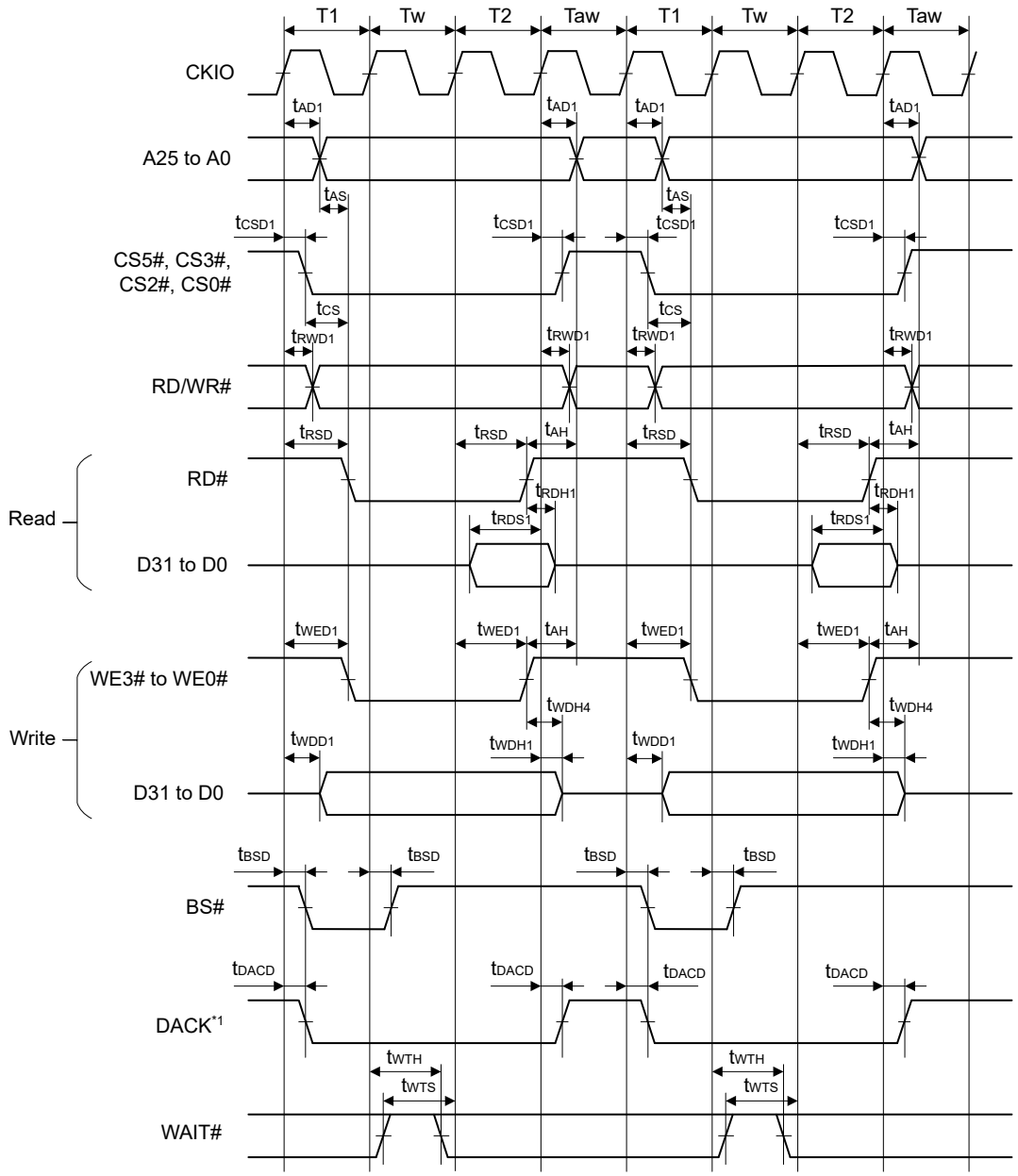
Note 1. DACK is waveform when active-low is specified.

Figure 2.12 SRAM interface basic bus cycle (software wait 1)



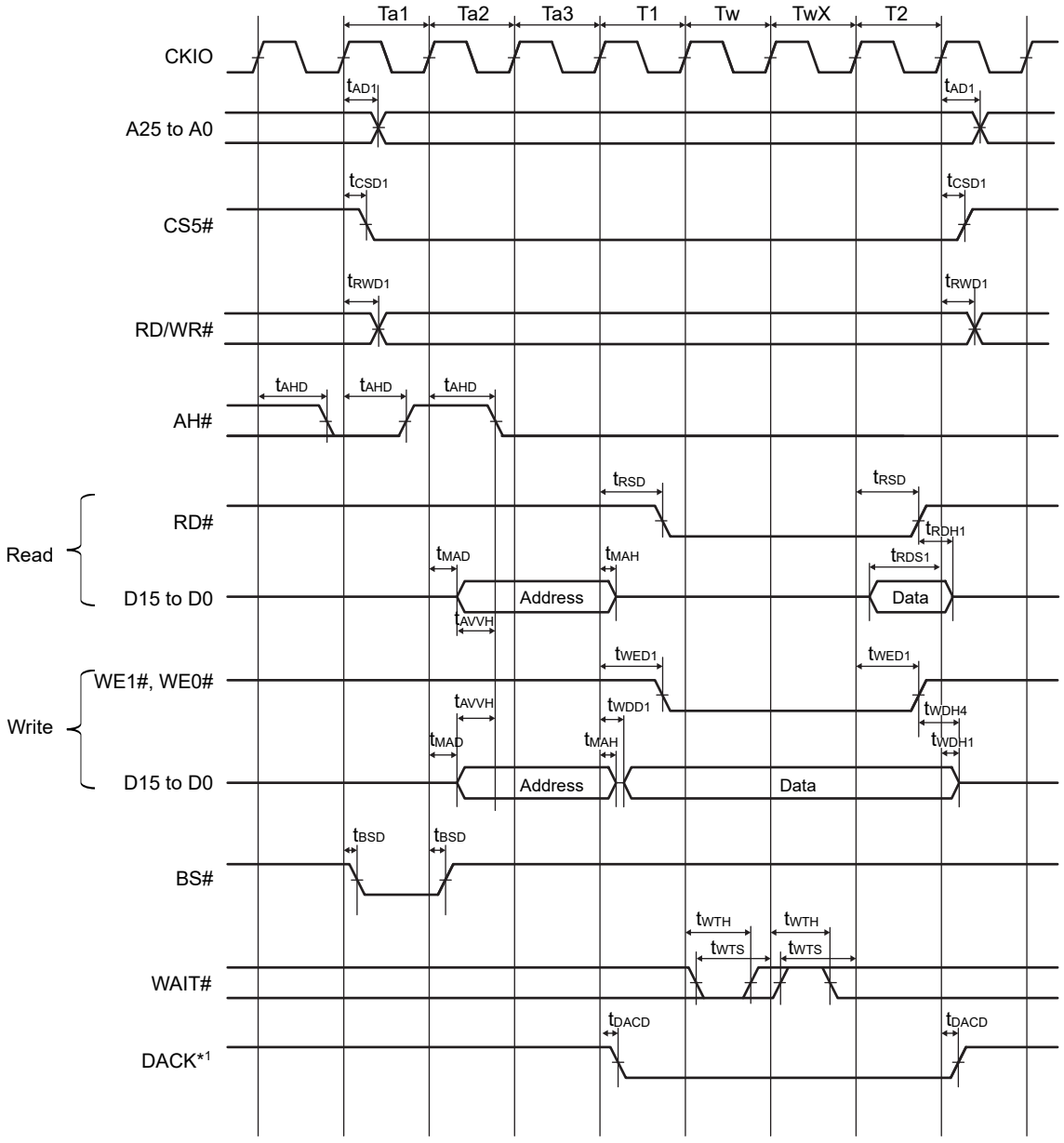
Note 1. DACK is waveform when active-low is specified.

Figure 2.13 SRAM interface basic bus cycle (software wait 1, external wait 1 inserted)



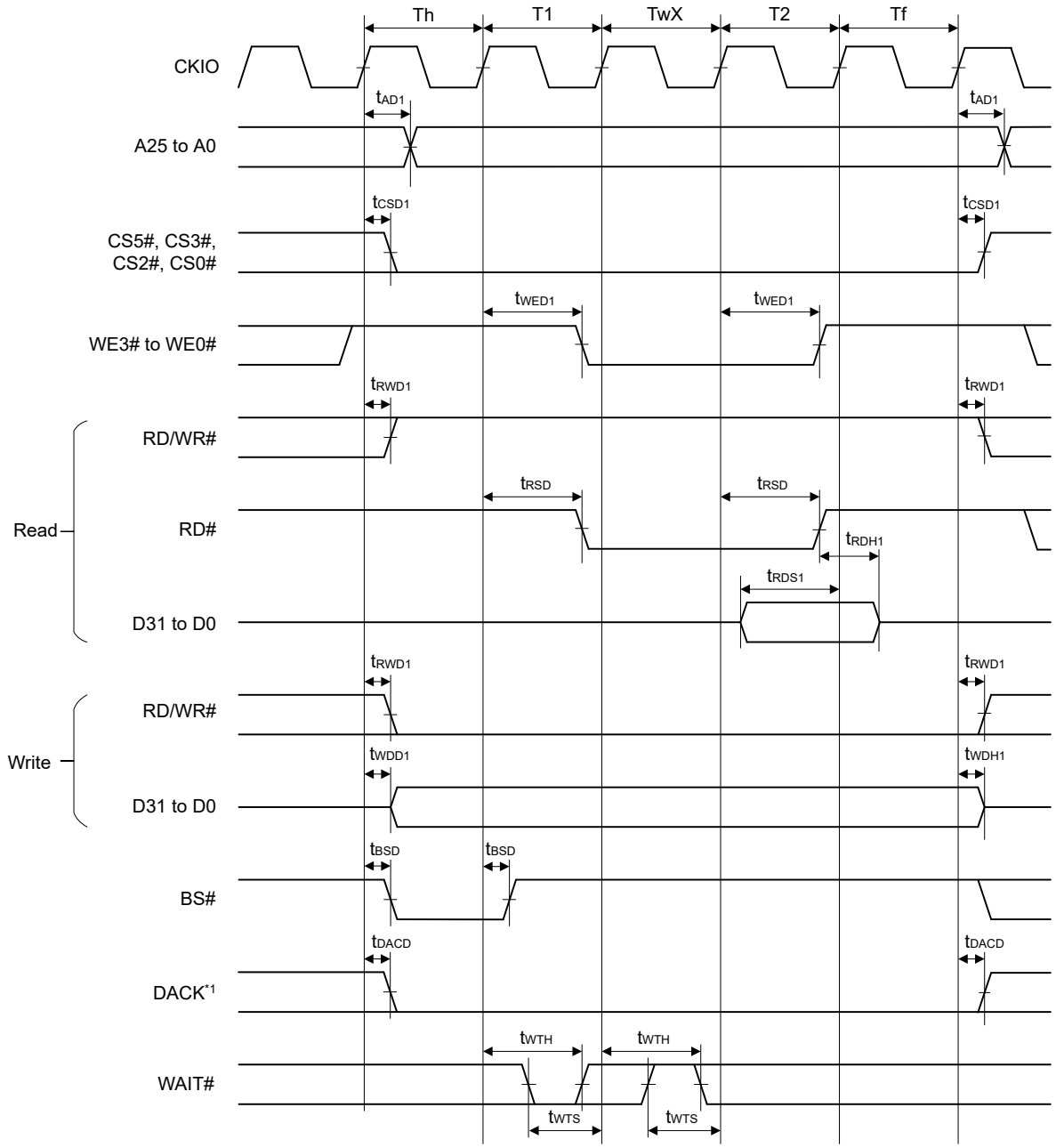
Note 1. DACK is waveform when active-low is specified.

Figure 2.14 SRAM interface basic bus cycle (software wait 1, external wait enabled (WM = 0), no idle cycle)



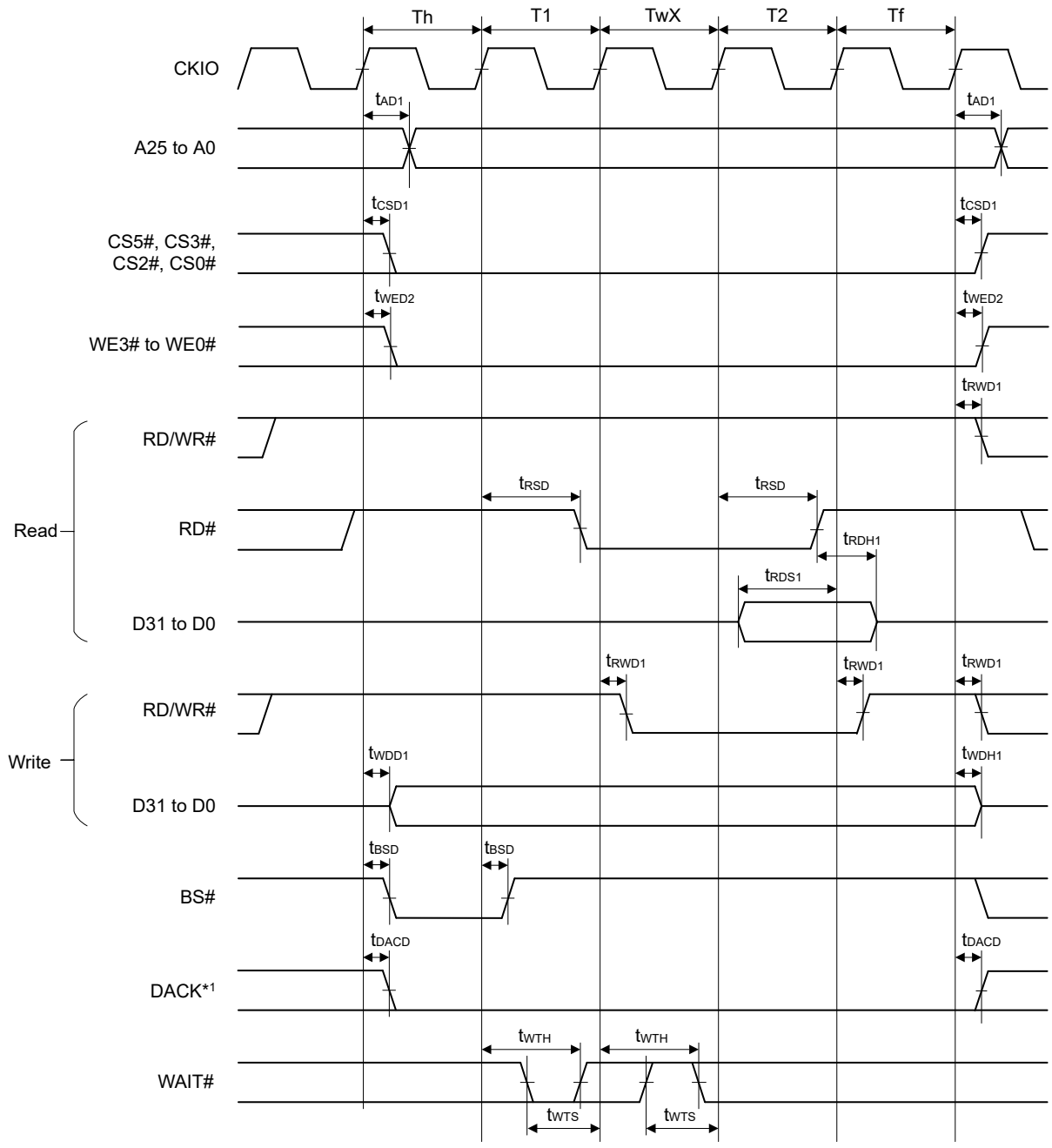
Note 1. DACK is waveform when active-low is specified.

Figure 2.15 MPX-I/O interface bus cycle (address cycle 3, software wait 1, external wait 1 inserted)



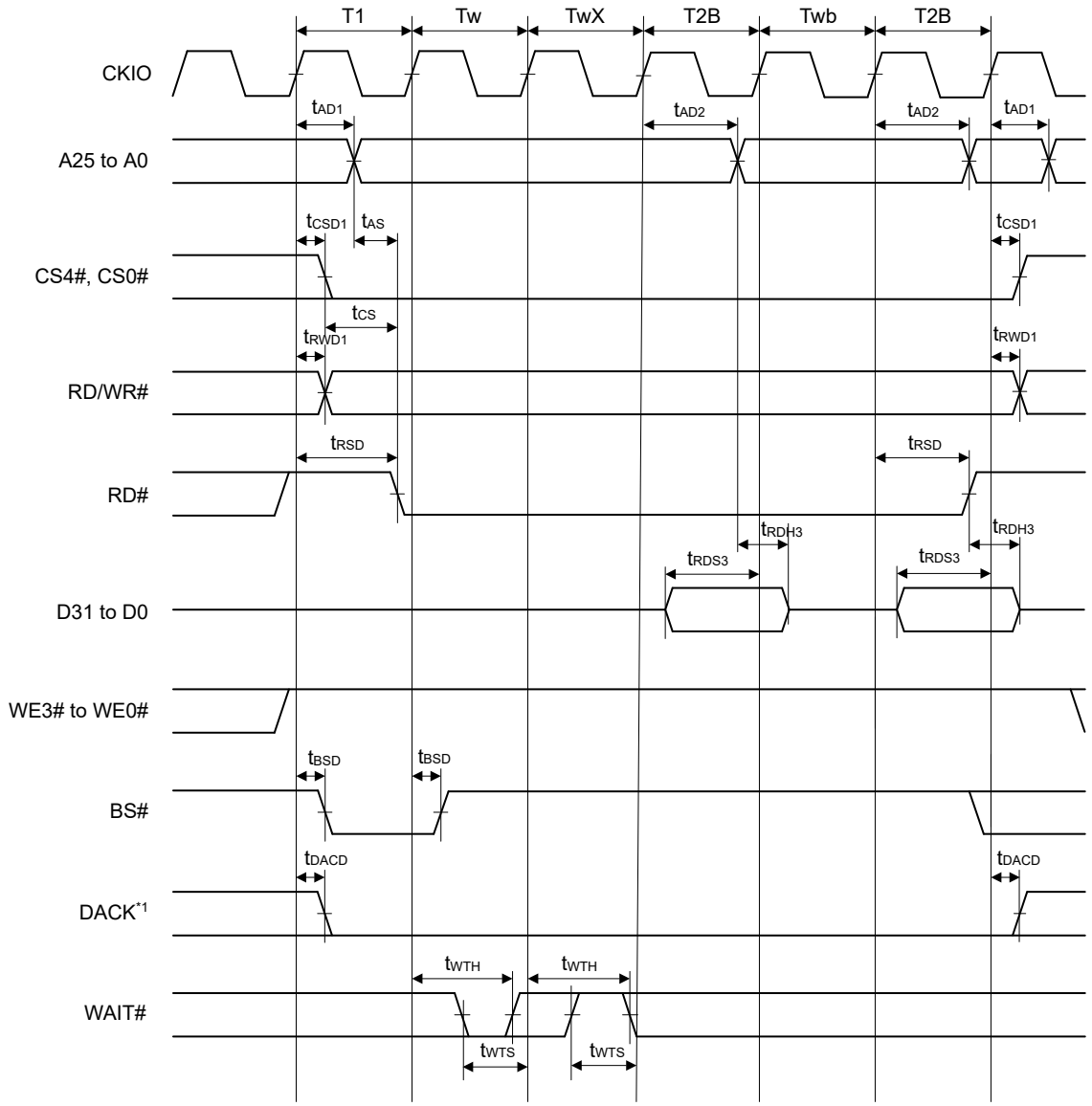
Note 1. DACK is waveform when active-low is specified.

Figure 2.16 SRAM bus cycle with byte selection (SW = 1 cycle, HW = 1 cycle, asynchronous external wait 1 inserted, BAS = 0 (write cycle UB/LB control))



Note 1. DACK is waveform when active-low is specified.

Figure 2.17 SRAM bus cycle with byte selection (SW = 1 cycle, HW = 1 cycle, asynchronous external wait 1 inserted, BAS = 1 (write cycle WE control))



Note 1. DACK is waveform when active-low is specified.

Figure 2.18 Burst ROM read cycle (software wait 1, asynchronous external wait 1 inserted, burst wait 1, 2)

2.5.4 DMAC Timing

Table 2.23 DMAC timing

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (CKIO), 30 pF (others), $T_j$min = −40°C

Parameter		Symbol	Min.*1	Max.	Unit	Reference figure
DMAC	DREQ pulse width	t_{DRQW}	t_{PHcyc} × 2	—	ns	Figure 2.19
	DACK and TEND delay time	t_{DACD}	0	10	ns	Figure 2.20

Note 1. t_{PHcyc}: PCLKH cycle

Table 2.24 DMAC timing

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 12 pF (CKIO), 12 pF (others), $T_j$min = −20°C

Parameter		Symbol	Min.*1	Max.	Unit	Reference figure
DMAC	DREQ pulse width	t_{DRQW}	t_{PHcyc} × 2	—	ns	Figure 2.19
	DACK and TEND delay time	t_{DACD}	-0.5	8	ns	Figure 2.20

Note 1. t_{PHcyc}: PCLKH cycle

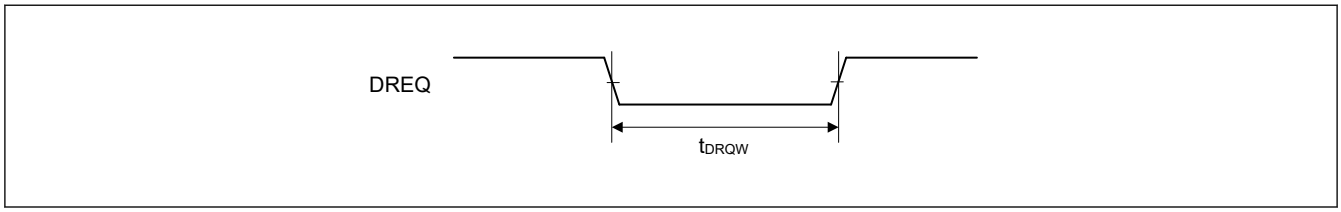


Figure 2.19 DREQ input timing

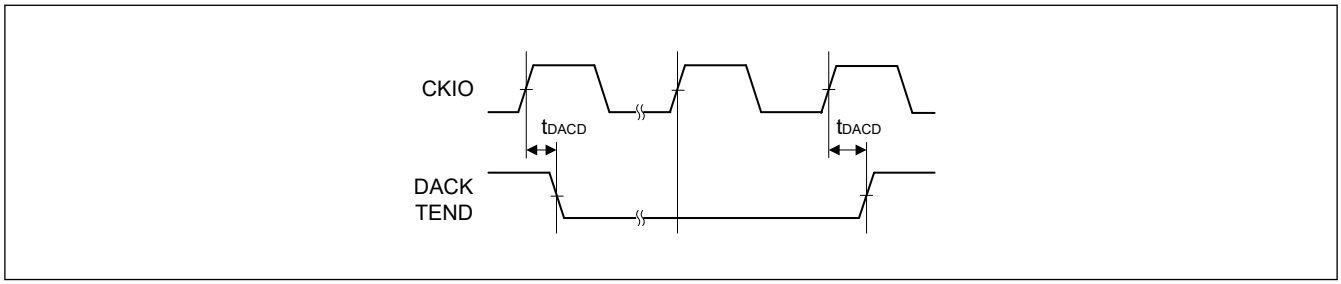


Figure 2.20 DACK and TEND output timing

2.5.5 On-Chip Peripheral Module Timing

2.5.5.1 I/O Port Timing

Table 2.25 I/O port timing

Parameter		Symbol	Min.	Max.	Unit*1	Reference figure
I/O port	Input data pulse width	t_{PRW}	1.5	—	t_{PLcyc}	Figure 2.21

Note 1. t_{PLcyc}: PCLKL cycle

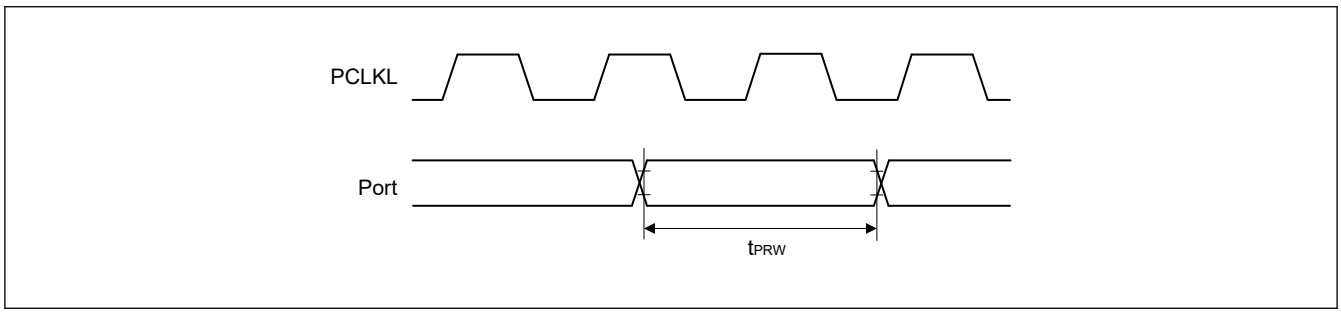


Figure 2.21 I/O port input timing

2.5.5.2 CMTW Timing

Table 2.26 CMTW timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PLcyc}	Figure 2.22
		Both-edge setting		2.5	—		

Note 1. t_{PLcyc}: PCLKL cycle

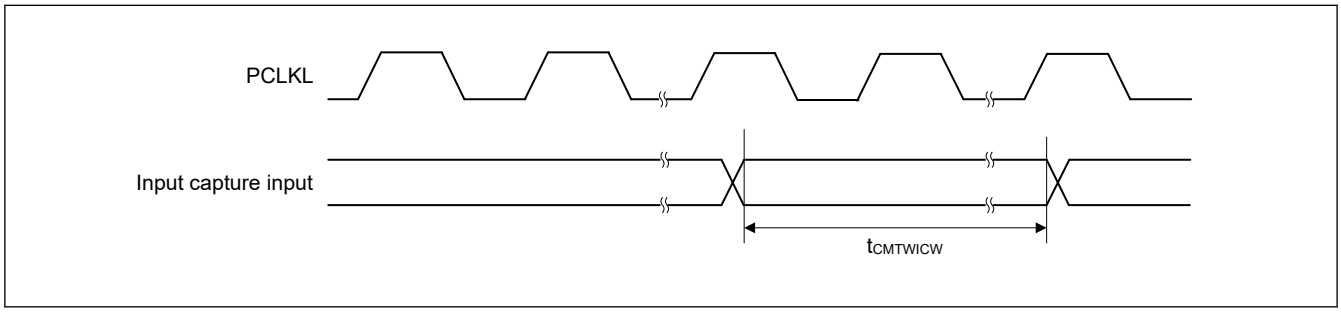


Figure 2.22 CMTW input capture input timing

2.5.5.3 MTU3 Timing

Table 2.27 MTU3 timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
MTU3	Input capture input pulse width	Single-edge setting	t_{MTICW}	2.5	—	t_{PHcyc}	Figure 2.23
		Both-edge setting		3.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	2.5	—	t_{PHcyc}	Figure 2.24
		Both-edge setting		3.5	—		
		Phase counting mode		3.5	—		

Note 1. t_{PHcyc}: PCLKH cycle

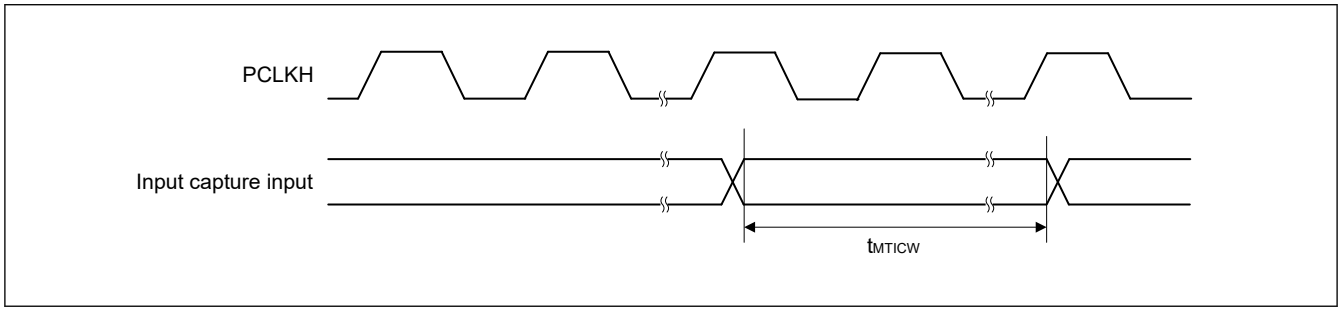


Figure 2.23 MTU3 input capture input timing

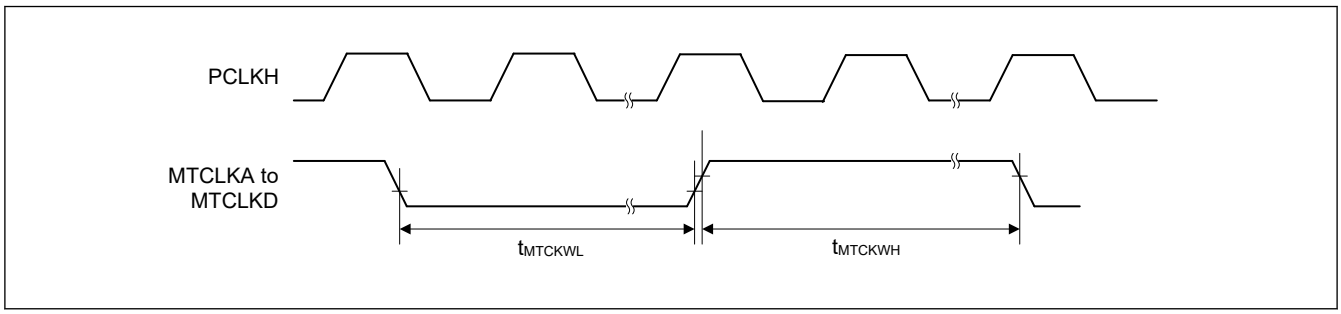


Figure 2.24 MTU3 clock input timing

2.5.5.4 POE3 Timing

Table 2.28 POE3 timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
POE3	POEn# input pulse width		t_{POEW}	2.5	—	t_{PHcyc}	Figure 2.25
	Output disable time	Transition of the POEn# signal level	t_{POEDI}	—	5 × PCLKH + 0.1	µs	Figure 2.26
		Simultaneous conduction of output pins	t_{POEDO}	—	3 × PCLKH + 0.1	µs	Figure 2.27
		Register setting	t_{POEDS}	—	PCLKH + 0.1	µs	Figure 2.28
		Oscillation stop detection	t_{POEDOS}	—	74	µs	Figure 2.29

Note 1. t_{PHcyc}: PCLKH cycle

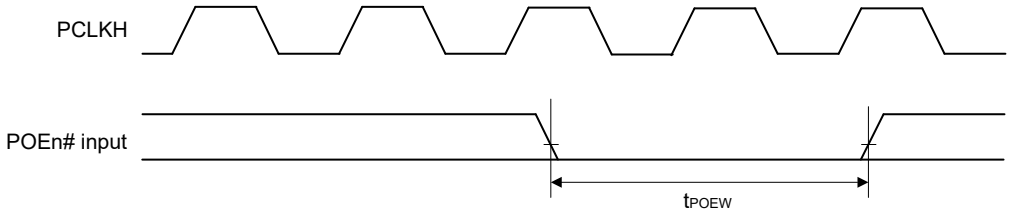


Figure 2.25 POEn# input pulse timing

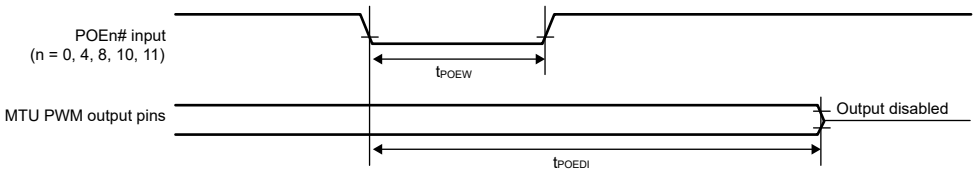
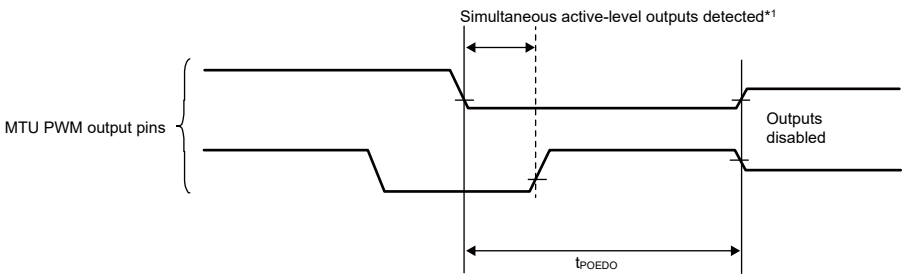


Figure 2.26 Output disable time for POE in response to transition of the POEn# signal level



Note 1. When the active level is set to low.

Figure 2.27 Output disable time for POE in response to the simultaneous conduction of output pins

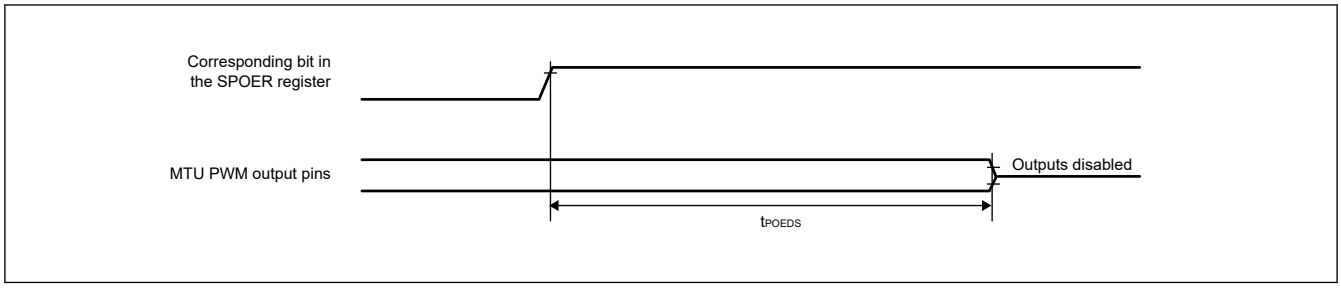


Figure 2.28 Output disable time for POE in response to the register setting

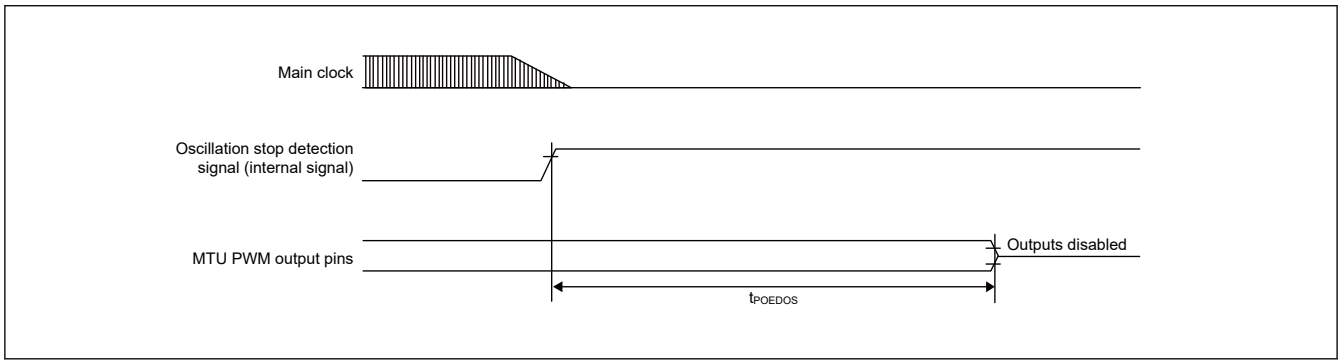


Figure 2.29 Output disable time for POE in response to the oscillation stop detection

2.5.5.5 GPT Timing

Table 2.29 GPT timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
GPT	Input capture input pulse width	Single-edge setting	t_{GTICW}	2.5	—	t_{PHcyc}	Figure 2.30
		Both-edge setting		3.5	—		
	External trigger input pulse width	Single-edge setting	t_{GTEW}	2.5	—	t_{PHcyc}	Figure 2.31
		Both-edge setting		3.5	—		

Note 1. t_{PHcyc}: PCLKH cycle (LLPP channels), PCLKM cycle (Other channels)

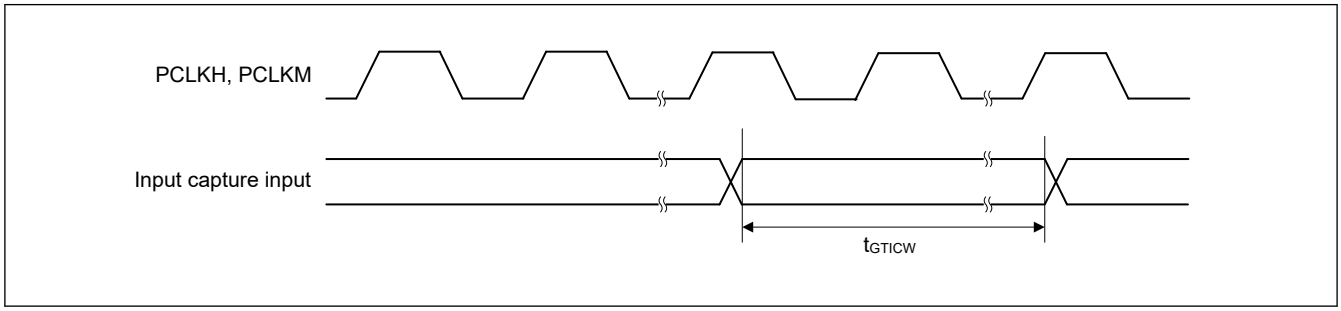


Figure 2.30 GPT input capture input timing

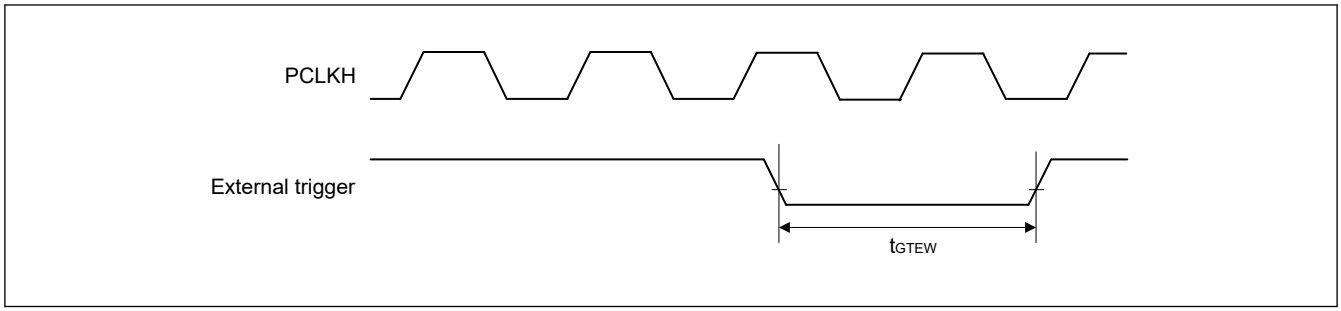


Figure 2.31 GPT external trigger input timing

2.5.5.6 POEG Timing

Table 2.30 POEG timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
POEG	GTETRGn input pulse width (n = A to D)		t_{POEGW}	2.5	—	t_{PHcyc}	Figure 2.32
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	3 × PCLKH + 0.1	µs	Figure 2.33
		Detection of the output stopping signal from GPT (dead time error, simultaneous high output, or simultaneous low output)	t_{POEGDO}	—	0.1	µs	Figure 2.34
		Register setting	t_{POEGDS}	—	PCLKH + 0.1	µs	Figure 2.35
		Oscillation stop detection	$t_{POEGDOS}$	—	74	µs	Figure 2.36

Note 1. t_{PHcyc}: PCLKH cycle (LLPP channels), PCLKL cycle (Other channels)

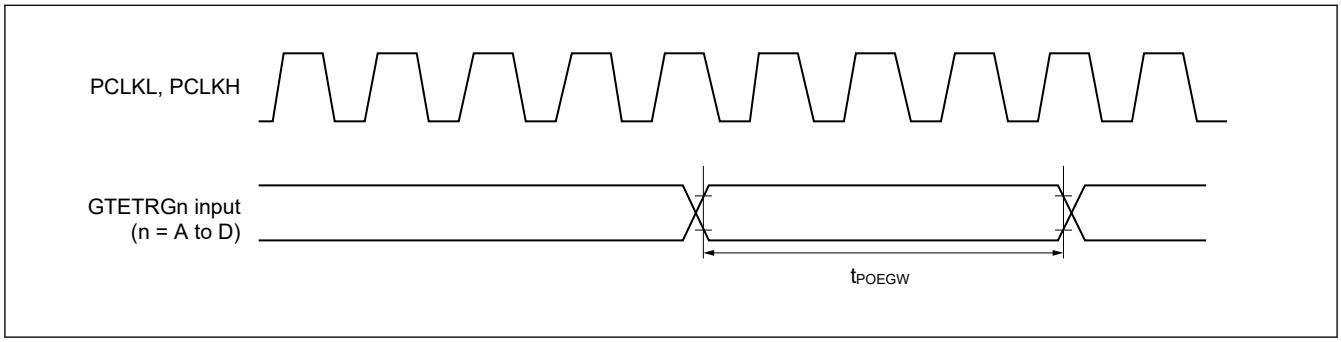


Figure 2.32 POEG input timing

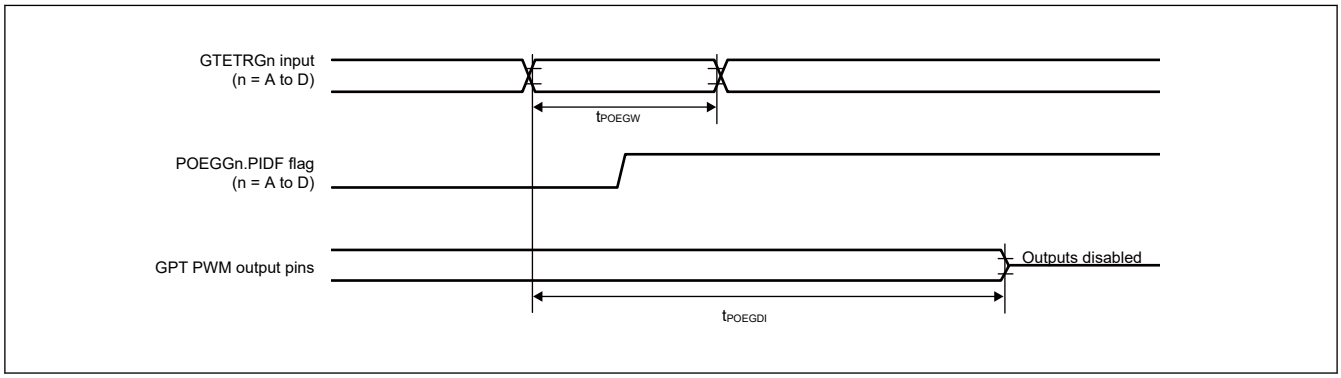
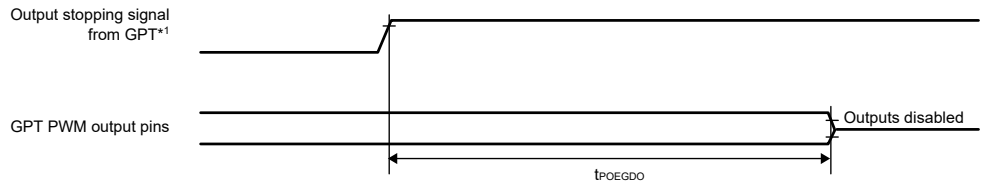


Figure 2.33 Output disable time for POEG via detection flag in response to the input level detection of the GTETRGn pin



Note 1. GPTn.GTST.DTEF (dead time error flag), GPTn.GTST.OABLF (simultaneous low out flag), or GPTn.GTST.OABHF (simultaneous high output flag)

Figure 2.34 Output disable time for POEG in response to detection of the output stopping signal from GPT

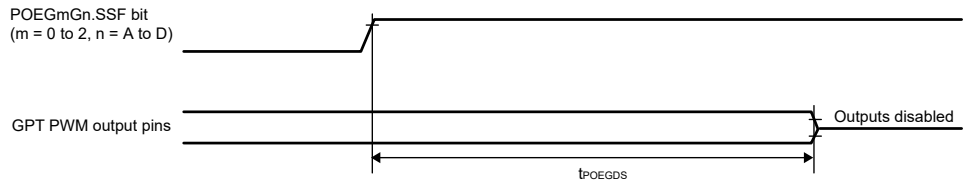


Figure 2.35 Output disable time for POEG in response to the register setting

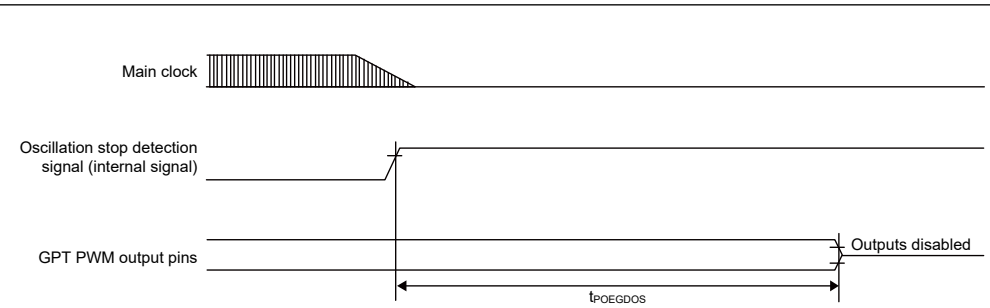


Figure 2.36 Output disable time for POEG in response to the oscillation stop detection

2.5.5.7 A/D Converter Trigger Timing

Table 2.31 A/D converter trigger timing

Parameter			Symbol	Min.	Max.	Unit*1	Reference figure
A/D converter	A/D converter trigger input pulse width	ADTRG0#, ADTRG1#	t_{TRGW}	1.5	—	$t_{PADCcyc}$	Figure 2.37

Note 1. $t_{PADCcyc}$: PCLKADC cycle

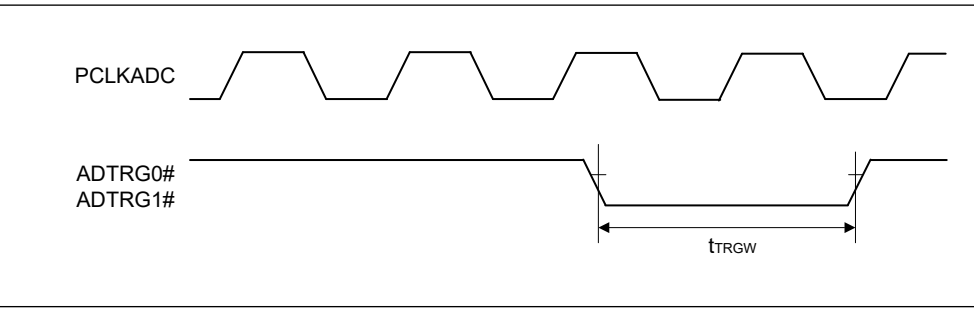


Figure 2.37 A/D converter trigger input timing (ADTRG0#, ADTRG1#)

2.5.5.8 SCI, SCIE Timing

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF (except Simple I2C)

Table 2.32 SCI timing (1 of 2)

Parameter		Symbol	Min.	Max.	Unit	Reference figure
SCI, SCIE (Asynchronous)	Input clock cycle	t_{Scyc}	4	—	$t_{PSCIcyc}$	Figure 2.38
	Input clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time	t_{SCKr}	—	3	ns	
	Input clock fall time	t_{SCKf}	—	3	ns	
	Output clock cycle	t_{Scyc}	6	—	$t_{PSCIcyc}$	
	Output clock pulse width	t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time	t_{SCKr}	—	3	ns	
	Output clock fall time	t_{SCKf}	—	3	ns	
SCI (Simple I2C, Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.39
	SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	2 × NF_{cyc} *1	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
SCI (Simple I2C, Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.39
	SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	2 × NF_{cyc} *1	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Table 2.32 SCI timing (2 of 2)

Parameter			Symbol	Min.	Max.	Unit	Reference figure
SCI (Clock sync, Simple SPI) SCIE (Clock sync)	SCK output clock cycle (master)		t_{SPcyc}	2	65536	$t_{PSCIcyc}$	Figure 2.40 to Figure 2.45
	SCK input clock cycle (slave)			2	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKR}, t_{SPCKF}	—	3	ns	
	Data input setup time	Internal clock	t_{SU}	7	—	ns	
		External clock		4	—		
	Data input hold time	Internal clock	t_H	3	—	ns	
		External clock		4	—		
	Data output delay time	Internal clock	t_{OD}	—	3	ns	
		External clock		—	14		
	Data output hold time	Internal clock	t_{OH}	-3	—	ns	
		External clock		0	—		
	Data rise/fall time		t_{DR}, t_{DF}	—	3	ns	
	Slave access time	Internal clock	t_{SA}	—	3 × $t_{PSCIcyc}$ + 14	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 14		
	Slave output release time	Internal clock	t_{REL}	—	3 × $t_{PSCIcyc}$ + 12	ns	
		External clock		—	3 × $t_{PSCIcyc}$ + 12		
SCI (Simple SPI)	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	SS input rise/fall time		t_{SSR}, t_{SSF}	—	3	ns	

Note: $t_{PSCIcyc}$: PCLKSCIn cycle

Note 1. $N_{Fcyc} = 4^n \times 2^{m-1} \times t_{PSCIcyc}$
n: CCR2.CKS[1:0] (n = 0, 1, 2, 3)
m: CCR1.NFCS[2:0] (m = 1, 2, 3, 4)

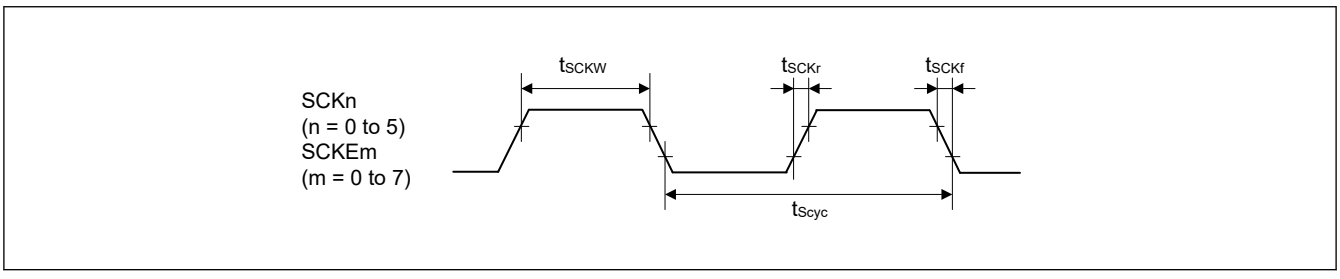
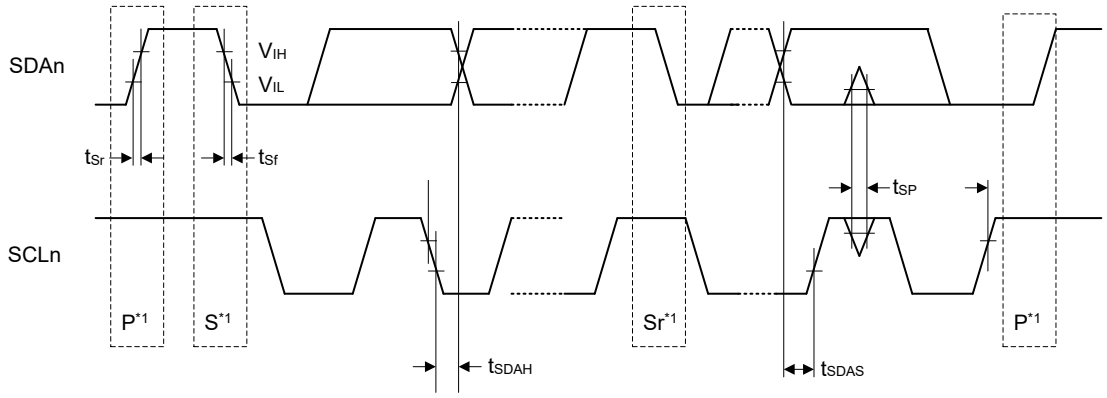


Figure 2.38 SCK clock input/output timing



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.39 SCI simple I2C mode timing

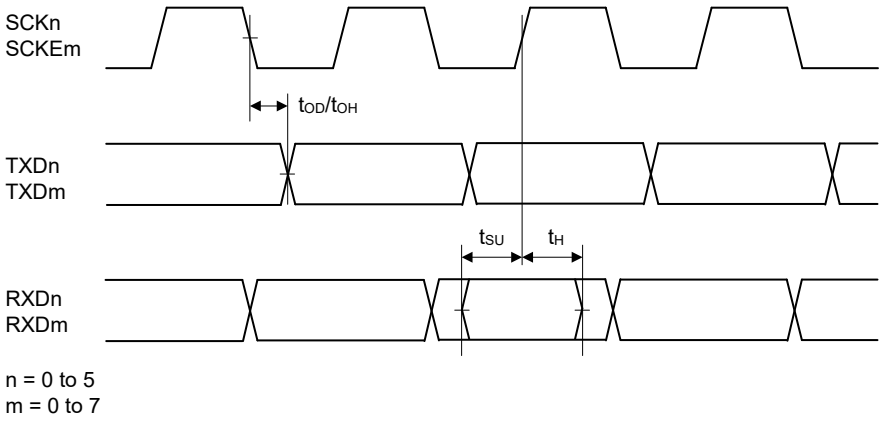
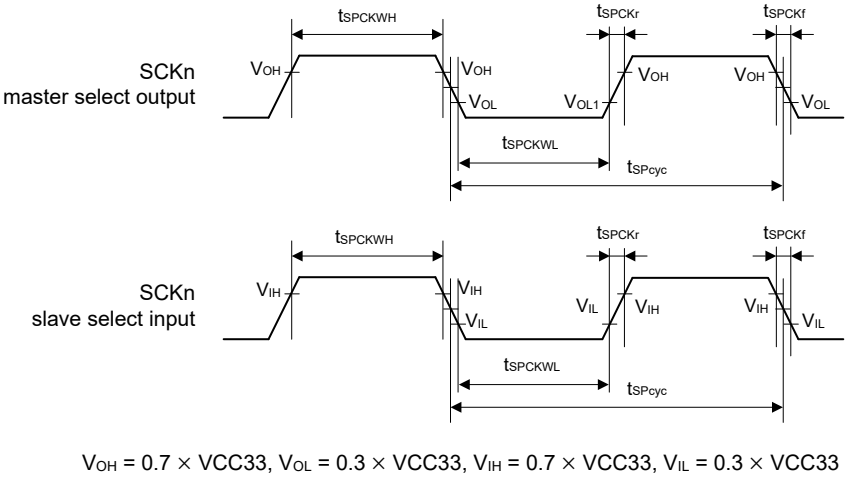


Figure 2.40 SCI input/output timing in clock synchronous mode



V_{OH} = 0.7 × VCC33, V_{OL} = 0.3 × VCC33, V_{IH} = 0.7 × VCC33, V_{IL} = 0.3 × VCC33

Figure 2.41 SCI simple SPI mode clock timing

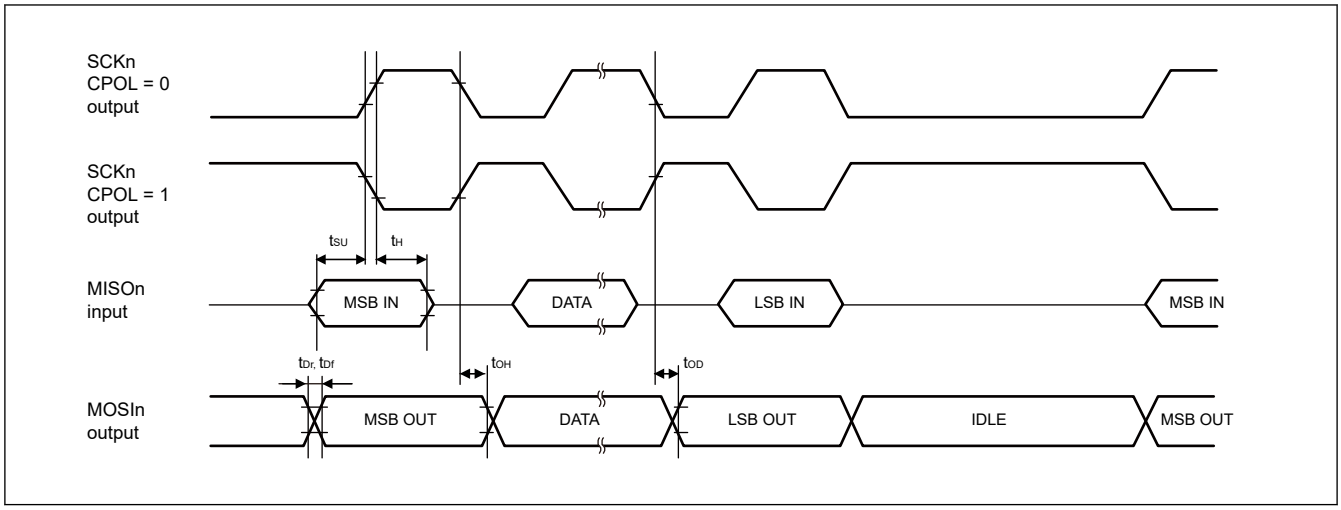


Figure 2.42 SCI simple SPI mode timing for master when CPHA = 0

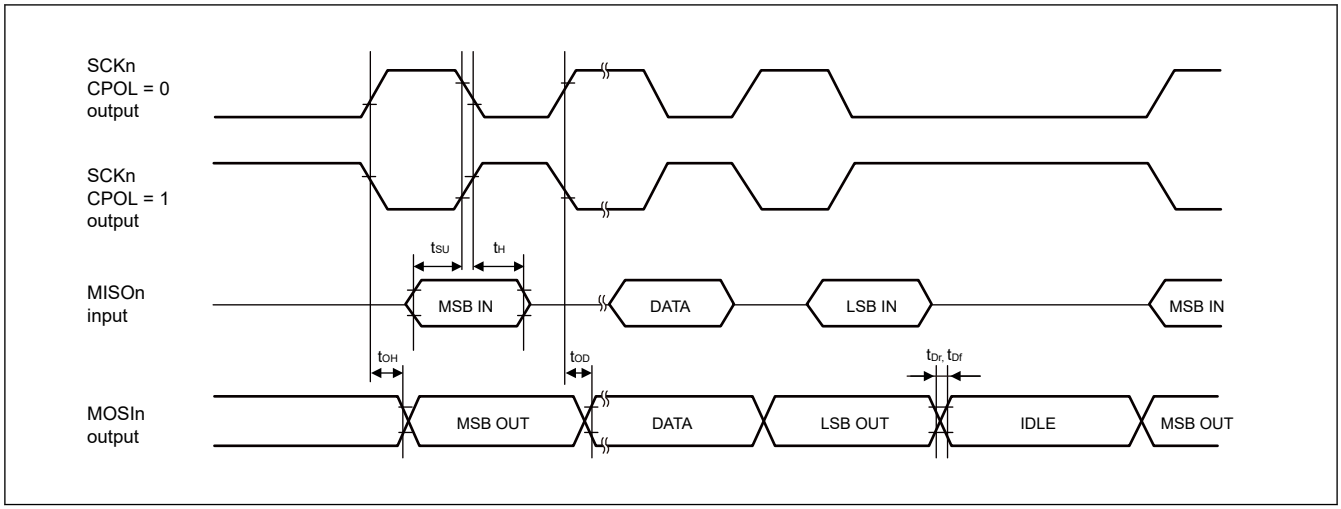


Figure 2.43 SCI simple SPI mode timing for master when CPHA = 1

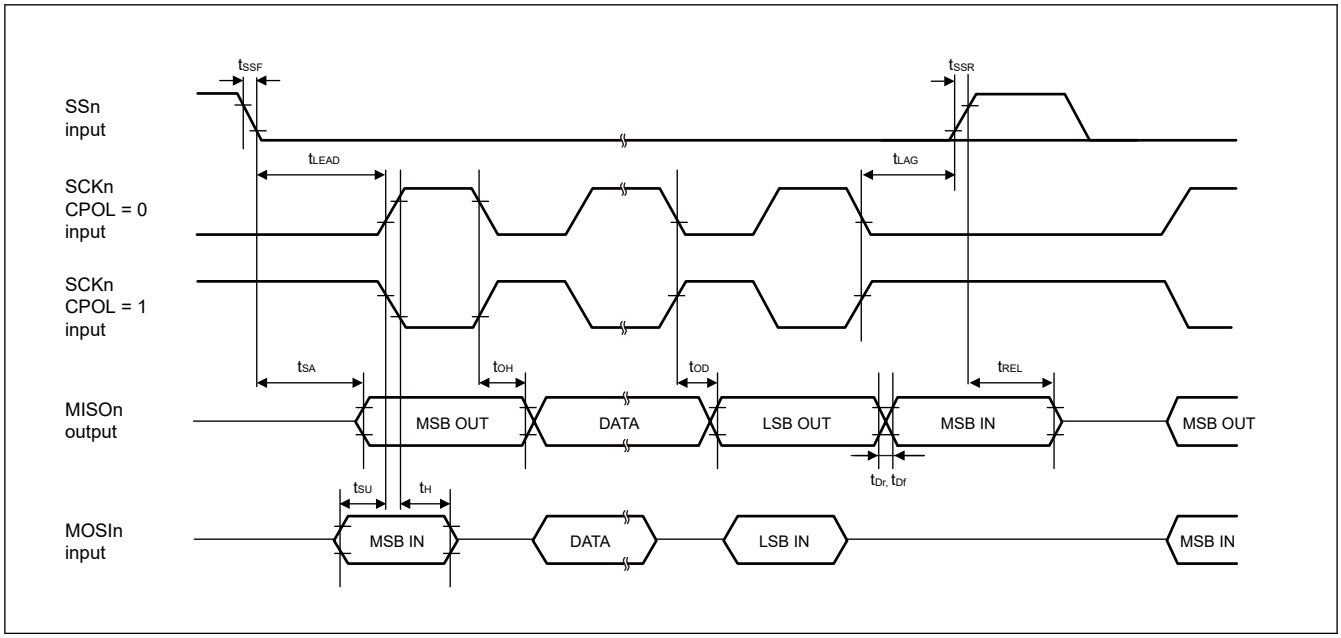


Figure 2.44 SCI simple SPI mode timing for slave when CPHA = 0

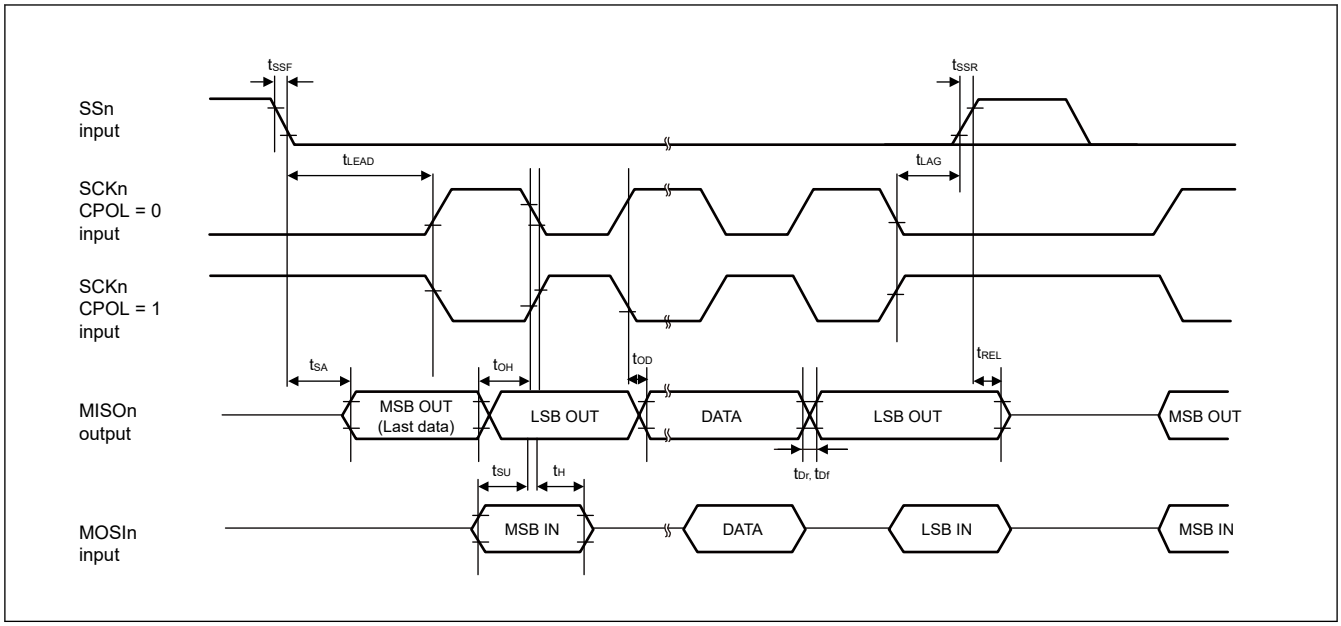


Figure 2.45 SCI simple SPI mode timing for slave when CPHA = 1

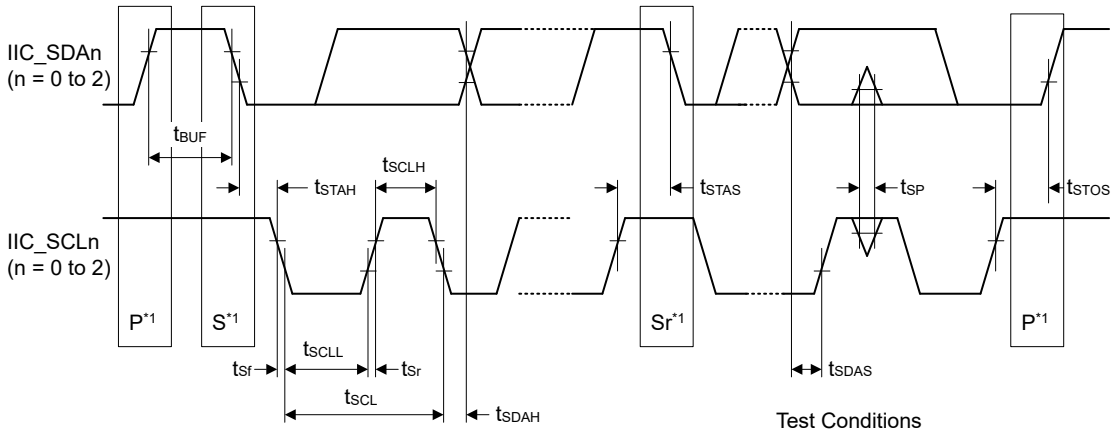
2.5.5.9 IIC Timing

Conditions: V_{OL} = 0.4 V, I_{OL} = 4 mA

Table 2.33 IIC timing

Parameter		Symbol	Min.*1 *2	Max.*1 *2	Unit	Reference figure
IIC (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.46
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—	1000	ns	
	SCL, SDA input falling time	t_{sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
IIC (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—*4	300	ns	
	SCL, SDA input falling time	t_{sf}	—*4	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load*3	C_b	—	400	pF	

Note 1. t_{IICcyc}: IIC internal reference clock (IICΦ) cycle
Note 2. The value out of parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 00b while the digital filter is enabled by setting ICFER.NFE = 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by setting ICFER.NFE = 1.
Note 3. Cb is the total capacitance of the bus lines.
Note 4. The minimum values are not specified for t_{sr} and t_{sf} in Fast-mode.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.46 IIC bus interface input/output timing

2.5.5.10 CANFD Timing

Table 2.34 CANFD timing

Parameter		Symbol	CAN		CANFD		Unit	Reference figure
			Min.	Max.	Min.	Max.		
CANFD	Internal delay time	t_{node}	—	100	—	50	ns	Figure 2.47
	Transmission rate	—	—	1	—	8	Mbps	

Note: Internal delay time (t_{node}) = Internal transmission delay time (t_{output}) + Internal reception delay time (t_{input})

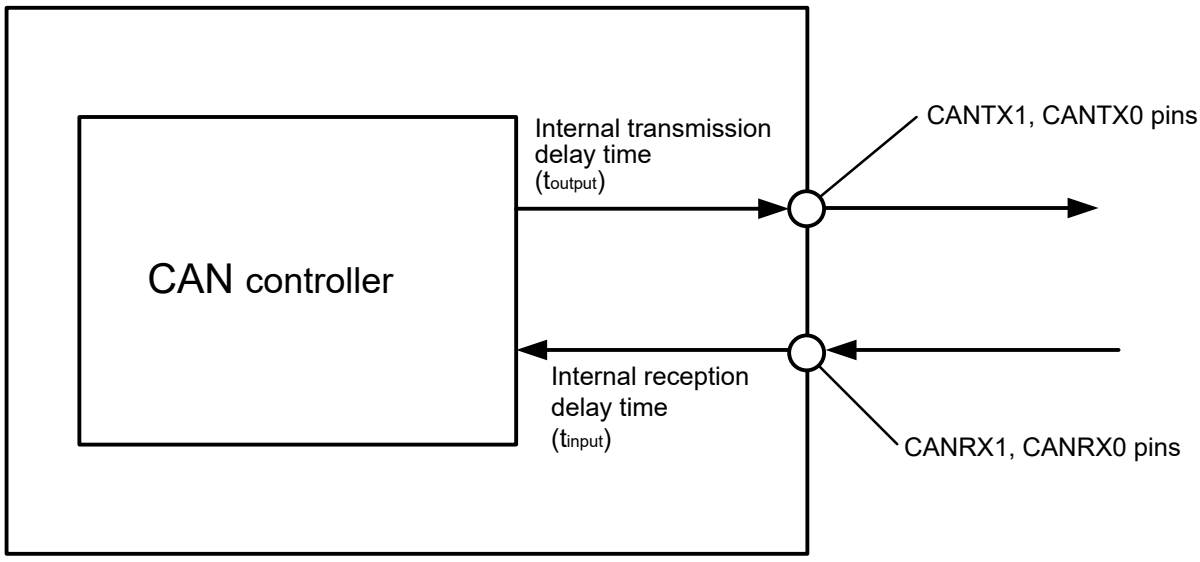


Figure 2.47 CAN interface condition

2.5.5.11 SPI Timing

Table 2.35 SPI timing (1 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF

Parameter		Symbol	Min.*1	Max.*1	Unit*1	Reference figure
RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{SPIcyc}	Figure 2.48
	Slave		2	4096		
RSPCK clock high level pulse width	Master	t_{SPCKWH}	(t_{SPcyc} − t_{SPCKr} − t_{SPCKf}) / 2 − 2.5	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPCK clock low level pulse width	Master	t_{SPCKWL}	(t_{SPcyc} − t_{SPCKr} − t_{SPCKf}) / 2 − 2.5	—	ns	
	Slave		1	—	t_{SPIcyc}	
RSPCK clock rising/falling time	Output	t_{SPCKr}, t_{SPCKf}	—	3	ns	
	Input		—	1	ns	
Data input setup time	Master	t_{SU}	5	—	ns	Figure 2.49 to Figure 2.55
	Slave		3	—		
Data input hold time	Master	t_H	3	—	ns	
	Slave		3	—		
SSL setup time	Master	t_{LEAD}	N × t_{SPcyc} − 3*2	N × t_{SPcyc} + 3*2	ns	Figure 2.49 to Figure 2.52
	Slave		4	—	t_{SPIcyc}	
SSL hold time	Master	t_{LAG}	N × t_{SPcyc} − 3*3	N × t_{SPcyc} + 3*3	ns	
	Slave		4	—	t_{SPIcyc}	
Continuous transmission delay	Master	t_{TD}	t_{SPcyc} + 2 × t_{SPIcyc}	8 × t_{SPcyc} + 2 × t_{SPIcyc}	ns	
	Slave		t_{SPcyc} + 5 × t_{SPIcyc}	—		
TI-SSP SS input setup time		t_{TISS}	3	—	ns	Figure 2.53 to Figure 2.55
TI-SSP SS input hold time		t_{TISH}	3	—	ns	
TI-SSP next access time		t_{TIND}	M*4	—	t_{SPIcyc}	
TI-SSP Master SS output delay		t_{TISSOD}	-3	3	ns	
TI-SSP Master OE delay 1		$t_{TIMOED1}$	—	2	ns	
TI-SSP Master OE delay 2		$t_{TIMOED2}$	—	2	ns	
TI-SSP Slave OE delay 1		$t_{TISOED1}$	—	14	ns	
TI-SSP Slave OE delay 2		$t_{TISOED2}$	—	11	ns	
Data output delay time	Master	t_{OD}	—	3	ns	Figure 2.49 to Figure 2.55
	Slave		—	12	ns	
Data output hold time	Master	t_{OH}	-3	—	ns	
	Slave		3	—		
MOSI, MISO rising/falling time	Output	t_{Dr}, t_{Df}	—	3	ns	
	Input		—	1	µs	
SSL rising/falling time	Output	t_{SSLr}, t_{SSLf}	—	3	ns	Figure 2.49, Figure 2.50
	Input		—	1	µs	

Table 2.35 SPI timing (2 of 2)

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF

Parameter	Symbol	Min.*1	Max.*1	Unit*1	Reference figure
Slave access time	t_{SA}	—	14	ns	Figure 2.51, Figure 2.52
Slave output release time	t_{REL}	—	12	ns	

Note 1. t_{SPIcyc}: PCLKSPIn cycle
Note 2. SPCKD set value + 1 (1 to 8)
Note 3. SSLND set value + 1 (1 to 8)
Note 4. SSLND set value + 2 (2 to 9)

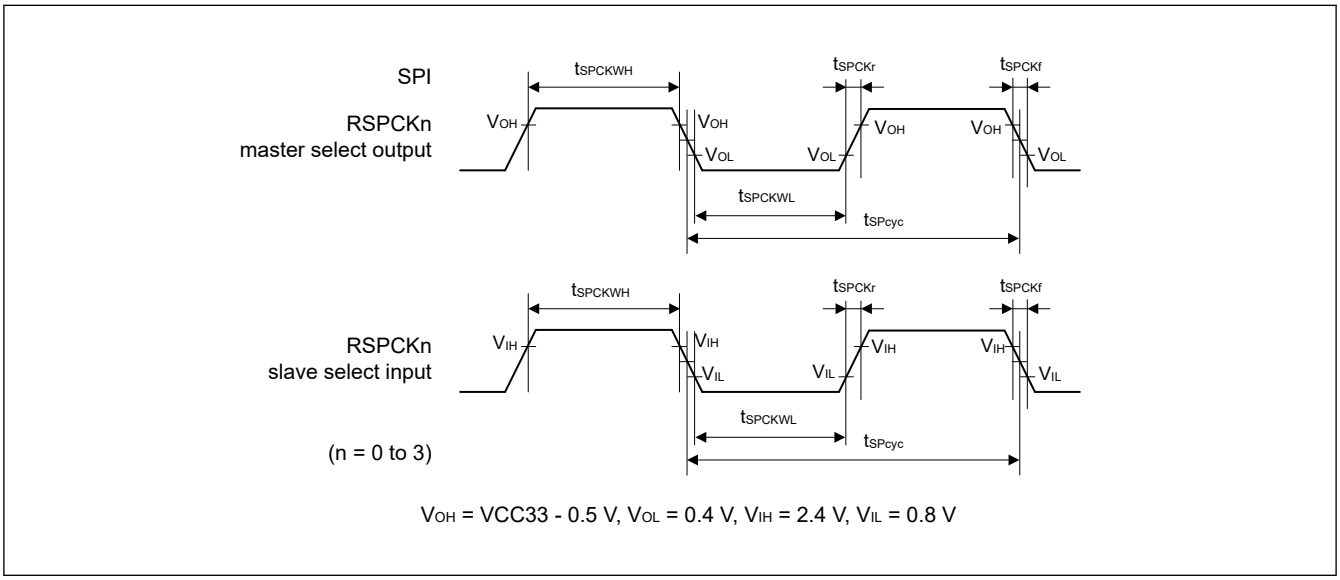


Figure 2.48 SPI clock timing

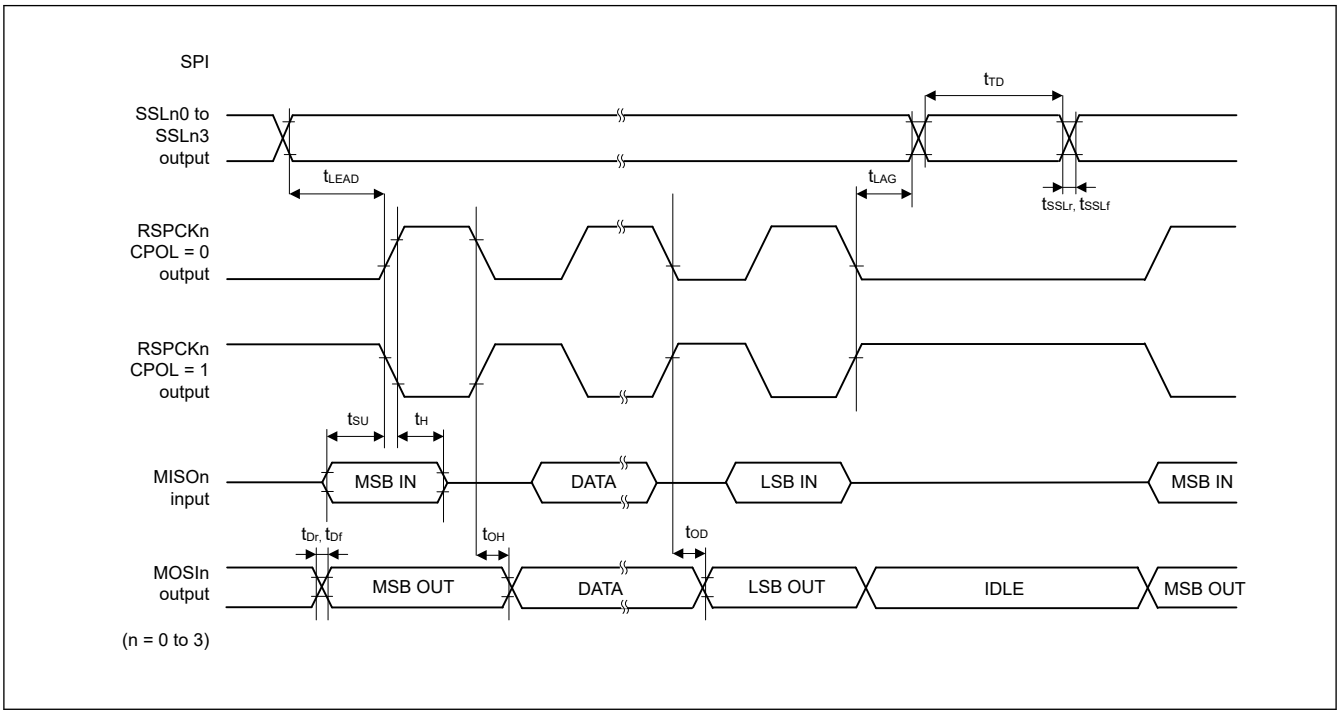


Figure 2.49 SPI timing (Master, Motorola SPI, CPHA = 0)

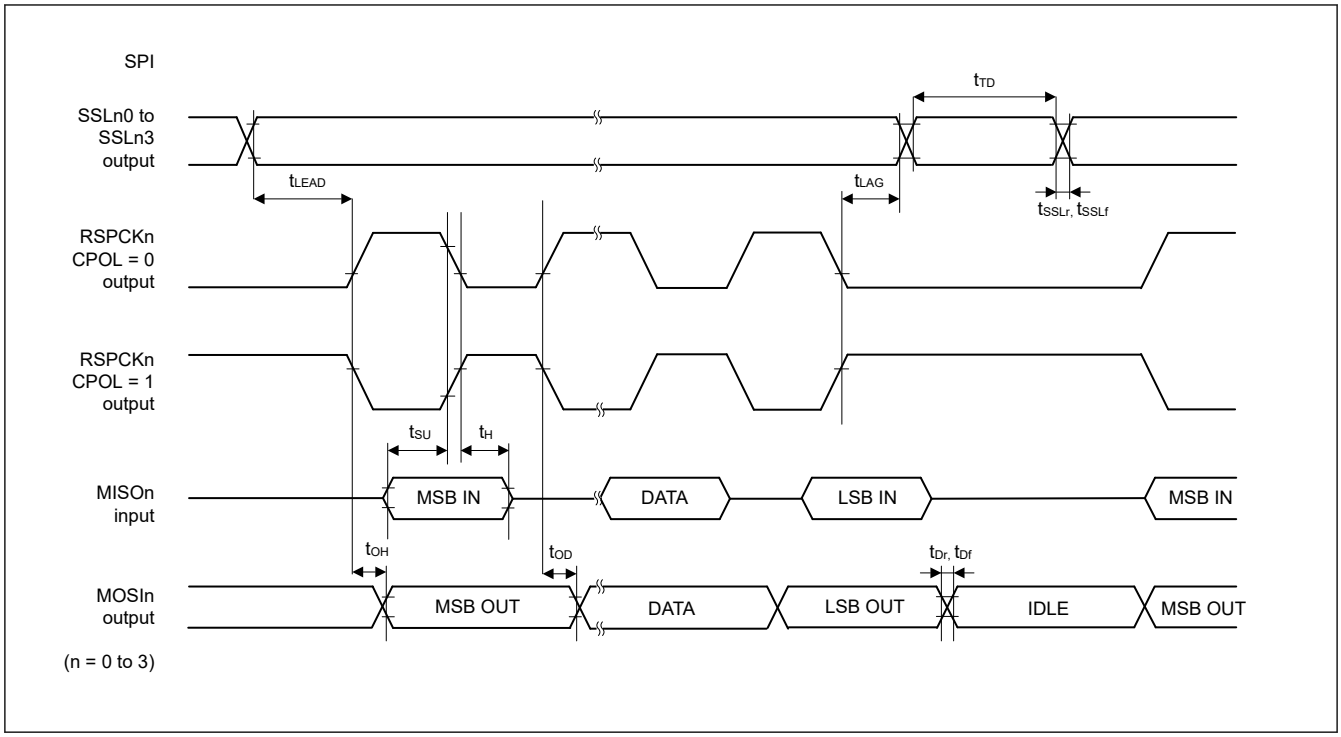


Figure 2.50 SPI timing (Master, Motorola SPI, CPHA = 1)

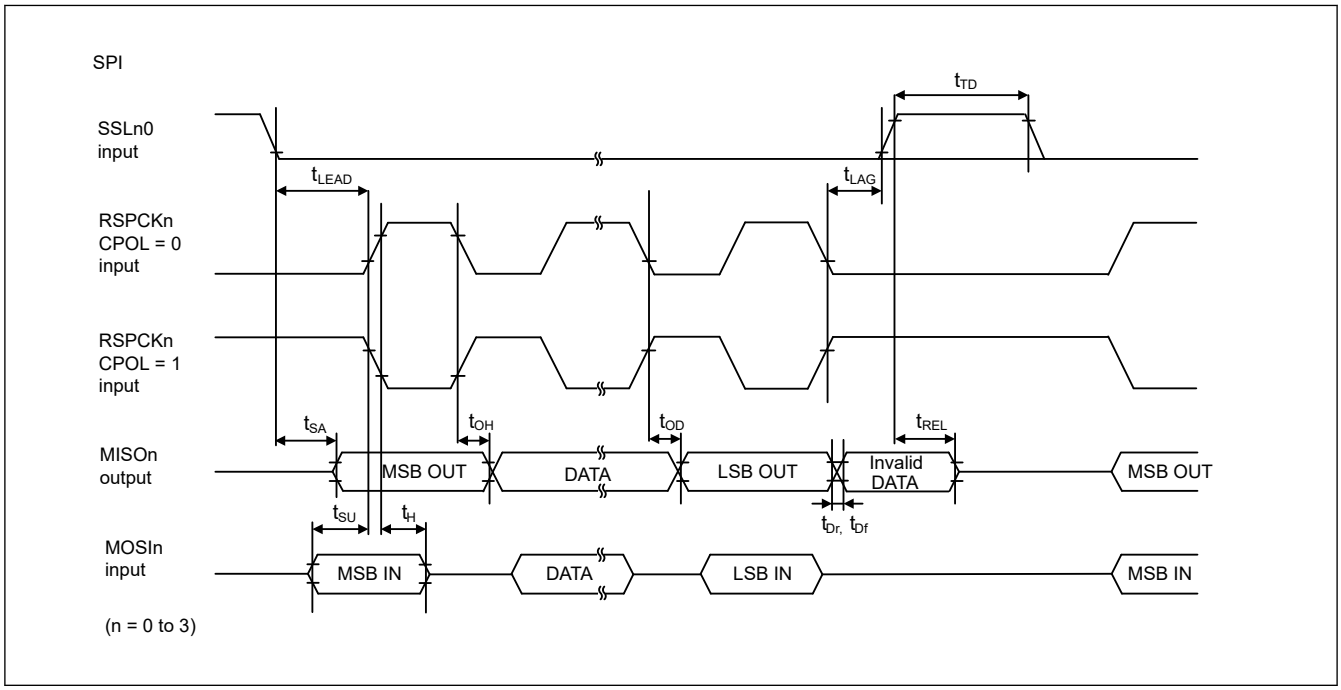


Figure 2.51 SPI timing (Slave, Motorola SPI, CPHA = 0)

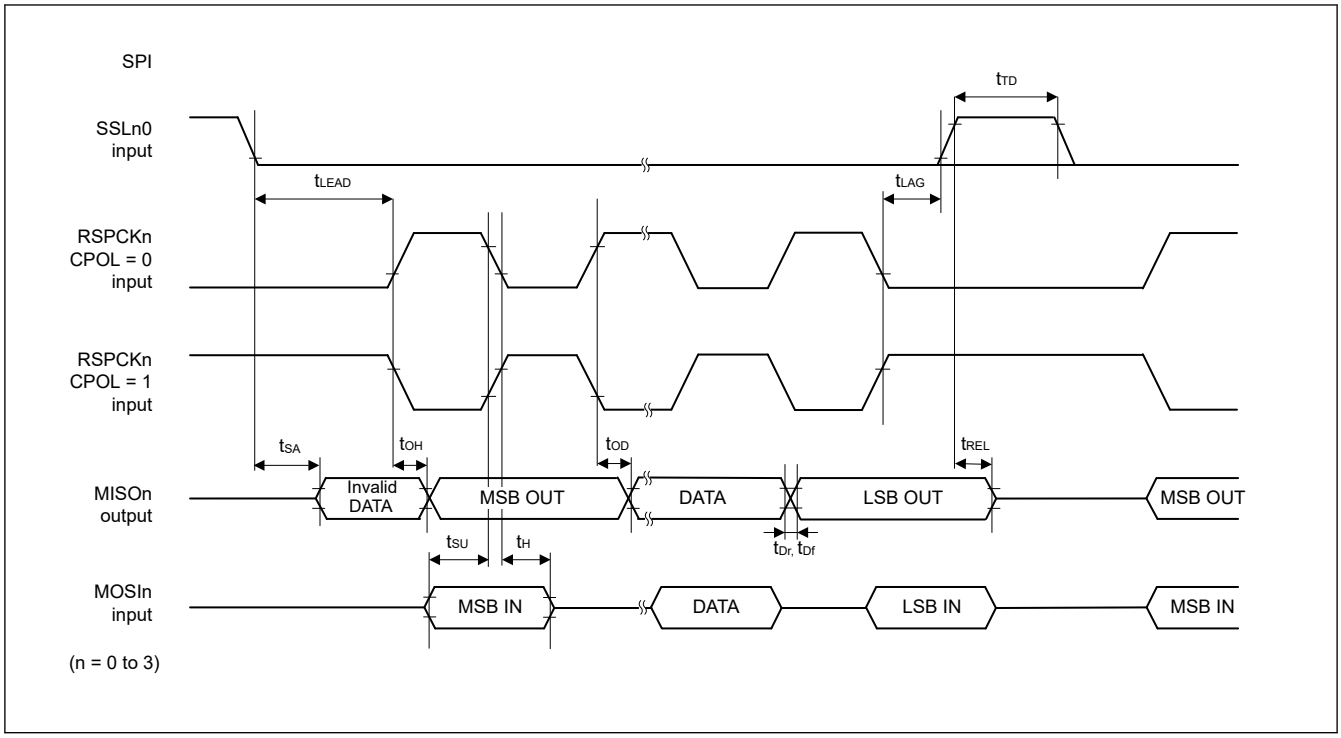


Figure 2.52 SPI timing (Slave, Motorola SPI, CPHA = 1)

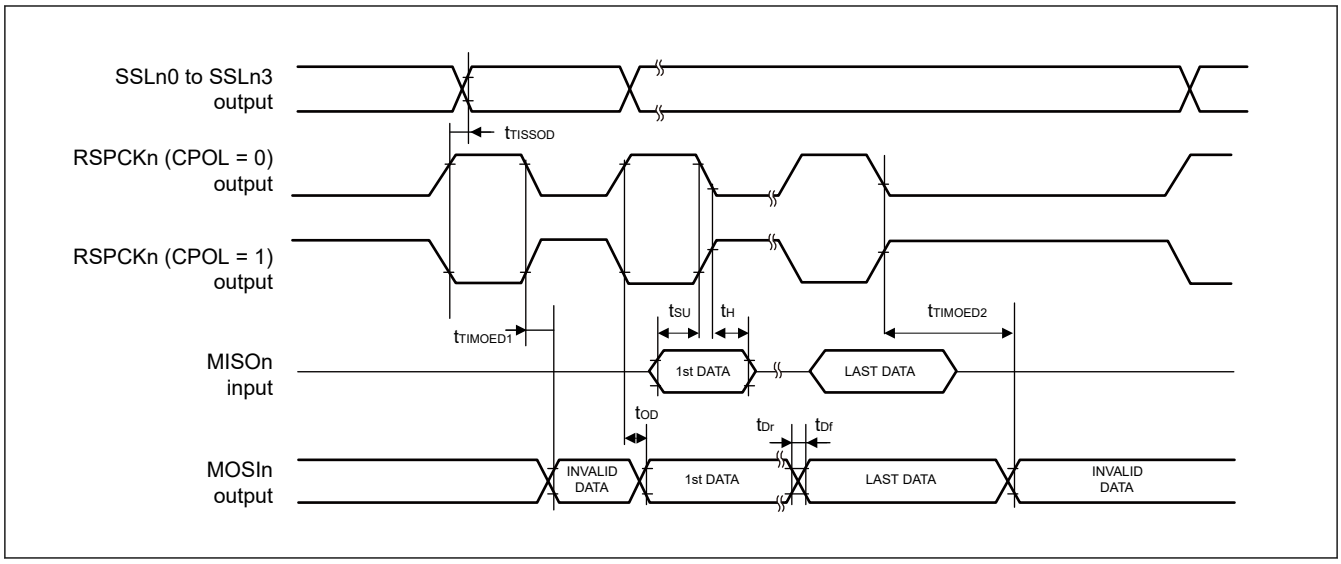


Figure 2.53 SPI timing (Master, TI SSP)

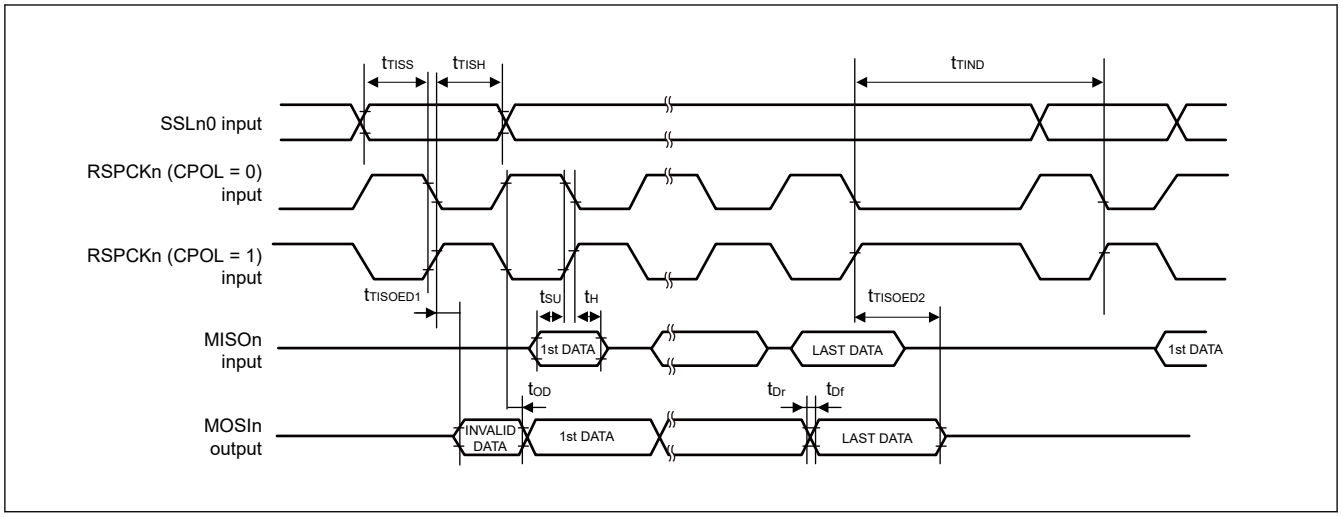


Figure 2.54 SPI timing (Slave, TI-SSP, with delay in burst transfer)

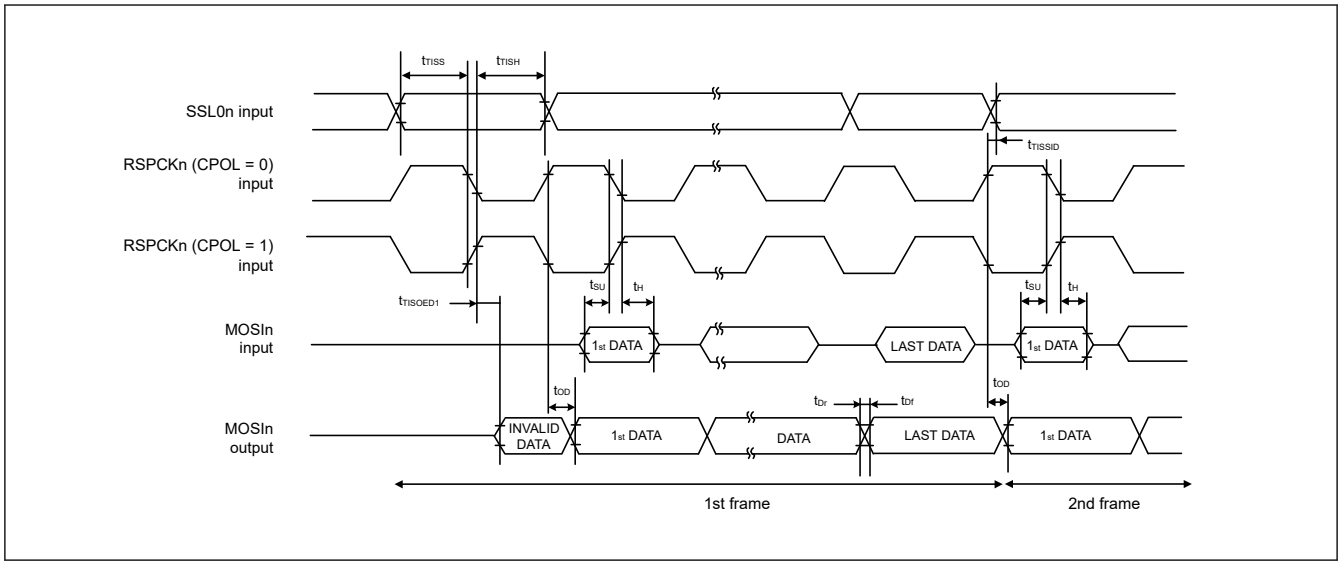


Figure 2.55 SPI timing (Slave, TI-SSP, without delay in burst transfer)

2.5.5.12 xSPI Timing

Conditions:

Single end Clock

V_{OH} = VCC18 × 0.5, V_{OL} = VCC18 × 0.5, C = 15 pF (1.8 V)

V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (3.3 V)

Data

V_{OH} = VCC18 × 0.5, V_{OL} = VCC18 × 0.5, C = 15 pF (1.8 V)

V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 15 pF (3.3 V)

Table 2.36 xSPI timing

Parameter		Symbol	1.8 V		3.3 V		Unit	Reference figure
			Min.	Max.	Min.	Max.		
Cycle time	SDR	t_{PERIOD}	7.5	—	13.3	—	ns	Figure 2.56
	DDR		10.0	—	13.3	—	ns	
Clock output slew rate		t_{SRck}	0.75/0.56*2	—	0.56	—	V/ns	
Clock Duty cycle distortion		t_{CKDCD}	0.0	t_{PERIOD} × 0.05	0.0	t_{PERIOD} × 0.05	ns	
Clock Minimum Pulse width		t_{CKMPW}	t_{PERIOD} × 0.45	—	t_{PERIOD} × 0.45	—	ns	
Differential clock crossing voltage		$V_{OX(AC)}$	0.4 × VCC18	0.6 × VCC18	—	—	V	
DS Duty cycle distortion		t_{DSDCD}	0.0	t_{PERIOD} × 0.04	0.0	t_{PERIOD} × 0.04	ns	
DS Minimum Pulse width		t_{DSMPW}	t_{PERIOD} × 0.41	—	t_{PERIOD} × 0.41	—	ns	
Data input/output slew rate		t_{SR}	0.75/0.56*2	—	0.56	—	V/ns	
Data input setup time (to CK)	SDR	t_{SU}	2.0	—	2.3	—	ns	Figure 2.57
Data input hold time (to CK)		t_{H}	1.0	—	1.0	—	ns	
Data output delay time		t_{OD}	—	1.0*3	—	1.4*3	ns	
Data output hold time		t_{OH}	-1.0	—	-2.3	—	ns	
Data output buffer off time		t_{BOFF}	-1.0	—	-2.3	—	ns	
Data input setup time (to DS)	DDR*1 *3	t_{SU}	-0.6	—	-0.8	—	ns	Figure 2.58, Figure 2.59
Data input hold time (to DS)		t_{H}	t_{PERIOD} × 0.41 - 0.6	—	t_{PERIOD} × 0.41 - 0.8	—	ns	
Data input setup time (to CK)		t_{SU}	2.0	—	2.3	—	ns	
Data input hold time (to CK)		t_{H}	1.0	—	1.0	—	ns	
Data output setup time (to CK)		t_{SUO}	1.0/1.5/2.5*5	—	1.5/2.5*6	—	ns	
Data output hold time (to CK)		t_{HO}	1.0/1.5/2.5*5	—	1.5/2.5*6	—	ns	
CS Low to Clock High		t_{CSLCKH}	6.0/8.0*2 *4	—	8.0*4	—	ns	Figure 2.57 to Figure 2.59
Clock Low to CS High		t_{CKLCSH}	6.0/8.0*2	—	8.0	—	ns	
CS High time		t_{CSTD}	1	16	1	16	t_{PERIOD}	
DS Low to CS High		t_{DSLCSH}	6.0/8.0*2 *7	—	10.6*7	—	ns	Figure 2.60
CS High to DS Tri-State		t_{CSHDST}	0.0	t_{PERIOD}	0.0	t_{PERIOD}	ns	
CS Low to DS Low*10		t_{CSLDSL}	0.0	16.0*11	0.0	20.0*11	ns	
DS Tri-State to CS Low		t_{DSTCSL}	0.0	—	0.0	—	ns	
CK low to DS low*8		t_{CKLDSL}	—	(0.45 + e) × t_{PERIOD} - 2*9	—	(0.45 + e) × t_{PERIOD} - 2*9	ns	

Note 1. The DS shift setting (WRAPCFG.DSSFTCSx[4:0]) is 01000b for xSPI200.
Note 2. Specification at 133 MHz / Specification at 100 MHz
Note 3. These are values when the OEN assertion is extended in the Output Enable Asserting extension bit (COMCFG.OEASTEX = 1).
Note 4. These are the values when the CS assertion is extended in the CS asserting extension bit (LIOCFGCSn.CSASTEX = 1).
Note 5. Specification at 100 MHz / Specification at 75 MHz / Specification at 50 MHz
Note 6. Specification at 75 MHz / Specification at 50 MHz
Note 7. These are the values when the t_{CKLDSL} constraint is satisfied.
Note 8. This constraint is necessary only to satisfy the t_{DSLCSH} requirement in JESD251, which specifies that t_{DSLCSH} must be at least 80% of t_{PERIOD}. Set LIOCFGCSn.CSNEGEX to the appropriate value to ensure the memory specification complies with this constraint.

Note 9. e = LIOCFGCSn.CSNEGEX
Note 10. If the DS is high during the command & modifier phase when using JESD251 Profile 2.0 memory, the time from CS low to DS high must also meet this specification.
Note 11. When using JESD251 Profile 1.0 memory or JESD251 Profile 2.0 memory with LIOCFGCSn.LATEMD set to 0, this constraint does not apply if the internal pull-down resistor of the DS pin is enabled.

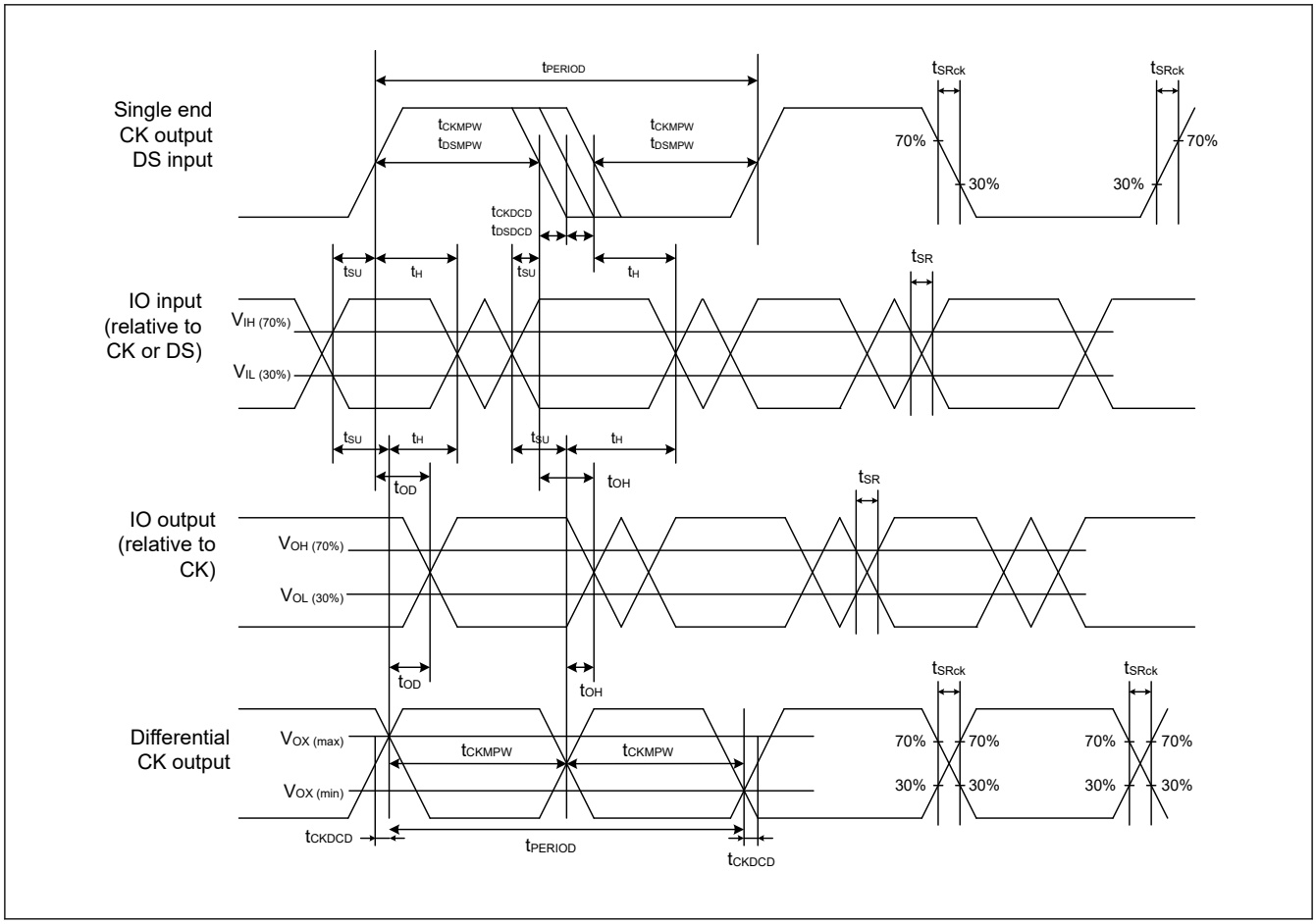


Figure 2.56 xSPI clock / DS timing

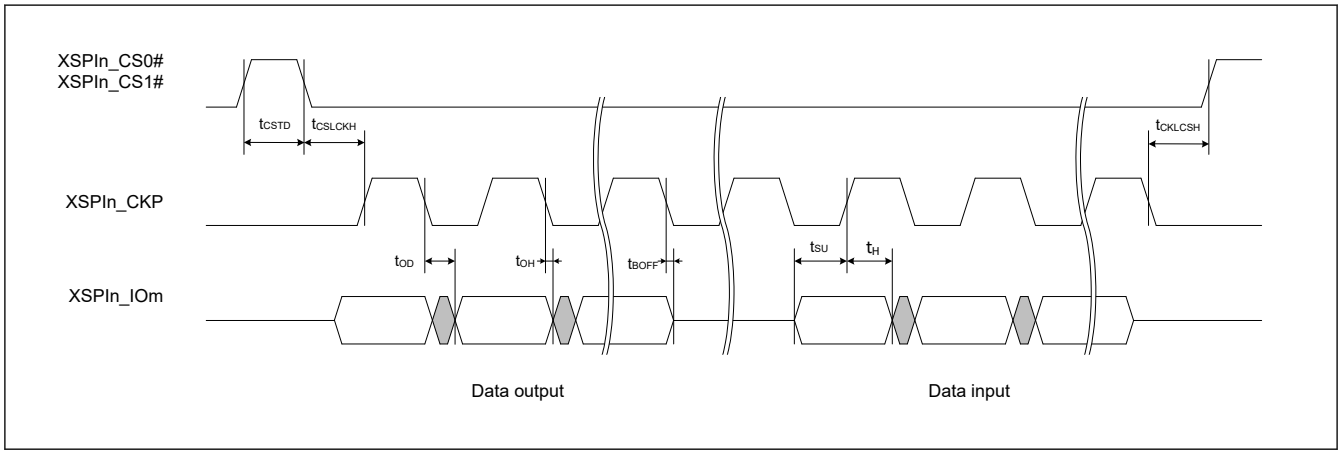


Figure 2.57 SDR transmit/receive timing (1S-1S-1S, 1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S)

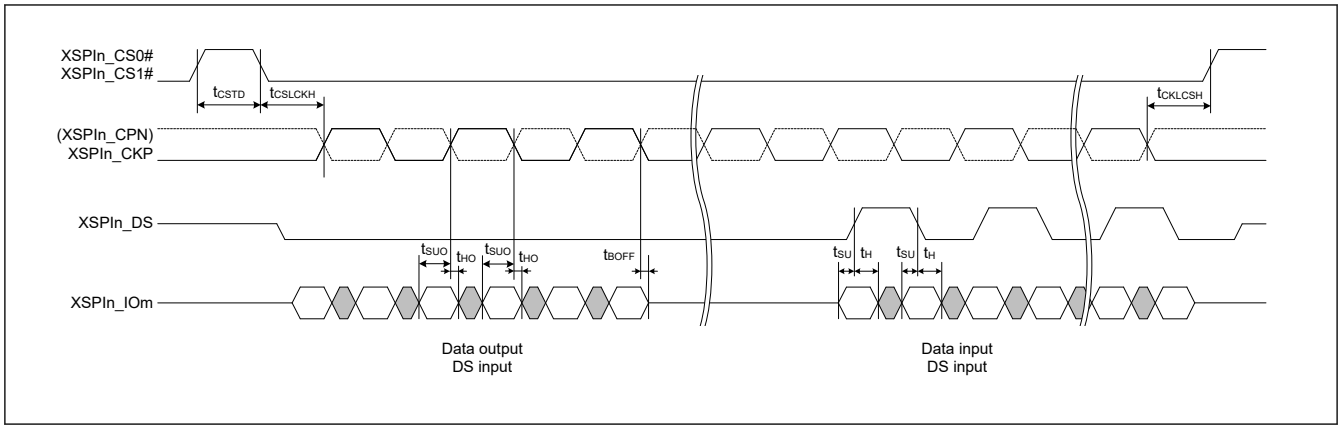


Figure 2.58 DDR transmit/receive timing (4S-4D-4D, 8D-8D-8D)

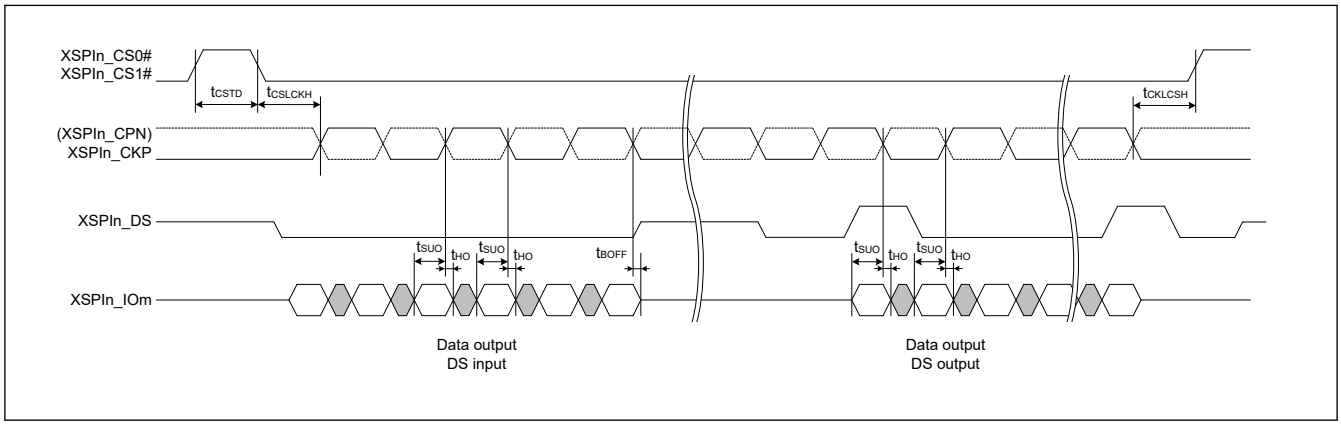


Figure 2.59 DDR transmit/receive timing (HyperRAM write)

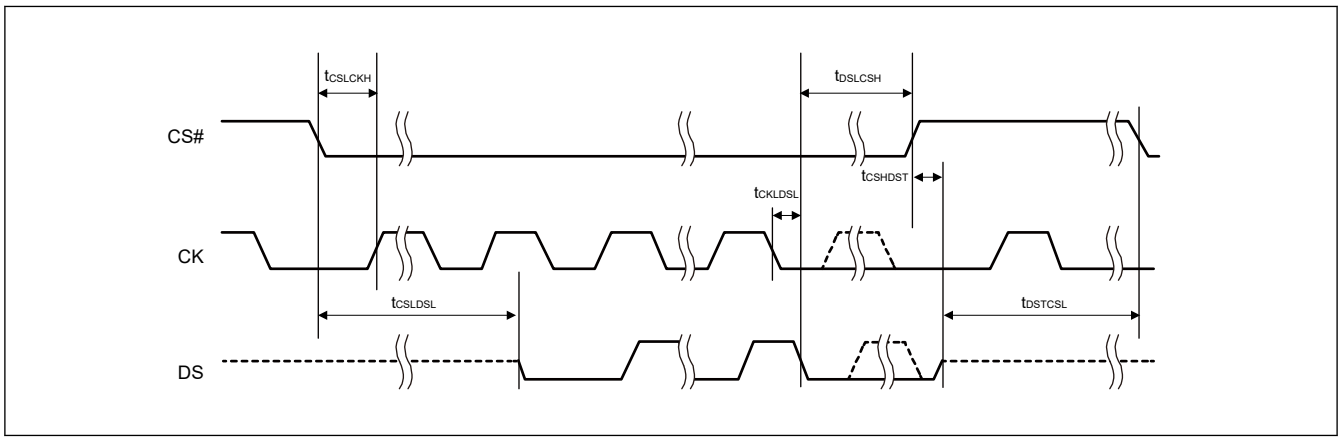


Figure 2.60 DS to CS signal timing

2.5.5.13 Delta-Sigma Interface Timing

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF

Table 2.37 ΔΣ interface timing

Parameter			Symbol	Min.	Max.	Unit	Reference figure
DSMIF	Clock cycle	Master	t_{DScyc}	40	200	ns	Figure 2.61
		Slave		40	200		
	Clock high level	Master	t_{DSCKWH}	16	—	ns	
		Slave		16	—		
	Clock low level	Master	t_{DSCKWL}	16	—	ns	
		Slave		16	—		
	Setup time	Master	t_{SU}	15	—	ns	Figure 2.62, Figure 2.63
		Slave		5	—		
	Hold time	Master	t_H	0	—	ns	
		Slave		5	—		

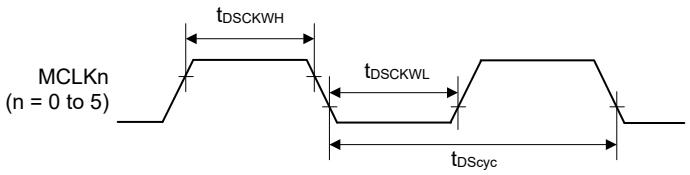


Figure 2.61 Clock input/output timing

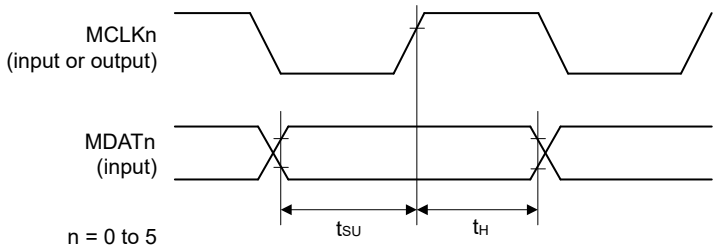


Figure 2.62 Reception timing (MCLKn rising synchronous)

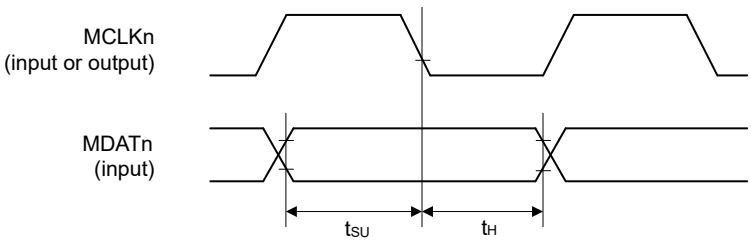


Figure 2.63 Reception timing (MCLKn falling synchronous)

2.5.5.14 Ethernet Interface Timing

Conditions:

V_{OH} = VCC18 × 0.5, V_{OL} = VCC18 × 0.5, C = 15 pF (RGMII)*1

V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 25 pF (RMII)

V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF (MII)

Table 2.38 Ethernet interface timing (1 of 2)

Parameter			Symbol	Min.	Max.	Unit	Reference figure
Ethernet (RGMII)	ETHn_TXCLK, ETHn_RXCLK cycle time duration	1 Gbps	$t_{RGMIIck}$	7.2	8.8	ns	Figure 2.64
		100 Mbps		36	44		
		10 Mbps		360	440		
	ETHn_TXCLK, ETHn_RXCLK frequency	1 Gbps	—	125 − 50 ppm	125 + 50 ppm	MHz	
		100 Mbps		25 − 50 ppm	25 + 50 ppm		
		10 Mbps		2.5 − 50 ppm	2.5 + 50 ppm		
	ETHn_TXCLK, ETHn_RXCLK duty cycle	1 Gbps	—	45	55	%	
		100 Mbps 10 Mbps		40	60		
	ETHn_TXCLK, ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL), ETHn_RXCLK, ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) rise/fall time		t_{RGMIIr}, t_{RGMIIf} *1	—	0.75	ns	
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN (TX_CTL) to ETHn_TXCLK output skew		$t_{RGMIIos}$	−0.5	0.5	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) setup time		t_{RGMIIs}	1	—	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV (RX_CTL) hold time		t_{RGMIIh}	1	—	ns	
Ethernet (RMII)	ETHn_RXCLK cycle time		t_{RMIIck}	20	—	ns	Figure 2.65 Figure 2.66
	ETHn_RXCLK frequency Typ. 50 MHz		—	50 − 50 ppm	50 + 50 ppm	MHz	
	ETHn_RXCLK duty		—	35	65	%	
	ETHn_RXCLK rise/fall time		$t_{RMIIckr}$, $t_{RMIIckf}$	0.5	3.0	ns	
	ETHn_TXD0, ETHn_TXD1, ETHn_TXEN output delay time		t_{RMIId}	2.5	12	ns	
	ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) setup time	Case A*2	t_{RMIIs}	4.0	—	ns	
		Case B*2		4.0	—		
		Case C*2		4.8	—		
	ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) hold time		t_{RMIIh}	2	—	ns	
	ETHn_TXD0, ETHn_TXD1, ETHn_TXEN, ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) rise/fall time		t_{RMIIr}, t_{RMIIf}	0.5	4	ns	

Table 2.38 Ethernet interface timing (2 of 2)

Parameter			Symbol	Min.	Max.	Unit	Reference figure
Ethernet (MII)	ETHn_TXCLK, ETHn_RXCLK cycle time	100 Mbps	t_{MIIck}	40	—	ns	Figure 2.67 Figure 2.68
		10 Mbps		400	—		
	ETHn_TXCLK, ETHn_RXCLK frequency	100 Mbps	—	25 − 50 ppm	25 + 50 ppm	MHz	
		10 Mbps		2.5 − 50 ppm	2.5 + 50 ppm		
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN, ETHn_TXER output delay time		t_{MIId}	1	20	ns	
	ETHn_TXD0 to ETHn_TXD3, ETHn_TXEN output delay time (ESC, Automatic TX shift disabled (ETHn_TXCLK is clamped))	TXSFTn = 00b	$t_{MIIdESC}$	19.5	23.5	ns	
		TXSFTn = 01b		29.5	33.5		
		TXSFTn = 10b		-0.5	3.5		
		TXSFTn = 11b		9.5	13.5		
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV, ETHn_RXER setup time		t_{MIIs}	10	—	ns	
	ETHn_RXD0 to ETHn_RXD3, ETHn_RXDV, ETHn_RXER hold time		t_{MIIh}	10	—	ns	

Note 1. Measurement condition of tRGMIIr and tRGMIIf is FIGURE 3 in Reduced Gigabit Media Independent Interface (RGMII) 12/10/2000 Version 1.3.

Note 2. Details for each case are as follows:

Case A: ETHn_RXD0, ETHn_RXD1, ETHn_RXER, ETHn_RXDV (CRS_DV) setup time when using ETHn_RXCLK (Reference clock input)

Case B: ETHn_RXD0, ETHn_RXD1, ETHn_RXDV (CRS_DV) setup time when using RMIIn_REFCLK (Reference clock output)

Case C: ETHn_RXER setup time when using RMIIn_REFCLK (Reference clock output)

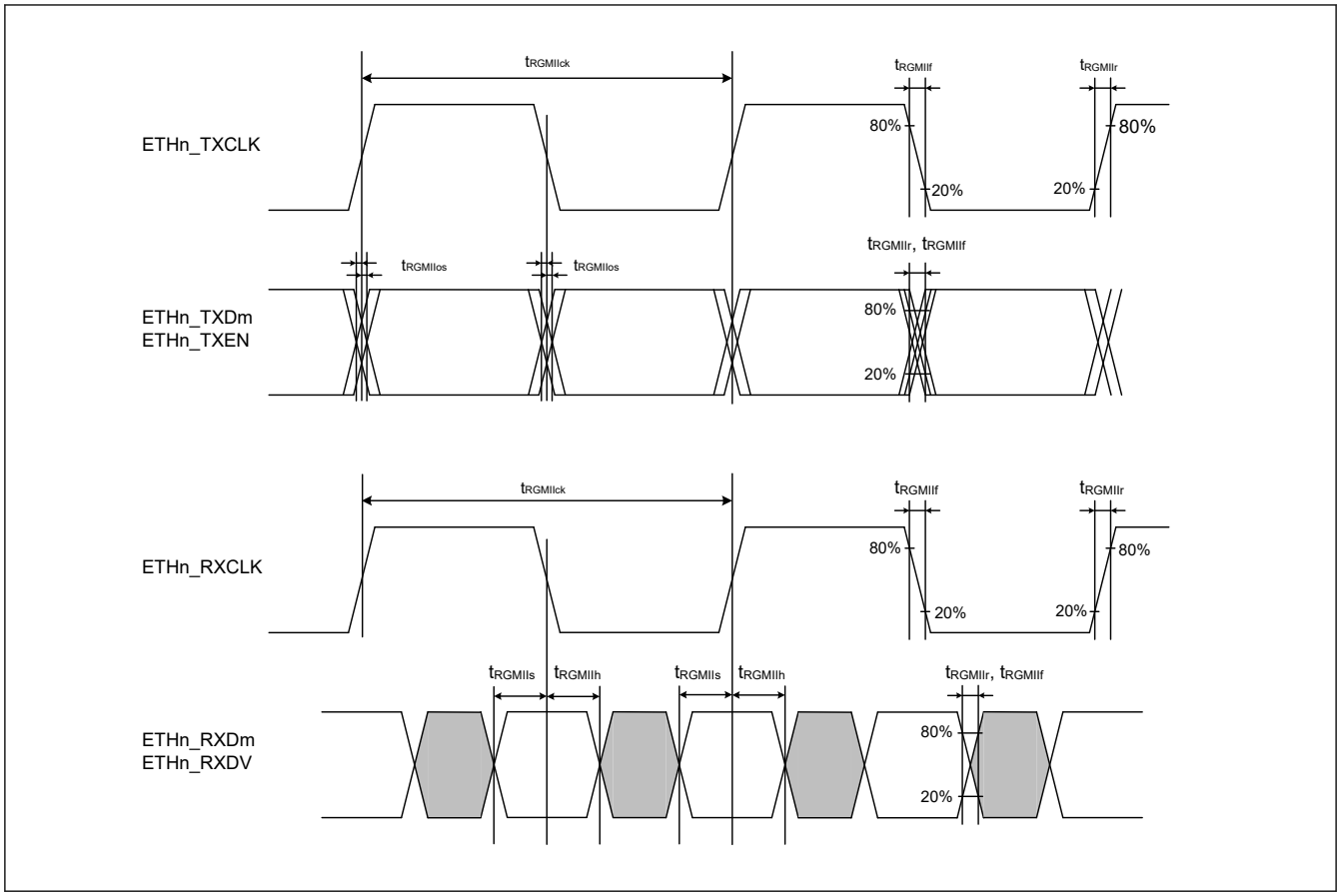


Figure 2.64 RGMII transmission and reception timing (n = 0 to 4, m = 0 to 3)

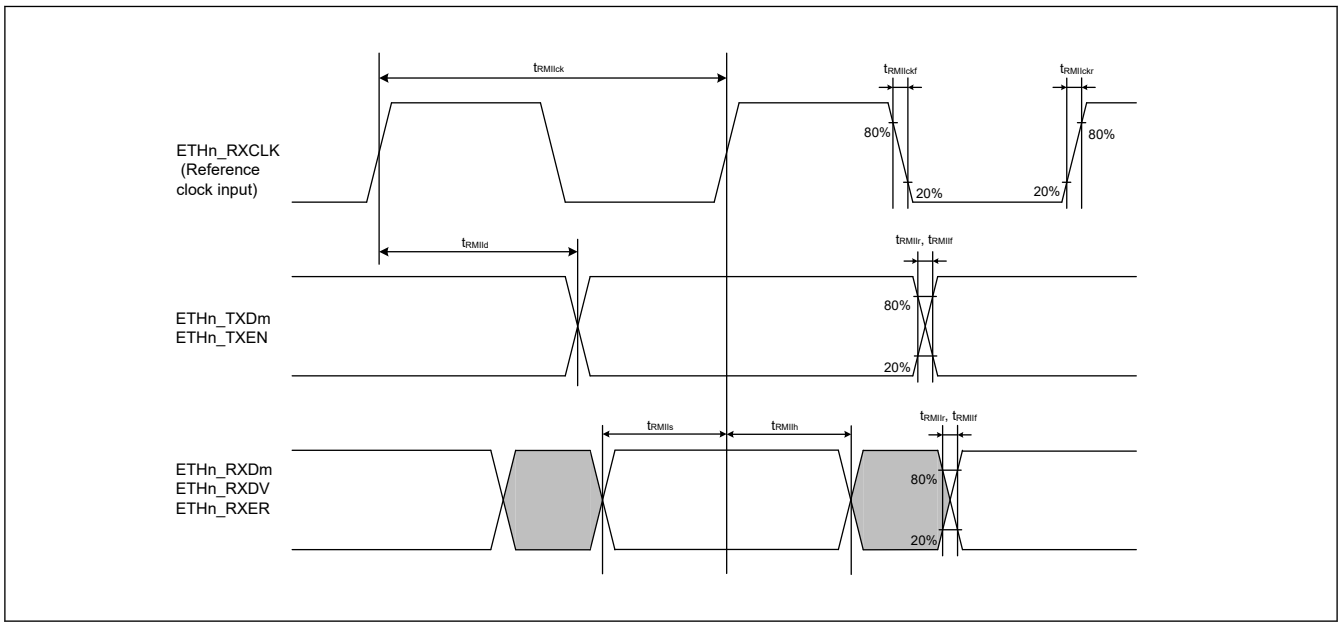


Figure 2.65 RMII transmission and reception timing (Reference clock input) (n = 0 to 4, m = 0 to 1)

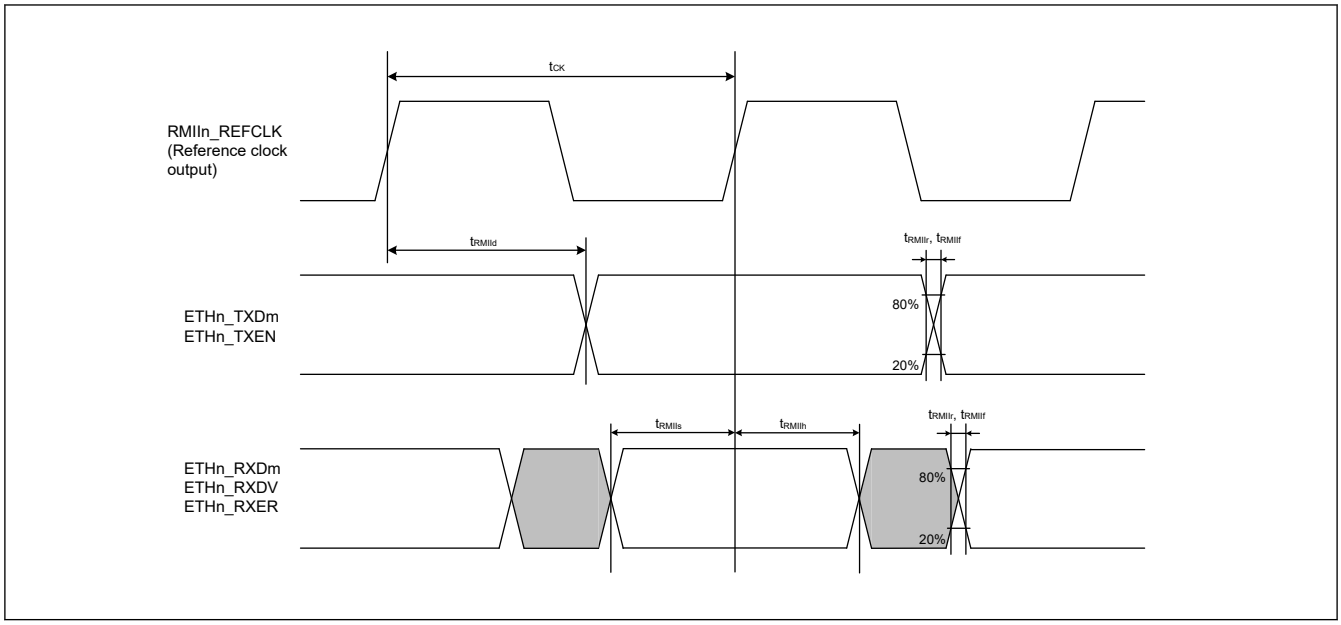


Figure 2.66 RMII transmission and reception timing (Reference clock output) (n = 0 to 4, m = 0 to 1)

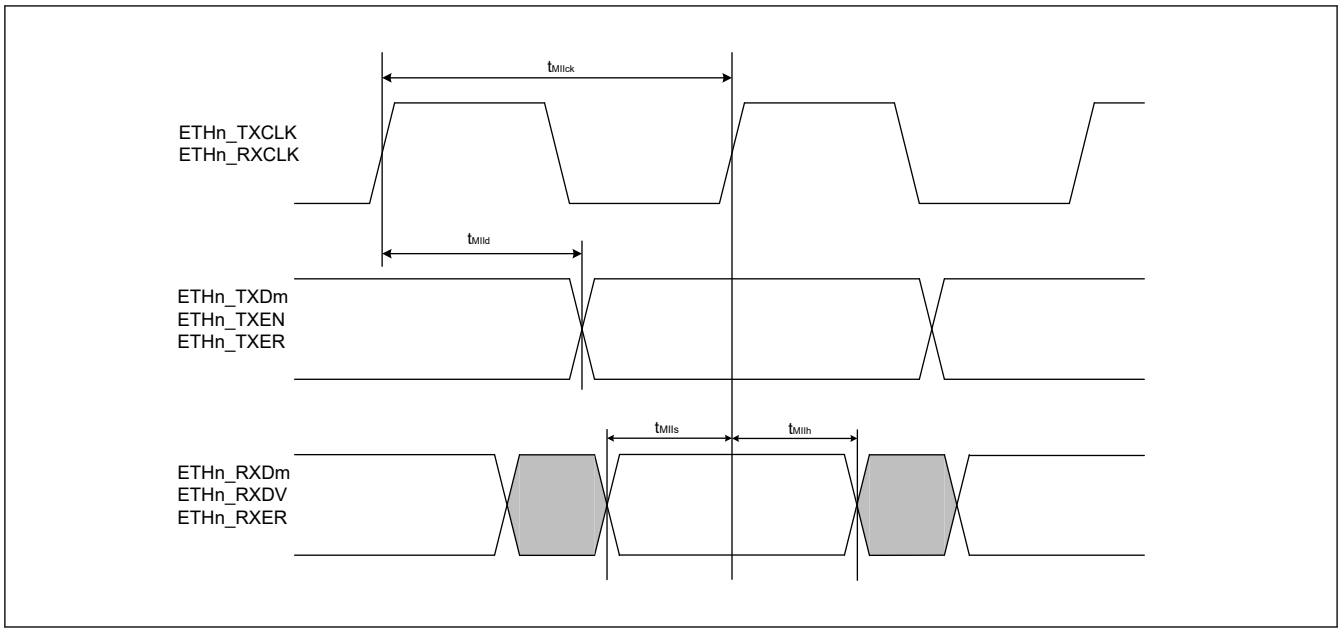


Figure 2.67 MII transmission and reception timing (n = 0 to 4, m = 0 to 3)

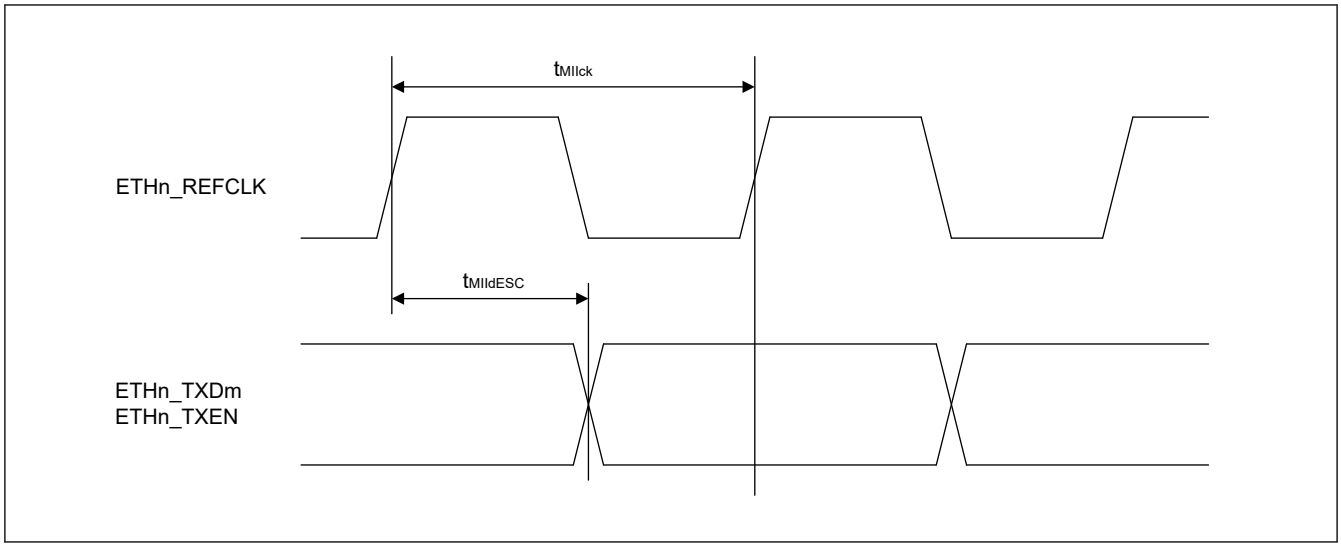


Figure 2.68 ESC MII transmission timing (Automatic TX shift disabled) (n = 0 to 2, m = 0 to 3)

2.5.5.15 Serial Management Interface Timing

Conditions:

V_{OH} = VCC18 × 0.5, V_{OL} = VCC18 × 0.5, C = 30 pF (1.8 V)

V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF (3.3 V)

Table 2.39 Serial management interface timing

Parameter			Symbol	Min.	Max.	Unit	Reference figure
MDIO	MDC output cycle time	GMAC_MDC, ETHSW_MDC	T_{MDCck}	80	—	ns	Figure 2.69
		ESC_MDC		400	—	ns	
	MDIO output delay time (for MDC fall)*1		T_{MDIOd}	—	20	ns	
	MDIO input setup time (for MDC rise)	GMAC_MDC, ETHSW_MDC	T_{MDIOs}	18	—	ns	
		ESC_MDC		70	—	ns	
	MDIO input hold time (for MDC rise)		T_{MDIOh}	0	—	ns	

Note 1. The output timing from ETHSW is based on the rising edge of MDC, and the output delay can be set in the register.

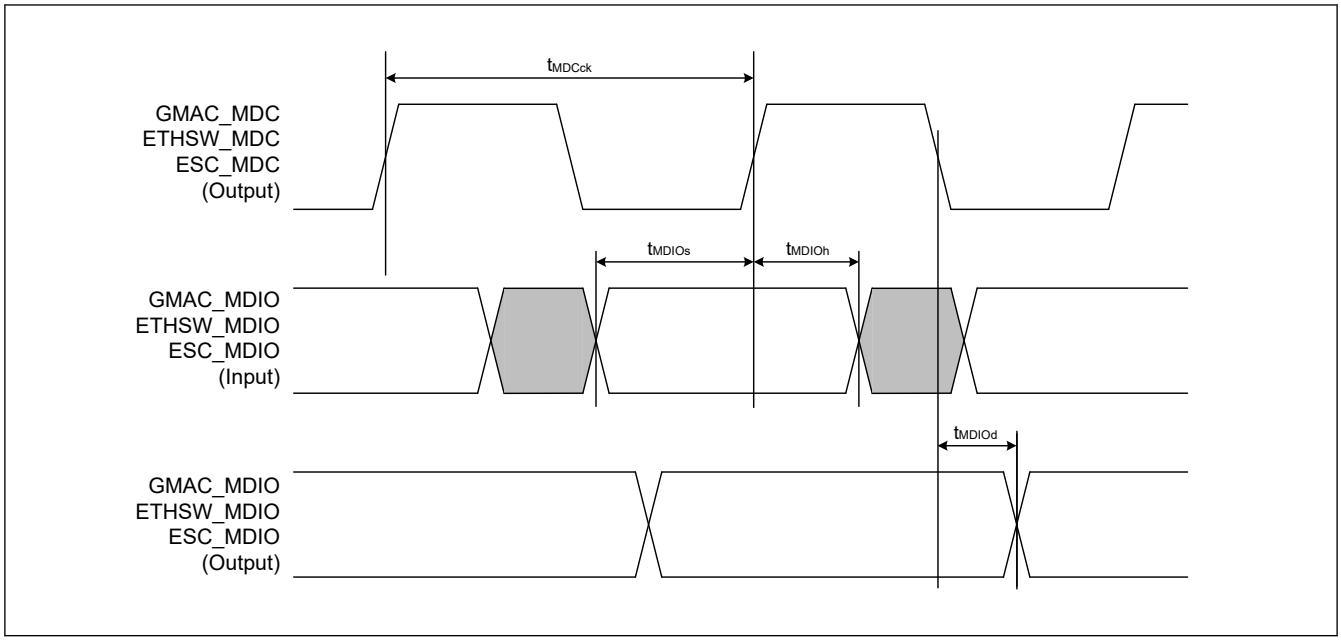


Figure 2.69 Serial management interface timing

2.5.5.16 SHOSTIF Timing

Conditions:

V_{OH} = VCC18 × 0.5, V_{OL} = VCC18 × 0.5, C = 30 pF (1.8 V)

V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF (3.3 V)

Table 2.40 SHOSTIF timing

Parameter		Symbol	Min.	Max.	Unit	Reference figure
SHOSTIF	Clock cycle time	t_{SHck}	25	—	ns	Figure 2.70
	Clock high time	t_{CH}	0.45	0.55	t_{SHck}	
	Clock low time	t_{CL}	0.45	0.55	t_{SHck}	
	Clock rise slew rate	t_{CRT}	0.1	—	V/ns	
	Clock fall slew rate	t_{CFT}	0.1	—	V/ns	
	CS# high time	t_{CS}	2	—	t_{SHck}	Figure 2.71, Figure 2.72
	CS# active setup time	t_{CSS}	15	—	ns	
	CS# active hold time	t_{CSH}	15	—	ns	
	Data input setup time	t_{SU}	3	—	ns	
	Data input hold time	t_{HD}	10.5	—	ns	
	Clock low to output valid	t_V	—	15.5	ns	
	Data output hold time	t_{HO}	6		ns	
	Data output disable time	t_{DIS}	—	18	ns	

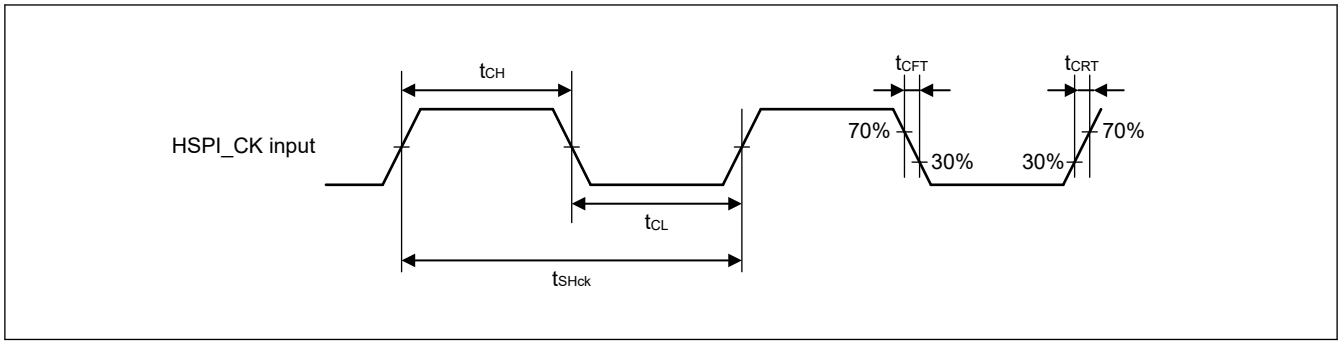


Figure 2.70 SHOSTIF clock timing

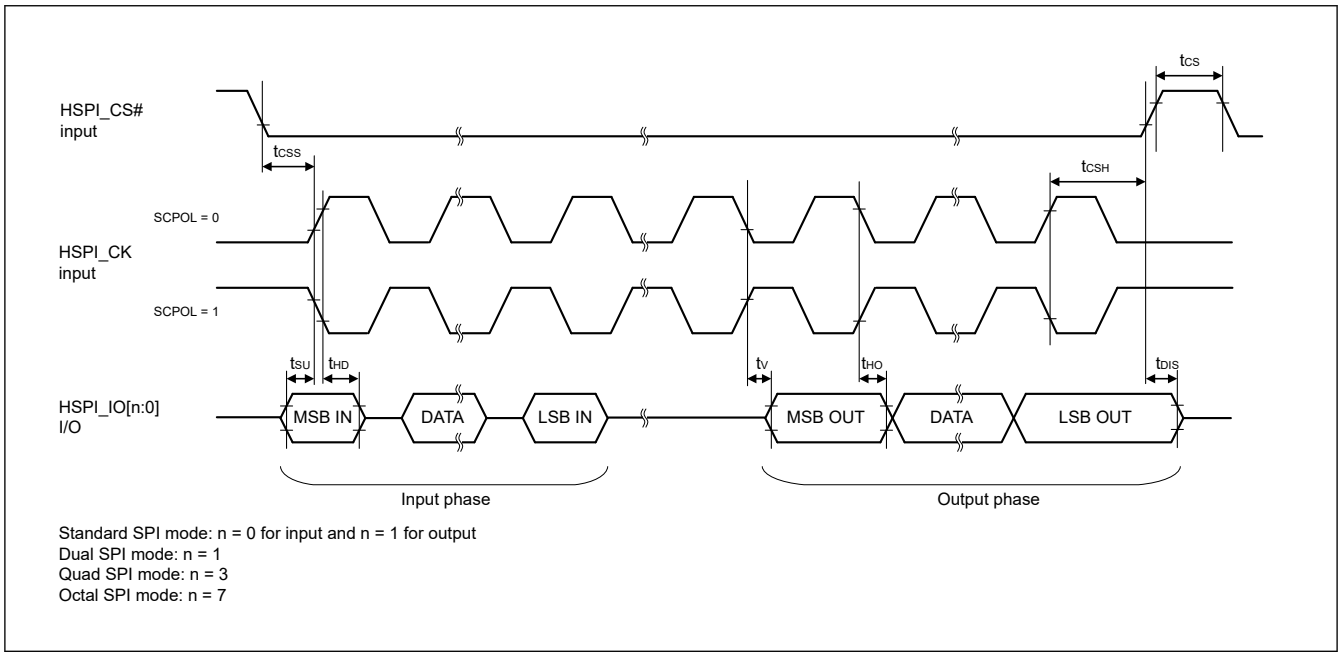


Figure 2.71 SHOSTIF timing (SCPH = 0)

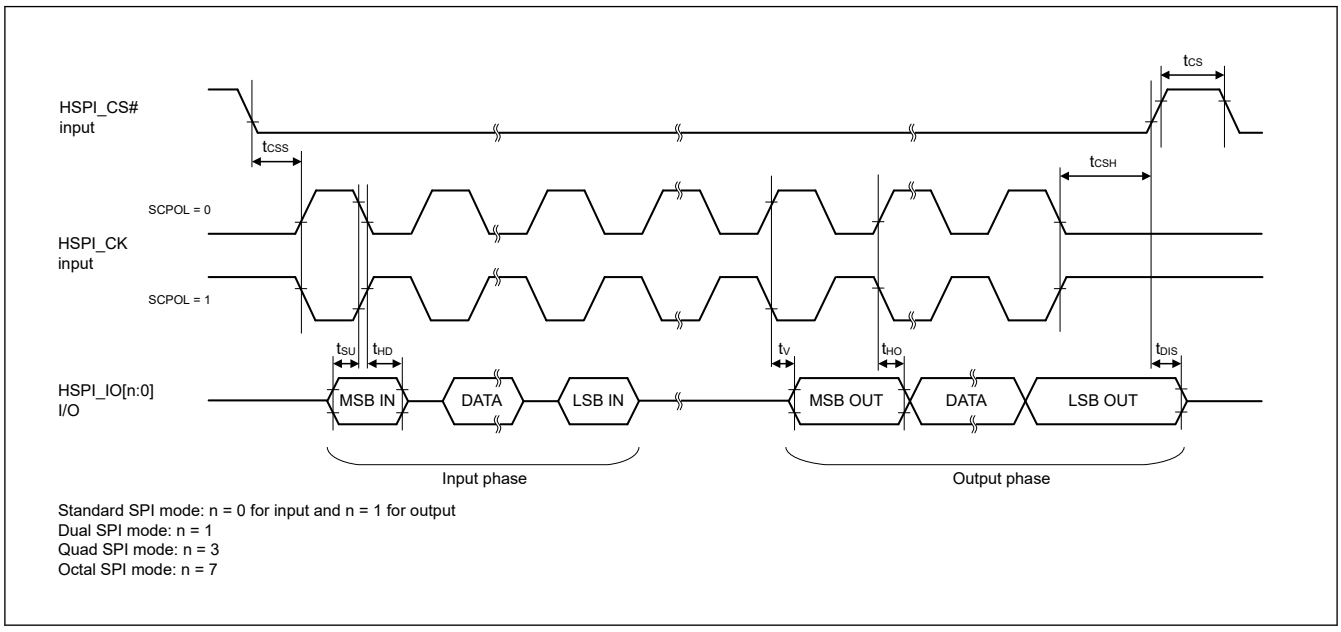


Figure 2.72 SHOSTIF timing (SCPH = 1)

2.5.5.17 PHOSTIF Timing

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF (3.3 V)

2.5.5.17.1 Synchronous SRAM Interface Mode

Table 2.41 PHOSTIF timing (Synchronous SRAM interface mode) (1 of 2)

Parameter	Symbol	Min.	Max.	Unit	Reference figure
HCKIO input cycle	t_{HCKIO}	20.0	—	ns	Figure 2.73 to Figure 2.77
HCKIO High-level width	t_{HBHIGH}	0.5 × t_{HCKIO} - 2.1	0.5 × t_{HCKIO} + 2.1	ns	
HCKIO Low-level width	t_{HBLOW}	0.5 × t_{HCKIO} - 2.1	0.5 × t_{HCKIO} + 2.1	ns	
Address and HCS0#/HCS# input setup time (to HCKIO rising edge)	t_{SKHA}	4.8	—	ns	
Address and HCS0#/HCS# input hold time (to HCKIO rising edge)	t_{HKHA}	1.0	—	ns	
HWR0#/HWR1#/HWR2#/HWR3# input setup time (to HCKIO rising edge)	t_{SKHWR}	4.8	—	ns	
HWR0#/HWR1#/HWR2#/HWR3# input hold time (to HCKIO rising edge)	t_{HKHWR}	1.0	—	ns	
HWRSTB# input setup time (to HCKIO rising edge)	$t_{SKHWRSTB}$	4.8	—	ns	
HWRSTB# input hold time (to HCKIO rising edge)	$t_{HKHWRSTB}$	1.0	—	ns	
HRD# input setup time (to HCKIO rising edge)	t_{SKHRD}	4.8	—	ns	
HRD# input hold time (to HCKIO rising edge)	t_{HKHRD}	1.0	—	ns	
Data input setup time (to HCKIO rising edge)	t_{SKIHD}	4.8	—	ns	
Data input hold time (to HCKIO rising edge)	t_{HKIHD}	1.0	—	ns	
Data and HWAIT# output delay time (to HRD# falling edge)	t_{DKHDHR}	2.0	—	ns	
Data and HWAIT# output hold time (to HRD# rising edge)	t_{HKOHD}	—	15.0	ns	
Data and HWAIT# output delay time (to HCS0#/HCS1# falling edge)	t_{DKHD}	2.0	—	ns	
Data and HWAIT# output hold time (to HCS0#/HCS1# rising edge)	t_{HKWTCS}	—	15.0	ns	
HWAIT# output delay time (to HWRSTB#, HWR0#/HWR1#/HWR2#/HWR3# falling edge)	t_{DKHWT}	2.0	—	ns	
HWAIT# output hold time (to HWRSTB#, HWR0#/HWR1#/HWR2#/HWR3# rising edge)	t_{HKWTWR}	—	15.0	ns	
HWAIT# output delay time (to HCKIO rising edge)	t_{DKHWTV}	2.0	16.0	ns	

Table 2.41 PHOSTIF timing (Synchronous SRAM interface mode) (2 of 2)

Parameter	Symbol	Min.	Max.	Unit	Reference figure
Data output delay time (to HCKIO rising edge)	t_{DKHDV}	2.0	16.0	ns	Figure 2.73 to Figure 2.77
Data and HWAIT# valid data output hold time (to HRD# rising edge)	$t_{HKHWTHR}$	2.0	—	ns	
HWR0#/HWR1#/HWR2#/HWR3#, HWRSTB# recovery time (High-level width)	t_{WHWR}	40.0	—	ns	
HRD# recovery time (High-level width)	t_{WHRD}	40.0	—	ns	

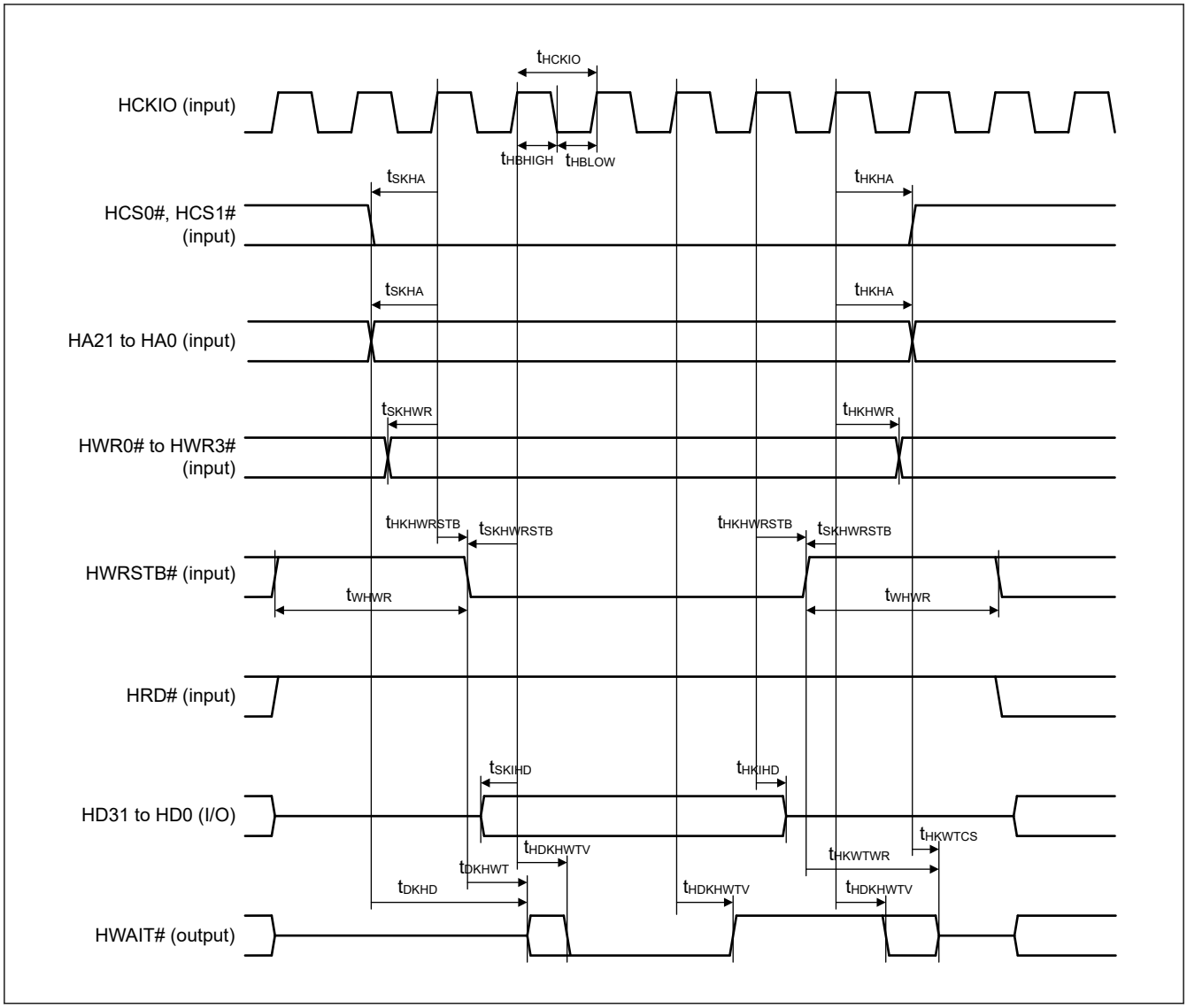


Figure 2.73 PHOSTIF write timing (Synchronous SRAM interface mode)

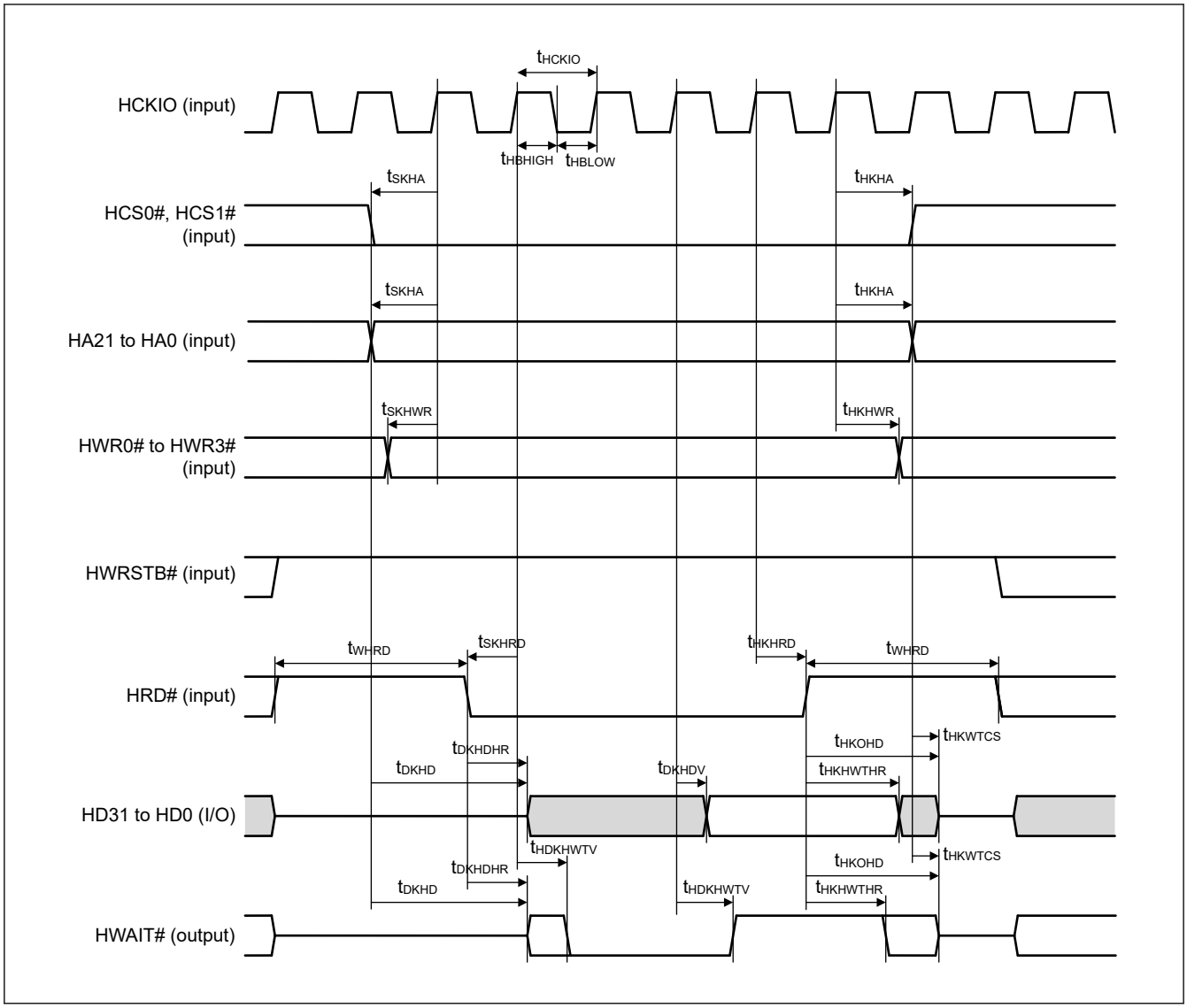


Figure 2.74 PHOSTIF read timing (Synchronous SRAM interface mode)

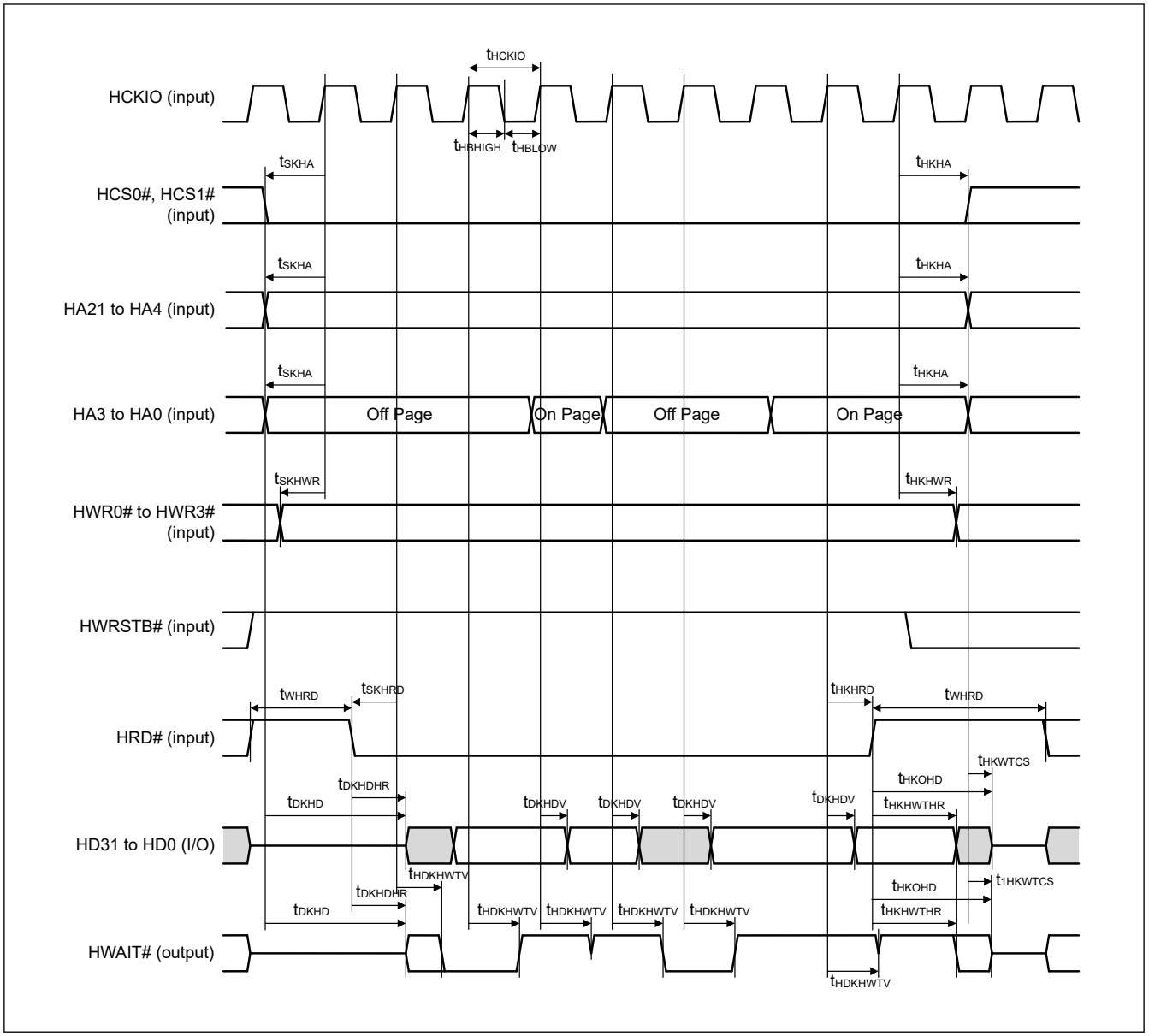


Figure 2.75 PHOSTIF page read timing (Synchronous SRAM interface mode)

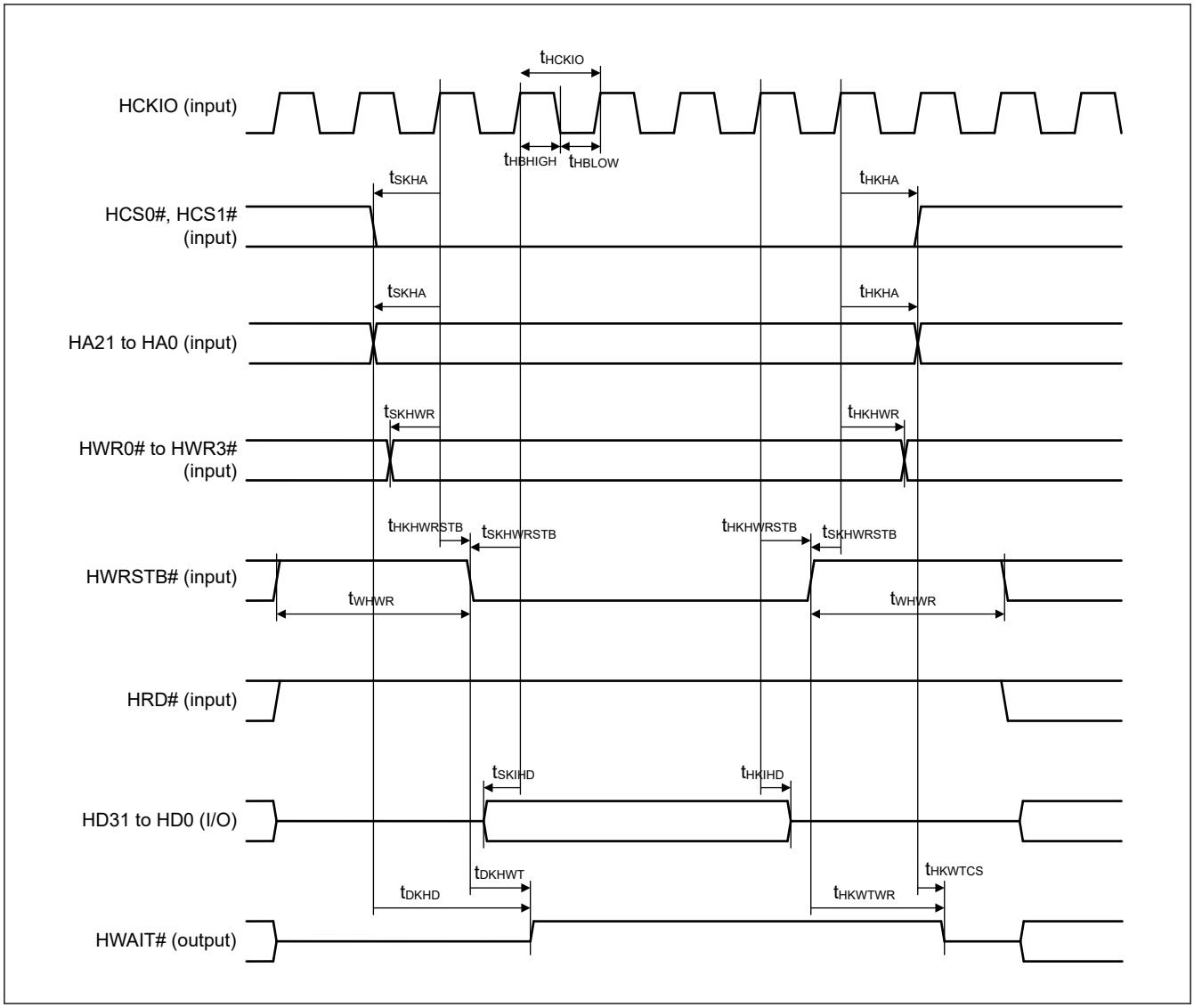


Figure 2.76 PHOSTIF page write timing (PHOSTIF register write) (Synchronous SRAM interface mode)

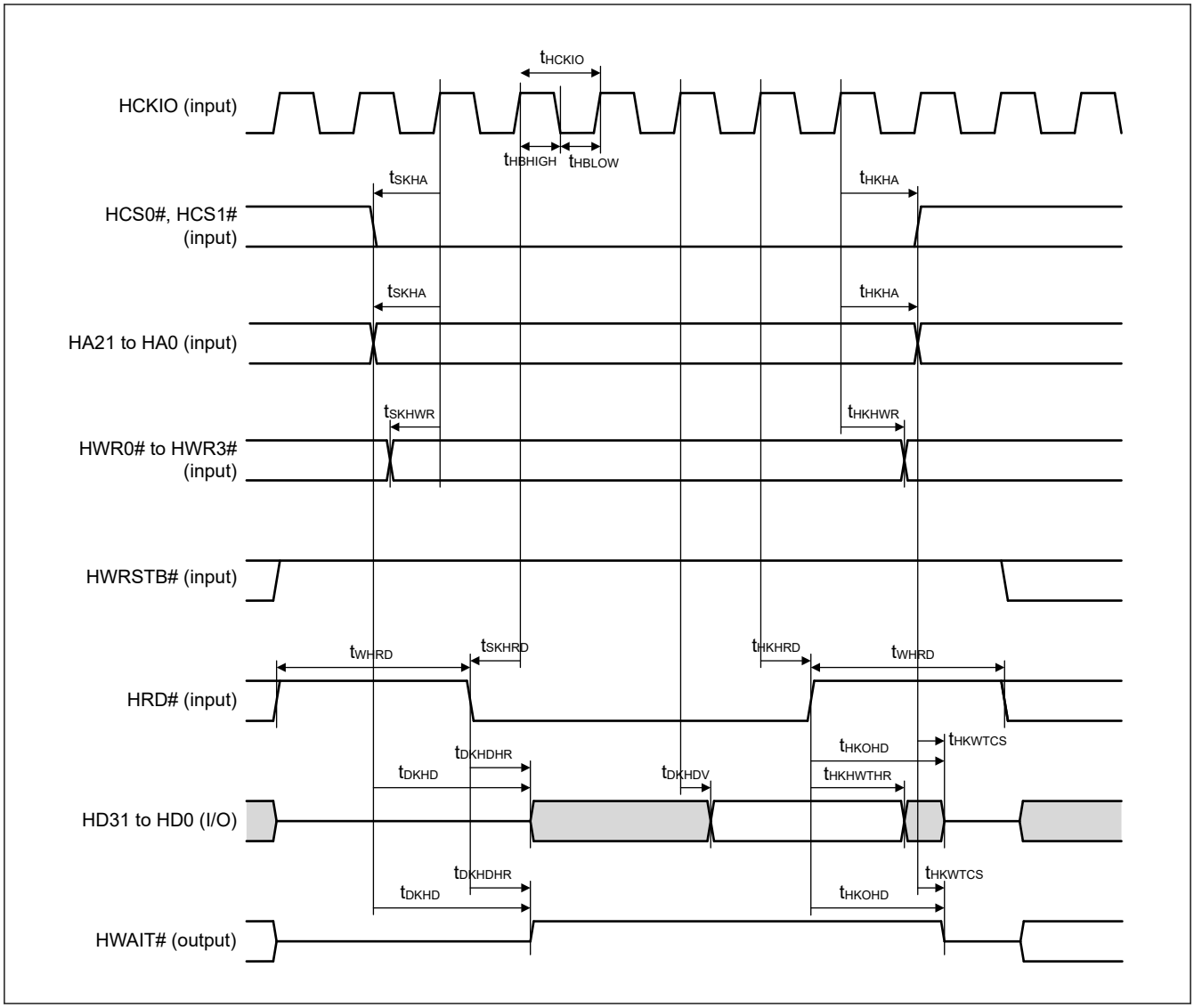


Figure 2.77 PHOSTIF page read timing (PHOSTIF register write) (Synchronous SRAM interface mode)

2.5.5.17.2 Asynchronous SRAM Interface Mode

Table 2.42 PHOSTIF timing (Asynchronous SRAM interface mode) (1 of 2)

Parameter	Symbol	Min.	Max.	Unit	Reference figure
Address, HCS0#/HCS1# input setup time (to HWRSTB#, HWR0#/HWR1#/HWR2#/HWR3# falling edge)	t_{ADDWRS}	0	—	ns	Figure 2.78 to Figure 2.81
HWR0#/HWR1#/HWR2#/HWR3# and HWRSTB# recovery time (High-level width)	t_{WRW}	20.0	—	ns	
Data input setup time (to HWRSTB#, HWR0#/HWR1#/HWR2#/HWR3# falling edge)	t_{WRS}	0	—	ns	
Data input hold time (to HWRSTB#, HWR0#/HWR1#/HWR2#/HWR3# rising edge)	t_{WRH}	0	—	ns	
HWAIT# output delay time (to HCS0#/HCS1# falling edge)	t_{CLZ}	2.0	—	ns	
HWAIT# output delay time (to HWRSTB#, HWR0#/HWR1#/HWR2#/HWR3# falling edge)	t_{WAITD}	2.0	—	ns	
HWAIT# valid data output delay time (for HWRSTB#, HWR0#/HWR1#/HWR2#/HWR3# falling edge)	$t_{WRWAITF}$	—	45.0	ns	
HWAIT# valid data output hold time (for HWRSTB#, HWR0#/HWR1#/HWR2#/HWR3# rising edge)	t_{WAITVH}	0	—	ns	
HWAIT# output hold time (to HWR0#/HWR1#/HWR2#/HWR3#, HWRSTB# rising edge)	t_{WAITH}	—	15.0	ns	
HWAIT# output hold time (to HCS0#/HCS1# rising edge)	t_{CHZ}	—	15.0	ns	
Address and HCS0#/HCS1# input setup time (to HRD# falling edge)	t_{ADDRDS}	0	—	ns	
Address input hold time in page access (to HRD# rising edge)	t_{ADDRDH}	0	—	ns	
HRD# recovery time (High-level width)	t_{RDW}	20.0	—	ns	
Data and HWAIT# output delay time (to HRD# falling edge)	t_{RDLZ}	2.0	—	ns	
HWAIT# valid data output delay time (to HRD# falling edge)	$t_{RDWAITF}$	—	45.0	ns	

Table 2.42 PHOSTIF timing (Asynchronous SRAM interface mode) (2 of 2)

Parameter	Symbol	Min.	Max.	Unit	Reference figure
Data fixing time (to HWAIT# rising edge)	t_{WAITR}	0	—	ns	Figure 2.78 to Figure 2.81
Data and HWAIT# valid data output hold time (to HRD# rising edge)	t_{DATAOH}	2.0	—	ns	
Data and HWAIT# output hold time (to HRD# rising edge)	t_{RDHZ}	—	15.0	ns	
Data and HWAIT# output delay time in on-page access (to addresses)	$t_{PAGEOND}$	18.0	35.0	ns	
Data and HWAIT# output delay time in off-page access (to addresses) (when not crossing a 16-byte boundary)	$t_{PAGEOFD}$	18.0	35.0	ns	
Data and HWAIT# output delay time in off-page access (to addresses) (when crossing a 16-byte boundary)	$t_{PAGEOFD}$	18.0	35.0	ns	
HWAIT# valid data output delay time (to HCS0#/HCS1# falling edge)	t_{WAITVD}	—	45.0	ns	
Data fixing time (to addresses)	t_{ADDFIX}	18.0	—	ns	

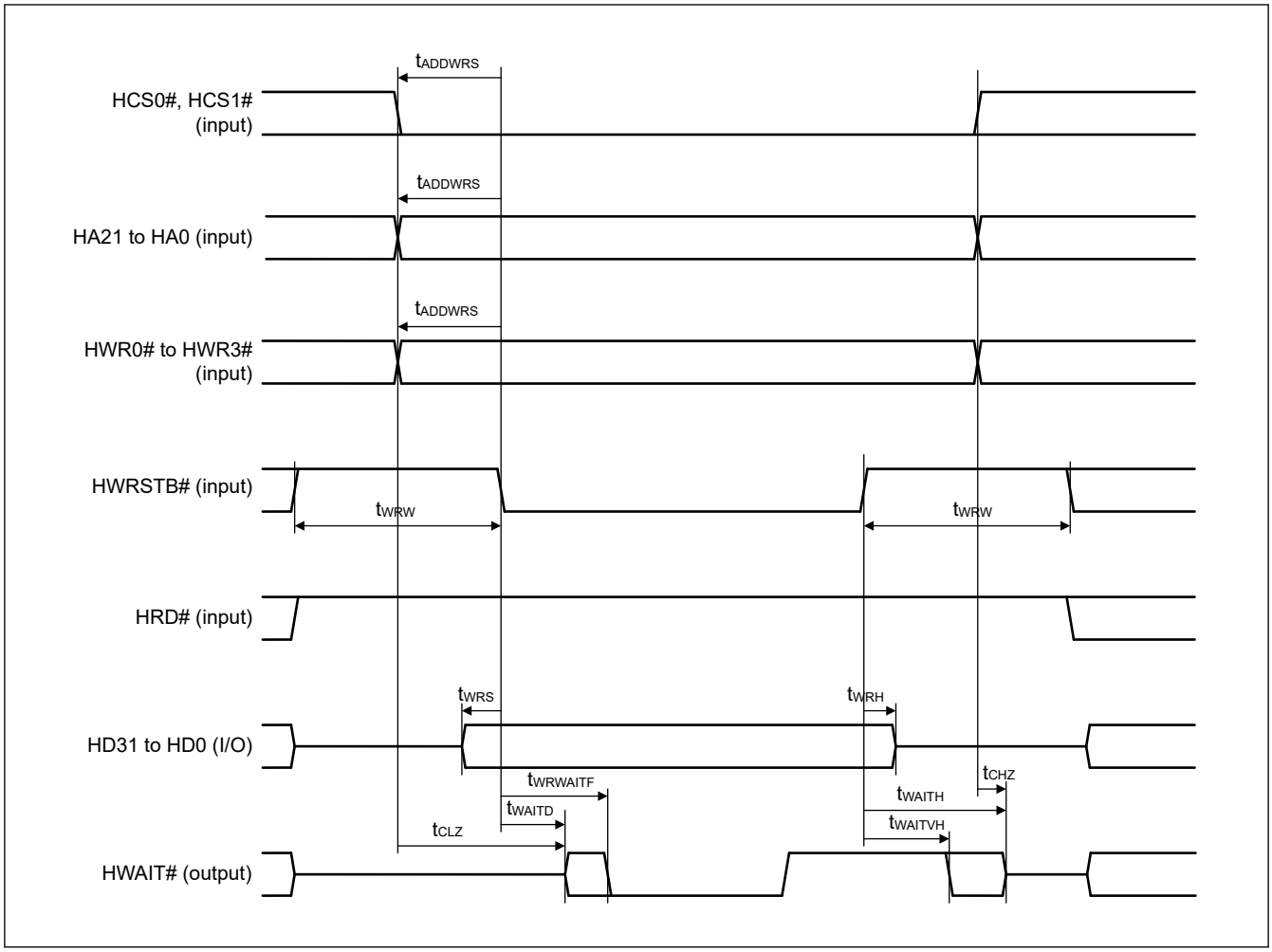


Figure 2.78 PHOSTIF write timing (Asynchronous SRAM interface mode)

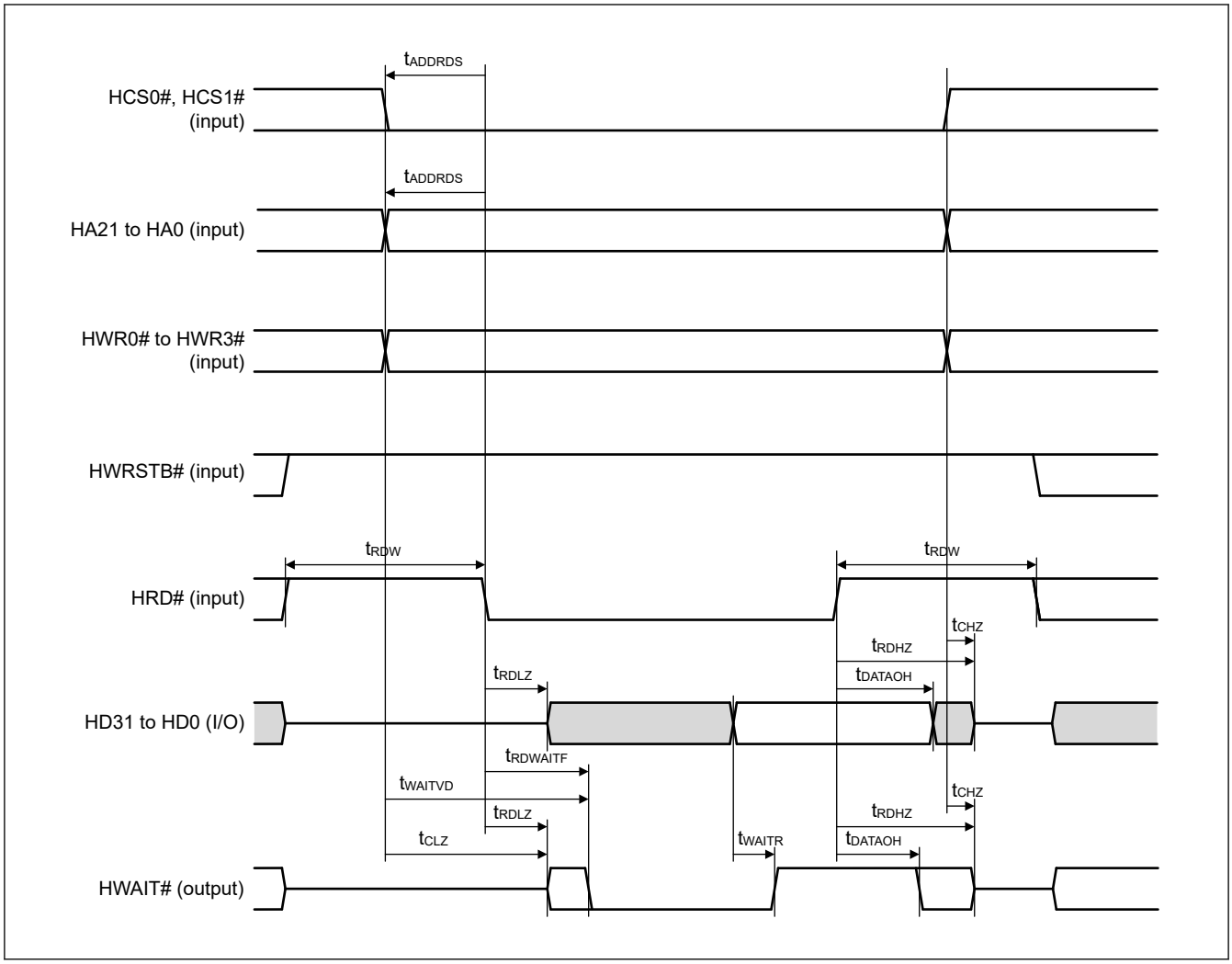


Figure 2.79 PHOSTIF read timing (Asynchronous SRAM interface mode)

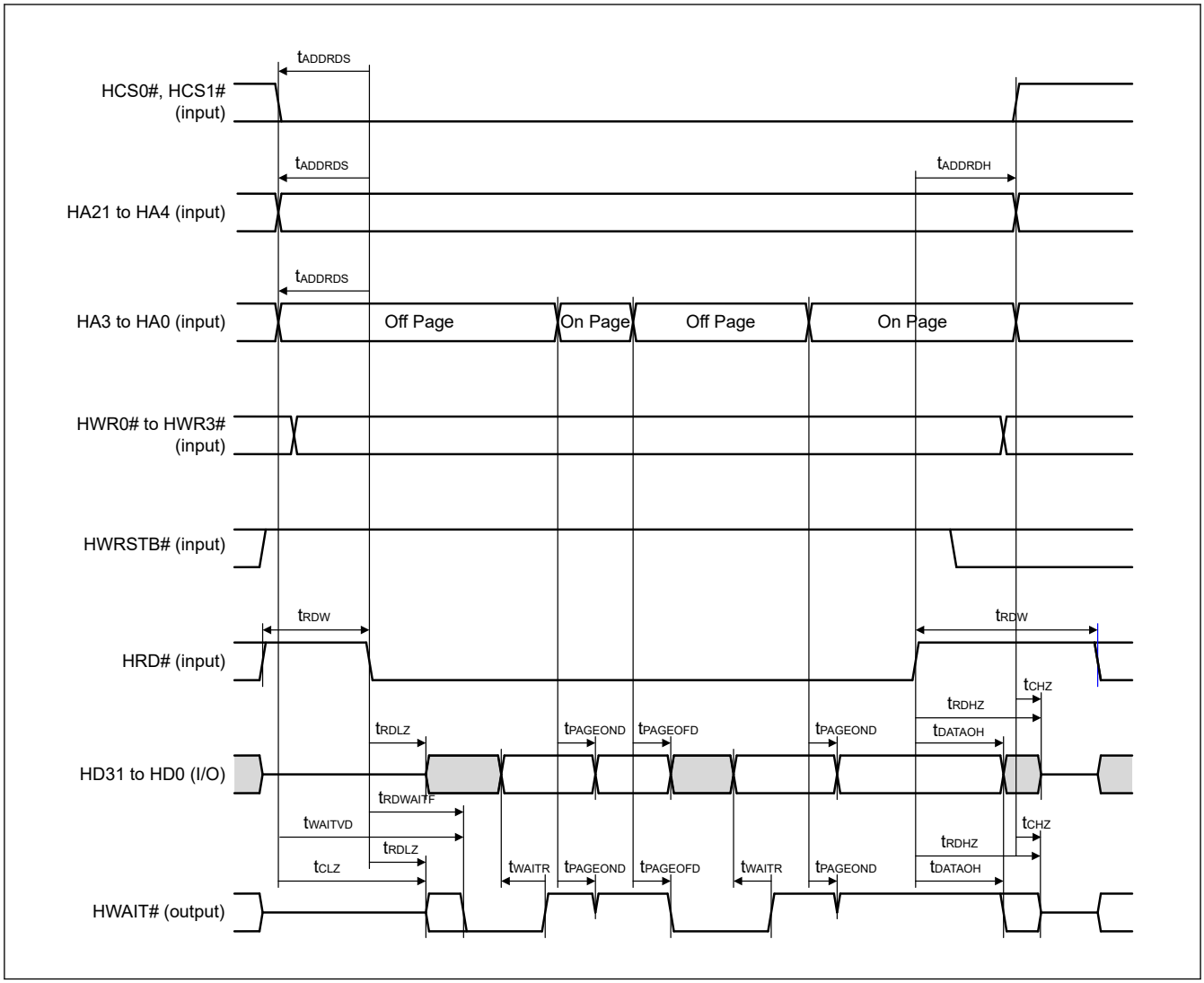


Figure 2.80 PHOSTIF page read timing (Asynchronous SRAM interface mode)

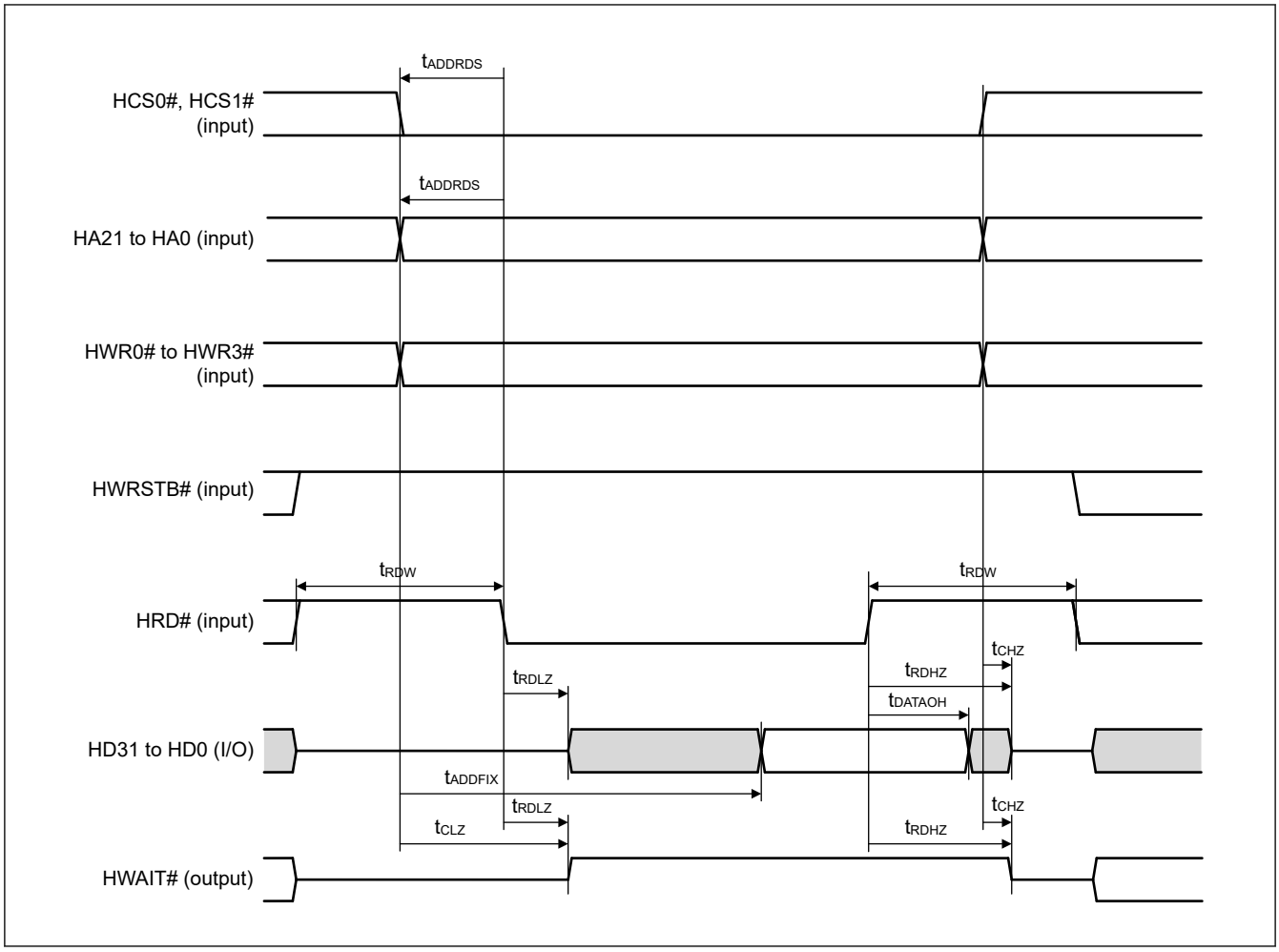


Figure 2.81 PHOSTIF register read timing (Asynchronous SRAM interface mode)

2.5.5.17.3 Synchronous Burst SRAM Type Transfer Mode

Table 2.43 PHOSTIF timing (Synchronous Burst SRAM Type interface mode) (1 of 2)

Parameter	Symbol	Min.	Max.	Unit	Reference figure
HCKIO input cycle	t_{HCKIO}	20.0	—	ns	Figure 2.82 to Figure 2.85
HCKIO High-level width	t_{HBHIGH}	0.5 × t_{HCKIO} - 2.1	0.5 × t_{HCKIO} + 2.1	ns	
HCKIO Low-level width	t_{HBLOW}	0.5 × t_{HCKIO} - 2.1	0.5 × t_{HCKIO} + 2.1	ns	
Address and HCS0#/HCS1# input setup time (to HCKIO rising edge)	t_{SKPHA}	4.8	—	ns	
Address and HCS0#/HCS1# input hold time (to HCKIO rising edge)	t_{HKPHA}	1.0	—	ns	
Address and HCS0#/HCS1# input setup time (to HCKIO falling edge)	t_{SKNHA}	4.8	—	ns	
Address and HCS0#/HCS1# input hold time (to HCKIO falling edge)	t_{HKNHA}	1.0	—	ns	
HWR0#/HWR1#/HWR2#/HWR3# input setup time (to HCKIO rising edge)	t_{SKPHWR}	4.8	—	ns	
HWR0#/HWR1#/HWR2#/HWR3# input hold time (to HCKIO rising edge)	t_{HKPHWR}	1.0	—	ns	
HWR0#/HWR1#/HWR2#/HWR3# input setup time (to HCKIO falling edge)	t_{SKNHWR}	4.8	—	ns	
HWR0#/HWR1#/HWR2#/HWR3# input hold time (to HCKIO falling edge)	t_{HKNHWR}	1.0	—	ns	
HBS#, HWRSTB# input setup time (to CKIO rising edge)	$t_{SKPHBCY}$	4.8	—	ns	
HBS#, HWRSTB# input hold time (to CKIO rising edge)	$t_{HKPHBCY}$	1.0	—	ns	
HBS#, HWRSTB# input setup time (to CKIO falling edge)	$t_{SKNHBCY}$	4.8	—	ns	
HBS#, HWRSTB# input hold time (to CKIO falling edge)	$t_{HKNHBCY}$	1.0	—	ns	
HRD# input setup time (to CKIO rising edge)	t_{SKPHRD}	4.8	—	ns	
HRD# input hold time (to CKIO rising edge)	t_{HKPHRD}	1.0	—	ns	
HRD# input setup time (to CKIO falling edge)	t_{SKNHRD}	4.8	—	ns	
HRD# input hold time (to CKIO falling edge)	t_{HKNHRD}	1.0	—	ns	

Table 2.43 PHOSTIF timing (Synchronous Burst SRAM Type interface mode) (2 of 2)

Parameter	Symbol	Min.	Max.	Unit	Reference figure
Data input setup time (to CKIO rising edge)	t_{SKPHD}	4.8	—	ns	Figure 2.82 to Figure 2.85
Data input hold time (to CKIO rising edge)	t_{HKPHD}	1.0	—	ns	
Data input setup time (to CKIO falling edge)	t_{SKNHD}	4.8	—	ns	
Data input hold time (to CKIO falling edge)	t_{HKNHD}	1.0	—	ns	
Data output delay time (to HRD# falling edge)	t_{DKNHRD}	2.0	—	ns	
Data output hold time (to HRD# rising edge)	t_{HKPHRD}	—	15.0	ns	
Data output delay time (to HCKIO rising edge)	t_{DKPHD}	2.0	16.0	ns	
Data output delay time (to HCKIO falling edge)	t_{DKNHD}	2.0	16.0	ns	
HWAIT# output delay time (to HCKIO rising edge)	t_{DKPHWT}	2.0	16.0	ns	
HWAIT# output delay time (to HCKIO falling edge)	t_{DKNHWT}	2.0	16.0	ns	
Data output hold time (to HCS0#/HCS1# rising edge)	t_{HKPHCS}	—	15.0	ns	
HWRSTB# recovery time (High-level width)	t_{WHWR}	40.0	—	ns	
HRD# recovery time (High-level width)	t_{WHRD}	40.0	—	ns	

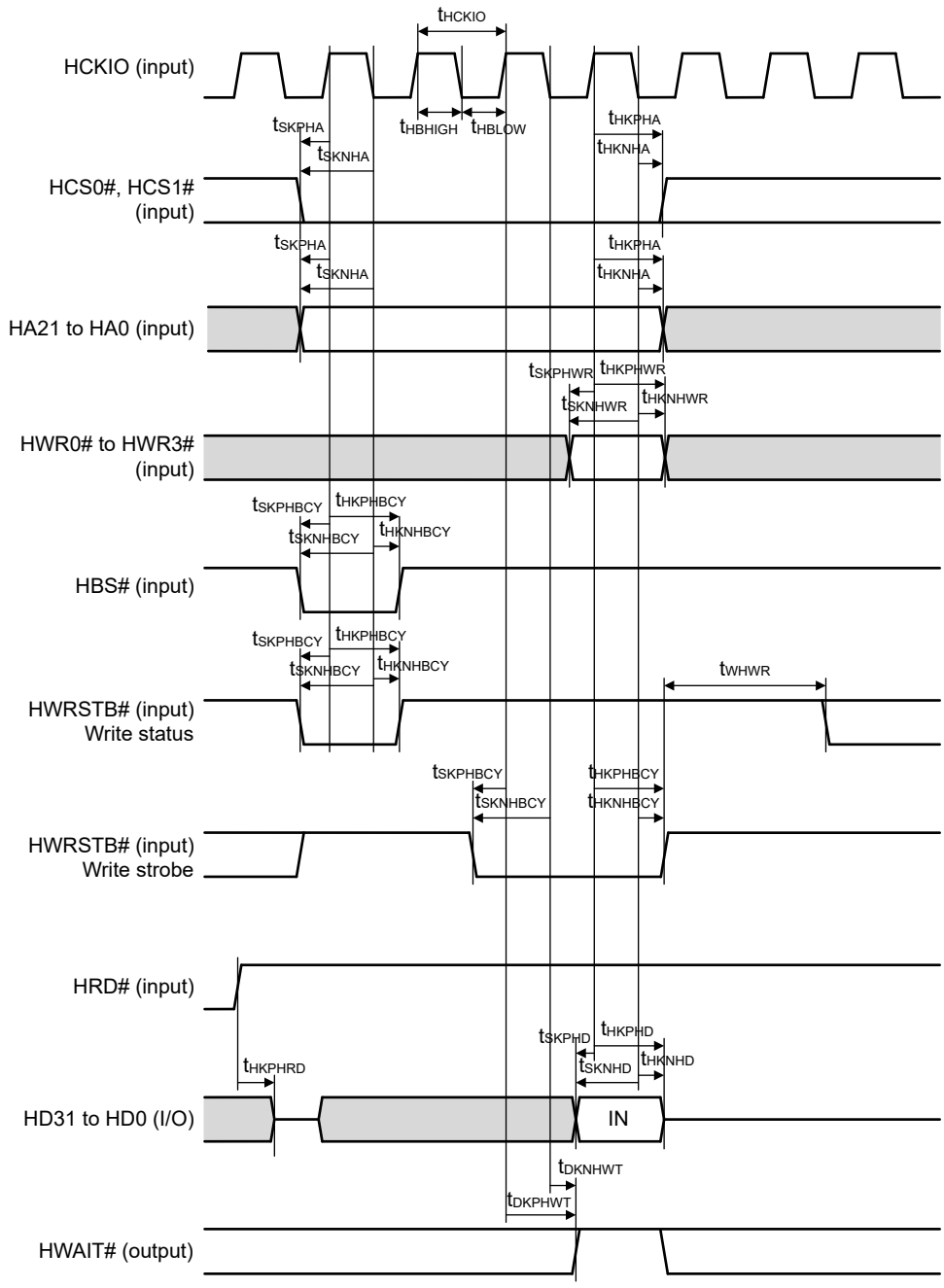


Figure 2.82 PHOSTIF write timing (Synchronous Burst SRAM Type transfer mode, Address/Data separation)

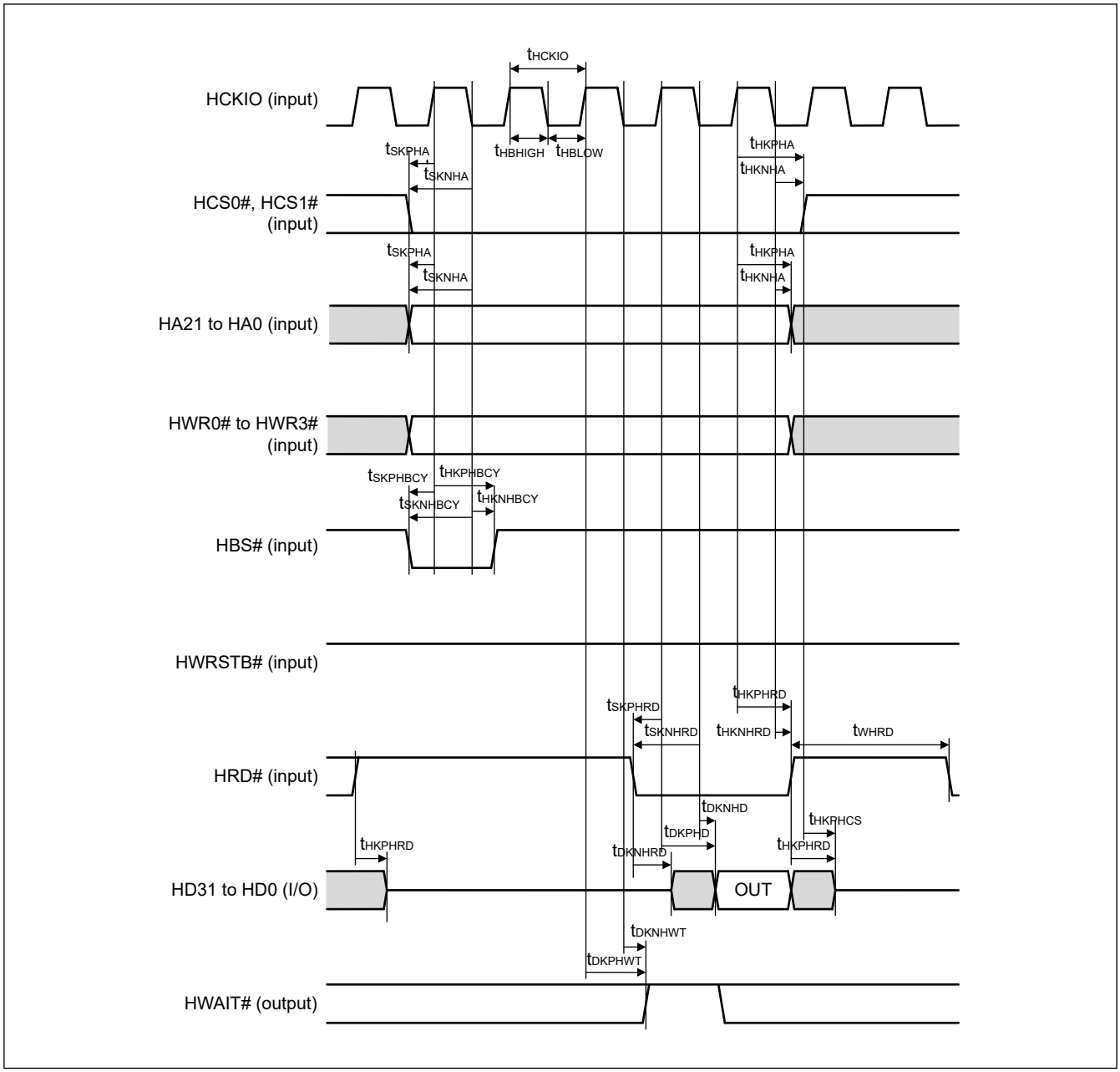


Figure 2.83 PHOSTIF read timing (Synchronous Burst SRAM Type transfer mode, Address/Data separation)

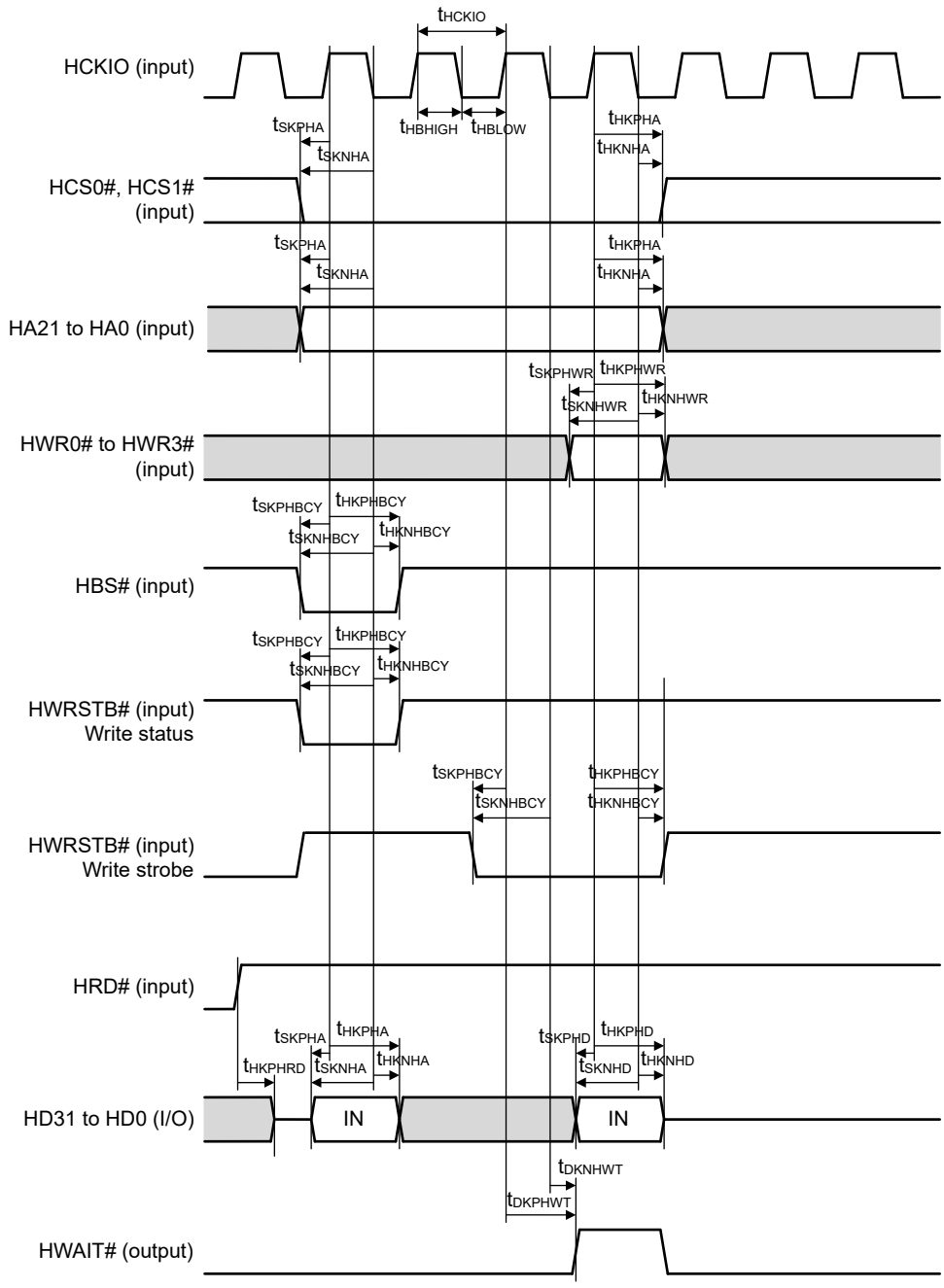


Figure 2.84 PHOSTIF write timing (Synchronous Burst SRAM Type transfer mode, Address/Data multiplexing)

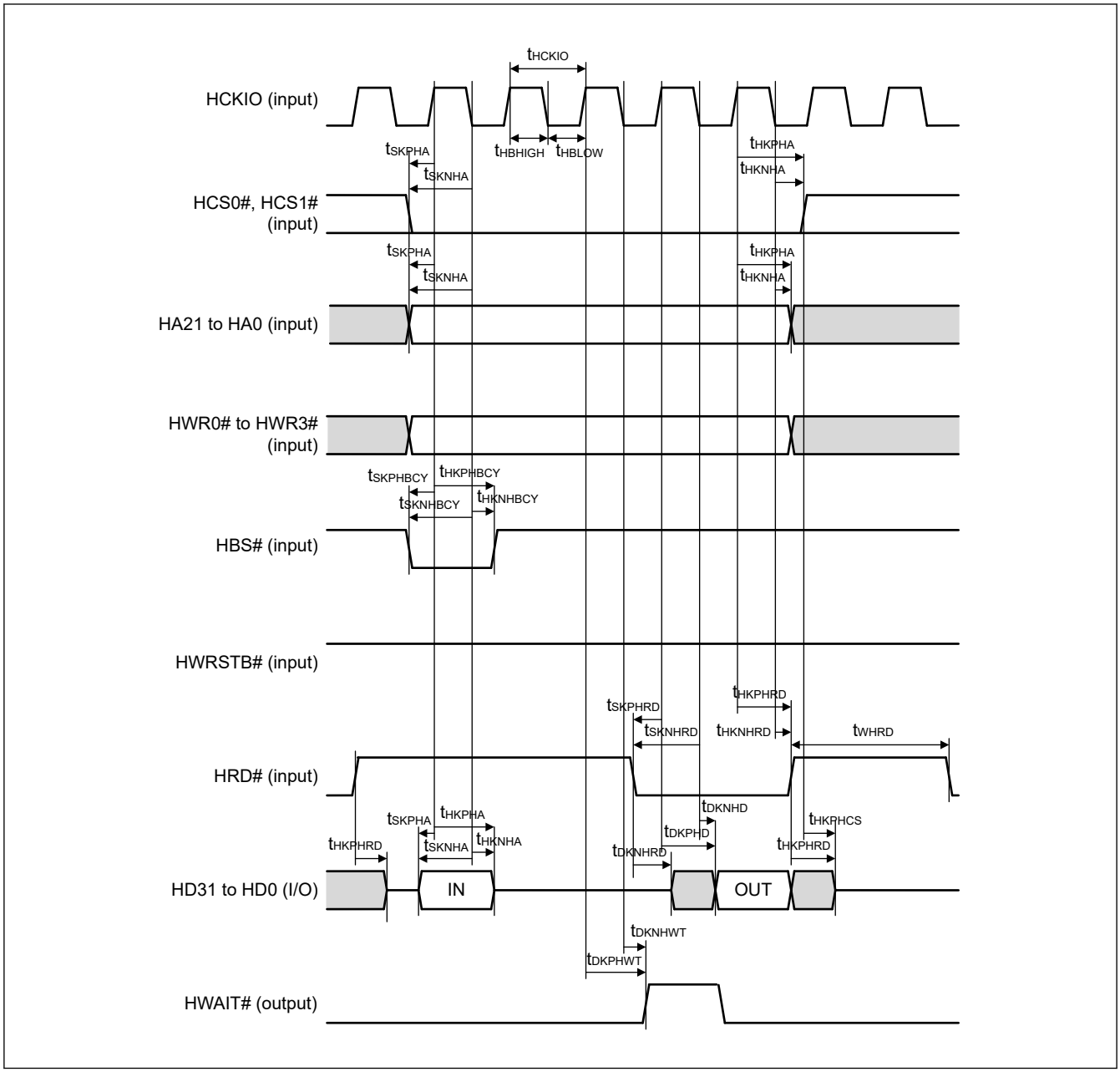


Figure 2.85 PHOSTIF read timing (Synchronous Burst SRAM Type transfer mode, Address/Data multiplexing)

2.5.5.18 SDHC Timing

Conditions: V_{OH} = VCC18 × 0.5, V_{OL} = VCC18 × 0.5

Table 2.44 1.8V SDHI timing (1 of 2)

Parameter		Symbol	Conditions	Min.	Max.	Unit.	Reference figure
(SD) SDR104 (eMMC) HS200	SD_CLK clock cycle	T_{SDCYC}	C = 15 pF Drive strength Clock: Ultra-high Others: High	6.67		ns	Figure 2.86
	SD_CLK clock high level width	T_{SDWH}		1.99	—	ns	
	SD_CLK clock low level width	T_{SDWL}		1.99	—	ns	
	SD_CLK clock rise time	T_{SDLH}		—	1	ns	
	SD_CLK clock fall time	T_{SDHL}		—	1	ns	
	SD_CMD, SD_DATA output delay	T_{SDODLY}		-2.2	1.5	ns	
	SD_CMD, SD_DATA input setup time	T_{SDIS}		—	—	ns	
	SD_CMD, SD_DATA input hold time	T_{SDIH}		—	—	ns	
	SD_CMD, SD_DATA input data width	T_{SDIDW}		3.83	—	ns	
(SD) SDR50, SDR25, SDR12 (eMMC) High Speed SDR, Backwards Compatibility	SD_CLK clock cycle	T_{SDCYC}	C = 30 pF Drive strength Clock: Ultra-high Others: High	10/13.33*1	—	ns	Figure 2.86
	SD_CLK clock high level width	T_{SDWH}		3/3.99*1	—	ns	
	SD_CLK clock low level width	T_{SDWL}		3/3.99*1	—	ns	
	SD_CLK clock rise time	T_{SDLH}		—	2	ns	
	SD_CLK clock fall time	T_{SDHL}		—	2	ns	
	SD_CMD, SD_DATA output delay	T_{SDODLY}		-4.2	1.8	ns	
	SD_CMD, SD_DATA input set up time	T_{SDIS}		1.3/1.4*1	—	ns	
	SD_CMD, SD_DATA input hold time	T_{SDIH}		1.8	—	ns	
	SD_CMD, SD_DATA input data width	T_{SDIDW}		—	—	ns	

Table 2.44 1.8V SDHI timing (2 of 2)

Parameter		Symbol	Conditions	Min.	Max.	Unit.	Reference figure
(SD) DDR50 (eMMC) High Speed DDR	SD_CLK clock cycle	T_{SDCYC}	C = 25 pF Drive strength Clock: High Others: High	20/26.66*1	—	ns	Figure 2.87
	SD_CLK clock high level width	T_{SDWH}		9/11.9*1	11/14.66*1	ns	
	SD_CLK clock low level width	T_{SDWL}		9/11.9*1	11/14.66*1	ns	
	SD_CLK clock rise time	T_{SDLH}		—	3	ns	
	SD_CLK clock fall time	T_{SDHL}		—	3	ns	
	SD_CMD output delay (SDR)	T_{SDODLY}		-6	3	ns	
	SD_CMD input set up time (SDR)	T_{SDIS}		4.8	—	ns	
	SD_CMD input hold time (SDR)	T_{SDIH}		2.5	—	ns	
	SD_DATA output delay (DDR)	T_{SDODLY_DDR}		2.6	6	ns	
	SD_DATA input set up time (DDR)	T_{SDIS_DDR}		1.5	—	ns	
	SD_DATA input hold time (DDR)	T_{SDIH_DDR}		1.5	—	ns	

Note 1. Specification at 200 MHz/Specification at 150 MHz

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5

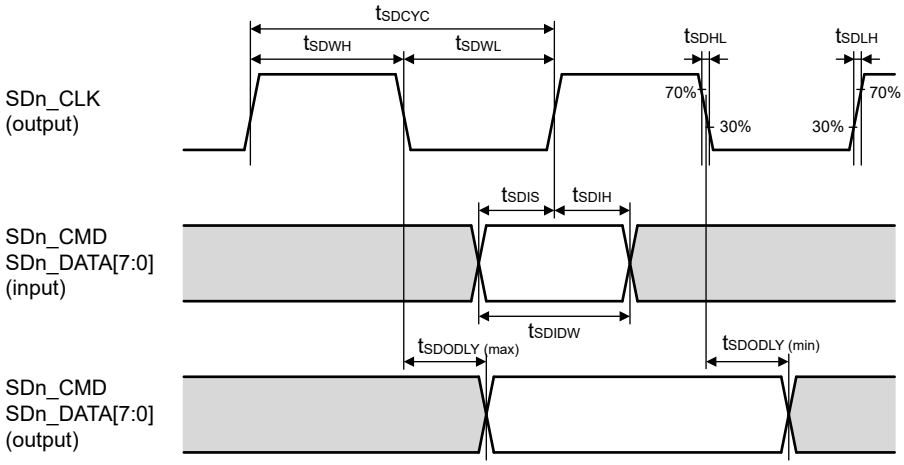
Table 2.45 3.3V SDHI timing (1 of 2)

Parameter		Symbol	Conditions	Min.	Max.	Unit.	Reference figure
(SD) High Speed (eMMC) High Speed SDR	SD_CLK clock cycle	T_{SDCYC}	C = 30 pF Drive strength Clock: High Others: Middle	20/26.66*1	—	ns	Figure 2.86
	SD_CLK clock high level width	T_{SDWH}		7	—	ns	
	SD_CLK clock low level width	T_{SDWL}		7	—	ns	
	SD_CLK clock reset time	T_{SDLH}		—	3	ns	
	SD_CLK clock fall time	T_{SDHL}		—	3	ns	
	SD_CMD, SD_DATA output delay	T_{SDODLY}		-6.2	2.5	ns	
	SD_CMD, SD_DATA input setup time	T_{SDIS}		4	—	ns	
	SD_CMD, SD_DATA input hold time	T_{SDIH}		2	—	ns	
	SD_CMD, SD_DATA input data width	T_{SDIDW}		—	—	ns	

Table 2.45 3.3V SDHI timing (2 of 2)

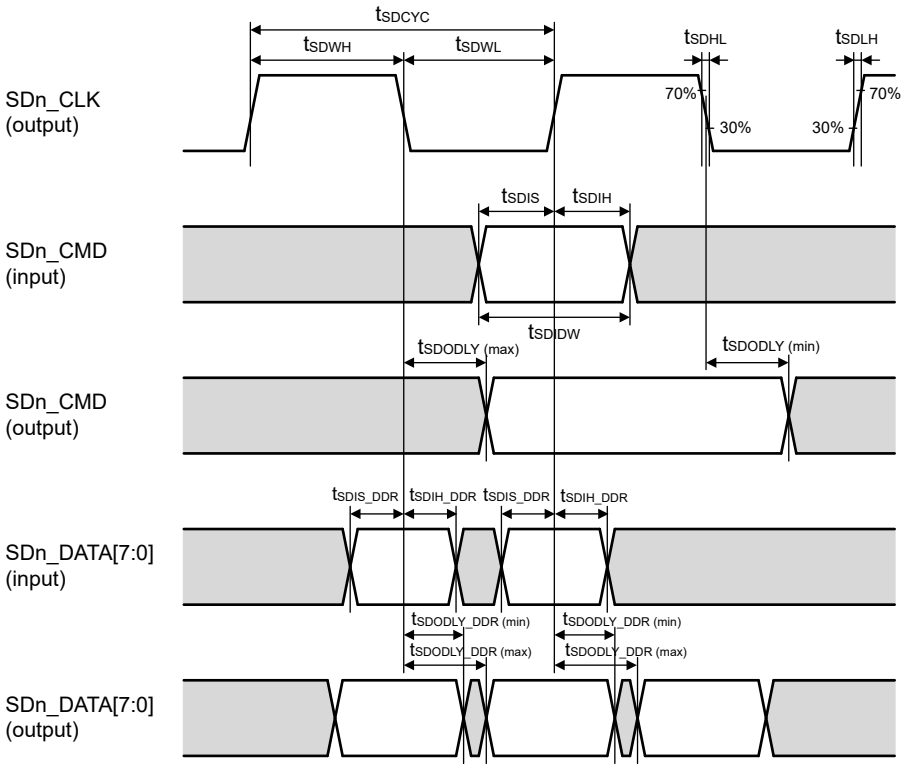
Parameter		Symbol	Conditions	Min.	Max.	Unit.	Reference figure
(SD) Default Speed (eMMC) Backwards Compatibility	SD_CLK clock cycle	T_{SDCYC}	C = 30 pF Drive strength Clock: High Others: Middle	40/53.32*1	—	ns	Figure 2.86
	SD_CLK clock high level width	T_{SDWH}		10	—	ns	
	SD_CLK clock low level width	T_{SDWL}		10	—	ns	
	SD_CLK clock reset time	T_{SDLH}		—	10	ns	
	SD_CLK clock fall time	T_{SDHL}		—	10	ns	
	SD_CMD, SD_DATA output delay	T_{SDODLY}		-7.5	2.5	ns	
	SD_CMD, SD_DATA input setup time	T_{SDIS}		4	—	ns	
	SD_CMD, SD_DATA input hold time	T_{SDIH}		2	—	ns	
	SD_CMD, SD_DATA input data width	T_{SDIDW}		—	—	ns	
(eMMC) High Speed DDR	SD_CLK clock cycle	T_{SDCYC}	C = 20 pF Drive strength Clock: High Others: High	20/26.66*1	—	ns	Figure 2.86 to Figure 2.87
	SD_CLK clock high level width	T_{SDWH}		9/11.99*1	11/14.66*1	ns	
	SD_CLK clock low level width	T_{SDWL}		9/11.99*1	11/14.66*1	ns	
	SD_CLK clock rise time	T_{SDLH}		—	3	ns	
	SD_CLK clock fall time	T_{SDHL}		—	3	ns	
	SD_CMD output delay (SDR)	T_{SDODLY}		-6	6	ns	
	SD_CMD input setup time (SDR)	T_{SDIS}		4.8	—	ns	
	SD_CMD input hold time (SDR)	T_{SDIH}		2.5	—	ns	
	SD_DATA output delay (DDR)	T_{SDODLY_DDR}		2.5	6.5/6.8*1	ns	
	SD_DATA input setup time (DDR)	T_{SDIS_DDR}		2.23/2.5*1	—	ns	
	SD_DATA input hold time (DDR)	T_{SDIH_DDR}		1.5	—	ns	

Note 1. Specification at 200 MHz/Specification at 150 MHz



n = 0, 1
For n = 1, SDn_DATA[7:4] are not available.

Figure 2.86 SDHI timing (SDR)



n = 0, 1
For n = 1, SDn_DATA[7:4] are not available.

Figure 2.87 SDHI timing (DDR)

2.5.5.19 NANDC Timing

Conditions: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5, C = 30 pF (3.3 V)

Table 2.46 NANDC timing

Parameter			Symbol	Min.	Max.	Unit	Reference figure
NANDC	CLE hold time	Performance mode	t_{CLH}	1.5 × t_{NF_CLK} - 2.0	—	ns	Figure 2.88 to Figure 2.91
		Extended mode		t_{NF_CLK} - 3.0*1	—	ns	
	CE# hold time	Performance mode	t_{CH}	2.5 × t_{NF_CLK} - 2.0	—	ns	
		Extended mode		t_{NF_CLK} - 8.0*1	—	ns	
	WE# pulse width	Performance mode	t_{WP}	0.5 × t_{NF_CLK} - 2.0	—	ns	
		Extended mode		t_{NF_CLK} - 3.0*1	—	ns	
	WE# high hold time	Performance mode	t_{WH}	0.5 × t_{NF_CLK} - 2.0	—	ns	
		Extended mode		t_{NF_CLK} - 3.0*1	—	ns	
	ALE hold time	Performance mode	t_{ALH}	0.5 × t_{NF_CLK} - 3.0	—	ns	
		Extended mode		t_{NF_CLK} - 4.0*1	—	ns	
	RE# pulse width	Performance mode	t_{RP}	0.5 × t_{NF_CLK} - 2.0	—	ns	
		Extended mode		t_{NF_CLK} - 3.0*1	—	ns	
	RE# high hold time	Performance mode	t_{RH}	0.5 × t_{NF_CLK} - 2.0	—	ns	
		Extended mode		t_{NF_CLK} - 3.0*1	—	ns	
	Data output hold time	Performance mode	t_{DH}	0.5 × t_{NF_CLK} - 4.0	—	ns	
		Extended mode		t_{NF_CLK} - 6.0*1	—	ns	
	Waiting time from WE# high to RY_BY[3:0]#		t_{WB}	52 × t_{NF_CLK} - 2.0*2	—	ns	

Note: t_{NF_CLK}: NF_CLK cycle
Note 1. Performance mode. In the extended mode, it depends on the register settings.
Note 2. RY/BY# capture timing can be extended by the register setting.

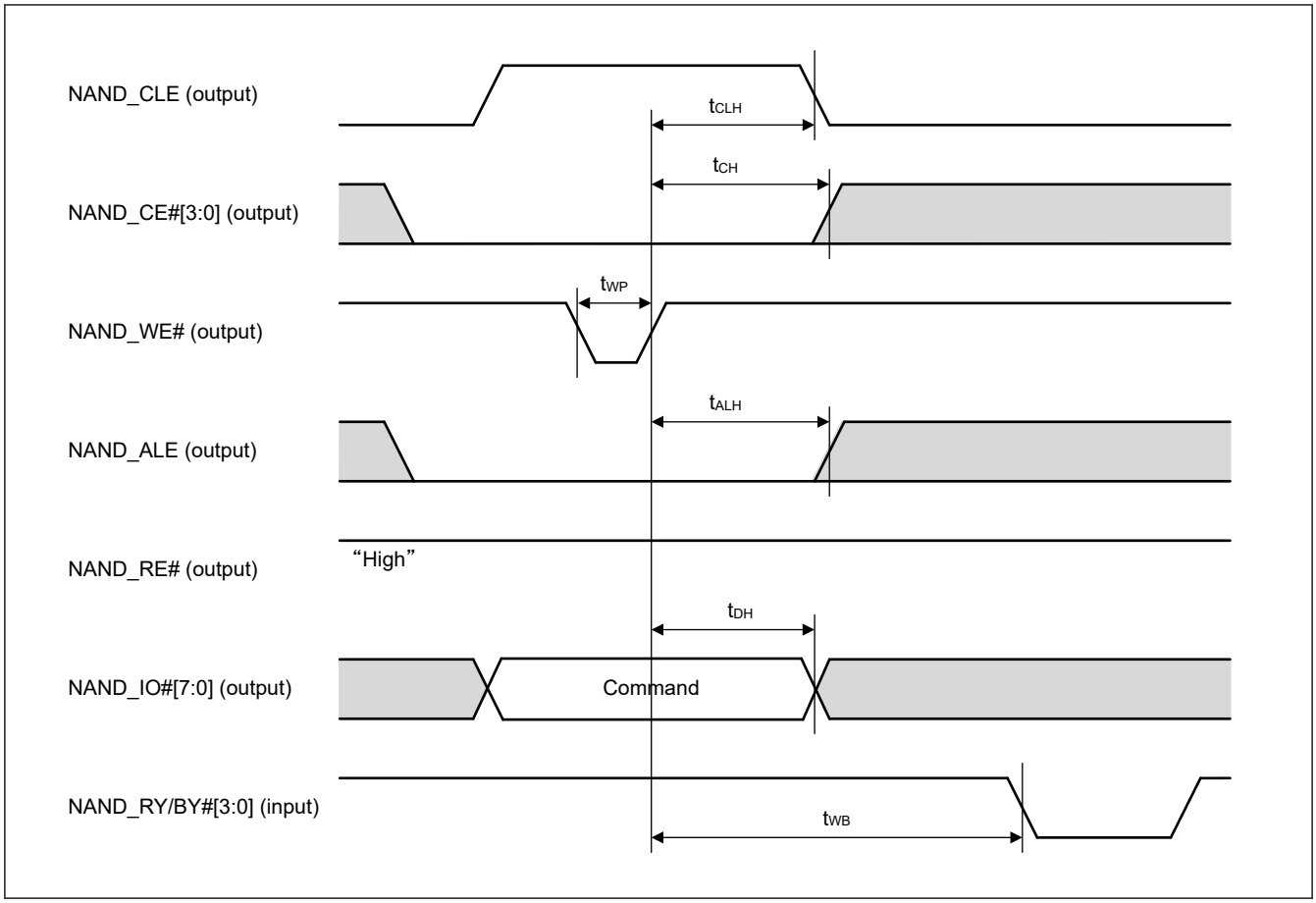


Figure 2.88 Command timing

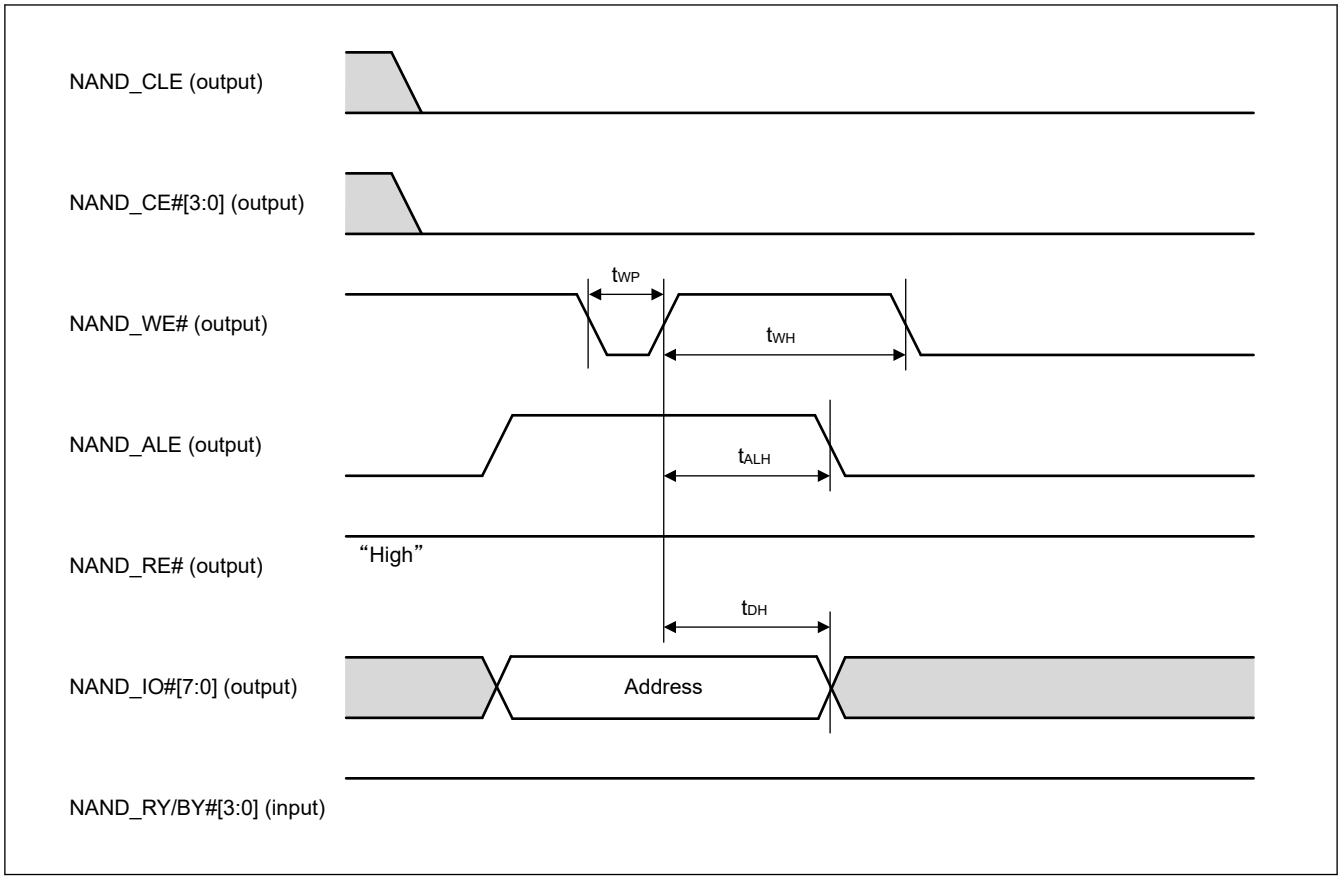


Figure 2.89 Address timing

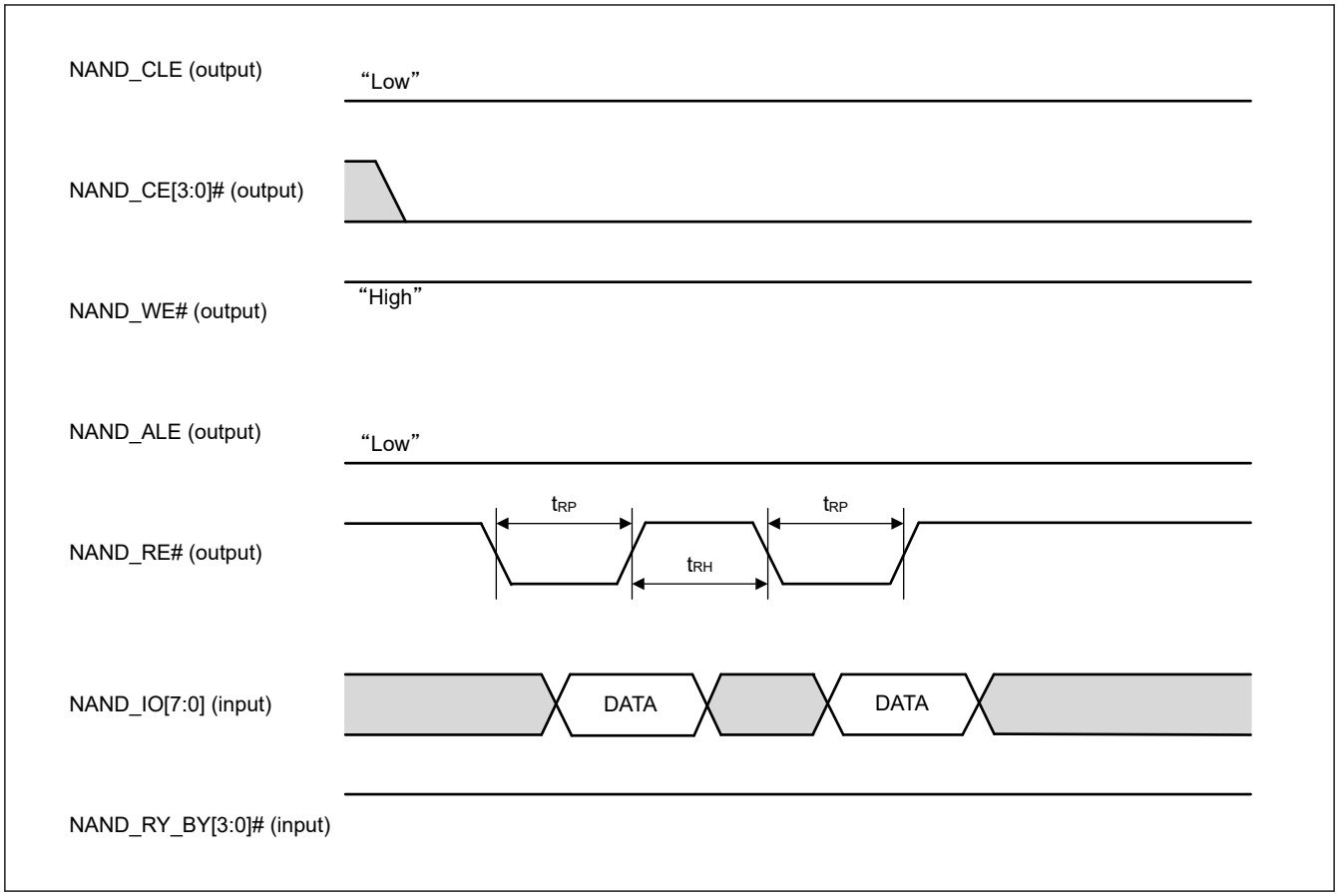


Figure 2.90 Data read timing

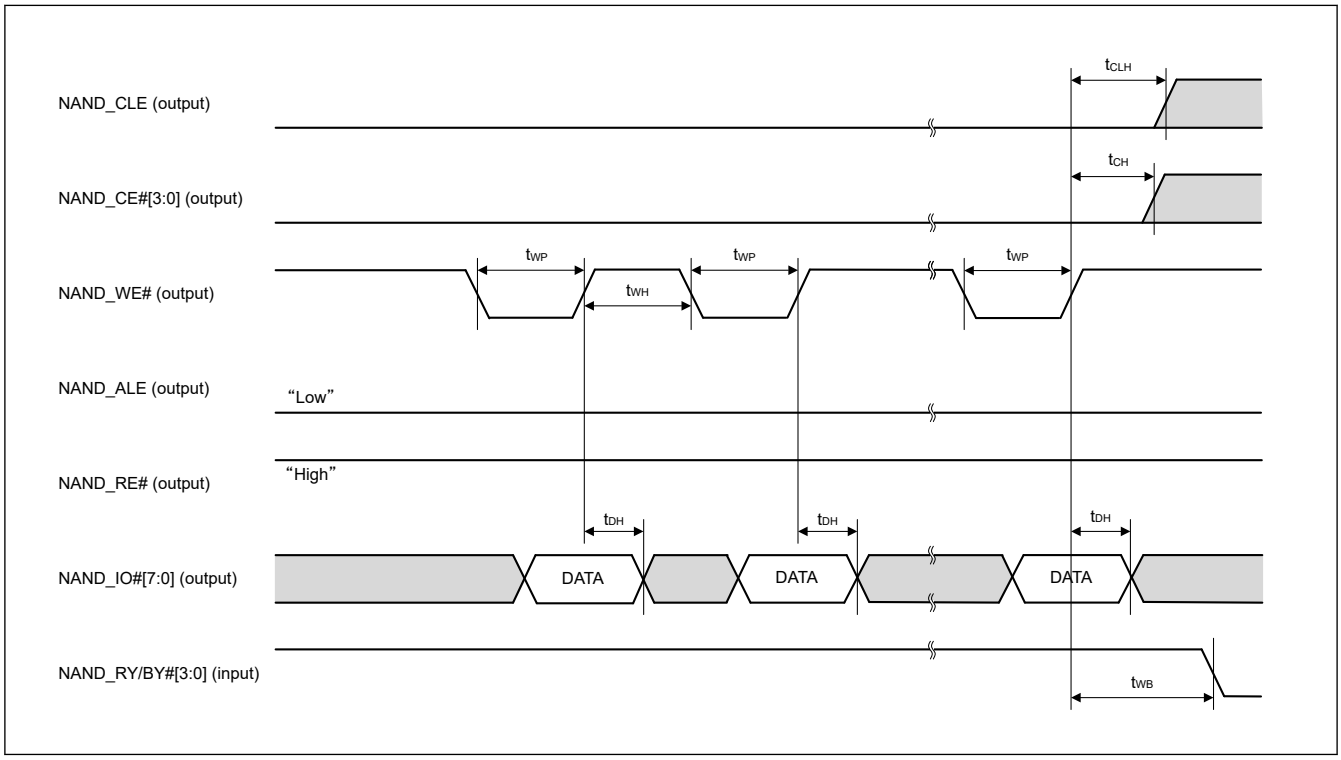


Figure 2.91 Data write timing

2.6 USB Characteristics

Table 2.47 On-chip USB low-speed (host only) characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference figure
Rising time	t_{LR}	75	—	300	ns	Figure 2.92, Figure 2.93
Falling time	t_{LF}	75	—	300	ns	
Rising/falling time ratio	t_{LR}/t_{LF}	80	—	125	%	

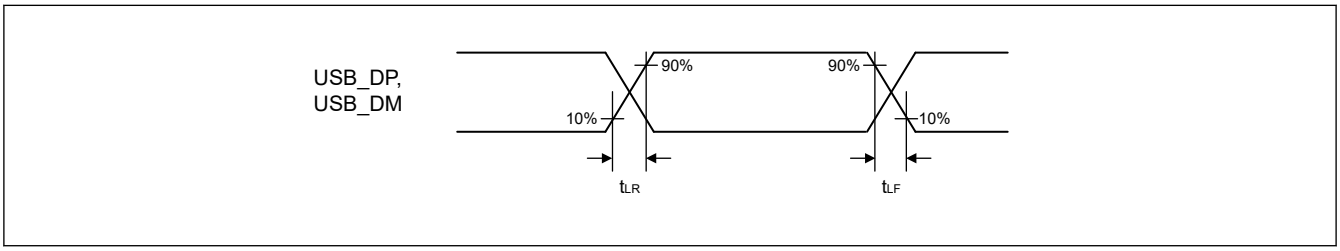


Figure 2.92 USB_DP, USB_DM output timing (low-speed/host only)

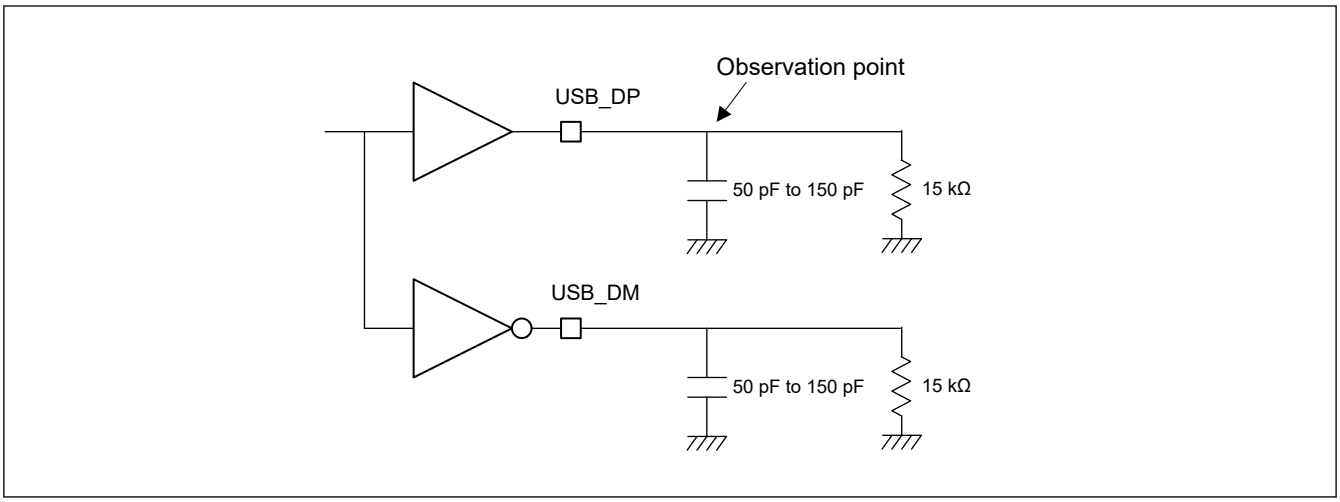


Figure 2.93 Measurement circuit (low-speed/host only)

Table 2.48 On-chip USB full-speed characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference figure
Rising time	t_{FR}	4	—	20	ns	Figure 2.94, Figure 2.95
Falling time	t_{FF}	4	—	20	ns	
Rising/falling time ratio	t_{FR}/t_{FF}	90	—	111.11	%	

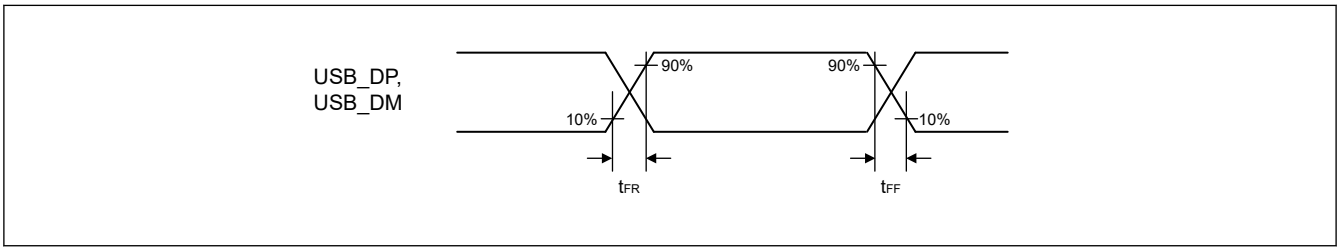


Figure 2.94 USB_DP, USB_DM output timing (full speed)

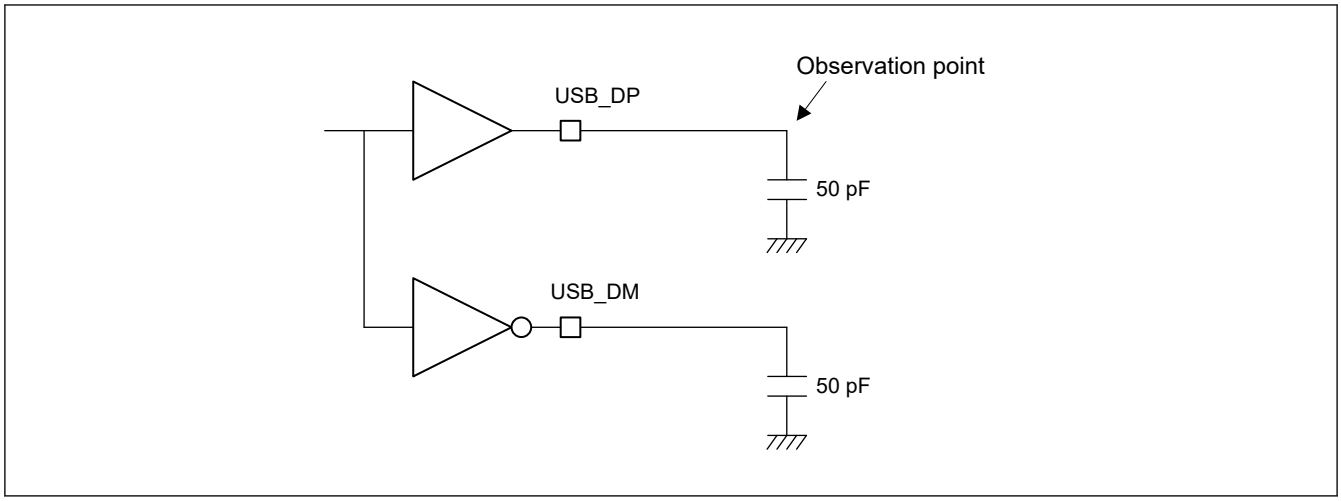


Figure 2.95 Measurement circuit (full speed)

Table 2.49 On-chip USB high-speed characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference figure
Rising time	t_{HSR}	—	—	2.133	V/µs	Figure 2.96, Figure 2.97
Falling time	t_{HSF}	—	—	2.133	V/µs	
Output resistors (also used as high-speed terminating resistor)	Z_{HSDRV}	40.5	—	49.5	Ω	—

Note: The output resistors (ZHSDRV) for connection to the USB_DP and USB_DM pins are within the LSI.

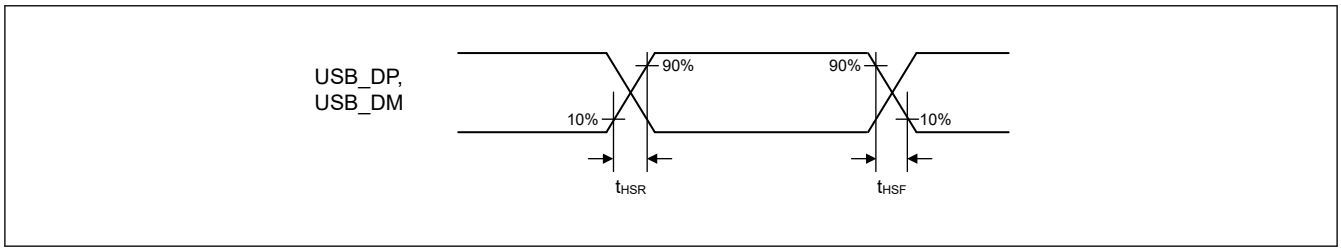


Figure 2.96 USB_DP, USB_DM output timing (high speed)

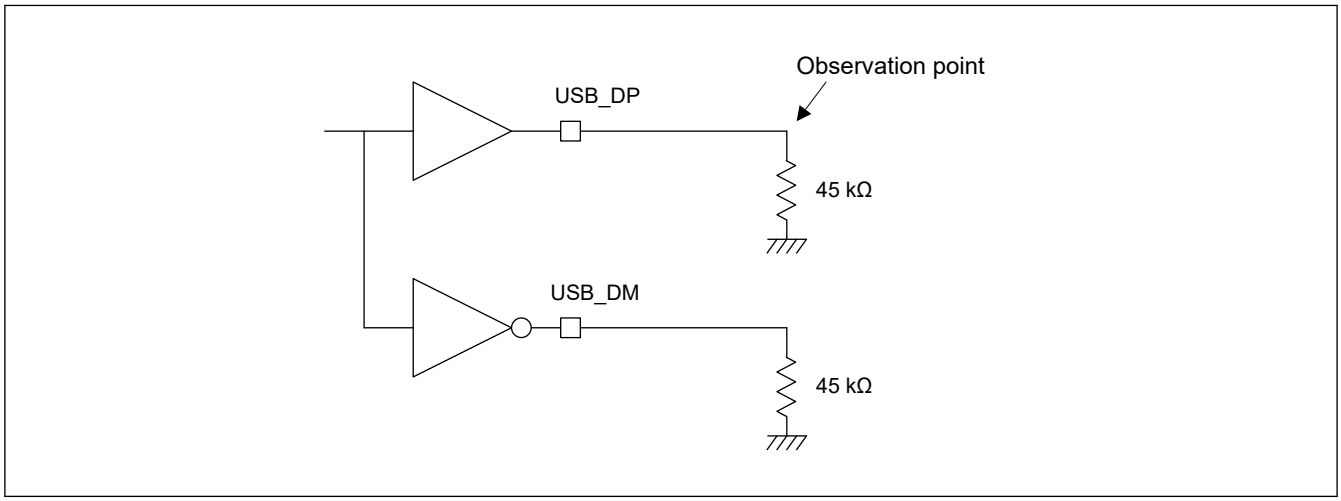


Figure 2.97 Measurement circuit (high speed)

2.7 A/D Conversion Characteristics

Table 2.50 12-Bit A/D conversion characteristics

Parameter			Min.	Typ.	Max.	Unit	Reference figure
Resolution			12			bits	—
Analog input capacitance		BGA package	—	—	13	pF	—
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002, AN100 to AN102, AN200 to AN202)	Conversion time*1 Permissible signal source impedance Max. = 1.0 kΩ		1.52	—	—	µs	—
	Offset error		—	—	±13	LSB	—
	Full-scale error		—	—	±13	LSB	—
	Quantization error		—	±0.5	—	LSB	—
	Absolute accuracy	BGA package	—	—	±14	LSB	—
	DNL differential non-linearity error	BGA package	—	—	±3	LSB	—
	INL integral non-linearity error	BGA package	—	—	±4	LSB	—
	Holding characteristics of sample-and-hold circuits		—	—	2.67	µs	—
	Dynamic range		0.15	—	VREFH0 - 0.15	V	—
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN003, AN100 to AN103, AN200 to AN207)	Conversion time*1 Permissible signal source impedance Max. = 1.0 kΩ		0.84	—	—	µs	—
	Offset error		—	—	±11	LSB	—
	Full-scale error		—	—	±11	LSB	—
	Quantization error		—	±0.5	—	LSB	—
	Absolute accuracy	BGA package	—	—	±12	LSB	—
	DNL differential non-linearity error	BGA package	—	—	±3	LSB	—
	INL integral non-linearity error	BGA package	—	—	±4	LSB	—

Note: The specified values in the table apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the specified ranges.

Note 1. The conversion time is the total of the sampling time and the comparison time.

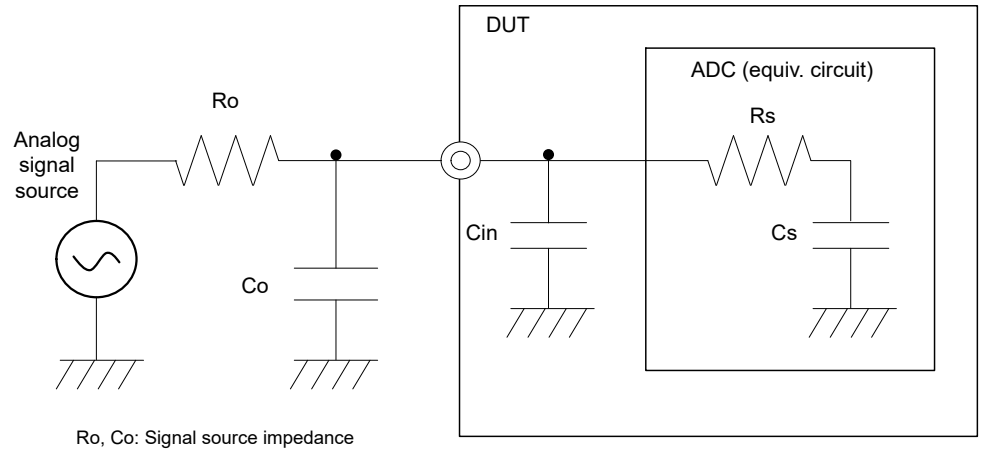


Figure 2.98 A/D converter equivalent circuit and peripheral configuration diagram

2.8 Temperature Sensor Characteristics

Table 2.51 Temperature sensor characteristics

Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	*1
Temperature slope	—	0.0625	—	°C/LSB	—
Output code (at 25°C)	—	1545 (decimal)	—	—	SCRR register

Note 1. 2-point calibration (Tj = 25°C and Tj = 85°C) and 8 times averaging.

2.9 PCI-Express Characteristics

The PCI Express PHY of this LSI is compliant with the PCI Express® Base Specification 2.1 (Gen1/Gen2).

Table 2.52 PCI Express REFCLK input characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input single-end termination impedance	$t_{RX-SINGLEEND}$	—	10	—	—	kΩ
Differential input peak-to-peak voltage	$t_{RXCLK-DPP}$	—	150	—	—	mV
Input common mode voltage	$t_{RXLLK-DC-CML}$	—	0.25	—	0.55	V
Absolute single-end input voltage	$t_{RXCLK-SE}$	—	-0.3	—	1.15	V

2.10 DDRSS (LPDDR4) Characteristics

The LPDDR4 PHY of this LSI is compliant with the JEDEC 209-4D standard.

Note: 240 (±1%) Ω external resistor must be connected between DDR_CALIBRATION and DDR_VDDQ.

2.11 Debug Interface Timing

Condition: V_{OH} = VCC33 × 0.5, V_{OL} = VCC33 × 0.5

Table 2.53 Debug interface timing

Parameter		Symbol	Min.	Max.	Unit	Reference figure
TCK cycle time	With an ICE connected	t_{TCKcyc}	30*1	—	ns	Figure 2.99
	For use in BSCAN		80	—		
TCK high pulse width		t_{TCKH}	0.4	0.6	t_{TCKcyc}	
TCK low pulse width		t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time		t_{TDIS}	5	—	ns	Figure 2.100 Output load: 30 pF
TDI hold time		t_{TDIH}	5	—	ns	
TMS/SWDIO setup time		t_{TMSS}	5	—	ns	
TMS/SWDIO hold time		t_{TMSH}	5	—	ns	
SWDIO delay time		t_{SWDO}	—	11	ns	
TDO delay time	With an ICE connected	t_{TDOD}	—	11	ns	
	For use in BSCAN		—	22		
Capture register setup time		t_{CAPTS}	5	—	ns	Figure 2.101
Capture register hold time		t_{CAPTH}	5	—	ns	
Update register delay time		$t_{UPDATED}$	—	15	ns	

Note 1. This value is the minimum cycle time for the normal operation of internal circuits.
The actual cycle time should be determined in consideration of the TCK capture edge timing and cable length of the connected ICE.

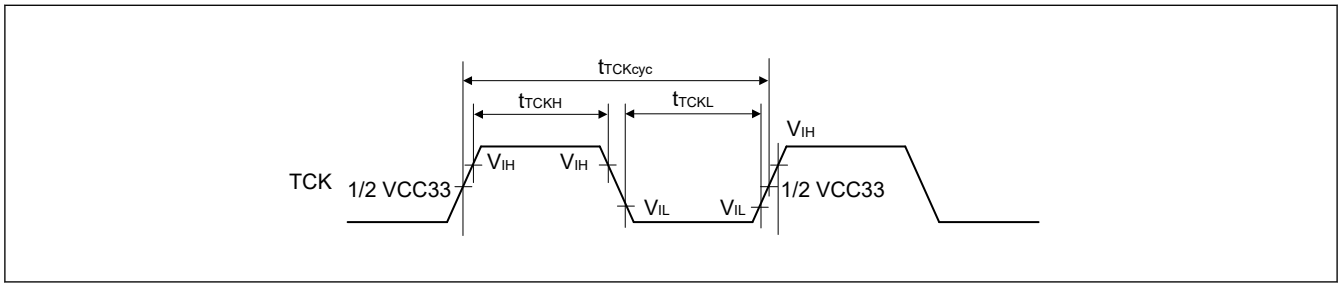


Figure 2.99 TCK input timing

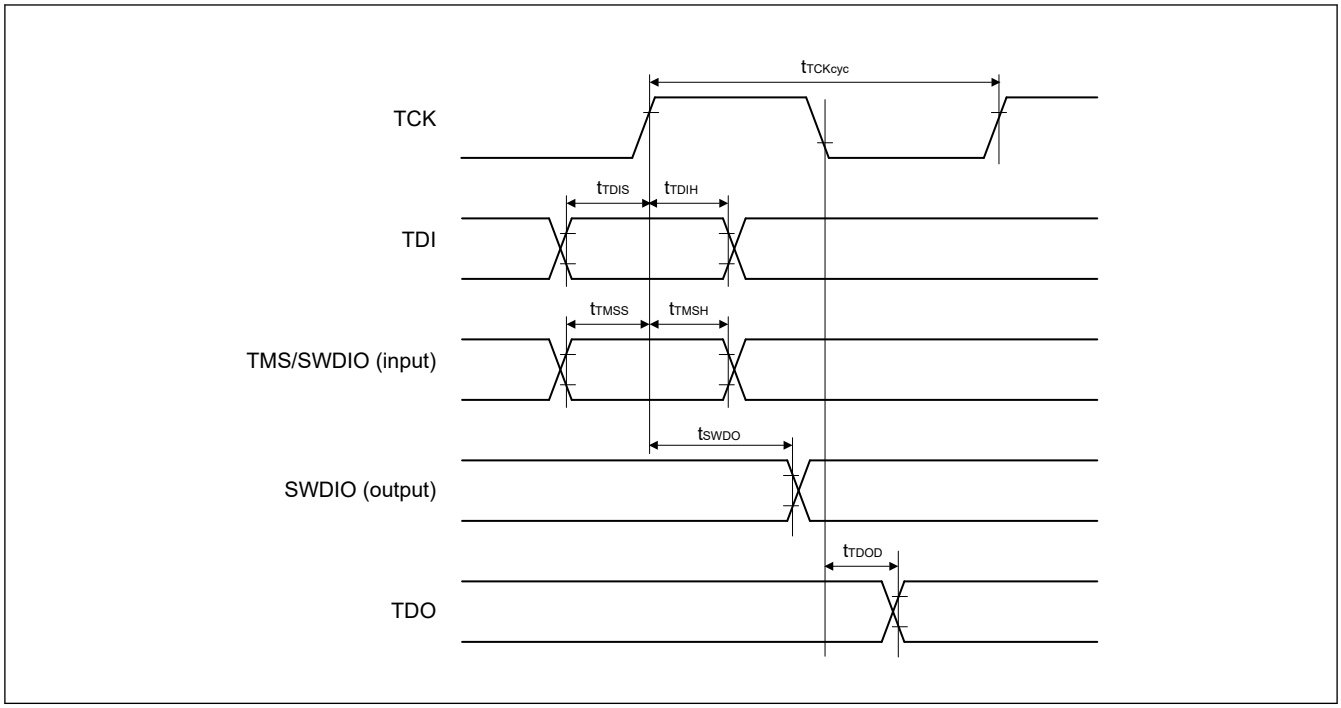


Figure 2.100 Data transfer timing

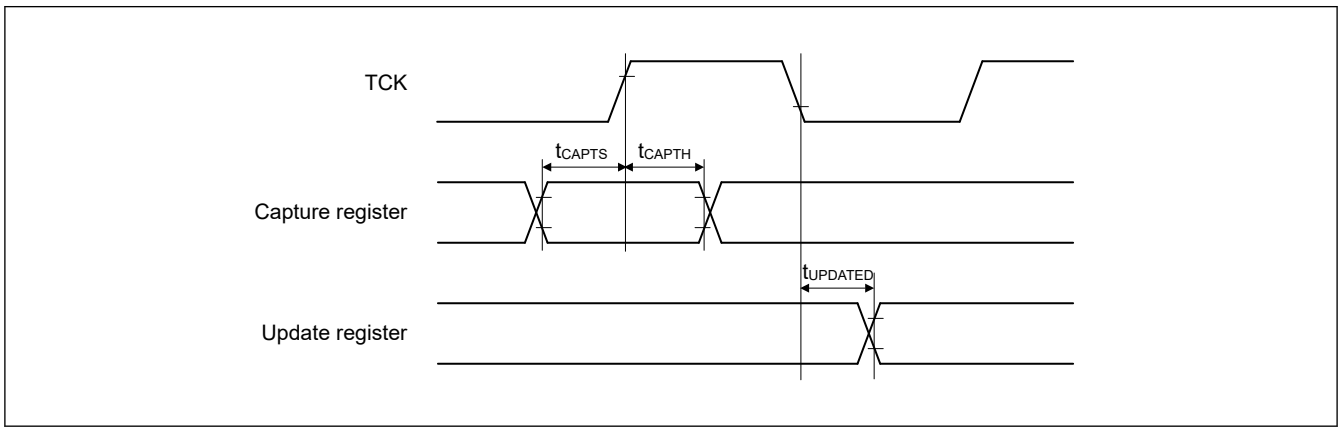
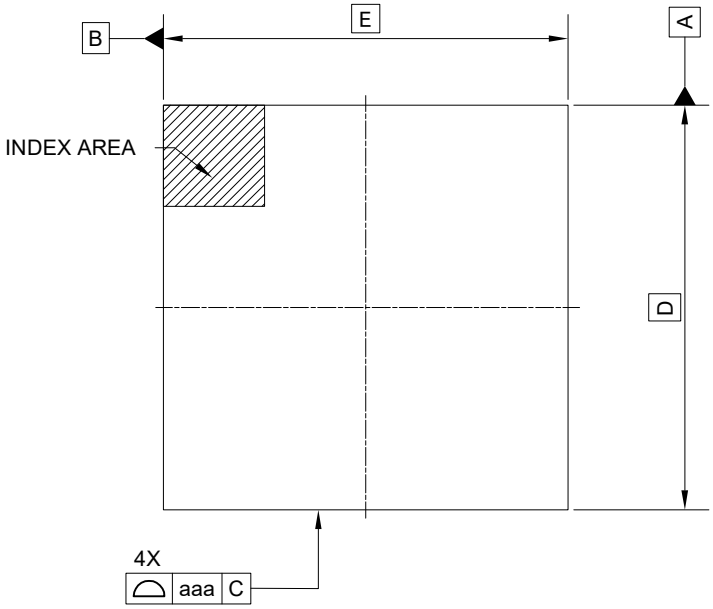


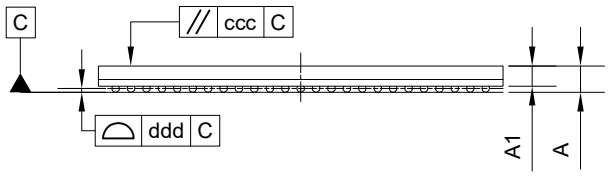
Figure 2.101 Boundary scan input/output timing

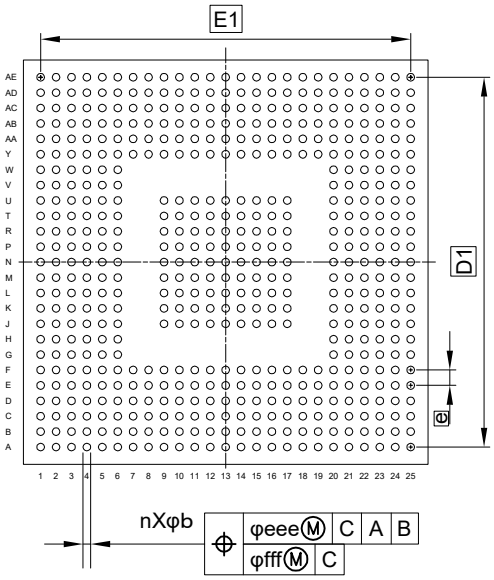
Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA537-21x21-0.80	PLBG0537GB-A	1.10



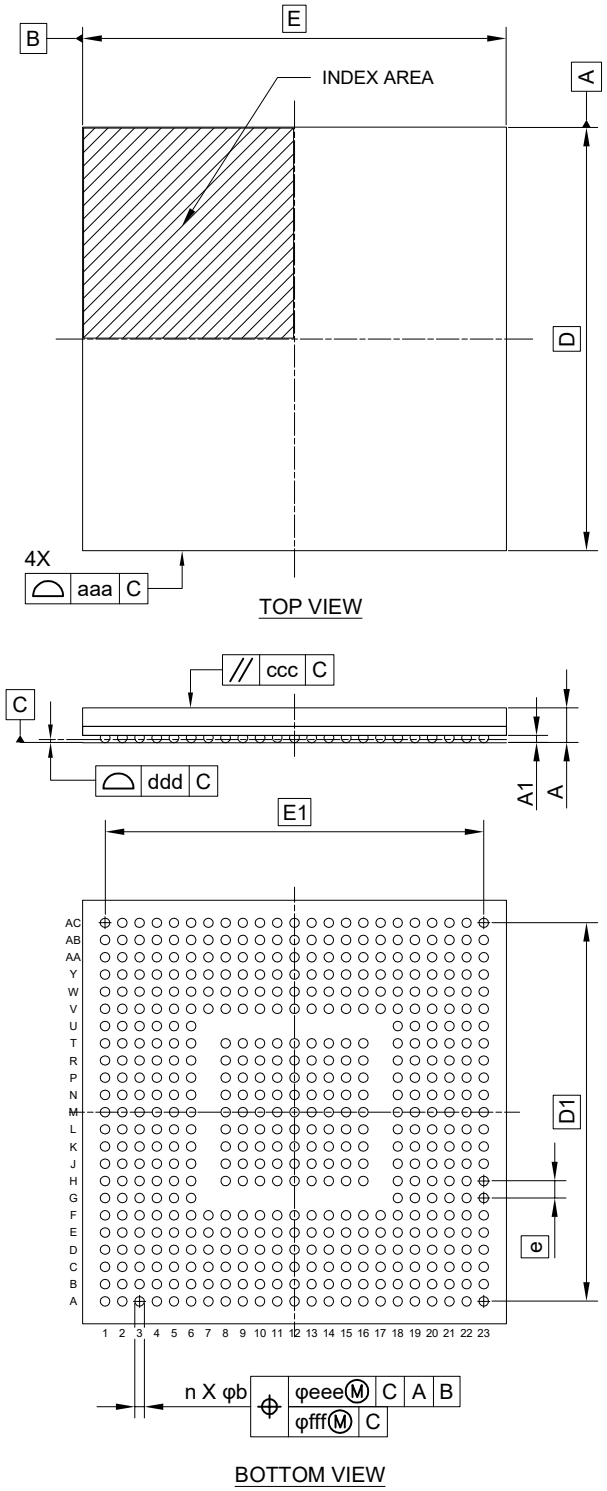




Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	21.00	—
E	—	21.00	—
D1	—	19.20	—
E1	—	19.20	—
A	—	—	1.45
A1	0.27	—	—
b	0.38	0.43	0.48
e	—	0.80	—
aaa	—	—	0.15
ccc	—	—	0.35
ddd	—	—	0.20
eee	—	—	0.15
fff	—	—	0.08
n	—	537	—

Figure A1.1 537-pin FBGA

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA489-16x16-0.65	PLBG0489JA-A	0.65



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	16.00	—
E	—	16.00	—
D1	—	14.30	—
E1	—	14.30	—
A	—	—	1.40
A1	0.22	—	—
b	0.32	0.37	0.42
e	—	0.65	—
aaa	—	—	0.15
ccc	—	—	0.20
ddd	—	—	0.15
eee	—	—	0.15
fff	—	—	0.08
n	—	489	—

Figure A1.2 489-pin FBGA

Appendix 2. ECAD Design Information

2.1 Part Number Indexing

Orderable part number	Number of pins	Package type	Package Code/POD number
R9A07G076M48GBG	537	FBGA	PLBG0537GB-A
R9A07G076M47GBG	537	FBGA	PLBG0537GB-A
R9A07G076M45GBG	537	FBGA	PLBG0537GB-A
R9A07G076M43GBG	537	FBGA	PLBG0537GB-A
R9A07G076M37GBG	537	FBGA	PLBG0537GB-A
R9A07G076M35GBG	537	FBGA	PLBG0537GB-A
R9A07G076M30GBG	537	FBGA	PLBG0537GB-A
R9A07G076M48GBA	489	FBGA	PLBG0489JA-A
R9A07G076M47GBA	489	FBGA	PLBG0489JA-A
R9A07G076M45GBA	489	FBGA	PLBG0489JA-A
R9A07G076M43GBA	489	FBGA	PLBG0489JA-A
R9A07G076M37GBA	489	FBGA	PLBG0489JA-A
R9A07G076M35GBA	489	FBGA	PLBG0489JA-A
R9A07G076M30GBA	489	FBGA	PLBG0489JA-A

2.2 Symbol Pin Information

2.2.1 537-FBGA

Pin number	Primary pin name	Primary electrical type	Alternate pin names
A1	VSS	Power	—
A2	P23_5	I/O	IRQ23_5/GTIOC4_2B/DE3/ETH2_TXEN/ESC_LEDERR/SPI_SSL02/MCLK30/MCLK42/ HDSL7_MOSI1
A3	P23_0	I/O	IRQ23_0/GTIOC3_3A/GTIOC4_0A/RXD3/SCL3/MISO3/ETH2_TXCLK/SPI_RSPCK0/MDAT01/ HDSL7_LINK
A4	VSS	Power	—
A5	P22_2	I/O	IRQ22_2/GTIOC0_3A/GTIOC4_5B/GTIOC5_0B/ETH1_RXD2/HDSL6_MISO1
A6	P21_6	I/O	IRQ21_6/ETH1_TXEN/HDSL6_LINK
A7	VSS	Power	—
A8	P21_4	I/O	IRQ21_4/ETH1_TXD2/HDSL5_MISO2
A9	P20_4	I/O	MD0/IRQ20_4/GMAC0_MDC/GMAC1_MDC/GMAC2_MDC/ETHSW_MDC/ESC_MDC/ ESWM_MDC/CANTX1
A10	P20_1	I/O	IRQ20_1/ETH0_RXD2/CANRXDP0/HDSL4_MISO2
A11	VSS	Power	—
A12	P19_5	I/O	IRQ19_5/ETH0_TXEN/HDSL4_MISO1
A13	VSS	Power	—
A14	P18_4	I/O	IRQ18_4/GTETRGA/DEE4/ESWM_TASGATE1_5/XSPI0_IO5/MDAT21/ENCIFOE4/ HDSL3_MOSI1
A15	P18_1	I/O	IRQ18_1/ESWM_TASGATE1_2/XSPI0_IO2/MCLK32/HDSL3_CLK1
A16	P17_6	I/O	IRQ17_6/ESWM_TASGATE0_8/XSPI0_DS/MCLK20/HDSL2_MOSI2

Pin number	Primary pin name	Primary electrical type	Alternate pin names
A17	VSS	Power	—
A18	P17_1	I/O	IRQ17_1/MTIOC0B/MTIOC6C/GTIOC4_4B/RXDE3/IIC_SDA1/ETH2_COL/ETH3_COL/ CANTX0/XSPI1_IO7/MDAT31/MBX_HINT#/ENCIFDI3/HDSL2_MISO1
A19	P16_4	I/O	IRQ16_4/MTIOC7B/GTIOC3_2A/GTIOC4_2A/RXD4/SCL3/MISO3/SCKE7/ETH4_CRS, SPI_MISO0/XSPI1_IO2/MCLK01/ENCIFCK7/HDSL1_MOSI2
A20	P16_1	I/O	IRQ16_1/MTIOC6D/GTIOC3_0B/GTIOC4_0B/TXD1/SDA1/MOSI1/RXDE1/IIC_SDA2/ ESWM_TASGATE0_3/XSPI1_DS/MDAT22/ENCIFDI1/HDSL1_CLK2
A21	VSS	Power	—
A22	P15_3	I/O	IRQ15_3/D10/MTIOC1A/MTIOC3C/GTIOC2_4B/CMTW1_TOC0/RXDE2/SD1_IOVS/ADTRG0#/ HD10/ENCIFDI2/HDSL1_LINK
A23	P14_6	I/O	IRQ14_6/D5/MTIOC1B/MTIOC4B/GTIOC2_2A/CMTW0_TIC0/SD0_PWEN/HD5/ HDSL0_MOSI1/POUTA
A24	P14_3	I/O	IRQ14_3/D2/POE0#/GTIOC0_2A/GTETRGA/RTCAT1HZ/SCIEXTCLK/ADTRG0#/ USB_EXICEN/HD2/MBX_HINT#/HDSL0_CLK1
A25	VSS	Power	—
B1	P24_3	I/O	IRQ24_3/GTIOC4_5B/CMTW0_TIC1/RXD5/SDA5/MOSI5/IIC_SCL1/ETH0_RXER/ ETH2_RXDV/ESC_I2CCLK/SPI_MOSI1/SD0_PWEN/MDAT12/HDSL0_LINK
B2	P23_6	I/O	IRQ23_6/GTIOC4_3A/GTIOC5_3A/RTCAT1HZ/SCK4/ETH2_RXCLK/ESC_LEDRUN/SD0_CD/ MDAT30/MDAT42/HDSL7_CLK2
B3	P23_2	I/O	IRQ23_2/GTIOC4_1A/IIC_SDA0/ETH2_TXD1/ESC_LINKACT0/CANTXDP1/SPI_MOSI0/ MDAT21/MDAT40/HDSL7_CLK1
B4	P22_4	I/O	IRQ22_4/GTIOC0_2B/ETH1_RXDV/HDSL6_CLK2
B5	P22_6	I/O	ETH1_REFCLK/RMII1_REFCLK/IRQ22_6/HDSL6_MISO2
B6	P21_5	I/O	IRQ21_5/ETH1_TXD3/HDSL5_MOSI2
B7	P21_7	I/O	IRQ21_7/GTIOC4_4A/ETH1_RXCLK/HDSL6_SMPL
B8	P21_1	I/O	IRQ21_1/ETH1_TXCLK/HDSL5_MOSI1
B9	P20_6	I/O	IRQ20_6/ETHSW_PHYLINK0/ESC_PHYLINK0/ESWM_PHYLINK0/HPSW_PHYLINK0/ CANRXDP1/HDSL5_CLK1
B10	P20_7	I/O	ETH0_REFCLK/RMII0_REFCLK/IRQ20_7/CANTXDP1/HDSL5_SEL1
B11	P19_6	I/O	IRQ19_6/ETH0_RXCLK/HDSL4_MOSI1
B12	P19_2	I/O	IRQ19_2/ETH0_TXD1/HDSL4_SMPL
B13	P19_0	I/O	IRQ19_0/ETH0_TXCLK/HDSL3_MOSI2
B14	P18_5	I/O	IRQ18_5/GTETRGB/RXDE4/ESWM_TASGATE1_6/XSPI0_IO6/MCLK20/ENCIFDI4/ HDSL3_CLK2
B15	P18_0	I/O	IRQ18_0/ESWM_TASGATE1_1/XSPI0_IO1/MCLK02/HDSL3_SMPL
B16	P17_3	I/O	IRQ17_3/DEE7/ESWM_TASGATE0_5/XSPI0_CKN/MDAT30/ENCIFOE7/HDSL2_CLK2
B17	P17_2	I/O	IRQ17_2/SCKE7/ESWM_TASGATE0_4/XSPI0_CKP/MCLK30/ENCIFCK7/HDSL2_MOSI1
B18	P16_6	I/O	IRQ16_6/MTCLKC/MTIOC0C/GTIOC3_3A/SCKE3/IIC_SCL0/ETH2_TXER/ETH3_TXER/ CANRXDP0/SPI_RSPCK0/XSPI1_IO4/MCLK30/ENCIFCK3/HDSL2_SMPL
B19	P16_3	I/O	IRQ16_3/MTIOC7C/GTIOC3_1A/GTIOC4_1B/TXD5/SDA5/MOSI5/TXDE4/ETH4_RXER/ SPI_SSL02/XSPI1_IO1/ENCIFDO4/HDSL1_MISO2
B20	P16_0	I/O	IRQ16_0/MTIOC1B/MTIOC6B/GTIOC3_0A/GTIOC4_0A/RXD1/SCL1/MISO1/TXDE1/IIC_SCL2/ ESWM_TASGATE0_2/XSPI1_CS1#/MCLK22/ENCIFDO1/HDSL1_MOSI1
B21	P15_6	I/O	IRQ15_6/GTIOC0_4A/DE1/TXDE6/TXDE7/IIC_SCL1/ESWM_TASGATE0_0/XSPI1_CKP/ MCLK21/ENCIFDO6/ENCIFDO7/HDSL1_SEL1
B22	P15_1	I/O	IRQ15_1/D8/MTCLKB/MTIOC8D/GTIOC2_3B/CMTW0_TOC1/DEE2/SD1_WP/HD8/ENCIFOE2/ HDSL0_MISO2

Pin number	Primary pin name	Primary electrical type	Alternate pin names
B23	P14_7	I/O	IRQ14_7/D6/MTIOC1A/MTIOC4D/GTIOC2_2B/CMTW0_TOC0/SD0_IOVS/HD6/HDSL0_CLK2/ POUTB
B24	P14_1	I/O	IRQ14_1/D0/MTIOC3B/MTIOC8A/GTIOC0_0A/GTIOC2_0A/GTIOC4_6A/SCKE6/ETH2_TXER/ ETH3_TXER/USB_VBUSEN/HD0/ENCIFCK6/HDSL0_LINK
B25	P13_4	I/O	IRQ13_4/D23/GTADSM3_1/RTCAT1HZ/ETH1_COL/GMAC0_MDIO/GMAC1_MDIO/ GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO/ESWM_MDIO/SD1_IOVS/MDAT42/HD23/ HDSL7_MOSI1
C1	P25_0	I/O	IRQ25_0/RXD1/SCL1/MISO1/RXD3/SCL3/MISO3/ETHSW_PHYLINK2/ESC_PHYLINK2/ CANTX1/SPI_SSL03/MCLK22
C2	P24_2	I/O	IRQ24_2/TEND/POE8#/GTIOC4_5A/CMTW0_TOC0/CTS4#/RXDE0/ETH2_RXD3/ ESC_RESETOUT#/SPI_SSL11/MDAT11/ENCIFDI0/HDSL7_MOSI2
C3	P24_0	I/O	IRQ24_0/DREQ/POE0#/GTIOC4_4A/DEE0/IIC_SDA1/ETH0_CRS/ETH2_RXD1/ ESC_LINKACT2/SPI_SSL13/SD1_CD/MDAT10/MDAT32/ENCIFOE0/HDSL7_MISO2
C4	P23_3	I/O	IRQ23_3/GTIOC4_1B/GTIOC4_3A/SS3#/CTS3#/RTS3#/ETH2_TXD2/ESC_LINKACT1/ SPI_SSL00/MCLK01/MCLK41/HDSL7_SEL1
C5	P23_1	I/O	IRQ23_1/GTIOC3_3B/GTIOC4_0B/SCK3/IIC_SCL0/ETH2_TXD0/GMAC0_PTPTRG0/ ESC_LATCH0/CANRXDP1/SPI_MISO0/MCLK21/MCLK40/HDSL7_SMPL
C6	P22_0	I/O	IRQ22_0/GTIOC4_4B/ETH1_RXD0/HDSL6_CLK1
C7	P20_5	I/O	IRQ20_5/GMAC0_MDIO/GMAC1_MDIO/GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO/ ESWM_MDIO/CANRX1/HDSL5_SMPL
C8	P21_3	I/O	IRQ21_3/ETH1_TXD1/HDSL5_SEL2
C9	P21_0	I/O	IRQ21_0/HDSL5_MISO1
C10	P20_2	I/O	IRQ20_2/ETH0_RXD3/CANTXDP0/HDSL4_MOSI2
C11	P20_0	I/O	IRQ20_0/ETH0_RXD1/CANTX0/HDSL4_SEL2
C12	P19_3	I/O	IRQ19_3/ETH0_TXD2/HDSL4_CLK1
C13	P18_7	I/O	IRQ18_7/ESWM_TASGATE1_8/XSPI0_RESET0#/MCLK30/MDAT02/HDSL3_MISO2
C14	P18_2	I/O	IRQ18_2/ESWM_TASGATE1_3/XSPI0_IO3/MDAT32/HDSL3_SEL1
C15	P17_7	I/O	IRQ17_7/ESWM_TASGATE1_0/XSPI0_IO0/MDAT20/HDSL3_LINK
C16	P17_5	I/O	IRQ17_5/RXDE7/ESWM_TASGATE0_7/XSPI0_CS1#/MDAT31/ENCIFDI7/HDSL2_MISO2
C17	P17_0	I/O	IRQ17_0/MTIOC0A/MTIOC6A/GTIOC3_4A/TXDE3/IIC_SCL1/ETH2_CRS/ETH3_CRS/ CANRX0/XSPI1_IO6/MCLK31/USB_VBUSEN/ENCIFDO3/HDSL2_SEL1
C18	P16_5	I/O	IRQ16_5/MTIOC7D/GTIOC3_2B/GTIOC4_2B/TXD3/SDA3/MOSI3/DEE7/ETH4_COL/ SPI_MOSI0/XSPI1_IO3/MDAT01/ENCIFOE7/HDSL2_LINK
C19	P15_7	I/O	IRQ15_7/GTIOC0_4B/DE3/RXDE6/RXDE7/IIC_SDA1/ESWM_TASGATE0_1/XSPI1_CS0#/ MDAT21/ENCIFDI6/ENCIFDI7/HDSL1_MISO1
C20	P15_2	I/O	IRQ15_2/D9/MTIOC3A/MTIC5W/GTIOC2_4A/CMTW1_TIC0/TXDE2/SD1_PWEN/HD9/ ENCIFDO2/HDSL0_MOSI2
C21	P15_4	I/O	IRQ15_4/D11/GTIOC2_0A/CMTW1_TIC1/SCKE6/IIC_SCL0/ESC_I2CCLK/MCLK20/ADTRG1#/ HD11/ENCIFCK6/HDSL1_SMPL
C22	P14_4	I/O	IRQ14_4/D3/MTIOC4A/MTIC5U/GTIOC0_1B/GTIOC2_1A/TXDE6/ETH2_CRS/ETH3_CRS/ ADTRG1#/HD3/ENCIFDO6/HDSL0_SEL1
C23	P14_2	I/O	IRQ14_2/D1/MTIOC3D/MTIOC8B/GTIOC0_0B/GTIOC2_0B/GTIOC4_6B/DEE6/ETH2_RXER/ ETH3_RXER/USB_OVRCUR/HD1/ENCIFOE6/HDSL0_SMPL
C24	P13_3	I/O	IRQ13_3/D22/GTADSM3_0/ETH1_CRS/GMAC0_MDC/GMAC1_MDC/GAMC2_MDC/ ETHSW_MDC/ESC_MDC/ESWM_MDC/SD1_PWEN/MCLK42/HD22/HDSL7_MISO1
C25	P13_2	I/O	IRQ13_2/D21/GTADSM2_1/ESC_EDERR/SD1_IOVS/MDAT10/HD21/HDSL7_SEL1
D1	VSS	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
D2	P24_7	I/O	IRQ24_7/TXD3/SDA3/MOSI3/GMAC0_MDIO/GMAC1_MDIO/GMAC2_MDIO/ETHSW_MDIO/ ESC_MDIO/ESWM_MDIO/CANRX1/SPI_RSPCK1
D3	P24_6	I/O	MD1/IRQ24_6/DE5/GMAC0_MDC/GMAC1_MDC/GMAC2_MDC/ETHSW_MDC/ESC_MDC/ ESWM_MDC
D4	P24_1	I/O	IRQ24_1/DACK/POE4#/GTIOC4_4B/CMTW0_TIC0/SS4#/CTS4#/RTS4#/TXDE0/ETH0_TXER/ ETH2_RXD2/ESC_IRQ/ SPI_SSL10/SD1_WP/MCLK11/MBX_HINT#/ENCIFDO0
D5	P23_4	I/O	IRQ23_4/GTIOC4_2A/GTIOC4_3B/CTS3#/ETH2_TXD3/ETHSW_PTPOUT2/ESC_SYNC0/ SPI_SSL01/MDAT01/MDAT41/HDSL7_MISO1
D6	P22_3	I/O	IRQ22_3/GTIOC0_3B/ETH1_RXD3/HDSL6_MOSI1
D7	P22_1	I/O	IRQ22_1/GTIOC4_5A/GTIOC5_0A/ETH1_RXD1/HDSL6_SEL1
D8	P21_2	I/O	IRQ21_2/ETH1_TXD0/HDSL5_CLK2
D9	P22_5	I/O	IRQ22_5/ETHSW_PHYLINK1/ESC_PHYLINK1/ESWM_PHYLINK1/HPSW_PHYLINK1/ HDSL6_SEL2
D10	P20_3	I/O	IRQ20_3/ETH0_RXDV/HDSL5_LINK
D11	P19_7	I/O	IRQ19_7/ETH0_RXD0/CANRX0/HDSL4_CLK2
D12	P19_4	I/O	IRQ19_4/ETH0_TXD3/HDSL4_SEL1
D13	P19_1	I/O	IRQ19_1/ETH0_TXD0/HDSL4_LINK
D14	P18_6	I/O	IRQ18_6/GTETRGC/TXDE4/ESWM_TASGATE1_7/XSPI0_IO7/MDAT20/ENCIFDO4/ HDSL3_SEL2
D15	P18_3	I/O	IRQ18_3/SCKE4/ESWM_TASGATE1_4/XSPI0_IO4/MCLK21/ENCIFCK4/HDSL3_MISO1
D16	P17_4	I/O	IRQ17_4/TXDE7/ESWM_TASGATE0_6/XSPI0_CS0#/MCLK31/ENCIFDO7/HDSL2_SEL2
D17	P16_7	I/O	IRQ16_7/MTCLKD/MTIOC0D/GTIOC3_3B/DEE3/IIC_SDA0/ETH2_RXER/ETH3_RXER/ CANTXDP0/SPI_SSL00/XSPI1_IO5/MDAT30/ENCIFOE3/HDSL2_CLK1
D18	P16_2	I/O	IRQ16_2/MTIOC7A/GTIOC3_1B/GTIOC4_1A/RXD5/SCL5/MISO5/RXDE4/ETH4_TXER/ SPI_SSL01/XSPI1_IO0/ENCIFDI4/HDSL1_SEL2
D19	P15_5	I/O	IRQ15_5/D12/GTIOC2_0B/CMTW1_TOC1/RTCAT1HZ/DEE6/IIC_SDA0/ESC_I2CDATA/ MDAT20/ADTRG2#/HD12/ENCIFDO6/HDSL1_CLK1
D20	P14_5	I/O	IRQ14_5/D4/MTIOC4C/MTIC5V/GTIOC0_1A/GTIOC2_1B/RXDE6/ETH2_COL/ETH3_COL/ ADTRG2#/HD4/ENCIFDI6/HDSL0_MISO1
D21	P15_0	I/O	IRQ15_0/D7/MTCLKA/MTIOC8C/GTIOC2_3A/CMTW0_TIC1/SCKE2/SD1_CD/HD7/ENCIFCK2/ HDSL0_SEL2/POUTZ
D22	P13_5	I/O	IRQ13_5/D24/GTADSM4_0/SCKE7/ESC_LEDSTER/MCLK11/HD24/ENCIFCK7/HDSL7_CLK2
D23	P13_1	I/O	IRQ13_1/D20/TEND/GTADSM2_0/ESC_LEDRUN/SD1_PWEN/MCLK10/HD20/HDSL7_CLK1
D24	P13_0	I/O	IRQ13_0/D19/GTADSM1_1/CMTW1_TOC1/ETHSW_PTPOUT1/ESC_SYNC1/MDAT41/HD19/ HDSL7_SMPL
D25	P12_6	I/O	IRQ12_6/D17/DACK/GTADSM0_1/GTETRGC/CMTW1_TOC0/MDAT40/HD17/HDSL6_MOSI2
E1	P00_0	I/O	IRQ00_0/A16/MTIOC3B/GTIOC0_0A/GTADSM0_0/SCKE1/ETH3_TXCLK/SPI_RSPCK2/HA16/ ENCIFCK1/HDSL0_SEL1
E2	P00_6	I/O	IRQ00_6/A22/MTCLKA/MTIOC8D/GTIOC0_3A/GTADSM3_0/RXD4/SCL4/MISO4/SCKE0/ SCKE6/ETH3_RXCLK/SPI_SSL23/MBX_HINT#/ENCIFCK0/ENCIFCK6
E3	P24_5	I/O	IRQ24_5/POE10#/GTIOC4_6B/GTETRGA/TXD4/SDA4/MOSI4/SCIEXTCLK/MDAT22/ PCIE_RSTOUTB/HDSL0_CLK1
E4	P00_1	I/O	IRQ00_1/A17/MTIOC3D/GTIOC0_0B/GTADSM0_1/DEE1/IIC_SCL2/ETH3_TXD0/CANRX0/ SPI_MISO2/HA17/ENCIFOE1/HDSL0_MISO1
E5	P23_7	I/O	IRQ23_7/GTIOC4_3B/GTIOC5_3B/SCKE0/IIC_SCL1/ETH0_COL/ETH2_RXD0/SPI_SSL12/ SD0_WP/MCLK10/MCLK32/ENCIFCK0/HDSL7_SEL2
E6	P22_7	I/O	IRQ22_7/HDSL6_MOSI2
E7	VCC1833_1	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
E8	VSS	Power	—
E9	VCC1833_0	Power	—
E10	VSS	Power	—
E11	VCC1833_0	Power	—
E12	VSS	Power	—
E13	VCC1833_3	Power	—
E14	VSS	Power	—
E15	VSS	Power	—
E16	VCC1833_4	Power	—
E17	VSS	Power	—
E18	VCC33	Power	—
E19	VSS	Power	—
E20	P13_7	I/O	IRQ13_7/D26/TXDE7/MCLK12/HD26/ENCIFDO7/HDSL7_MISO2
E21	P14_0	I/O	IRQ14_0/D27/RXDE7/ETHSW_PTPOUT3/ESC_SYNC1/MDAT12/HD27/ENCIFDI7/ HDSL7_MOSI2
E22	P12_7	I/O	IRQ12_7/D18/GTADSM1_0/GTETRGD/CMTW1_TIC1/ETHSW_PTPOUT0/ESC_SYNC0/ MCLK41/HD18/HDSL7_LINK
E23	P13_6	I/O	IRQ13_6/D25/GTADSM4_1/DEE7/MDAT11/HD25/ENCIFOE7/HDSL7_SEL2
E24	P12_5	I/O	IRQ12_5/D16/DREQ/GTADSM0_0/GTETRGB/CMTW1_TIC0/MCLK40/HD16/HDSL6_MISO2
E25	VSS	Power	—
F1	P00_3	I/O	IRQ00_3/A19/MTIOC4C/GTIOC0_1A/GTADSM1_1/RXDE1/ETH3_TXD2/CANRXDP0/ SPI_SSL20/MDAT41/HA19/ENCIFDI1/HDSL0_CLK2
F2	P00_5	I/O	IRQ00_5/A21/MTIOC4D/MTIOC8C/GTIOC0_2B/GTADSM2_1/RXDE6/ETH3_TXEN/ SPI_SSL22/MDAT20/HA21/ENCIFDI6/HDSL0_MISO2
F3	P00_2	I/O	IRQ00_2/A18/MTIOC4A/GTIOC0_1B/GTADSM1_0/TXDE1/IIC_SDA2/ETH3_TXD1/CANTX0/ SPI_MOSI2/MCLK41/HA18/ENCIFDO1/HDSL0_MOSI1
F4	P00_4	I/O	IRQ00_4/A20/MITOC4B/GTIOC0_2A/GTADSM2_0/TXDE6/ETH3_TXD3/CANTXDP0/ SPI_SSL21/MCLK20/HA20/ENCIFDO6/HDSL0_SEL2
F5	P24_4	I/O	ETH2_REFCLK/RMII2_REFCLK/IRQ24_4/POE11#/GTIOC4_6A/CMTW0_TOC1/RXD5/SCL5/ MISO5/IIC_SDA1/ETH1_RXER/ESC_I2CDATA/SPI_MISO1/SD0_IOVS/MCLK12/HDSL0_SMPL
F6	VSS	Power	—
F7	VCC1833_1	Power	—
F8	VSS	Power	—
F9	VCC1833_0	Power	—
F10	VSS	Power	—
F11	VCC1833_0	Power	—
F12	VSS	Power	—
F13	VCC1833_3	Power	—
F14	VSS	Power	—
F15	VCC18_PLL1	Power	—
F16	VCC1833_4	Power	—
F17	VSS	Power	—
F18	VCC33	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
F19	VSS	Power	—
F20	VCC33	Power	—
F21	VSS	Power	—
F22	VSS	Power	—
F23	VSS	Power	—
F24	VSS	Power	—
F25	VSS	Power	—
G1	VSS	Power	—
G2	P01_4	I/O	ETH3_REFCLK/RMII3_REFCLK/IRQ01_4/CS5#/TEND/TXD1/SDA1/MOSI1/RXDE4/IIC_SDA1/ ETH1_RXER/ETH1_CRS/ESC_I2CDATA/SPI_RSPCK2/MCLK01/USB_EXICEN/ADTRG2#/ ENCIFDI4
G3	P01_5	I/O	IRQ01_5/CS2#/DREQ/TXDE4/ETH1_COL/ETH3_TXER/ESC_RESETOUT#/ ESWM_PHYLINK0/HPSW_PHYLINK0/SPI_SSL20/MDAT01/USB_EXICEN/HCS1#/ENCIFDO4
G4	P01_2	I/O	IRQ01_2/BS#/DREQ/SS5#/CTS5#/RST5#/TXD5/SDA5/MOSI5/SCKE4/ETH3_RXD3/ SPI_MOSI2/SD1_IOVS/MCLK00/ADTRG0#/HBS#/ENCIFCK4
G5	P00_7	I/O	IRQ00_7/A23/MTCLKB/MTIOC1B/GTIOC0_3B/GTADSM3_1/TXD4/SDA4/MOSI4/DEE0/DEE6/ ETH3_RXD0/SPI_SSL22/HERROUT#/ENCIFOE0/ENCIFOE6
G6	VSS	Power	—
G7	—	—	—
G8	—	—	—
G9	—	—	—
G10	—	—	—
G11	—	—	—
G12	—	—	—
G13	—	—	—
G14	—	—	—
G15	—	—	—
G16	—	—	—
G17	—	—	—
G18	—	—	—
G19	—	—	—
G20	DDR_VDDQ	Power	—
G21	VSS	Power	—
G22	VSS	Power	—
G23	VSS	Power	—
G24	VSS	Power	—
G25	VSS	Power	—
H1	P01_6	I/O	IRQ01_6/D13/MTIOC6B/MTIOC8B/GTIOC1_0A/GTADSM0_0/GTETRGB/CMTW1_TIC0/SCK1/ ETH0_RXER/ETH4_TXCLK/SPI_RSPCK3/SD1_CD/MCLK02/HD13/—
H2	P01_1	I/O	IRQ01_1/RD/WR#/MITOC3C/MTIOC8A/GTIOC0_4B/GTADSM4_1/SCK5/RXD5/SCL5/ MISO5/ RXDE0/ETH3_RXD2/SD1_PWEN/USB_OVRCUR/HWRSTB#/ENCIFDI0
H3	P01_3	I/O	IRQ01_3/CS3#/DACK/CTS5#/RXD1/ SCL1/MISO1/ DEE4/IIC_SCL1/ETH1_TXER/ ETH3_RXDV/ESC_I2CCLK/SPI_MISO2/MDAT00/ADTRG1#/MBX_HINT#/ENCIFOE4

Pin number	Primary pin name	Primary electrical type	Alternate pin names
H4	P01_0	I/O	IRQ01_0/A0/MTIOC1A/MTIOC3A/GTIOC0_4A/GTADSM4_0_/DE4/TXDE0/ETH3_RXD1/ SPI_SSL21/HA0/ENCIFDO0
H5	VSS	Power	—
H6	VSS	Power	—
H7	—	—	—
H8	—	—	—
H9	—	—	—
H10	—	—	—
H11	—	—	—
H12	—	—	—
H13	—	—	—
H14	—	—	—
H15	—	—	—
H16	—	—	—
H17	—	—	—
H18	—	—	—
H19	—	—	—
H20	DDR_VDDQ	Power	—
H21	VSS	Power	—
H22	DDR_DQA15	I/O	—
H23	DDR_DQA8	I/O	—
H24	VSS	Power	—
H25	DDR_DQA14	I/O	—
J1	P02_5	I/O	IRQ02_5/A11/MTCLKD/MTIOC0D/GTIOC1_3B/GTADSM3_1/RXD2/SCL2/MISO2/DEE1/ ETH4_RXD0/GMAC2_PTPTRG1/SPI_SSL32/MDAT12/ MDAT40/HA11/ENCIFOE1
J2	P02_1	I/O	IRQ02_1/WE3#/A H#/MTIC5W/MTIOC7C/GTIOC1_1A/GTADSM1_1/SS1#/ CTS1#/RTS1#/RXD3/SCL3/MISO3/TXDE5/ETH4_TXD2/GMAC0_PTPTRG0/ESC_LATCH0/ SPI_SSL30/SPI_SSL00/HWR3#/ENCIFDO5
J3	P02_0	I/O	IRQ02_0/WE2#/MTIC5V/MTIOC7A/GTIOC1_1B/GTADSM1_0/GTETRGD/TXD1/SDA1/MOSI1/ SCIEXTCLK/ETH4_TXD1/ETHSW_PTPOUT0/ESC_SYNC0/SPI_MOSI3/SD1_PWEN/HWR2#
J4	P01_7	I/O	IRQ01_7/D14/MTIC5U/MTIOC6D/GTIOC1_0B/GTADSM0_1/GTETRGC/CMTW1_TOC0/RXD1/ SCL1/MISO1/ETH1_RXER/ETH4_TXD0/SPI_MISO3/SD1_WP/MDAT02/HD14
J5	VCC1833_2	Power	—
J6	VCC1833_2	Power	—
J7	—	—	—
J8	—	—	—
J9	VDD	Power	—
J10	VSS	Power	—
J11	VSS	Power	—
J12	VDD	Power	—
J13	VDD	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
J14	VSS	Power	—
J15	VSS	Power	—
J16	VDD	Power	—
J17	VDD	Power	—
J18	—	—	—
J19	—	—	—
J20	VSS	Power	—
J21	DDR_DQA12	I/O	—
J22	DDR_DQA11	I/O	—
J23	VSS	Power	—
J24	DDR_DQSA_T1	I/O	—
J25	DDR_DQSA_C1	I/O	—
K1	VSS	Power	—
K2	P02_4	I/O	IRQ02_4/A10/MTCLKC/MTIOC0C/GTIOC1_3A/GTADSM3_0/SCK2/ SCKE1/ETH4_RXCLK/ GMAC1_PTPTRG1/SPI_SSL03/SPI_SSL33/MCLK12/MCLK40/HA10/ENCIFCK1
K3	P03_1	I/O	IRQ03_1/A15/GTIOC3_3B/DE2/DEE5/IIC_SDA2/ETH0_CRS/ETH4_RXDV/ETHSW_PTPOUT3/ ESC_SYNC1/SPI_MISO3/MDAT10/HA15/ENCIFOE5/SI3#/HDSL1_LINK
K4	P02_2	I/O	IRQ02_2/D15/MTIOC0A/MTIOC7B/GTIOC1_2A/GTADSM2_0/CTS1#/ETH4_TXD3/ GMAC0_PTPTRG1/ESC_LEDRUN/ESC_LATCH1/SPI_SSL01/SPI_SSL31/SD1_PWEN/HD15
K5	P02_3	I/O	IRQ02_3/A9/MTIOC0B/MTIOC7D/GTIOC1_2B/GTADSM2_1/DE1/ETH4_TXEN/ GMAC1_PTPTRG0/ESC_LEDERR/SPI_SSL02/SPI_SSL32/SD1_IOVS/HA9
K6	VCC1833_2	Power	—
K7	—	—	—
K8	—	—	—
K9	VSS	Power	—
K10	VDD	Power	—
K11	VDD	Power	—
K12	VSS	Power	—
K13	VSS	Power	—
K14	VDD	Power	—
K15	VDD	Power	—
K16	VSS	Power	—
K17	VSS	Power	—
K18	—	—	—
K19	—	—	—
K20	DDR_VDDQ	Power	—
K21	DDR_DQA13	I/O	—
K22	VSS	Power	—
K23	DDR_DQA9	I/O	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
K24	DDR_DMIA1	I/O	—
K25	VSS	Power	—
L1	P03_3	I/O	IRQ03_3/TEND/CMTW1_TIC1/TXD1/SDA1/MOSI1/TXD3/SDA3/MOSI3/GMAC0_MDIO/GMAC1_MDIO/GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO/ESWM_MDIO/ESC_LINKACT0/SD1_PWEN
L2	P03_2	I/O	MD2/IRQ03_2/DACK/CMTW1_TOC1/RTCAT1HZ/DE2/TXDE4/ETH0_TXER/GMAC0_MDC/GMAC1_MDC/GMAC2_MDC/ETHSW_MDC/ESC_MDC/ESWM_MDC/SD1_IOVS/ENCIFDO4
L3	P03_0	I/O	IRQ03_0/A14/GTIOC3_3A/CTS2#/SCKE5/IIC_SCL2/ETH0_COL/ETH4_RXD3/SPI_MOSI3/MCLK10/HA14/ENCIFCK5/TST_OUT3/HDSL0_MOSI2
L4	P02_7	I/O	IRQ02_7/A13/MTIOC1B/MTIOC6C/GTIOC1_4B/GTADSM4_1/SS2#/CTS2#/RTS2#/RXDE1/ETH4_RXD2/MDAT11/MDAT42/HA13/ENCIFDI1/DUEI3
L5	P02_6	I/O	IRQ02_6/A12/MTIOC1A/MTIOC6A/GTIOC1_4A/GTADSM4_0/TXD2/SDA2/MOSI2/TXDE1/ETH4_RXD1/GMAC2_PTPTRG0/ESC_LEDSTER/SPI_SSL31/MCLK11/MCLK42/HA12/ENCIFDO1
L6	VCC1833_2	Power	—
L7	—	—	—
L8	—	—	—
L9	VDD	Power	—
L10	VSS	Power	—
L11	VSS	Power	—
L12	VSS	Power	—
L13	VSS	Power	—
L14	VSS	Power	—
L15	VSS	Power	—
L16	VDD	Power	—
L17	VDD	Power	—
L18	—	—	—
L19	—	—	—
L20	VSS	Power	—
L21	DDR_DQA10	I/O	—
L22	VSS	Power	—
L23	DDR_DQA1	I/O	—
L24	DDR_DQA3	I/O	—
L25	VSS	Power	—
M1	P04_1	I/O	IRQ04_1/GTIOC1_1A/SS0#/CTS0#/RST0#/DEE1/SD1_DATA1/MDAT00/MDAT30/ENCIFOE1/DUEI5/HDSL1_MISO1
M2	P03_5	I/O	IRQ03_5/A25/GTETRGSB/RXD3/SCL3/MISO3/RXDE5/ETH4_RXER/ESWM_PHYLINK1/HPSW_PHYLINK1/SPI_MISO0/SPI_SSL30/SD1_WP/MDAT11/MCLK30/ENCIFDI5
M3	P03_7	I/O	IRQ03_7/GTIOC1_0B/RXD0/SCL0/MISO0/DEE0/IIC_SCL0/SD1_CMD/MDAT02/MDAT32/ENCIFOE0/TST_OUT4/HDSL1_CLK1
M4	P03_4	I/O	ETH4_REFCLK/RMII4_REFCLK/IRQ03_4/A24/GTETRGSA/TXDE5/ESC_RESETOUT#/SPI_MOSI0/SPI_RSPCK3/SD1_CD/MCLK11/ENCIFDO5
M5	VSS	Power	—
M6	VSS	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
M7	—	—	—
M8	—	—	—
M9	VSS	Power	—
M10	VDD	Power	—
M11	VSS	Power	—
M12	VSS	Power	—
M13	VSS	Power	—
M14	VSS	Power	—
M15	VSS	Power	—
M16	VSS	Power	—
M17	VSS	Power	—
M18	—	—	—
M19	—	—	—
M20	DDR_VDDQ	Power	—
M21	DDR_DMIA0	I/O	—
M22	DDR_DQA7	I/O	—
M23	VSS	Power	—
M24	DDR_DQSA_C0	I/O	—
M25	DDR_DQSA_T0	I/O	—
N1	VSS	Power	—
N2	P03_6	I/O	IRQ03_6/GTIOC1_0A/SCK0/SCKE0/SD1_CLK/MCLK02/MCLK32/ENCIFCK0/DUEI4/HDSL1_SMPL
N3	P04_0	I/O	IRQ04_0/GTIOC1_1B/TXD0/SDA0/MOSI0/SCKE1/IIC_SDA0/SD1_DATA0/MCLK00/MCLK30/ENCIFCK1/SI4#/HDSL1_SEL1
N4	P04_2	I/O	IRQ04_2/GTIOC1_2A/CTS0#/TXDE2/SD1_DATA2/MCLK01/MCLK31/ENCIFDO2/TST_OUT5/HDSL1_MOSI1
N5	VCC1833_6	Power	—
N6	VCC1833_6	Power	—
N7	—	—	—
N8	—	—	—
N9	VDD	Power	—
N10	VSS	Power	—
N11	VSS	Power	—
N12	VSS	Power	—
N13	VSS	Power	—
N14	VSS	Power	—
N15	VSS	Power	—
N16	VDD	Power	—
N17	VCC18_PLL2	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
N18	—	—	—
N19	—	—	—
N20	VSS	Power	—
N21	DDR_DQA2	I/O	—
N22	VSS	Power	—
N23	DDR_DQA5	I/O	—
N24	DDR_DQA4	I/O	—
N25	VSS	Power	—
P1	P04_5	I/O	IRQ04_5/GTIOC5_1B/CMTW0_TOC0/RXD1/SCL1/MISO1/ESC_LINKACT0/CANRX0/ SPI_MISO1/SD0_CMD/NAND_RE#/HSPI_CS#/TST_OUT6/HDSL1_MISO2
P2	P04_4	I/O	IRQ04_4/GTIOC5_1A/CMTW0_TIC0/SCK1/GMAC0_PTPTRG0/ESC_LATCH0/SPI_RSPCK1/ SD0_CLK/NAND_WE#/HSPI_INT#/DUEI6/HDSL1_SEL2
P3	P04_3	I/O	IRQ04_3/GTIOC1_2B/DE0/RXDE2/SD1_DATA3/MDAT01/MDAT31/ENCIFDI2/SI5#/ HDSL1_CLK2
P4	P04_6	I/O	IRQ04_6/GTIOC2_4A/GTIOC5_2A/CMTW0_TIC1/TXD1/SDA1/MOSI1/ESC_LINKACT1/ CANTX0/SPI_MOSI1/SD0_DATA0/NAND_IO0/HSPI_IO0/SI6#/HDSL1_MOSI2
P5	VSS	Power	—
P6	VSS	Power	—
P7	—	—	—
P8	—	—	—
P9	VSS	Power	—
P10	VDD	Power	—
P11	VSS	Power	—
P12	VSS	Power	—
P13	VSS	Power	—
P14	VSS	Power	—
P15	VSS	Power	—
P16	VSS	Power	—
P17	VSS	Power	—
P18	—	—	—
P19	—	—	—
P20	DDR_VDDQ	Power	—
P21	VSS	Power	—
P22	DDR_DQA0	I/O	—
P23	VSS	Power	—
P24	DDR_DQA6	I/O	—
P25	VSS	Power	—
R1	P05_2	I/O	IRQ05_2/GTIOC1_3B/GTIOC5_0A/CMTW1_TIC1/SCK2/TXDE5/ESC_LEDRUN/SPI_RSPCK2/ SD0_DATA4/NAND_IO4/HSPI_CK/ENCIFDO5/HDSL2_CLK1
R2	P05_0	I/O	IRQ05_0/GTIOC3_4A/GTIOC5_3A/CMTW1_TIC0/CTS1#/SCKE5/ESC_LEDERR/CANTXDP0/ SPI_SSL11/SD0_DATA2/NAND_IO2/HSPI_IO2/ENCIFCK5/TST_OUT7/HDSL2_SMPL
R3	P04_7	I/O	IRQ04_7/GTIOC2_4B/GTIOC5_2B/CMTW0_TOC1/SS1#/CTS1#/RTS1#/ESC_RESETOUT#/ CANRXDP0/SPI_DDL10/SD0_DATA1/NAND_IO1/HSPI_IO1/DUEI7/HDSL2_LINK

Pin number	Primary pin name	Primary electrical type	Alternate pin names
R4	P05_1	I/O	IRQ05_1/GTIOC4_4B/GTIOC5_3B/CMTW1_TOC0/DE1/DEE5/ETHSW_PTPOUT0/ ESC_SYNC0/SPI_SSL12/SPI_RSPCK0/SD0_DATA3/NAND_IO3/HSPI_IO3/ENCIFOE5/SI7#
R5	VCC1833_5	Power	—
R6	VCC1833_5	Power	—
R7	—	—	—
R8	—	—	—
R9	VCC18_PLL0	Power	—
R10	VSS	Power	—
R11	VSS	Power	—
R12	VSS	Power	—
R13	VSS	Power	—
R14	VSS	Power	—
R15	VSS	Power	—
R16	VDD	Power	—
R17	VDD	Power	—
R18	—	—	—
R19	—	—	—
R20	VSS	Power	—
R21	DDR_CSA0	I/O	—
R22	DDR_CAA0	I/O	—
R23	VSS	Power	—
R24	DDR_CKA_C	I/O	—
R25	DDR_CKA_T	I/O	—
T1	VSS	Power	—
T2	P05_5	I/O	IRQ05_5/GTIOC2_3B/SS2#/CTS2#/RTS2#/RXD2/SCL2/MISO2/ETH0_CRS/SPI_SSL20/ SD0_DATA7/NAND_IO7/MDAT00/HSPI_IO6/HDSL2_MOSI1
T3	P05_3	I/O	IRQ05_3/GTIOC5_0B/CMTW1_TOC1/RXD2/SCL2/MISO2/RXDE5/IIC_SCL2/ETH0_TXER/ ETH1_RXER/SPI_MISO2/SD0_DATA5/NAND_IO5/HSPI_IO4/ENCIFDI5/HDSL2_SEL1
T4	P05_4	I/O	IRQ05_4/GTIOC2_3A/TXD2/SDA2/MOSI2/IIC_SDA2/ETH0_RXER/SPI_MOSI2/SD0_DATA6/ NAND_IO6/MCLK00/HSPI_IO5/HDSL2_MISO1
T5	VSS	Power	—
T6	VSS	Power	—
T7	—	—	—
T8	—	—	—
T9	VSS	Power	—
T10	VSS	Power	—
T11	VDD	Power	—
T12	VDD	Power	—
T13	VDD	Power	—
T14	VDD	Power	—
T15	VSS	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
T16	VSS	Power	—
T17	VSS	Power	—
T18	—	—	—
T19	—	—	—
T20	DDR_VDDQ	Power	—
T21	VSS	Power	—
T22	DDR_CAA2	I/O	—
T23	DDR_CAA1	I/O	—
T24	DDR_CKEA0	I/O	—
T25	VSS	Power	—
U1	P06_0	I/O	IRQ06_0/CS3#/GTIOC1_0A/SS3#/CTS3#/RTS3#/ETH1_RXER/ESC_LEDSTER/CANRXDP1/ SPI_SSL00/TST_OUT4/HDSL2_MISO2
U2	P05_7	I/O	IRQ05_7/CS2#/GTIOC1_3A/SCK3/SCKE5/ETH1_TXER/ESC_RESETOUT#/SPI_RSPCK0/ MCLK00/ENCIFCK5/DUEI4/HDSL2_SEL2
U3	P05_6	I/O	IRQ05_6/CTS2#/TXD2/SDA2/ MOSI2/ETH2_COL/SPI_SSL21/SD0_RST#/NAND_WP#/ MCLK01/HSPI_IO7/HDSL2_CLK2
U4	P06_3	I/O	IRQ06_3/D29/GTIOC1_1B/GTIOC2_0B/CTS3#/GMAC1_PTPTRG0/ESC_LEDERR/ CANTXDP1/SPI_SSL01/HD29/TST_OUT5/HDSL3_SMPL
U5	P06_1	I/O	IRQ06_1/CS5#/GTIOC1_3B/DEE5/TXD3/SDA3/ MOSI3/ETH1_CRS/CANTX1/SPI_MOSI0/ MDAT00/ENCIFOE5/SI4#/HDSL2_MOSI2
U6	VCC33	Power	—
U7	—	—	—
U8	—	—	—
U9	VDD	Power	—
U10	VDD	Power	—
U11	VSS	Power	—
U12	VCC18_PLL3	Power	—
U13	VCC18_PLL4	Power	—
U14	VSS	Power	—
U15	VDD	Power	—
U16	VCC33	Power	—
U17	VDD	Power	—
U18	—	—	—
U19	—	—	—
U20	VSS	Power	—
U21	DDR_CAA4	I/O	—
U22	DDR_CAA3	I/O	—
U23	VSS	Power	—
U24	DDR_CSA1	I/O	—
U25	DDR_CKEA1	I/O	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
V1	P06_5	I/O	IRQ06_5/D31/MTIOC2B/GTIOC1_2A/GTIOC2_1B/SCK4/SPI_SSL03/MCLK30/HD31/DUIE6/HDSL3_SEL1
V2	P06_4	I/O	IRQ06_4/D30/GTIOC1_1A/GTIOC2_1A/DE3/GMAC1_PTPTRG1/SPI_SSL02/MDAT01/HD30/SI5#/HDSL3_CLK1
V3	P06_2	I/O	IRQ06_2/D28/GTIOC1_0B/GITOC02_0A/RXD3/SCL3/MISO3/ETH1_COL/CANRX1/SPI_MISO0/MCLK01/HD28/DUEI5/HDSL3_LINK
V4	P06_7	I/O	IRQ06_7/GTIOC1_4B/GITOC02_2B/TXD4/SDA4/MOSI4/RXDE5/CANTX0/SD1_IOVS/MDAT02/ENCIFDI5/SI6#/HDCL3_MOSI1
V5	P07_1	I/O	IRQ07_1/POE4#/CTS4#/DEE1/ETH4_RXER/ETHSW_TDMAOUT1/ESC_LEDERR/CANRXDP0/SPI_SSL22/MCLK31/ADTRG0#/ENCIFOE1/TST_OUT7/HDSL3_SEL2
V6	VCC33	Power	—
V7	—	—	—
V8	—	—	—
V9	—	—	—
V10	—	—	—
V11	—	—	—
V12	—	—	—
V13	—	—	—
V14	—	—	—
V15	—	—	—
V16	—	—	—
V17	—	—	—
V18	—	—	—
V19	—	—	—
V20	DDR_VDDQ	Power	—
V21	DDR_CALIBRATION	Input	—
V22	DDR_RETENTION	Input	—
V23	DDR_RESET#	Output	—
V24	DDR_CAA5	I/O	—
V25	VSS	Power	—
W1	VSS	Power	—
W2	P07_0	I/O	IRQ07_0/POE0#/GTIOC1_2B/SS4#/CTS4#/RTS4#/IIC_SDA1/ETH4_TXER/ESC_RESETOUT#/SPI_SSL13/MDAT30/ADTRG2#/DUEI7/HDSL3_CLK2/POUTA
W3	P06_6	I/O	IRQ06_6/GTIOC1_4A/GTIOC2_2A/RXD4/SCL4/MISO4/TXDE5/CANRX0/SD1_PWEN/MCLK02/ENCIFDO5/TST_OUT6/HDSL3_MISO1
W4	P07_4	I/O	IRQ07_4/A16/POE11#/GTIOC1_1B/SCKE1/GMAC2_PTPTRG0/ETHSW_TDMAOUT0/ESC_LEDRUN/MDAT22/ENCIFCK1/HDSL3_MOSI2
W5	P07_2	I/O	IRQ07_2/POE8#/DE4/TXDE1/ETH4_CRS/ETHSW_PTPOUT2/ESC_SYNC0/CANTXDP0/SPI_SSL23/MDAT31/ADTRG1#/ENCIFDO1/SI7#/POUTB
W6	VSS	Power	—
W7	—	—	—
W8	—	—	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
W9	—	—	—
W10	—	—	—
W11	—	—	—
W12	—	—	—
W13	—	—	—
W14	—	—	—
W15	—	—	—
W16	—	—	—
W17	—	—	—
W18	—	—	—
W19	—	—	—
W20	VSS	Power	—
W21	VSS	Power	—
W22	VSS	Power	—
W23	VSS	Power	—
W24	VSS	Power	—
W25	VSS	Power	—
Y1	P07_5	I/O	IRQ07_5/MTCLKC/MTIOC0C/GTETRGA/TXDE6/IIC_SDA0/ETH0_TXER/CANTX0/SPI_MOSI3/MCLK21/ENCIFDO6/DUEI0/HDSL6_LINK
Y2	P07_6	I/O	IRQ07_6/A23/GTETRGB/ETH0_RXER/CANRXDP0/SPI_SSL30/TST_OUT0/HDSL6_SMPL
Y3	P07_3	I/O	IRQ07_3/POE10#/GTIOC1_0A/RXDE1/IIC_SCL1/ETH4_COL/GMAC2_PTPTRG1/ETHSW_PTPOUT3/ESC_SYNC1/MCLK22/ENCIFDI1/HDSL3_MISO2/POUTZ
Y4	P07_7	I/O	IRQ07_7/A22/MTCLKD/MTIOC0D/GTIOC0_1B/GTIOC4_0B/GTETRGC/SCK5/DEE6/IIC_SCL0/ETH0_CRS/CANRX0/SPI_MISO3/MCLK32/ENCIFOE6
Y5	P08_3	I/O	IRQ08_3/A18/TXD5/SDA5/MOSI5/ETH1_CRS/ETHSW_TDMAOUT2/ESC_LINKACT0/CANRXDP1/SPI_SSL33/SI0#/HDSL6_CLK2
Y6	VSS	Power	—
Y7	VCC33	Power	—
Y8	VCC33	Power	—
Y9	VSS	Power	—
Y10	VDD18ABG	Power	—
Y11	NCPOUT	Input	—
Y12	VSS_USB	Power	—
Y13	VSS	Power	—
Y14	PCIE_VDDA_RX	Power	—
Y15	PCIE_VDDA_TX	Power	—
Y16	VSS	Power	—
Y17	PCIE_VCC18A_ CMN	Power	—
Y18	VSS	Power	—
Y19	VSS	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
Y20	VCC18_ADC1	Power	—
Y21	VCC18_ADC2	Power	—
Y22	VCC18_OTP	Power	—
Y23	AVCC18_TSU	Power	—
Y24	VSS	Power	—
Y25	VSS	Power	—
AA1	P08_0	I/O	IRQ08_0/A21/MTIOC0A/MTIOC6A/GTIOC4_1A/GTETRGD/SS5#/CTS5#/RTS5#/SCKE6/ETH0_COL/CANRX1/SPI_RSPCK3/MDAT32/ENCIFCK6/DUEI1/HDSL6_SEL1
AA2	P08_2	I/O	IRQ08_2/A19/MTIOC0B/MTIOC6C/GTETRGSB/DE5/RXDE6/GMAC0_PTPTRG1/ESC_LATCH1/CANTX1/SPI_SSL32/SD0_WP/MDAT21/ENCIFDI6
AA3	P08_1	I/O	IRQ08_1/A20/GTETRGSA/CTS5#/GMAC0_PTPTRG0/ESC_LATCH0/CANTXDP0/SPI_SSL31/SD0_CD/TST_OUT1/HDSL6_MISO1
AA4	P08_5	I/O	MDW0/IRQ08_5/A6/SCKE3/SD1_PWEN/NAND_ALE/HA6/ENCIFCK3/DUIE0
AA5	P09_0	I/O	MDV0/IRQ09_0/WE0#/TXDE7/ETHSW_PTPOUT1/ESC_SYNC1/SD0_IOVS/HWR0#/ENCIFDO7/DUEI1
AA6	P09_3	I/O	IRQ09_3/CS0#/MTIOC2A/GTIOC4_3A/SS0#/CTS0#/RST0#/RXDE6/SCKE4/ETHSW_LPI0/ESWM_MPINT0/SD0_CD/NAND_RY_BY0#/MCLK31/HCS0#/ENCIFCK4/ENCIFDI6/HDSL6_MOSi1
AA7	VSS	Power	—
AA8	VSS	Power	—
AA9	VSS	Power	—
AA10	VSS	Power	—
AA11	VCC33_USB	Power	—
AA12	AVCC18_USB	Power	—
AA13	VSS	Power	—
AA14	PCIE_VDDA_RX	Power	—
AA15	PCIE_VDDA_TX	Power	—
AA16	VSS	Power	—
AA17	VSS	Power	—
AA18	VREFH0	Input	—
AA19	VCC18_ADC0	Power	—
AA20	VREFH1	Input	—
AA21	VREFH2	Input	—
AA22	VSS	Power	—
AA23	VSS	Power	—
AA24	VSS	Power	—
AA25	VSS	Power	—
AB1	VSS	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
AB2	P08_4	I/O	IRQ08_4/A17/RXD5/SCL5/MISO5/ETH1_COL/ETHSW_TDMAOUT3/ESC_LINKACT1/ CANTXDP1/SI1#/HDSL6_SEL2
AB3	P08_7	I/O	MDD/IRQ08_7/A8/DEE7/SD0_PWEN/NAND_CE0#/HA8/ENCIFOE7/SI0#
AB4	P09_5	I/O	MDV2/IRQ09_5/A1/TXDE3/TXDE4/ETHSW_LPI2/HA1/ENCIFDO3/ENCIFDO4/DUEI2
AB5	P10_3	I/O	IRQ10_3/MTIOC6D/GTIOC3_0B/RXD2/SCL2/MISO2/MDAT22/TST_OUT2
AB6	P10_6	I/O	IRQ10_6/MTIOC7B/GTIOC3_2A/CMTW0_TIC1/CTS2#/SCKE2/ENCIFCK2/TST_OUT3
AB7	P11_2	I/O	IRQ11_2/GTIOC0_3B/TXD1/SDA1/MOSI1/IIC_SDA0/ESC_I2CDATA/USB_EXICEN
AB8	P11_3	I/O	IRQ11_3/POE4#/GTETRGD/RXD0/SCL0/MISO0/IIC_SCL1
AB9	TRST#	Input	—
AB10	VSS	Power	—
AB11	VSS_USB	Power	—
AB12	USB_RREF	Input	—
AB13	VSS	Power	—
AB14	PCIE_VCC 18A	Power	—
AB15	PCIE_REF CLKN	Input	—
AB16	VSS	Power	—
AB17	RES#	Input	—
AB18	VSS	Power	—
AB19	VSS	Power	—
AB20	VSS	Power	—
AB21	VSS	Power	—
AB22	AN204	Input	—
AB23	VSS	Power	—
AB24	VSS	Power	—
AB25	VSS	Power	—
AC1	P08_6	I/O	MDW1/IRQ08_6/A7/DEE3/SD1_IOVS/NAND_CLE/HA7/ENCIFOE3/TST_OUT0
AC2	P09_1	I/O	MDV1/IRQ09_1/WE1#/SCKE7/NAND_CE1#/HWR1#/ENCIFCK7/TST_OUT1
AC3	P09_7	I/O	MDV4/IRQ09_7/A3/SCKE6/ETHSW_TDMAOUT1/ESC_LINKACT1/ESC_LINKACT2/HA3/ ENCIFCK6/SI2#/POUTA
AC4	P10_5	I/O	IRQ10_5/MTIOC7C/GTIOC3_1A/GTIOC4_2B/CMTW0_TOC0/SS2#/CTS2#/RTS2#/IIC_SDA2/ DUEI3
AC5	P10_4	I/O	IRQ10_4/MTIOC7A/GTIOC3_1B/GTIOC4_2A/CMTW0_TIC0/TXD2/SDA2/MOSI2/SI2#
AC6	P10_7	I/O	IRQ10_7/MTIOC7D/GTIOC3_2B/CMTW0_TOC1/DE2/DEE2/ENCIFOE2/SI3#
AC7	TMS	I/O	P12_0/IRQ12_0
AC8	P11_7	I/O	IRQ11_7/POE11#/GTIOC5_2A/GTETRGB/RTCAT1HZ/USB_OTG_ID/MBX_HINT#
AC9	P12_4	I/O	IRQ12_4/USB_VBUSIN
AC10	VSS	Power	—
AC11	VSS_USB	Power	—
AC12	VCC18_US B	Power	—
AC13	VSS_USB	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
AC14	VSS	Power	—
AC15	VSS	Power	—
AC16	PCIE_REFCLKP	Input	—
AC17	MDX	Input	—
AC18	EXTCLKIN	Input	—
AC19	VSS	Power	—
AC20	AN002	Input	—
AC21	AN100	Input	—
AC22	AN102	Input	—
AC23	AN202	Input	—
AC24	AN203	Input	—
AC25	AN207	Input	—
AD1	P09_2	I/O	IRQ09_2/WAIT#/SCK0/RXDE3/RXDE4/NAND_RY_BY1#/HWAIT#/ENCIFDI3/ENCIFDI4/SI1#/HDCL6_CLK1
AD2	P09_4	I/O	IRQ09_4/RD#/MTIOC2B/GTIOC4_3B/CTS0#/RXDE7/DEE4/ETHSW_LPI1/ESWM_MPINT1/SD0_WP/NAND_RY_BY2#/MDAT31/HRD#/ENCIFOE4/ENCIFDI7
AD3	P09_6	I/O	MDV3/IRQ09_6/A2/DE0/TXDE6/ETHSW_TDMAOUT0/NAND_CE2#/HA2/ENCIFDO6/TST_OUT2
AD4	P10_2	I/O	IRQ10_2/MTIOC1B/MTIOC6B/GTIOC3_0A/GTIOC4_1B/SCK2/IIC_SCL2/MCLK22/DUEI2
AD5	P11_0	I/O	IRQ11_0/TXDE2/USB_VBUSEN/ENCIFDO2
AD6	P11_1	I/O	IRQ11_1/GTIOC0_3A/RXD1/SCL1/MISO1/RXDE2/IIC_SCL0/ESC_I2CCLK/USB_OVRCUR/ENCIFDI2
AD7	P11_5	I/O	CKIO/IRQ11_5/POE0#/GTIOC5_0A/GTETRGA/SCIEXTCLK/IIC_SCL2/NAND_RY_BY3#/HCKIO
AD8	TDI	Input	P12_1/IRQ12_1
AD9	TDO	Output	P12_3/IRQ12_3
AD10	VSS	Power	—
AD11	USB_DP	I/O	—
AD12	VSS_USB	Power	—
AD13	VSS	Power	—
AD14	PCIE_RXDP	Input	—
AD15	VSS	Power	—
AD16	PCIE_TXDP	Output	—
AD17	VSS	Power	—
AD18	XTAL	Output	—
AD19	VSS	Power	—
AD20	AN001	Input	—
AD21	AN101	Input	—
AD22	AN103	Input	—
AD23	AN200	Input	—
AD24	AN201	Input	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
AD25	AN205	Input	—
AE1	VSS	Power	—
AE2	P10_0	I/O	MDV5/IRQ10_0/A4/DEE6/ETHSW_TDMAOUT2/ESC_IRQ/NAND_CE3#/HA4/ENCIFOE6/POUTB
AE3	P10_1	I/O	MDB/IRQ10_1/A5/ETHSW_TDMAOUT3/ESC_RESETOUT#/ESC_LEDRUN/HA5/POUTZ
AE4	VSS	Power	—
AE5	RSTOUT#	Output	P11_4/IRQ11_4/GTETRGSA/TXD0/SDA0/MOSI0/IIC_SDA1
AE6	P11_6	I/O	IRQ11_6/IIC_SDA2/USB_OVRCUR
AE7	VSS	Power	—
AE8	TCK	Input	P12_2/IRQ12_2
AE9	BSCANP	Input	—
AE10	VSS	Power	—
AE11	USB_DM	I/O	—
AE12	VSS_USB	Power	—
AE13	VSS	Power	—
AE14	PCIE_RXDN	Input	—
AE15	VSS	Power	—
AE16	PCIE_TXDN	Output	—
AE17	VSS	Power	—
AE18	EXTAL	Input	—
AE19	VSS	Power	—
AE20	AN000	Input	—
AE21	AN003	Input	—
AE22	VSS	Power	—
AE23	VSS	Power	—
AE24	AN206	Input	—
AE25	VSS	Power	—

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Pin number	Primary pin name	Primary electrical type	Alternate pin names
A1	VSS	Power	—
A2	P22_3	I/O	IRQ22_3/GTIOC0_3B/ETH1_RXD3/HDSL6_MOSI1
A3	P22_2	I/O	IRQ22_2/GTIOC0_3A/GTIOC4_5B/GTIOC5_0B/ETH1_RXD2/HDSL6_MISO1
A4	P21_6	I/O	IRQ21_6/ETH1_TXEN/HDSL6_LINK
A5	P21_4	I/O	IRQ21_4/ETH1_TXD2/HDSL5_MISO2
A6	P21_3	I/O	IRQ21_3/ETH1_TXD1/HDSL5_SEL2
A7	VSS	Power	—
A8	P20_4	I/O	MD0/IRQ20_4/GMAC0_MDC/GMAC1_MDC/GMAC2_MDC/ETHSW_MDC/ESC_MDC/ESWM_MDC/CANTX1

Pin number	Primary pin name	Primary electrical type	Alternate pin names
A9	P20_1	I/O	IRQ20_1/ETH0_RXD2/CANRXDP0/HDSL4_MISO2
A10	VSS	Power	—
A11	P20_0	I/O	IRQ20_0/ETH0_RXD1/CANTX0/HDSL4_SEL2
A12	P19_2	I/O	IRQ19_2/ETH0_TXD1/HDSL4_SMPL
A13	VSS	Power	—
A14	P18_4	I/O	IRQ18_4/GTETRGA/DEE4/ESWM_TASGATE1_5/XSPI0_IO5/MDAT21/ENCIFOE4/ HDSL3_MOSI1
A15	P18_0	I/O	IRQ18_0/ESWM_TASGATE1_1/XSPI0_IO1/MCLK02/HDSL3_SMPL
A16	P17_2	I/O	IRQ17_2/SCKE7/ESWM_TASGATE0_4/XSPI0_CKP/MCLK30/ENCIFCK7/HDSL2_MOSI1
A17	VSS	Power	—
A18	P16_6	I/O	IRQ16_6/MTCLKC/MTIOC0C/GTIOC3_3A/SCKE3/IIC_SCL0/ETH2_TXER/ETH3_TXER/ CANRXDP0/SPI_RSPCK0/XSPI1_IO4/MCLK30/ENCIFCK3/HDSL2_SMPL
A19	P16_4	I/O	IRQ16_4/MTIOC7B/GTIOC3_2A/GTIOC4_2A/RXD4/SCL3/MISO3/SCKE7/ETH4_CRS, SPI_MISO0/XSPI1_IO2/MCLK01/ENCIFCK7/HDSL1_MOSI2
A20	VSS	Power	—
A21	P15_3	I/O	IRQ15_3/D10/MTIOC1A/MTIOC3C/GTIOC2_4B/CMTW1_TOC0/RXDE2/SD1_IOVS/ADTRG0#/ HD10/ENCIFDI2/HDSL1_LINK
A22	P14_6	I/O	IRQ14_6/D5/MTIOC1B/MTIOC4B/GTIOC2_2A/CMTW0_TIC0/SD0_PWEN/HD5/ HDSL0_MOSI1/POUTA
A23	VSS	Power	—
B1	P23_6	I/O	IRQ23_6/GTIOC4_3A/GTIOC5_3A/RTCAT1HZ/SCK4/ETH2_RXCLK/ESC_LEDRUN/SD0_CD/ MDAT30/MDAT42/HDSL7_CLK2
B2	P23_0	I/O	IRQ23_0/GTIOC3_3A/GTIOC4_0A/RXD3/SCL3/MISO3/ETH2_TXCLK/SPI_RSPCK0/MDAT01/ HDSL7_LINK
B3	P23_1	I/O	IRQ23_1/GTIOC3_3B/GTIOC4_0B/SCK3/IIC_SCL0/ETH2_TXD0/GMAC0_PTPTRG0/ ESC_LATCH0/CANRXDP1/SPI_MISO0/MCLK21/MCLK40/HDSL7_SMPL
B4	P22_1	I/O	IRQ22_1/GTIOC4_5A/GTIOC5_0A/ETH1_RXD1/HDSL6_SEL1
B5	VSS	Power	—
B6	P21_1	I/O	IRQ21_1/ETH1_TXCLK/HDSL5_MOSI1
B7	P21_2	I/O	IRQ21_2/ETH1_TXD0/HDSL5_CLK2
B8	P20_6	I/O	IRQ20_6/ETHSW_PHYLINK0/ESC_PHYLINK0/ESWM_PHYLINK0/HPSW_PHYLINK0/ CANRXDP1/HDSL5_CLK1
B9	P20_3	I/O	IRQ20_3/ETH0_RXDV/HDSL5_LINK
B10	P19_6	I/O	IRQ19_6/ETH0_RXCLK/HDSL4_MOSI1
B11	P19_3	I/O	IRQ19_3/ETH0_TXD2/HDSL4_CLK1
B12	P19_0	I/O	IRQ19_0/ETH0_TXCLK/HDSL3_MOSI2
B13	P18_7	I/O	IRQ18_7/ESWM_TASGATE1_8/XSPI0_RESET0#/MCLK30/MDAT02/HDSL3_MISO2
B14	P18_3	I/O	IRQ18_3/SCKE4/ESWM_TASGATE1_4/XSPI0_IO4/MCLK21/ENCIFCK4/HDSL3_MISO1
B15	P17_7	I/O	IRQ17_7/ESWM_TASGATE1_0/XSPI0_IO0/MDAT20/HDSL3_LINK
B16	P17_3	I/O	IRQ17_3/DEE7/ESWM_TASGATE0_5/XSPI0_CKN/MDAT30/ENCIFOE7/HDSL2_CLK2
B17	P17_1	I/O	IRQ17_1/MTIOC0B/MTIOC6C/GTIOC4_4B/RXDE3/IIC_SDA1/ETH2_COL/ETH3_COL/ CANTX0/XSPI1_IO7/MDAT31/MBX_HINT#/ENCIFDI3/HDSL2_MISO1
B18	P16_5	I/O	IRQ16_5/MTIOC7D/GTIOC3_2B/GTIOC4_2B/TXD3/SDA3/MOSI3/DEE7/ETH4_COL/ SPI_MOSI0/XSPI1_IO3/MDAT01/ENCIFOE7/HDSL2_LINK
B19	P16_1	I/O	IRQ16_1/MTIOC6D/GTIOC3_0B/GTIOC4_0B/TXD1/SDA1/MOSI1/RXDE1/IIC_SDA2/ ESWM_TASGATE0_3/XSPI1_DS/MDAT22/ENCIFDI1/HDSL1_CLK2

Pin number	Primary pin name	Primary electrical type	Alternate pin names
B20	P15_6	I/O	IRQ15_6/GTIOC0_4A/DE1/TXDE6/TXDE7/IIC_SCL1/ESWM_TASGATE0_0/XSPI1_CKP/ MCLK21/ENCIFDO6/ENCIFDO7/HDSL1_SEL1
B21	P15_2	I/O	IRQ15_2/D9/MTIOC3A/MTIC5W/GTIOC2_4A/CMTW1_TIC0/TXDE2/SD1_PWEN/HD9/ ENCIFDO2/HDSL0_MOSI2
B22	P14_5	I/O	IRQ14_5/D4/MTIOC4C/MTIC5V/GTIOC0_1A/GTIOC2_1B/RXDE6/ETH2_COL/ETH3_COL/ ADTRG2#/HD4/ENCIFDI6/HDSL0_MISO1
B23	P15_4	I/O	IRQ15_4/D11/GTIOC2_0A/CMTW1_TIC1/SCKE6/IIC_SCL0/ESC_I2CCLK/MCLK20/ADTRG1#/ HD11/ENCIFCK6/HDSL1_SMPL
C1	P23_4	I/O	IRQ23_4/GTIOC4_2A/GTIOC4_3B/CTS3#/ETH2_TXD3/ETHSW_PTPOUT2/ESC_SYNC0/ SPI_SSL01/MDAT01/MDAT41/HDSL7_MISO1
C2	P24_1	I/O	IRQ24_1/DACK/POE4#/GTIOC4_4B/CMTW0_TIC0/SS4#/CTS4#/RTS4#/TXDE0/ETH0_TXER/ ETH2_RXD2/ESC_IRQ/ SPI_SSL10/SD1_WP/MCLK11/MBX_HINT#/ENCIFDO0
C3	P23_3	I/O	IRQ23_3/GTIOC4_1B/GTIOC4_3A/SS3#/CTS3#/RTS3#/ETH2_TXD2/ESC_LINKACT1/ SPI_SSL00/MCLK01/MCLK41/HDSL7_SEL1
C4	P23_2	I/O	IRQ23_2/GTIOC4_1A/IIC_SDA0/ETH2_TXD1/ESC_LINKACT0/CANTXDP1/SPI_MOSI0/ MDAT21/MDAT40/HDSL7_CLK1
C5	P22_4	I/O	IRQ22_4/GTIOC0_2B/ETH1_RXDV/HDSL6_CLK2
C6	P21_7	I/O	IRQ21_7/GTIOC4_4A/ETH1_RXCLK/HDSL6_SMPL
C7	P22_5	I/O	IRQ22_5/ETHSW_PHYLINK1/ESC_PHYLINK1/ESWM_PHYLINK1/HPSW_PHYLINK1/ HDSL6_SEL2
C8	P21_0	I/O	IRQ21_0/HDSL5_MISO1
C9	P20_5	I/O	IRQ20_5/GMAC0_MDIO/GMAC1_MDIO/GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO/ ESWM_MDIO/CANRX1/HDSL5_SMPL
C10	P19_7	I/O	IRQ19_7/ETH0_RXD0/CANRX0/HDSL4_CLK2
C11	P19_5	I/O	IRQ19_5/ETH0_TXEN/HDSL4_MISO1
C12	VSS	Power	—
C13	P18_5	I/O	IRQ18_5/GTETRGB/RXDE4/ESWM_TASGATE1_6/XSPI0_IO6/MCLK20/ENCIFDI4/ HDSL3_CLK2
C14	P18_2	I/O	IRQ18_2/ESWM_TASGATE1_3/XSPI0_IO3/MDAT32/HDSL3_SEL1
C15	P17_5	I/O	IRQ17_5/RXDE7/ESWM_TASGATE0_7/XSPI0_CS1#/MDAT31/ENCIFDI7/HDSL2_MISO2
C16	P17_4	I/O	IRQ17_4/TXDE7/ESWM_TASGATE0_6/XSPI0_CS0#/MCLK31/ENCIFDO7/HDSL2_SEL2
C17	P17_0	I/O	IRQ17_0/MTIOC0A/MTIOC6A/GTIOC3_4A/TXDE3/IIC_SCL1/ETH2_CRS/ETH3_CRS/ CANRX0/XSPI1_IO6/MCLK31/USB_VBUSEN/ENCIFDO3/HDSL2_SEL1
C18	P16_3	I/O	IRQ16_3/MTIOC7C/GTIOC3_1A/GTIOC4_1B/TXD5/SDA5/MOSI5/TXDE4/ETH4_RXER/ SPI_SSL02/XSPI1_IO1/ENCIFDO4/HDSL1_MISO2
C19	P16_0	I/O	IRQ16_0/MTIOC1B/MTIOC6B/GTIOC3_0A/GTIOC4_0A/RXD1/SCL1/MISO1/TXDE1/IIC_SCL2/ ESWM_TASGATE0_2/XSPI1_CS1#/MCLK22/ENCIFDO1/HDSL1_MOSI1
C20	P15_5	I/O	IRQ15_5/D12/GTIOC2_0B/CMTW1_TOC1/RTCAT1HZ/DEE6/IIC_SDA0/ESC_I2CDATA/ MDAT20/ADTRG2#/HD12/ENCIFDO6/HDSL1_CLK1
C21	P15_0	I/O	IRQ15_0/D7/MTCLKA/MTIOC8C/GTIOC2_3A/CMTW0_TIC1/SCKE2/SD1_CD/HD7/ENCIFCK2/ HDSL0_SEL2/POUTZ
C22	P14_3	I/O	IRQ14_3/D2/POE0#/GTIOC0_2A/GTETRGA/RTCAT1HZ/SCIEXTCLK/ADTRG0#/ USB_EXICEN/HD2/MBX_HINT#/HDSL0_CLK1
C23	P14_1	I/O	IRQ14_1/D0/MTIOC3B/MTIOC8A/GTIOC0_0A/GTIOC2_0A/GTIOC4_6A/SCKE6/ETH2_TXER/ ETH3_TXER/USB_VBUSEN/HD0/ENCIFCK6/HDSL0_LINK
D1	P24_2	I/O	IRQ24_2/TEND/POE8#/GTIOC4_5A/CMTW0_TOC0/CTS4#/RXDE0/ETH2_RXD3/ ESC_RESETOUT#/SPI_SSL11/MDAT11/ENCIFDI0/HDSL7_MOSI2
D2	P24_0	I/O	IRQ24_0/DREQ/POE0#/GTIOC4_4A/DEE0/IIC_SDA1/ETH0_CRS/ETH2_RXD1/ ESC_LINKACT2/SPI_SSL13/SD1_CD/MDAT10/MDAT32/ENCIFOE0/HDSL7_MISO2

Pin number	Primary pin name	Primary electrical type	Alternate pin names
D3	P23_5	I/O	IRQ23_5/GTIOC4_2B/DE3/ETH2_TXEN/ESC_LEDERR/SPI_SSL02/MCLK30/MCLK42/ HDSL7_MOSI1
D4	VSS	Power	—
D5	P22_7	I/O	IRQ22_7/HDSL6_MOSI2
D6	P22_6	I/O	ETH1_REFCLK/RMII1_REFCLK/IRQ22_6/HDSL6_MISO2
D7	P22_0	I/O	IRQ22_0/GTIOC4_4B/ETH1_RXD0/HDSL6_CLK1
D8	P21_5	I/O	IRQ21_5/ETH1_TXD3/HDSL5_MOSI2
D9	P20_7	I/O	ETH0_REFCLK/RMII0_REFCLK/IRQ20_7/CANTXDP1/HDSL5_SEL1
D10	P20_2	I/O	IRQ20_2/ETH0_RXD3/CANTXDP0/HDSL4_MOSI2
D11	P19_4	I/O	IRQ19_4/ETH0_TXD3/HDSL4_SEL1
D12	P19_1	I/O	IRQ19_1/ETH0_TXD0/HDSL4_LINK
D13	P18_6	I/O	IRQ18_6/GTETRGC/TXDE4/ESWM_TASGATE1_7/XSPI0_IO7/MDAT20/ENCIFDO4/ HDSL3_SEL2
D14	P18_1	I/O	IRQ18_1/ESWM_TASGATE1_2/XSPI0_IO2/MCLK32/HDSL3_CLK1
D15	P17_6	I/O	IRQ17_6/ESWM_TASGATE0_8/XSPI0_DS/MCLK20/HDSL2_MOSI2
D16	P16_7	I/O	IRQ16_7/MTCLKD/MTIOC0D/GTIOC3_3B/DEE3/IIC_SDA0/ETH2_RXER/ETH3_RXER/ CANTXDP0/SPI_SSL00/XSPI1_IO5/MDAT30/ENCIFOE3/HDSL2_CLK1
D17	P16_2	I/O	IRQ16_2/MTIOC7A/GTIOC3_1B/GTIOC4_1A/RXD5/SCL5/MISO5/RXDE4/ETH4_TXER/ SPI_SSL01/XSPI1_IO0/ENCIFDI4/HDSL1_SEL2
D18	P15_7	I/O	IRQ15_7/GTIOC0_4B/DE3/RXDE6/RXDE7/IIC_SDA1/ESWM_TASGATE0_1/XSPI1_CS0#/ MDAT21/ENCIFDI6/ENCIFDI7/HDSL1_MISO1
D19	P15_1	I/O	IRQ15_1/D8/MTCLKB/MTIOC8D/GTIOC2_3B/CMTW0_TOC1/DEE2/SD1_WP/HD8/ENCIFOE2/ HDSL0_MISO2
D20	P14_7	I/O	IRQ14_7/D6/MTIOC1A/MTIOC4D/GTIOC2_2B/CMTW0_TOC0/SD0_IOVS/HD6/HDSL0_CLK2/ POUTB
D21	P14_4	I/O	IRQ14_4/D3/MTIOC4A/MTIC5U/GTIOC0_1B/GTIOC2_1A/TXDE6/ETH2_CRS/ETH3_CRS/ ADTRG1#/HD3/ENCIFDO6/HDSL0_SEL1
D22	P14_2	I/O	IRQ14_2/D1/MTIOC3D/MTIOC8B/GTIOC0_0B/GTIOC2_0B/GTIOC4_6B/DEE6/ETH2_RXER/ ETH3_RXER/USB_OVRCUR/HD1/ENCIFOE6/HDSL0_SMPL
D23	VSS	Power	—
E1	P24_7	I/O	IRQ24_7/TXD3/SDA3/MOSI3/GMAC0_MDIO/GMAC1_MDIO/GMAC2_MDIO/ETHSW_MDIO/ ESC_MDIO/ESWM_MDIO/CANRX1/SPI_RSPCK1
E2	P24_5	I/O	IRQ24_5/POE10#/GTIOC4_6B/GTETRGA/TXD4/SDA4/MOSI4/SCIEXTCLK/MDAT22/ PCIE_RSTOUTB/HDSL0_CLK1
E3	P24_3	I/O	IRQ24_3/GTIOC4_5B/CMTW0_TIC1/RXD5/SDA5/MOSI5/IIC_SCL1/ETH0_RXER/ ETH2_RXDV/ESC_I2CCLK/SPI_MOSI1/SD0_PWEN/MDAT12/HDSL0_LINK
E4	VSS	Power	—
E5	P23_7	I/O	IRQ23_7/GTIOC4_3B/GTIOC5_3B/SCKE0/IIC_SCL1/ETH0_COL/ETH2_RXD0/SPI_SSL12/ SD0_WP/MCLK10/MCLK32/ENCIFCK0/HDSL7_SEL2
E6	VSS	Power	—
E7	VCC1833_1	Power	—
E8	VSS	Power	—
E9	VCC1833_0	Power	—
E10	VSS	Power	—
E11	VCC1833_0	Power	—
E12	VSS	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
E13	VCC1833_3	Power	—
E14	VSS	Power	—
E15	VCC1833_4	Power	—
E16	VSS	Power	—
E17	VCC33	Power	—
E18	VSS	Power	—
E19	VSS	Power	—
E20	VSS	Power	—
E21	VSS	Power	—
E22	VSS	Power	—
E23	VSS	Power	—
F1	VSS	Power	—
F2	P25_0	I/O	IRQ25_0/RXD1/SCL1/MISO1/RXD3/SCL3/MISO3/ETHSW_PHYLINK2/ESC_PHYLINK2/ CANTX1/SPI_SSL03/MCLK22
F3	P24_6	I/O	MD1/IRQ24_6/DE5/GMAC0_MDC/GMAC1_MDC/GMAC2_MDC/ETHSW_MDC/ESC_MDC/ ESWM_MDC
F4	P24_4	I/O	ETH2_REFCLK/RMII2_REFCLK/IRQ24_4/POE11#/GTIOC4_6A/CMTW0_TOC1/RXD5/SCL5/ MISO5/IIC_SDA1/ETH1_RXER/ESC_I2CDATA/SPI_MISO1/SD0_IOVS/MCLK12/HDSL0_SMPL
F5	P00_1	I/O	IRQ00_1/A17/MTIOC3D/GTIOC0_0B/GTADSM0_1/DEE1/IIC_SCL2/ETH3_TXD0/CANRX0/ SPI_MISO2/HA17/ENCIFOE1/HDSL0_MISO1
F6	VSS	Power	—
F7	VCC1833_1	Power	—
F8	VSS	Power	—
F9	VCC1833_0	Power	—
F10	VSS	Power	—
F11	VCC1833_0	Power	—
F12	VSS	Power	—
F13	VCC1833_3	Power	—
F14	VCC18_PLL1	Power	—
F15	VCC1833_4	Power	—
F16	VSS	Power	—
F17	VCC33	Power	—
F18	VSS	Power	—
F19	DDR_VDDQ	Power	—
F20	VSS	Power	—
F21	VSS	Power	—
F22	VSS	Power	—
F23	VSS	Power	—
G1	VSS	Power	—
G2	P00_0	I/O	IRQ00_0/A16/MTIOC3B/GTIOC0_0A/GTADSM0_0/SCKE1/ETH3_TXCLK/SPI_RSPCK2/HA16/ ENCIFCK1/HDSL0_SEL1

Pin number	Primary pin name	Primary electrical type	Alternate pin names
G3	P00_2	I/O	IRQ00_2/A18/MTIOC4A/GTIOC0_1B/GTADSM1_0/TXDE1/IIC_SDA2/ETH3_TXD1/CANTX0/ SPI_MOSI2/MCLK41/HA18/ENCIFDO1/HDSL0_MOSI1
G4	P00_4	I/O	IRQ00_4/A20/MITOC4B/GTIOC0_2A/GTADSM2_0/TXDE6/ETH3_TXD3/CANTXDP0/ SPI_SSL21/MCLK20/HA20/ENCIFDO6/HDSL0_SEL2
G5	VSS	Power	—
G6	VSS	Power	—
G7	—	—	—
G8	—	—	—
G9	—	—	—
G10	—	—	—
G11	—	—	—
G12	—	—	—
G13	—	—	—
G14	—	—	—
G15	—	—	—
G16	—	—	—
G17	—	—	—
G18	DDR_VDDQ	Power	—
G19	VSS	Power	—
G20	DDR_DQA15	I/O	—
G21	DDR_DQA8	I/O	—
G22	VSS	Power	—
G23	DDR_DQA14	I/O	—
H1	P00_5	I/O	IRQ00_5/A21/MTIOC4D/MTIOC8C/GTIOC0_2B/GTADSM2_1/RXDE6/ETH3_TXEN/ SPI_SSL22/MDAT20/HA21/ENCIFDI6/HDSL0_MISO2
H2	P00_6	I/O	IRQ00_6/A22/MTCLKA/MTIOC8D/GTIOC0_3A/GTADSM3_0/RXD4/SCL4/MISO4/SCKE0/ SCKE6/ETH3_RXCLK/SPI_SSL23/MBX_HINT#/ENCIFCK0/ENCIFCK6
H3	P00_3	I/O	IRQ00_3/A19/MTIOC4C/GTIOC0_1A/GTADSM1_1/RXDE1/ETH3_TXD2/CANRXDP0/ SPI_SSL20/MDAT41/HA19/ENCIFDI1/HDSL0_CLK2
H4	P00_7	I/O	IRQ00_7/A23/MTCLKB/MTIOC1B/GTIOC0_3B/GTADSM3_1/TXD4/SDA4/MOSI4/DEE0/DEE6/ ETH3_RXD0/SPI_SSL22/HERROUT#/ENCIFOE0/ENCIFOE6
H5	VCC1833_2	Power	—
H6	VCC1833_2	Power	—
H7	—	—	—
H8	VDD	Power	—
H9	VSS	Power	—
H10	VSS	Power	—
H11	VDD	Power	—
H12	VSS	Power	—
H13	VSS	Power	—
H14	VDD	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
H15	VSS	Power	—
H16	VDD	Power	—
H17	—	—	—
H18	VSS	Power	—
H19	DDR_DQA12	I/O	—
H20	DDR_DQA11	I/O	—
H21	VSS	Power	—
H22	DDR_DQSA_T1	I/O	—
H23	DDR_DQSA_C1	I/O	—
J1	P01_0	I/O	IRQ01_0/A0/MTIOC1A/MTIOC3A/GTIOC0_4A/GTADSM4_0_/DE4/TXDE0/ETH3_RXD1/ SPI_SSL21/HA0/ENCIFDO0
J2	P01_1	I/O	IRQ01_1/RD/WR#/MITOC3C/MTIOC8A/GTIOC0_4B/GTADSM4_1/SCK5/RXD5/SCL5/ MISO5/ RXDE0/ETH3_RXD2/SD1_PWEN/USB_OVRCUR/HWRSTB#/ENCIFDI0
J3	P01_2	I/O	IRQ01_2/BS#/DREQ/SS5#/CTS5#/RST5#/TXD5/SDA5/MOSI5/SCKE4/ETH3_RXD3/ SPI_MOSI2/SD1_IOVS/MCLK00/ADTRG0#/HBS#/ENCIFCK4
J4	P01_4	I/O	ETH3_REFCLK/RMII3_REFCLK/IRQ01_4/CS5#/TEND/TXD1/SDA1/MOSI1/RXDE4/IIC_SDA1/ ETH1_RXER/ETH1_CRS/ESC_I2CDATA/SPI_RSPCK2/MCLK01/USB_EXICEN/ADTRG2#/ ENCIFDI4
J5	VSS	Power	—
J6	VSS	Power	—
J7	—	—	—
J8	VSS	Power	—
J9	VDD	Power	—
J10	VDD	Power	—
J11	VSS	Power	—
J12	VDD	Power	—
J13	VDD	Power	—
J14	VSS	Power	—
J15	VDD	Power	—
J16	VSS	Power	—
J17	—	—	—
J18	DDR_VDDQ	Power	—
J19	DDR_DQA13	I/O	—
J20	VSS	Power	—
J21	DDR_DQA9	I/O	—
J22	DDR_DMIA1	I/O	—
J23	VSS	Power	—
K1	VSS	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
K2	P01_3	I/O	IRQ01_3/CS3#/DACK/CTS5#/RXD1/ SCL1/MISO1/ DEE4/IIC_SCL1/ETH1_TXER/ ETH3_RXDV/ESC_I2CCLK/SPI_MISO2/MDAT00/ADTRG1#/MBX_HINT#/ENCIFOE4
K3	P01_5	I/O	IRQ01_5/CS2#/DREQ/TXDE4/ETH1_COL/ETH3_TXER/ESC_RESETOUT#/ ESWM_PHYLINK0/HPSW_PHYLINK0/SPI_SSL20/MDAT01/USB_EXICEN/HCS1#/ENCIFDO4
K4	P02_0	I/O	IRQ02_0/WE2#/MTIC5V/MTIOC7A/GTIOC1_1B/GTADSM1_0/GTETRGD/TXD1/SDA1/MOSI1/ SCIEXTCLK/ETH4_TXD1/ETHSW_PTPOUT0/ESC_SYNC0/SPI_MOSI3/SD1_PWEN/HWR2#
K5	VCC1833_2	Power	—
K6	VCC1833_2	Power	—
K7	—	—	—
K8	VDD	Power	—
K9	VSS	Power	—
K10	VSS	Power	—
K11	VSS	Power	—
K12	VSS	Power	—
K13	VSS	Power	—
K14	VSS	Power	—
K15	VSS	Power	—
K16	VDD	Power	—
K17	—	—	—
K18	VSS	Power	—
K19	DDR_DQA10	I/O	—
K20	VSS	Power	—
K21	DDR_DQA1	I/O	—
K22	DDR_DQA3	I/O	—
K23	VSS	Power	—
L1	P01_7	I/O	IRQ01_7/D14/MTIC5U/MTIOC6D/GTIOC1_0B/GTADSM0_1/GTETRGC/CMTW1_TOC0/RXD1/ SCL1/MISO1/ETH1_RXER/ETH4_TXD0/SPI_MISO3/SD1_WP/MDAT02/HD14
L2	P01_6	I/O	IRQ01_6/D13/MTIOC6B/MTIOC8B/GTIOC1_0A/GTADSM0_0/GTETRGB/CMTW1_TIC0/SCK1/ ETH0_RXER/ETH4_TXCLK/SPI_RSPCK3/SD1_CD/MCLK02/HD13
L3	P02_1	I/O	IRQ02_1/WE3#/A H#/MTIC5W/MTIOC7C/GTIOC1_1A/GTADSM1_1/SS1#/ CTS1#/RTS1#/RXD3/SCL3/MISO3/TXDE5/ETH4_TXD2/GMAC0_PTPTRG0/ESC_LATCH0/ SPI_SSL30/SPI_SSL00/HWR3#/ENCIFDO5
L4	P02_3	I/O	IRQ02_3/A9/MTIOC0B/MTIOC7D/GTIOC1_2B/GTADSM2_1/DE1/ETH4_TXEN/ GMAC1_PTPTRG0/ESC_LEDERR/SPI_SSL02/SPI_SSL32/SD1_IOVS/HA9
L5	VSS	Power	—
L6	VSS	Power	—
L7	—	—	—
L8	VSS	Power	—
L9	VDD	Power	—
L10	VSS	Power	—
L11	VSS	Power	—
L12	VSS	Power	—
L13	VSS	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
L14	VSS	Power	—
L15	VDD	Power	—
L16	VSS	Power	—
L17	—	—	—
L18	DDR_VDDQ	Power	—
L19	DDR_DMIA0	I/O	—
L20	DDR_DQA7	I/O	—
L21	VSS	Power	—
L22	DDR_DQSA_C0	I/O	—
L23	DDR_DQSA_T0	I/O	—
M1	VSS	Power	—
M2	P02_4	I/O	IRQ02_4/A10/MTCLKC/MTIOC0C/GTIOC1_3A/GTADSM3_0/SCK2/ SCKE1/ETH4_RXCLK/ GMAC1_PTPTRG1/SPI_SSL03/SPI_SSL33/MCLK12/MCLK40/HA10/ENCIFCK1
M3	P02_6	I/O	IRQ02_6/A12/MTIOC1A/MTIOC6A/GTIOC1_4A/GTADSM4_0/TXD2/SDA2/MOSI2/TXDE1/ ETH4_RXD1/GMAC2_PTPTRG0/ESC_LEDSTER/SPI_SSL31/MCLK11/MCLK42/HA12/ ENCIFDO1
M4	P03_1	I/O	IRQ03_1/A15/GTIOC3_3B/DE2/DEE5/IIC_SDA2/ETH0_CRS/ETH4_RXDV/ETHSW_PTPOUT3/ ESC_SYNC1/SPI_MISO3/MDAT10/HA15/ENCIFOE5/SI3#/HDSL1_LINK
M5	VCC1833_6	Power	—
M6	VCC1833_6	Power	—
M7	—	—	—
M8	VDD	Power	—
M9	VSS	Power	—
M10	VSS	Power	—
M11	VSS	Power	—
M12	VSS	Power	—
M13	VSS	Power	—
M14	VSS	Power	—
M15	VSS	Power	—
M16	VCC18_PLL2	Power	—
M17	—	—	—
M18	VSS	Power	—
M19	DDR_DQA2	I/O	—
M20	VSS	Power	—
M21	DDR_DQA5	I/O	—
M22	DDR_DQA4	I/O	—
M23	VSS	Power	—
N1	P02_2	I/O	IRQ02_2/D15/MTIOC0A/MTIOC7B/GTIOC1_2A/GTADSM2_0/CTS1#/ETH4_TXD3/ GMAC0_PTPTRG1/ESC_LEDRUN/ESC_LATCH1/SPI_SSL01/SPI_SSL31/SD1_PWEN/HD15

Pin number	Primary pin name	Primary electrical type	Alternate pin names
N2	P02_5	I/O	IRQ02_5/A11/MTCLKD/MTIOC0D/GTIOC1_3B/GTADSM3_1/RXD2/SCL2/MISO2/DEE1/ ETH4_RXD0/GMAC2_PTPTRG1/SPI_SSL32/MDAT12/ MDAT40/HA11/ENCIFOE1
N3	P03_0	I/O	IRQ03_0/A14/GTIOC3_3A/CTS2#/SCKE5/IIC_SCL2/ETH0_COL/ETH4_RXD3/SPI_MOSI3/ MCLK10/HA14/ENCIFCK5/TST_OUT3/HDSL0_MOSI2
N4	P03_4	I/O	ETH4_REFCLK/RMII4_REFCLK/IRQ03_4/A24/GTETRGSA/TXDE5/ESC_RESETOUT#/ SPI_MOSI0/SPI_RSPCK3/SD1_CD/MCLK11/ENCIFDO5
N5	VSS	Power	—
N6	VSS	Power	—
N7	—	—	—
N8	VSS	Power	—
N9	VDD	Power	—
N10	VSS	Power	—
N11	VSS	Power	—
N12	VSS	Power	—
N13	VSS	Power	—
N14	VSS	Power	—
N15	VDD	Power	—
N16	VSS	Power	—
N17	—	—	—
N18	DDR_VDDQ	Power	—
N19	VSS	Power	—
N20	DDR_DQA0	I/O	—
N21	VSS	Power	—
N22	DDR_DQA6	I/O	—
N23	VSS	Power	—
P1	P02_7	I/O	IRQ02_7/A13/MTIOC1B/MTIOC6C/GTIOC1_4B/GTADSM4_1/SS2#/CTS2#/RTS2#/RXDE1/ ETH4_RXD2/MDAT11/MDAT42/HA13/ENCIFDI1/DUEI3
P2	P03_3	I/O	IRQ03_3/TEND/CMTW1_TIC1/TXD1/SDA1/MOSI1/TXD3/SDA3/MOSI3/GMAC0_MDIO/ GMAC1_MDIO/GMAC2_MDIO/ETHSW_MDIO/ESC_MDIO/ESWM_MDIO/ESC_LINKACT0/ SD1_PWEN
P3	P04_0	I/O	IRQ04_0/GTIOC1_1B/TXD0/SDA0/MOSI0/SCKE1/IIC_SDA0/SD1_DATA0/MCLK00/MCLK30/ ENCIFCK1/SI4#/HDSL1_SEL1
P4	P03_7	I/O	IRQ03_7/GTIOC1_0B/RXD0/SCL0/MISO0/DEE0/IIC_SCL0/SD1_CMD/MDAT02/MDAT32/ ENCIFOE0/TST_OUT4/HDSL1_CLK1
P5	VSS	Power	—
P6	VCC18_PLL0	Power	—
P7	—	—	—
P8	VDD	Power	—
P9	VSS	Power	—
P10	VSS	Power	—
P11	VSS	Power	—
P12	VSS	Power	—
P13	VSS	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
P14	VSS	Power	—
P15	VSS	Power	—
P16	VDD	Power	—
P17	—	—	—
P18	VSS	Power	—
P19	DDR_CSA0	I/O	—
P20	DDR_CAA0	I/O	—
P21	VSS	Power	—
P22	DDR_CKA_C	I/O	—
P23	DDR_CKA_T	I/O	—
R1	P03_2	I/O	MD2/IRQ03_2/DACK/CMTW1_TOC1/RTCAT1HZ/DE2/TXDE4/ETH0_TXER/GMAC0_MDC/GMAC1_MDC/GMAC2_MDC/ETHSW_MDC/ESC_MDC/ESWM_MDC/SD1_IOVS/ENCIFDO4
R2	P03_5	I/O	IRQ03_5/A25/GTETRGSB/RXD3/SCL3/MISO3/RXDE5/ETH4_RXER/ESWM_PHYLINK1/HPSW_PHYLINK1/SPI_MISO0/SPI_SSL30/SD1_WP/MDAT11/MCLK30/ENCIFDI5
R3	P04_1	I/O	IRQ04_1/GTIOC1_1A/SS0#/CTS0#/RST0#/DEE1/SD1_DATA1/MDAT00/MDAT30/ENCIFOE1/DUEI5/HDSL1_MISO1
R4	P04_2	I/O	IRQ04_2/GTIOC1_2A/CTS0#/TXDE2/SD1_DATA2/MCLK01/MCLK31/ENCIFDO2/TST_OUT5/HDSL1_MOSI1
R5	VCC1833_5	Power	—
R6	VCC1833_5	Power	—
R7	—	—	—
R8	VSS	Power	—
R9	VDD	Power	—
R10	VSS	Power	—
R11	VDD	Power	—
R12	VDD	Power	—
R13	VSS	Power	—
R14	VDD	Power	—
R15	VDD	Power	—
R16	VSS	Power	—
R17	—	—	—
R18	DDR_VDDQ	Power	—
R19	VSS	Power	—
R20	DDR_CAA2	I/O	—
R21	DDR_CAA1	I/O	—
R22	DDR_CKEA0	I/O	—
R23	VSS	Power	—
T1	P03_6	I/O	IRQ03_6/GTIOC1_0A/SCK0/SCKE0/SD1_CLK/MCLK02/MCLK32/ENCIFCK0/DUEI4/HDSL1_SMPL
T2	P04_3	I/O	IRQ04_3/GTIOC1_2B/DE0/RXDE2/SD1_DATA3/MDAT01/MDAT31/ENCIFDI2/SI5#/HDSL1_CLK2

Pin number	Primary pin name	Primary electrical type	Alternate pin names
T3	P04_6	I/O	IRQ04_6/GTIOC2_4A/GTIOC5_2A/CMTW0_TIC1/TXD1/SDA1/MOSI1/ESC_LINKACT1/ CANTX0/SPI_MOSI1/SD0_DATA0/NAND_IO0/HSPI_IO0/SI6#/HDSL1_MOSI2
T4	P05_1	I/O	IRQ05_1/GTIOC4_4B/GTIOC5_3B/CMTW1_TOC0/DE1/DEE5/ETHSW_PTPOUT0/ ESC_SYNC0/SPI_SSL12/SPI_RSPCK0/SD0_DATA3/NAND_IO3/HSPI_IO3/ENCIFOE5/SI7#
T5	VSS	Power	—
T6	VSS	Power	—
T7	—	—	—
T8	VDD	Power	—
T9	VSS	Power	—
T10	VDD	Power	—
T11	VCC18_PLL4	Power	—
T12	VSS	Power	—
T13	VDD	Power	—
T14	VCC33	Power	—
T15	VSS	Power	—
T16	VDD	Power	—
T17	—	—	—
T18	VSS	Power	—
T19	DDR_CAA4	I/O	—
T20	DDR_CAA3	I/O	—
T21	VSS	Power	—
T22	DDR_CSA1	I/O	—
T23	DDR_CKEA1	I/O	—
U1	VSS	Power	—
U2	P04_4	I/O	IRQ04_4/GTIOC5_1A/CMTW0_TIC0/SCK1/GMAC0_PTPTRG0/ESC_LATCH0/SPI_RSPCK1/ SD0_CLK/NAND_WE#/HSPI_INT#/DUEI6/HDSL1_SEL2
U3	P05_2	I/O	IRQ05_2/GTIOC1_3B/GTIOC5_0A/CMTW1_TIC1/SCK2/TXDE5/ESC_LEDRUN/SPI_RSPCK2/ SD0_DATA4/NAND_IO4/HSPI_CK/ENCIFDO5/HDSL2_CLK1
U4	P05_4	I/O	IRQ05_4/GTIOC2_3A/TXD2/SDA2/MOSI2/IIC_SDA2/ETH0_RXER/SPI_MOSI2/SD0_DATA6/ NAND_IO6/MCLK00/HSPI_IO5/HDSL2_MISO1
U5	VSS	Power	—
U6	VCC33	Power	—
U7	—	—	—
U8	—	—	—
U9	—	—	—
U10	—	—	—
U11	—	—	—
U12	—	—	—
U13	—	—	—
U14	—	—	—
U15	—	—	—
U16	—	—	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
U17	—	—	—
U18	DDR_VDDQ	Power	—
U19	DDR_CALIBRATION	Input	—
U20	DDR_RETENTION	Input	—
U21	DDR_RESET#	Output	—
U22	DDR_CAA5	I/O	—
U23	VSS	Power	—
V1	P04_5	I/O	IRQ04_5/GTIOC5_1B/CMTW0_TOC0/RXD1/SCL1/MISO1/ESC_LINKACT0/CANRX0/SPI_MISO1/SD0_CMD/NAND_RE#/HSPI_CS#/TST_OUT6/HDSL1_MISO2
V2	P04_7	I/O	IRQ04_7/GTIOC2_4B/GTIOC5_2B/CMTW0_TOC1/SS1#/CTS1#/RTS1#/ESC_RESETOUT#/CANRXDP0/SPI_DDL10/SD0_DATA1/NAND_IO1/HSPI_IO1/DUEI7/HDSL2_LINK
V3	VSS	Power	—
V4	P05_3	I/O	IRQ05_3/GTIOC5_0B/CMTW1_TOC1/RXD2/SCL2/MISO2/RXDE5/IIC_SCL2/ETH0_TXER/ETH1_RXER/SPI_MISO2/SD0_DATA5/NAND_IO5/HSPI_IO4/ENCIFDI5/HDSL2_SEL1
V5	VSS	Power	—
V6	VSS	Power	—
V7	VCC33	Power	—
V8	VCC33	Power	—
V9	VSS	Power	—
V10	VCC18_PLL3	Power	—
V11	VSS	Power	—
V12	PCIE_VDDA_RX	Power	—
V13	PCIE_VDDA_TX	Power	—
V14	PCIE_VDDA_TX	Power	—
V15	PCIE_VCC18A_CMN	Power	—
V16	VSS	Power	—
V17	VSS	Power	—
V18	VSS	Power	—
V19	VSS	Power	—
V20	VCC18_OTP	Power	—
V21	VSS	Power	—
V22	VSS	Power	—
V23	VSS	Power	—
W1	P05_0	I/O	IRQ05_0/GTIOC3_4A/GTIOC5_3A/CMTW1_TIC0/CTS1#/SCKE5/ESC_LEDERR/CANTXDP0/SPI_SSL11/SD0_DATA2/NAND_IO2/HSPI_IO2/ENCIFCK5/TST_OUT7/HDSL2_SMPL
W2	P05_5	I/O	IRQ05_5/GTIOC2_3B/SS2#/CTS2#/RTS2#/RXD2/SCL2/MISO2/ETH0_CRS/SPI_SSL20/SD0_DATA7/NAND_IO7/MDAT00/HSPI_IO6/HDSL2_MOSI1

Pin number	Primary pin name	Primary electrical type	Alternate pin names
W3	P05_6	I/O	IRQ05_6/CTS2#/TXD2/SDA2/ MOSI2/ETH2_COL/SPI_SSL21/SD0_RST#/NAND_WP#/ MCLK01/HSPI_IO7/HDSL2_CLK2
W4	P08_5	I/O	MDW0/IRQ08_5/A6/SCKE3/SD1_PWEN/NAND_ALE/HA6/ENCIFCK3/DUIE0
W5	P08_7	I/O	MDD/IRQ08_7/A8/DEE7/SD0_PWEN/NAND_CE0#/HA8/ENCIFOE7/SI0#
W6	VSS	Power	—
W7	VSS	Power	—
W8	VSS	Power	—
W9	VDD18ABG	Power	—
W10	VCC33_USB	Power	—
W11	VSS_USB	Power	—
W12	VSS	Power	—
W13	PCIE_VDDA_RX	Power	—
W14	PCIE_REFCLKN	Input	—
W15	VSS	Power	—
W16	VSS	Power	—
W17	VCC18_ADC0	Power	—
W18	VCC18_ADC1	Power	—
W19	VCC18_ADC2	Power	—
W20	VSS	Power	—
W21	AVCC18_TSU	Power	—
W22	VSS	Power	—
W23	VSS	Power	—
Y1	P08_6	I/O	MDW1/IRQ08_6/A7/DEE3/SD1_IOVS/NAND_CLE/HA7/ENCIFOE3/TST_OUT0
Y2	P09_0	I/O	MDV0/IRQ09_0/WE0#/TXDE7/ETHSW_PTPOUT1/ESC_SYNC1/SD0_IOVS/HWR0#/ ENCIFDO7/DUEI1
Y3	P09_3	I/O	IRQ09_3/CS0#/MTIOC2A/GTIOC4_3A/SS0#/CTS0#/RST0#/RXDE6/SCKE4/ETHSW_LPI0/ ESWM_MPINT0/SD0_CD/NAND_RY_BY0#/MCLK31/HCS0#/ENCIFCK4/ENCIFDI6/ HDSL6_MOSi1
Y4	P09_5	I/O	MDV2/IRQ09_5/A1/TXDE3/TXDE4/ETHSW_LPI2/HA1/ENCIFDO3/ENCIFDO4/DUEI2
Y5	P09_7	I/O	MDV4/IRQ09_7/A3/SCKE6/ETHSW_TDMAOUT1/ESC_LINKACT1/ESC_LINKACT2/HA3/ ENCIFCK6/SI2#/POUTA
Y6	TDI	Input	P12_1/IRQ12_1
Y7	TRST#	Input	—
Y8	VSS	Power	—
Y9	NCPOUT	Input	—
Y10	AVCC18_USB	Power	—
Y11	VSS_USB	Power	—
Y12	VSS	Power	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
Y13	PCIE_VCC 18A	Power	—
Y14	PCIE_REF CLKP	Input	—
Y15	EXTCLKIN	Input	—
Y16	MDX	Input	—
Y17	VREFH0	Power	—
Y18	VREFH1	Power	—
Y19	VREFH2	Power	—
Y20	VSS	Power	—
Y21	VSS	Power	—
Y22	VSS	Power	—
Y23	AN205	Input	—
AA1	P09_1	I/O	MDV1/IRQ09_1/WE1#/SCKE7/NAND_CE1#/HWR1#/ENCIFCK7/TST_OUT1
AA2	P09_2	I/O	IRQ09_2/WAIT#/SCK0/RXDE3/RXDE4/NAND_RY_BY1#/HWAIT#/ENCIFDI3/ENCIFDI4/SI1#/ HDCL6_CLK1
AA3	P09_4	I/O	IRQ09_4/RD#/MTIOC2B/GTIOC4_3B/CTS0#/RXDE7/DEE4/ETHSW_LPI1/ESWM_MPINT1/ SD0_WP/NAND_RY_BY2#/MDAT31/HRD#/ENCIFOE4/ENCIFDI7
AA4	P11_3	I/O	IRQ11_3/POE4#/GTETRGD/RXD0/SCL0/MISO0/IIC_SCL1
AA5	P11_7	I/O	IRQ11_7/POE11#/GTIOC5_2A/GTETRGB/RTCAT1HZ/USB_OTG_ID/MBX_HINT#
AA6	TDO	Output	P12_3/IRQ12_3
AA7	P12_4	I/O	IRQ12_4/USB_VBUSIN
AA8	VSS	Power	—
AA9	VSS_USB	Power	—
AA10	USB_RREF	Power	—
AA11	VSS_USB	Power	—
AA12	VSS	Power	—
AA13	VSS	Power	—
AA14	VSS	Power	—
AA15	VSS	Power	—
AA16	VSS	Power	—
AA17	VSS	Power	—
AA18	VSS	Power	—
AA19	AN102	Input	—
AA20	AN103	Input	—
AA21	AN201	Input	—
AA22	AN203	Input	—
AA23	AN207	Input	—
AB1	P09_6	I/O	MDV3/IRQ09_6/A2/DE0/TXDE6/ETHSW_TDMAOUT0/NAND_CE2#/HA2/ENCIFDO6/ TST_OUT2
AB2	P10_0	I/O	MDV5/IRQ10_0/A4/DEE6/ETHSW_TDMAOUT2/ESC_IRQ/NAND_CE3#/HA4/ENCIFOE6/ POUTB
AB3	P10_1	I/O	MDB/IRQ10_1/A5/ETHSW_TDMAOUT3/ESC_RESETOUT#/ESC_LEDRUN/HA5/POUTZ

Pin number	Primary pin name	Primary electrical type	Alternate pin names
AB4	P11_0	I/O	IRQ11_0/TXDE2/USB_VBUSEN/ENCIFDO2
AB5	P11_2	I/O	IRQ11_2/GTIOC0_3B/TXD1/SDA1/MOSI1/IIC_SDA0/ESC_I2CDATA/USB_EXICEN
AB6	P11_5	I/O	CKIO/IRQ11_5/POE0#/GTIOC5_0A/GTETRGA/SCIEXTCLK/IIC_SCL2/NAND_RY_BY3#/ HCKIO
AB7	BSCANP	Input	—
AB8	VSS	Power	—
AB9	USB_DP	I/O	—
AB10	VCC18_USB	Power	—
AB11	VSS	Power	—
AB12	PCIE_RXDP	Input	—
AB13	VSS	Power	—
AB14	PCIE_TXDP	Output	—
AB15	VSS	Power	—
AB16	XTAL	Power	—
AB17	VSS	Power	—
AB18	AN000	Input	—
AB19	AN002	Input	—
AB20	AN101	Input	—
AB21	AN202	Input	—
AB22	AN204	Input	—
AB23	AN206	Input	—
AC1	VSS	Power	—
AC2	P11_1	I/O	IRQ11_1/GTIOC0_3A/RXD1/SCL1/MISO1/RXDE2/IIC_SCL0/ESC_I2CCLK/USB_OVRCUR/ ENCIFDI2
AC3	RSTOUT#	Output	P11_4/IRQ11_4/GTETRGSA/TXD0/SDA0/MOSI0/IIC_SDA1
AC4	P11_6	I/O	IRQ11_6/IIC_SDA2/USB_OVRCUR
AC5	TMS	I/O	P12_0/IRQ12_0
AC6	VSS	Power	—
AC7	TCK	Input	P12_2/IRQ12_2
AC8	VSS	Power	—
AC9	USB_DM	I/O	—
AC10	VSS_USB	Power	—
AC11	VSS	Power	—
AC12	PCIE_RXDN	Input	—
AC13	VSS	Power	—
AC14	PCIE_TXDN	Output	—
AC15	VSS	Power	—
AC16	EXTAL	Input	—
AC17	RES#	Input	—

Pin number	Primary pin name	Primary electrical type	Alternate pin names
AC18	AN001	Input	—
AC19	AN003	Input	—
AC20	AN100	Input	—
AC21	VSS	Power	—
AC22	AN200	Input	—
AC23	VSS	Power	—

2.3 Symbol Parameters

Orderable Part Number	Min Input Voltage	Max Input Voltage	Frequency	Min Operating Temperature	Max Operating Temperature	RAM size	Memory Size	Interface	Number of A/D Converters	Number of I2C Channels	Number of SPI Channels	Number of UART Channels	Number of Timers/ Counters
R9A07G076M48GBG	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1
R9A07G076M47GBG	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1
R9A07G076M45GBG	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1
R9A07G076M43GBG	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1

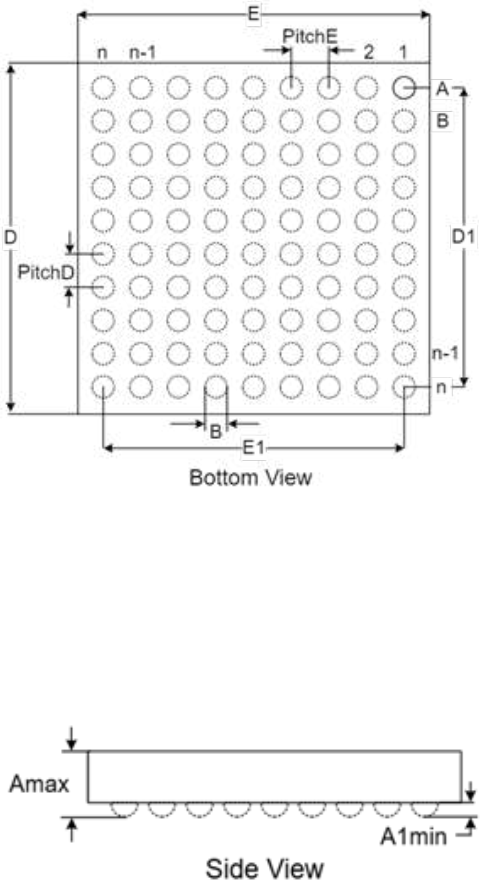
Orderable Part Number	Min Input Voltage	Max Input Voltage	Frequency	Min Operating Temperature	Max Operating Temperature	RAM size	Memory Size	Interface	Number of A/D Converters	Number of I2C Channels	Number of SPI Channels	Number of UART Channels	Number of Timers/ Counters
R9A07G076M37GBG	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1
R9A07G076M35GBG	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1
R9A07G076M30GBG	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1
R9A07G076M48GBA	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1
R9A07G076M47GBA	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1
R9A07G076M45GBA	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1

Orderable Part Number	Min Input Voltage	Max Input Voltage	Frequency	Min Operating Temperature	Max Operating Temperature	RAM size	Memory Size	Interface	Number of A/D Converters	Number of I2C Channels	Number of SPI Channels	Number of UART Channels	Number of Timers/ Counters
R9A07G076M43GBA	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1
R9A07G076M37GBA	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1
R9A07G076M35GBA	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1
R9A07G076M30GBA	1.05	1.10	1200 MHz	-40 °C	125 °C	2 MB	N/A	USB, SCI, I2C, CANFD, SPI, xSPI, SDHI, PCIE	3	3	4	0	MTU3 × 1, GPT × 6, CMT × 3, CMTW × 2, WDT × 4, RTC × 1

2.4 Footprint Design Information

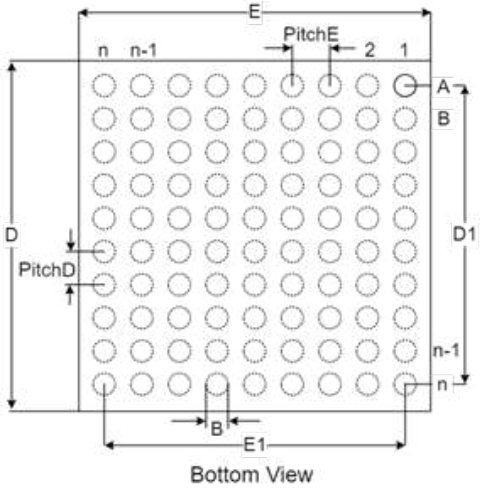
2.4.1 537-FBGA

IPC footprint type	Package Code/ POD number	Number of pins
BGA	PLBG0537GB-A	537

Description	Dimension	Value (mm)	Diagram
Minimum body Length (vertical side)	D_{min}	20.85	
Maximum body Length (vertical side)	D_{max}	21.15	
Average length of grid (vertical side)	$D1_{ave}$	19.20	
Minimum body Width (horizontal side)	E_{min}	20.85	
Maximum body Width (horizontal side)	E_{max}	21.15	
Average length of grid (horizontal side)	$E1_{ave}$	19.20	
Average ball diameter	B_{nom}	0.43	
Distance between the center of any two adjacent balls (vertical side)	PitchD	0.80	
Distance between the center of any two adjacent balls (horizontal side)	PitchE	0.80	
P = Plain Grid, S = Staggered Grid	GridType	P	
F = Full Matrix, P = Perimeter, SD = Selectively Depopulated, TE = Thermally Enhanced	MatrixType	TE	
Number of balls (vertical side)	Rows	25	
Number of balls (horizontal side)	Columns	25	
Maximum number of ball positions (Rows × Columns)	Nmax	625	
Number of actual balls present	PinCount	537	
Ball positions removed from matrix. Example: C5-H10, B6-B9, A1	Depopulate Balls	G7-W19	
Ball positions added back into depopulated matrix. Example: C8, D6-F9	Repopulate Balls	J9-U17	
Minimum Standoff Height	$A1_{min}$	0.27	
Maximum Height	A_{max}	1.45	

2.4.2 489-FBGA

IPC footprint type	Package Code/ POD number	Number of pins
BGA	PLBG0489JA-A	489

Description	Dimension	Value (mm)	Diagram
Minimum body Length (vertical side)	D_{min}	15.85	
Maximum body Length (vertical side)	D_{max}	16.15	
Average length of grid (vertical side)	$D1_{ave}$	14.30	
Minimum body Width (horizontal side)	E_{min}	15.85	
Maximum body Width (horizontal side)	E_{max}	16.15	
Average length of grid (horizontal side)	$E1_{ave}$	14.30	
Average ball diameter	B_{nom}	0.37	
Distance between the center of any two adjacent balls (vertical side)	PitchD	0.65	
Distance between the center of any two adjacent balls (horizontal side)	PitchE	0.65	
P = Plain Grid, S = Staggered Grid	GridType	P	
F = Full Matrix, P = Perimeter, SD = Selectively Depopulated, TE = Thermally Enhanced	MatrixType	TE	
Number of balls (vertical side)	Rows	23	
Number of balls (horizontal side)	Columns	23	
Maximum number of ball positions (Rows × Columns)	Nmax	529	
Number of actual balls present	PinCount	489	
Ball positions removed from matrix. Example: C5-H10, B6-B9, A1	Depopulate Balls	G7-U17	
Ball positions added back into depopulated matrix. Example: C8, D6-F9	Repopulate Balls	H8-T16	
Minimum Standoff Height	$A1_{min}$	0.22	
Maximum Height	A_{max}	1.40	

Revision History

Revision 1.00 — Dec. 5, 2025

- Initial release

Revision 1.10 — May 29, 2026

1. Overview:
- Updated 1.1 Outline of Specifications
- Updated Table 1.6 Event link
- Updated Table 1.8 Communication interfaces
- Updated Table 1.12 Security
- Updated Table 1.17 Product lineup
- Updated Figure 1.1 Block diagram
- Updated Table 1.18 Pin functions

2. Electrical Characteristics:
- Updated Table 2.3 Power on/off sequence timing
- Updated Table 2.14 IO setting (DRCTLm register setting) condition
- Updated Table 2.20 Reset, interrupt, and mode timing
- Updated Table 2.36 xSPI timing
- Updated Table 2.38 Ethernet interface timing

Appendix 2. ECAD Design Information:
- Added Appendix 2. ECAD Design Information

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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