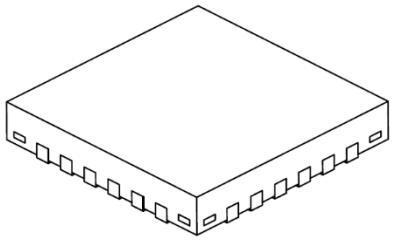
TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TCKE1401NM

75 V, 6 A eFuse IC with adjustable Overcurrent Protection

1. Description

The TCKE1401NM is a 75 V high input voltage single input-single output eFuse IC. It can be used as a reusable fuse, and includes protection features like adjustable overcurrent limit, adjustable undervoltage lockout and adjustable overvoltage protection by external resistor, short circuit protection, adjustable slew rate control by an external capacitance and thermal shutdown. With low ON resistance of 44.5 mΩ (Typ.) and high output current capability up to 6.0 A characteristics, this device is suitable for protecting the power supply circuit of fan line, storage power supply circuit and Industrial power supply applications, etc. This device is available in a small package VQFN24D (4.0 mm (Typ.) x 4.0 mm (Typ.)).



VQFN24D

Weight: 41.9 mg (Typ.)

2. Applications

48 to 54 V power line application (AI Server, PLC, Power tools etc.)

3. Features

- High input operation voltage: V_{IN} = 75 V (Max)
- Low ON resistance: R_{ON} = 44.5 mΩ (Typ.)
- Adjustable overcurrent limit by external resistor: 0.82 A to 6.43 A (Typ.)
- Adjustable overvoltage protection by external resistor
- Adjustable undervoltage lockout by external resistor
- Adjustable slew rate control by external capacitance for inrush current reduction
- Reverse current blocking by external MOSFET
- Input reverse polarity protection by external MOSFET
- 2 mode selectable overcurrent fault response between auto-retry and latch-off
- Power good output
- Flag function
- Thermal shutdown
- Small package: VQFN24D (4.0 mm (Typ.) x 4.0 mm (Typ.), t: 0.9 mm (Max)).

Start of commercial production
2026-07

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4. Block Diagram

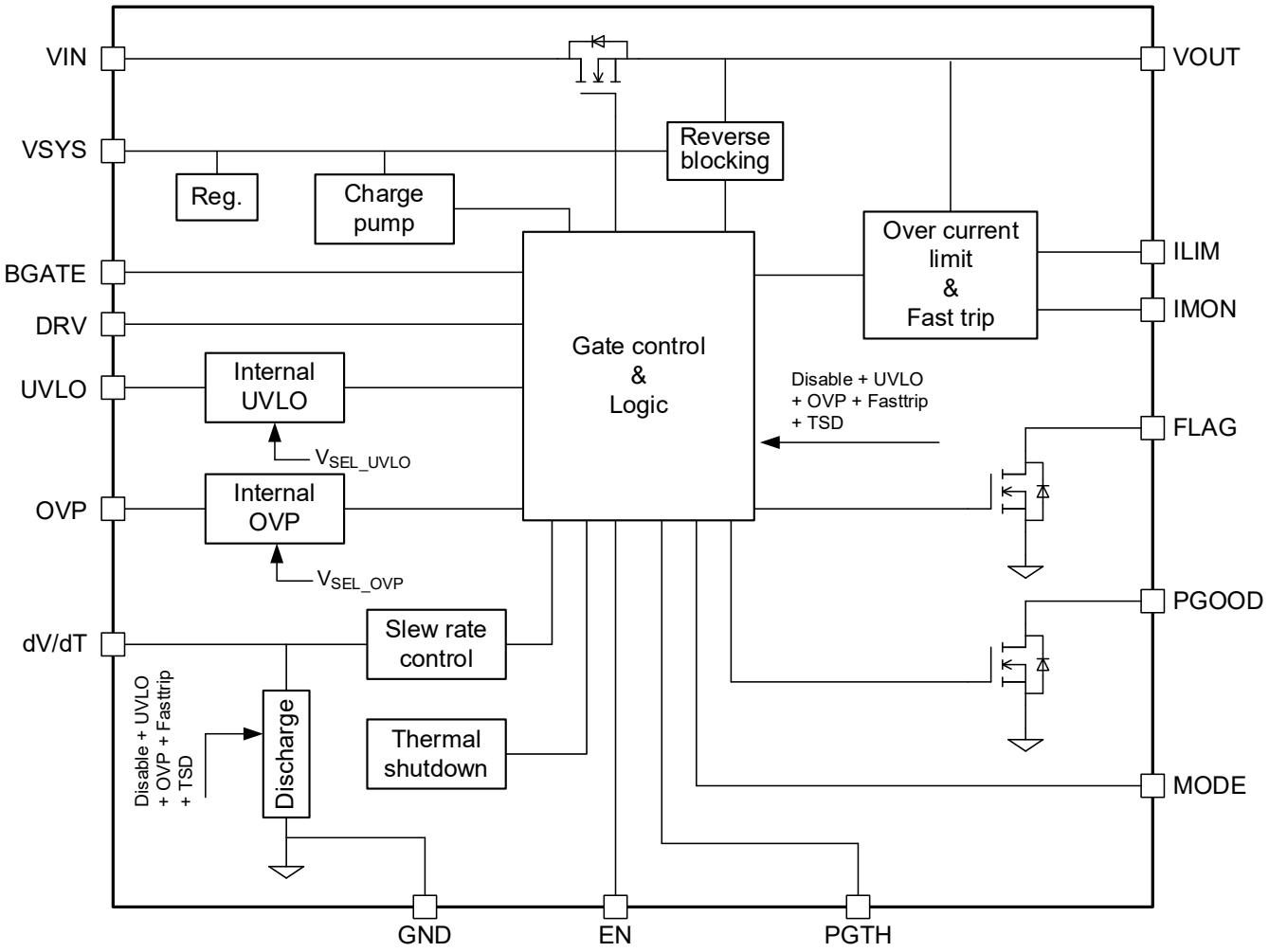


Figure 4.1 Block Diagram

Some of the functional blocks, circuits or constants labels in the block diagram may have been omitted or simplified for clarity.

5. Pin Assignments (Top view)

*Center electrode must be connected to GND or Open

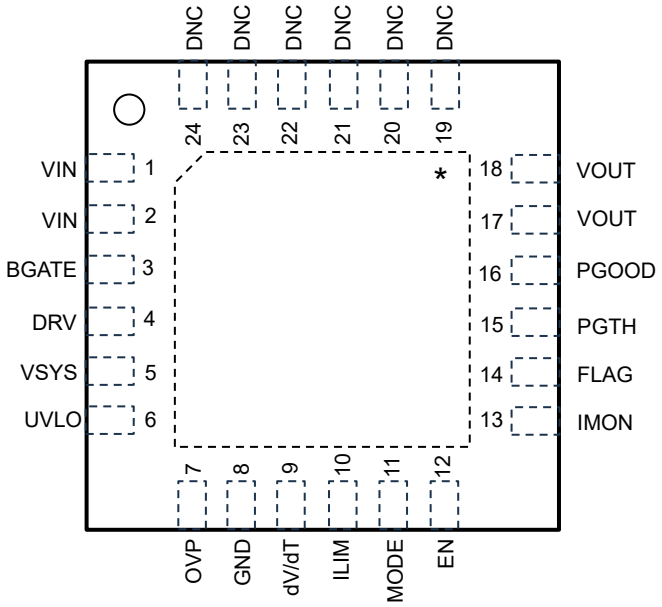
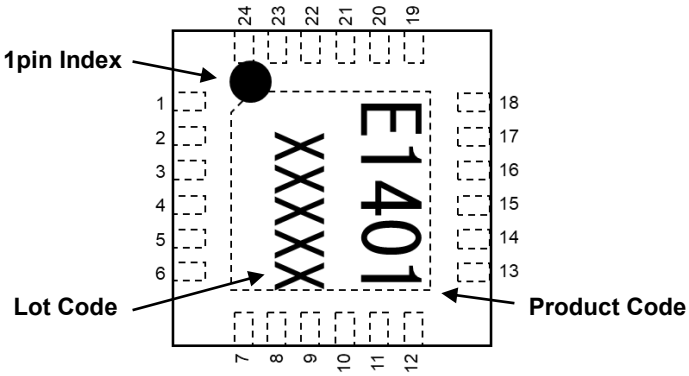


Figure 5.1 Pin Assignments

Top Marking



6. Pin Description

Table 6.1 Pin Description

PIN Name	Type (Note 1)	Description
VIN	P	Power input. Input to the power switch.
VSYS	P	Supply input. Input to the supply voltage for the device. When using the external blocking Nch MOSFET, refer to Figure 7.1 and connect VSYS to the source of the MOSFET. If the MOSFET is not used, short VSYS to VIN.
BGATE	O	Gate drive output for the external blocking Nch MOSFET. When using the MOSFET, refer to Figure 7.1 and connect this pin to the gate of the MOSFET. If the MOSFET is not used, leave this pin open.
DRV	O	Driving output for the fast pull-down Nch MOSFET. When using the MOSFET, refer to Figure 7.1 and connect this pin to the gate of the MOSFET. If the MOSFET is not used, leave this pin open.
UVLO	I	Undervoltage lockout (UVLO) input. This pin has an adjustable threshold by using external resistor. When this pin voltage falls below the threshold, the internal MOSFET turns off and the FLAG pin outputs at low level. This pin must not be left open. For operation using the internal UVLO threshold, connect this pin directly to GND.
OVP	I	Overvoltage protection (OVP) input. This pin has an adjustable threshold by using external resistor. When this pin voltage exceeds the threshold, the internal MOSFET turns off and the FLAG pin outputs at low level. This pin must not be left open. For operation using the internal OVP threshold, connect this pin directly to GND.
dV/dT	I/O	Rise time set input. A capacitor between dV/dT pin and GND sets the slew rate of V_{OUT} when the device turns on.
ILIM	I/O	Current limit set input. A resistor between ILIM pin and GND sets the current limit.
MODE	I	Mode selection pin for auto-retry or latch-off fault response. Refer to Table 7.3.
EN	I	Enable input. Active-high. If an external control is not used, this pin can be left open. In this case, this pin is internally pulled up. To reset a device that has latched off due to a fault condition, cycle this pin.
IMON	O	Current monitor output. When using the current monitor, connect a resistor between this pin and GND. If the current monitor function is not used, this pin can be left open except V_{SYS} < 9 V condition.
FLAG	O	FLAG open-drain output. This pin outputs at low level when a fault is detected. If this pin is not used, connect to GND or leave this pin open.
PGTH	I	PGOOD threshold input. This pin must not be left open.
PGOOD	O	PGOOD open-drain output. Active-high. When V_{PGTH} exceeds the V_{PGTHR} threshold, this pin outputs at high level, indicating that the output voltage is at a valid level. When V_{PGTH} falls below the V_{PGTHF} threshold, this pin outputs at low level, indicating that the output voltage has not reached a valid level. If this pin is not used, connect to GND or leave this pin open.
VOUT	P	Output. Output of the power switch.
DNC	-	Do Not Connect pin other than GND. Connect DNC to GND or leave this pin open.

Note 1: I = Input, O = Output, I/O = Input and Output, P = Power

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7. Functional Description

The TCKE1401NM is a 48 V/ 54 V industrial eFuse IC. The device protects power supplies for all systems and applications operating from 4.7 V to 75 V supplies. It also can protect power supply against reverse current blocking and reverse polarity protection by using an external MOSFET. It also includes a slew-rate control function using external capacitor, allowing controlled V_{OUT} ramp-up during hot plug events. Additionally, overcurrent limit, OVP and UVLO can be adjusted using external resistors. The effective load voltage detection threshold can be adjusted using resistors from VOUT, PGTH, and GND.

7.1. Inrush current reduction

When the output is turned on, an inrush current flows to charge the capacitor connected to the load side. If this current is too large, the overcurrent protection circuit may malfunction, making it impossible to start up.

To prevent this, this function controls the slew rate when the output voltage rises for limiting the inrush current. The output slew rate is determined by an external capacitor connected between the dV/dT pin and ground, allowing the turn-on behavior to be adjusted according to system requirements. The formula 1 and 2 for calculating the inrush current is as follows.

Formula 1 :
$$I\,(A) = C\,\frac{dV}{dT} \geq I_{INRUSH} = C_{OUT}\,\frac{V_{IN}}{t_{dV/dT}}$$

Formula 2 :
$$t_{dV/dT}\,(s) = 20.8 \times 10^{3} \times V_{IN} \times C_{dV/dT}$$

I_{INRUSH}	:	Inrush current (A)
C_{OUT}	:	Output Capacitance (F)
V_{IN}	:	Input voltage(V)
$t_{dV/dT}$	:	V_{OUT} startup time (0% to 100%) (s)
$C_{dV/dT}$	:	dV/dT pin External Capacitance (F)

7.2. Power Good (PGOOD)

The Power Good (PGOOD) function indicates whether the output voltage has reached a valid level. The PGOOD threshold level can be set by external resistors connected between VOUT, PGTH, and GND. PGOOD goes high when the internal MOSFET turns on, the output voltage rises, and V_{PGTH} exceeds V_{PGTHR}. Conversely, PGOOD pin outputs a low level when V_{PGTH} falls below V_{PGTHF}. PGOOD includes deglitch timing with t_{PGOODR} on the rising and t_{PGOODF} on the falling. PGOOD is an open-drain output and requires an external pull-up resistor. PGTH can be used to set the UVLO threshold level of the downstream power supply, and PGOOD can also be used for enable/disable control of downstream circuits.

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Table 7.1 PGOOD output status and operation of each protection function

Protective Function (Note 2)		IC Operation	PGOOD Output
Normal Operation		Normal Operation	High
Thermal Shutdown	$T_j > T_{SD}$	Shutdown	Low
Undervoltage Protection	$V_{UVLO} < V_{UVLOF}$ $V_{SYS} < V_{SYS_UVLO}$ (Note 3)	Shutdown	Low
Overvoltage Protection	$V_{OVP} > V_{OVPR}$ $V_{SYS} > V_{SYS_OVP}$ (Note 4)	Shutdown	Low
Over Current Protection (during t_{CL_PLIM})	$I_{LIM} < I_{OUT} < I_{FASTTRIP}$	I_{OUT} Current Limit	High / Low (Note 5)
Over Current Protection (after t_{CL_PLIM})	$I_{LIM} < I_{OUT} < I_{FASTTRIP}$	Shutdown	Low
Reverse Current Protection (Note 6)	$V_{OUT} - V_{SYS} \geqq 10$ mV	External MOSFET (Q1) OFF	High
Reverse connection (Note 6)	$V_{SYS} > -80$V, $V_{OUT} > -0.3$ V, $V_{SYS} - V_{OUT} \geqq -85$ V (Note 7)	Keeping OFF status	Low

Note 2: Unless otherwise specified, 4.7 V ≦ V_{SYS} = V_{IN} ≦ 75 V.
Note 3: When the UVLO pin is connected to GND, it enters internal UVLO mode.
Note 4: When the OVP pin is connected to GND, it enters internal OVP mode.
Note 5: If the PGTH pin voltage is V_{PGTHF} or higher, PGOOD output is High; if less than V_{PGTHF}, PGOOD output is Low.
Note 6: For details on the reverse current prevention function and reverse input connection prevention function, please refer to chapters 7.6 and 7.7.
Note 7: Voltage application is a condition for a 10 ms pulse.

Similar to the PGOOD function, the FLAG function notifies the IC status to external circuit. However, the FLAG function uses a detection circuit independent of the PGOOD function. Therefore, the PGOOD output does not affect the FLAG output. For details of the FLAG function, refer to chapter 7.11.

7.3. V_{OUT} sensing (PGTH)

The PGTH pin is a threshold input pin for output voltage monitoring. By connecting a resistor voltage divider from VOUT to the PGTH pin, you can set the voltage level at which the output is considered "Power Good."

The formula 3 calculating for the PGTH pin voltage based on Figure 12.1 is as follows.

$$\text{Formula 3 :} \quad V_{PGTH}\ (V) = V_{OUT} \times \frac{R5}{R4+R5}$$

When recovering from a fault condition such as OVP or UVLO, the device selects whether to turn on with a fast slew rate or in dV/dT mode based on the V_{PGTH} value. This allows the device to distinguish between actual fault conditions and transient events and control the turn-on timing accordingly.

If the V_{PGTH} level exceeds V_{PGTHF} at the time of fault recovery, the device turns on with a fast slew rate after OVP_t_{ON_fast} has elapsed, regardless of the $C_{dV/dT}$ value. This fast slew rate function becomes active approximately 500 µs after the device turns on.

If the V_{PGTH} level is below V_{PGTHF} at the time of fault recovery, the device turns on in dV/dT mode. In this case, the slew rate is determined by the capacitor connected to the dV/dT pin.

The fast turn-on feature can be disabled by connecting PGTH to GND. In this case, the PGOOD pin output remains in the low level.

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7.4. Undervoltage lockout (UVLO)

The device has adjustable undervoltage lockout (UVLO). When the voltage at UVLO pin falls below V_{UVLOF} during input undervoltage fault, the internal MOSFET turns off and the FLAG pin outputs a low level after 0.33 µs (Typ.). The UVLO comparator has a hysteresis of 70 mV (Typ.). To set the input UVLO threshold, connect a divider resistor from VIN supply to UVLO pin to GND as shown in the application circuit example (Figure 12.1). The device also has 14.84 V (Typ.) fixed threshold (V_{SYS_UVLO}) with 980 mV (Typ.) hysteresis. This feature can be enabled by connecting the UVLO pin directly to the GND pin. If the undervoltage lockout function is not needed, the UVLO pin can be connected to the VSYS pin. In this case, design the circuit with sufficient consideration of the UVLO pin rating: -0.3 V (min). UVLO pin must not be left open. If reverse polarity protection is required, connect a minimum of 300 kΩ resistor between UVLO and VSYS. The formula 4 and 5 calculating for the UVLO setpoint voltage based on Figure 12.1 is as follows.

Formula 4 :
$$V_{IN_UVLOF} = \frac{R_1 + R_2 + R_3}{R_2 + R_3} \times V_{UVLOF}$$

Formula 5 :
$$V_{IN_UVLOR} = \frac{R_1 + R_2 + R_3}{R_2 + R_3} \times V_{UVLOR}$$

V_{IN_UVLOF}	:	Input voltage at UVLO falling.
V_{UVLOF}	:	1.12 V (Typ.)
V_{IN_UVLOR}	:	Input voltage at UVLO rising.
V_{UVLOR}	:	1.19 V (Typ.)
R_1,R_2,R_3	:	Voltage divider resistor value.

7.5. Overvoltage protection (OVP)

The device has adjustable overvoltage protection (OVP). A voltage more than V_{OVPR} on OVP pin turns off the internal MOSFET and protects the downstream load. To set the OVP threshold externally, connect a divider resistor from VSYS supply to OVP pin to GND as shown in the application circuit example (Figure 12.1). The device also has 35.72 V (Typ.) fixed threshold (V_{SYS_OVP}) with a 380 mV (Typ.) hysteresis. This feature can be enabled by connecting the OVP pin directly to the GND pin. OVP pin must not be left open. The formula 6 and 7 for calculating the OVP setpoint voltage based on Figure 12.1 is as follows.

Formula 6 :
$$V_{IN_OVPF} = \frac{R_1 + R_2 + R_3}{R_3} \times V_{OVPF}$$

Formula 7 :
$$V_{IN_OVPR} = \frac{R_1 + R_2 + R_3}{R_3} \times V_{OVPR}$$

V_{IN_OVPF}	:	Input voltage at OVP falling.
V_{OVPF}	:	1.15 V (Typ.)
V_{IN_OVPR}	:	Input voltage at OVP rising.
V_{OVPR}	:	1.233 V (Typ.)
R_1,R_2,R_3	:	Voltage divider resistor value.

Upon entering overvoltage protection, the FLAG pin outputs a low level after 0.74 µs (Typ.) and remains low level until the overvoltage protection is released.

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7.6. Input reverse polarity protection (BGATE, DRV)

The input reverse polarity protection function protects the load when the input power supply is connected in reverse. If this protection is used, the external blocking Nch MOSFET (Q1) and the fast pull-down Nch MOSFET (Q2) must be connected, as shown in Figure 7.1. In this configuration, Q1 and the device are connected back-to-back on the power line, and Q2 operates as a pull-down switch for Q1. During normal operation, the gate drive voltage (V_{BGATE}) is supplied from the BGATE pin to turn on Q1.

Q2 is used as a high-speed pull-down switch, and during protection operation, it pulls down the gate voltage of Q1 to turn it off. For Q2, use an Nch MOSFET with a maximum $V_{DSS} \geq 15$ V, a maximum $V_{GSS} = \pm 20$ V, $C_{iss} \leq 50$ pF, and a gate drive voltage of 3 V or less.

When selecting the Nch MOSFETs, refer to the electrical characteristics of the BGATE and DRV pins.

If reverse polarity protection and reverse current blocking are not required, connect VSYS pin and VIN pin, and leave the BGATE and DRV pins open, as shown in Figure 7.1. (Right)

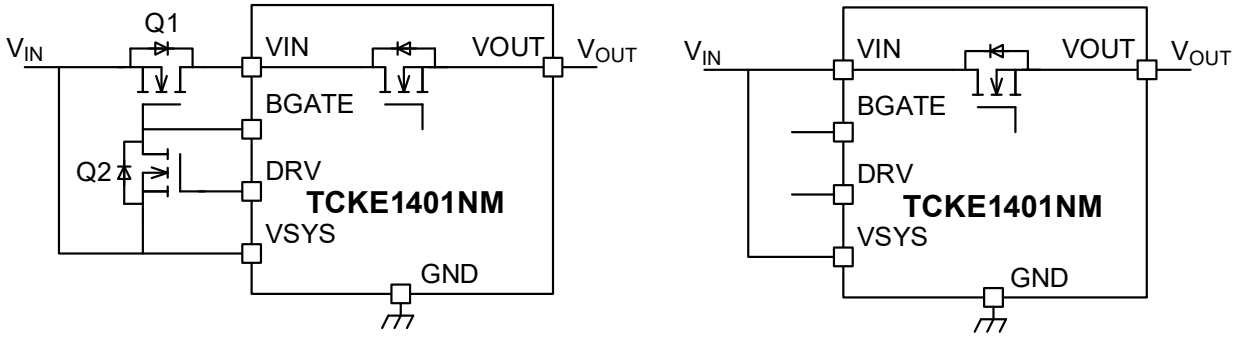


Figure 7.1 Circuit diagram for input reverse polarity protection and reverse current blocking (Left) And circuit diagram without these protections (Right).

7.7. Reverse current blocking

This device has true reverse current blocking using the external blocking Nch MOSFET Q1. When $V_{SYS} - V_{OUT}$ falls below reverse current blocking voltage threshold (V_{RB}), Q1 is turned off. The total time for Q1 to turn off under this condition is $t_{RCB_fast} + t_{Driver}$. The formula 8 for calculating the t_{Driver} is as follows.

$$\text{Formula 8:} \quad t_{Driver} = -R_{DS(ON)(Q2)} \times C_{iss(Q1)} \times \ln \frac{V_{GTH(Q1)}}{V_{BGATE}}$$

$R_{DS(ON)(Q2)}$	:	On resistance of the fast pull-down Nch MOSFET Q2
$C_{iss(Q1)}$	:	Input capacitance of Q1
$V_{GTH(Q1)}$	:	Gate threshold voltage of Q1
V_{BGATE}	:	10 V (Typ.)

Q1 turns on when the forward differential voltage $V_{SYS} - V_{OUT}$ exceeds V_{RBR}. The greater the difference in $V_{SYS} - V_{OUT}$, the faster the turn-off time t_{RCB} becomes.

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7.8. Overcurrent protection (OCL)

The overcurrent limit function prevents damage to the IC and load by suppressing power consumption in the fault event during start-up and normal operation. The formula 9 for the current limit setting as follows.

$$\text{Formula 9 :} \quad I_{LIM} = \frac{18.9}{R_{ILIM}} + 0.13$$

I_{LIM} : The overcurrent limit (A)
R_{ILIM} : The current limit resistor (kΩ)

If the load current exceeds the programmed current limit, I_{LIM}, the device regulates the current through it at I_{LIM}, eventually reducing the output voltage. The power dissipation across the device during this operation is (V_{IN} – V_{OUT}) × I_{LIM}, and this can heat up the device and eventually enter into thermal shutdown. The maximum duration for the overcurrent through the internal MOSFET (t_{CL_PLIM}) is 160 ms (Typ.). If the thermal shutdown occurs before this time, the internal MOSFET turns off and the fault response (auto-retry or latch-off) depends on the MODE pin state in Table 7.3.

7.9. Short circuit protection

To respond to the rapid increase in current caused by an output short circuit, the device has a fast-trip comparator. This comparator is designed for fast turn off t_{SCP} = 1 µs (Typ.) with I_{SCP} = 45 A (Typ.) of the internal MOSFET during an output short-circuit event. The fast-trip threshold is internally set to $I_{FASTTRIP}$. The fast-trip circuit holds the internal MOSFET off for only a few microseconds, after which the device turns back on slowly, it transitions to OCL operation under ILIM limiting.

This behavior is achieved by controlling the turn off time of the internal MOSFET based on the overcurrent level, $I_{FASTTRIP}$, through the device. The higher the overcurrent, the faster the turn off time, $t_{FASTTRIP}$. At overcurrent level in the range of $I_{FASTTRIP}$ < I_{OUT} < I_{SCP}, the fast-trip comparator response is 3 µs (Typ.).

7.10. Output current monitor (IMON)

The IMON pin is the output current monitor as an analog voltage. The current source at the IMON pin is proportional to the current flowing from VIN to VOUT. This current is converted to a voltage by the resistor R_{IMON} connected from the IMON pin to the GND pin. The maximum voltage for current monitoring (V_{IMON} max) is limited to 4 V (9 V ≤ V_{SYS} = V_{IN}) or 2 V (V_{SYS} = V_{IN} < 9 V). The formula 10 for calculating the R_{IMON} value to ensure V_{IMON} max is not exceeded is as follows. A capacitor must not connect to the IMON pin, as it will degrade the current monitor tracking performance. If the output current monitor is not used, the IMON pin can be left open except V_{SYS} < 9 V condition.

$$\text{Formula 10 :} \quad V_{IMON} = [I_{OUT} \times G_{IMON}] \times R_{IMON}$$

G_{IMON} : The gain factor IMON/ I_{OUT} = 27.9 µA/A (Typ.)
I_{OUT} : Output current (A)

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7.11. FAULT response (FLAG)

The FLAG pin outputs a low level when this device detects fault conditions such as undervoltage lockout, overvoltage protection, overcurrent protection, reverse current blocking, ILIM pin short, and thermal shutdown. An internal deglitch circuit is implemented to prevent false triggering during fault conditions. The FLAG pin can be left open or connected to GND when not used.

Table 7.2 Target functions and operations of FLAG output

Protective Function (Note 2)		IC Operation	FLAG Output
Normal Operation		Normal Operation	High
Thermal Shutdown	$T_j > T_{SD}$	Shutdown	Low
Undervoltage Protection	$V_{UVLO} < V_{UVLOF}$ $V_{SYS} < V_{SYS_UVLO}$ (Note 3)	Shutdown	Low
Overvoltage Protection	$V_{OVP} > V_{OVPR}$ $V_{SYS} > V_{SYS_OVP}$ (Note 4)	Shutdown	Low
Over Current Protection	$I_{LIM} < I_{OUT} < I_{FASTTRIP}$ $t_{CL_PLIM_FLAG} < t_{CL_PLIM}$	I_{OUT} Current Limit	Low
Reverse Current Protection (Note 6)	$V_{OUT} - V_{SYS} \geqq 10$ mV	External MOSFET (Q1) OFF	Low
Reverse connection (Note 6)	$V_{SYS} > -80$ V, $V_{OUT} > -0.3$ V, $V_{SYS} - V_{OUT} \geqq -85$ V (Note 7)	Maintaining OFF status	Indefinite

Note 2: Unless otherwise specified, the condition is 4.7 V ≦ V_{SYS} = VIN ≦ 75 V.
Note 3: When the UVLO pin is connected to GND, it enters internal UVLO mode.
Note 4: When the OVP pin is connected to GND, it enters internal OVP mode.
Note 6: For details on the reverse current prevention function and reverse input connection prevention function, please refer to chapter 7.6 and 7.7.
Note 7: Voltage application is a condition for a 10 ms pulse.

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7.12. VSYS, VIN and GND pins

Connect a capacitor between VSYS pin and GND pin to remain stable the V_{SYS} supply.
When using reverse polarity protection and reverse current blocking, connect external MOSFETs Q1 and Q2. Refer to Figure 7.1 for the connection method.

7.13. Thermal shutdown (TSD)

The overheat protection function (thermal shutdown) stops IC operation and transitions to the shutdown state when the junction temperature (T_j) of the device exceeds the set value due to continuously high current output. After the thermal shutdown event, depending on the mode of fault response (auto-retry or latch-off) mentioned as per Table 7.3, the device either latches off or initiates an auto-retry cycle of t_{TSD_retry} = 330 ms (Typ.) after T_j <140°C (Typ.).

7.14. External control (EN)

The EN pin is used to input an external control signal. When this pin is left open, it is internally pulled up to a high level. To set the EN pin to a low level, it must be below 0.8 V. When an external signal is applied to set the EN pin high, the voltage must be 2 V or higher.

7.15. Mode pin setting

The device can change the fault response depending on the MODE pin state. Refer to Table 7.3 for the MODE pin state.

Table 7.3 Fault response setting

MODE pin state	Fault response
Open	After the abnormal state, the eFuse IC will latch off. To restart the eFuse IC, either apply the EN pin again, set the VSYS pin input voltage to 0 V once and then apply again, or lower the UVLO pin voltage below V_{UVLOF} and recover from UVLO state.
Shorted to GND	Auto-retry mode with t_{TSD_retry}.

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8. Absolute Maximum Ratings

Table 8.1 Absolute Maximum Ratings (Note 8)

(T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Rating	Unit
VSYS		V_{SYS}	-80 to 80	V
VIN, VOUT, UVLO, FLAG, PGOOD, PGTH		V_{IN}, V_{OUT}, V_{UVLO}, V_{FLAG}, V_{PGOOD}, V_{PGTH}	-0.3 to 80	V
VSYS – VOUT with the external blocking MOSFET (10 ms Pulse)		V_{SYS} - V_{OUT}	-85 (Min)	V
BGATE		V_{BGATE}	-80 to 94	V
BGATE - VSYS		V_{BGATE} - V_{SYS}	-0.3 to 14	V
DRV		V_{DRV}	-80 to 85	V
DRV - VSYS		V_{DRV} - V_{SYS}	-0.3 to 6	V
OVP, dV/dT, IMON, MODE, EN, ILIM		V_{OVP}, $V_{dV/dT}$, V_{IMON}, V_{MODE}, V_{EN}	-0.3 to 6	V
		V_{ILIM}	Internally limited	V
Sink current	FLAG, dV/dT, PGOOD	I_{FLAG}, $I_{dV/dT}$, I_{PGOOD}	0 to 10	mA
Source current	dV/dT, ILIM, MODE, EN	$I_{dV/dT}$, I_{ILIM}, I_{MODE}, I_{EN}	Internally limited	A
Power dissipation		P_D	2.2 (Note 9)	W
Junction temperature		T_j	150	°C
Storage temperature		T_{stg}	-55 to 150	°C

Note 8: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 9: Rating at mounting on a board: FR4 board. (76.2 mm × 114.3 mm × 1.6 mm, 4 layer)

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9. Operating Ranges

Table 9.1 Operating Ranges

Characteristics	Symbol	Ranges		Unit
Input voltage	V_{SYS}, V_{IN}	4.7 to 75		V
UVLO, FLAG, PGOOD, PGTH	V_{UVLO}, V_{FLAG}, V_{PGOOD}, V_{PGTH}	0 to 75		V
OVP, MODE	V_{OVP}, V_{MODE}	0 to 4		V
IMON	V_{IMON}	9 V ≤ V_{SYS} = V_{IN}	0 to 4	V
		V_{SYS} = V_{IN} < 9 V	0 to 2	V
dV/dT	$V_{dV/dT}$	0 to 3		V
EN pin voltage	V_{EN}	0 to 5		V
ILIM External resistance	R_{ILIM}	3 to 30		kΩ
IMON External resistance	R_{IMON}	1 (Min) (Note 10)		kΩ
Input external capacitance	C_{VSYS}, C_{IN}	0.1 (Min)		μF
Operation junction temperature	T_{j_opr}	-40 to 125		°C
dV/dT external capacitance	$C_{dV/dT}$	10 (Min)		nF

Note 10: Please refer to Current monitor gain (G_{IMON}) and use it within V_{IMON} operating range.

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10. Electrical Characteristics

Table 10.1 DC Characteristics (1)

(Unless otherwise specified, T_a = -40°C to 125°C, 4.7 V ≤ V_{SYS} = V_{IN} ≤ 75 V, V_{EN} = 2 V, R_{ILIM} = 30 kΩ)

Characteristics	Symbol	Test Condition		T_a = 25°C			T_a = -40 to 125°C (Note 12)		Unit
				Min	Typ.	Max	Min	Max	
Basic operation									
On resistance (Note 11)	R_{ON}	0.6 A ≤ I_{OUT} ≤ 6 A		—	44.5	—	—	80	mΩ
Quiescent current (ON state)	I_Q	V_{EN} = 2 V		—	0.5	—	—	1.2	mA
Quiescent current (OFF state)	$I_{Q(OFF)}$	V_{EN} = 0 V		—	41	—	—	79	μA
Ground current during reverse polarity	I_{GND}	V_{SYS} = -24 V, V_{IN} = Open, V_{OUT} = 0 V		—	144	—	—	200	μA
UVLO									
Fixed V_{SYS} undervoltage lockout (UVLO) threshold	V_{SYS_UVLO}	V_{SYS} rising, V_{UVLO} = 0 V		—	15.82	—	14.61	23.62	V
		V_{SYS} falling, V_{UVLO} = 0 V		—	14.84	—	13.45	22.23	V
Undervoltage lockout threshold	V_{UVLOR}	Rising		—	1.19	—	1.142	1.224	V
	V_{UVLOF}	Falling		—	1.12	—	1.039	1.15	V
Internal UVLO select threshold	V_{SEL_UVLO}			—	213	—	153.2	272.8	mV
UVLO leak current	I_{UVLO}	0 V ≤ V_{UVLO} ≤ 75 V		—	8	—	-320	320	nA
OVP									
Fixed V_{SYS} overvoltage protection (OVP) threshold	V_{SYS_OVP}	V_{SYS} rising, V_{OVP} = 0 V		—	35.72	—	33.11	45.93	V
		V_{SYS} falling, V_{OVP} = 0 V		—	35.34	—	32.74	45.46	V
Overvoltage protection threshold	V_{OVPR}	Rising		—	1.233	—	1.18	1.298	V
	V_{OVPF}	Falling		—	1.15	—	1.09	1.187	V
Internal OVP select threshold	V_{SEL_OVP}			—	216	—	167	265	mV
OVP leak current	I_{OVP}	0 V ≤ V_{OVP} ≤ 4 V		—	0	—	-320	320	nA
ILIM (Note 13)									
Overcurrent limit (Note 11)	I_{LIM}	V_{IN} – V_{OUT} = 1 V	R_{ILIM} = 30 kΩ	—	0.82	—	0.54	1.10	A
			R_{ILIM} = 9 kΩ	—	2.21	—	1.84	2.59	A
			R_{ILIM} = 4.02 kΩ	—	4.83	—	4.18	5.47	A
			R_{ILIM} = 3 kΩ	—	6.43	—	5.58	7.28	A
Fast trip comparator level	$I_{FASTTRIP}$			—	I_{LIM} × 2.0	—	—	—	A
Short circuit protect current	I_{SCP}	4.7 V ≤ V_{SYS} = V_{IN} ≤ 75 V		—	45	—	—	—	A

Note 11: Pulsed testing techniques used during this test maintain junction temperature approximately equal to ambient temperature.

Note 12: This parameter is warranted by design.

Note 13: IMON pin can be left open when the IMON function is not used, except V_{SYS} < 9 V (1 kΩ ≤ R_{IMON} ≤ 10 kΩ).

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Table 10.2 DC Characteristics (2)

(Unless otherwise specified, T_a = -40°C to 125°C, 4.7 V ≤ V_{SYS} = V_{IN} ≤ 75 V, V_{EN} = 2 V, R_{ILIM} = 30 kΩ)

Characteristics	Symbol	Test Condition	T_a = 25°C			T_a = -40 to 125°C (Note 12)		Unit
			Min	Typ.	Max	Min	Max	
BGATE								
BGATE output voltage	V_{BGATE}		—	V_{SYS} +10	—	V_{SYS} +8	V_{SYS} +14	V
BGATE charging current	I_{BGATE}	$V_{BGATE} - V_{SYS}$ = 1 V	—	22	—	16	25	μA
BGATE pulldown resistance (Note 14)	R_{BGATE}		—	—	—	—	16	MΩ
DRV								
DRV output voltage	V_{DRV}	C_{DRV} ≤ 50 pF	—	V_{SYS} +4.5	—	V_{SYS} +3.0	V_{SYS} +5.2	V
Reverse current protection								
Reverse current blocking voltage threshold	V_{RB}	$V_{SYS} - V_{OUT}$	—	-15	—	-45	-3	mV
Reverse current blocking release voltage threshold	V_{RBR}	$V_{SYS} - V_{OUT}$	—	61	—	28	82	mV
Reverse current blocking leak current	I_{RB}	V_{SYS} = 0 V, V_{OUT} = 24 V	—	—	—	-100	—	μA
dV/dT								
dVdT charging current	$I_{dV/dT}$	$V_{dV/dT}$ = 0 V	—	1.5	—	1.33	1.67	μA
dVdT to V_{OUT} gain ($V_{OUT}/V_{dV/dT}$)	$G_{dV/dT}$		—	32	—	30	34	V/V
dVdT maximum capacitor voltage	$V_{dV/dT}$		—	3.0	—	2.8	3.2	V
dVdT discharging resistance	$R_{dV/dT}$		—	5.5	—	2.2	22.7	Ω
EN								
EN voltage (ON)	V_{EN_ON}		—	—	—	2	5	V
EN voltage (OFF)	V_{EN_OFF}		—	—	—	0	0.8	V
EN pullup voltage	V_{ENUP}	I_{EN} = -20 nA	—	3.2	—	2	4.6	V
EN leak current	I_{EN}	V_{EN} = 0 V	—	—	—	-10	—	μA
IMON								
Current monitor gain (I_{IMON}/I_{OUT})	G_{IMON}	0.6 A ≤ I_{OUT} < 1 A < I_{LIM}	—	27.9	—	17.58	38.22	μA/A
		1 A ≤ I_{OUT} < 2 A < I_{LIM}	—	27.9	—	22.3	33.5	μA/A
		2 A ≤ I_{OUT} < 4.5 A < I_{LIM}	—	27.9	—	23.9	31.9	μA/A
		4.5 A ≤ I_{OUT} < 6 A < I_{LIM}	—	27.9	—	24.4	31.4	μA/A
		6 A ≤ I_{OUT} < I_{LIM}	—	27.9	—	25.0	30.8	μA/A
FLAG								
FLAG pin pulldown resistance	R_{FLAG}	I_{FLAG} = 1 mA, FLAG = L	—	16	—	5	40	Ω
FLAG leak current	I_{FLAG}	0 V ≤ V_{FLAG} ≤ 75 V	—	6	—	-320	320	nA
PGOOD								
PGOOD pin pulldown resistance	R_{PGOOD}	I_{PGOOD} = 1 mA, PGOOD = L	—	16	—	5	40	Ω
PGOOD leak current	I_{PGOOD}	0 V ≤ V_{PGOOD} ≤ 75 V	—	—	—	-320	320	nA
PGTH								
PGTH threshold voltage rising	V_{PGTHR}		—	1.17	—	1.13	1.22	V
PGTH threshold voltage falling	V_{PGTHF}		—	1.11	—	1.06	1.15	V
PGTH leak current	I_{PGTH}	0 V ≤ V_{PGTH} ≤ 75 V	—	—	—	-320	320	nA
Thermal shutdown Protection (Note 14)								
Thermal shutdown threshold	T_{SD}	T_j	—	165	—	—	—	°C
Thermal shutdown hysteresis	T_{SDH}	T_j	—	20	—	—	—	°C

Note 12: This parameter is warranted by design.
Note 14: This parameter is reference only.

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Table 10.3 AC Characteristics (1)

(Unless otherwise specified, T_a = -40°C to 125°C, 4.7 V ≤ V_{SYS} = V_{IN} ≤ 75 V, R_{ILIM} = 30 kΩ, V_{EN} = 2 V, C_{OUT} = 1 µF)

Characteristics	Symbol	Test Condition			T_a = -40 to 125°C (Note 12)			Unit
					Min	Typ.	Max	
UVLO switch turn on delay	UVLO_t_{on}	UVLO = H (100 mV above V_{UVLOR}) to V_{OUT} = 100 mV with V_{PGTH} < V_{PGTHF}, $C_{dV/dT}$ ≥ 10 nF, [$C_{dV/dT}$ in nF]			—	220 + 14.5 × $C_{dV/dT}$	—	µs
UVLO switch turn on delay (fast)	UVLO_t_{on_fast}	UVLO = H (100 mV above V_{UVLOR}) to MOSFET ON with V_{PGTH} > V_{PGTHF}			—	195	410	µs
UVLO switch turnoff delay	UVLO_t_{off}	UVLO = L (20 mV below V_{UVLOF}) to FLAG = L			—	0.33	3	µs
UVLO to fault de-assertion delay	UVLO_t_{FLAG}	UVLO = H to FLAG = H delay			382	580	772	µs
OVP switch turn off delay	OVP_t_{off}	OVP = H (20 mV above V_{OVPR}) to FLAG = L			—	0.74	3	µs
OVP switch turn on delay (fast)	OVP_t_{on_fast}	OVP = L (100 mV below V_{OVPF}) to MOSFET ON with V_{PGTH} > V_{PGTHF}			—	165	374	µs
OVP switch disable delay	OVP_t_{on}	OVP = L (100 mV below V_{OVPF}) to MOSFET ON with V_{PGTH} < V_{PGTHF}, $C_{dV/dT}$ ≥ 10 nF, [$C_{dV/dT}$ in nF]			—	190 + 14.5 × $C_{dV/dT}$	—	µs
Shutdown delay	$t_{Shutdown}$	V_{EN} = L (below V_{EN_OFF}) to MOSFET OFF, V_{IN} = 48 V			0.35	0.64	2	µs
Fast trip response time	$t_{FASTTRIP}$	$I_{FASTTRIP}$ < I_{OUT} = I_{LIM} × 3 < I_{SCP}, I_{OUT} > I_{LIM} × 2 to I_{OUT} = I_{LIM} × 1	3 kΩ ≤ R_{ILIM} ≤ 6 kΩ	V_{IN} = 24 V	—	3	5.2	µs
				V_{IN} = 48 V	—	3	5.2	µs
			6 kΩ < R_{ILIM} ≤ 30 kΩ	V_{IN} = 24 V	—	4	8	µs
				V_{IN} = 48 V	—	4	8	µs
	t_{SCP}	I_{OUT} > I_{SCP} to V_{OUT} = 0 V			—	1	—	µs
Current limit response time	t_{LIM}	T_a = 25°C, I_{OUT} > I_{LIM} to I_{OUT} = I_{LIM}, I_{LIM} (Typ.) × 1.4 < I_{OUT} < $I_{FASTTRIP}$			—	100	150	µs
Maximum duration in current limit	t_{CL_PLIM}	I_{LIM} < I_{OUT} < $I_{FASTTRIP}$ to V_{OUT} = 0 V			130	160	190	ms
FLAG delay in current limit	$t_{CL_PLIM_FLAG}$	I_{LIM} (Typ.) ×1.4 < I_{OUT} < $I_{FASTTRIP}$		12 V ≤ V_{IN} ≤ 75 V	1.0	1.9	3.5	ms
				4.7 V ≤ V_{IN} < 12 V	1.0	2.2	5	ms

Note 12: This parameter is warranted by design.

Table 10.4 AC Characteristics (2)

(Unless otherwise specified, T_a = -40°C to 125°C, 4.7 V ≤ V_{SYS} = V_{IN} ≤ 75 V, R_{ILIM} = 30 kΩ, V_{EN} = 2 V, C_{OUT} = 1 µF)

Characteristics	Symbol	Test Condition		T_a = -40 to 125°C (Note 12)			Unit
				Min	Typ.	Max	
Retry delay in TSD	t_{TSD_retry}	MODE = GND		230	330	430	ms
IC startup time	t_{start}	V_{SYS} = V_{IN} = 4.7 V × 90% to V_{OUT} = 4.7 V × 50% during a ramp-up to ≥ 4.7 V, V_{EN} = H (above V_{EN_ON}), UVLO = H (100 mV above V_{UVLOR}), OVP = L (100 mV below V_{OVPF})		—	291 + 57.5 × $C_{dV/dT}$	—	µs
V_{OUT} rise time (10% to 90%)	t_r	$C_{dV/dT}$ = OPEN	V_{IN} = 24 V	450	595	800	µs
		$C_{dV/dT}$ = 22 nF	V_{IN} = 24 V	6.68	8.35	11.69	ms
PGOOD delay (deglitch) time	t_{PGOODR}	Rising edge		0.89	1.3	1.8	ms
	t_{PGOODF}	Falling edge, PGTH = L (10mV below V_{PGTHF})		1.3	2.5	4.0	µs
Reverse protection comparator detection delay (reverse)	t_{RCB_fast}	(V_{SYS} – V_{OUT})↓ (1 V overdrive below V_{RB}) to V_{DRV} - V_{SYS} = 3 V		—	1.4	3.0	µs
	t_{RCB}	(V_{SYS} – V_{OUT})↓ (10 mV overdrive below V_{RB}) to V_{DRV} - V_{SYS} = 3 V		—	2.3	7	µs
Fault assertion delay in Reverse current blocking	t_{RCB_FLAG}	(V_{SYS} – V_{OUT})↓ (10 mV overdrive below V_{RB}) to FLAG = L		368	550	743	µs
Reverse protection comparator detection delay (forward)	t_{FWD_FLAG}	(V_{SYS} – V_{OUT})↑ (10 mV overdrive above V_{RBR}) to (V_{BGATE} – V_{SYS}) = 5 V, $C_{BGATE-VSYS}$ = 3.6 nF		0.45	1.8	3.33	ms
Fault de-assertion delay		(V_{SYS} – V_{OUT})↑ (10 mV overdrive above V_{RBR}) to FLAG = H		457	690	923	µs

Note 12: This parameter is warranted by design.

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11. Timing waveform

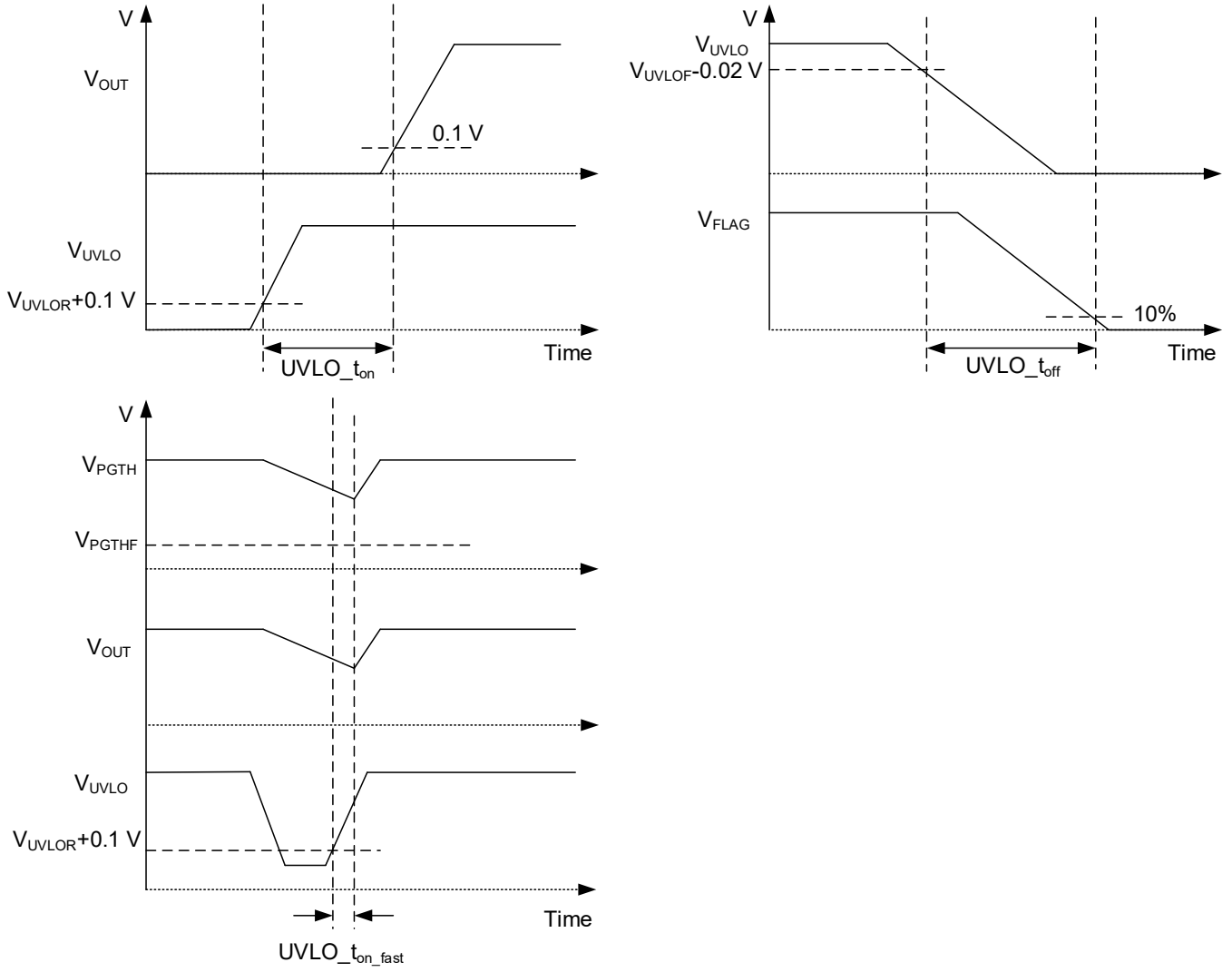


Figure 11.1 UVLO characteristics

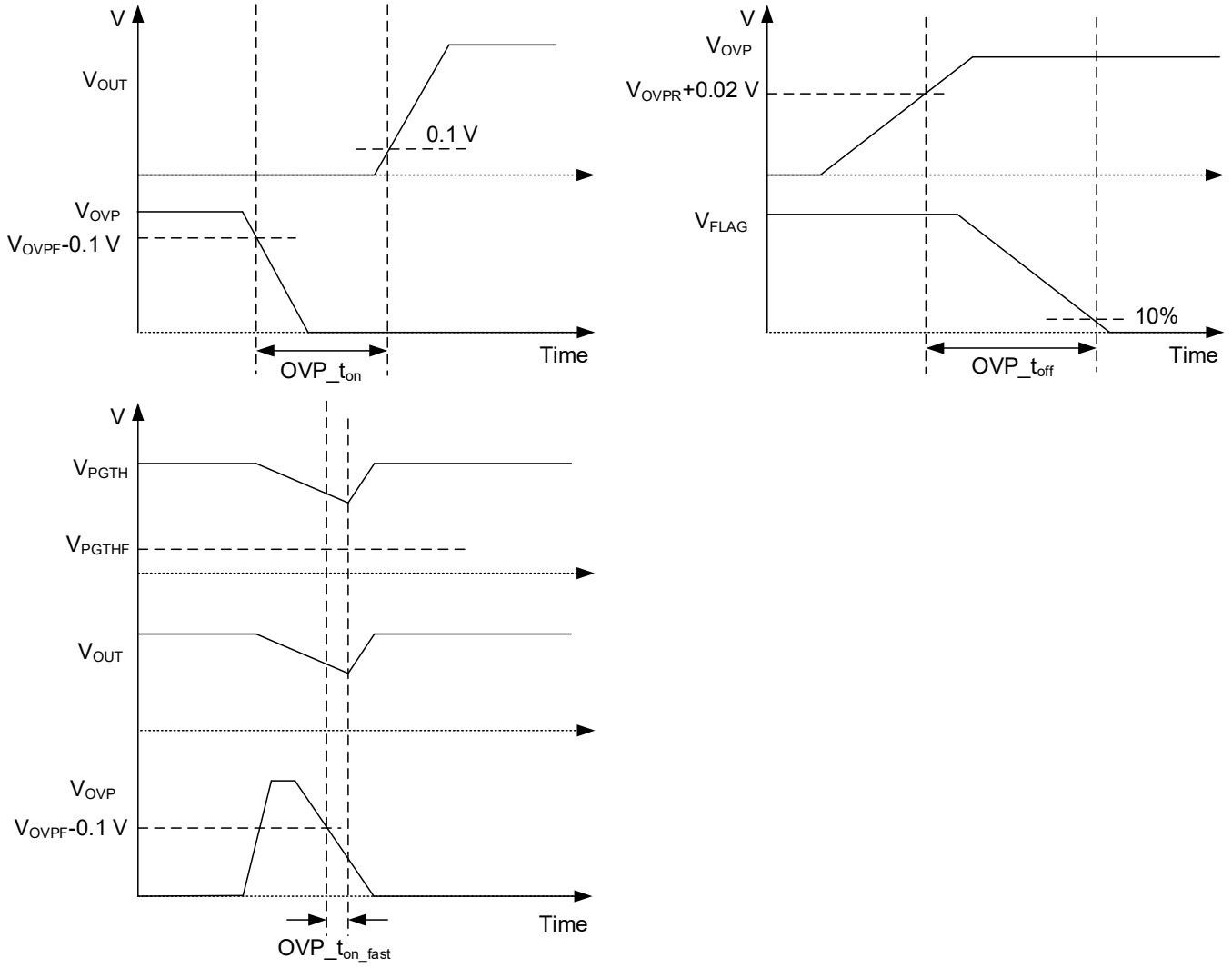


Figure 11.2 OVP characteristics

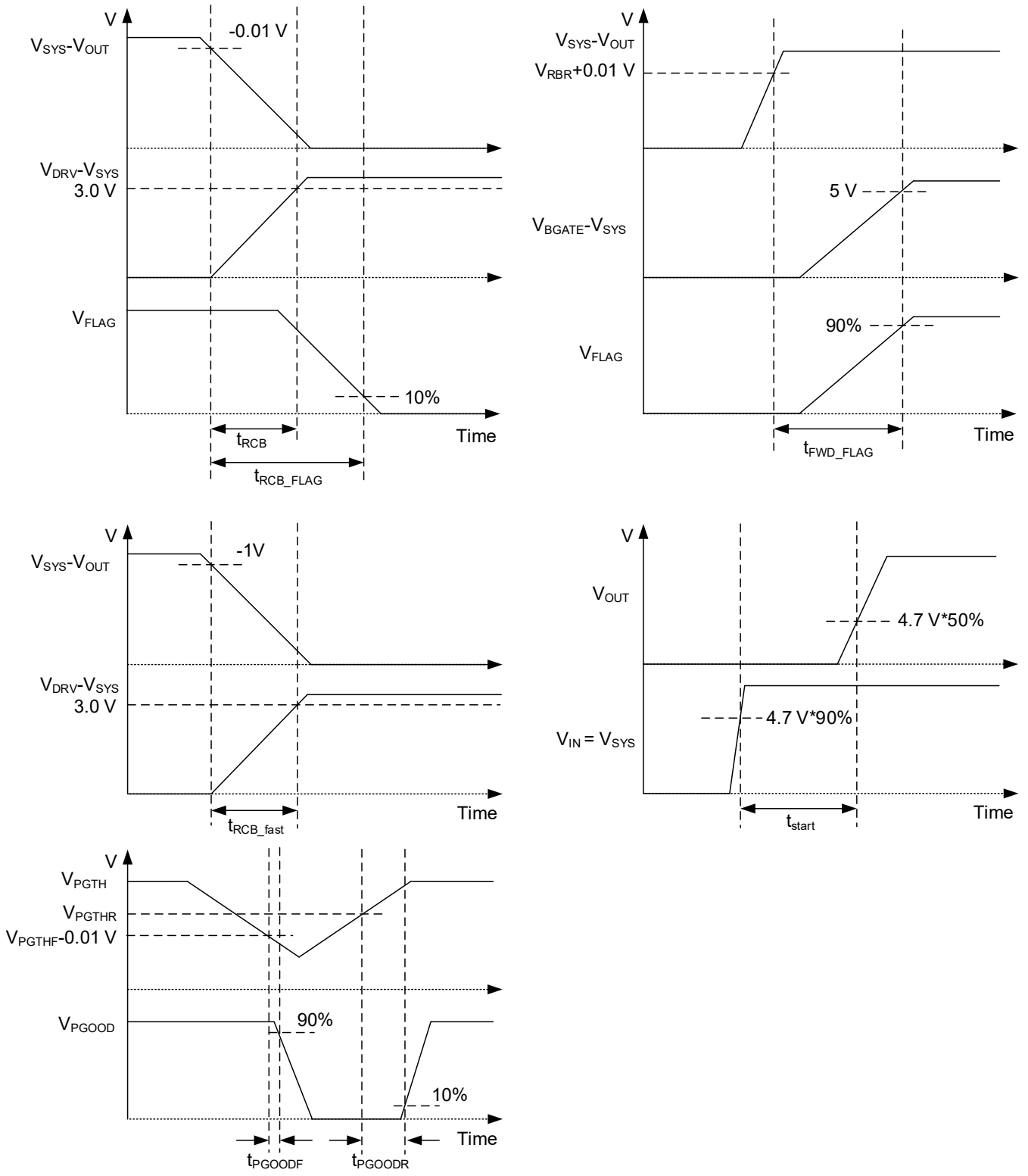


Figure 11.3 Other characteristics

12. Application Note

12.1. Application circuit example

Figure 12.1 shows the application circuit example under 48 V power line condition. Connect the power supply to the VIN pin and VSYS pin. During normal operation, almost the same voltage as the VIN voltage is output from the VOUT pin through the MOSFET. If the current suddenly decreases, for example, when short-circuiting or overcurrent is protected, high-spike voltages may be generated due to back electromotive force of inductance components such as wirings connected to the input/output pins of the eFuse IC, causing damage to the eFuse IC and resulting destruction. In this case, a positive spike voltage is generated on the input side and a negative spike voltage is generated on the output side. When designing boards, design patterns so that the length of the wires on the input-side and output-side of the eFuse IC is as short as possible. Also, the GND wiring area should be as wide as possible to reduce the impedance.

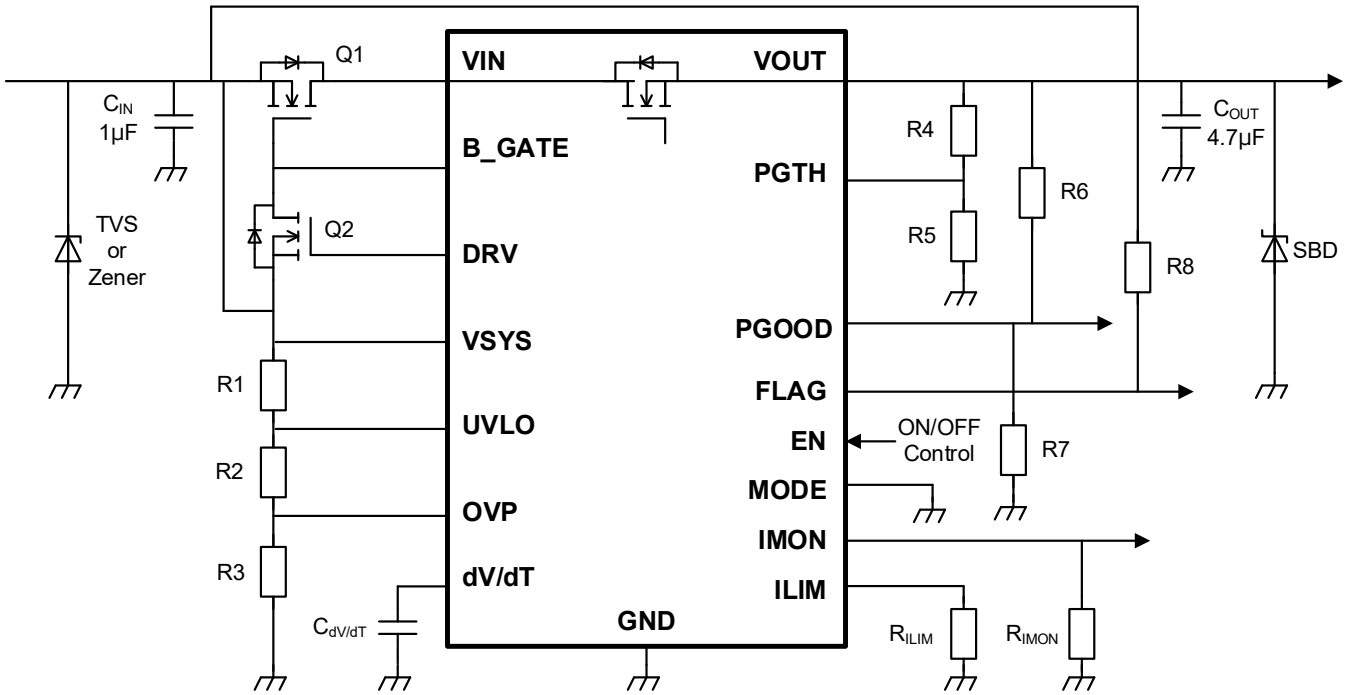


Figure 12.1 application circuit example under 48 V power line condition

C_{IN} functions to suppress the peak value against the positive spike voltage generated by the inputs. A C_{IN} of at least 0.1 µF is recommended for this device, but the appropriate capacitor value should be determined based on operation on the actual PCB board. The peak value V_{SPIKE} of the spike voltage and the capacitance value of the C_{IN} have the following relationship. It can be understood that the spike voltage can be reduced by increasing the C_{IN}, and it is determined by formula 11.

$$\text{Formula 11 :} \quad V_{SPIKE} = V_{IN} + I_{OUT} \times \sqrt{\frac{L_{IN}}{C_{IN}}}$$

V_{SPIKE}	:	Peak value of spiked voltage generated (V)
V_{IN}	:	Power supply voltage during normal operation (V)
I_{OUT}	:	Output current (A)
L_{IN}	:	Effective inductance component of the input pin (H)
C_{IN}	:	Input capacity (F)

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If V_{IN} is high, V_{OUT} is also high, and the current change during short-circuit or overcurrent protection is large, causing unstable operation due to unstable V_{IN} and V_{OUT} and possibly leading to IC destruction. If transient voltages exceeding the absolute maximum ratings are applied to the VIN pin, connect a TVS diode (ESD protection diode) or a Zener diode between the input pins and GND. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS or a Zener diode can help to absorb the excessive energy dump and prevent the device from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

For negative spike voltages generated on the output side, such as during short-circuit protection operation, connect an SBD (Schottky barrier diode) between the output pin and GND. This will prevent the output potential from dropping significantly below GND.

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12.2. Attention in Use

- **Absolute maximum ratings**
  The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.

- **Input/ Output capacitors**
  Ceramic capacitors can be used with the IC, however some type capacitors may have very large temperature dependence. Please consider usage environment conditions carefully to select the capacitors.

- **Mounting**
  The long distance between IC and C_{OUT} might affect phase assurance by impedance in wire and inductor. For stable power supply, C_{OUT} needs to mount near IC as much as possible. Also, VIN and GND patterns need to be large and make the wire impedance small as possible.

- **VSYS pin**
  The VSYS pin is the power supply pin for the device's internal circuit. To prevent unexpected behavior, we recommend designing the system so that a stable power supply is provided to this pin, taking into consideration C_{IN}, C_{OUT}, and impedance.

- **Maximum permissible loss and output current**
  Please have enough design margin for expected maximum permissible loss and output current. And under consideration of surrounding temperature, input voltage etc., we recommend proper dissipation ratings for maximum permissible loss and output current; in general, maximum dissipation rating is 70 to 80 %.

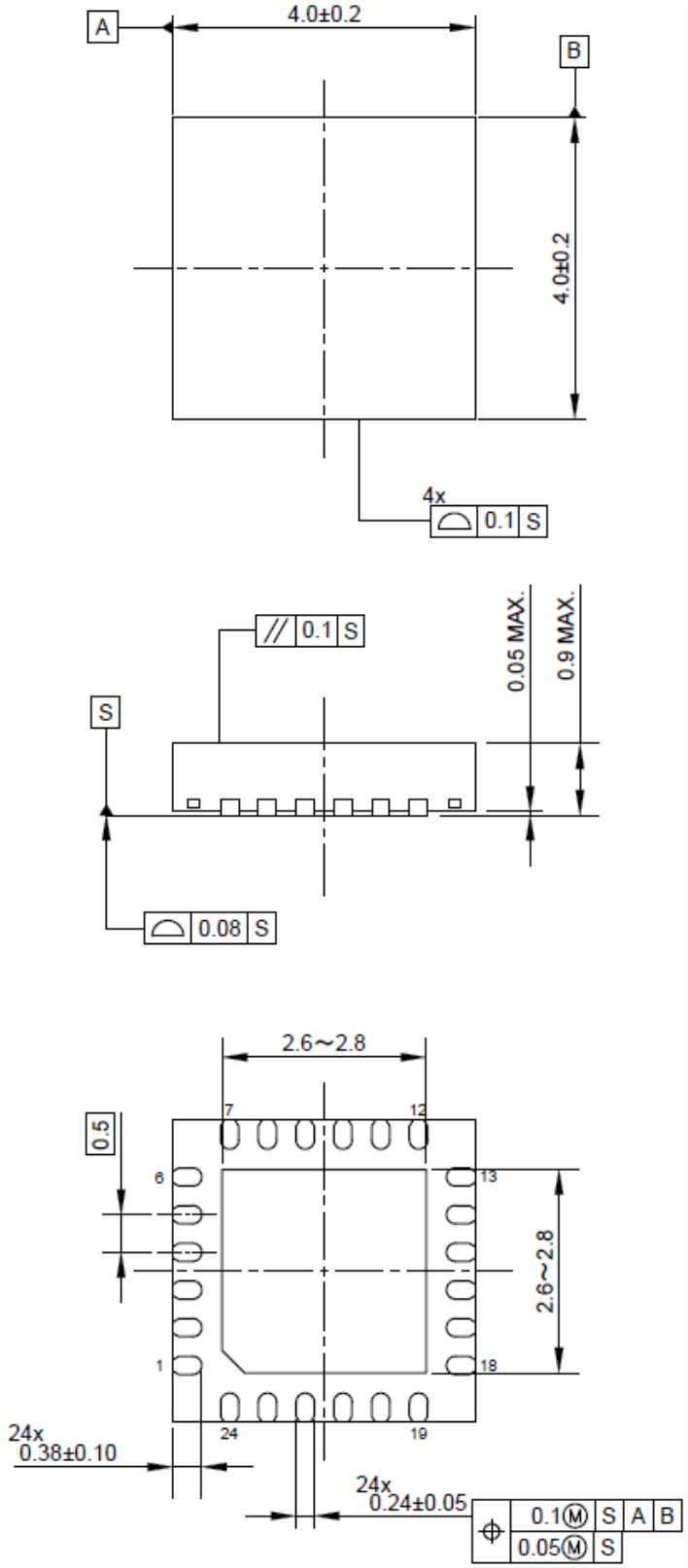
- **Protection circuit**
  Overcurrent protection, overvoltage protection and thermal shutdown function are designed in this device, but these are not intended to constantly ensure the suppression of this device within operation limits. Depending on the condition during actual usage, it could affect the electrical characteristic specification and reliability.
  When using these products, please read through and understand the concept of dissipation for absolute maximum ratings from the above-mentioned or our 'Semiconductor Reliability Handbook'. Then use these products under absolute maximum ratings in any condition. Furthermore, Toshiba recommend inserting failsafe system into the design.

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13. Package Information

13.1. Package Dimensions

Unit: mm



Weight: 41.9 mg (Typ.)

Figure 13.1 Package Dimensions (VQFN24D)

13.2. Land Pattern Dimensions for Reference only

Package type: VQFN24D

Unit: mm

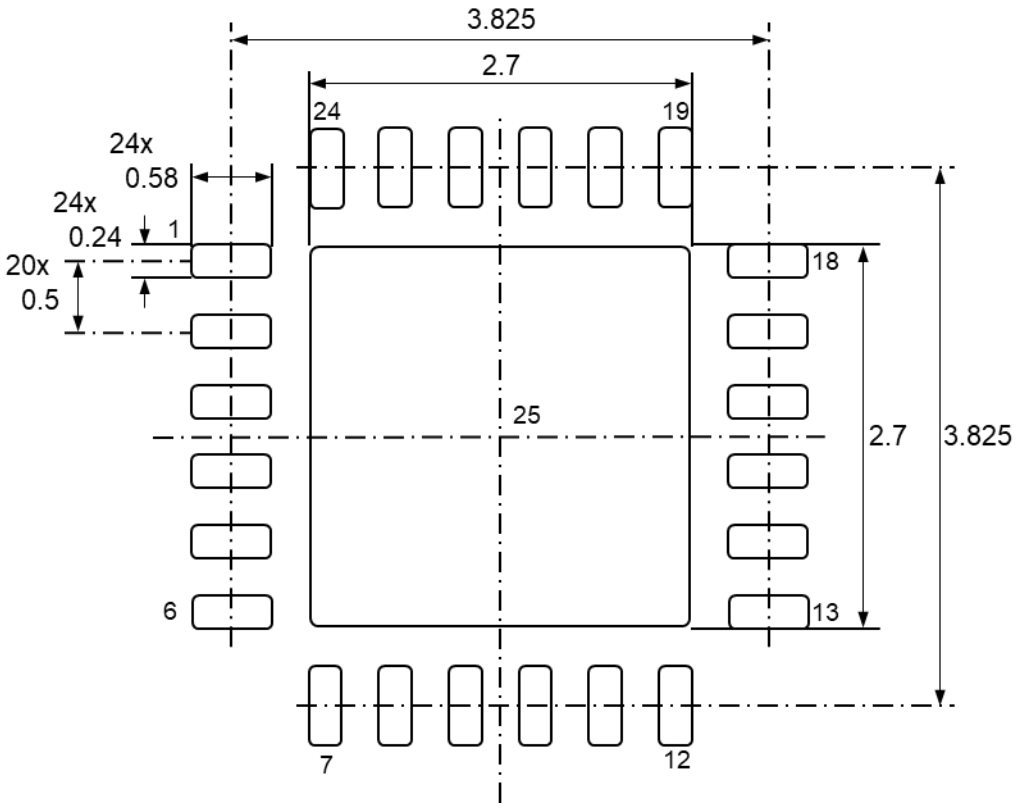


Figure 13.2 Land Pattern Dimensions for Reference only

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