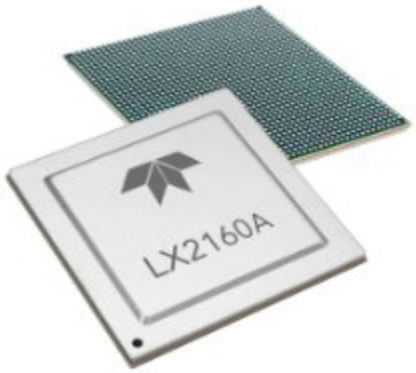
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LX2160A

Datasheet DS 60S 222625



Features

Arm Cortex®-A72 cores:

Up to 2.2 GHz

Single-threaded cores with 48KB L1 instruction cache and 32 KB L1 data cache

Layerscape® LX2160A has 16 cores, 8 MB L2 cache; LX2120A has 12 cores, 6 MB L2 cache; LX2080A has 8 cores, 8 MB L2 cache

Cache Coherent Interconnect Fabric

Up to 1500 MHz

8 MB Level 3 cache with ECC and On-Chip Memory (OCM) mode

Two 72-bit (64-bit + ECC) 3.2 GT/s DDR4 SDRAM memory controllers with ECC

Datapath acceleration architecture 2.0 (DPAA2)

Packet parsing, classification, and distribution (WRIOP)

Queue and hardware buffer management

Cryptography acceleration (SEC) at up to 50 Gbps

Decompression/compression acceleration (DCE) at up to 100 Gbps

Queue Direct Memory Access (QDMA) engine

Management complex (MC)

2 MB Packet express buffer

L2 Switching (114 Gbps)

24 SerDes lanes at up to 25 Gbps

High-speed peripheral interfaces

Two PCI express Gen 3.0 8-lane controllers supporting SR-IOV

Four PCI express Gen 3.0 4-lane controllers

Four serial ATA (SATA 3.0) controllers

Ethernet interfaces supporting IEEE 1588

Up to 18 Ethernet MACs

Support for 10G-SXGMII (USXGMII)

Support for SGMII (and 1000Base-KX)

Support for XFI, SFI, and 10GBase-KR

Support for CAUI4 (100G), 50GAUI-2 (50G), 25G- AUI (25G)

Support for XLAUI4 (and 40GBase-KR4) for 40G

Support for two RGMII parallel interfaces

Energy-efficient support (802.3az)

Additional peripheral interfaces

Two USB 3.0 controllers with integrated PHY

Two enhanced secure digital host controllers

Two Controller Area Network (CAN) modules, optionally supporting Flexible Data rate

Flexible Serial Peripheral Interface (FlexSPI) and three Serial Peripheral Interface (SPI) controllers

Eight I2C controllers

Four UARTs

General Purpose IO (GPIO)

Support for hardware virtualization and partitioning enforcement (Arm MMU-500)

QorIQ platform trust architecture 3.0 with 256 KB on-chip RAM for trusted accesses

Global interrupt controller (Arm GIC-500)

Two Flextimers, one secure watchdog timer and one non-secure watchdog timer

Debug supporting run control, data acquisition, high- speed trace, and performance/event monitoring

Support for Voltage ID (VID) for yield improvement

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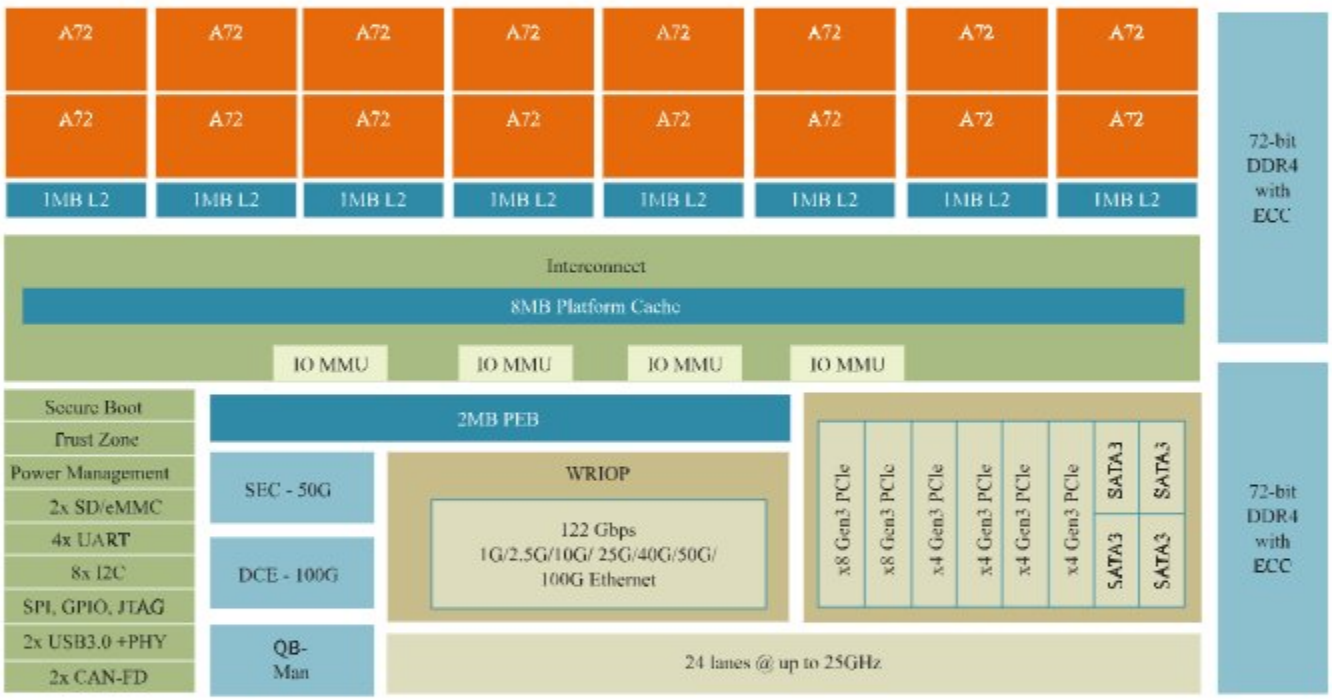
1 INTRODUCTION

The Layerscape® LX2160A processor is built on software-aware, core-agnostic DPAA2(*) architecture, which delivers scalable acceleration elements sized for application needs, unprecedented efficiency, and smarter, more capable networks. When coupled with ease-of-use facilities such as real-time monitoring and debug, virtualization, and software management utilities, the available toolkits allow for both hardware and software engineers to bring a complete solution to market faster than ever.[1]

The device integrated multicore processor combines sixteen Arm Cortex®-A72 processor cores with high-performance data path acceleration logic and network and peripheral bus interfaces required for networking, storage, telecom/datacom, wireless infrastructure, automotive, and military/aerospace applications.

The device processor is supported by a consistent API that provides both basic and complex manipulation of the hardware peripherals in the device, releasing the developer from the classic programming challenges of interfacing with new peripherals at the hardware level.

Figure 1. LX2160A Block diagram



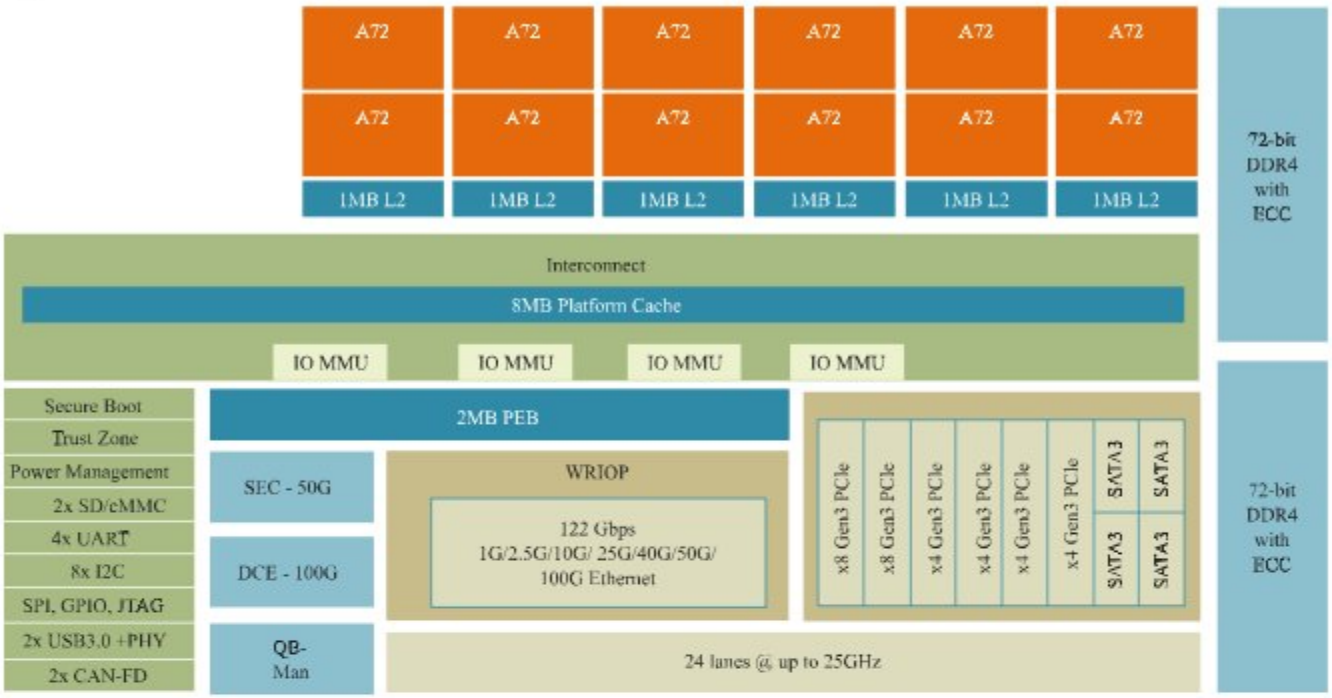
The LX2120A integrated multicore processor combines twelve Arm® v8 A72 cores. This figure shows the major functional units within the chip

(*) DPAA2 architecture is an evolution and extension of DPAA, a comprehensive architecture which integrates all aspects of packet processing in the SoC, addressing issues and requirements resulting from the multicore nature of QorIQ™ SoCs.

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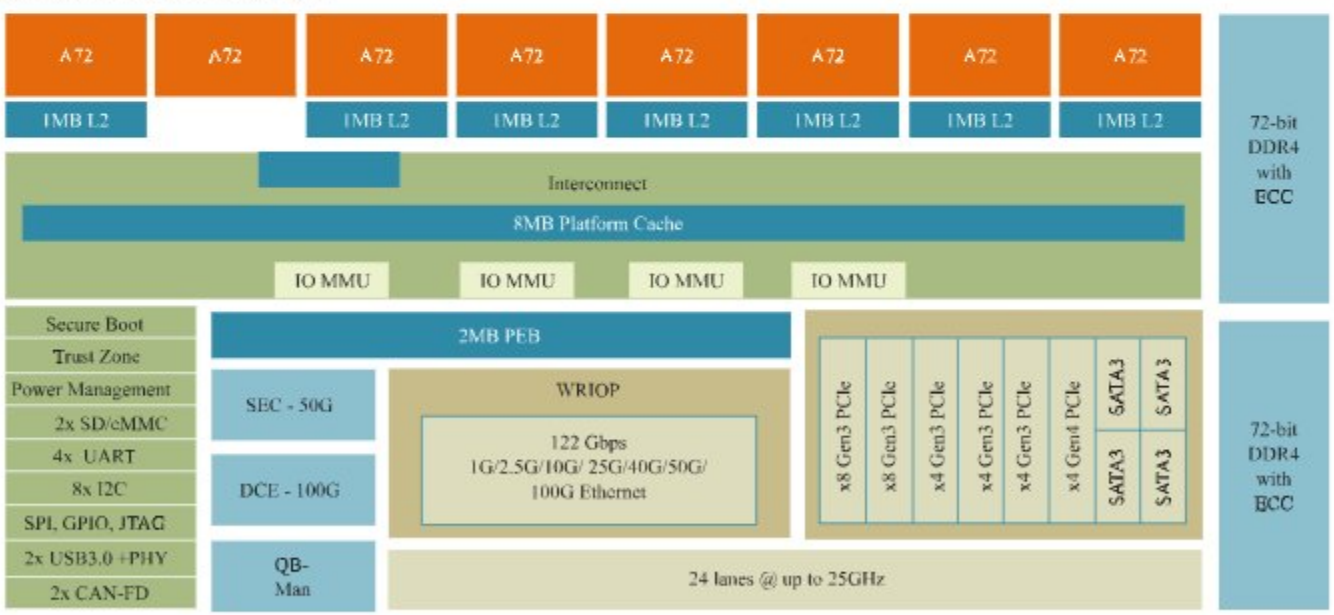
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Figure 2. LX2120A Block diagram



The LX2080A integrated multicore processor combines eight Arm® v8 A72 cores. This figure shows the major functional units within the chip.

Figure 3. LX2080A Block diagram



1.1 Device selection

This table shows how to set the TEST_SEL_B and the cfg_svr[0:1] pins to select between LX2160A, LX2120A, and LX2080A.

Table 1. Device Personality Selection

Personality	TEST_SEL_B	cfg_svr0 (primary signal XSPI1_A_CS0_B)	cfg_svr1 (primary signal XSPI1_A_CS1_B)
LX2160A	1	1	1
LX2120A	0	1	1
LX2080A	1	0	1

2 PIN ASSIGNMENTS

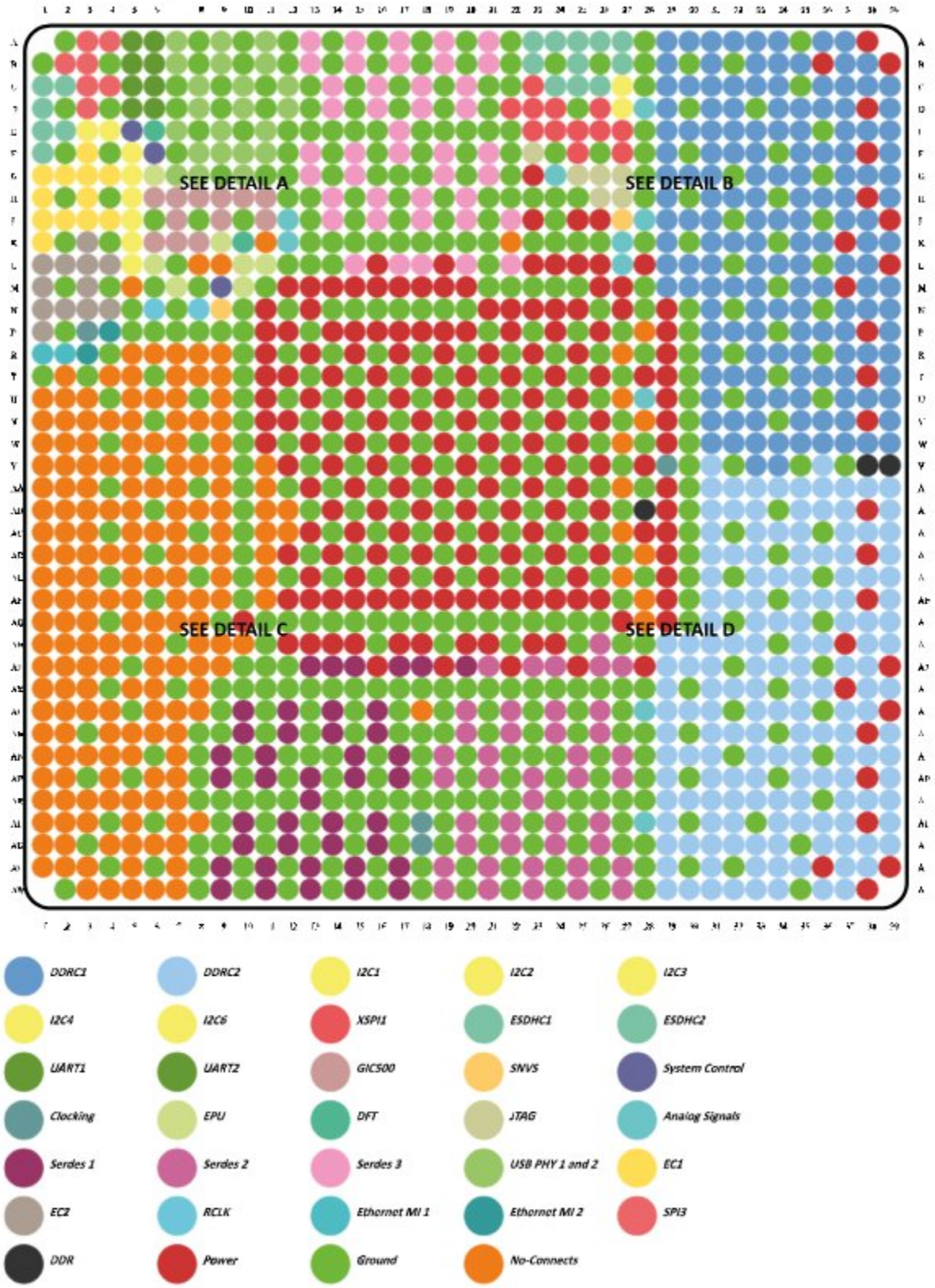
2.1 1517 ball layout diagrams

This figure shows the complete view of the LX2160A BGA ball map diagram. Figure 5, Figure 6, Figure 7, and Figure 8 show quadrant views.

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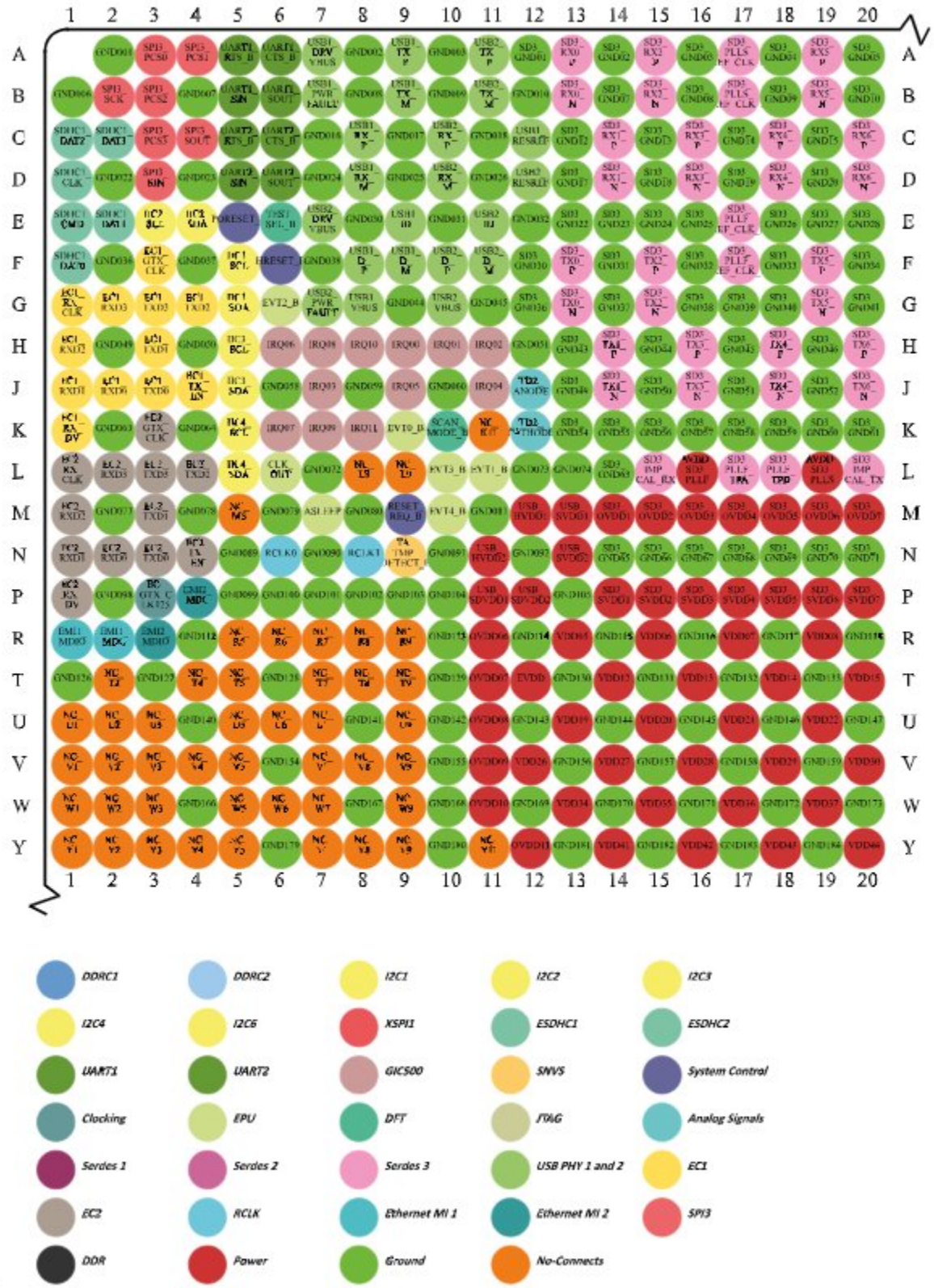
Figure 4. Complete BGA Map for the LX2160A



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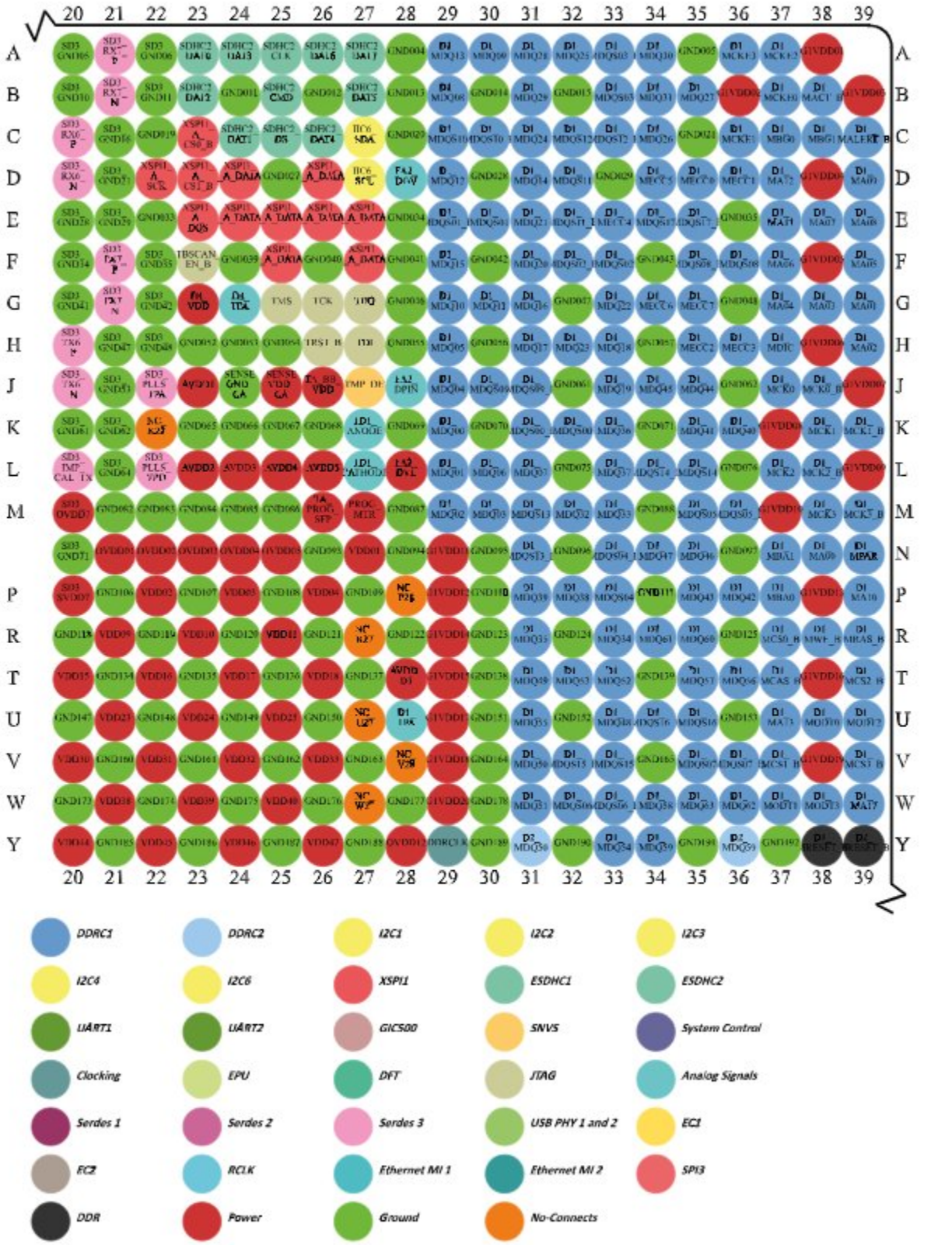
Figure 5. Detail A



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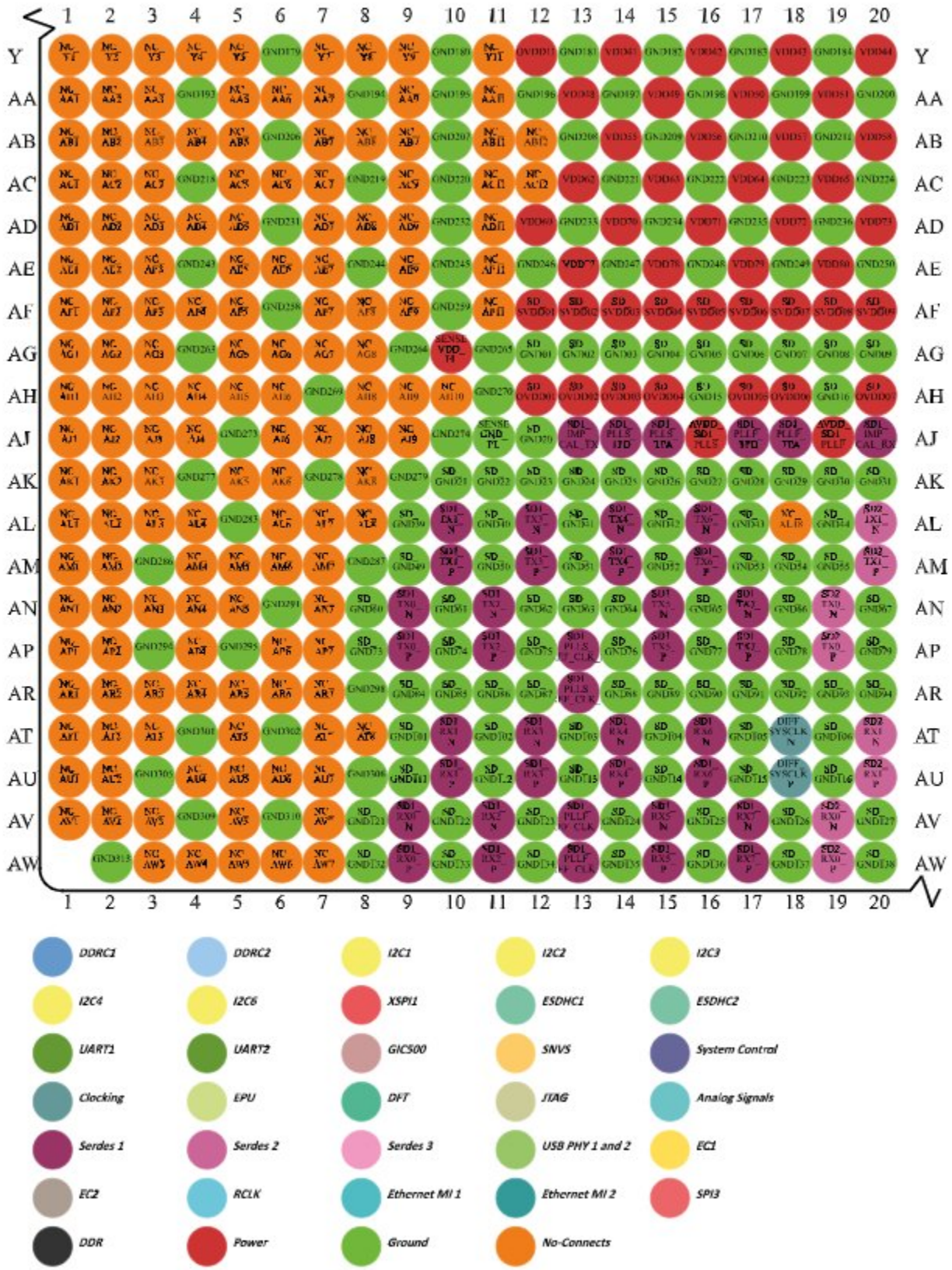
Figure 6. Detail B



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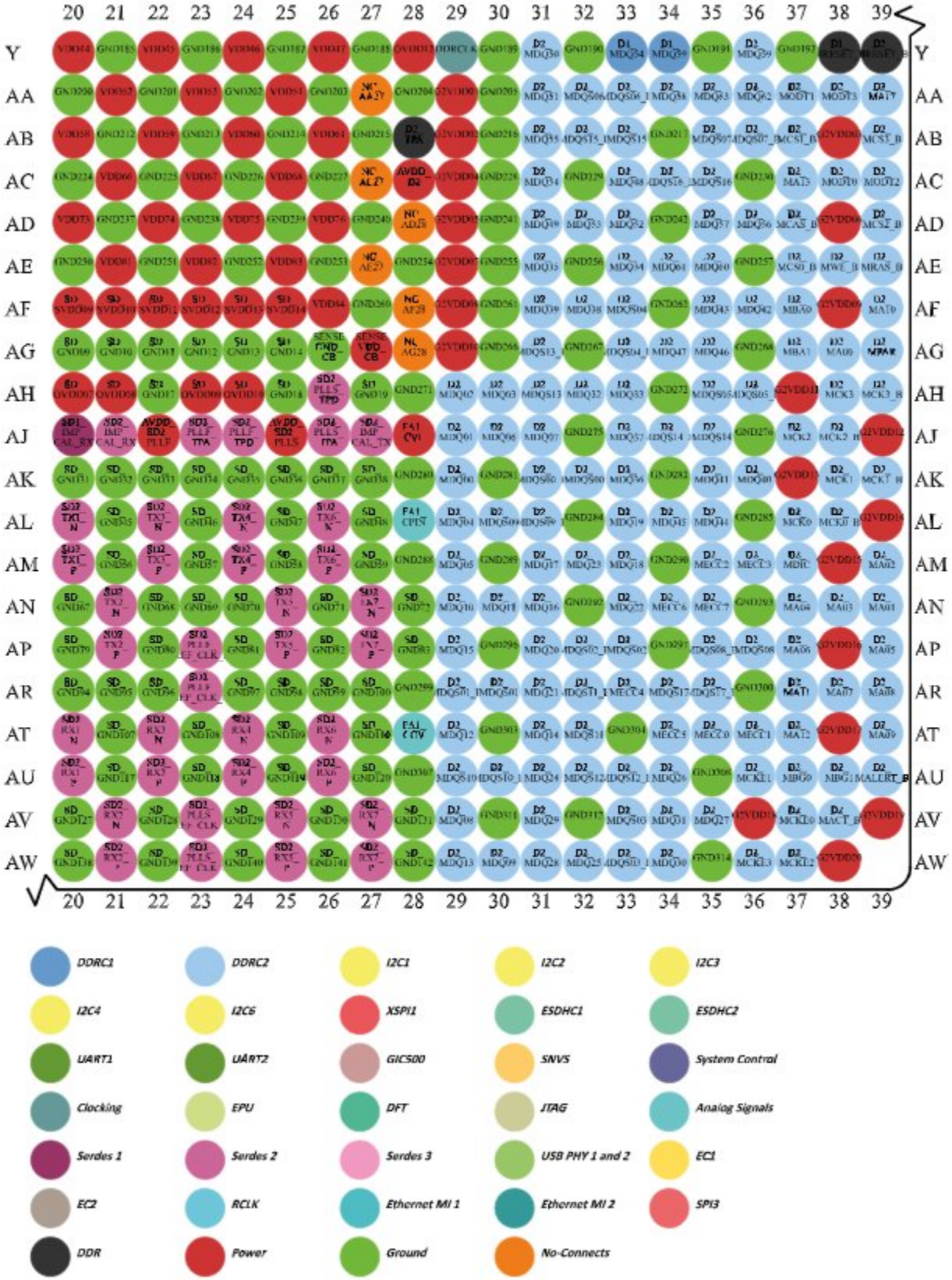
Figure 7. Detail C



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Figure 8. Detail D



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2.2 Pinout list

This table provides the pinout listing for the LX2160A by bus. Primary functions are **bolded** in the table.

Table 2. Pinout list by bus

Signal	Signal Description	Package pin number	Pin type	Power Supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	N38	O	$G1V_{DD}$	---
D1_MA01	Address	G39	O	$G1V_{DD}$	---
D1_MA02	Address	H39	O	$G1V_{DD}$	---
D1_MA03	Address	G38	O	$G1V_{DD}$	---
D1_MA04	Address	G37	O	$G1V_{DD}$	---
D1_MA05	Address	F39	O	$G1V_{DD}$	---
D1_MA06	Address	F37	O	$G1V_{DD}$	---
D1_MA07	Address	E38	O	$G1V_{DD}$	---
D1_MA08	Address	E39	O	$G1V_{DD}$	---
D1_MA09	Address	D39	O	$G1V_{DD}$	---
D1_MA10	Address	P39	O	$G1V_{DD}$	---
D1_MA11	Address	E37	O	$G1V_{DD}$	---
D1_MA12	Address	D37	O	$G1V_{DD}$	---
D1_MA13	Address	U37	O	$G1V_{DD}$	---
D1_MA17	Address	W39	O	$G1V_{DD}$	---
D1_MACT_B	Activate	B38	O	$G1V_{DD}$	---
D1_MALERT_B	Alert	C39	I	$G1V_{DD}$	1, 16
D1_MBA0	Bank Select	P37	O	$G1V_{DD}$	---
D1_MBA1	Bank Select	N37	O	$G1V_{DD}$	---
D1_MBG0	Bank Group	C37	O	$G1V_{DD}$	---
D1_MBG1	Bank Group	C38	O	$G1V_{DD}$	---
D1_MCAS_B	Column Address Strobe / MA[15]	T37	O	$G1V_{DD}$	---
D1_MCK0	Clock	J37	O	$G1V_{DD}$	---
D1_MCK0_B	Clock Complement	J38	O	$G1V_{DD}$	---
D1_MCK1	Clock	K38	O	$G1V_{DD}$	---
D1_MCK1_B	Clock Complement	K39	O	$G1V_{DD}$	---
D1_MCK2	Clock	L37	O	$G1V_{DD}$	---
D1_MCK2_B	Clock Complement	L38	O	$G1V_{DD}$	---

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