RX74M Group

Renesas MCUs

R01DS0433EJ0110
Rev.1.10
Jul 31, 2026

600-MHz 32-bit RX MCU, on-chip double-precision floating-point coprocessor, 3604 CoreMark, arithmetic unit for trigonometric functions, up to 1-MB code MRAM (supporting the dual bank function), 1.5-MB SRAM, EtherCAT slave controller, Ethernet switch module supporting TSN, SD/MMC host interface, expanded serial peripheral interfaces, various communications interfaces including CAN FD, 16-bit A/D converters, RTC, encryption functions, serial sound interfaces

Features

■ 32-bit RXv3e CPU core

- Maximum operating frequency: 600 MHz
  Capable of 3604 CoreMark performance in operation at 600 MHz
- 64-bit double-precision IEEE-754 floating point
- A collective register bank save function is available.
- Supports memory-protection units (MPUs)
- JTAG, SWD, and FINE (one-line) debugging interfaces
- Supports the Protect Zone function
- Instruction cache and data cache: 32 Kbytes each; support for ECC
- Two local RAMs: 128 Kbytes each; support for ECC

■ Low-power design and architecture

- Operation from a single 1.62- to 3.63-V supply
- The RTC and backup registers are capable of operation from a battery power supply.
- Seven low power consumption modes

■ On-chip user extra MRAM

- 128 Kbytes (switchable to operate as MTJ-OTP memory)
- User code is programmable by on-board or off-board programming.
- Capable of holding the user boot program, data, etc.

■ On-chip code MRAM

- Devices with up to 1 Mbyte are available.
- No wait cycles when the prefetch buffer is hit
- Supports reading at 100 MHz
- User code is programmable by on-board or off-board programming.
- Programming as a background operation (BGO)
- A dual-bank structure allows swapping the start-up bank.

■ On-chip data MRAM

- 48 Kbytes; programmable up to 100,000 times
- Programming as a background operation (BGO)

■ On-chip SRAM

- 1.5 Mbytes; support for ECC and reading at 150 MHz

■ Data transfer

- Eight DMA controllers (DMACs), DTCA, two EXDMA controllers (EXDMACs), Ethernet DMAC (GWCA), and two XSPIs serving as target modules

■ Reset and supply management

- Power-on reset (POR)
- Programmable voltage detection (PVD)
- Core voltage monitoring (CVM)
- Temperature monitoring reset
- Backup area reset
- Reset output function

■ Clock functions

- Main clock oscillator for an 8- to 48-MHz external resonator
- Sub-clock oscillator for a 32.768-kHz crystal resonator
- Two PLL circuits
- 8-MHz MOCO, HOCO with 16, 18, 20, 32, or 48 MHz selectable, and 32.768-kHz LOCO
- Clock output function

■ Realtime clock

- Adjustment functions (for 30 seconds, leap year, and time error)
- Realtime clock counting and binary counting modes are selectable.
- Time capture in response to event-signal input

■ Independent watchdog timer

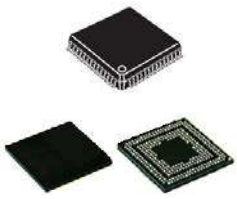
- Operation at 16.384 kHz. Operation in deep software standby mode 1 is possible.

■ Useful functions for IEC60730 compliance

- Oscillation stop detection (MOSC, SOSC), clock frequency accuracy measurement circuits, CRCA, IWDTa, DOCA, self-diagnosis and disconnection detection assist functions for the A/D converters, etc.
- Register write protection function protects important registers against overwriting.

■ External address space

- Buses for high-speed data transfer (max. operating frequency of 80 MHz)
- 8 CS areas with 8-, 16-, or 32-bit bus space selectable per area
- Independent SDRAM area (128 Mbytes) and XSPI areas (1 Gbyte)



PLQP0176KJ-A	24 × 24 mm, 0.5-mm pitch
PLQP0144KA-B	20 × 20 mm, 0.5-mm pitch
PLQP0100KP-A	14 × 14 mm, 0.5-mm pitch
PLBG0320GD-A	17 × 17 mm, 0.8-mm pitch
PLBG0224GE-A	13 × 13 mm, 0.8-mm pitch
PLBG0176GG-A	13 × 13 mm, 0.8-mm pitch

■ Various communications interfaces

- EtherCAT slave controller with two ports
- Two Ethernet MAC units for transfer at up to 1 Gbps, Ethernet switch module with two ports, support for Ethernet TSN
- One high-speed USB 2.0 port for host/function, OTG controller, or BC 1.2, with on-chip PHY layer
- One full-speed USB 2.0 port for host/function or OTG controller, with on-chip PHY layer
- Three CAN FD modules compliant with the specifications of ISO 11898-1:2015
- 13 RSCIs with 16-byte transmission and reception FIFO buffers
  The serial communications mode can be selected from among asynchronous, clock synchronous, smart card interface, simple SPI, simple I^2C, and extended serial.
  Communications in Manchester code available, support for HBS functionality
- Two I^2C-bus interfaces for transfer at up to 3.4 Mbps
- I3C bus interface for transfer at up to 12 Mbps in SDR mode
- Three RSPIAs with single I/O for transmission and reception at up to 50 Mbps
- Parallel data capture unit (PDC) for the CMOS camera interface
- SD/MMC host interface with a 1- or 4-bit SD bus for use with SD memory or SDIO
- Two SSIEs for various audio formats such as I^2S
- Two XSPIs for transfer at up to 266 MT/s, switchable between controller and target, support for 1-, 2-, 4-, and 8-bit protocols and decryption on the fly (DOTF)
- PDM-IF connectable with an external microphone

■ Up to 26 extended-function timers

- 16 32-bit general PWM timers (GPTWs), two 8-bit timers (TMRs) with 2 channels per unit, two 16-bit CMTs with 2 channels per unit, two 32-bit compare match timers W (CMTWs) with a single channel per unit

■ Three 16-bit A/D converters

- Up to 36 analog input channels
- Self-diagnosis, detection of analog input disconnection

■ Two 12-bit D/A converters

■ Temperature sensor for measuring temperature within the chip

■ Arithmetic unit for trigonometric functions

■ Two DSMIFs with 3 channels per unit, connectable with up to six external delta-sigma modulators

■ Two phase-counting interfaces

■ Security features

- Renesas Secure IP (RSIP-E50D) (true-random number generator (TRNG), AES, ChaCha20-Poly1305, RSA, ECC, SHA-512, SHA3-512, and 128-bit unique ID)
- Zeroization
- Device lifecycle management
- Support for decryption on the fly (DOTF)
- Secure boot
- Detection of tampering
- The security attribute is specifiable per pin.
- Protect Zone function

■ Up to 197 pins for general I/O ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability
- Software configurable 32-bit programmable I/O port

■ Operating temperature range

- Tj = –40 to +125°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 give a comparison of the functions of products in different packages.

Table 1.1 is an outline of maximum specifications, and the peripheral modules and the number of channels of the modules differ depending on the number of pins on the package. For details, refer to Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/10)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 600 MHz • 32-bit RX CPU (RXv3e) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Protect Zone: Three worlds (non-secure, secure, and root) • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Fourteen 32-bit registers Accumulator: Two 72-bit registers • 117 instructions Instructions installed as standard: 111 Basic instructions: 77 Single-precision floating-point operation instructions: 11 DSP instructions: 23 Instructions for register bank save function: 2 Protect Zone instructions: 4 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Instruction cache and data cache: 32 Kbytes each • Accelerator for branch instruction processing: 272 bytes
	FPU	• Single-precision floating-point numbers (32 bits) • Data types and floating-point exceptions in conformance with the IEEE754 standard
	Double-precision floating point coprocessor	• Double-precision floating-point register set Double-precision floating-point data registers: 16, each with 64-bit width Double-precision floating-point control registers: Four, each with 32-bit width • Double-precision floating-point processing instructions: 21 • Notifying the interrupt controller of double-precision floating-point exceptions
	Register bank save function	• Fast collective saving and restoration of the values of CPU registers • Sixteen save register banks are incorporated in each of the root world, secure world, and non-secure world.

Table 1.1 Outline of Specifications (2/10)

Classification	Module/Function	Description
Memory	Code MRAM	• Capacity: 512 Kbytes/1 Mbyte • On-board programming: Five types • A dual-bank structure allows programming during reading or exchanging the start-up areas
	Data MRAM	• Capacity: 48 Kbytes • Programming: 100,000 times
	User extra MRAM	• Capacity: 128 Kbytes • On-board programming: Five types • Switchable to operate as MTJ-OTP
	Unique ID	• 128-bit unique ID for each device of this product family
	RAM	• Capacity: 1.5 Mbytes • Error-correcting code (ECC), single-error correcting and double-error detecting code (SEC-DED)
	Local RAM	• Capacity: 128 Kbytes × 2 • Up to 600 MHz, no-wait access • Error-correcting code (ECC), single-error correcting and double-error detecting code (SEC-DED)
Operating modes		• Operating modes by the mode-setting pins at the time of release from the reset state Single-chip mode Boot mode (SCI interface) Boot mode (USB interface) Boot mode (FINE interface) Boot mode (JTAG interface) Boot mode (SWD interface) • Selection of operating mode by register setting Single-chip mode • Endian selectable
Clocks	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed/middle-speed/high-speed on-chip oscillator, and PLL frequency synthesizer (two circuits) • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Sub-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the CPU clock (CPUCLK0), system clock (ICLK), MRAM code bus clock (MRICLK), MRAM peripheral clock (MRPCLK), peripheral module clocks (PCLKA, PCLKB, PCLKD, PCLKE), and external bus clock (BCLK) The CPU and local RAM run in synchronization with CPUCLK0: Up to 600 MHz The MRAM bus and code MRAM run in synchronization with MRICLK: Up to 300 MHz The data MRAM runs in synchronization with MRPCLK: Up to 150 MHz The RAM and other bus masters run in synchronization with the system clock (ICLK): Up to 300 MHz Peripheral modules of CRCA, DOCA, RSPIA, RSCI, ESWM, GPTW, HRPWM, POEG, DSMIF, ADC16H, CANFDG, CANFD, RSIP, RI3C, RIICHS, USBHS, and ESC run in synchronization with PCLKA, which operates at up to 150 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 75 MHz The counter reference clock for the GPTW runs in synchronization with PCLKD: Up to 150 MHz The CANFDRAM runs in synchronization with PCLKE: Up to 300 MHz Devices connected to the external bus run in synchronization with BCLK: Up to 150 MHz • The high-speed on-chip oscillator (HOCO) can be obtained through frequency-multiplication of the PLL1 or PLL2 reference clock • External clock input frequency for the main clock oscillator: Up to 48 MHz • External clock input frequency for the sub-clock oscillator: 32.768 kHz • Clock output function

Table 1.1 Outline of Specifications (3/10)

Classification	Module/Function	Description
Resets		Sixteen types of reset • RES# pin reset: Triggered when the RES# pin is driven low. • Power-on reset: Triggered when the RES# pin is driven high and VCC rises above specific levels. • Core voltage monitoring reset: Triggered when the core voltage falls below or rises above specific levels. • Voltage-monitoring 0 reset: Triggered when VCC falls below specific levels. • Voltage-monitoring 1, 2, 4, and 5 resets: Triggered when VCC falls below or rises above specific levels. • Temperature-monitoring reset: Triggered due to the detection of temperatures outside the specified range. • Deep software standby reset: Triggered in response to an interrupt to trigger release from deep software standby. • Independent watchdog timer reset: Triggered when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Triggered when the watchdog timer underflows, or a refresh error occurs. • Software reset: Triggered by register setting. • Bus error reset: Triggered in response to an illicit address or size error • Common memory error reset: Triggered in response to an ECC error in the RAM • Local memory error reset: Triggered in response to an ECC error in the CPU cache or local RAM Reset output is available.
Power-on reset		• If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Programmable voltage detection circuit (PVD)		Monitors the voltage being input to the VCC pins and generates an internal reset or interrupt. • Voltage detection circuit 0 Capable of generating an internal reset The option-setting memory can be used to select enabling or disabling of the reset. Voltage detection level: Selectable from seven different levels (2.85 V, 2.58 V, 2.15 V, 2.00 V, 1.90 V, 1.80 V, 1.67 V) • Voltage detection circuits 1, 2, 4 and 5 Voltage detection level: Selectable from twelve different levels (3.14 V, 3.10 V, 3.08 V, 2.85 V, 2.83 V, 2.80 V, 2.62 V, 2.33 V, 1.90 V, 1.86 V, 1.74 V, 1.71 V) Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) Capable of generating an internal reset • Two types of timing are selectable for release from reset An internal interrupt can be requested only from voltage detection circuits 1 and 2. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable Voltage detection monitoring Event linking
Low power consumption	Low power consumption function	• Module stop function • Seven low power consumption modes Sleep mode, deep sleep mode, software standby modes 1 and 2, and deep software standby modes 1 to 3
	Battery backup function	• When the voltage on the VCC pin drops below a certain point, battery power from the VBATT pin is supplied to the backup power area. • Backup power area: sub clock oscillator real-time clock backup register Tamper detection • Detection of voltage drop in the backup power area

Table 1.1 Outline of Specifications (4/10)

Classification	Module/Function	Description
Interrupt	Interrupt controller (ICUM)	• Number of interrupt vectors: 256 • External interrupts: 32 (pins IRQ0 to IRQ31) • Software interrupts: 2 sources • Non-maskable interrupts: 13 sources • 32 levels specifiable for the order of priority • Method of interrupt source selection: The interrupt vectors consist of 256 vectors (128 sources are fixed. The remaining 128 vectors are selected from among the other 374 sources.)
External bus extension		• The external address space can be divided into eight areas (CS0 to CS7), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS7) A chip-select signal (CS0# to CS7#) can be output for each area. Each area is specifiable as an 8-, 16-, or 32-bit bus space. The data arrangement in each area is selectable as little or big endian (only for data). • SDRAM interface connectable • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility • Connection for a memory device compliant with the expanded serial peripheral interface (xSPI) is possible (JEDEC Standards JESD 251, JESD 251-1, and JESD 252).
DMA	DMA controller (DMACAa)	• 8 channels • Four transfer modes: Normal transfer, repeat transfer, block transfer, and repeat block transfer • Request sources: Software trigger and interrupt requests from peripheral functions
	EXDMA controller (EXDMACAa)	• 2 channels • Four transfer modes: Normal transfer, repeat transfer, block transfer, and repeat block transfer • Request sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCA)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: External interrupts and interrupt requests from peripheral functions • Sequence transfer
I/O ports	Programmable I/O ports	• I/O ports for the 320-pin LFBGA I/O pins: 197 Input pins: 3 Pull-up resistors: 198 Open-drain outputs: 197 5-V tolerant pins: 16 • I/O ports for the 224-pin LFBGA I/O pins: 159 Input pins: 3 Pull-up resistors: 160 Open-drain outputs: 159 5-V tolerant pins: 16 • I/O ports for the 176-pin LFBGA and 176-pin LFQFP I/O pins: 120 Input pins: 3 Pull-up resistors: 121 Open-drain outputs: 120 5-V tolerant pins: 16 • I/O ports for the 144-pin LFQFP I/O pins: 100 Input pins: 3 Pull-up resistors: 101 Open-drain outputs: 100 5-V tolerant pins: 16 • I/O ports for the 100-pin LFQFP I/O pins: 72 Input pins: 3 Pull-up resistors: 73 Open-drain outputs: 72 5-V tolerant pins: 9

Table 1.1 Outline of Specifications (5/10)

Classification	Module/Function	Description
I/O ports	Software configurable 32-bit programmable I/O port (PIO)	• Of the 64 port pins, up to 32 can be selected for simultaneous use. • Input or output can be enabled, and for outputs, the high or low level can be specified through register settings.
Event link controller (ELC)		• Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions. • 381 internal event signals can be freely combined for interlinked operation with connected functions. • Event signals from peripheral modules can be used to change the states of output pins (of ports B, C, D, and E). • Changes in the states of pins (of ports B, C, D, and E) being used as inputs can be interlinked with the operation of peripheral modules.
Timers	General PWM timer (GPTW)	• 32 bits × 16 channels (GPTW0 to GPTW15) • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Generation of dead times in PWM operation • Generation of highly accurate PWM waveforms with duty cycles close to the settings for values in the vicinity of duty 0% and 100%. • In output compare operation, settings of the comparison registers are immediately reflected, and the generation of PWM waveforms with secured dead times is possible. • Switching the direction of counting during operations in the triangle-wave PWM mode is possible. • The counter can be synchronously started, stopped, cleared, or have its direction of counting switched in any channel. • The counter can be started, stopped, cleared, or have its direction of counting switched, incremented, or decremented in response to up to eight ELC events. • The counter can be started, stopped, cleared, or have its direction of counting switched, incremented, or decremented in response to detecting a state transition in one event input signal while another input signal is at a particular level. • The counter can be started, stopped, cleared, or have its direction of counting switched, incremented, or decremented in response to up to four external triggers. • Disabling of output on detection of a dead time error or a short-circuit among output pins is possible. • Using a timer to generate a trigger signal to start A/D conversion is possible. The trigger signal can be output to the external pin is possible. • Output of events, such as compare-matches from A to F, overflow, and underflow, to the ELC is possible. • The noise filter of input capture is available. • Cycle counting • Measurement of the pulse width of the input signal • Output of the result of a logical operation on the output signal from one channel and that from another channel is possible. • Synchronous counter setting/counter clearing/input capture among channels • The timer-linked synchronization signal output function enables synchronous operation between channels synchronized with the timer period, and synchronous operation with other IPs synchronized with the timer period. • GTIOCnA/GTIOCnB pin input/output polarity inversion
	High resolution PWM waveform generation circuit (HRPWMb)	• Finely adjusting a PWM waveform generated by GPTW0 to GPTW3 with a minimum resolution of approximately 49 ps is possible.

Table 1.1 Outline of Specifications (6/10)

Classification	Module/Function	Description
Timers	GPTW port output enable (POEGd)	Various types of request to stop output from general PWM timers (GPTWs) are available. • Stopping output in response to detecting the input level on the GTETRGx pin • Stopping output in response to an output stopping signal from the GPTW • Stopping output in response to detecting the stopping of oscillation, or to requests by software • Stopping output in response to detecting a DSMIF error • Stopping output in response to detecting the input level or an edge on the POEG pin
	8-bit timer (TMRa)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Capable of generating baud-rate clocks for RSCI • Event linking by the ELC
	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512)
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Event linking by the ELC
	Realtime clock (RTCBb)	• Clock sources: Low-speed on-chip oscillator, sub-clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192) • Event linking by the ELC
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: Low-speed on-chip oscillator (IWDT-dedicated clock) • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC • Operation in the deep software standby mode 1 is possible.
Communications functions	Ethernet module (ESWM)	• One channel (two ports) • Ethernet switch with a high-level routing function and multi-protocol interface • Transfer at 10, 100, or 1000 Mbps • Full- and half-duplex modes • Detection of Magic Packets™*1 or output of a “Wake-On-LAN” signal (WOL) • Management frame transmission/reception with PHY-LSI compliant with the following specifications: MII (Media-Independent Interface), RMII (Reduced Media-Independent Interface), GMII (Gigabit Media-Independent Interface), and RGMII (Reduced Gigabit Media-Independent Interface) • Support for MII MAC-to-MAC connection • Two gPTP channels
	EtherCAT slave controller (ESC)*2	• One channel (two ports) • The Beckoff EtherCAT Slave Controller IP Core was adopted for this.

Table 1.1 Outline of Specifications (7/10)

Classification	Module/Function	Description
Communications functions	USB 2.0 full-speed host/function module (USBf)	• Includes a USB device controller (UDC) and transceiver for USB 2.0 FS • One port • Compliant with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-powered mode and bus-powered mode are supported • On-the-Go (OTG) operation is possible (low-speed is not supported) • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required
	USB 2.0 high-speed host/function module (USBHS)	• Includes a USB device controller (UDC) and transceiver for USB 2.0 HS • One port (320-pin/224-pin/176-pin products only) • Compliant with the USB 2.0 specification • Transfer rate: High speed (480 Mbps), full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-powered mode and bus-powered mode are supported • On-the-Go (OTG) operation is possible (low-speed is not supported) • Compliant with Battery Charging Specification Revision 1.2 (BC1.2) • Incorporates 8.5 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required
	Serial communications interface (RSCI)	• 13 channels • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multi-processor function • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Start-bit detection: Level or edge detection is selectable. • Simple I^2C • Simple SPI • 9-bit transfer mode • Bit rate modulation • Double-speed mode • Average transfer rate clock can be input from TMR timers • Event linking by the ELC • Supports the serial communications protocol, which contains the start frame and information frame • Supports the LIN format • Data can be transmitted or received in sequence by the 16-byte FIFO buffers of the transmission and reception unit • Manchester encoding is supported. • RSCI has some home bus system (HBS) functionality. • Data match detection • Adjustment of the timing of sampling of the RXD signals
	I3C bus interface (RI3C)	• Single channel (I^2C/I3C) • I^2C protocol mode Communication formats: I^2C-bus format/SMBus format Supports the multi-master Max. transfer rate: 3.4 Mbps • I3C protocol mode Communication protocols: SDR mode, Legacy I^2C message support Supports the multi-master Max. transfer rate: 12 Mbps • Event linking by the ELC
	High-speed I^2C-bus interface (RIICHS)	• Two channels (I^2C only) • I^2C-bus interface Communication formats: I^2C-bus format/SMBus format Supports the multi-master Max. transfer rate: 3.4 Mbps

Table 1.1 Outline of Specifications (8/10)

Classification	Module/Function	Description
Communications functions	CAN FD module with gateway functionality (CANFDG)	• 2 channels • Compliance with the ISO11898-1:2015 specification (standard frame and extended frame) • Gateway function • Message buffers 32 receive message buffers 16 transmit message buffers per channel Four transmit queues per channel • FIFO Eight receive FIFOs Six common FIFOs
	CAN FD module (CANFD)	• 1 channel • Compliance with the ISO11898-1:2015 specification (standard frame and extended frame) • Message buffers 16 receive message buffers Four transmit message buffers One transmit queue • FIFO Tow receive FIFOs One common FIFO
	Serial peripheral interface (RSPIA)	• 3 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Transmit/receive data can be swapped in byte units • Buffered structure The transmitter and receiver each have four-stage 32-bit FIFO buffers to enable continuous transmission and reception. • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC • Communications protocol: RSPIA supports the Texas Instruments Synchronous Serial Protocol (TI SSP).
	Expanded serial peripheral interface (XSPI)	• 2 units (switchable between controller and target) • Compliant with xSPI (JEDEC Standards JESD 251, JESD 251-1, and JESD 252) • 1-bit, 2-bit, 4-bit, and 8-bit protocols supported • Supports Octal SPI in the JESD 251 Profile 1.0, and HyperBus™ (HyperRAM™ and HyperFlash™) in the JESD 251 Profile 2.0. • Supports decryption on the fly (DOTF) • Maximum operating rate as a controller: 266 MT/s (133-MHz clock) • Maximum operating rate as a target: 200 MT/s (100-MHz clock)
Serial sound interface (SSIE)		• 2 channels • Full-duplex transmission (for both channel 0 and channel 1) • Various types of serial audio formatting are supported. • Master and slave operations are supported. • The bit-clock frequency is selectable from among 13 frequencies (1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, or 1/128). • Data formats with 8, 16, 18, 20, 22, 24, and 32 bits are supported. • 32-stage FIFO buffers for transmission and reception • Stopping or not stopping the SSILRCK signal on stopping of data transmission is selectable. • Clock signal from a GPTW is selectable.

Table 1.1 Outline of Specifications (9/10)

Classification	Module/Function	Description
SD/MMC host interface (SDHIc)		• 1 channel • SD bus interface One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses) Compatible with the SD, SDHC, and SDXC formats • MMC bus interface Data buses: Support for 1-, 4-, and 8-bit MMC buses • Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt, interrupt of SD buffer access • DMA transfer requests: SD_BUF write and SD_BUF read • Support for card detection and write protection
Arithmetic unit for trigonometric functions (TFUv2)		• Calculation of sine, cosine, arctangent, and hypotenuse Simultaneous calculation of sine and cosine Simultaneous calculation of arctangent and hypotenuse
Delta-sigma modulator interface (DSMIFA)		• 6 channels • Up to six external delta-sigma modulators are connectable. • The sinc filters are selectable as first-, second-, or third-order. • PWM synchronization triggered by a GPTW output.
Parallel data capture unit (PDC)		• 1 channel • Acquisition of synchronization through external 8-bit horizontal and vertical synchronization signals • Setting of the image size when clipping of the output for a one-frame image is required
Pulse-density modulation interface (PDM-IF)		• 1 channel • Connectable with an external microphone • 1-bit digital input data can be converted to 20- or 16-bit data. • Four filters: Sinc filter, high-pass filter, correction filter, and half-band decimation filter • Incorporates an internal buffer
Phase-counting interface (PCIF)		• Two units • Outputs ABZ-phase waveforms similar to incremental encoder outputs • Carrier-cycle event input from the ELC
16-bit A/D converter (ADC16H)		• Three units • Hybrid architecture that combines successive comparison and delta-sigma modulation • Up to 16-bit resolution (switchable between 16, 14, 12, and 10 bits) • High-speed conversion: 0.16 μs at the 50-MHz A/D conversion clock • Self-calibration • Extended analog functions: Self-diagnostic function, temperature sensor, internal reference voltage, VBATT voltage, D/A converter • Channel-dedicated sample-and-hold function (3 channels only in unit 0) • Supports single-ended and differential inputs
12-bit D/A converter (DAC12R)		• 2 channels • 12-bit resolution • Output voltage: 0.2 V to AVCC0 – 0.2 V (buffered output), 0 V to AVCC0 (unbuffered output) • Buffered output or unbuffered output can be selected. • Event linking by the ELC
Temperature sensor		• 1 channel • Relative precision: ± 1°C • The voltage of the temperature is converted into a digital value by the 16-bit A/D converter. • Detection of abnormally high and low temperatures
Safety	Memory-protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 32 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An access exception occurs when the detected access is not in the permitted area.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.

Table 1.1 Outline of Specifications (10/10)

Classification	Module/Function	Description
Safety	CRC calculator (CRCA)	• Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop detection	• Main clock oscillation stop detection: Available
	Sub clock oscillation stop detection	• Sub clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Three units • Monitors the clock output from the main clock oscillator, sub-clock oscillator, low-, middle-, and high-speed on-chip oscillators, PLL1P, PLL1Q, PLL1R, PLL2P, PLL2Q, PLL2R, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOCA)	• This handles the comparison, addition, subtraction, comparison in terms of which is larger or smaller, or window comparison of 32-bit values.
Security	Security function	• Protect Zone function Security state of the CPU: Secure or non-secure Access to the secure area is only possible through the CPU when it is in the secure state. • Privilege control • Device lifecycle management • Configurable range for access by the debugger at the debug authentication level • Secure key injection • Secure multi-function pin controller • Secure boot • Secure factory programming • The RSIP can be used for data confidentiality and protection against tampering with data. 256-bit hardware unique key (HUK) 128-bit unique ID OEM boot loader version Key data for use with circuits for decryption on the fly (DOTFs) Protection against SPA or DPA
	Decryption on the fly (DOTF)	Decrypt encrypted content stored in external memory in real time.
Encryption function	Renesas Secure IP (RSIP-E50D)	• Common key encryption: AES, ChaCha20-Poly1305 • Public key encryption: RSA, ECC • Hash value generation: SHA-512, SHA3-512 • TRNG (true-random number generator) : 128-bit
Operating frequency		Up to 600 MHz
Power supply voltage		VCC = VCC2 = 1.62 to 3.63 V VCC_USB = VCC_USBHS = AVCC_USBHS = 1.62 to 3.63 V AVCC0 = 1.62 to 3.63 V, 1.62 ≤ VREFH0 ≤ AVCC0 V_{BATT} = 1.62 to 3.63 V The level of each power supply voltage can independently be set. Connect the VCC_DCDC pin to VCC or VSS in accord with the power-supply mode.
Junction temperature		‘4’ version: –40 to +125°C
Package		320-pin LFBGA (PLBG0320GD-A) 224-pin LFBGA (PLBG0224GE-A) 176-pin LFBGA (PLBG0176GG-A) 176-pin LFQFP (PLQP0176KJ-A) 144-pin LFQFP (PLQP0144KA-B) 100-pin LFQFP (PLQP0100KP-A)
On-chip debugging system		• JTAG, SWD, and FINE interfaces

Note 1. Magic Packet™ is a registered trademark of Advanced Micro Devices, Inc.
Note 2. EtherCAT® is a registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.

Table 1.2 Comparison of Functions for Different Packages (1/2)

Functions		**RX74M Group**					
Package		**320-Pin LFBGA**	**224-Pin LFBGA**	**176-Pin LFBGA**	**176-Pin LFQFP**	**144-Pin LFQFP**	**100-Pin LFQFP**
Operating frequency (max.)		600/300 MHz			480/300 MHz		
External bus	External bus width	32 bits/16 bits/8 bits				16 bits/8 bits	Not available
	SDRAM area controller	Available					Not available
DMA	DMA controller	Ch. 0 to 7					
	Data transfer controller	Available					
	EXDMA controller	Ch. 0 and 1					Not available
Timers	General PWM timer	Ch. 0 to 15					
	High resolution PWM	Ch. 0 to 3					
	Port output enable for GPTW	Available					
	8-bit timers	Ch. 0 to 3					
	Compare match timer	Ch. 0 to 3					
	Compare match timer W	Ch. 0 and 1					Ch. 1
	Realtime clock	Available					
	Watchdog timer	Available					
	Independent watchdog timer	Available					
Communications functions	Ethernet module	ch0 (GMII/MII/RMII/RGMII), ch1 (GMII/MII/RMII/RGMII)	ch0 (MII/RMII/RGMII), ch1 (MII/RMII/RGMII)		ch0 (MII/RMII), ch1 (MII/RMII)		
	EtherCAT slave controller	Available (Ch. 0 and 1)/Not available					
	USB 2.0 full-speed host/function module	Ch. 0					
	USB 2.0 high-speed host/function module	Ch. 0				Not available	
	Serial communications interface	Ch. 0 to 12					Ch. 0 to 5, 7, 8, 10 to 12
	I3C bus interface	Ch. 0					
	High-speed I^{2}C-bus interface	Ch. 1 and 2					
	Serial peripheral interface	Ch. 0 to 2					
	CAN FD module	Ch. 0 to 2					
	Expanded serial peripheral interface	Unit 0 (1 bit, 2 bits, 4 bits, 8 bits), Unit 1 (1 bit, 2 bits, 4 bits, 8 bits)	Unit 0 (1 bit, 2 bits, 4 bits, 8 bits), Unit 1 (1 bit, 2 bits, 4 bits)				Unit 0 (1 bit, 2 bits, 4 bits), Unit 1 (1 bit, 2 bits, 4 bits)
	Serial sound interface	Ch. 0					
	SD/MMC host interface	Ch. 0					
	Pulse-density modulation interface	Ch. 0					
	Phase-counting interface	Ch. 0 and 1					
	Parallel data capture unit	Available					Not available

Table 1.2 Comparison of Functions for Different Packages (2/2)

Functions		RX74M Group					
Package		**320-Pin LFBGA**	**224-Pin LFBGA**	**176-Pin LFBGA**	**176-Pin LFQFP**	**144-Pin LFQFP**	**100-Pin LFQFP**
16-bit A/D converter	Unit 0	AN000 to 007 (8 channels)				AN000 to 005 (6 channels)	AN000, 002, 004 (3 channels)
	Unit 1	AN008 to 035 (28 channels)	AN014 to 035 (22 channels)			AN014 to 033 (20 channels)	AN014, 017 to 031 (16 channels)
	Unit 2	AN008 to 035 (28 channels)	AN014 to 035 (22 channels)			AN014 to 033 (20 channels)	AN014, 017 to 031 (16 channels)
12-bit D/A converter		Ch. 0 and 1					Ch. 0
Temperature sensor		Available					
Arithmetic unit for trigonometric functions		Available					
Delta-sigma modulator interface		Unit 0 and 1					Unit 0
CRC calculator		Available					
Data operation circuit		Available					
Clock frequency accuracy measurement circuit		Available					
Renesas Secure IP		Available					
Event link controller		Available					

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/2)

Group	Part No.	Package	Code MRAM Capacity	RAM Capacity	Operating Frequency (Max.)	CANFD	ESC	Junction tempera-ture (°C)
RX74M	R5K574MCC4FC	PLQP0176KJ-A	1 Mbyte	1.5 Mbytes	480 MHz	Available*1	Available	–40 to +125
	R5K574MCD4FC	PLQP0176KJ-A	1 Mbyte	1.5 Mbytes	480 MHz	Available	Available	–40 to +125
	R5K574M6C4FC	PLQP0176KJ-A	512 Kbytes	1.5 Mbytes	480 MHz	Available*1	Available	–40 to +125
	R5K574M6D4FC	PLQP0176KJ-A	512 Kbytes	1.5 Mbytes	480 MHz	Available	Available	–40 to +125
	R5K574MCC4FB	PLQP0144KA-B	1 Mbyte	1.5 Mbytes	480 MHz	Available*1	Available	–40 to +125
	R5K574MCD4FB	PLQP0144KA-B	1 Mbyte	1.5 Mbytes	480 MHz	Available	Available	–40 to +125
	R5K574M6C4FB	PLQP0144KA-B	512 Kbytes	1.5 Mbytes	480 MHz	Available*1	Available	–40 to +125
	R5K574M6D4FB	PLQP0144KA-B	512 Kbytes	1.5 Mbytes	480 MHz	Available	Available	–40 to +125
	R5K574MCC4FP	PLQP0100KP-A	1 Mbyte	1.5 Mbytes	480 MHz	Available*1	Available	–40 to +125
	R5K574MCD4FP	PLQP0100KP-A	1 Mbyte	1.5 Mbytes	480 MHz	Available	Available	–40 to +125
	R5K574M6C4FP	PLQP0100KP-A	512 Kbytes	1.5 Mbytes	480 MHz	Available*1	Available	–40 to +125
	R5K574M6D4FP	PLQP0100KP-A	512 Kbytes	1.5 Mbytes	480 MHz	Available	Available	–40 to +125
	R5K574MCA4AE	PLBG0320GD-A	1 Mbyte	1.5 Mbytes	600 MHz	Available*1	Available	–40 to +125
	R5K574MCB4AE	PLBG0320GD-A	1 Mbyte	1.5 Mbytes	600 MHz	Available	Available	–40 to +125
	R5K574M6A4AE	PLBG0320GD-A	512 Kbytes	1.5 Mbytes	600 MHz	Available*1	Available	–40 to +125
	R5K574M6B4AE	PLBG0320GD-A	512 Kbytes	1.5 Mbytes	600 MHz	Available	Available	–40 to +125
	R5K574MCA4BD	PLBG0224GE-A	1 Mbyte	1.5 Mbytes	600 MHz	Available*1	Available	–40 to +125
	R5K574MCB4BD	PLBG0224GE-A	1 Mbyte	1.5 Mbytes	600 MHz	Available	Available	–40 to +125
	R5K574M6A4BD	PLBG0224GE-A	512 Kbytes	1.5 Mbytes	600 MHz	Available*1	Available	–40 to +125
	R5K574M6B4BD	PLBG0224GE-A	512 Kbytes	1.5 Mbytes	600 MHz	Available	Available	–40 to +125
	R5K574MCA4BG	PLBG0176GG-A	1 Mbyte	1.5 Mbytes	600 MHz	Available*1	Available	–40 to +125
	R5K574MCB4BG	PLBG0176GG-A	1 Mbyte	1.5 Mbytes	600 MHz	Available	Available	–40 to +125
	R5K574M6A4BG	PLBG0176GG-A	512 Kbytes	1.5 Mbytes	600 MHz	Available*1	Available	–40 to +125
	R5K574M6B4BG	PLBG0176GG-A	512 Kbytes	1.5 Mbytes	600 MHz	Available	Available	–40 to +125
	R5K574MCE4FC	PLQP0176KJ-A	1 Mbyte	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574MCF4FC	PLQP0176KJ-A	1 Mbyte	1.5 Mbytes	300 MHz	Available	Available	–40 to +125
	R5K574M6E4FC	PLQP0176KJ-A	512 Kbytes	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574M6F4FC	PLQP0176KJ-A	512 Kbytes	1.5 Mbytes	300 MHz	Available	Available	–40 to +125
	R5K574MCE4FB	PLQP0144KA-B	1 Mbyte	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574MCF4FB	PLQP0144KA-B	1 Mbyte	1.5 Mbytes	300 MHz	Available	Available	–40 to +125
	R5K574M6E4FB	PLQP0144KA-B	512 Kbytes	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574M6F4FB	PLQP0144KA-B	512 Kbytes	1.5 Mbytes	300 MHz	Available	Available	–40 to +125
	R5K574MCE4FP	PLQP0100KP-A	1 Mbyte	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574MCF4FP	PLQP0100KP-A	1 Mbyte	1.5 Mbytes	300 MHz	Available	Available	–40 to +125
	R5K574M6E4FP	PLQP0100KP-A	512 Kbytes	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574M6F4FP	PLQP0100KP-A	512 Kbytes	1.5 Mbytes	300 MHz	Available	Available	–40 to +125
	R5K574MCE4AE	PLBG0320GD-A	1 Mbyte	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574MCF4AE	PLBG0320GD-A	1 Mbyte	1.5 Mbytes	300 MHz	Available	Available	–40 to +125
	R5K574M6E4AE	PLBG0320GD-A	512 Kbytes	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574M6F4AE	PLBG0320GD-A	512 Kbytes	1.5 Mbytes	300 MHz	Available	Available	–40 to +125

Table 1.3 List of Products (2/2)

Group	Part No.	Package	Code MRAM Capacity	RAM Capacity	Operating Frequency (Max.)	CANFD	ESC	Junction tempera-ture (°C)
RX74M	R5K574MCE4BD	PLBG0224GE-A	1 Mbyte	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574MCF4BD	PLBG0224GE-A	1 Mbyte	1.5 Mbytes	300 MHz	Available	Available	–40 to +125
	R5K574M6E4BD	PLBG0224GE-A	512 Kbytes	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574M6F4BD	PLBG0224GE-A	512 Kbytes	1.5 Mbytes	300 MHz	Available	Available	–40 to +125
	R5K574MCE4BG	PLBG0176GG-A	1 Mbyte	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574MCF4BG	PLBG0176GG-A	1 Mbyte	1.5 Mbytes	300 MHz	Available	Available	–40 to +125
	R5K574M6E4BG	PLBG0176GG-A	512 Kbytes	1.5 Mbytes	300 MHz	Available*1	Available	–40 to +125
	R5K574M6F4BG	PLBG0176GG-A	512 Kbytes	1.5 Mbytes	300 MHz	Available	Available	–40 to +125
	R5K574MCV4FC	PLQP0176KJ-A	1 Mbyte	1.5 Mbytes	480 MHz	Available*1	Not Available	–40 to +125
	R5K574MCW4FC	PLQP0176KJ-A	1 Mbyte	1.5 Mbytes	480 MHz	Available	Not Available	–40 to +125
	R5K574M6V4FC	PLQP0176KJ-A	512 Kbytes	1.5 Mbytes	480 MHz	Available*1	Not Available	–40 to +125
	R5K574M6W4FC	PLQP0176KJ-A	512 Kbytes	1.5 Mbytes	480 MHz	Available	Not Available	–40 to +125
	R5K574MCV4FB	PLQP0144KA-B	1 Mbyte	1.5 Mbytes	480 MHz	Available*1	Not Available	–40 to +125
	R5K574MCW4FB	PLQP0144KA-B	1 Mbyte	1.5 Mbytes	480 MHz	Available	Not Available	–40 to +125
	R5K574M6V4FB	PLQP0144KA-B	512 Kbytes	1.5 Mbytes	480 MHz	Available*1	Not Available	–40 to +125
	R5K574M6W4FB	PLQP0144KA-B	512 Kbytes	1.5 Mbytes	480 MHz	Available	Not Available	–40 to +125
	R5K574MCV4FP	PLQP0100KP-A	1 Mbyte	1.5 Mbytes	480 MHz	Available*1	Not Available	–40 to +125
	R5K574MCW4FP	PLQP0100KP-A	1 Mbyte	1.5 Mbytes	480 MHz	Available	Not Available	–40 to +125
	R5K574M6V4FP	PLQP0100KP-A	512 Kbytes	1.5 Mbytes	480 MHz	Available*1	Not Available	–40 to +125
	R5K574M6W4FP	PLQP0100KP-A	512 Kbytes	1.5 Mbytes	480 MHz	Available	Not Available	–40 to +125
	R5K574MCT4AE	PLBG0320GD-A	1 Mbyte	1.5 Mbytes	600 MHz	Available*1	Not Available	–40 to +125
	R5K574MCU4AE	PLBG0320GD-A	1 Mbyte	1.5 Mbytes	600 MHz	Available	Not Available	–40 to +125
	R5K574M6T4AE	PLBG0320GD-A	512 Kbytes	1.5 Mbytes	600 MHz	Available*1	Not Available	–40 to +125
	R5K574M6U4AE	PLBG0320GD-A	512 Kbytes	1.5 Mbytes	600 MHz	Available	Not Available	–40 to +125
	R5K574MCT4BD	PLBG0224GE-A	1 Mbyte	1.5 Mbytes	600 MHz	Available*1	Not Available	–40 to +125
	R5K574MCU4BD	PLBG0224GE-A	1 Mbyte	1.5 Mbytes	600 MHz	Available	Not Available	–40 to +125
	R5K574M6T4BD	PLBG0224GE-A	512 Kbytes	1.5 Mbytes	600 MHz	Available*1	Not Available	–40 to +125
	R5K574M6U4BD	PLBG0224GE-A	512 Kbytes	1.5 Mbytes	600 MHz	Available	Not Available	–40 to +125
	R5K574MCT4BG	PLBG0176GG-A	1 Mbyte	1.5 Mbytes	600 MHz	Available*1	Not Available	–40 to +125
	R5K574MCU4BG	PLBG0176GG-A	1 Mbyte	1.5 Mbytes	600 MHz	Available	Not Available	–40 to +125
	R5K574M6T4BG	PLBG0176GG-A	512 Kbytes	1.5 Mbytes	600 MHz	Available*1	Not Available	–40 to +125
	R5K574M6U4BG	PLBG0176GG-A	512 Kbytes	1.5 Mbytes	600 MHz	Available	Not Available	–40 to +125

Note 1. Products with this part number support only CAN 2.0 protocol.

R 5 K 5 7 4 M C A 4 F C # 1 0

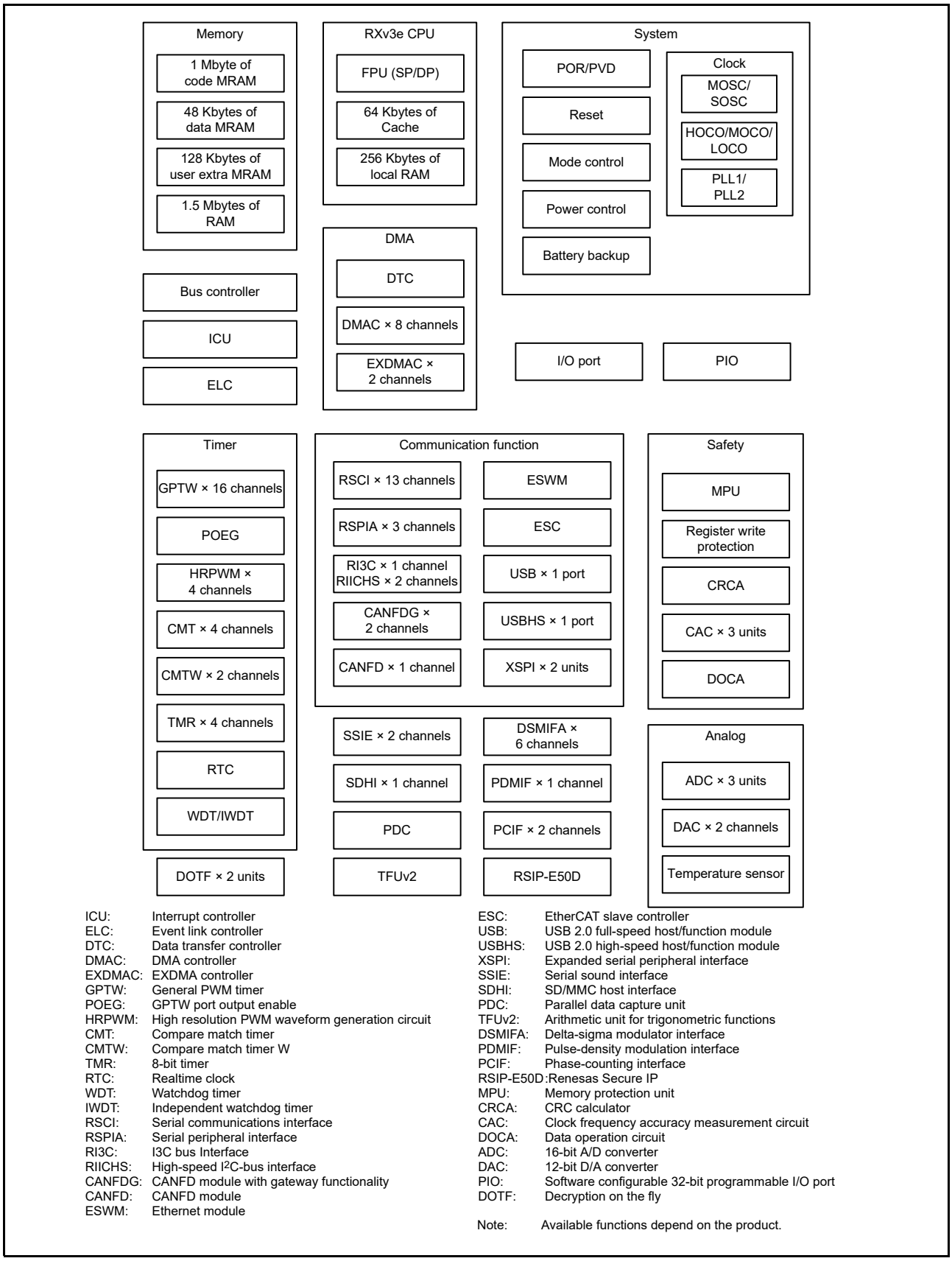
- 0: Production identification code
- 1: Packing
- FC: Package type, number of pins, and pin pitch
  - AE: LFBGA/320/0.80
  - BD: LFBGA/224/0.80
  - BG: LFBGA/176/0.80
  - FC: LFQFP/176/0.50
  - FB: LFQFP/144/0.50
  - FP: LFQFP/100/0.50
- 4: 4 : Junction temperature: –40 to +125°C
- A: A : Operating frequency: 600 MHz, Only CAN 2.0 protocol supported, with ESC
  - B : Operating frequency: 600 MHz, CAN FD protocol supported, with ESC
  - C : Operating frequency: 480 MHz, Only CAN 2.0 protocol supported, with ESC
  - D : Operating frequency: 480 MHz, CAN FD protocol supported, with ESC
  - E : Operating frequency: 300 MHz, Only CAN 2.0 protocol supported, with ESC
  - F : Operating frequency: 300 MHz, CAN FD protocol supported, with ESC
  - T : Operating frequency: 600 MHz, Only CAN 2.0 protocol supported, without ESC
  - U : Operating frequency: 600 MHz, CAN FD protocol supported, without ESC
  - V : Operating frequency: 480 MHz, Only CAN 2.0 protocol supported, without ESC
  - W: Operating frequency: 480 MHz, CAN FD protocol supported, without ESC
- C: Code MRAM and RAM capacity
  - C : 1 Mbyte/1.5 Mbytes
  - 6 : 512 Kbytes/1.5 Mbytes
- 4M: Group name
  - RX74M Group
- 57: Series name
  - RX700 Series
- K: Type of memory
  - K : MRAM microcontroller
- 5: Renesas MCU
- R: Renesas semiconductor product

Note: Visit the Renesas Electronics Web site to check and obtain the ordering part numbers.

Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICU: Interrupt controller
ELC: Event link controller
DTC: Data transfer controller
DMAC: DMA controller
EXDMAC: EXDMA controller
GPTW: General PWM timer
POEG: GPTW port output enable
HRPWM: High resolution PWM waveform generation circuit
CMT: Compare match timer
CMTW: Compare match timer W
TMR: 8-bit timer
RTC: Realtime clock
WDT: Watchdog timer
IWDT: Independent watchdog timer
RSCI: Serial communications interface
RSPIA: Serial peripheral interface
RI3C: I3C bus Interface
RIICHS: High-speed I^{2}C-bus interface
CANFDG: CANFD module with gateway functionality
CANFD: CANFD module
ESWM: Ethernet module
ESC: EtherCAT slave controller
USB: USB 2.0 full-speed host/function module
USBHS: USB 2.0 high-speed host/function module
XSPI: Expanded serial peripheral interface
SSIE: Serial sound interface
SDHI: SD/MMC host interface
PDC: Parallel data capture unit
TFUv2: Arithmetic unit for trigonometric functions
DSMIFA: Delta-sigma modulator interface
PDMIF: Pulse-density modulation interface
PCIF: Phase-counting interface
RSIP-E50D: Renesas Secure IP
MPU: Memory protection unit
CRCA: CRC calculator
CAC: Clock frequency accuracy measurement circuit
DOCA: Data operation circuit
ADC: 16-bit A/D converter
DAC: 12-bit D/A converter
PIO: Software configurable 32-bit programmable I/O port
DOTF: Decryption on the fly

Note: Available functions depend on the product.

Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/8)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCC2	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	The pin setting depends on the power-supply mode.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Switching regulator	VCC_DCDC	Input	Power supply pin of the switching regulator
	VLO	Output	Output pin of the switching regulator Connect this pin to an external inductor and capacitor.
	VSS_DCDC	Input	Ground pin of the switching regulator
Clock	XTAL	Output	Input/output pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	EBCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	XCOUT	Output	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
	EXCIN	Input	External sub-clock input pin
	CLKOUT	Output	Clock output pin.
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Operating mode control	MD	Input	Input pin for setting the operating mode. The signal level on this pin must not be changed during operation.
System control	RES#/RSTOUT#	I/O	Reset signal input pin. This MCU enters the reset state when this signal goes low.
On-chip emulator	FINED	I/O	FINE interface pin
	TMS	Input	On-chip emulator or boundary scan pins.
	TDI	Input	
	TCK	Input	
	TDO	Output	
	SWDIO	I/O	Serial wire debugging data input/output pin
	SWCLK	Input	Serial wire clock pin
Address bus	A0 to A23	Output	Output pins for the address
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus

Table 1.4 Pin Functions (2/8)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16 and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
	BREQ#	Input	External bus request signal from an external device
	BACK#	Output	External bus acknowledge signal from the MCU
SDRAM interface	CKE	Output	SDRAM clock enable signal
	SDCS#	Output	SDRAM chip select signal
	RAS#	Output	SDRAM row address strobe signal
	CAS#	Output	SDRAM column address strobe signal
	WE#	Output	SDRAM write enable pin
	DQM0 to DQM3	Output	SDRAM I/O data mask enable signals
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ31, IRQ0-DS to IRQ31-DS	Input	Maskable interrupt request pins
General PWM timer	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	Input pins for the external trigger signals
	GTIOC0A to GTIOC15A, GTIOC0B to GTIOC15B	I/O	Input capture input/output compare output/PWM output pins
	GTCPPO0 to GTCPPO15	Output	PWM synchronous output
	GTIU, GTIV, GTIW	Input	Hall sensor input pins
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W-phase)
	GTADSM0, GTADSM1	Output	Output pins for monitoring A/D conversion start requests.
GPTW port output enable	POEGA, POEGB, POEGC, POEGD	Input	Input pins for request signals to place GPTW outputs in the high-impedance state
8-bit timer	TMO0 to TMO3	Output	Compare match output pins
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter
	TMRI0 to TMRI3	Input	Input pins for the counter reset
Compare match timer W	TIC0 to TIC3	Input	Input pins for CMTW
	TOC0 to TOC3	Output	Output pins for CMTW

Table 1.4 Pin Functions (3/8)

Classifications	Pin Name	I/O	Description
Serial communications interface	• Asynchronous mode/clock synchronous mode		
	SCK000 to SCK012	I/O	Input/output pins for the clock
	RXD000 to RXD012	Input	Input pins for received data
	TXD000 to TXD012	Output	Output pins for transmitted data
	CTS000# to CTS012#	Input	Input pins for controlling the start of transmission and reception
	RTS000# to RTS012#	Output	Output pins for controlling the start of transmission and reception
	DE000 to DE012	Output	Output pins for controlling the RS-485 driver
	• Simple I^{2}C mode		
	SSCL000 to SSCL012	I/O	Input/output pins for the I^{2}C clock
	SSDA000 to SSDA012	I/O	Input/output pins for the I^{2}C data
	• Simple SPI mode		
	SCK000 to SCK012	I/O	Input/output pins for the clock
	SMISO000 to SMISO012	I/O	Input/output pins for slave transmission of data
	SMOSI000 to SMOSI012	I/O	Input/output pins for master transmission of data
	SS000# to SS012#	Input	Chip-select input pins
	• HBS support mode		
	RXD000 to RXD012	Input	Input pins for received data
	TXDA000 to TXDA012	Output	Output pins for transmitted data
	TXDB000 to TXDB012		
I3C bus interface	SCL00	I/O	Input/output pins for clocks
	SDA00	I/O	Input/output pins for data
High-speed I^{2}C-bus interface	SCLHS1, SCLHS2	I/O	Input/output pins for clocks
	SDAHS1, SDAHS2	I/O	Input/output pins for data
Ethernet module	• RMII mode		
	RMII0_REF50CK, RMII1_REF50CK	Input	50-MHz reference clocks. These pins input reference signals for transmission/reception timing in RMII mode.
	RMII0_CRS_DV, RMII1_CRS_DV	Input	These pins indicate that there are carrier detection signals and valid receive data on RMIIn_RXD1 and RMIIn_RXD0 in RMII mode.
	RMII0_TXD0, RMII0_TXD1, RMII1_TXD0, RMII1_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1, RMII1_RXD0, RMII1_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TX_EN, RMII1_TX_EN	Output	Output pin for data transmit enable signal in RMII mode
	RMII0_RX_ER, RMII1_RX_ER	Input	These pins indicate an error has occurred during reception of data in RMII mode.
	• RGMII mode		
	RGMII0_TXC, RGMII1_TXC	Output	Transmission clock signals in RGMII mode
	RGMII0_RXC, RGMII1_RXC	Input	Reception clock signals in RGMII mode
	RGMII0_TX_CTL, RGMII1_TX_CTL	Output	Control of transmission in RGMII mode
	RGMII0_TXD0 to RGMII0_TXD3, RGMII1_TXD0 to RGMII1_TXD3	Output	4-bit transmission data in RGMII mode
	RGMII0_RX_CTL, RGMII1_RX_CTL	Input	Control of reception in RGMII mode

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Ethernet module	RGMII0_RXD0 to RGMII0_RXD3, RGMII1_RXD0 to RGMII1_RXD3	Input	4-bit reception data in RGMII mode
	• GMII/MII mode		
	ET0_GTX_CLK, ET1_GTX_CLK	Output	1000-Mbps transmission clock pin
	ET0_CRS, ET1_CRS	Input	Carrier detection/data reception enable pins
	ET0_RX_DV, ET1_RX_DV	Input	These pins indicate that there are valid receive data.
	ET0_TXD0 to ET0_TXD7, ET1_TXD0 to ET1_TXD7	Output	8 bits of GMII transmit data/4 bits of MII transmit data
	ET0_RXD0 to ET0_RXD7, ET1_RXD0 to ET1_RXD7	Input	8 bits of GMII receive data/4 bits of MII receive data
	ET0_TX_EN, ET1_TX_EN	Output	Transmit enable pins.
	ET0_TX_ER, ET1_TX_ER	Output	Transmit error pins. These pins function as signals notifying the PHY-LSI of an error during transmission.
	ET0_RX_ER, ET1_RX_ER	Input	Receive error pins. These pins function as signals to recognize an error during reception.
	ET0_TX_CLK, ET1_TX_CLK	I/O	100-Mbps/10-Mbps transmission clock pins (input for MII, output for MAC-to-MAC connection)
	ET0_RX_CLK, ET1_RX_CLK	Input	Receive clock pins.
	ET0_COL, ET1_COL	Input	Input collision detection signals.
	• Common		
	ET0_LINKSTA, ET1_LINKSTA	Input	Input link status from the PHY-LSI.
	ET0_INT, ET1_INT	Input	Input for an interrupt signal from PHY-LSI
	ET0_WOL, ET1_WOL	Output	Signals indicating receipt of Magic Packet.
	ET0_MDC, ET1_MDC	Output	Output reference clock signals for information transfer via ETn_MDIO.
	ET0_MDIO, ET1_MDIO	I/O	Input or output bidirectional signals for exchange of management information between this MCU and the PHY-LSI.
	GPTP_CAPTURE0, GPTP_CAPTURE1	Input	Media clock capture input
	GPTP_MATCH0, GPTP_MATCH1	Output	Media clock recovery output
	GPTP0_PPS, GPTP1_PPS	Output	PPS signals
	GPTP_PTPOUT0 to GPTP_PTPOUT3	Output	PTP pulse generation signals
	ET_TAS_STA0 to ET_TAS_STA3	Output	TAS state monitor
	ETHPHYCLK	Output	Clock output pin for PHY clock input (shared with the EtherCAT slave controller (ESC))
EtherCAT slave controller	• MII mode		
	CAT0_LINKSTA, CAT1_LINKSTA	Input	PHY link signal input pins
	CAT0_RX_CLK, CAT1_RX_CLK	Input	Receive clock input pins
	CAT0_RX_DV, CAT1_RX_DV	Input	Receive data enabling signal input pins
	CAT0_ERXD0 to CAT0_ERXD3, CAT1_ERXD0 to CAT1_ERXD3	Input	Receive data signal input pins
	CAT0_RX_ER, CAT1_RX_ER	Input	Receive data error signal input pins

Table 1.4 Pin Functions (5/8)

Classifications	Pin Name	I/O	Description
EtherCAT slave controller	CAT0_TX_CLK, CAT1_TX_CLK	Input	Transmit clock input pins
	CAT0_TX_EN, CAT1_TX_EN	Output	Transmit enabling signal output pins
	CAT0_ETXD0 to CAT0_ETXD3, CAT1_ETXD0 to CAT1_ETXD3	Output	Transmit data signal output pins
	CAT0_MDC	Output	Management interface clock output pin
	CAT0_MDIO	I/O	Management data signal input/output pin
	ETHPHYCLK	Output	Clock output pin for PHY clock input (shared with the layer 3 Ethernet switching module (ESWM))
	• Exclusively for EtherCAT		
	CATRESTOUT	Output	Output signal for resetting the PHY chip
	CATLEDRUN	Output	EtherCAT run LED signal output pin
	CATIRQ	Output	EtherCAT IRQ signal output pin
	CATLEDSTER	Output	EtherCAT dual-color state LED signal output pin
	CATLEDERR	Output	EtherCAT error LED signal output pin
	CATLINKACT0, CATLINKACT1	Output	EtherCAT link/activity LED signal output pins
	CATSYNC0, CATSYNC1	Output	EtherCAT sync signal output pins
	CATLATCH0, CATLATCH1	Input	EtherCAT latch signal output pins
	CATI2CCLK	Output	EtherCAT EEPROM I^2C clock signal output pin
	CATI2CDATA	I/O	EtherCAT EEPROM I^2C data signal input/output pin
USB 2.0 host/function module	VCC_USB, VCC_USBHS	Input	Power supply pins
	VSS_USB, VSS_USBHS	Input	Ground pins
	AVCC_USBHS	Input	Analog voltage supply pin for USBHS
	AVSS_USBHS	Input	Analog ground pin for USBHS
	USBHS_RREF	I/O	Reference voltage supply pin for USBHS
	USB0_DP, USBHS_DP	I/O	Input or output USB transceiver D+ data.
	USB0_DM, USBHS_DM	I/O	Input or output USB transceiver D- data.
	USB0_EXICEN, USBHS_EXICEN	Output	Connect to the OTG power IC.
	USB0_ID, USBHS_ID	Input	Connect to the OTG power IC.
	USB0_VBUSEN, USBHS_VBUSEN	Output	USB VBUS power enable pins
	USB0_OVRCURA/ USB0_OVRCURB, USBHS_OVRCURA/ USBHS_OVRCURB, USB0_OVRCURA-DS/ USB0_OVRCURB-DS, USBHS_OVRCURA-DS/ USBHS_OVRCURB-DS	Input	USB overcurrent pins
	USB0_VBUS, USBHS_VBUS, USB0_VBUS-DS, USBHS_VBUS-DS	Input	USB cable connection/disconnection detection input pin
CANFD module	CRX0, CRX1, CRX2	Input	CAN input pins
	CTX0, CTX1, CTX2	Output	CAN output pins

Table 1.4 Pin Functions (6/8)

Classifications	Pin Name	I/O	Description
Serial peripheral interface	RSPCK0 to RSPCK2	I/O	Clock input/output pins
	MOSI0 to MOSI2	I/O	Input or output data output from the master
	MISO0 to MISO2	I/O	Input or output data output from the slave
	SSL00, SSL10, SSL20	I/O	Input or output pins for slave selection
	SSL01 to SSL03, SSL11 to SSL13, SSL21 to SSL23	Output	Output pins for slave selection
Expanded serial peripheral interface	XSPI0_CK, XSPI1_CK	I/O	Clock input/output pins (output in the controller mode; input in the target mode)
	XSPI0_CKN#, XSPI1_CKN#	Output	Inverted clock output (output in the controller mode; N/A in the target mode)
	XSPI0_CS0#, XSPI0_CS1#, XSPI1_CS0#, XSPI1_CS1#	I/O	Chip select signals (output in the controller mode; input in the target mode)
	XSPI0_DS, XSPI1_DS	I/O	Read data strobe/write data mask signal
	XSPI0_IO0 to XSPI0_IO7, XSPI1_IO0 to XSPI1_IO7	I/O	Data input/output pins
	XSPI0_RESET0#, XSPI0_RESET1#, XSPI1_RESET0#, XSPI1_RESET1#	I/O	Signals from the controller device to reset the target device (output in the controller mode; input in the target mode)
	XSPI0_ECS0#, XSPI0_ECS1#, XSPI1_ECS0#, XSPI1_ECS1#	Input	Signals that indicate the state of error correction in the target device
	XSPI0_INT0#, XSPI1_INT0#	I/O	Interrupt signals from the target device (input in the controller mode; output in the target mode)
	XSPI0_INT1#, XSPI1_INT1#	Input	Interrupt signals from the target device (input in the controller mode; N/A in the target mode)
	XSPI0_RSTO0#, XSPI1_RSTO0#	I/O	Signals from the target device to reset the controller device (input in the controller mode; output in the target mode)
	XSPI0_RSTO1#, XSPI1_RSTO1#	Input	Signals from the target device to reset the controller device (input in the controller mode; N/A in the target mode)
	XSPI0_WP0#, XSPI0_WP1#, XSPI1_WP0#, XSPI1_WP1#	Output	Signals to control protection of the target device against writing by the controller device
Serial sound interface	SSIBCK0, SSIBCK1	I/O	SSIE serial bit-clock pins
	SSILRCK0, SSILRCK1	I/O	LR clock
	SSITXD0, SSITXD1	Output	Serial data output pins
	SSIRXD0, SSIRXD1	Input	Serial data input pins
	AUDIO_CLK	Input	External clock pin for audio (input for an oversampling clock)
SD/MMC host interface	SD0_CLK	Output	SD clock output pin
	SD0_CMD	I/O	SD command output or response input signal pin
	SD0_DAT0 to SD0_DAT7	I/O	SD/MMC data bus pins
	SD0_CD	Input	SD card detection pin
	SD0_WP	Input	SD write-protect signal
Delta-sigma modulator interface	DSM0_CLK0 to DSM0_CLK2, DSM1_CLK0 to DSM1_CLK2	I/O	Input/output pins for the clock
	DSM0_DAT0 to DSM0_DAT2, DSM1_DAT0 to DSM1_DAT2	Input	Input pins for data

Table 1.4 Pin Functions (7/8)

Classifications	Pin Name	I/O	Description
Parallel data capture unit	PIXCLK	Input	Image transfer clock pin
	VSYNC	Input	Vertical synchronization signal pin
	HSYNC	Input	Horizontal synchronization signal pin
	PIXD0 to PIXD7	Input	8-bit image data pins
	PCKO	Output	Output pin for dot clock
Pulse-density modulation interface	PDMCLK0	Output	Output pin for the clock
	PDMDAT0	Input	Input pin for data
Phase-counting interface	PCINA0, PCINA1	Input	A-phase input pins
	PCINB0, PCINB1	Input	B-phase input pins
	PCINZ0, PCINZ1	Input	Z-phase input pins
	PCOUTA0, PCOUTA1	Output	A-phase output pins
	PCOUTB0, PCOUTB1	Output	B-phase output pins
	PCOUTZ0, PCOUTZ1	Output	Z-phase output pins
Realtime clock	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
Battery backup	TAMPI0 to TAMPI2	Input	Input pins for detecting tampering
16-bit A/D converter	AN000 to AN035	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0# to ADTRG2#	Input	Input pins for the external trigger signals that start the A/D conversion
	ADST0 to ADST2	Output	Scan period monitor output
	ADCNV0 to ADCNV2	Output	Successive approximation period monitor output
	ADSYNC	Output	Synchronous A/D conversion start signal monitor output
12-bit D/A converter	DA0, DA1	Output	Output pins for the analog signals to be processed by the D/A converter
Analog power supply	AVCC0	Input	Analog power supply pin for the 16-bit A/D converter, and analog power supply and reference voltage pin for the D/A converter.
	AVSS0	Input	Analog ground pin for the 16-bit A/D converter, and analog ground and reference ground pin for the D/A converter
	VREFH0	Input	Analog reference voltage supply pin for the 16-bit A/D converter
	VREFL0	Input	Analog reference ground pin for the 16-bit A/D converter
	VREFH00 to VREFH02*1	Input	Analog reference voltage supply pin for the 16-bit A/D converter
	VREFL00 to VREFL02*1	Input	Analog reference ground pin for the 16-bit A/D converter
Software Configurable 32-Bit Programmable I/O Port	PIO_000 to PIO_063	I/O	Pins composing the software configured general-purpose I/O port
I/O ports	P000 to P015	I/O	16-bit input/output pins
	P100 to P115	I/O	16-bit input/output pins
	P200 to P215	I/O	16-bit input/output pins
	P300 to P312, P315	I/O	14-bit input/output pins (P305, P308, P309: input pin)
	P400 to P415	I/O	16-bit input/output pins
	P500 to P515	I/O	16-bit input/output pins
	P600 to P607	I/O	8-bit input/output pins
	P700 to P715	I/O	16-bit input/output pins
	P800 to P807	I/O	8-bit input/output pins
	P900 to P907	I/O	8-bit input/output pins
	PA00 to PA07	I/O	8-bit input/output pins
	PB00 to PB07	I/O	8-bit input/output pins

Table 1.4 Pin Functions (8/8)

Classifications	Pin Name	I/O	Description
I/O ports	PC00 to PC07	I/O	8-bit input/output pins
	PD00 to PD07	I/O	8-bit input/output pins
	PE00 to PE07	I/O	8-bit input/output pins
	PF00 to PF09	I/O	10-bit input/output pins
	PG00 to PG15	I/O	16-bit input/output pins

Note: Note the following points regarding pin names. For details, refer to section 1.6, List of Pin and Pin Functions.
- Suffixes such as “-A” or “-B” appended to pin names indicate pin group identifiers. Electrical characteristics were evaluated per pin group. AC electrical characteristics are only guaranteed when pins within the same group are used together.
- When a pin function has “-DS” appended to its name, it can also be used as a trigger for release from deep software standby mode.

Note 1. This pin is only present in 320-pin products.

1.5 Pin Assignments

1.5.1 320-Pin LFBGA

RX74M Group
PLBG0320GD-A (320-pin LFBGA)
(Upper Perspective View)

INDEX

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	P514	P515	PC01	PC03	PC04	PC07	P801	P800	VLO	VSS_DCDC	VSS_DCDC	VCC_DCDC	P504	P103	P104	P106	P200	P300/TMS	VSS	A
B	PG03	P512	P513	PC00	PC02	VSS	PC05	PC06	P802	VLO	VSS_DCDC	VSS_DCDC	VCC_DCDC	P505	P102	VSS	P107	P201	P301/TCK	P302/TDO	B
C	PG02	PG01	PB01	PB03	PB04	PB06	PB07	PB05	P803	VLO	VLO	VCC_DCDC	VCC_DCDC	P506	P105	P805	P806	P807	P304	P303/TDI	C
D	PA06	PG00	P511															P108	P109	P110	D
E	PA05	PA07	P510		PG05	PB02	PB00	VCC	VCC	P500	P502	P100	VCC	VCC	P507	P804		P111	P112	P113	E
F	PA03	PA04	P509		PG07	PG06	PG04	VSS	VSS	P501	P503	P101	VSS	VSS	PF02	P115		P114	VSS	VCC	F
G	PA02	PA01	P508		VCC	VSS									PF03	PF04		VSS_USB	PF00/USB0_DP	PF01/USB0_DM	G
H	PA00	PG13	PG15		VCC	VSS		VSS	VCL	VSS	VSS	VCL	VSS		P204	P203		PF05	VCC_USB	VCC_USB	H
J	PG11	PG14	PG12		VCC	VSS		VSS	VCL	VSS	VSS	VSS	VCL		P205	P202		AVSS_USBHS	USBHS_DP	USBHS_DM	J
K	PG09	PG10	P705		P704	P702		VCL	VSS	VCL	VCL	VCC	VSS		P207	P206		USBHS_RREF	VSS_USBHS	VCC_USBHS	K
L	PG08	VSS	P707		P706	P703		VSS	VSS	VCL	VCL	VSS	VCC		P310	P305/NMI		AVCC_USBHS	VCC	VCC	L
M	P701	P715	P714		VCC	VSS		VCL	VCL	VSS	VSS	VSS	VCL		P312	P311		VSS	P306/EXTAL	P307/XTAL	M
N	P700	P712	P713		VCC	VSS		VSS	VCL	VSS	VSS	VCL	VSS		P209	P208		P315/MD	VSS	VSS	N
P	PE06	PE07	PF09		VCC	VSS									P211	P210		VSS	P309/XCIN/EXCIN	P308/XCOUT	P
R	PE03	PE05	PF08		P607	P606	VSS	VSS	VSS	P906	P405	P404	VSS	VSS	P215	P214		RES#	VCC	VBATT/VCC	R
T	PE01	PE04	PF07		P604	P602	VCC2	VCC2	VCC2	P907	P406	P407	VCC	VCC	P013	P012		P213	P212	P000	T
U	PE00	PE02	PF06															P008	P009	P001	U
V	P709	P711	P605	P603	P600	P601	P905	P904	AVCC0	AVSS0	VREFL00	VREFH00	P412	P413	P414	P415	P014	P011	P010	P002	V
W	P708	P710	PD05	PD03	VSS	PD02	P902	P900	AVCC0	AVSS0	VREFL01	VREFH01	P403	P401	P411	P409	VSS	P006	P004	P003	W
Y	VSS	PD07	PD06	PD04	PD01	PD00	P903	P901	AVCC0	AVSS0	VREFL02	VREFH02	P402	P400	P410	P408	P015	P007	P005	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.5, List of Pin and Pin Functions (320-Pin LFBGA).

Figure 1.3 Pin Assignment (320-Pin LFBGA)

1.5.2 224-Pin LFBGA

RX74M Group
PLBG0224GE-A (224-pin LFBGA)
(Upper Perspective View)

INDEX

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	VSS	PC03	PC07	P801	P802	VLO	VSS_DCDC	VCC_DCDC	P103	P104	P106	P200	P301/TCK	P302/TDO	VSS	A
B	PC04	PC01	PC05	PC06	P803	VLO	VSS_DCDC	VCC_DCDC	P102	P105	P107	P201	P300/TMS	P303/TDI	P304	B
C	PC00	PC02	PB06	PB05	P800	VLO	P100	VCC_DCDC	P804	P805	P114	P111	P108	P110	P113	C
D	PG00	PG02	PB04	PB07	P502	P500	P101	P504	P506	P806	P109	P115	P112	VSS	VCC	D
E	PG01	PG03	PB02	PB03	VCC	P501	P503	P505	P507	P807	PF02	PF04	PF03	PF00/USB0_DP	PF01/USB0_DM	E
F	PA05	PA07	PB01	PB00	VSS	VCL	VSS	VCC	VSS	VSS	PF05	P202	P203	VCC_USB	VSS_USB	F
G	PA04	PA06	PG05	PG07	PF09	VSS	VCL	VSS	VCL	VCL	P205	P204	VCC_USBHS	USBHS_DP	USBHS_DM	G
H	PA02	PA03	PG06	PG04	PF08	VCC	VSS	VCL	VSS	VCL	P206	AVSS_USBHS	USBHS_RREF	VSS_USBHS	VCC	H
J	PA00	PA01	P703	PF06	PF07	VSS	VCL	VSS	VCL	VSS	P207	P305/NMI	AVCC_USBHS	P307/XTAL	P306/EXTAL	J
K	P707	P706	P702	P605	VSS	VCC	VSS	VCC2	VCL	VSS	P310	P311	P315/MD	VSS	VSS	K
L	P705	P704	P604	P606	VCC2	P904	P906	P407	P406	P215	P209	P312	VCC	P309/XCIN/EXCIN	P308/XCOUT	L
M	P700	P701	P607	P603	P907	P905	P902	P900	P405	P415	P212	P214	RES#	VSS	VBATT/VCC	M
N	PE07	PE04	PE06	P602	P601	P600	P903	P901	P404	P414	P210	P213	P208	P211	P000	N
P	PE05	PE03	PE02	PD07	PD05	PD03	PD02	AVSS0	VREFL0	P403	P401	P006	P004	P003	P001	P
R	VSS	PE01	PE00	PD06	PD04	PD00	PD01	AVCC0	VREFH0	P402	P400	P007	P005	P002	NC	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.6, List of Pin and Pin Functions (224-Pin LFBGA).

Figure 1.4 Pin Assignment (224-Pin LFBGA)

1.5.3 176-Pin LFBGA

INDEX

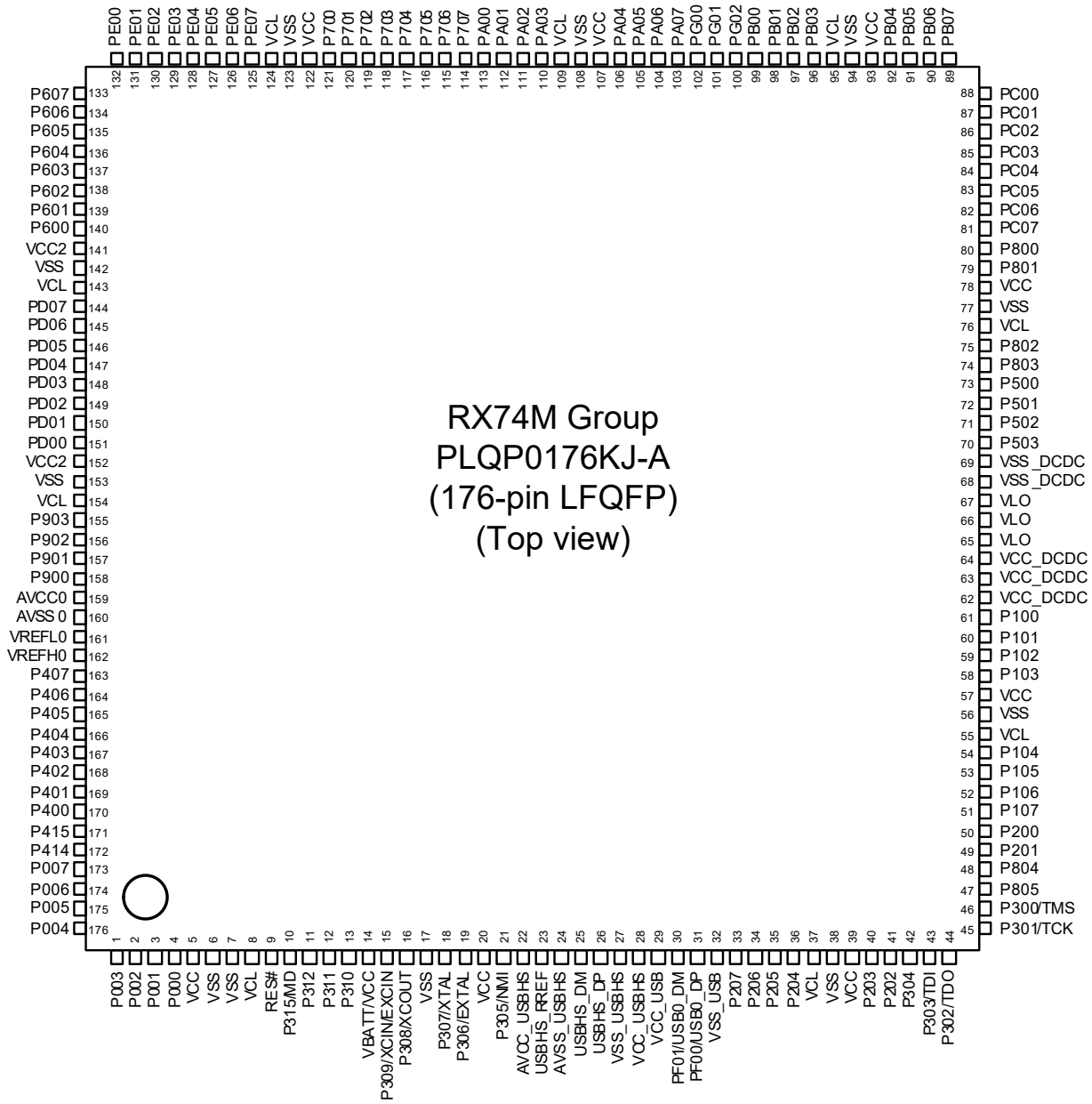
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	PC01	PC03	PC05	PC07	P801	P503	VLO	VSS_DCDC	VCC_DCDC	P102	P106	P200	P805	P301/TCK	P302/TDO	A
B	PC00	PC02	PC04	PC06	P803	P502	VLO	VSS_DCDC	VCC_DCDC	P103	P107	P201	P804	P300/TMS	P303/TDI	B
C	PB06	PB07	P802	VCC	P500	P501	VLO	VCC_DCDC	VCC	P100	P104	P205	P304	P202	P203	C
D	PB04	PB05	PG01	P800	VCC	VSS	VCL	P101	VSS	VCL	P105	VCC	P204	PF00/USB0_DP	PF01/USB0_DM	D
E	PB02	PB03	PG00	VSS								VSS	P206	VSS_USB	VCC_USB	E
F	PB00	PB01	PG02	VCL								VCL	AVSS_USBHS	USBHS_DP	USBHS_DM	F
G	PA06	PA07	P706	VCC								AVCC_USBHS	USBHS_RREF	VSS_USBHS	VCC_USBHS	G
H	PA04	PA05	P707	VSS								P207	VSS	P306/EXTAL	P307/XTAL	H
J	PA02	PA03	P705	VCL								VCL	P305/NMI	VSS	VCC	J
K	PA00	PA01	P702	VCC								VSS	P310	P309/XCIN/EXCIN	P308/XCOUT	K
L	P700	P701	P703	P704								P312	P311	VCC	VBATT/VCC	L
M	PE07	PE03	PD04	PD06	VSS	VCL	VCC2	VSS	VCL	P407	P404	P315/MD	RES#	P001	P000	M
N	PE05	PE04	P607	P604	PD07	PD05	VCC2	VSS	VCL	P406	P405	P415	P414	P003	P002	N
P	PE01	PE02	P606	P603	P601	PD03	PD00	P902	P900	AVSS0	VREFL0	P402	P400	P005	P004	P
R	PE00	PE06	P605	P602	P600	PD02	PD01	P903	P901	AVCC0	VREFH0	P403	P401	P007	P006	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

RX74M Group
PLBG0176GG-A
(176-pin LFBGA)
(Upper Perspective View)

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.7, List of Pin and Pin Functions (176-Pin LFBGA).

Figure 1.5 Pin Assignment (176-Pin LFBGA)

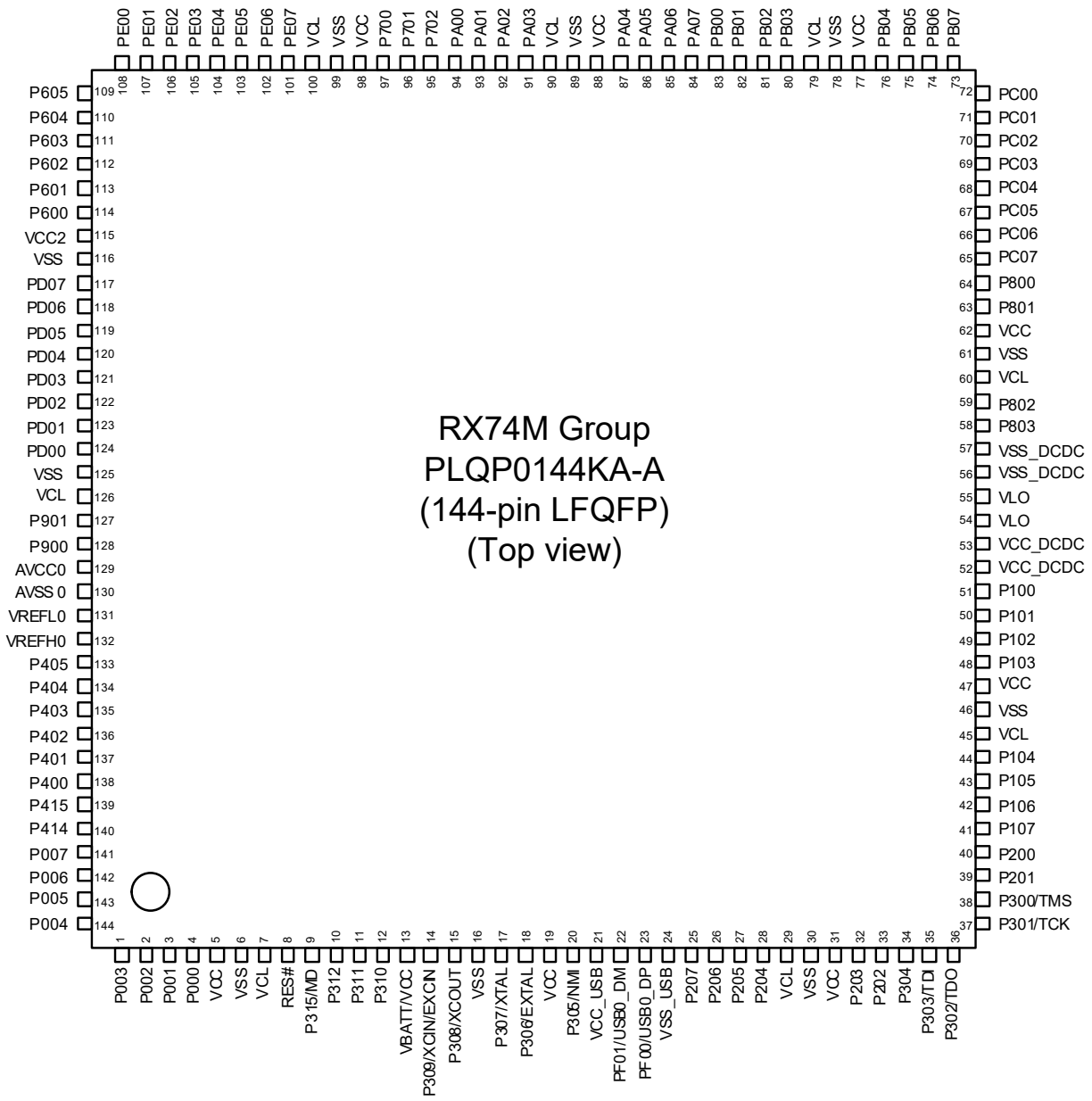
1.5.4 176-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.8, List of Pin and Pin Functions (176-Pin LFQFP).

Figure 1.6 Pin Assignment (176-Pin LFQFP)

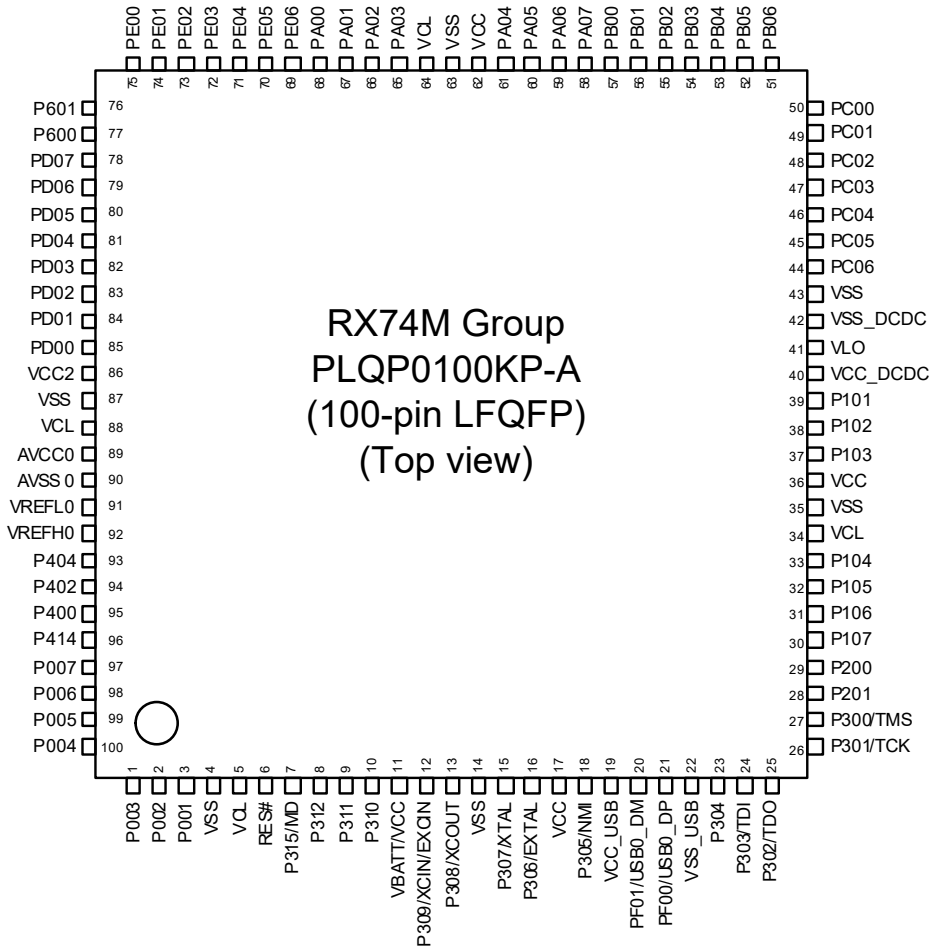
1.5.5 144-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.9, List of Pin and Pin Functions (144-Pin LFQFP).

Figure 1.7 Pin Assignment (144-Pin LFQFP)

1.5.6 100-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, refer to Table 1.10, List of Pin and Pin Functions (100-Pin LFQFP).

Figure 1.8 Pin Assignment (100-Pin LFQFP)

1.6 List of Pin and Pin Functions

1.6.1 320-Pin LFBGA

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (1/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
A1	VSS											
A2		P514	PIO_006	D17-A		GTIOC9A	CTS008#/ SSL23-D	ET0_TXD6-A	SD0_WP	IRQ22		DSM0_CLK0-G
A3		P515	PIO_007	D16-A		GTIOC9B	CTS010#	ET0_TXD7-A	SD0_CD	IRQ23		DSM0_DAT0-G
A4		PC01	PIO_025	D6-A		GTOULO/ GTIOC7B	SCK011-A/ CTS011#/ TXDB011/ SSL02-A/ SDA00-C	ET0_TXD0-A/ RMII0_TXD0-A/ RGMII0_TXD0-A/ CAT0_ETXD0-A	SD0_DAT3-A	IRQ12		PCOUTB0
A5		PC03	PIO_027	D4-A		GTOVLO/ GTIOC8B	TXD011-A/ SMOSI011-A/ SSDA011/ TXDA011/ SDAHS1-C	ET0_TXD2-A/ RGMII0_TXD2-A/ CAT0_ETXD2-A	SD0_CLK-A	IRQ11		PCOUTA1
A6		PC04	PIO_028	D3-A	TMCI1	GTOWUP/ GTIOC9A	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008/ CTS011#/ SSL00-A/ AUDIO_CLK	ET0_TXD3-A/ RGMII0_TXD3-A/ CAT0_ETXD3-A	SD0_DAT0-A	IRQ12		PCOUTB1
A7	ETHPHYCLK	PC07	PIO_031	D0-A	TMO2/ TOC0/ CACREF	GTETRGD/ GTADSM1/ GTIOC15B/ POEGA	TXD008-A/ SMOSI008-A/ SSDA008/ TXDA008/ MISO0-A/ SSITXD0	ET0_GTX_CLK-A/ RGMII0_TXC-A/ CATRESTOUT	SD0_CD	IRQ14		DSM1_DAT2-C/ PDMDAT0
A8	CLKOUT	P801	PIO_057	EBCLK-A		GTIV/ GTIOC0B/ POEGC	TXD010-B/ SMOSI010-B/ SSDA010/ TXDA010	ET0_CRS/ CATSYNC0		IRQ9	ADCNV1	DSM1_DAT1-C
A9		P800	PIO_056	CS1#-A/ DQM0-B		GTIU/ GTIOC0A/ POEGD	RXD010-B/ SMISO010-B/ SSCL010	ET0_COL/ CATLATCH0		IRQ8	ADCNV0	DSM1_CLK1-C
A10	VLO											
A11	VSS_DCDC											
A12	VSS_DCDC											
A13	VCC_DCDC											
A14		P504	PIO_036		TMCI1	GTETRGA/ GTIOC4A	CTS002#/ RXD007-B/ SMISO007-B/ SSCL007/ MOSI2-B	ET0_TX_ER-C/ GPTP_CAPTURE0/ CATLINKACT0		IRQ4		DSM0_CLK0-E
A15		P103	PIO_011		TMO3	GTADSM1/ GTIOC13B	CTS002#/ SDA00-A	ET0_CRS/ CATI2CDATA-A		IRQ3		

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (2/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
A16		P104	PIO_012		TMRI2	GTIW/ GTIOC14A	RXD002-B/ SMISO002-B/ SSCL002/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ CTX2/ USB0_OVRCURA-DS/ USBHS_VBUS	ET0_TXD0-B/ RMII0_TXD0-B/ CAT0_ETXD0-B/ CATLEDSTER	PIXD0	IRQ4	ADST0	DSM0_CLK1-C/ PCINA0
A17	CLKOUT	P106	PIO_014		TMO2/ RTCOUT	GTIU/ GTIOC15A/ POEGB	RXD003-B/ SMISO003-B/ SSCL003/ SCLHS2-A	ET0_TXD2-B/ CAT0_ETXD2-B/ CATI2CCLK-B	SD0_DAT2-C/PIXD2	IRQ30-DS	ADTRG0#	PCINA1
A18		P200	PIO_016		TMRI0	GTETRGA/ GTIOC3A/ GTIOC14A	CTS006#/ RTS006#/ SS006#/ DE006/ TXDB006/ MOSI0-C/ SDAHS1-A/ USB0_ID/ SSIRXD0	ET0_TX_EN-B/ RMII0_TX_EN-B/ CAT0_TX_EN-B	SD0_CMD-C/PIXD4	IRQ8	ADTRG2#	PCINZ1
A19	TMS/ SWDIO	P300	PIO_024		TMO1	GTCPPO10	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000/ CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001/ SSL10-C	ET0_WOL		IRQ6		
A20	VSS											
B1		PG03	PIO_059	DQM2-A/ WR2#-C/ BC2#-C		GTIOC11B	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008	ET0_INT/ GPTP_MATCH1		IRQ11		DSM0_DAT1-D
B2		P512	PIO_004	D19-A		GTIOC8A	SSL21-D	ET0_TXD4-A	SD0_DAT0-D	IRQ20		DSM0_CLK1-G/ PCINZ0
B3		P513	PIO_005	D18-A		GTIOC8B	SSL22-D	ET0_TXD5-A	SD0_DAT1-D	IRQ21		DSM0_DAT1-G/ PCINZ1
B4		PC00	PIO_024	D7-A		GTOUUP/ GTIOC7A	CTS011#/ RTS011#/ SS011#/ DE011/ TXDB011/ SSL01-A/ SCL00-C	ET0_TX_CLK-A/ CAT0_TX_CLK-A	SD0_DAT2-A	IRQ14		PCOUTA0
B5		PC02	PIO_026	D5-A		GTOVUP/ GTIOC8A	RXD011-A/ SMISO011-A/ SSCL011/ SSL03-A/ SCLHS1-C	ET0_TXD1-A/ RMII0_TXD1-A/ RGMII0_TXD1-A/ CAT0_ETXD1-A	SD0_CMD-A	IRQ10		PCOUTZ0
B6	VSS											

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (3/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
B7		PC05	PIO_029	D2-A	TMRI2	GTOWLO/ GTIOC9B	SCK008-A/ CTS008#/ TXDB008/ RSPCK0-A/ SSIBCK0	ET0_TX_EN -A/ RMII0_TX_ EN-A/ RGMII0_TX _CTL-A/ CAT0_TX_E N-A	SD0_DAT1-A	IRQ5		PCOUTZ1
B8		PC06	PIO_030	D1-A	TMCI2/ TIC0	GTETRGC/ GTCPPO7/ GTIOC15A/ POEGB	RXD008-A/ SMISO008-A/ SSCL008/ MOSI0-A/ SSILRCK0	ET0_TX_ER -A/ CATLINKAC T0	SD0_WP	IRQ13		DSM1_CL K2-C/ PDMCLK0
B9		P802	PIO_058	CS2#-A/ WR#-B/ WR0#-B		GTIW/ GTIOC1A/ POEGB	SCK010-B/ CTS010#/ TXDB010/ CRX2/ USB0_EXICE N	ET0_MDIO-B/ CAT0_MDIO -B		IRQ2	ADCNV2	DSM1_CL K0-C
B10	VLO											
B11	VSS_DCD C											
B12	VSS_DCD C											
B13	VCC_DCD C											
B14		P505	PIO_037		TMO3	GTETRGB/ GTIOC4B	TXD007-B/ SMOSI007-B/ SSDA007/ TXDA007/ MISO2-B	ET0_TX_CL K-C/ GPTP_MAT CH0/ CAT0_TX_C LK-C		IRQ10		DSM0_DA T0-E
B15		P102	PIO_010		TMCI1	GTADSM0/ GTIOC13A	SCL00-A	ET0_COL/ CATI2CCLK -A		IRQ2		
B16	VSS											
B17		P107	PIO_015		TMO1	GTIV/ GTIOC15B/ POEGA	TXD003-B/ SMOSI003-B/ SSDA003/ TXDA003/ SDAHS2-A/ SSITXD0	ET0_TXD3-B/ CAT0_ETX D3-B/ CATI2CDAT A-B	SD0_DAT3-C/PIXD3	IRQ31-DS	ADTRG1 #	PCINB1
B18		P201	PIO_017		TMCI0	GTIW/ GTIOC3B/ GTIOC14B	SCK006-A/ CTS006#/ TXDB006/ MISO0-C/ SCLHS1-A/ USB0_EXICE N/SSILRCK0	ET0_RX_E R-B/ RMII0_RX_ ER-B/ CAT0_RX_E R-B	SD0_CLK-C/PIXD5	IRQ9		PCINZ0
B19	TCK/ SWCLK	P301	PIO_025		TMCI3	GTCPPO1 1	SCK000-A/ CTS000#/ TXDB000/ SCK001-A/ CTS001#/ TXDB001/ RSPCK1-C	ET1_WOL		IRQ7		
B20	TDO	P302	PIO_026		TMRI3	GTCPPO1 2	TXD000-A/ SMOSI000-A/ SSDA000/ TXDA000/ TXD001-A/ SMOSI001-A/ SSDA001/ TXDA001/ MOSI1-C	ET1_COL		IRQ4		

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (4/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
C1		PG02	PIO_058	DQM3-A/ WR3#-C/ BC3#-C		GTIOC11A	TXD008-C/ SMOSI008-C/ SSDA008/ TXDA008	ET1_RX_ER-A/ RMII1_RX_ER-A/ CAT1_RX_ER-A		IRQ10		DSM0_CLK1-D
C2		PG01	PIO_057	DQM0-A/ WR#-C/ WR0#-C		GTCPPO1	RXD008-C/ SMISO008-C/ SSCL008	ET1_RX_DV-A/ RMII1_CRS_DV-A/ RGMII1_RX_CTL-A/ CAT1_RX_DV-A		IRQ9		DSM0_DAT2-D
C3		PB01	PIO_017	D14-A	TMCI0	GTETRGB/ GTCPPO4/ GTIOC14B/ POEGA	TXD004-A/ SMOSI004-A/ SSDA004/ TXDA004	ET0_RXD1-A/ RMII0_RXD1-A/ RGMII0_RXD1-A/ CAT0_ERXD1-A		IRQ4-DS		DSM0_DAT2-A/ PCINB1
C4		PB03	PIO_019	D12-A	TMO0	GTOULO/ GTIOC4B	SCK004-A/ CTS004#/ TXDB004	ET0_RXD3-A/ RGMII0_RXD3-A/ CAT0_ERXD3-A		IRQ3		
C5		PB04	PIO_020	D11-A		GTOVUP/ GTIOC5A	CTS004#/ CTS009#/ RTS009#/ SS009#/ DE009/ TXDB009	ET0_RX_CLK-A/ RMII0_REF50CK-A/ RGMII0_RXC-A/ CAT0_RX_CLK-A		IRQ4		
C6		PB06	PIO_022	D9-A		GTOWUP/ GTIOC6A	RXD009-A/ SMISO009-A/ SSCL009	ET0_RX_ER-A/ RMII0_RX_ER-A/ CAT0_RX_ER-A		IRQ6		
C7		PB07	PIO_023	D8-A		GTOWLO/ GTIOC6B	TXD009-A/ SMOSI009-A/ SSDA009/ TXDA009	ET0_LINKSTA/ CAT0_LINKSTA		IRQ15		
C8		PB05	PIO_021	D10-A	TMRI1	GTOVLO/ GTIOC5B	SCK009-A/ CTS009#/ TXDB009	ET0_RX_DV-A/ RMII0_CRS_DV-A/ RGMII0_RX_CTL-A/ CAT0_RX_DV-A		IRQ13		
C9		P803	PIO_059	CS3#-A/ WR1#-B/ BC1#-B		GTIOC1B/ POEGA	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ CTX2/ USB0_ID	ET0_MDC-B/ CAT0_MDC-B		IRQ3	ADSYNC	DSM1_DAT0-C
C10	VLO											
C11	VLO											
C12	VCC_DCDC											
C13	VCC_DCDC											

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (5/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
C14		P506	PIO_038			GTETRGC/ GTIOC5A/ POEGD	SCK007-B/ CTS007#/ TXDB007/ RSPCK2-B	ET0_TXD2-C/ GPTP0_PPS/ CAT0_ETXD2-C		IRQ6		
C15		P105	PIO_013		TMCI2	GTIV/ GTIOC14B	TXD002-B/ SMOSI002-B/ SSDA002/ TXDA002/ SCK003-B/ CTS003#/ TXDB003/ CRX2/ USB0_VBUS/ USBHS_OVRCURB/ SSILRCK1	ET0_TXD1-B/ RMII0_TXD1-B/ CAT0_ETXD1-B/ CATLEDRUN	PIXD1	IRQ29-DS	ADST1	DSM0_DAT1-C/ PCINB0
C16		P805	PIO_061			GTADSM1/ GTIOC15B	SCK005-B/ CTS005#/ TXDB005/ SSL22-B/ CRX0/ USB0_VBUSEN/ USBHS_VBUSEN	ET0_TXD0-C/ RMII0_TXD0-C/ CAT0_ETXD0-C	HSYNC	IRQ5	ADSYNC	DSM0_DAT0-F/ PCINB0
C17		P806	PIO_062			GTCPPO7/ GTIOC14A	RXD005-B/ SMISO005-B/ SSCL005/ SSL23-B/ CTX1	ET0_TXD1-C/ RMII0_TXD1-C/ CAT0_ETXD1-C	VSYNC	IRQ14		DSM0_CLK1-F/ PCINA1
C18		P807	PIO_063			GTCPPO4/ GTIOC14B/ POEGD	TXD005-B/ SMOSI005-B/ SSDA005/ TXDA005/ CRX1	ET0_RX_ER-C/ RMII0_RX_ER-C/ CAT0_RX_ER-C	PIXCLK	IRQ15		DSM0_DAT1-F/ PCINB1
C19	ETHPHYCLK	P304	PIO_028	ALE-C/ WAIT#-B	TMCI3	GTETRGD/ GTCPPO0/ POEGA	CTS000#/ CTS001#/ USB0_VBUSEN/ USBHS_ID	ET0_INT/ CATRESTOUT		IRQ0-DS	ADTRG0#	
C20	TDI	P303	PIO_027		TMCI2	GTCPPO13	RXD000-A/ SMISO000-A/ SSCL000/ RXD001-A/ SMISO001-A/ SSCL001/ MISO1-C	ET1_CRS		IRQ1		
D1		PA06	PIO_014	A1-A/ DQM2-B	TMCI3	GTIOC3A/ GTIOC13A	TXD010-A/ SMOSI010-A/ SSDA010/ TXDA010/ MOSI0-B	ET1_TXD3-A/ RGMII1_TXD3-A/ CAT1_ETXD3-A		IRQ14		PCINZ1
D2		PG00	PIO_056	DQM1-A/ WR1#-C/ BC1#-C		GTCPPO0	SCK008-C/ CTS008#/ TXDB008	ET1_RX_CLK-A/ RMII1_REF50CK-A/ RGMII1_RXC-A/ CAT1_RX_CLK-A		IRQ8		DSM0_CLK2-D
D3		P511	PIO_003	D20-A		GTETRGA/ GTIOC7B/ POEGC	SSL20-D	ET0_RXD7-A	SD0_CLK-D	IRQ19		DSM0_DAT2-G

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (6/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
D18		P108	PIO_040		TIC0	GTCPPO8	SCK009-C/ CTS009#/ TXDB009/ RSPCK2-C	ET0_RX_DV-C/ RMII0_CRS_DV-C/ CAT0_RX_DV-C	SD0_DAT4-C/PIXD0	IRQ16	ADCNV0	DSM0_CLK2-F
D19		P109	PIO_041		TOC0	GTCPPO9	RXD009-C/ SMISO009-C/ SSCL009/ MOSI2-C	ET0_RX_CLK-C/ RMII0_REF50CK-C/ CAT0_RX_CLK-C	SD0_DAT5-C/PIXD1	IRQ17	ADCNV1	DSM0_DAT2-F
D20		P110	PIO_042			GTCPPO10	TXD009-C/ SMOSI009-C/ SSDA009/ TXDA009/ MISO2-C	ET0_RXD0-C/ RMII0_RXD0-C/ CAT0_ERXD0-C	SD0_DAT6-C/PIXD2	IRQ18	ADCNV2	
E1		PA05	PIO_013	A2-A		GTIOC2B/ GTIOC12B	SCK010-A/ CTS010#/ TXDB010/ RSPCK0-B	ET1_TXD2-A/ RGMII1_TXD2-A/ CAT1_ETXD2-A		IRQ5		PCINA0
E2	ETHPHYCLK	PA07	PIO_015	A0-A/ BC0#-A/ DQM1-B		GTIOC3B/ GTIOC13B	RXD010-A/ SMISO010-A/ SSCL010/ MISO0-B	ET1_TX_ER-A/ CATLINKACT1		IRQ7		PCINB0
E3	CLKOUT	P510	PIO_002	D21-A		GTETRGB/ GTIOC7A/ POEGB	MISO2-D	ET0_RXD6-A	SD0_CMD-D	IRQ18		DSM0_CLK2-G/ PCOUTZ0
E5		PG05	PIO_061	A10-A		GTIOC12B	RXD003-C/ SMISO003-C/ SSCL003	ET0_MDIO-A/ CAT0_MDIO-A		IRQ13		
E6		PB02	PIO_018	D13-A		GTOUUP/ GTIOC4A	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004/ CTS009#	ET0_RXD2-A/ RGMII0_RXD2-A/ CAT0_ERXD2-A		IRQ2		
E7		PB00	PIO_016	D15-A		GTETRGA/ GTADSM0/ GTIOC14A/ POEGC	RXD004-A/ SMISO004-A/ SSCL004	ET0_RXD0-A/ RMII0_RXD0-A/ RGMII0_RXD0-A/ CAT0_ERXD0-A		IRQ12	ADST2	DSM0_CLK2-A/ PCINA1
E8	VCC											
E9	VCC											
E10		P500	PIO_032	WR#-A/ WR0#-A/ A16-C		GTIOC2A	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS007#/ SSL11-C/ CTX0	ET0_LINKSTA/ CAT0_LINKSTA	SD0_DAT4-A	IRQ0	ADST0	DSM0_CLK2-E
E11		P502	PIO_034	WR2#-A/ BC2#-A/ A18-C		GTIOC3A	TXD002-C/ SMOSI002-C/ SSDA002/ TXDA002/ SSL13-C/ CTX1	ET0_WOL/ CATLEDRUN	SD0_DAT6-A	IRQ2	ADST2	DSM0_CLK1-E

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (7/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
E12		P100	PIO_008	CS1#-B/ WAIT#-A	TMRI3/ CACREF	GTIU/ GTADSM0/ GTIOC12A	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS005#/ USB0_OVRCURB-DS/ USBHS_VBUS	ET0_TX_ER-B/ CATLINKACT0/ CATLEDER R		IRQ0	ADTRG2#	DSM0_CLK0-C
E13	VCC											
E14	VCC											
E15		P507	PIO_039			GTETRGD/ GTIOC5B/ POEGC	CTS007#/ RTS007#/ SS007#/ DE007/ TXDB007/ SSL20-B	ET0_TXD3-C/ GPTP1_PPS/ CAT0_ETXD3-C		IRQ7		
E16		P804	PIO_060			GTADSM0/ GTIOC15A	CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ SSL21-B/ CTX0/ USB0_OVRCURA/ USBHS_OVRCURA	ET0_TX_EN-C/ RMII0_TX_EN-C/ CAT0_TX_EN-C	PCKO	IRQ4		DSM0_CLK0-F/ PCINA0
E18		P111	PIO_043			GTCPPO11	CTS012#/ CTS009#/ RTS009#/ SS009#/ DE009/ TXDB009/ SSL20-C	ET0_RXD1-C/ RMII0_RXD1-C/ CAT0_ERXD1-C	SD0_DAT7-C/PIXD3	IRQ19		
E19		P112	PIO_044			GTCPPO12	CTS012#/ RTS012#/ SS012#/ DE012/ TXDB012/ CTS009#/ SSL21-C	ET0_RXD2-C/ CAT0_ERXD2-C	PIXD4	IRQ20	ADST0	DSM0_CLK1-H/ PDMCLK0
E20		P113	PIO_045			GTCPPO13	SCK012-B/ CTS012#/ TXDB012/ SSL22-C	ET0_RXD3-C/ CAT0_ERXD3-C	PIXD5	IRQ21	ADST1	DSM0_DAT1-H/ PDMDAT0
F1		PA03	PIO_011	A4-A		GTIOC1B/ GTIOC11B	RXD005-A/ SMISO005-A/ SSCL005	ET1_TXD0-A/ RMII1_TXD0-A/ RGMII1_TXD0-A/ CAT1_ETXD0-A		IRQ6-DS	ADSYNC	DSM0_DAT1-A
F2		PA04	PIO_012	A3-A	TMRI0	GTIOC2A/ GTIOC12A	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ SSL00-B	ET1_TXD1-A/ RMII1_TXD1-A/ RGMII1_TXD1-A/ CAT1_ETXD1-A		IRQ5-DS		PCINZ0
F3		P509	PIO_001	D22-A	TOC2	GTIOC6B	MOSI2-D	ET0_RXD5-A	SD0_DAT3-D	IRQ17		PCOUTB0

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (8/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
F5		PG07	PIO_063	A8-A		GTIOC13B	CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003	ET0_CRS		IRQ15		
F6		PG06	PIO_062	A9-A		GTIOC13A	TXD003-C/ SMOSI003-C/ SSDA003/ TXDA003	ET0_COL		IRQ14		
F7		PG04	PIO_060	A11-A		GTIOC12A	SCK003-C/ CTS003#/ TXDB003	ET0_MDC-A/ CAT0_MDC-A		IRQ12		
F8	VSS											
F9	VSS											
F10		P501	PIO_033	WR1#-A/ BC1#-A/ A17-C		GTIOC2B	SCK002-C/ CTS002#/ TXDB002/ SSL12-C/ CRX0	ET0_INT/ CATLEDSTER	SD0_DAT5-A	IRQ1	ADST1	DSM0_DAT2-E
F11		P503	PIO_035	WR3#-A/ BC3#-A/ A19-C		GTIOC3B	RXD002-C/ SMISO002-C/ SSCL002/ CRX1/ USB0_OVRCURB/ SSIRXD0	ET1_WOL/ CATLEDER R	SD0_DAT7-A	IRQ3		DSM0_DAT1-E
F12		P101	PIO_009	CS0#-A/ ALE-B	TMCI3	GTETRGC/ GTADSM1/ GTIOC12B	SCK002-B/ CTS002#/ TXDB002/ USB0_VBUS-DS/ USBHS_EXICEN	ET0_TX_CLK-B/ CAT0_TX_CLK-B/ CAT0_LINKSTA		IRQ1	ADTRG1#	DSM0_DAT0-C
F13	VSS											
F14	VSS											
F15		PF02	PIO_050	CS6#-B/ BREQ#-C		GTCPPO1/ GTIOC7A	RXD000-C/ SMISO000-C/ SSCL000/ RXD007-C/ SMISO007-C/ SSCL007	ET1_TXD2-C/ CAT1_ETXD2-C		IRQ2	ADSYNC	DSM1_CLK0-F
F16		P115	PIO_047			GTCPPO15	RXD012-B/ SMISO012-B/ SSCL012	ET1_TX_CLK-C/ CAT1_TX_CLK-C	PIXD7	IRQ23		DSM0_DAT0-H
F18		P114	PIO_046			GTCPPO14	TXD012-B/ SMOSI012-B/ SSDA012/ TXDA012/ SSL23-C	ET1_TX_ER-C/ CATLINKACT1	PIXD6	IRQ22	ADST2	DSM0_CLK0-H
F19	VSS											
F20	VCC											
G1		PA02	PIO_010	A5-A		GTIW/ GTIOC1A/ GTIOC11A	TXD005-A/ SMOSI005-A/ SSDA005/ TXDA005/ SSL03-B	ET1_TX_CLK-A/ CAT1_TX_CLK-A		IRQ10	ADCNV2	DSM0_CLK1-A

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (9/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
G2		PA01	PIO_009	A6-A		GTIV/ GTIOC0B/ GTIOC10B	SCK005-A/ CTS005#/ TXDB005/ SSL02-B	ET1_TX_EN-A/ RMII1_TX_EN-A/ RGMII1_TX_CTL-A/ CAT1_TX_EN-A		IRQ11	ADCNV1	DSM0_DAT0-A
G3		P508	PIO_000	D23-A	TIC2	GTIOC6A	RSPCK2-D	ET0_RXD4-A	SD0_DAT2-D	IRQ16		PCOUTA0
G5	VCC											
G6	VSS											
G15		PF03	PIO_051	CS7#-B/ BACK#-C		GTCPPO2/ GTIOC7B	TXD000-C/ SMOSI000-C/ SSDA000/ TXDA000/ TXD007-C/ SMOSI007-C/ SSDA007/ TXDA007	ET1_TXD3-C/ CAT1_ETXD3-C		IRQ3		DSM1_DAT0-F
G16		PF04	PIO_052	CS4#-B		GTCPPO3/ GTIOC8A	SCK000-C/ CTS000#/ TXDB000/ SCK007-C/ CTS007#/ TXDB007	ET1_TXD0-C/ RMII1_TXD0-C/ CAT1_ETXD0-C		IRQ4		DSM1_CLK1-F
G18	VSS_USB											
G19		PF00	PIO_048			GTCPPO14	USB0_DP			IRQ0		
G20		PF01	PIO_049			GTCPPO15	USB0_DM			IRQ1		
H1	ETHPHYCLK	PA00	PIO_008	A7-A	CACREF	GTIU/ GTIOC0A/ GTIOC10A	CTS010#/ CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ SSL01-B	ET1_GTX_CLK-A/ RGMII1_TXC-A/ CATIRQ		IRQ1-DS	ADCNV0	DSM0_CLK0-A
H2		PG13	PIO_029	D26-A		GTCPPO13	CTS003#	ET1_MDC-A/ GPTP_PTPOUT1	SD0_DAT5-D/ XSPI1_RESET1#/PIXD5	IRQ29		DSM1_DAT1-H/ PCOUTB0
H3		PG15	PIO_031	D24-A		GTCPPO15	CTS011#	ET1_CRS/ GPTP_PTPOUT3	SD0_DAT7-D/ XSPI1_RSTO1#/PIXD7	IRQ31		DSM1_DAT2-H
H5	VCC											
H6	VSS											
H8	VSS											
H9	VCL											
H10	VSS											
H11	VSS											
H12	VCL											
H13	VSS											

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (10/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
H15	ETHPHYCLK	P204	PIO_020	A20-C/ CS7#-C	TMRI1	GTOVUP/ GTIOC1A/ GTIOC5A	CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001/ SSL10-B/ SCLHS1-B/ CTX0/ USB0_VBUSEN/ USBHS_VBUS-DS/ SSIBCK1	ET0_RXD0-B/ RMII0_RXD0-B/ CAT0_ERXD0-B	SD0_WP/ PIXCLK	IRQ12		DSM1_CLK1-B/ PCOUTA1
H16		P203	PIO_019	CS2#-B/ BACK#-A		GTOULO/ GTIOC0B/ GTIOC4B	RXD006-A/ SMISO006-A/ SSCL006/ CTS003#/ SSL00-C/ SDA00-B/ CRX2/ USB0_OVRCURB/ USBHS_ID/ SSIBCK0	ET0_RX_CLK-B/ RMII0_REF50CK-B/ CAT0_RX_CLK-B/ CATI2CDATA-C	SD0_DAT1-C/PIXD7	IRQ3		DSM1_DAT0-B/ PDMDAT0
H18		PF05	PIO_053	CS5#-B		GTCPPO5/ GTIOC8B/ POEGD	CTS007#/ RTS007#/ SS007#/ DE007/ TXDB007/ SSL01-C	ET1_TXD1-C/ RMII1_TXD1-C/ CAT1_ETXD1-C		IRQ5		DSM1_DAT1-F
H19	VCC_USB											
H20	VCC_USB											
J1		PG11	PIO_027	D28-A		GTCPPO13	CTS012#/ RTS012#/ SS012#/ DE012/ TXDB012	ET1_TXD7-A/ ET_TAS_STA3	PIXD3	IRQ27		DSM1_DAT0-H/ PCOUTZ1
J2		PG14	PIO_030	D25-A		GTCPPO14		ET1_MDIO-A/ GPTP_PTPOUT2	SD0_DAT6-D/ XSPI1_WP1#/PIXD6	IRQ30		DSM1_CLK2-H/ PCOUTZ0
J3		PG12	PIO_028	D27-A		GTCPPO12	CTS008#/ CTS005#	ET1_COL/ GPTP_PTPOUT0	SD0_DAT4-D/ XSPI1_INT1#/ XSPI1_ECS1#/PIXD4	IRQ28		DSM1_CLK1-H/ PCOUTA0
J5	VCC											
J6	VSS											
J8	VSS											
J9	VCL											
J10	VSS											
J11	VSS											
J12	VSS											
J13	VCL											
J15	CLKOUT	P205	PIO_021	A21-C/ CS6#-C		GTOVLO/ GTIOC1B/ GTIOC5B	SCK001-B/ CTS001#/ TXDB001/ RSPCK1-B/ SDAHS1-B/ CRX0/ USB0_VBUS/ USBHS_VBUSEN/ SSIRXD1	ET0_RXD1-B/ RMII0_RXD1-B/ CAT0_ERXD1-B	SD0_CD/ HSYNC	IRQ5	ADTRG0#	DSM1_DAT1-B/ PCOUTB1

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (11/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
J16		P202	PIO_018	CS3#-B/ BREQ#-A	TMO0	GTOUUP/ GTIOC0A/ GTIOC4A	TXD006-A/ SMOSI006-A/ SSDA006/ TXDA006/ RSPCK0-C/ SCL00-B/ CTX2/ USB0_OVRCURA/ USBHS_EXICEN/ AUDIO_CLK	ET0_RX_DV-B/ RMII0_CRS_DV-B/ CAT0_RX_DV-B/ CATI2CCLK-C	SD0_DAT0-C/PIXD6	IRQ15		DSM1_CLK0-B/ PDMCLK0
J18	AVSS_USBHS											
J19							USBHS_DP					
J20							USBHS_DM					
K1		PG09	PIO_025	D30-A	TOC3	GTCPPO11	RXD012-C/ SMISO012-C/ SSCL012	ET1_TXD5-A/ ET_TAS_STA1	PIXD1	IRQ25		DSM0_DAT2-H/ PCOUTA1
K2		PG10	PIO_026	D29-A		GTCPPO12	TXD012-C/ SMOSI012-C/ SSDA012/ TXDA012	ET1_TXD6-A/ ET_TAS_STA2	PIXD2	IRQ26		DSM1_CLK0-H/ PCOUTB1
K3		P705	PIO_053	RAS#-A/ CS5#-A		GTIOC12B	SCK011-B/ CTS011#/ TXDB011	ET1_RXD1-A/ RMII1_RXD1-A/ RGMII1_RXD1-A/ CAT1_ERXD1-A	XSPI1_RSTO1#	IRQ13	ADCNV1	DSM1_DAT2-D
K5		P704	PIO_052	SDCS#-A/ CS4#-A		GTIOC12A	CTS004#/ CTS011#/ RTS011#/ SS011#/ DE011/ TXDB011	ET1_RXD0-A/ RMII1_RXD0-A/ RGMII1_RXD0-A/ CAT1_ERXD0-A	XSPI1_INT1#/ XSPI1_ECS1#	IRQ12	ADCNV0	DSM1_CLK2-D
K6		P702	PIO_050	RD#-A/ DQM3-B		GTETRGA/ GTIOC11A	SCK004-B/ CTS004#/ TXDB004	ET1_CRS/ CATSYNC1	XSPI1_WP0#/ XSPI1_RESET1#/ HSYNC	IRQ10	ADST2	DSM1_CLK1-D
K8	VCL											
K9	VSS											
K10	VCL											
K11	VCL											
K12	VCC											
K13	VSS											
K15		P207	PIO_023	A23-C/ CS4#-C	TMRI3	GTOWLO/ GTIOC2B/ GTIOC6B	RXD001-B/ SMISO001-B/ SSCL001/ MISO1-B/ SDAHS2-B/ CRX1/ USB0_ID/ USBHS_OVRCURB-DS	ET0_RXD3-B/ CAT0_ERXD3-B	PCKO	IRQ3-DS	ADTRG2#	DSM1_DAT2-B

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (12/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
K16		P206	PIO_022	A22-C/ CS5#-C	TMO3/ RTCOUT	GTOWUP/ GTIOC2A/ GTIOC6A	CTS006#/ TXD001-B/ SMOSI001-B/ SSDA001/ TXDA001/ MOSI1-B/ SCLHS2-B/ CTX1/ USB0_EXICEN/ USBHS_OVRCURA-DS/ SSITXD1	ET0_RXD2-B/ CAT0_ERXD2-B	VSYNC	IRQ2-DS	ADTRG1#	DSM1_CLK2-B/ PCOUTZ1
K18	USBHS_REF											
K19	VSS_USBHS											
K20	VCC_USBHS											
L1		PG08	PIO_024	D31-A	TIC3	GTCPPO10	SCK012-C/ CTS012#/ TXDB012	ET1_TXD4-A/ ET_TAS_STA0	PIXD0	IRQ24		DSM0_CLK2-H
L2	VSS											
L3		P707	PIO_055	WE#-A/ CS7#-A		GTIOC13B	TXD011-B/ SMOSI011-B/ SSDA011/ TXDA011	ET1_RXD3-A/ RGMII1_RXD3-A/ CAT1_ERXD3-A	XSPI1_RESET1#	IRQ7		DSM0_DAT0-D
L5		P706	PIO_054	CAS#-A/ CS6#-A		GTIOC13A	RXD011-B/ SMISO011-B/ SSCL011	ET1_RXD2-A/ RGMII1_RXD2-A/ CAT1_ERXD2-A	XSPI1_WP1#	IRQ14	ADCNV2	DSM0_CLK0-D
L6		P703	PIO_051	ALE-A/ WR2#-B/ BC2#-B	CACREF	GTETRGB/ GTIOC11B	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004	ET1_LINKSTA/ CAT1_LINKSTA	XSPI1_RESET0#/PCKO	IRQ8		DSM1_DAT1-D
L8	VSS											
L9	VSS											
L10	VCL											
L11	VCL											
L12	VSS											
L13	VCC											
L15		P310	PIO_058		RTCIC0/ CACREF	GTETRGB/ GTCPPO1/ POEGC	CTS000#/ CTS001#/ SSL11-B/ SSITXD0	ET1_INT/ CATIRQ		IRQ18	ADTRG0#	TAMPI0
L16		P305								NMI/IRQ0		
L18	AVCC_USBHS											
L19	VCC											
L20	VCC											
M1		P701	PIO_049	CKE-A/ WR3#-B/ BC3#-B		GTIOC10B	RXD004-B/ SMISO004-B/ SSCL004	ET1_COL/ CATLATCH1	XSPI1_RSTO0#/ XSPI1_RESET0#/ VSYNC	IRQ1	ADST1	DSM1_DAT0-D

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (13/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
M2		P715	PIO_023	A12-A		GTCPPO9/ GTIOC15B	RXD010-C/ SMISO010-C/ SSCL010	ET1_RXD7-A	HSYNC	IRQ23		
M3		P714	PIO_022	A13-A		GTCPPO8/ GTIOC15A	TXD010-C/ SMOSI010-C/ SSDA010/ TXDA010	ET1_RXD6-A	VSYNC	IRQ22		
M5	VCC											
M6	VSS											
M8	VCL											
M9	VCL											
M10	VSS											
M11	VSS											
M12	VSS											
M13	VCL											
M15		P312	PIO_060	BACK#-B	RTCIC2	GTETRGD/ GTCPPO1 5/POEGA	SSL13-B/ SSILRCK0	ET1_WOL		IRQ20	ADTRG2 #	DSM0_DA T2-C/ TAMPI2
M16		P311	PIO_059	BREQ#-B	RTCIC1	GTETRGC/ GTCPPO1 4/POEGD	CTS007#/ SSL12-B/ SSIRXD0	ET0_WOL		IRQ19	ADTRG1 #	DSM0_CL K2-C/ TAMPI1
M18	VSS											
M19	EXTAL	P306										
M20	XTAL	P307										
N1	ETHPHYC LK	P700	PIO_048	SDCLK-A		GTIOC10A	TXD004-B/ SMOSI004-B/ SSDA004/ TXDA004	ET1_INT/ CATRESTO UT	XSPI1_INT0 #/ XSPI1_ECS 0#/PIXCLK	IRQ0	ADST0	DSM1_CL K0-D
N2		P712	PIO_020	A15-A		GTCPPO5/ GTIOC14A	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ CTS011#	ET1_RXD4-A	PCKO	IRQ20		DSM1_CL K0-G
N3		P713	PIO_021	A14-A		GTCPPO6/ GTIOC14B	SCK010-C/ CTS010#/ TXDB010	ET1_RXD5-A	PIXCLK	IRQ21		DSM1_DA T0-G
N5	VCC											
N6	VSS											
N8	VSS											
N9	VCL											
N10	VSS											
N11	VSS											
N12	VCL											
N13	VSS											
N15		P209	PIO_049		TOC1	GTETRGB	RXD004-C/ SMISO004-C/ SSCL004/ MOSI1-D	ET1_RX_CL K-C/ RMII1_REF 50CK-C/ CAT1_RX_ CLK-C		IRQ25		PCINB1
N16		P208	PIO_048		TIC1	GTETRGA	SCK004-C/ CTS004#/ TXDB004/ RSPCK1-D	ET1_TX_EN -C/ RMII1_TX_ EN-C/ CAT1_TX_E N-C		IRQ24		PCINA1

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (14/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
N18	MD/FINED	P315										
N19	VSS											
N20	VSS											
P1		PE06	PIO_046	A9-B/A21-D	TIC1	GTETRGC/ GTADSM1/ GTIOC10A/ POEGB	SSL13-A	ET1_RX_CLK-D/ RMII1_REF50CK-D/ CAT1_RX_CLK-D/ CATLEDER R	XSPI1_DS/ PIXD6	IRQ6		
P2		PE07	PIO_047	A8-B/A20-D	TOC1	GTETRGD/ GTCPPO7/ GTIOC10B/ POEGD		ET1_LINKSTA/ CAT1_LINKSTA/ CATRESTOUT	XSPI1_CS0#/PIXD7	IRQ7		
P3		PF09	PIO_017	A20-A/ A16-D			CTS012#	GPTP_CAPTURE1	XSPI1_INT0#/ XSPI1_ECS0#	IRQ17		
P5	VCC											
P6	VSS											
P15		P211	PIO_051			GTETRGD	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004/ CTS005#/ SSL10-D/ USBHS_OVRCURB	ET1_RXD1-C/ RMII1_RXD1-C/ CAT1_ERXD1-C		IRQ27		
P16		P210	PIO_050			GTETRGC	TXD004-C/ SMOSI004-C/ SSDA004/ TXDA004/ MISO1-D	ET1_RXD0-C/ RMII1_RXD0-C/ CAT1_ERXD0-C		IRQ26		PCINZ1
P18	VSS											
P19	XCIN/ EXCIN	P309										
P20	XCOUT	P308										
R1		PE03	PIO_043	A12-B	TOC3	GTOVLO/ GTIOC8B	CTS012#/ RTS012#/ SS012#/ DE012/ TXDB012/ MISO1-A	ET1_RXD1-D/ RMII1_RXD1-D/ CAT1_ERXD1-D	SD0_DAT7-B/ XSPI1_IO1/ PIXD3	IRQ11		
R2		PE05	PIO_045	A10-B/ A22-D		GTOWLO/ GTIOC9B	SSL12-A	ET1_RXD3-D/ CAT1_ERXD3-D/ CATLEDRUN	XSPI1_IO3/ PIXD5	IRQ5		
R3		PF08	PIO_016	A21-A/ A17-D		GTCPPO12/POEGA			XSPI1_RESET0#	IRQ16		
R5		P607	PIO_015	CS0#-B/ D16-B		GTETRGB/ GTADSM0/ GTIOC15B/ POEGA	CTS008#/ CTS009#/ RTS009#/ SS009#/ DE009/ TXDB009/ CRX2	ET1_INT/ ET_TAS_ST A3/CATIRQ	XSPI0_RSTO0#	IRQ15		DSM1_DAT2-A

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (15/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
R6		P606	PIO_014	CS1#-C/ D17-B		GTETRGA/ GTCPPO4/ GTIOC15A/ POEGC	SCK009-B/ CTS009#/ TXDB009/ SSL03-D/ CTX2	ET1_TX_ER -B/ ET_TAS_ST A2/ CATLINKAC T1	XSPI0_RES ET0#	IRQ14		DSM1_CL K2-A
R7	VSS											
R8	VSS											
R9	VSS											
R10		P906	PIO_006			GTCPPO2/ POEGA	SCK006-B/ CTS006#/ TXDB006	ET0_MDC- C/ GPTP_PTP OUT2		IRQ14		
R11		P405	PIO_053							IRQ13-DS	AN005	
R12		P404	PIO_052							IRQ12-DS	AN004	
R13	VSS											
R14	VSS											
R15		P215	PIO_055			GTCPPO1 3	CTS004#/ CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ USBHS_ID	ET1_RXD3- C/ CAT1_ERX D3-C		IRQ31		PDMDAT0 /PCINZ0
R16		P214	PIO_054			GTCPPO1 2	TXD005-C/ SMOSI005-C/ SSDA005/ TXDA005/ SSL13-D/ USBHS_EXIC EN	ET1_RXD2- C/ CAT1_ERX D2-C		IRQ30	ADTRG2 #	PDMCLK0 /PCINB0
R18	RES#											
R19	VCC											
R20	VBATT/ VCC											
T1	CLKOUT	PE01	PIO_041	A14-B		GTOULO/ GTIOC7B	TXD012-A/ SMOSI012-A/ SSDA012/ TXDA012/ RSPCK1-A	ET1_RX_D V-D/ RMII1_CRS _DV-D/ CAT1_RX_ DV-D	SD0_DAT5- B/ XSPI1_CK/ PIXD1	IRQ9		
T2		PE04	PIO_044	A11-B/ A23-D		GTOWUP/ GTIOC9A	CTS012#/ SSL11-A	ET1_RXD2- D/ CAT1_ERX D2-D/ CATLEDST ER	XSPI1_IO2/ XSPI1_WP0 #/PIXD4	IRQ12		
T3		PF07	PIO_055	A22-A/ A18-D		GTCPPO1 1/GTIOC9B	SSL03-C		XSPI1_RST O0#	IRQ7		DSM1_DA T2-F
T5		P604	PIO_012	CS3#-C/ D19-B		GTIOC6A	TXD009-B/ SMOSI009-B/ SSDA009/ TXDA009/ SSL01-D	ET1_TXD2- B/ ET_TAS_ST A0/ CAT1_ETX D2-B	XSPI0_CS1 #/ XSPI0_RST O0#	IRQ4		DSM1_CL K1-A

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (16/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
T6		P602	PIO_010	CAS#-B/ D21-B		GTIOC5A	SCK008-B/ CTS008#/ TXDB008/ MOSI0-D	ET1_TXD0-B/ RMII1_TXD0-B/ GPTP_PTPOUT2/ CAT1_ETXD0-B/ CATLATCH0	XSPI0_IO6/ HSYNC	IRQ2	ADTRG2#	DSM1_CLK0-A
T7	VCC2											
T8	VCC2											
T9	VCC2											
T10		P907	PIO_007			GTCPPO3/ POEGD	CTS006#/ RTS006#/ SS006#/ DE006/ TXDB006/ CTS001#	ET0_MDIO-C/ GPTP_PTPOUT3	XSPI0_WP0#	IRQ15		
T11		P406	PIO_054							IRQ14-DS	AN006	
T12		P407	PIO_055							IRQ15-DS	AN007	
T13	VCC											
T14	VCC											
T15		P013	PIO_037			GTCPPO13		ET1_CRS/ GPTP_CAPTURE1/ CATLATCH0		IRQ29		DSM1_DAT1-E
T16		P012	PIO_036			GTCPPO12	CTS006#	ET1_COL/ GPTP0_PPS/ CATSYNC0		IRQ28		DSM1_CLK1-E
T18		P213	PIO_053			GTCPPO11	RXD005-C/ SMISO005-C/ SSCL005/ SSL12-D/ USBHS_VBUSEN	ET1_RX_ER-C/ RMII1_RX_ER-C/ CAT1_RX_ER-C		IRQ29	ADTRG1#	PCINA0
T19		P212	PIO_052			GTCPPO10	SCK005-C/ CTS005#/ TXDB005/ SSL11-D/ USBHS_OVRCURA	ET1_RX_DV-C/ RMII1_CRS_DV-C/ CAT1_RX_DV-C		IRQ28	ADTRG0#	
T20		P000	PIO_000		TMRI0	GTCPPO7/ GTIOC10A/ POEGB	CTS000#/ CTS007#/ RTS007#/ SS007#/ DE007/ TXDB007/ AUDIO_CLK	ET0_INT/ CATRESTOUT		IRQ16-DS	AN016	DSM0_CLK0-B
U1	ETHPHYCLK	PE00	PIO_040	A15-B		GTOUUP/ GTIOC7A	SCK012-A/ CTS012#/ TXDB012/ SSL10-A	ET1_RX_ER-D/ RMII1_RX_ER-D/ CAT1_RX_ER-D	SD0_DAT4-B/ XSPI1_CKN#/ XSPI1_CS1#/PIXD0	IRQ8		
U2		PE02	PIO_042	A13-B	TIC3	GTOVUP/ GTIOC8A	RXD012-A/ SMISO012-A/ SSCL012/ MOSI1-A	ET1_RXD0-D/ RMII1_RXD0-D/ CAT1_ERXD0-D	SD0_DAT6-B/ XSPI1_IO0/ PIXD2	IRQ7-DS		

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (17/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
U3		PF06	PIO_054	A23-A/ A19-D		GTCPPO6/ GTIOC9A/ POEGC	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000/ CTS007#/ SSL02-C		XSPI1_CS1 #/ XSPI1_WP0 #	IRQ6		DSM1_CL K2-F
U18		P008	PIO_032			GTCPPO8/ GTIOC14A	TXD006-C/ SMOSI006-C/ SSDA006/ TXDA006	ET1_LINKS TA/ CAT1_LINK STA		IRQ24	ADTRG1 #	
U19		P009	PIO_033			GTCPPO9/ GTIOC14B	RXD006-C/ SMISO006-C/ SSCL006	ET0_LINKS TA/ CAT0_LINK STA		IRQ25	ADTRG2 #	
U20		P001	PIO_001		TMCI0	GTCPPO0/ GTIOC10B/ GTIOC7A	SCK007-A/ CTS007#/ TXDB007/ SSIBCK0	ET0_LINKS TA/ CAT0_LINK STA		IRQ17-DS	AN017	DSM0_DA T0-B/ PCOUTZ0
V1		P709	PIO_017	A18-A		GTETRGD/ GTCPPO7/ GTIOC10B	RXD011-C/ SMISO011-C/ SSCL011	ET1_INT	XSPI1_IO5	IRQ17		DSM1_DA T2-G
V2		P711	PIO_019	A16-A		GTETRGB/ GTADSM1/ GTIOC11B	CTS010#/ CTS011#/ RTS011#/ SS011#/ DE011/ TXDB011	ET1_MDIO-C	XSPI1_IO7	IRQ19		DSM1_DA T1-G
V3		P605	PIO_013	CS2#-C/ D18-B		GTIOC6B	RXD009-B/ SMISO009-B/ SSCL009/ SSL02-D	ET1_TXD3-B/ ET_TAS_ST A1/ CAT1_ETX D3-B	XSPI0_INT0 #/ XSPI0_ECS 0#	IRQ13		DSM1_DA T1-A
V4		P603	PIO_011	WE#-B/ D20-B		GTIOC5B	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008/ CTS009#/ MISO0-D	ET1_TXD1-B/ RMII1_TXD 1-B/ GPTP_PTP OUT3/ CAT1_ETX D1-B/ CATSYNC0	XSPI0_IO7/ PCKO	IRQ3		DSM1_DA T0-A
V5		P600	PIO_008	SDCS#-B/ D23-B		GTIOC4A	TXD008-B/ SMOSI008-B/ SSDA008/ TXDA008/ SSL00-D	ET1_TX_CL K-B/ GPTP_PTP OUT0/ CAT1_TX_C LK-B/ CATLATCH 1	XSPI0_IO4/ PIXCLK	IRQ0	ADTRG0 #	
V6		P601	PIO_009	RAS#-B/ D22-B		GTIOC4B	RXD008-B/ SMISO008-B/ SSCL008/ RSPCK0-D	ET1_TX_EN -B/ RMII1_TX_ EN-B/ GPTP_PTP OUT1/ CAT1_TX_E N-B/ CATSYNC1	XSPI0_IO5/ VSYNC	IRQ1	ADTRG1 #	
V7		P905	PIO_005			GTCPPO1/ POEGB	RXD006-B/ SMISO006-B/ SSCL006	ET0_CRS/ GPTP_PTP OUT1		IRQ13		
V8		P904	PIO_004			GTCPPO0/ POEGC	TXD006-B/ SMOSI006-B/ SSDA006/ TXDA006	ET0_COL/ GPTP_PTP OUT0		IRQ12		
V9	AVCC0											

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (18/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
V10	AVSS0											
V11	VREFL00											
V12	VREFH00											
V13		P412	PIO_060							IRQ28-DS	AN012	
V14		P413	PIO_061							IRQ29	AN013	
V15		P414	PIO_062							IRQ30	AN014/ DA0	
V16		P415	PIO_063							IRQ31	AN015/ DA1	
V17		P014	PIO_038			GTCPPO1 4		ET0_COL/ GPTP_MAT CH1/ CATSYNC1		IRQ30		DSM1_CL K2-E
V18		P011	PIO_035			GTCPPO1 1/ GTIOC15B	CTS006#/ RTS006#/ SS006#/ DE006/ TXDB006	ET1_WOL/ GPTP_MAT CH0/ CAT0_MDIO -C		IRQ27		DSM1_DA T0-E
V19		P010	PIO_034			GTCPPO1 0/ GTIOC15A	SCK006-C/ CTS006#/ TXDB006	ET0_WOL/ GPTP_CAP TURE0/ CAT0_MDC-C		IRQ26		DSM1_CL K0-E
V20		P002	PIO_002		TMCI1	GTCPPO1/ GTIOC11A/ GTIOC7B	TXD007-A/ SMOSI007-A/ SSDA007/ TXDA007/ SSIBCK1	ET0_MDC-D/ CAT0_MDC-E		IRQ18-DS	AN018	DSM0_CL K1-B/ PCOUTA0
W1		P708	PIO_016	A19-A		GTETRGC/ GTCPPO4/ GTIOC10A	SCK011-C/ CTS011#/ TXDB011	ET0_INT	XSPI1_IO4	IRQ16		DSM1_CL K2-G
W2		P710	PIO_018	A17-A		GTETRGA/ GTADSM0/ GTIOC11A	TXD011-C/ SMOSI011-C/ SSDA011/ TXDA011	ET1_MDC-C	XSPI1_IO6	IRQ18		DSM1_CL K1-G
W3		PD05	PIO_037	A18-B/ D26-B		GTIU/ GTIOC2B/ POEGD	SCK003-A/ CTS003#/ TXDB003/ SSL22-A/ CTX0	ET1_RX_D V-B/ RMII1_CRS _DV-B/ CAT1_RX_ DV-B/ CATLEDST ER	SD0_DAT1-B/ XSPI0_IO3/ PIXD5	IRQ5	AN029	
W4		PD03	PIO_035	A20-B/ D28-B	TOC2	GTIOC1B/ POEGA	TXD002-A/ SMOSI002-A/ SSDA002/ TXDA002/ MISO2-A	ET1_RXD3-B/ CAT1_ERX D3-B/ CAT0_MDIO -D	SD0_CLK-B/ XSPI0_IO1/ PIXD3	IRQ3	AN027	
W5	VSS											
W6		PD02	PIO_034	A21-B/ D29-B	TIC2	GTETRGB/ GTIOC1A/ POEGB	RXD002-A/ SMISO002-A/ SSCL002/ MOSI2-A	ET1_RXD2-B/ CAT1_ERX D2-B/ CAT0_MDC-D	SD0_CMD-B/ XSPI0_IO0/ PIXD2	IRQ2	AN026	
W7		P902	PIO_002			GTETRGC/ GTCPPO8	SCK001-C/ CTS001#/ TXDB001	ET1_MDC-B/ ET_TAS_ST A2/ CATRESTO UT	XSPI0_RES ET1#	IRQ10	AN034	

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (19/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
W8		P900	PIO_000			GTETRGA/ GTCPPO5	RXD001-C/ SMISO001-C/ SSCL001	ET1_COL/ ET_TAS_STA0/ CATSYNC1	XSPI0_INT1#/ XSPI0_ECS1#	IRQ0	AN032	
W9	AVCC0											
W10	AVSS0											
W11	VREFL01											
W12	VREFH01											
W13		P403	PIO_051							IRQ11-DS	AN003	
W14		P401	PIO_049							IRQ9-DS	AN001	
W15		P411	PIO_059							IRQ27-DS	AN011	
W16		P409	PIO_057							IRQ25-DS	AN009	
W17	VSS											
W18		P006	PIO_006			GTCPPO5/ GTIOC13A/ GTIOC9B	SCK000-B/ CTS000#/ TXDB000	ET1_LINKSTA/ CAT1_LINKSTA		IRQ22-DS	ADTRG1#/AN022	PDMCLK0/ PCOUTZ1
W19		P004	PIO_004			GTCPPO3/ GTIOC12A/ GTIOC8B	TXD000-B/ SMOSI000-B/ SSDA000/ TXDA000/ SSITXD1	ET1_MDC-D/ CATSYNC0		IRQ20-DS	AN020	DSM0_CLK2-B/ PCOUTA1
W20		P003	PIO_003			GTCPPO2/ GTIOC11B/ GTIOC8A	RXD007-A/ SMISO007-A/ SSCL007/ SSIRXD1	ET0_MDIO-D/ CAT0_MDIO-E		IRQ19-DS	AN019	DSM0_DAT1-B/ PCOUTB0
Y1	VSS											
Y2		PD07	PIO_039	A16-B/ D24-B		GTIW/ GTIOC3B/ POEGA	TXD003-A/ SMOSI003-A/ SSDA003/ TXDA003/ CTX1	ET1_LINKSTA/ CAT1_LINKSTA	SD0_CD/ XSPI0_CS0#/ XSPI0_RESET1#/PIXD7	IRQ7	AN031	
Y3		PD06	PIO_038	A17-B/ D25-B		GTIV/ GTIOC3A/ POEGB	RXD003-A/ SMISO003-A/ SSCL003/ SSL23-A/ CRX1	ET1_RX_ER-B/ RMII1_RX_ER-B/ CAT1_RX_ER-B/ CATLEDER R	SD0_WP/ XSPI0_DS/ PIXD6	IRQ6	AN030	
Y4		PD04	PIO_036	A19-B/ D27-B		GTETRGA/ GTIOC2A/ POEGC	CTS002#/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ SSL21-A/ CRX0	ET1_RX_CLK-B/ RMII1_REF50CK-B/ CAT1_RX_CLK-B/ CATLEDRUN	SD0_DAT0-B/ XSPI0_IO2/ XSPI0_WP0#/PIXD4	IRQ4	AN028	
Y5		PD01	PIO_033	A22-B/ D30-B		GTETRGC/ GTIOC0B/ POEGC	SCK002-A/ CTS002#/ TXDB002/ RSPCK2-A	ET1_RXD1-B/ RMII1_RXD1-B/ CAT1_ERXD1-B/ CATSYNC0	SD0_DAT3-B/ XSPI0_CK/ PIXD1	IRQ1	AN025	

Table 1.5 List of Pin and Pin Functions (320-Pin LFBGA) (20/20)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
320-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
Y6		PD00	PIO_032	A23-B/ D31-B		GTETRGD/ GTIOC0A/ POEGD	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS003#/ SSL20-A	ET1_RXD0-B/ RMII1_RXD0-B/ CAT1_ERXD0-B/ CATLATCH0	SD0_DAT2-B/ XSPI0_CKN#/ XSPI0_CS1#/PIXD0	IRQ0	AN024	
Y7		P903	PIO_003			GTETRGD/ GTCPPO9/ POEGD	CTS006#/ CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001	ET1_MDIO-B/ ET_TAS_STA3/CATIRQ	XSPI0_WP1#	IRQ11	AN035	
Y8		P901	PIO_001			GTETRGB/ GTCPPO6	TXD001-C/ SMOSI001-C/ SSDA001/ TXDA001	ET1_CRS/ ET_TAS_STA1/ CATLATCH1	XSPI0_RSTO1#/ XSPI0_RESET0#	IRQ9	AN033	
Y9	AVCC0											
Y10	AVSS0											
Y11	VREFL02											
Y12	VREFH02											
Y13		P402	PIO_050							IRQ10-DS	AN002	
Y14		P400	PIO_048							IRQ8-DS	AN000	
Y15		P410	PIO_058							IRQ26-DS	AN010	
Y16		P408	PIO_056							IRQ24-DS	AN008	
Y17		P015	PIO_039			GTCPPO15		ET0_CRS/ GPTP1_PPS/ CATLATCH1		IRQ31		DSM1_DAT2-E
Y18		P007	PIO_007			GTCPPO6/ GTIOC13B/ POEGA	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000	ET1_INT/ CATIRQ		IRQ23-DS	ADTRG0#/AN023	PDMDAT0
Y19		P005	PIO_005			GTCPPO4/ GTIOC12B/ GTIOC9A	RXD000-B/ SMISO000-B/ SSCL000/ SSILRCK1	ET1_MDIO-D/ CATLATCH0		IRQ21-DS	ADTRG2#/AN021	DSM0_DAT2-B/ PCOUTB1
Y20	VSS											

1.6.2 224-Pin LFBGA

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (1/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
A1	VSS											
A2		PC03	PIO_027	D4-A		GTOVLO/ GTIOC8B	TXD011-A/ SMOSI011-A/ SSDA011/ TXDA011/ SDAHS1-C	ET0_TXD2-A/ RGMII0_TXD2-A/ CAT0_ETXD2-A	SD0_CLK-A	IRQ11		PCOUTA1
A3	ETHPHYCLK	PC07	PIO_031	D0-A	TMO2/ TOC0/ CACREF	GTETRGD/ GTADSM1/ GTIOC15B/ POEGA	TXD008-A/ SMOSI008-A/ SSDA008/ TXDA008/ MISO0-A/ SSITXD0	RGMII0_TXC-A/ CATRESTOUT	SD0_CD	IRQ14		DSM1_DAT2-C/ PDMDAT0
A4	CLKOUT	P801	PIO_057	EBCLK-A		GTIV/ GTIOC0B/ POEGC	TXD010-B/ SMOSI010-B/ SSDA010/ TXDA010	ET0_CRS/ CATSYNC0		IRQ9	ADCNV1	DSM1_DAT1-C
A5		P802	PIO_058	CS2#-A/ WR#-B/ WR0#-B		GTIW/ GTIOC1A/ POEGB	SCK010-B/ CTS010#/ TXDB010/ CRX2/ USB0_EXICEN	ET0_MDIO-B/ CAT0_MDIO-B		IRQ2	ADCNV2	DSM1_CLK0-C
A6	VLO											
A7	VSS_DCDC											
A8	VCC_DCDC											
A9		P103	PIO_011		TMO3	GTADSM1/ GTIOC13B	CTS002#/ SDA00-A	ET0_CRS/ CATI2CDATA-A		IRQ3		
A10		P104	PIO_012		TMRI2	GTIW/ GTIOC14A	RXD002-B/ SMISO002-B/ SSCL002/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ CTX2/ USB0_OVRCURA-DS/ USBHS_VBUS	ET0_TXD0-B/ RMII0_TXD0-B/ CAT0_ETXD0-B/ CATLEDSTER	PIXD0	IRQ4	ADST0	DSM0_CLK1-C/ PCINA0
A11	CLKOUT	P106	PIO_014		TMO2/ RTCOUT	GTIU/ GTIOC15A/ POEGB	RXD003-B/ SMISO003-B/ SSCL003/ SCLHS2-A	ET0_TXD2-B/ CAT0_ETXD2-B/ CATI2CCLK-B	SD0_DAT2-C/PIXD2	IRQ30-DS	ADTRG0#	PCINA1
A12		P200	PIO_016		TMRI0	GTETRGA/ GTIOC3A/ GTIOC14A	CTS006#/ RTS006#/ SS006#/ DE006/ TXDB006/ MOSI0-C/ SDAHS1-A/ USB0_ID/ SSIRXD0	ET0_TX_EN-B/ RMII0_TX_EN-B/ CAT0_TX_EN-B	SD0_CMD-C/PIXD4	IRQ8	ADTRG2#	PCINZ1

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (2/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
A13	TCK/ SWCLK	P301	PIO_025		TMCI3	GTCPPO11	SCK000-A/ CTS000#/ TXDB000/ SCK001-A/ CTS001#/ TXDB001/ RSPCK1-C	ET1_WOL		IRQ7		
A14	TDO	P302	PIO_026		TMRI3	GTCPPO12	TXD000-A/ SMOSI000-A/ SSDA000/ TXDA000/ TXD001-A/ SMOSI001-A/ SSDA001/ TXDA001/ MOSI1-C	ET1_COL		IRQ4		
A15	VSS											
B1		PC04	PIO_028	D3-A	TMCI1	GTOWUP/ GTIOC9A	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008/ CTS011#/ SSL00-A/ AUDIO_CLK	ET0_TXD3-A/ RGMII0_TXD3-A/ CAT0_ETXD3-A	SD0_DAT0-A	IRQ12		PCOUTB1
B2		PC01	PIO_025	D6-A		GTOULO/ GTIOC7B	SCK011-A/ CTS011#/ TXDB011/ SSL02-A/ SDA00-C	ET0_TXD0-A/ RMII0_TXD0-A/ RGMII0_TXD0-A/ CAT0_ETXD0-A	SD0_DAT3-A	IRQ12		PCOUTB0
B3		PC05	PIO_029	D2-A	TMRI2	GTOWLO/ GTIOC9B	SCK008-A/ CTS008#/ TXDB008/ RSPCK0-A/ SSIBCK0	ET0_TX_EN-A/ RMII0_TX_EN-A/ RGMII0_TX_CTL-A/ CAT0_TX_EN-A	SD0_DAT1-A	IRQ5		PCOUTZ1
B4		PC06	PIO_030	D1-A	TMCI2/ TIC0	GTETRGC/ GTCPPO7/ GTIOC15A/ POEGB	RXD008-A/ SMISO008-A/ SSCL008/ MOSI0-A/ SSILRCK0	ET0_TX_ER-A/ CATLINKACT0	SD0_WP	IRQ13		DSM1_CLK2-C/ PDMCLK0
B5		P803	PIO_059	CS3#-A/ WR1#-B/ BC1#-B		GTIOC1B/ POEGA	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ CTX2/ USB0_ID	ET0_MDC-B/ CAT0_MDC-B		IRQ3	ADSYNC	DSM1_DAT0-C
B6	VLO											
B7	VSS_DCDC											
B8	VCC_DCDC											
B9		P102	PIO_010		TMCI1	GTADSM0/ GTIOC13A	SCL00-A	ET0_COL/ CATI2CCLK-A		IRQ2		

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (3/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
B10		P105	PIO_013		TMCI2	GTIV/ GTIOC14B	TXD002-B/ SMOSI002-B/ SSDA002/ TXDA002/ SCK003-B/ CTS003#/ TXDB003/ CRX2/ USB0_VBUS/ USBHS_OVRCURB/ SSILRCK1	ET0_TXD1-B/ RMII0_TXD1-B/ CAT0_ETXD1-B/ CATLEDRUN	PIXD1	IRQ29-DS	ADST1	DSM0_DAT1-C/ PCINB0
B11		P107	PIO_015		TMO1	GTIV/ GTIOC15B/ POEGA	TXD003-B/ SMOSI003-B/ SSDA003/ TXDA003/ SDAHS2-A/ SSITXD0	ET0_TXD3-B/ CAT0_ETXD3-B/ CATI2CDATA-B	SD0_DAT3-C/PIXD3	IRQ31-DS	ADTRG1#	PCINB1
B12		P201	PIO_017		TMCI0	GTIW/ GTIOC3B/ GTIOC14B	SCK006-A/ CTS006#/ TXDB006/ MISO0-C/ SCLHS1-A/ USB0_EXICEN/SSILRCK0	ET0_RX_ER-B/ RMII0_RX_ER-B/ CAT0_RX_ER-B	SD0_CLK-C/PIXD5	IRQ9		PCINZ0
B13	TMS/ SWDIO	P300	PIO_024		TMO1	GTCPPO10	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000/ CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001/ SSL10-C	ET0_WOL		IRQ6		
B14	TDI	P303	PIO_027		TMCI2	GTCPPO13	RXD000-A/ SMISO000-A/ SSCL000/ RXD001-A/ SMISO001-A/ SSCL001/ MISO1-C	ET1_CRS		IRQ1		
B15	ETHPHYCLK	P304	PIO_028	ALE-C/ WAIT#-B	TMCI3	GTETRGD/ GTCPPO0/ POEGA	CTS000#/ CTS001#/ USB0_VBUSEN/ USBHS_ID	ET0_INT/ CATRESTOUT		IRQ0-DS	ADTRG0#	
C1		PC00	PIO_024	D7-A		GTOUUP/ GTIOC7A	CTS011#/ RTS011#/ SS011#/ DE011/ TXDB011/ SSL01-A/ SCL00-C	ET0_TX_CLK-A/ CAT0_TX_CLK-A	SD0_DAT2-A	IRQ14		PCOUTA0
C2		PC02	PIO_026	D5-A		GTOVUP/ GTIOC8A	RXD011-A/ SMISO011-A/ SSCL011/ SSL03-A/ SCLHS1-C	ET0_TXD1-A/ RMII0_TXD1-A/ RGMII0_TXD1-A/ CAT0_ETXD1-A	SD0_CMD-A	IRQ10		PCOUTZ0
C3		PB06	PIO_022	D9-A		GTOWUP/ GTIOC6A	RXD009-A/ SMISO009-A/ SSCL009	ET0_RX_ER-A/ RMII0_RX_ER-A/ CAT0_RX_ER-A		IRQ6		

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (4/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
C4		PB05	PIO_021	D10-A	TMRI1	GTOVLO/ GTIOC5B	SCK009-A/ CTS009#/ TXDB009	ET0_RX_DV-A/ RMII0_CRS_DV-A/ RGMII0_RX_CTL-A/ CAT0_RX_DV-A		IRQ13		
C5		P800	PIO_056	CS1#-A/ DQM0-B		GTIU/ GTIOC0A/ POEGD	RXD010-B/ SMISO010-B/ SSCL010	ET0_COL/ CATLATCH0		IRQ8	ADCNV0	DSM1_CLK1-C
C6	VLO											
C7		P100	PIO_008	CS1#-B/ WAIT#-A	TMRI3/ CACREF	GTIU/ GTADSM0/ GTIOC12A	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS005#/ USB0_OVRCURB-DS/ USBHS_VBUS	ET0_TX_ER-B/ CATLINKACT0/ CATLEDER R		IRQ0	ADTRG2#	DSM0_CLK0-C
C8	VCC_DCDC											
C9		P804	PIO_060			GTADSM0/ GTIOC15A	CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ SSL21-B/ CTX0/ USB0_OVRCURA/ USBHS_OVRCURA	ET0_TX_EN-C/ RMII0_TX_EN-C/ CAT0_TX_EN-C	PCKO	IRQ4		DSM0_CLK0-F/ PCINA0
C10		P805	PIO_061			GTADSM1/ GTIOC15B	SCK005-B/ CTS005#/ TXDB005/ SSL22-B/ CRX0/ USB0_VBUSEN/ USBHS_VBUSEN	ET0_TXD0-C/ RMII0_TXD0-C/ CAT0_ETXD0-C	HSYNC	IRQ5	ADSYNC	DSM0_DAT0-F/ PCINB0
C11		P114	PIO_046			GTCPPO14	TXD012-B/ SMOSI012-B/ SSDA012/ TXDA012/ SSL23-C	ET1_TX_ER-C/ CATLINKACT1	PIXD6	IRQ22	ADST2	DSM0_CLK0-H
C12		P111	PIO_043			GTCPPO11	CTS012#/ CTS009#/ RTS009#/ SS009#/ DE009/ TXDB009/ SSL20-C	ET0_RXD1-C/ RMII0_RXD1-C/ CAT0_ERXD1-C	SD0_DAT7-C/PIXD3	IRQ19		
C13		P108	PIO_040		TIC0	GTCPPO8	SCK009-C/ CTS009#/ TXDB009/ RSPCK2-C	ET0_RX_DV-C/ RMII0_CRS_DV-C/ CAT0_RX_DV-C	SD0_DAT4-C/PIXD0	IRQ16	ADCNV0	DSM0_CLK2-F
C14		P110	PIO_042			GTCPPO10	TXD009-C/ SMOSI009-C/ SSDA009/ TXDA009/ MISO2-C	ET0_RXD0-C/ RMII0_RXD0-C/ CAT0_ERXD0-C	SD0_DAT6-C/PIXD2	IRQ18	ADCNV2	

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (5/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
C15		P113	PIO_045			GTCPPO13	SCK012-B/ CTS012#/ TXDB012/ SSL22-C	ET0_RXD3-C/ CAT0_ERXD3-C	PIXD5	IRQ21	ADST1	DSM0_DAT1-H/ PDMDAT0
D1		PG00	PIO_056	DQM1-A/ WR1#-C/ BC1#-C		GTCPPO0	SCK008-C/ CTS008#/ TXDB008	ET1_RX_CLK-A/ RMII1_REF50CK-A/ RGMII1_RXC-A/ CAT1_RX_CLK-A		IRQ8		DSM0_CLK2-D
D2		PG02	PIO_058	DQM3-A/ WR3#-C/ BC3#-C		GTIOC11A	TXD008-C/ SMOSI008-C/ SSDA008/ TXDA008	ET1_RX_ER-A/ RMII1_RX_ER-A/ CAT1_RX_ER-A		IRQ10		DSM0_CLK1-D
D3		PB04	PIO_020	D11-A		GTOVUP/ GTIOC5A	CTS004#/ CTS009#/ RTS009#/ SS009#/ DE009/ TXDB009	ET0_RX_CLK-A/ RMII0_REF50CK-A/ RGMII0_RXC-A/ CAT0_RX_CLK-A		IRQ4		
D4		PB07	PIO_023	D8-A		GTOWLO/ GTIOC6B	TXD009-A/ SMOSI009-A/ SSDA009/ TXDA009	ET0_LINKSTA/ CAT0_LINKSTA		IRQ15		
D5		P502	PIO_034	WR2#-A/ BC2#-A/ A18-C		GTIOC3A	TXD002-C/ SMOSI002-C/ SSDA002/ TXDA002/ SSL13-C/ CTX1	ET0_WOL/ CATLEDRUN	SD0_DAT6-A	IRQ2	ADST2	DSM0_CLK1-E
D6		P500	PIO_032	WR#-A/ WR0#-A/ A16-C		GTIOC2A	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS007#/ SSL11-C/ CTX0	ET0_LINKSTA/ CAT0_LINKSTA	SD0_DAT4-A	IRQ0	ADST0	DSM0_CLK2-E
D7		P101	PIO_009	CS0#-A/ ALE-B	TMCI3	GTETRGC/ GTADSM1/ GTIOC12B	SCK002-B/ CTS002#/ TXDB002/ USB0_VBUS-DS/ USBHS_EXICEN	ET0_TX_CLK-B/ CAT0_TX_CLK-B/ CAT0_LINKSTA		IRQ1	ADTRG1#	DSM0_DAT0-C
D8		P504	PIO_036		TMCI1	GTETRGA/ GTIOC4A	CTS002#/ RXD007-B/ SMISO007-B/ SSCL007/ MOSI2-B	ET0_TX_ER-C/ GPTP_CAPTURE0/ CATLINKACT0		IRQ4		DSM0_CLK0-E
D9		P506	PIO_038			GTETRGC/ GTIOC5A/ POEGD	SCK007-B/ CTS007#/ TXDB007/ RSPCK2-B	ET0_TXD2-C/ GPTP0_PPS/ CAT0_ETXD2-C		IRQ6		
D10		P806	PIO_062			GTCPPO7/ GTIOC14A	RXD005-B/ SMISO005-B/ SSCL005/ SSL23-B/ CTX1	ET0_TXD1-C/ RMII0_TXD1-C/ CAT0_ETXD1-C	VSYNC	IRQ14		DSM0_CLK1-F/ PCINA1

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (6/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
D11		P109	PIO_041		TOC0	GTCPPO9	RXD009-C/ SMISO009-C/ SSCL009/ MOSI2-C	ET0_RX_CLK-C/ RMII0_REF50CK-C/ CAT0_RX_CLK-C	SD0_DAT5-C/PIXD1	IRQ17	ADCNV1	DSM0_DAT2-F
D12		P115	PIO_047			GTCPPO15	RXD012-B/ SMISO012-B/ SSCL012	ET1_TX_CLK-C/ CAT1_TX_CLK-C	PIXD7	IRQ23		DSM0_DAT0-H
D13		P112	PIO_044			GTCPPO12	CTS012#/ RTS012#/ SS012#/ DE012/ TXDB012/ CTS009#/ SSL21-C	ET0_RXD2-C/ CAT0_ERXD2-C	PIXD4	IRQ20	ADST0	DSM0_CLK1-H/ PDMCLK0
D14	VSS											
D15	VCC											
E1		PG01	PIO_057	DQM0-A/ WR#-C/ WR0#-C		GTCPPO1	RXD008-C/ SMISO008-C/ SSCL008	ET1_RX_DV-A/ RMII1_CRS_DV-A/ RGMII1_RX_CTL-A/ CAT1_RX_DV-A		IRQ9		DSM0_DAT2-D
E2		PG03	PIO_059	DQM2-A/ WR2#-C/ BC2#-C		GTIOC11B	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008	ET0_INT/ GPTP_MATCH1		IRQ11		DSM0_DAT1-D
E3		PB02	PIO_018	D13-A		GTOUUP/ GTIOC4A	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004/ CTS009#	ET0_RXD2-A/ RGMII0_RXD2-A/ CAT0_ERXD2-A		IRQ2		
E4		PB03	PIO_019	D12-A	TMO0	GTOULO/ GTIOC4B	SCK004-A/ CTS004#/ TXDB004	ET0_RXD3-A/ RGMII0_RXD3-A/ CAT0_ERXD3-A		IRQ3		
E5	VCC											
E6		P501	PIO_033	WR1#-A/ BC1#-A/ A17-C		GTIOC2B	SCK002-C/ CTS002#/ TXDB002/ SSL12-C/ CRX0	ET0_INT/ CATLEDSTER	SD0_DAT5-A	IRQ1	ADST1	DSM0_DAT2-E
E7		P503	PIO_035	WR3#-A/ BC3#-A/ A19-C		GTIOC3B	RXD002-C/ SMISO002-C/ SSCL002/ CRX1/ USB0_OVRCURB/ SSIRXD0	ET1_WOL/ CATLEDER R	SD0_DAT7-A	IRQ3		DSM0_DAT1-E
E8		P505	PIO_037		TMO3	GTETRGB/ GTIOC4B	TXD007-B/ SMOSI007-B/ SSDA007/ TXDA007/ MISO2-B	ET0_TX_CLK-C/ GPTP_MATCH0/ CAT0_TX_CLK-C		IRQ10		DSM0_DAT0-E

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (7/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
E9		P507	PIO_039			GTETRGD/ GTIOC5B/ POEGC	CTS007#/ RTS007#/ SS007#/ DE007/ TXDB007/ SSL20-B	ET0_TXD3-C/ GPTP1_PPS/ CAT0_ETXD3-C		IRQ7		
E10		P807	PIO_063			GTCPPO4/ GTIOC14B/ POEGD	TXD005-B/ SMOSI005-B/ SSDA005/ TXDA005/ CRX1	ET0_RX_ER-C/ RMII0_RX_ER-C/ CAT0_RX_ER-C	PIXCLK	IRQ15		DSM0_DAT1-F/ PCINB1
E11		PF02	PIO_050	CS6#-B/ BREQ#-C		GTCPPO1/ GTIOC7A	RXD000-C/ SMISO000-C/ SSCL000/ RXD007-C/ SMISO007-C/ SSCL007	ET1_TXD2-C/ CAT1_ETXD2-C		IRQ2	ADSYNC	DSM1_CLK0-F
E12		PF04	PIO_052	CS4#-B		GTCPPO3/ GTIOC8A	SCK000-C/ CTS000#/ TXDB000/ SCK007-C/ CTS007#/ TXDB007	ET1_TXD0-C/ RMII1_TXD0-C/ CAT1_ETXD0-C		IRQ4		DSM1_CLK1-F
E13		PF03	PIO_051	CS7#-B/ BACK#-C		GTCPPO2/ GTIOC7B	TXD000-C/ SMOSI000-C/ SSDA000/ TXDA000/ TXD007-C/ SMOSI007-C/ SSDA007/ TXDA007	ET1_TXD3-C/ CAT1_ETXD3-C		IRQ3		DSM1_DAT0-F
E14		PF00	PIO_048			GTCPPO14	USB0_DP			IRQ0		
E15		PF01	PIO_049			GTCPPO15	USB0_DM			IRQ1		
F1		PA05	PIO_013	A2-A		GTIOC2B/ GTIOC12B	SCK010-A/ CTS010#/ TXDB010/ RSPCK0-B	ET1_TXD2-A/ RGMII1_TXD2-A/ CAT1_ETXD2-A		IRQ5		PCINA0
F2	ETHPHYCLK	PA07	PIO_015	A0-A/ BC0#-A/ DQM1-B		GTIOC3B/ GTIOC13B	RXD010-A/ SMISO010-A/ SSCL010/ MISO0-B	ET1_TX_ER-A/ CATLINKACT1		IRQ7		PCINB0
F3		PB01	PIO_017	D14-A	TMCI0	GTETRGB/ GTCPPO4/ GTIOC14B/ POEGA	TXD004-A/ SMOSI004-A/ SSDA004/ TXDA004	ET0_RXD1-A/ RMII0_RXD1-A/ RGMII0_RXD1-A/ CAT0_ERXD1-A		IRQ4-DS		DSM0_DAT2-A/ PCINB1
F4		PB00	PIO_016	D15-A		GTETRGA/ GTADSM0/ GTIOC14A/ POEGC	RXD004-A/ SMISO004-A/ SSCL004	ET0_RXD0-A/ RMII0_RXD0-A/ RGMII0_RXD0-A/ CAT0_ERXD0-A		IRQ12	ADST2	DSM0_CLK2-A/ PCINA1
F5	VSS											
F6	VCL											
F7	VSS											
F8	VCC											

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (8/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
F9	VSS											
F10	VSS											
F11		PF05	PIO_053	CS5#-B		GTCPPO5/ GTIOC8B/ POEGD	CTS007#/ RTS007#/ SS007#/ DE007/ TXDB007/ SSL01-C	ET1_TXD1-C/ RMII1_TXD1-C/ CAT1_ETXD1-C		IRQ5		DSM1_DAT1-F
F12		P202	PIO_018	CS3#-B/ BREQ#-A	TMO0	GTOUUP/ GTIOC0A/ GTIOC4A	TXD006-A/ SMOSI006-A/ SSDA006/ TXDA006/ RSPCK0-C/ SCL00-B/ CTX2/ USB0_OVRCURA/ USBHS_EXICEN/ AUDIO_CLK	ET0_RX_DV-B/ RMII0_CRS_DV-B/ CAT0_RX_DV-B/ CATI2CCLK-C	SD0_DAT0-C/PIXD6	IRQ15		DSM1_CLK0-B/ PDMCLK0
F13		P203	PIO_019	CS2#-B/ BACK#-A		GTOULO/ GTIOC0B/ GTIOC4B	RXD006-A/ SMISO006-A/ SSCL006/ CTS003#/ SSL00-C/ SDA00-B/ CRX2/ USB0_OVRCURB/ USBHS_ID/ SSIBCK0	ET0_RX_CLK-B/ RMII0_REF50CK-B/ CAT0_RX_CLK-B/ CATI2CDATA-C	SD0_DAT1-C/PIXD7	IRQ3		DSM1_DAT0-B/ PDMDAT0
F14	VCC_USB											
F15	VSS_USB											
G1		PA04	PIO_012	A3-A	TMRI0	GTIOC2A/ GTIOC12A	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ SSL00-B	ET1_TXD1-A/ RMII1_TXD1-A/ RGMII1_TXD1-A/ CAT1_ETXD1-A		IRQ5-DS		PCINZ0
G2		PA06	PIO_014	A1-A/ DQM2-B	TMCI3	GTIOC3A/ GTIOC13A	TXD010-A/ SMOSI010-A/ SSDA010/ TXDA010/ MOSI0-B	ET1_TXD3-A/ RGMII1_TXD3-A/ CAT1_ETXD3-A		IRQ14		PCINZ1
G3		PG05	PIO_061	A10-A		GTIOC12B	RXD003-C/ SMISO003-C/ SSCL003	ET0_MDIO-A/ CAT0_MDIO-A		IRQ13		
G4		PG07	PIO_063	A8-A		GTIOC13B	CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003	ET0_CRS		IRQ15		
G5		PF09	PIO_017	A20-A/ A16-D			CTS012#	GPTP_CAPTURE1	XSPI1_INT0#/ XSPI1_ECS0#	IRQ17		
G6	VSS											
G7	VCL											
G8	VSS											
G9	VCL											
G10	VCL											

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (9/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
G11	CLKOUT	P205	PIO_021	A21-C/ CS6#-C		GTOVLO/ GTIOC1B/ GTIOC5B	SCK001-B/ CTS001#/ TXDB001/ RSPCK1-B/ SDAHS1-B/ CRX0/ USB0_VBUS/ USBHS_VBUSEN/ SSIRXD1	ET0_RXD1-B/ RMII0_RXD1-B/ CAT0_ERXD1-B	SD0_CD/ HSYNC	IRQ5	ADTRG0#	DSM1_DAT1-B/ PCOUTB1
G12	ETHPHYCLK	P204	PIO_020	A20-C/ CS7#-C	TMRI1	GTOVUP/ GTIOC1A/ GTIOC5A	CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001/ SSL10-B/ SCLHS1-B/ CTX0/ USB0_VBUSEN/ USBHS_VBUS-DS/ SSIBCK1	ET0_RXD0-B/ RMII0_RXD0-B/ CAT0_ERXD0-B	SD0_WP/ PIXCLK	IRQ12		DSM1_CLK1-B/ PCOUTA1
G13	VCC_USBHS											
G14							USBHS_DP					
G15							USBHS_DM					
H1		PA02	PIO_010	A5-A		GTIW/ GTIOC1A/ GTIOC11A	TXD005-A/ SMOSI005-A/ SSDA005/ TXDA005/ SSL03-B	ET1_TX_CLK-A/ CAT1_TX_CLK-A		IRQ10	ADCNV2	DSM0_CLK1-A
H2		PA03	PIO_011	A4-A		GTIOC1B/ GTIOC11B	RXD005-A/ SMISO005-A/ SSCL005	ET1_TXD0-A/ RMII1_TXD0-A/ RGMII1_TXD0-A/ CAT1_ETXD0-A		IRQ6-DS	ADSYNC	DSM0_DAT1-A
H3		PG06	PIO_062	A9-A		GTIOC13A	TXD003-C/ SMOSI003-C/ SSDA003/ TXDA003	ET0_COL		IRQ14		
H4		PG04	PIO_060	A11-A		GTIOC12A	SCK003-C/ CTS003#/ TXDB003	ET0_MDC-A/ CAT0_MDC-A		IRQ12		
H5		PF08	PIO_016	A21-A/ A17-D		GTCPPO12/POEGA			XSPI1_RESET0#	IRQ16		
H6	VCC											
H7	VSS											
H8	VCL											
H9	VSS											
H10	VCL											

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (10/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
H11		P206	PIO_022	A22-C/ CS5#-C	TMO3/ RTCOUT	GTOWUP/ GTIOC2A/ GTIOC6A	CTS006#/ TXD001-B/ SMOSI001-B/ SSDA001/ TXDA001/ MOSI1-B/ SCLHS2-B/ CTX1/ USB0_EXICEN/ USBHS_OVRCURA-DS/ SSITXD1	ET0_RXD2-B/ CAT0_ERXD2-B	VSYNC	IRQ2-DS	ADTRG1#	DSM1_CLK2-B/ PCOUTZ1
H12	AVSS_USBHS											
H13	USBHS_REF											
H14	VSS_USBHS											
H15	VCC											
J1	ETHPHYCLK	PA00	PIO_008	A7-A	CACREF	GTIU/ GTIOC0A/ GTIOC10A	CTS010#/ CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ SSL01-B	RGMII1_TXC-A/ CATIRQ		IRQ1-DS	ADCNV0	DSM0_CLK0-A
J2		PA01	PIO_009	A6-A		GTIV/ GTIOC0B/ GTIOC10B	SCK005-A/ CTS005#/ TXDB005/ SSL02-B	ET1_TX_EN-A/ RMII1_TX_EN-A/ RGMII1_TX_CTL-A/ CAT1_TX_EN-A		IRQ11	ADCNV1	DSM0_DAT0-A
J3		P703	PIO_051	ALE-A/ WR2#-B/ BC2#-B	CACREF	GTETRGB/ GTIOC11B	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004	ET1_LINKSTA/ CAT1_LINKSTA	XSPI1_RESET0#/PCKO	IRQ8		DSM1_DAT1-D
J4		PF06	PIO_054	A23-A/ A19-D		GTCPPO6/ GTIOC9A/ POEGC	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000/ CTS007#/ SSL02-C		XSPI1_CS1#/ XSPI1_WP0#	IRQ6		DSM1_CLK2-F
J5		PF07	PIO_055	A22-A/ A18-D		GTCPPO11/GTIOC9B	SSL03-C		XSPI1_RSTO0#	IRQ7		DSM1_DAT2-F
J6	VSS											
J7	VCL											
J8	VSS											
J9	VCL											
J10	VSS											
J11		P207	PIO_023	A23-C/ CS4#-C	TMRI3	GTOWLO/ GTIOC2B/ GTIOC6B	RXD001-B/ SMISO001-B/ SSCL001/ MISO1-B/ SDAHS2-B/ CRX1/ USB0_ID/ USBHS_OVRCURB-DS	ET0_RXD3-B/ CAT0_ERXD3-B	PCKO	IRQ3-DS	ADTRG2#	DSM1_DAT2-B
J12		P305								NMI/IRQ0		

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (11/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
J13	AVCC_USBHS											
J14	XTAL	P307										
J15	EXTAL	P306										
K1		P707	PIO_055	WE#-A/ CS7#-A		GTIOC13B	TXD011-B/ SMOSI011-B/ SSDA011/ TXDA011	ET1_RXD3-A/ RGMII1_RXD3-A/ CAT1_ERXD3-A	XSPI1_RESET1#	IRQ7		DSM0_DAT0-D
K2		P706	PIO_054	CAS#-A/ CS6#-A		GTIOC13A	RXD011-B/ SMISO011-B/ SSCL011	ET1_RXD2-A/ RGMII1_RXD2-A/ CAT1_ERXD2-A	XSPI1_WP1#	IRQ14	ADCNV2	DSM0_CLK0-D
K3		P702	PIO_050	RD#-A/ DQM3-B		GTETRGA/ GTIOC11A	SCK004-B/ CTS004#/ TXDB004	ET1_CRS/ CATSYNC1	XSPI1_WP0#/ XSPI1_RESET1#/ HSYNC	IRQ10	ADST2	DSM1_CLK1-D
K4		P605	PIO_013	CS2#-C/ D18-B		GTIOC6B	RXD009-B/ SMISO009-B/ SSCL009/ SSL02-D	ET1_TXD3-B/ ET_TAS_STA1/ CAT1_ETXD3-B	XSPI0_INT0#/ XSPI0_ECS0#	IRQ13		DSM1_DAT1-A
K5	VSS											
K6	VCC											
K7	VSS											
K8	VCC2											
K9	VCL											
K10	VSS											
K11		P310	PIO_058		RTCIC0/ CACREF	GTETRGB/ GTCPPO1/ POEGC	CTS000#/ CTS001#/ SSL11-B/ SSITXD0	ET1_INT/ CATIRQ		IRQ18	ADTRG0#	TAMPI0
K12		P311	PIO_059	BREQ#-B	RTCIC1	GTETRGC/ GTCPPO14/POEGD	CTS007#/ SSL12-B/ SSIRXD0	ET0_WOL		IRQ19	ADTRG1#	DSM0_CLK2-C/ TAMPI1
K13	MD/FINED	P315										
K14	VSS											
K15	VSS											
L1		P705	PIO_053	RAS#-A/ CS5#-A		GTIOC12B	SCK011-B/ CTS011#/ TXDB011	ET1_RXD1-A/ RMII1_RXD1-A/ RGMII1_RXD1-A/ CAT1_ERXD1-A	XSPI1_RSTO1#	IRQ13	ADCNV1	DSM1_DAT2-D
L2		P704	PIO_052	SDCS#-A/ CS4#-A		GTIOC12A	CTS004#/ CTS011#/ RTS011#/ SS011#/ DE011/ TXDB011	ET1_RXD0-A/ RMII1_RXD0-A/ RGMII1_RXD0-A/ CAT1_ERXD0-A	XSPI1_INT1#/ XSPI1_ECS1#	IRQ12	ADCNV0	DSM1_CLK2-D

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (12/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
L3		P604	PIO_012	CS3#-C/ D19-B		GTIOC6A	TXD009-B/ SMOSI009-B/ SSDA009/ TXDA009/ SSL01-D	ET1_TXD2-B/ ET_TAS_STA0/ CAT1_ETXD2-B	XSPI0_CS1#/ XSPI0_RSTO0#	IRQ4		DSM1_CLK1-A
L4		P606	PIO_014	CS1#-C/ D17-B		GTETRGA/ GTCPPO4/ GTIOC15A/ POEGC	SCK009-B/ CTS009#/ TXDB009/ SSL03-D/ CTX2	ET1_TX_ER-B/ ET_TAS_STA2/ CATLINKACT1	XSPI0_RESET0#	IRQ14		DSM1_CLK2-A
L5	VCC2											
L6		P904	PIO_004			GTCPPO0/ POEGC	TXD006-B/ SMOSI006-B/ SSDA006/ TXDA006	ET0_COL/ GPTP_PTPOUT0		IRQ12		
L7		P906	PIO_006			GTCPPO2/ POEGA	SCK006-B/ CTS006#/ TXDB006	ET0_MDC-C/ GPTP_PTPOUT2		IRQ14		
L8		P407	PIO_055							IRQ15-DS	AN007	
L9		P406	PIO_054							IRQ14-DS	AN006	
L10		P215	PIO_055			GTCPPO13	CTS004#/ CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ USBHS_ID	ET1_RXD3-C/ CAT1_ERXD3-C		IRQ31		PDMDAT0/PCINZ0
L11		P209	PIO_049		TOC1	GTETRGB	RXD004-C/ SMISO004-C/ SSCL004/ MOSI1-D	ET1_RX_CLK-C/ RMII1_REF50CK-C/ CAT1_RX_CLK-C		IRQ25		PCINB1
L12		P312	PIO_060	BACK#-B	RTCIC2	GTETRGD/ GTCPPO15/POEGA	SSL13-B/ SSILRCK0	ET1_WOL		IRQ20	ADTRG2#	DSM0_DAT2-C/ TAMPI2
L13	VCC											
L14	XCIN/ EXCIN	P309										
L15	XCOUT	P308										
M1	ETHPHYCLK	P700	PIO_048	SDCLK-A		GTIOC10A	TXD004-B/ SMOSI004-B/ SSDA004/ TXDA004	ET1_INT/ CATRESTOUT	XSPI1_INT0#/ XSPI1_ECS0#/PIXCLK	IRQ0	ADST0	DSM1_CLK0-D
M2		P701	PIO_049	CKE-A/ WR3#-B/ BC3#-B		GTIOC10B	RXD004-B/ SMISO004-B/ SSCL004	ET1_COL/ CATLATCH1	XSPI1_RSTO0#/ XSPI1_RESET0#/ VSYNC	IRQ1	ADST1	DSM1_DAT0-D
M3		P607	PIO_015	CS0#-B/ D16-B		GTETRGB/ GTADSM0/ GTIOC15B/ POEGA	CTS008#/ CTS009#/ RTS009#/ SS009#/ DE009/ TXDB009/ CRX2	ET1_INT/ ET_TAS_STA3/CATIRQ	XSPI0_RSTO0#	IRQ15		DSM1_DAT2-A

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (13/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
M4		P603	PIO_011	WE#-B/ D20-B		GTIOC5B	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008/ CTS009#/ MISO0-D	ET1_TXD1-B/ RMII1_TXD1-B/ GPTP_PTPOUT3/ CAT1_ETXD1-B/ CATSYNC0	XSPI0_IO7/ PCKO	IRQ3		DSM1_DAT0-A
M5		P907	PIO_007			GTCPPO3/ POEGD	CTS006#/ RTS006#/ SS006#/ DE006/ TXDB006/ CTS001#	ET0_MDIO-C/ GPTP_PTPOUT3	XSPI0_WP0#	IRQ15		
M6		P905	PIO_005			GTCPPO1/ POEGB	RXD006-B/ SMISO006-B/ SSCL006	ET0_CRS/ GPTP_PTPOUT1		IRQ13		
M7		P902	PIO_002			GTETRGC/ GTCPPO8	SCK001-C/ CTS001#/ TXDB001	ET1_MDC-B/ ET_TAS_STA2/ CATRESTOUT	XSPI0_RESET1#	IRQ10	AN034	
M8		P900	PIO_000			GTETRGA/ GTCPPO5	RXD001-C/ SMISO001-C/ SSCL001	ET1_COL/ ET_TAS_STA0/ CATSYNC1	XSPI0_INT1#/ XSPI0_ECS1#	IRQ0	AN032	
M9		P405	PIO_053							IRQ13-DS	AN005	
M10		P415	PIO_063							IRQ31	AN015/ DA1	
M11		P212	PIO_052			GTCPPO10	SCK005-C/ CTS005#/ TXDB005/ SSL11-D/ USBHS_OVRCURA	ET1_RX_DV-C/ RMII1_CRS_DV-C/ CAT1_RX_DV-C		IRQ28	ADTRG0#	
M12		P214	PIO_054			GTCPPO12	TXD005-C/ SMOSI005-C/ SSDA005/ TXDA005/ SSL13-D/ USBHS_EXICEN	ET1_RXD2-C/ CAT1_ERXD2-C		IRQ30	ADTRG2#	PDMCLK0/PCINB0
M13	RES#											
M14	VSS											
M15	VBATT/ VCC											
N1		PE07	PIO_047	A8-B/A20-D	TOC1	GTETRGD/ GTCPPO7/ GTIOC10B/ POEGD		ET1_LINKSTA/ CAT1_LINKSTA/ CATRESTOUT	XSPI1_CS0#/PIXD7	IRQ7		
N2		PE04	PIO_044	A11-B/ A23-D		GTOWUP/ GTIOC9A	CTS012#/ SSL11-A	ET1_RXD2-D/ CAT1_ERXD2-D/ CATLEDSTER	XSPI1_IO2/ XSPI1_WP0#/PIXD4	IRQ12		

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (14/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
N3		PE06	PIO_046	A9-B/A21-D	TIC1	GTETRGC/ GTADSM1/ GTIOC10A/ POEGB	SSL13-A	ET1_RX_CLK-D/ RMII1_REF50CK-D/ CAT1_RX_CLK-D/ CATLEDER R	XSPI1_DS/ PIXD6	IRQ6		
N4		P602	PIO_010	CAS#-B/ D21-B		GTIOC5A	SCK008-B/ CTS008#/ TXDB008/ MOSI0-D	ET1_TXD0-B/ RMII1_TXD0-B/ GPTP_PTPOUT2/ CAT1_ETXD0-B/ CATLATCH0	XSPI0_IO6/ HSYNC	IRQ2	ADTRG2#	DSM1_CLK0-A
N5		P601	PIO_009	RAS#-B/ D22-B		GTIOC4B	RXD008-B/ SMISO008-B/ SSCL008/ RSPCK0-D	ET1_TX_EN-B/ RMII1_TX_EN-B/ GPTP_PTPOUT1/ CAT1_TX_EN-B/ CATSYNC1	XSPI0_IO5/ VSYNC	IRQ1	ADTRG1#	
N6		P600	PIO_008	SDCS#-B/ D23-B		GTIOC4A	TXD008-B/ SMOSI008-B/ SSDA008/ TXDA008/ SSL00-D	ET1_TX_CLK-B/ GPTP_PTPOUT0/ CAT1_TX_CLK-B/ CATLATCH1	XSPI0_IO4/ PIXCLK	IRQ0	ADTRG0#	
N7		P903	PIO_003			GTETRGD/ GTCPPO9/ POEGD	CTS006#/ CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001	ET1_MDIO-B/ ET_TAS_STA3/CATIRQ	XSPI0_WP1#	IRQ11	AN035	
N8		P901	PIO_001			GTETRGB/ GTCPPO6	TXD001-C/ SMOSI001-C/ SSDA001/ TXDA001	ET1_CRS/ ET_TAS_STA1/ CATLATCH1	XSPI0_RSTO1#/ XSPI0_RESET0#	IRQ9	AN033	
N9		P404	PIO_052							IRQ12-DS	AN004	
N10		P414	PIO_062							IRQ30	AN014/ DA0	
N11		P210	PIO_050			GTETRGC	TXD004-C/ SMOSI004-C/ SSDA004/ TXDA004/ MISO1-D	ET1_RXD0-C/ RMII1_RXD0-C/ CAT1_ERXD0-C		IRQ26		PCINZ1
N12		P213	PIO_053			GTCPPO11	RXD005-C/ SMISO005-C/ SSCL005/ SSL12-D/ USBHS_VBUSEN	ET1_RX_ER-C/ RMII1_RX_ER-C/ CAT1_RX_ER-C		IRQ29	ADTRG1#	PCINA0
N13		P208	PIO_048		TIC1	GTETRGA	SCK004-C/ CTS004#/ TXDB004/ RSPCK1-D	ET1_TX_EN-C/ RMII1_TX_EN-C/ CAT1_TX_EN-C		IRQ24		PCINA1

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (15/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
N14		P211	PIO_051			GTETRGD	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004/ CTS005#/ SSL10-D/ USBHS_OVR CURB	ET1_RXD1-C/ RMII1_RXD 1-C/ CAT1_ERX D1-C		IRQ27		
N15		P000	PIO_000		TMRI0	GTCPPO7/ GTIOC10A/ POEGB	CTS000#/ CTS007#/ RTS007#/ SS007#/ DE007/ TXDB007/ AUDIO_CLK	ET0_INT/ CATRESTO UT		IRQ16-DS	AN016	DSM0_CL K0-B
P1		PE05	PIO_045	A10-B/ A22-D		GTOWLO/ GTIOC9B	SSL12-A	ET1_RXD3-D/ CAT1_ERX D3-D/ CATLEDRU N	XSPI1_IO3/ PIXD5	IRQ5		
P2		PE03	PIO_043	A12-B	TOC3	GTOVLO/ GTIOC8B	CTS012#/ RTS012#/ SS012#/ DE012/ TXDB012/ MISO1-A	ET1_RXD1-D/ RMII1_RXD 1-D/ CAT1_ERX D1-D	SD0_DAT7-B/ XSPI1_IO1/ PIXD3	IRQ11		
P3		PE02	PIO_042	A13-B	TIC3	GTOVUP/ GTIOC8A	RXD012-A/ SMISO012-A/ SSCL012/ MOSI1-A	ET1_RXD0-D/ RMII1_RXD 0-D/ CAT1_ERX D0-D	SD0_DAT6-B/ XSPI1_IO0/ PIXD2	IRQ7-DS		
P4		PD07	PIO_039	A16-B/ D24-B		GTIW/ GTIOC3B/ POEGA	TXD003-A/ SMOSI003-A/ SSDA003/ TXDA003/ CTX1	ET1_LINKS TA/ CAT1_LINK STA	SD0_CD/ XSPI0_CS0 #/ XSPI0_RES ET1#/PIXD7	IRQ7	AN031	
P5		PD05	PIO_037	A18-B/ D26-B		GTIU/ GTIOC2B/ POEGD	SCK003-A/ CTS003#/ TXDB003/ SSL22-A/ CTX0	ET1_RX_D V-B/ RMII1_CRS _DV-B/ CAT1_RX_ DV-B/ CATLEDST ER	SD0_DAT1-B/ XSPI0_IO3/ PIXD5	IRQ5	AN029	
P6		PD03	PIO_035	A20-B/ D28-B	TOC2	GTIOC1B/ POEGA	TXD002-A/ SMOSI002-A/ SSDA002/ TXDA002/ MISO2-A	ET1_RXD3-B/ CAT1_ERX D3-B/ CAT0_MDIO -D	SD0_CLK-B/ XSPI0_IO1/ PIXD3	IRQ3	AN027	
P7		PD02	PIO_034	A21-B/ D29-B	TIC2	GTETRGB/ GTIOC1A/ POEGB	RXD002-A/ SMISO002-A/ SSCL002/ MOSI2-A	ET1_RXD2-B/ CAT1_ERX D2-B/ CAT0_MDC-D	SD0_CMD-B/ XSPI0_IO0/ PIXD2	IRQ2	AN026	
P8	AVSS0											
P9	VREFL0											
P10		P403	PIO_051							IRQ11-DS	AN003	
P11		P401	PIO_049							IRQ9-DS	AN001	
P12		P006	PIO_006			GTCPPO5/ GTIOC13A/ GTIOC9B	SCK000-B/ CTS000#/ TXDB000	ET1_LINKS TA/ CAT1_LINK STA		IRQ22-DS	ADTRG1 #/AN022	PDMCLK0 / PCOUTZ1

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (16/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
P13		P004	PIO_004			GTCPPO3/ GTIOC12A/ GTIOC8B	TXD000-B/ SMOSI000-B/ SSDA000/ TXDA000/ SSITXD1	ET1_MDC-D/ CATSYNC0		IRQ20-DS	AN020	DSM0_CLK2-B/ PCOUTA1
P14		P003	PIO_003			GTCPPO2/ GTIOC11B/ GTIOC8A	RXD007-A/ SMISO007-A/ SSCL007/ SSIRXD1	ET0_MDIO-D/ CAT0_MDIO-E		IRQ19-DS	AN019	DSM0_DAT1-B/ PCOUTB0
P15		P001	PIO_001		TMCI0	GTCPPO0/ GTIOC10B/ GTIOC7A	SCK007-A/ CTS007#/ TXDB007/ SSIBCK0	ET0_LINKSTA/ CAT0_LINKSTA		IRQ17-DS	AN017	DSM0_DAT0-B/ PCOUTZ0
R1	VSS											
R2	CLKOUT	PE01	PIO_041	A14-B		GTOULO/ GTIOC7B	TXD012-A/ SMOSI012-A/ SSDA012/ TXDA012/ RSPCK1-A	ET1_RX_DV-D/ RMII1_CRS_DV-D/ CAT1_RX_DV-D	SD0_DAT5-B/ XSPI1_CK/ PIXD1	IRQ9		
R3	ETHPHYCLK	PE00	PIO_040	A15-B		GTOUUP/ GTIOC7A	SCK012-A/ CTS012#/ TXDB012/ SSL10-A	ET1_RX_ER-D/ RMII1_RX_ER-D/ CAT1_RX_ER-D	SD0_DAT4-B/ XSPI1_CKN#/ XSPI1_CS1#/PIXD0	IRQ8		
R4		PD06	PIO_038	A17-B/ D25-B		GTIV/ GTIOC3A/ POEGB	RXD003-A/ SMISO003-A/ SSCL003/ SSL23-A/ CRX1	ET1_RX_ER-B/ RMII1_RX_ER-B/ CAT1_RX_ER-B/ CATLEDER R	SD0_WP/ XSPI0_DS/ PIXD6	IRQ6	AN030	
R5		PD04	PIO_036	A19-B/ D27-B		GTETRGA/ GTIOC2A/ POEGC	CTS002#/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ SSL21-A/ CRX0	ET1_RX_CLK-B/ RMII1_REF50CK-B/ CAT1_RX_CLK-B/ CATLEDRUN	SD0_DAT0-B/ XSPI0_IO2/ XSPI0_WP0#/PIXD4	IRQ4	AN028	
R6		PD00	PIO_032	A23-B/ D31-B		GTETRGD/ GTIOC0A/ POEGD	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS003#/ SSL20-A	ET1_RXD0-B/ RMII1_RXD0-B/ CAT1_ERXD0-B/ CATLATCH0	SD0_DAT2-B/ XSPI0_CKN#/ XSPI0_CS1#/PIXD0	IRQ0	AN024	
R7		PD01	PIO_033	A22-B/ D30-B		GTETRGC/ GTIOC0B/ POEGC	SCK002-A/ CTS002#/ TXDB002/ RSPCK2-A	ET1_RXD1-B/ RMII1_RXD1-B/ CAT1_ERXD1-B/ CATSYNC0	SD0_DAT3-B/ XSPI0_CK/ PIXD1	IRQ1	AN025	
R8	AVCC0											
R9	VREFH0											
R10		P402	PIO_050							IRQ10-DS	AN002	
R11		P400	PIO_048							IRQ8-DS	AN000	

Table 1.6 List of Pin and Pin Functions (224-Pin LFBGA) (17/17)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
224-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
R12		P007	PIO_007			GTCPPO6/ GTIOC13B/ POEGA	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000	ET1_INT/ CATIRQ		IRQ23-DS	ADTRG0 #/AN023	PDMDAT0
R13		P005	PIO_005			GTCPPO4/ GTIOC12B/ GTIOC9A	RXD000-B/ SMISO000-B/ SSCL000/ SSILRCK1	ET1_MDIO-D/ CATLATCH 0		IRQ21-DS	ADTRG2 #/AN021	DSM0_DA T2-B/ PCOUTB1
R14		P002	PIO_002		TMCI1	GTCPPO1/ GTIOC11A/ GTIOC7B	TXD007-A/ SMOSI007-A/ SSDA007/ TXDA007/ SSIBCK1	ET0_MDC-D/ CAT0_MDC-E		IRQ18-DS	AN018	DSM0_CL K1-B/ PCOUTA0
R15	NC											

1.6.3 176-Pin LFBGA

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (1/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
A1		PC01	PIO_025	D6-A		GTOULO/ GTIOC7B	SCK011-A/ CTS011#/ TXDB011/ SSL02-A/ SDA00-C	ET0_TXD0-A/ RMII0_TXD0-A/ RGMII0_TXD0-A/ CAT0_ETXD0-A	SD0_DAT3-A	IRQ12		PCOUTB0
A2		PC03	PIO_027	D4-A		GTOVLO/ GTIOC8B	TXD011-A/ SMOSI011-A/ SSDA011/ TXDA011/ SDAHS1-C	ET0_TXD2-A/ RGMII0_TXD2-A/ CAT0_ETXD2-A	SD0_CLK-A	IRQ11		PCOUTA1
A3		PC05	PIO_029	D2-A	TMRI2	GTOWLO/ GTIOC9B	SCK008-A/ CTS008#/ TXDB008/ RSPCK0-A/ SSIBCK0	ET0_TX_EN-A/ RMII0_TX_EN-A/ RGMII0_TX_CTL-A/ CAT0_TX_EN-A	SD0_DAT1-A	IRQ5		PCOUTZ1
A4	ETHPHYCLK	PC07	PIO_031	D0-A	TMO2/ TOC0/ CACREF	GTETRGD/ GTADSM1/ GTIOC15B/ POEGA	TXD008-A/ SMOSI008-A/ SSDA008/ TXDA008/ MISO0-A/ SSITXD0	RGMII0_TXC-A/ CATRESTOUT	SD0_CD	IRQ14		DSM1_DAT2-C/ PDMDAT0
A5	CLKOUT	P801	PIO_057	EBCLK-A		GTIV/ GTIOC0B/ POEGC	TXD010-B/ SMOSI010-B/ SSDA010/ TXDA010	ET0_CRS/ CATSYNC0		IRQ9	ADCNV1	DSM1_DAT1-C
A6		P503	PIO_035	WR3#-A/ BC3#-A/ A19-C		GTIOC3B	RXD002-C/ SMISO002-C/ SSCL002/ CRX1/ USB0_OVRCURB/ SSIRXD0	ET1_WOL/ CATLEDER R	SD0_DAT7-A	IRQ3		DSM0_DAT1-E
A7	VLO											
A8	VSS_DCDC											
A9	VCC_DCDC											
A10		P102	PIO_010		TMCI1	GTADSM0/ GTIOC13A	SCL00-A	ET0_COL/ CATI2CCLK-A		IRQ2		
A11	CLKOUT	P106	PIO_014		TMO2/ RTCOUT	GTIU/ GTIOC15A/ POEGB	RXD003-B/ SMISO003-B/ SSCL003/ SCLHS2-A	ET0_TXD2-B/ CAT0_ETXD2-B/ CATI2CCLK-B	SD0_DAT2-C/PIXD2	IRQ30-DS	ADTRG0#	PCINA1
A12		P200	PIO_016		TMRI0	GTETRGA/ GTIOC3A/ GTIOC14A	CTS006#/ RTS006#/ SS006#/ DE006/ TXDB006/ MOSI0-C/ SDAHS1-A/ USB0_ID/ SSIRXD0	ET0_TX_EN-B/ RMII0_TX_EN-B/ CAT0_TX_EN-B	SD0_CMD-C/PIXD4	IRQ8	ADTRG2#	PCINZ1

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (2/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
A13		P805	PIO_061			GTADSM1/ GTIOC15B	SCK005-B/ CTS005#/ TXDB005/ SSL22-B/ CRX0/ USB0_VBUS EN/ USBHS_VBU SEN	ET0_TXD0-C/ RMII0_TXD 0-C/ CAT0_ETX D0-C	HSYNC	IRQ5	ADSYNC	DSM0_DA T0-F/ PCINB0
A14	TCK/ SWCLK	P301	PIO_025		TMCI3	GTCPPO1 1	SCK000-A/ CTS000#/ TXDB000/ SCK001-A/ CTS001#/ TXDB001/ RSPCK1-C	ET1_WOL		IRQ7		
A15	TDO	P302	PIO_026		TMRI3	GTCPPO1 2	TXD000-A/ SMOSI000-A/ SSDA000/ TXDA000/ TXD001-A/ SMOSI001-A/ SSDA001/ TXDA001/ MOSI1-C	ET1_COL		IRQ4		
B1		PC00	PIO_024	D7-A		GTOUUP/ GTIOC7A	CTS011#/ RTS011#/ SS011#/ DE011/ TXDB011/ SSL01-A/ SCL00-C	ET0_TX_CL K-A/ CAT0_TX_C LK-A	SD0_DAT2-A	IRQ14		PCOUTA0
B2		PC02	PIO_026	D5-A		GTOVUP/ GTIOC8A	RXD011-A/ SMISO011-A/ SSCL011/ SSL03-A/ SCLHS1-C	ET0_TXD1-A/ RMII0_TXD 1-A/ RGMII0_TX D1-A/ CAT0_ETX D1-A	SD0_CMD-A	IRQ10		PCOUTZ0
B3		PC04	PIO_028	D3-A	TMCI1	GTOWUP/ GTIOC9A	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008/ CTS011#/ SSL00-A/ AUDIO_CLK	ET0_TXD3-A/ RGMII0_TX D3-A/ CAT0_ETX D3-A	SD0_DAT0-A	IRQ12		PCOUTB1
B4		PC06	PIO_030	D1-A	TMCI2/ TIC0	GTETRGC/ GTCPPO7/ GTIOC15A/ POEGB	RXD008-A/ SMISO008-A/ SSCL008/ MOSI0-A/ SSILRCK0	ET0_TX_ER -A/ CATLINKAC T0	SD0_WP	IRQ13		DSM1_CL K2-C/ PDMCLK0
B5		P803	PIO_059	CS3#-A/ WR1#-B/ BC1#-B		GTIOC1B/ POEGA	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ CTX2/ USB0_ID	ET0_MDC-B/ CAT0_MDC-B		IRQ3	ADSYNC	DSM1_DA T0-C
B6		P502	PIO_034	WR2#-A/ BC2#-A/ A18-C		GTIOC3A	TXD002-C/ SMOSI002-C/ SSDA002/ TXDA002/ SSL13-C/ CTX1	ET0_WOL/ CATLEDRU N	SD0_DAT6-A	IRQ2	ADST2	DSM0_CL K1-E
B7	VLO											
B8	VSS_DCD C											

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (3/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
B9	VCC_DCDC											
B10		P103	PIO_011		TMO3	GTADSM1/ GTIOC13B	CTS002#/ SDA00-A	ET0_CRS/ CATI2CDATA-A		IRQ3		
B11		P107	PIO_015		TMO1	GTIV/ GTIOC15B/ POEGA	TXD003-B/ SMOSI003-B/ SSDA003/ TXDA003/ SDAHS2-A/ SSITXD0	ET0_TXD3-B/ CAT0_ETXD3-B/ CATI2CDATA-B	SD0_DAT3-C/PIXD3	IRQ31-DS	ADTRG1#	PCINB1
B12		P201	PIO_017		TMCI0	GTIW/ GTIOC3B/ GTIOC14B	SCK006-A/ CTS006#/ TXDB006/ MISO0-C/ SCLHS1-A/ USB0_EXICEN/SSILRCK0	ET0_RX_ER-B/ RMII0_RX_ER-B/ CAT0_RX_ER-B	SD0_CLK-C/PIXD5	IRQ9		PCINZ0
B13		P804	PIO_060			GTADSM0/ GTIOC15A	CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ SSL21-B/ CTX0/ USB0_OVRCURA/ USBHS_OVRCURA	ET0_TX_EN-C/ RMII0_TX_EN-C/ CAT0_TX_EN-C	PCKO	IRQ4		DSM0_CLK0-F/ PCINA0
B14	TMS/ SWDIO	P300	PIO_024		TMO1	GTCPPO10	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000/ CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001/ SSL10-C	ET0_WOL		IRQ6		
B15	TDI	P303	PIO_027		TMCI2	GTCPPO13	RXD000-A/ SMISO000-A/ SSCL000/ RXD001-A/ SMISO001-A/ SSCL001/ MISO1-C	ET1_CRS		IRQ1		
C1		PB06	PIO_022	D9-A		GTOWUP/ GTIOC6A	RXD009-A/ SMISO009-A/ SSCL009	ET0_RX_ER-A/ RMII0_RX_ER-A/ CAT0_RX_ER-A		IRQ6		
C2		PB07	PIO_023	D8-A		GTOWLO/ GTIOC6B	TXD009-A/ SMOSI009-A/ SSDA009/ TXDA009	ET0_LINKSTA/ CAT0_LINKSTA		IRQ15		
C3		P802	PIO_058	CS2#-A/ WR#-B/ WR0#-B		GTIW/ GTIOC1A/ POEGB	SCK010-B/ CTS010#/ TXDB010/ CRX2/ USB0_EXICEN	ET0_MDIO-B/ CAT0_MDIO-B		IRQ2	ADCNV2	DSM1_CLK0-C
C4	VCC											

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (4/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
C5		P500	PIO_032	WR#-A/ WR0#-A/ A16-C		GTIOC2A	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS007#/ SSL11-C/ CTX0	ET0_LINKSTA/ CAT0_LINKSTA	SD0_DAT4-A	IRQ0	ADST0	DSM0_CLK2-E
C6		P501	PIO_033	WR1#-A/ BC1#-A/ A17-C		GTIOC2B	SCK002-C/ CTS002#/ TXDB002/ SSL12-C/ CRX0	ET0_INT/ CATLEDSTER	SD0_DAT5-A	IRQ1	ADST1	DSM0_DAT2-E
C7	VLO											
C8	VCC_DCDC											
C9	VCC											
C10		P100	PIO_008	CS1#-B/ WAIT#-A	TMRI3/ CACREF	GTIU/ GTADSM0/ GTIOC12A	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS005#/ USB0_OVRCURB-DS/ USBHS_VBUS	ET0_TX_ER-B/ CATLINKACT0/ CATLEDER R		IRQ0	ADTRG2#	DSM0_CLK0-C
C11		P104	PIO_012		TMRI2	GTIW/ GTIOC14A	RXD002-B/ SMISO002-B/ SSCL002/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ CTX2/ USB0_OVRCURA-DS/ USBHS_VBUS	ET0_TXD0-B/ RMII0_TXD0-B/ CAT0_ETXD0-B/ CATLEDSTER	PIXD0	IRQ4	ADST0	DSM0_CLK1-C/ PCINA0
C12	CLKOUT	P205	PIO_021	A21-C/ CS6#-C		GTOVLO/ GTIOC1B/ GTIOC5B	SCK001-B/ CTS001#/ TXDB001/ RSPCK1-B/ SDAHS1-B/ CRX0/ USB0_VBUS/ USBHS_VBUSEN/ SSIRXD1	ET0_RXD1-B/ RMII0_RXD1-B/ CAT0_ERXD1-B	SD0_CD/ HSYNC	IRQ5	ADTRG0#	DSM1_DAT1-B/ PCOUTB1
C13	ETHPHYCLK	P304	PIO_028	ALE-C/ WAIT#-B	TMCI3	GTETRGD/ GTCPPO0/ POEGA	CTS000#/ CTS001#/ USB0_VBUSEN/ USBHS_ID	ET0_INT/ CATRESTOUT		IRQ0-DS	ADTRG0#	
C14		P202	PIO_018	CS3#-B/ BREQ#-A	TMO0	GTOUUP/ GTIOC0A/ GTIOC4A	TXD006-A/ SMOSI006-A/ SSDA006/ TXDA006/ RSPCK0-C/ SCL00-B/ CTX2/ USB0_OVRCURA/ USBHS_EXICEN/ AUDIO_CLK	ET0_RX_DV-B/ RMII0_CRS_DV-B/ CAT0_RX_DV-B/ CATI2CCLK-C	SD0_DAT0-C/PIXD6	IRQ15		DSM1_CLK0-B/ PDMCLK0

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (5/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
C15		P203	PIO_019	CS2#-B/ BACK#-A		GTOULO/ GTIOC0B/ GTIOC4B	RXD006-A/ SMISO006-A/ SSCL006/ CTS003#/ SSL00-C/ SDA00-B/ CRX2/ USB0_OVRCURB/ USBHS_ID/ SSIBCK0	ET0_RX_CLK-B/ RMII0_REF50CK-B/ CAT0_RX_CLK-B/ CATI2CDATA-C	SD0_DAT1-C/PIXD7	IRQ3		DSM1_DAT0-B/ PDMDAT0
D1		PB04	PIO_020	D11-A		GTOVUP/ GTIOC5A	CTS004#/ CTS009#/ RTS009#/ SS009#/ DE009/ TXDB009	ET0_RX_CLK-A/ RMII0_REF50CK-A/ RGMII0_RXC-A/ CAT0_RX_CLK-A		IRQ4		
D2		PB05	PIO_021	D10-A	TMRI1	GTOVLO/ GTIOC5B	SCK009-A/ CTS009#/ TXDB009	ET0_RX_DV-A/ RMII0_CRS_DV-A/ RGMII0_RX_CTL-A/ CAT0_RX_DV-A		IRQ13		
D3		PG01	PIO_057	DQM0-A/ WR#-C/ WR0#-C		GTCPPO1	RXD008-C/ SMISO008-C/ SSCL008	ET1_RX_DV-A/ RMII1_CRS_DV-A/ RGMII1_RX_CTL-A/ CAT1_RX_DV-A		IRQ9		DSM0_DAT2-D
D4		P800	PIO_056	CS1#-A/ DQM0-B		GTIU/ GTIOC0A/ POEGD	RXD010-B/ SMISO010-B/ SSCL010	ET0_COL/ CATLATCH0		IRQ8	ADCNV0	DSM1_CLK1-C
D5	VCC											
D6	VSS											
D7	VCL											
D8		P101	PIO_009	CS0#-A/ ALE-B	TMCI3	GTETRGC/ GTADSM1/ GTIOC12B	SCK002-B/ CTS002#/ TXDB002/ USB0_VBUS-DS/ USBHS_EXICEN	ET0_TX_CLK-B/ CAT0_TX_CLK-B/ CAT0_LINKSTA		IRQ1	ADTRG1#	DSM0_DAT0-C
D9	VSS											
D10	VCL											
D11		P105	PIO_013		TMCI2	GTIV/ GTIOC14B	TXD002-B/ SMOSI002-B/ SSDA002/ TXDA002/ SCK003-B/ CTS003#/ TXDB003/ CRX2/ USB0_VBUS/ USBHS_OVRCURB/ SSILRCK1	ET0_TXD1-B/ RMII0_TXD1-B/ CAT0_ETXD1-B/ CATLEDRUN	PIXD1	IRQ29-DS	ADST1	DSM0_DAT1-C/ PCINB0
D12	VCC											

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (6/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
D13	ETHPHYCLK	P204	PIO_020	A20-C/ CS7#-C	TMRI1	GTOVUP/ GTIOC1A/ GTIOC5A	CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001/ SSL10-B/ SCLHS1-B/ CTX0/ USB0_VBUSEN/ USBHS_VBUS-DS/ SSIBCK1	ET0_RXD0-B/ RMII0_RXD0-B/ CAT0_ERXD0-B	SD0_WP/ PIXCLK	IRQ12		DSM1_CLK1-B/ PCOUTA1
D14		PF00	PIO_048			GTCPPO14	USB0_DP			IRQ0		
D15		PF01	PIO_049			GTCPPO15	USB0_DM			IRQ1		
E1		PB02	PIO_018	D13-A		GTOUUP/ GTIOC4A	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004/ CTS009#	ET0_RXD2-A/ RGMII0_RXD2-A/ CAT0_ERXD2-A		IRQ2		
E2		PB03	PIO_019	D12-A	TMO0	GTOULO/ GTIOC4B	SCK004-A/ CTS004#/ TXDB004	ET0_RXD3-A/ RGMII0_RXD3-A/ CAT0_ERXD3-A		IRQ3		
E3		PG00	PIO_056	DQM1-A/ WR1#-C/ BC1#-C		GTCPPO0	SCK008-C/ CTS008#/ TXDB008	ET1_RX_CLK-A/ RMII1_REF50CK-A/ RGMII1_RXC-A/ CAT1_RX_CLK-A		IRQ8		DSM0_CLK2-D
E4	VSS											
E12	VSS											
E13		P206	PIO_022	A22-C/ CS5#-C	TMO3/ RTCOUT	GTOWUP/ GTIOC2A/ GTIOC6A	CTS006#/ TXD001-B/ SMOSI001-B/ SSDA001/ TXDA001/ MOSI1-B/ SCLHS2-B/ CTX1/ USB0_EXICEN/ USBHS_OVRCURA-DS/ SSITXD1	ET0_RXD2-B/ CAT0_ERXD2-B	VSYNC	IRQ2-DS	ADTRG1#	DSM1_CLK2-B/ PCOUTZ1
E14	VSS_USB											
E15	VCC_USB											
F1		PB00	PIO_016	D15-A		GTETRGA/ GTADSM0/ GTIOC14A/ POEGC	RXD004-A/ SMISO004-A/ SSCL004	ET0_RXD0-A/ RMII0_RXD0-A/ RGMII0_RXD0-A/ CAT0_ERXD0-A		IRQ12	ADST2	DSM0_CLK2-A/ PCINA1

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (7/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
F2		PB01	PIO_017	D14-A	TMCI0	GTETRGB/ GTCPPO4/ GTIOC14B/ POEGA	TXD004-A/ SMOSI004-A/ SSDA004/ TXDA004	ET0_RXD1-A/ RMII0_RXD1-A/ RGMII0_RXD1-A/ CAT0_ERXD1-A		IRQ4-DS		DSM0_DAT2-A/ PCINB1
F3		PG02	PIO_058	DQM3-A/ WR3#-C/ BC3#-C		GTIOC11A	TXD008-C/ SMOSI008-C/ SSDA008/ TXDA008	ET1_RX_ER-A/ RMII1_RX_ER-A/ CAT1_RX_ER-A		IRQ10		DSM0_CLK1-D
F4	VCL											
F12	VCL											
F13	AVSS_USBHS											
F14							USBHS_DP					
F15							USBHS_DM					
G1		PA06	PIO_014	A1-A/ DQM2-B	TMCI3	GTIOC3A/ GTIOC13A	TXD010-A/ SMOSI010-A/ SSDA010/ TXDA010/ MOSI0-B	ET1_TXD3-A/ RGMII1_TXD3-A/ CAT1_ETXD3-A		IRQ14		PCINZ1
G2	ETHPHYCLK	PA07	PIO_015	A0-A/ BC0#-A/ DQM1-B		GTIOC3B/ GTIOC13B	RXD010-A/ SMISO010-A/ SSCL010/ MISO0-B	ET1_TX_ER-A/ CATLINKACT1		IRQ7		PCINB0
G3		P706	PIO_054	CAS#-A/ CS6#-A		GTIOC13A	RXD011-B/ SMISO011-B/ SSCL011	ET1_RXD2-A/ RGMII1_RXD2-A/ CAT1_ERXD2-A	XSPI1_WP1#	IRQ14	ADCNV2	DSM0_CLK0-D
G4	VCC											
G12	AVCC_USBHS											
G13	USBHS_REF											
G14	VSS_USBHS											
G15	VCC_USBHS											
H1		PA04	PIO_012	A3-A	TMRI0	GTIOC2A/ GTIOC12A	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ SSL00-B	ET1_TXD1-A/ RMII1_TXD1-A/ RGMII1_TXD1-A/ CAT1_ETXD1-A		IRQ5-DS		PCINZ0
H2		PA05	PIO_013	A2-A		GTIOC2B/ GTIOC12B	SCK010-A/ CTS010#/ TXDB010/ RSPCK0-B	ET1_TXD2-A/ RGMII1_TXD2-A/ CAT1_ETXD2-A		IRQ5		PCINA0

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (8/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
H3		P707	PIO_055	WE#-A/ CS7#-A		GTIOC13B	TXD011-B/ SMOSI011-B/ SSDA011/ TXDA011	ET1_RXD3-A/ RGMII1_RXD3-A/ CAT1_ERXD3-A	XSPI1_RESET1#	IRQ7		DSM0_DAT0-D
H4	VSS											
H12		P207	PIO_023	A23-C/ CS4#-C	TMRI3	GTOWLO/ GTIOC2B/ GTIOC6B	RXD001-B/ SMISO001-B/ SSCL001/ MISO1-B/ SDAHS2-B/ CRX1/ USB0_ID/ USBHS_OVRCURB-DS	ET0_RXD3-B/ CAT0_ERXD3-B	PCKO	IRQ3-DS	ADTRG2#	DSM1_DAT2-B
H13	VSS											
H14	EXTAL	P306										
H15	XTAL	P307										
J1		PA02	PIO_010	A5-A		GTIW/ GTIOC1A/ GTIOC11A	TXD005-A/ SMOSI005-A/ SSDA005/ TXDA005/ SSL03-B	ET1_TX_CLK-A/ CAT1_TX_CLK-A		IRQ10	ADCNV2	DSM0_CLK1-A
J2		PA03	PIO_011	A4-A		GTIOC1B/ GTIOC11B	RXD005-A/ SMISO005-A/ SSCL005	ET1_TXD0-A/ RMII1_TXD0-A/ RGMII1_TXD0-A/ CAT1_ETXD0-A		IRQ6-DS	ADSYNC	DSM0_DAT1-A
J3		P705	PIO_053	RAS#-A/ CS5#-A		GTIOC12B	SCK011-B/ CTS011#/ TXDB011	ET1_RXD1-A/ RMII1_RXD1-A/ RGMII1_RXD1-A/ CAT1_ERXD1-A	XSPI1_RSTO1#	IRQ13	ADCNV1	DSM1_DAT2-D
J4	VCL											
J12	VCL											
J13		P305								NMI/IRQ0		
J14	VSS											
J15	VCC											
K1	ETHPHYCLK	PA00	PIO_008	A7-A	CACREF	GTIU/ GTIOC0A/ GTIOC10A	CTS010#/ CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ SSL01-B	RGMII1_TXC-A/ CATIRQ		IRQ1-DS	ADCNV0	DSM0_CLK0-A
K2		PA01	PIO_009	A6-A		GTIV/ GTIOC0B/ GTIOC10B	SCK005-A/ CTS005#/ TXDB005/ SSL02-B	ET1_TX_EN-A/ RMII1_TX_EN-A/ RGMII1_TX_CTL-A/ CAT1_TX_EN-A		IRQ11	ADCNV1	DSM0_DAT0-A
K3		P702	PIO_050	RD#-A/ DQM3-B		GTETRGA/ GTIOC11A	SCK004-B/ CTS004#/ TXDB004	ET1_CRS/ CATSYNC1	XSPI1_WP0#/ XSPI1_RESET1#/ HSYNC	IRQ10	ADST2	DSM1_CLK1-D

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (9/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
K4	VCC											
K12	VSS											
K13		P310	PIO_058		RTCIC0/ CACREF	GTETRGB/ GTCPPO1/ POEGC	CTS000#/ CTS001#/ SSL11-B/ SSITXD0	ET1_INT/ CATIRQ		IRQ18	ADTRG0 #	TAMPI0
K14	XCIN/ EXCIN	P309										
K15	XCOUT	P308										
L1	ETHPHYC LK	P700	PIO_048	SDCLK-A		GTIOC10A	TXD004-B/ SMOSI004-B/ SSDA004/ TXDA004	ET1_INT/ CATRESTO UT	XSPI1_INT0 #/ XSPI1_ECS 0#/PIXCLK	IRQ0	ADST0	DSM1_CL K0-D
L2		P701	PIO_049	CKE-A/ WR3#-B/ BC3#-B		GTIOC10B	RXD004-B/ SMISO004-B/ SSCL004	ET1_COL/ CATLATCH 1	XSPI1_RST O0#/ XSPI1_RES ET0#/ VSYNC	IRQ1	ADST1	DSM1_DA T0-D
L3		P703	PIO_051	ALE-A/ WR2#-B/ BC2#-B	CACREF	GTETRGB/ GTIOC11B	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004	ET1_LINKS TA/ CAT1_LINK STA	XSPI1_RES ET0#/PCKO	IRQ8		DSM1_DA T1-D
L4		P704	PIO_052	SDCS#-A/ CS4#-A		GTIOC12A	CTS004#/ CTS011#/ RTS011#/ SS011#/ DE011/ TXDB011	ET1_RXD0-A/ RMII1_RXD 0-A/ RGMII1_RX D0-A/ CAT1_ERX D0-A	XSPI1_INT1 #/ XSPI1_ECS 1#	IRQ12	ADCNV0	DSM1_CL K2-D
L12		P312	PIO_060	BACK#-B	RTCIC2	GTETRGD/ GTCPPO1 5/POEGA	SSL13-B/ SSILRCK0	ET1_WOL		IRQ20	ADTRG2 #	DSM0_DA T2-C/ TAMPI2
L13		P311	PIO_059	BREQ#-B	RTCIC1	GTETRGC/ GTCPPO1 4/POEGD	CTS007#/ SSL12-B/ SSIRXD0	ET0_WOL		IRQ19	ADTRG1 #	DSM0_CL K2-C/ TAMPI1
L14	VCC											
L15	VBATT/ VCC											
M1		PE07	PIO_047	A8-B/A20-D	TOC1	GTETRGD/ GTCPPO7/ GTIOC10B/ POEGD		ET1_LINKS TA/ CAT1_LINK STA/ CATRESTO UT	XSPI1_CS0 #/PIXD7	IRQ7		
M2		PE03	PIO_043	A12-B	TOC3	GTOVLO/ GTIOC8B	CTS012#/ RTS012#/ SS012#/ DE012/ TXDB012/ MISO1-A	ET1_RXD1-D/ RMII1_RXD 1-D/ CAT1_ERX D1-D	SD0_DAT7-B/ XSPI1_IO1/ PIXD3	IRQ11		
M3		PD04	PIO_036	A19-B/ D27-B		GTETRGA/ GTIOC2A/ POEGC	CTS002#/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ SSL21-A/ CRX0	ET1_RX_CL K-B/ RMII1_REF 50CK-B/ CAT1_RX_ CLK-B/ CATLEDRU N	SD0_DAT0-B/ XSPI0_IO2/ XSPI0_WP0 #/PIXD4	IRQ4	AN028	

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (10/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
M4		PD06	PIO_038	A17-B/ D25-B		GTIV/ GTIOC3A/ POEGB	RXD003-A/ SMISO003-A/ SSCL003/ SSL23-A/ CRX1	ET1_RX_ER-B/ RMII1_RX_ER-B/ CAT1_RX_ER-B/ CATLEDER R	SD0_WP/ XSPI0_DS/ PIXD6	IRQ6	AN030	
M5	VSS											
M6	VCL											
M7	VCC2											
M8	VSS											
M9	VCL											
M10		P407	PIO_055							IRQ15-DS	AN007	
M11		P404	PIO_052							IRQ12-DS	AN004	
M12	MD/FINED	P315										
M13	RES#											
M14		P001	PIO_001		TMCI0	GTCPPO0/ GTIOC10B/ GTIOC7A	SCK007-A/ CTS007#/ TXDB007/ SSIBCK0	ET0_LINKSTA/ CAT0_LINKSTA		IRQ17-DS	AN017	DSM0_DAT0-B/ PCOUTZ0
M15		P000	PIO_000		TMRI0	GTCPPO7/ GTIOC10A/ POEGB	CTS000#/ CTS007#/ RTS007#/ SS007#/ DE007/ TXDB007/ AUDIO_CLK	ET0_INT/ CATRESTOUT		IRQ16-DS	AN016	DSM0_CLK0-B
N1		PE05	PIO_045	A10-B/ A22-D		GTOWLO/ GTIOC9B	SSL12-A	ET1_RXD3-D/ CAT1_ERXD3-D/ CATLEDRUN	XSPI1_IO3/ PIXD5	IRQ5		
N2		PE04	PIO_044	A11-B/ A23-D		GTOWUP/ GTIOC9A	CTS012#/ SSL11-A	ET1_RXD2-D/ CAT1_ERXD2-D/ CATLEDSTER	XSPI1_IO2/ XSPI1_WP0#/PIXD4	IRQ12		
N3		P607	PIO_015	CS0#-B/ D16-B		GTETRGB/ GTADSM0/ GTIOC15B/ POEGA	CTS008#/ CTS009#/ RTS009#/ SS009#/ DE009/ TXDB009/ CRX2	ET1_INT/ ET_TAS_STA3/CATIRQ	XSPI0_RSTO0#	IRQ15		DSM1_DAT2-A
N4		P604	PIO_012	CS3#-C/ D19-B		GTIOC6A	TXD009-B/ SMOSI009-B/ SSDA009/ TXDA009/ SSL01-D	ET1_TXD2-B/ ET_TAS_STA0/ CAT1_ETXD2-B	XSPI0_CS1#/ XSPI0_RSTO0#	IRQ4		DSM1_CLK1-A
N5		PD07	PIO_039	A16-B/ D24-B		GTIW/ GTIOC3B/ POEGA	TXD003-A/ SMOSI003-A/ SSDA003/ TXDA003/ CTX1	ET1_LINKSTA/ CAT1_LINKSTA	SD0_CD/ XSPI0_CS0#/ XSPI0_RESET1#/PIXD7	IRQ7	AN031	

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (11/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
N6		PD05	PIO_037	A18-B/ D26-B		GTIU/ GTIOC2B/ POEGD	SCK003-A/ CTS003#/ TXDB003/ SSL22-A/ CTX0	ET1_RX_DV-B/ RMII1_CRS_DV-B/ CAT1_RX_DV-B/ CATLEDSTER	SD0_DAT1-B/ XSPI0_IO3/ PIXD5	IRQ5	AN029	
N7	VCC2											
N8	VSS											
N9	VCL											
N10		P406	PIO_054							IRQ14-DS	AN006	
N11		P405	PIO_053							IRQ13-DS	AN005	
N12		P415	PIO_063							IRQ31	AN015/ DA1	
N13		P414	PIO_062							IRQ30	AN014/ DA0	
N14		P003	PIO_003			GTCPPO2/ GTIOC11B/ GTIOC8A	RXD007-A/ SMISO007-A/ SSCL007/ SSIRXD1	ET0_MDIO-D/ CAT0_MDIO-E		IRQ19-DS	AN019	DSM0_DAT1-B/ PCOUTB0
N15		P002	PIO_002		TMCI1	GTCPPO1/ GTIOC11A/ GTIOC7B	TXD007-A/ SMOSI007-A/ SSDA007/ TXDA007/ SSIBCK1	ET0_MDC-D/ CAT0_MDC-E		IRQ18-DS	AN018	DSM0_CLK1-B/ PCOUTA0
P1	CLKOUT	PE01	PIO_041	A14-B		GTOULO/ GTIOC7B	TXD012-A/ SMOSI012-A/ SSDA012/ TXDA012/ RSPCK1-A	ET1_RX_DV-D/ RMII1_CRS_DV-D/ CAT1_RX_DV-D	SD0_DAT5-B/ XSPI1_CK/ PIXD1	IRQ9		
P2		PE02	PIO_042	A13-B	TIC3	GTOVUP/ GTIOC8A	RXD012-A/ SMISO012-A/ SSCL012/ MOSI1-A	ET1_RXD0-D/ RMII1_RXD0-D/ CAT1_ERXD0-D	SD0_DAT6-B/ XSPI1_IO0/ PIXD2	IRQ7-DS		
P3		P606	PIO_014	CS1#-C/ D17-B		GTETRGA/ GTCPPO4/ GTIOC15A/ POEGC	SCK009-B/ CTS009#/ TXDB009/ SSL03-D/ CTX2	ET1_TX_ER-B/ ET_TAS_STA2/ CATLINKACT1	XSPI0_RESET0#	IRQ14		DSM1_CLK2-A
P4		P603	PIO_011	WE#-B/ D20-B		GTIOC5B	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008/ CTS009#/ MISO0-D	ET1_TXD1-B/ RMII1_TXD1-B/ GPTP_PTPOUT3/ CAT1_ETXD1-B/ CATSYNC0	XSPI0_IO7/ PCKO	IRQ3		DSM1_DAT0-A
P5		P601	PIO_009	RAS#-B/ D22-B		GTIOC4B	RXD008-B/ SMISO008-B/ SSCL008/ RSPCK0-D	ET1_TX_EN-B/ RMII1_TX_EN-B/ GPTP_PTPOUT1/ CAT1_TX_EN-B/ CATSYNC1	XSPI0_IO5/ VSYNC	IRQ1	ADTRG1#	

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (12/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
P6		PD03	PIO_035	A20-B/ D28-B	TOC2	GTIOC1B/ POEGA	TXD002-A/ SMOSI002-A/ SSDA002/ TXDA002/ MISO2-A	ET1_RXD3-B/ CAT1_ERXD3-B/ CAT0_MDIO-D	SD0_CLK-B/ XSPI0_IO1/ PIXD3	IRQ3	AN027	
P7		PD00	PIO_032	A23-B/ D31-B		GTETRGD/ GTIOC0A/ POEGD	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS003#/ SSL20-A	ET1_RXD0-B/ RMII1_RXD0-B/ CAT1_ERXD0-B/ CATLATCH0	SD0_DAT2-B/ XSPI0_CKN#/ XSPI0_CS1#/PIXD0	IRQ0	AN024	
P8		P902	PIO_002			GTETRGC/ GTCPPO8	SCK001-C/ CTS001#/ TXDB001	ET1_MDC-B/ ET_TAS_STA2/ CATRESTOUT	XSPI0_RESET1#	IRQ10	AN034	
P9		P900	PIO_000			GTETRGA/ GTCPPO5	RXD001-C/ SMISO001-C/ SSCL001	ET1_COL/ ET_TAS_STA0/ CATSYNC1	XSPI0_INT1#/ XSPI0_ECS1#	IRQ0	AN032	
P10	AVSS0											
P11	VREFL0											
P12		P402	PIO_050							IRQ10-DS	AN002	
P13		P400	PIO_048							IRQ8-DS	AN000	
P14		P005	PIO_005			GTCPPO4/ GTIOC12B/ GTIOC9A	RXD000-B/ SMISO000-B/ SSCL000/ SSILRCK1	ET1_MDIO-D/ CATLATCH0		IRQ21-DS	ADTRG2#/AN021	DSM0_DAT2-B/ PCOUTB1
P15		P004	PIO_004			GTCPPO3/ GTIOC12A/ GTIOC8B	TXD000-B/ SMOSI000-B/ SSDA000/ TXDA000/ SSITXD1	ET1_MDC-D/ CATSYNC0		IRQ20-DS	AN020	DSM0_CLK2-B/ PCOUTA1
R1	ETHPHYCLK	PE00	PIO_040	A15-B		GTOUUP/ GTIOC7A	SCK012-A/ CTS012#/ TXDB012/ SSL10-A	ET1_RX_ER-D/ RMII1_RX_ER-D/ CAT1_RX_ER-D	SD0_DAT4-B/ XSPI1_CKN#/ XSPI1_CS1#/PIXD0	IRQ8		
R2		PE06	PIO_046	A9-B/A21-D	TIC1	GTETRGC/ GTADSM1/ GTIOC10A/ POEGB	SSL13-A	ET1_RX_CLK-D/ RMII1_REF50CK-D/ CAT1_RX_CLK-D/ CATLEDER R	XSPI1_DS/ PIXD6	IRQ6		
R3		P605	PIO_013	CS2#-C/ D18-B		GTIOC6B	RXD009-B/ SMISO009-B/ SSCL009/ SSL02-D	ET1_TXD3-B/ ET_TAS_STA1/ CAT1_ETXD3-B	XSPI0_INT0#/ XSPI0_ECS0#	IRQ13		DSM1_DAT1-A

Table 1.7 List of Pin and Pin Functions (176-Pin LFBGA) (13/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFBGA	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
R4		P602	PIO_010	CAS#-B/ D21-B		GTIOC5A	SCK008-B/ CTS008#/ TXDB008/ MOSI0-D	ET1_TXD0-B/ RMII1_TXD0-B/ GPTP_PTPOUT2/ CAT1_ETXD0-B/ CATLATCH0	XSPI0_IO6/ HSYNC	IRQ2	ADTRG2#	DSM1_CLK0-A
R5		P600	PIO_008	SDCS#-B/ D23-B		GTIOC4A	TXD008-B/ SMOSI008-B/ SSDA008/ TXDA008/ SSL00-D	ET1_TX_CLK-B/ GPTP_PTPOUT0/ CAT1_TX_CLK-B/ CATLATCH1	XSPI0_IO4/ PIXCLK	IRQ0	ADTRG0#	
R6		PD02	PIO_034	A21-B/ D29-B	TIC2	GTETRGB/ GTIOC1A/ POEGB	RXD002-A/ SMISO002-A/ SSCL002/ MOSI2-A	ET1_RXD2-B/ CAT1_ERXD2-B/ CAT0_MDC-D	SD0_CMD-B/ XSPI0_IO0/ PIXD2	IRQ2	AN026	
R7		PD01	PIO_033	A22-B/ D30-B		GTETRGC/ GTIOC0B/ POEGC	SCK002-A/ CTS002#/ TXDB002/ RSPCK2-A	ET1_RXD1-B/ RMII1_RXD1-B/ CAT1_ERXD1-B/ CATSYNC0	SD0_DAT3-B/ XSPI0_CK/ PIXD1	IRQ1	AN025	
R8		P903	PIO_003			GTETRGD/ GTCPPO9/ POEGD	CTS006#/ CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001	ET1_MDIO-B/ ET_TAS_STA3/CATIRQ	XSPI0_WP1#	IRQ11	AN035	
R9		P901	PIO_001			GTETRGB/ GTCPPO6	TXD001-C/ SMOSI001-C/ SSDA001/ TXDA001	ET1_CRS/ ET_TAS_STA1/ CATLATCH1	XSPI0_RSTO1#/ XSPI0_RESET0#	IRQ9	AN033	
R10	AVCC0											
R11	VREFH0											
R12		P403	PIO_051							IRQ11-DS	AN003	
R13		P401	PIO_049							IRQ9-DS	AN001	
R14		P007	PIO_007			GTCPPO6/ GTIOC13B/ POEGA	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000	ET1_INT/ CATIRQ		IRQ23-DS	ADTRG0#/AN023	PDMDAT0
R15		P006	PIO_006			GTCPPO5/ GTIOC13A/ GTIOC9B	SCK000-B/ CTS000#/ TXDB000	ET1_LINKSTA/ CAT1_LINKSTA		IRQ22-DS	ADTRG1#/AN022	PDMCLK0/ PCOUTZ1

1.6.4 176-Pin LFQFP

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (1/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
1		P003	PIO_003			GTCPPO2/ GTIOC11B/ GTIOC8A	RXD007-A/ SMISO007-A/ SSCL007/ SSIRXD1	ET0_MDIO-D/ CAT0_MDIO-E		IRQ19-DS	AN019	DSM0_DAT1-B/ PCOUTB0
2		P002	PIO_002		TMCI1	GTCPPO1/ GTIOC11A/ GTIOC7B	TXD007-A/ SMOSI007-A/ SSDA007/ TXDA007/ SSIBCK1	ET0_MDC-D/ CAT0_MDC-E		IRQ18-DS	AN018	DSM0_CLK1-B/ PCOUTA0
3		P001	PIO_001		TMCI0	GTCPPO0/ GTIOC10B/ GTIOC7A	SCK007-A/ CTS007#/ TXDB007/ SSIBCK0	ET0_LINKSTA/ CAT0_LINKSTA		IRQ17-DS	AN017	DSM0_DAT0-B/ PCOUTZ0
4		P000	PIO_000		TMRI0	GTCPPO7/ GTIOC10A/ POEGB	CTS000#/ CTS007#/ RTS007#/ SS007#/ DE007/ TXDB007/ AUDIO_CLK	ET0_INT/ CATRESTOUT		IRQ16-DS	AN016	DSM0_CLK0-B
5	VCC											
6	VSS											
7	VSS											
8	VCL											
9	RES#											
10	MD/FINED	P315										
11		P312	PIO_060	BACK#-B	RTCIC2	GTETRGD/ GTCPPO15/POEGA	SSL13-B/ SSILRCK0	ET1_WOL		IRQ20	ADTRG2#	DSM0_DAT2-C/ TAMPI2
12		P311	PIO_059	BREQ#-B	RTCIC1	GTETRGC/ GTCPPO14/POEGD	CTS007#/ SSL12-B/ SSIRXD0	ET0_WOL		IRQ19	ADTRG1#	DSM0_CLK2-C/ TAMPI1
13		P310	PIO_058		RTCIC0/ CACREF	GTETRGB/ GTCPPO1/ POEGC	CTS000#/ CTS001#/ SSL11-B/ SSITXD0	ET1_INT/ CATIRQ		IRQ18	ADTRG0#	TAMPI0
14	VBATT/ VCC											
15	XCIN/ EXCIN	P309										
16	XCOUT	P308										
17	VSS											
18	XTAL	P307										
19	EXTAL	P306										
20	VCC											
21		P305								NMI/IRQ0		
22	AVCC_USBHS											
23	USBHS_REF											
24	AVSS_USBHS											
25							USBHS_DM					
26							USBHS_DP					

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (2/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
27	VSS_USB HS											
28	VCC_USB HS											
29	VCC_USB											
30		PF01	PIO_049			GTCPPO1 5	USB0_DM			IRQ1		
31		PF00	PIO_048			GTCPPO1 4	USB0_DP			IRQ0		
32	VSS_USB											
33		P207	PIO_023	A23-C/ CS4#-C	TMRI3	GTOWLO/ GTIOC2B/ GTIOC6B	RXD001-B/ SMISO001-B/ SSCL001/ MISO1-B/ SDAHS2-B/ CRX1/ USB0_ID/ USBHS_OVR CURB-DS	ET0_RXD3-B/ CAT0_ERX D3-B	PCKO	IRQ3-DS	ADTRG2 #	DSM1_DA T2-B
34		P206	PIO_022	A22-C/ CS5#-C	TMO3/ RTCOUT	GTOWUP/ GTIOC2A/ GTIOC6A	CTS006#/ TXD001-B/ SMOSI001-B/ SSDA001/ TXDA001/ MOSI1-B/ SCLHS2-B/ CTX1/ USB0_EXICE N/ USBHS_OVR CURA-DS/ SSITXD1	ET0_RXD2-B/ CAT0_ERX D2-B	VSYNC	IRQ2-DS	ADTRG1 #	DSM1_CL K2-B/ PCOUTZ1
35	CLKOUT	P205	PIO_021	A21-C/ CS6#-C		GTOVLO/ GTIOC1B/ GTIOC5B	SCK001-B/ CTS001#/ TXDB001/ RSPCK1-B/ SDAHS1-B/ CRX0/ USB0_VBUS/ USBHS_VBU SEN/ SSIRXD1	ET0_RXD1-B/ RMII0_RXD 1-B/ CAT0_ERX D1-B	SD0_CD/ HSYNC	IRQ5	ADTRG0 #	DSM1_DA T1-B/ PCOUTB1
36	ETHPHYC LK	P204	PIO_020	A20-C/ CS7#-C	TMRI1	GTOVUP/ GTIOC1A/ GTIOC5A	CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001/ SSL10-B/ SCLHS1-B/ CTX0/ USB0_VBUS EN/ USBHS_VBU S-DS/ SSIBCK1	ET0_RXD0-B/ RMII0_RXD 0-B/ CAT0_ERX D0-B	SD0_WP/ PIXCLK	IRQ12		DSM1_CL K1-B/ PCOUTA1
37	VCL											
38	VSS											
39	VCC											

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (3/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
40		P203	PIO_019	CS2#-B/ BACK#-A		GTOULO/ GTIOC0B/ GTIOC4B	RXD006-A/ SMISO006-A/ SSCL006/ CTS003#/ SSL00-C/ SDA00-B/ CRX2/ USB0_OVRCURB/ USBHS_ID/ SSIBCK0	ET0_RX_CLK-B/ RMII0_REF50CK-B/ CAT0_RX_CLK-B/ CATI2CDATA-C	SD0_DAT1-C/PIXD7	IRQ3		DSM1_DAT0-B/ PDMDAT0
41		P202	PIO_018	CS3#-B/ BREQ#-A	TMO0	GTOUUP/ GTIOC0A/ GTIOC4A	TXD006-A/ SMOSI006-A/ SSDA006/ TXDA006/ RSPCK0-C/ SCL00-B/ CTX2/ USB0_OVRCURA/ USBHS_EXICEN/ AUDIO_CLK	ET0_RX_DV-B/ RMII0_CRS_DV-B/ CAT0_RX_DV-B/ CATI2CCLK-C	SD0_DAT0-C/PIXD6	IRQ15		DSM1_CLK0-B/ PDMCLK0
42	ETHPHYCLK	P304	PIO_028	ALE-C/ WAIT#-B	TMCI3	GTETRGD/ GTCPPO0/ POEGA	CTS000#/ CTS001#/ USB0_VBUSEN/ USBHS_ID	ET0_INT/ CATRESTOUT		IRQ0-DS	ADTRG0#	
43	TDI	P303	PIO_027		TMCI2	GTCPPO13	RXD000-A/ SMISO000-A/ SSCL000/ RXD001-A/ SMISO001-A/ SSCL001/ MISO1-C	ET1_CRS		IRQ1		
44	TDO	P302	PIO_026		TMRI3	GTCPPO12	TXD000-A/ SMOSI000-A/ SSDA000/ TXDA000/ TXD001-A/ SMOSI001-A/ SSDA001/ TXDA001/ MOSI1-C	ET1_COL		IRQ4		
45	TCK/ SWCLK	P301	PIO_025		TMCI3	GTCPPO11	SCK000-A/ CTS000#/ TXDB000/ SCK001-A/ CTS001#/ TXDB001/ RSPCK1-C	ET1_WOL		IRQ7		
46	TMS/ SWDIO	P300	PIO_024		TMO1	GTCPPO10	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000/ CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001/ SSL10-C	ET0_WOL		IRQ6		
47		P805	PIO_061			GTADSM1/ GTIOC15B	SCK005-B/ CTS005#/ TXDB005/ SSL22-B/ CRX0/ USB0_VBUSEN/ USBHS_VBUSEN	ET0_TXD0-C/ RMII0_TXD0-C/ CAT0_ETXD0-C	HSYNC	IRQ5	ADSYNC	DSM0_DAT0-F/ PCINB0

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (4/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
48		P804	PIO_060			GTADSM0/ GTIOC15A	CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ SSL21-B/ CTX0/ USB0_OVRCURA/ USBHS_OVRCURA	ET0_TX_EN-C/ RMII0_TX_EN-C/ CAT0_TX_EN-C	PCKO	IRQ4		DSM0_CLK0-F/ PCINA0
49		P201	PIO_017		TMCI0	GTIW/ GTIOC3B/ GTIOC14B	SCK006-A/ CTS006#/ TXDB006/ MISO0-C/ SCLHS1-A/ USB0_EXICEN/SSILRCK0	ET0_RX_ER-B/ RMII0_RX_ER-B/ CAT0_RX_ER-B	SD0_CLK-C/PIXD5	IRQ9		PCINZ0
50		P200	PIO_016		TMRI0	GTETRGA/ GTIOC3A/ GTIOC14A	CTS006#/ RTS006#/ SS006#/ DE006/ TXDB006/ MOSI0-C/ SDAHS1-A/ USB0_ID/ SSIRXD0	ET0_TX_EN-B/ RMII0_TX_EN-B/ CAT0_TX_EN-B	SD0_CMD-C/PIXD4	IRQ8	ADTRG2#	PCINZ1
51		P107	PIO_015		TMO1	GTIV/ GTIOC15B/ POEGA	TXD003-B/ SMOSI003-B/ SSDA003/ TXDA003/ SDAHS2-A/ SSITXD0	ET0_TXD3-B/ CAT0_ETXD3-B/ CATI2CDATA-B	SD0_DAT3-C/PIXD3	IRQ31-DS	ADTRG1#	PCINB1
52	CLKOUT	P106	PIO_014		TMO2/ RTCOUT	GTIU/ GTIOC15A/ POEGB	RXD003-B/ SMISO003-B/ SSCL003/ SCLHS2-A	ET0_TXD2-B/ CAT0_ETXD2-B/ CATI2CCLK-B	SD0_DAT2-C/PIXD2	IRQ30-DS	ADTRG0#	PCINA1
53		P105	PIO_013		TMCI2	GTIV/ GTIOC14B	TXD002-B/ SMOSI002-B/ SSDA002/ TXDA002/ SCK003-B/ CTS003#/ TXDB003/ CRX2/ USB0_VBUS/ USBHS_OVRCURB/ SSILRCK1	ET0_TXD1-B/ RMII0_TXD1-B/ CAT0_ETXD1-B/ CATLEDRUN	PIXD1	IRQ29-DS	ADST1	DSM0_DAT1-C/ PCINB0
54		P104	PIO_012		TMRI2	GTIW/ GTIOC14A	RXD002-B/ SMISO002-B/ SSCL002/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ CTX2/ USB0_OVRCURA-DS/ USBHS_VBUS	ET0_TXD0-B/ RMII0_TXD0-B/ CAT0_ETXD0-B/ CATLEDSTER	PIXD0	IRQ4	ADST0	DSM0_CLK1-C/ PCINA0
55	VCL											
56	VSS											
57	VCC											

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (5/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
58		P103	PIO_011		TMO3	GTADSM1/ GTIOC13B	CTS002#/ SDA00-A	ET0_CRS/ CATI2CDATA-A		IRQ3		
59		P102	PIO_010		TMCI1	GTADSM0/ GTIOC13A	SCL00-A	ET0_COL/ CATI2CCLK-A		IRQ2		
60		P101	PIO_009	CS0#-A/ ALE-B	TMCI3	GTETRGC/ GTADSM1/ GTIOC12B	SCK002-B/ CTS002#/ TXDB002/ USB0_VBUS-DS/ USBHS_EXICEN	ET0_TX_CLK-B/ CAT0_TX_CLK-B/ CAT0_LINKSTA		IRQ1	ADTRG1#	DSM0_DAT0-C
61		P100	PIO_008	CS1#-B/ WAIT#-A	TMRI3/ CACREF	GTIU/ GTADSM0/ GTIOC12A	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS005#/ USB0_OVRCURB-DS/ USBHS_VBUS	ET0_TX_ER-B/ CATLINKACT0/ CATLEDER R		IRQ0	ADTRG2#	DSM0_CLK0-C
62	VCC_DCDC											
63	VCC_DCDC											
64	VCC_DCDC											
65	VLO											
66	VLO											
67	VLO											
68	VSS_DCDC											
69	VSS_DCDC											
70		P503	PIO_035	WR3#-A/ BC3#-A/ A19-C		GTIOC3B	RXD002-C/ SMISO002-C/ SSCL002/ CRX1/ USB0_OVRCURB/ SSIRXD0	ET1_WOL/ CATLEDER R	SD0_DAT7-A	IRQ3		DSM0_DAT1-E
71		P502	PIO_034	WR2#-A/ BC2#-A/ A18-C		GTIOC3A	TXD002-C/ SMOSI002-C/ SSDA002/ TXDA002/ SSL13-C/ CTX1	ET0_WOL/ CATLEDRUN	SD0_DAT6-A	IRQ2	ADST2	DSM0_CLK1-E
72		P501	PIO_033	WR1#-A/ BC1#-A/ A17-C		GTIOC2B	SCK002-C/ CTS002#/ TXDB002/ SSL12-C/ CRX0	ET0_INT/ CATLEDSTER	SD0_DAT5-A	IRQ1	ADST1	DSM0_DAT2-E
73		P500	PIO_032	WR#-A/ WR0#-A/ A16-C		GTIOC2A	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS007#/ SSL11-C/ CTX0	ET0_LINKSTA/ CAT0_LINKSTA	SD0_DAT4-A	IRQ0	ADST0	DSM0_CLK2-E

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (6/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
74		P803	PIO_059	CS3#-A/ WR1#-B/ BC1#-B		GTIOC1B/ POEGA	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ CTX2/ USB0_ID	ET0_MDC-B/ CAT0_MDC-B		IRQ3	ADSYNC	DSM1_DAT0-C
75		P802	PIO_058	CS2#-A/ WR#-B/ WR0#-B		GTIW/ GTIOC1A/ POEGB	SCK010-B/ CTS010#/ TXDB010/ CRX2/ USB0_EXICEN	ET0_MDIO-B/ CAT0_MDIO-B		IRQ2	ADCNV2	DSM1_CLK0-C
76	VCL											
77	VSS											
78	VCC											
79	CLKOUT	P801	PIO_057	EBCLK-A		GTIV/ GTIOC0B/ POEGC	TXD010-B/ SMOSI010-B/ SSDA010/ TXDA010	ET0_CRS/ CATSYNC0		IRQ9	ADCNV1	DSM1_DAT1-C
80		P800	PIO_056	CS1#-A/ DQM0-B		GTIU/ GTIOC0A/ POEGD	RXD010-B/ SMISO010-B/ SSCL010	ET0_COL/ CATLATCH0		IRQ8	ADCNV0	DSM1_CLK1-C
81	ETHPHYCLK	PC07	PIO_031	D0-A	TMO2/ TOC0/ CACREF	GTETRGD/ GTADSM1/ GTIOC15B/ POEGA	TXD008-A/ SMOSI008-A/ SSDA008/ TXDA008/ MISO0-A/ SSITXD0	CATRESTOUT	SD0_CD	IRQ14		DSM1_DAT2-C/ PDMDAT0
82		PC06	PIO_030	D1-A	TMCI2/ TIC0	GTETRGC/ GTCPPO7/ GTIOC15A/ POEGB	RXD008-A/ SMISO008-A/ SSCL008/ MOSI0-A/ SSILRCK0	ET0_TX_ER-A/ CATLINKACT0	SD0_WP	IRQ13		DSM1_CLK2-C/ PDMCLK0
83		PC05	PIO_029	D2-A	TMRI2	GTOWLO/ GTIOC9B	SCK008-A/ CTS008#/ TXDB008/ RSPCK0-A/ SSIBCK0	ET0_TX_EN-A/ RMII0_TX_EN-A/ CAT0_TX_EN-A	SD0_DAT1-A	IRQ5		PCOUTZ1
84		PC04	PIO_028	D3-A	TMCI1	GTOWUP/ GTIOC9A	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008/ CTS011#/ SSL00-A/ AUDIO_CLK	ET0_TXD3-A/ CAT0_ETXD3-A	SD0_DAT0-A	IRQ12		PCOUTB1
85		PC03	PIO_027	D4-A		GTOVLO/ GTIOC8B	TXD011-A/ SMOSI011-A/ SSDA011/ TXDA011/ SDAHS1-C	ET0_TXD2-A/ CAT0_ETXD2-A	SD0_CLK-A	IRQ11		PCOUTA1
86		PC02	PIO_026	D5-A		GTOVUP/ GTIOC8A	RXD011-A/ SMISO011-A/ SSCL011/ SSL03-A/ SCLHS1-C	ET0_TXD1-A/ RMII0_TXD1-A/ CAT0_ETXD1-A	SD0_CMD-A	IRQ10		PCOUTZ0
87		PC01	PIO_025	D6-A		GTOULO/ GTIOC7B	SCK011-A/ CTS011#/ TXDB011/ SSL02-A/ SDA00-C	ET0_TXD0-A/ RMII0_TXD0-A/ CAT0_ETXD0-A	SD0_DAT3-A	IRQ12		PCOUTB0

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (7/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
88		PC00	PIO_024	D7-A		GTOUUP/ GTIOC7A	CTS011#/ RTS011#/ SS011#/ DE011/ TXDB011/ SSL01-A/ SCL00-C	ET0_TX_CLK-A/ CAT0_TX_CLK-A	SD0_DAT2-A	IRQ14		PCOUTA0
89		PB07	PIO_023	D8-A		GTOWLO/ GTIOC6B	TXD009-A/ SMOSI009-A/ SSDA009/ TXDA009	ET0_LINKSTA/ CAT0_LINKSTA		IRQ15		
90		PB06	PIO_022	D9-A		GTOWUP/ GTIOC6A	RXD009-A/ SMISO009-A/ SSCL009	ET0_RX_ER-A/ RMII0_RX_ER-A/ CAT0_RX_ER-A		IRQ6		
91		PB05	PIO_021	D10-A	TMRI1	GTOVLO/ GTIOC5B	SCK009-A/ CTS009#/ TXDB009	ET0_RX_DV-A/ RMII0_CRS_DV-A/ CAT0_RX_DV-A		IRQ13		
92		PB04	PIO_020	D11-A		GTOVUP/ GTIOC5A	CTS004#/ CTS009#/ RTS009#/ SS009#/ DE009/ TXDB009	ET0_RX_CLK-A/ RMII0_REF50CK-A/ CAT0_RX_CLK-A		IRQ4		
93	VCC											
94	VSS											
95	VCL											
96		PB03	PIO_019	D12-A	TMO0	GTOULO/ GTIOC4B	SCK004-A/ CTS004#/ TXDB004	ET0_RXD3-A/ CAT0_ERXD3-A		IRQ3		
97		PB02	PIO_018	D13-A		GTOUUP/ GTIOC4A	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004/ CTS009#	ET0_RXD2-A/ CAT0_ERXD2-A		IRQ2		
98		PB01	PIO_017	D14-A	TMCI0	GTETRGB/ GTCPPO4/ GTIOC14B/ POEGA	TXD004-A/ SMOSI004-A/ SSDA004/ TXDA004	ET0_RXD1-A/ RMII0_RXD1-A/ CAT0_ERXD1-A		IRQ4-DS		DSM0_DAT2-A/ PCINB1
99		PB00	PIO_016	D15-A		GTETRGA/ GTADSM0/ GTIOC14A/ POEGC	RXD004-A/ SMISO004-A/ SSCL004	ET0_RXD0-A/ RMII0_RXD0-A/ CAT0_ERXD0-A		IRQ12	ADST2	DSM0_CLK2-A/ PCINA1
100		PG02	PIO_058	DQM3-A/ WR3#-C/ BC3#-C		GTIOC11A	TXD008-C/ SMOSI008-C/ SSDA008/ TXDA008	ET1_RX_ER-A/ RMII1_RX_ER-A/ CAT1_RX_ER-A		IRQ10		DSM0_CLK1-D
101		PG01	PIO_057	DQM0-A/ WR#-C/ WR0#-C		GTCPPO1	RXD008-C/ SMISO008-C/ SSCL008	ET1_RX_DV-A/ RMII1_CRS_DV-A/ CAT1_RX_DV-A		IRQ9		DSM0_DAT2-D

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (8/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
102		PG00	PIO_056	DQM1-A/ WR1#-C/ BC1#-C		GTCPPO0	SCK008-C/ CTS008#/ TXDB008	ET1_RX_CLK-A/ RMII1_REF50CK-A/ CAT1_RX_CLK-A		IRQ8		DSM0_CLK2-D
103	ETHPHYCLK	PA07	PIO_015	A0-A/ BC0#-A/ DQM1-B		GTIOC3B/ GTIOC13B	RXD010-A/ SMISO010-A/ SSCL010/ MISO0-B	ET1_TX_ER-A/ CATLINKACT1		IRQ7		PCINB0
104		PA06	PIO_014	A1-A/ DQM2-B	TMCI3	GTIOC3A/ GTIOC13A	TXD010-A/ SMOSI010-A/ SSDA010/ TXDA010/ MOSI0-B	ET1_TXD3-A/ CAT1_ETXD3-A		IRQ14		PCINZ1
105		PA05	PIO_013	A2-A		GTIOC2B/ GTIOC12B	SCK010-A/ CTS010#/ TXDB010/ RSPCK0-B	ET1_TXD2-A/ CAT1_ETXD2-A		IRQ5		PCINA0
106		PA04	PIO_012	A3-A	TMRI0	GTIOC2A/ GTIOC12A	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ SSL00-B	ET1_TXD1-A/ RMII1_TXD1-A/ CAT1_ETXD1-A		IRQ5-DS		PCINZ0
107	VCC											
108	VSS											
109	VCL											
110		PA03	PIO_011	A4-A		GTIOC1B/ GTIOC11B	RXD005-A/ SMISO005-A/ SSCL005	ET1_TXD0-A/ RMII1_TXD0-A/ CAT1_ETXD0-A		IRQ6-DS	ADSYNC	DSM0_DAT1-A
111		PA02	PIO_010	A5-A		GTIW/ GTIOC1A/ GTIOC11A	TXD005-A/ SMOSI005-A/ SSDA005/ TXDA005/ SSL03-B	ET1_TX_CLK-A/ CAT1_TX_CLK-A		IRQ10	ADCNV2	DSM0_CLK1-A
112		PA01	PIO_009	A6-A		GTIV/ GTIOC0B/ GTIOC10B	SCK005-A/ CTS005#/ TXDB005/ SSL02-B	ET1_TX_EN-A/ RMII1_TX_EN-A/ CAT1_TX_EN-A		IRQ11	ADCNV1	DSM0_DAT0-A
113	ETHPHYCLK	PA00	PIO_008	A7-A	CACREF	GTIU/ GTIOC0A/ GTIOC10A	CTS010#/ CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ SSL01-B	CATIRQ		IRQ1-DS	ADCNV0	DSM0_CLK0-A
114		P707	PIO_055	WE#-A/ CS7#-A		GTIOC13B	TXD011-B/ SMOSI011-B/ SSDA011/ TXDA011	ET1_RXD3-A/ CAT1_ERXD3-A	XSPI1_RESET1#	IRQ7		DSM0_DAT0-D
115		P706	PIO_054	CAS#-A/ CS6#-A		GTIOC13A	RXD011-B/ SMISO011-B/ SSCL011	ET1_RXD2-A/ CAT1_ERXD2-A	XSPI1_WP1#	IRQ14	ADCNV2	DSM0_CLK0-D
116		P705	PIO_053	RAS#-A/ CS5#-A		GTIOC12B	SCK011-B/ CTS011#/ TXDB011	ET1_RXD1-A/ RMII1_RXD1-A/ CAT1_ERXD1-A	XSPI1_RSTO1#	IRQ13	ADCNV1	DSM1_DAT2-D

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (9/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
117		P704	PIO_052	SDCS#-A/ CS4#-A		GTIOC12A	CTS004#/ CTS011#/ RTS011#/ SS011#/ DE011/ TXDB011	ET1_RXD0-A/ RMII1_RXD0-A/ CAT1_ERXD0-A	XSPI1_INT1#/ XSPI1_ECS1#	IRQ12	ADCNV0	DSM1_CLK2-D
118		P703	PIO_051	ALE-A/ WR2#-B/ BC2#-B	CACREF	GTETRGB/ GTIOC11B	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004	ET1_LINKSTA/ CAT1_LINKSTA	XSPI1_RESET0#/PCKO	IRQ8		DSM1_DAT1-D
119		P702	PIO_050	RD#-A/ DQM3-B		GTETRGA/ GTIOC11A	SCK004-B/ CTS004#/ TXDB004	ET1_CRS/ CATSYNC1	XSPI1_WP0#/ XSPI1_RESET1#/ HSYNC	IRQ10	ADST2	DSM1_CLK1-D
120		P701	PIO_049	CKE-A/ WR3#-B/ BC3#-B		GTIOC10B	RXD004-B/ SMISO004-B/ SSCL004	ET1_COL/ CATLATCH1	XSPI1_RSTO0#/ XSPI1_RESET0#/ VSYNC	IRQ1	ADST1	DSM1_DAT0-D
121	ETHPHYCLK	P700	PIO_048	SDCLK-A		GTIOC10A	TXD004-B/ SMOSI004-B/ SSDA004/ TXDA004	ET1_INT/ CATRESTOUT	XSPI1_INT0#/ XSPI1_ECS0#/PIXCLK	IRQ0	ADST0	DSM1_CLK0-D
122	VCC											
123	VSS											
124	VCL											
125		PE07	PIO_047	A8-B/A20-D	TOC1	GTETRGD/ GTCPPO7/ GTIOC10B/ POEGD		ET1_LINKSTA/ CAT1_LINKSTA/ CATRESTOUT	XSPI1_CS0#/PIXD7	IRQ7		
126		PE06	PIO_046	A9-B/A21-D	TIC1	GTETRGC/ GTADSM1/ GTIOC10A/ POEGB	SSL13-A	ET1_RX_CLK-D/ RMII1_REF50CK-D/ CAT1_RX_CLK-D/ CATLEDER R	XSPI1_DS/ PIXD6	IRQ6		
127		PE05	PIO_045	A10-B/ A22-D		GTOWLO/ GTIOC9B	SSL12-A	ET1_RXD3-D/ CAT1_ERXD3-D/ CATLEDRUN	XSPI1_IO3/ PIXD5	IRQ5		
128		PE04	PIO_044	A11-B/ A23-D		GTOWUP/ GTIOC9A	CTS012#/ SSL11-A	ET1_RXD2-D/ CAT1_ERXD2-D/ CATLEDSTER	XSPI1_IO2/ XSPI1_WP0#/PIXD4	IRQ12		
129		PE03	PIO_043	A12-B	TOC3	GTOVLO/ GTIOC8B	CTS012#/ RTS012#/ SS012#/ DE012/ TXDB012/ MISO1-A	ET1_RXD1-D/ RMII1_RXD1-D/ CAT1_ERXD1-D	SD0_DAT7-B/ XSPI1_IO1/ PIXD3	IRQ11		
130		PE02	PIO_042	A13-B	TIC3	GTOVUP/ GTIOC8A	RXD012-A/ SMISO012-A/ SSCL012/ MOSI1-A	ET1_RXD0-D/ RMII1_RXD0-D/ CAT1_ERXD0-D	SD0_DAT6-B/ XSPI1_IO0/ PIXD2	IRQ7-DS		

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (10/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
131	CLKOUT	PE01	PIO_041	A14-B		GTOULO/ GTIOC7B	TXD012-A/ SMOSI012-A/ SSDA012/ TXDA012/ RSPCK1-A	ET1_RX_DV-D/ RMII1_CRS_DV-D/ CAT1_RX_DV-D	SD0_DAT5-B/ XSPI1_CK/ PIXD1	IRQ9		
132	ETHPHYCLK	PE00	PIO_040	A15-B		GTOUUP/ GTIOC7A	SCK012-A/ CTS012#/ TXDB012/ SSL10-A	ET1_RX_ER-D/ RMII1_RX_ER-D/ CAT1_RX_ER-D	SD0_DAT4-B/ XSPI1_CKN#/ XSPI1_CS1#/PIXD0	IRQ8		
133		P607	PIO_015	CS0#-B/ D16-B		GTETRGB/ GTADSM0/ GTIOC15B/ POEGA	CTS008#/ CTS009#/ RTS009#/ SS009#/ DE009/ TXDB009/ CRX2	ET1_INT/ ET_TAS_STA3/CATIRQ	XSPI0_RSTO0#	IRQ15		DSM1_DAT2-A
134		P606	PIO_014	CS1#-C/ D17-B		GTETRGA/ GTCPPO4/ GTIOC15A/ POEGC	SCK009-B/ CTS009#/ TXDB009/ SSL03-D/ CTX2	ET1_TX_ER-B/ ET_TAS_STA2/ CATLINKACT1	XSPI0_RESET0#	IRQ14		DSM1_CLK2-A
135		P605	PIO_013	CS2#-C/ D18-B		GTIOC6B	RXD009-B/ SMISO009-B/ SSCL009/ SSL02-D	ET1_TXD3-B/ ET_TAS_STA1/ CAT1_ETXD3-B	XSPI0_INT0#/ XSPI0_ECS0#	IRQ13		DSM1_DAT1-A
136		P604	PIO_012	CS3#-C/ D19-B		GTIOC6A	TXD009-B/ SMOSI009-B/ SSDA009/ TXDA009/ SSL01-D	ET1_TXD2-B/ ET_TAS_STA0/ CAT1_ETXD2-B	XSPI0_CS1#/ XSPI0_RSTO0#	IRQ4		DSM1_CLK1-A
137		P603	PIO_011	WE#-B/ D20-B		GTIOC5B	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008/ CTS009#/ MISO0-D	ET1_TXD1-B/ RMII1_TXD1-B/ GPTP_PTPOUT3/ CAT1_ETXD1-B/ CATSYNC0	XSPI0_IO7/ PCKO	IRQ3		DSM1_DAT0-A
138		P602	PIO_010	CAS#-B/ D21-B		GTIOC5A	SCK008-B/ CTS008#/ TXDB008/ MOSI0-D	ET1_TXD0-B/ RMII1_TXD0-B/ GPTP_PTPOUT2/ CAT1_ETXD0-B/ CATLATCH0	XSPI0_IO6/ HSYNC	IRQ2	ADTRG2#	DSM1_CLK0-A
139		P601	PIO_009	RAS#-B/ D22-B		GTIOC4B	RXD008-B/ SMISO008-B/ SSCL008/ RSPCK0-D	ET1_TX_EN-B/ RMII1_TX_EN-B/ GPTP_PTPOUT1/ CAT1_TX_EN-B/ CATSYNC1	XSPI0_IO5/ VSYNC	IRQ1	ADTRG1#	

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (11/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
140		P600	PIO_008	SDCS#-B/ D23-B		GTIOC4A	TXD008-B/ SMOSI008-B/ SSDA008/ TXDA008/ SSL00-D	ET1_TX_CLK-B/ GPTP_PTPOUT0/ CAT1_TX_CLK-B/ CATLATCH1	XSPI0_IO4/ PIXCLK	IRQ0	ADTRG0#	
141	VCC2											
142	VSS											
143	VCL											
144		PD07	PIO_039	A16-B/ D24-B		GTIW/ GTIOC3B/ POEGA	TXD003-A/ SMOSI003-A/ SSDA003/ TXDA003/ CTX1	ET1_LINKSTA/ CAT1_LINKSTA	SD0_CD/ XSPI0_CS0#/ XSPI0_RESET1#/PIXD7	IRQ7	AN031	
145		PD06	PIO_038	A17-B/ D25-B		GTIV/ GTIOC3A/ POEGB	RXD003-A/ SMISO003-A/ SSCL003/ SSL23-A/ CRX1	ET1_RX_ER-B/ RMII1_RX_ER-B/ CAT1_RX_ER-B/ CATLEDER R	SD0_WP/ XSPI0_DS/ PIXD6	IRQ6	AN030	
146		PD05	PIO_037	A18-B/ D26-B		GTIU/ GTIOC2B/ POEGD	SCK003-A/ CTS003#/ TXDB003/ SSL22-A/ CTX0	ET1_RX_DV-B/ RMII1_CRS_DV-B/ CAT1_RX_DV-B/ CATLEDSTER	SD0_DAT1-B/ XSPI0_IO3/ PIXD5	IRQ5	AN029	
147		PD04	PIO_036	A19-B/ D27-B		GTETRGA/ GTIOC2A/ POEGC	CTS002#/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ SSL21-A/ CRX0	ET1_RX_CLK-B/ RMII1_REF50CK-B/ CAT1_RX_CLK-B/ CATLEDRUN	SD0_DAT0-B/ XSPI0_IO2/ XSPI0_WP0#/PIXD4	IRQ4	AN028	
148		PD03	PIO_035	A20-B/ D28-B	TOC2	GTIOC1B/ POEGA	TXD002-A/ SMOSI002-A/ SSDA002/ TXDA002/ MISO2-A	ET1_RXD3-B/ CAT1_ERXD3-B/ CAT0_MDIO-D	SD0_CLK-B/ XSPI0_IO1/ PIXD3	IRQ3	AN027	
149		PD02	PIO_034	A21-B/ D29-B	TIC2	GTETRGB/ GTIOC1A/ POEGB	RXD002-A/ SMISO002-A/ SSCL002/ MOSI2-A	ET1_RXD2-B/ CAT1_ERXD2-B/ CAT0_MDC-D	SD0_CMD-B/ XSPI0_IO0/ PIXD2	IRQ2	AN026	
150		PD01	PIO_033	A22-B/ D30-B		GTETRGC/ GTIOC0B/ POEGC	SCK002-A/ CTS002#/ TXDB002/ RSPCK2-A	ET1_RXD1-B/ RMII1_RXD1-B/ CAT1_ERXD1-B/ CATSYNC0	SD0_DAT3-B/ XSPI0_CK/ PIXD1	IRQ1	AN025	
151		PD00	PIO_032	A23-B/ D31-B		GTETRGD/ GTIOC0A/ POEGD	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS003#/ SSL20-A	ET1_RXD0-B/ RMII1_RXD0-B/ CAT1_ERXD0-B/ CATLATCH0	SD0_DAT2-B/ XSPI0_CKN#/ XSPI0_CS1#/PIXD0	IRQ0	AN024	
152	VCC2											

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (12/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
153	VSS											
154	VCL											
155		P903	PIO_003			GTETRGD/ GTCPPO9/ POEGD	CTS006#/ CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001	ET1_MDIO-B/ ET_TAS_STA3/CATIRQ	XSPI0_WP1#	IRQ11	AN035	
156		P902	PIO_002			GTETRGC/ GTCPPO8	SCK001-C/ CTS001#/ TXDB001	ET1_MDC-B/ ET_TAS_STA2/ CATRESTOUT	XSPI0_RESET1#	IRQ10	AN034	
157		P901	PIO_001			GTETRGB/ GTCPPO6	TXD001-C/ SMOSI001-C/ SSDA001/ TXDA001	ET1_CRS/ ET_TAS_STA1/ CATLATCH1	XSPI0_RSTO1#/ XSPI0_RESET0#	IRQ9	AN033	
158		P900	PIO_000			GTETRGA/ GTCPPO5	RXD001-C/ SMISO001-C/ SSCL001	ET1_COL/ ET_TAS_STA0/ CATSYNC1	XSPI0_INT1#/ XSPI0_ECS1#	IRQ0	AN032	
159	AVCC0											
160	AVSS0											
161	VREFL0											
162	VREFH0											
163		P407	PIO_055							IRQ15-DS	AN007	
164		P406	PIO_054							IRQ14-DS	AN006	
165		P405	PIO_053							IRQ13-DS	AN005	
166		P404	PIO_052							IRQ12-DS	AN004	
167		P403	PIO_051							IRQ11-DS	AN003	
168		P402	PIO_050							IRQ10-DS	AN002	
169		P401	PIO_049							IRQ9-DS	AN001	
170		P400	PIO_048							IRQ8-DS	AN000	
171		P415	PIO_063							IRQ31	AN015/ DA1	
172		P414	PIO_062							IRQ30	AN014/ DA0	
173		P007	PIO_007			GTCPPO6/ GTIOC13B/ POEGA	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000	ET1_INT/ CATIRQ		IRQ23-DS	ADTRG0#/AN023	PDMDAT0
174		P006	PIO_006			GTCPPO5/ GTIOC13A/ GTIOC9B	SCK000-B/ CTS000#/ TXDB000	ET1_LINKSTA/ CAT1_LINKSTA		IRQ22-DS	ADTRG1#/AN022	PDMCLK0/ PCOUTZ1
175		P005	PIO_005			GTCPPO4/ GTIOC12B/ GTIOC9A	RXD000-B/ SMISO000-B/ SSCL000/ SSILRCK1	ET1_MDIO-D/ CATLATCH0		IRQ21-DS	ADTRG2#/AN021	DSM0_DAT2-B/ PCOUTB1

Table 1.8 List of Pin and Pin Functions (176-Pin LFQFP) (13/13)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
176-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
176		P004	PIO_004			GTCPPO3/ GTIOC12A/ GTIOC8B	TXD000-B/ SMOSI000-B/ SSDA000/ TXDA000/ SSITXD1	ET1_MDC-D/ CATSYNC0		IRQ20-DS	AN020	DSM0_CLK2-B/ PCOUTA1

1.6.5 144-Pin LFQFP

Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (1/10)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
1		P003	PIO_003			GTCPPO2/ GTIOC11B/ GTIOC8A	RXD007-A/ SMISO007-A/ SSCL007/ SSIRXD1	ET0_MDIO-D/ CAT0_MDIO-E		IRQ19-DS	AN019	DSM0_DAT1-B/ PCOUTB0
2		P002	PIO_002		TMCI1	GTCPPO1/ GTIOC11A/ GTIOC7B	TXD007-A/ SMOSI007-A/ SSDA007/ TXDA007/ SSIBCK1	ET0_MDC-D/ CAT0_MDC-E		IRQ18-DS	AN018	DSM0_CLK1-B/ PCOUTA0
3		P001	PIO_001		TMCI0	GTCPPO0/ GTIOC10B/ GTIOC7A	SCK007-A/ CTS007#/ TXDB007/ SSIBCK0	ET0_LINKSTA/ CAT0_LINKSTA		IRQ17-DS	AN017	DSM0_DAT0-B/ PCOUTZ0
4		P000	PIO_000		TMRI0	GTCPPO7/ GTIOC10A/ POEGB	CTS000#/ CTS007#/ RTS007#/ SS007#/ DE007/ TXDB007/ AUDIO_CLK	ET0_INT/ CATRESTOUT		IRQ16-DS	AN016	DSM0_CLK0-B
5	VCC											
6	VSS											
7	VCL											
8	RES#											
9	MD/FINED	P315										
10		P312	PIO_060	BACK#-B	RTCIC2	GTETRGD/ GTCPPO15/POEGA	SSL13-B/ SSILRCK0	ET1_WOL		IRQ20	ADTRG2#	DSM0_DAT2-C/ TAMPI2
11		P311	PIO_059	BREQ#-B	RTCIC1	GTETRGC/ GTCPPO14/POEGD	CTS007#/ SSL12-B/ SSIRXD0	ET0_WOL		IRQ19	ADTRG1#	DSM0_CLK2-C/ TAMPI1
12		P310	PIO_058		RTCIC0/ CACREF	GTETRGB/ GTCPPO1/ POEGC	CTS000#/ CTS001#/ SSL11-B/ SSITXD0	ET1_INT/ CATIRQ		IRQ18	ADTRG0#	TAMPI0
13	VBATT/ VCC											
14	XCIN/ EXCIN	P309										
15	XCOUT	P308										
16	VSS											
17	XTAL	P307										
18	EXTAL	P306										
19	VCC											
20		P305								NMI/IRQ0		
21	VCC_USB											
22		PF01	PIO_049			GTCPPO15	USB0_DM			IRQ1		
23		PF00	PIO_048			GTCPPO14	USB0_DP			IRQ0		
24	VSS_USB											

Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (2/10)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
25		P207	PIO_023	A23-C/ CS4#-C	TMRI3	GTOWLO/ GTIOC2B/ GTIOC6B	RXD001-B/ SMISO001-B/ SSCL001/ MISO1-B/ SDAHS2-B/ CRX1/ USB0_ID	ET0_RXD3-B/ CAT0_ERXD3-B	PCKO	IRQ3-DS	ADTRG2#	DSM1_DAT2-B
26		P206	PIO_022	A22-C/ CS5#-C	TMO3/ RTCOUT	GTOWUP/ GTIOC2A/ GTIOC6A	CTS006#/ TXD001-B/ SMOSI001-B/ SSDA001/ TXDA001/ MOSI1-B/ SCLHS2-B/ CTX1/ USB0_EXICEN/SSITXD1	ET0_RXD2-B/ CAT0_ERXD2-B	VSYNC	IRQ2-DS	ADTRG1#	DSM1_CLK2-B/ PCOUTZ1
27	CLKOUT	P205	PIO_021	A21-C/ CS6#-C		GTOVLO/ GTIOC1B/ GTIOC5B	SCK001-B/ CTS001#/ TXDB001/ RSPCK1-B/ SDAHS1-B/ CRX0/ USB0_VBUS/ SSIRXD1	ET0_RXD1-B/ RMII0_RXD1-B/ CAT0_ERXD1-B	SD0_CD/ HSYNC	IRQ5	ADTRG0#	DSM1_DAT1-B/ PCOUTB1
28	ETHPHYCLK	P204	PIO_020	A20-C/ CS7#-C	TMRI1	GTOVUP/ GTIOC1A/ GTIOC5A	CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001/ SSL10-B/ SCLHS1-B/ CTX0/ USB0_VBUSEN/SSIBCK1	ET0_RXD0-B/ RMII0_RXD0-B/ CAT0_ERXD0-B	SD0_WP/ PIXCLK	IRQ12		DSM1_CLK1-B/ PCOUTA1
29	VCL											
30	VSS											
31	VCC											
32		P203	PIO_019	CS2#-B/ BACK#-A		GTOULO/ GTIOC0B/ GTIOC4B	RXD006-A/ SMISO006-A/ SSCL006/ CTS003#/ SSL00-C/ SDA00-B/ CRX2/ USB0_OVRCURB/ SSIBCK0	ET0_RX_CLK-B/ RMII0_REF50CK-B/ CAT0_RX_CLK-B/ CATI2CDATA-C	SD0_DAT1-C/PIXD7	IRQ3		DSM1_DAT0-B/ PDMDAT0
33		P202	PIO_018	CS3#-B/ BREQ#-A	TMO0	GTOUUP/ GTIOC0A/ GTIOC4A	TXD006-A/ SMOSI006-A/ SSDA006/ TXDA006/ RSPCK0-C/ SCL00-B/ CTX2/ USB0_OVRCURA/ AUDIO_CLK	ET0_RX_DV-B/ RMII0_CRS_DV-B/ CAT0_RX_DV-B/ CATI2CCLK-C	SD0_DAT0-C/PIXD6	IRQ15		DSM1_CLK0-B/ PDMCLK0
34	ETHPHYCLK	P304	PIO_028	ALE-C/ WAIT#-B	TMCI3	GTETRGD/ GTCPPO0/ POEGA	CTS000#/ CTS001#/ USB0_VBUSEN	ET0_INT/ CATRESTOUT		IRQ0-DS	ADTRG0#	
35	TDI	P303	PIO_027		TMCI2	GTCPPO13	RXD000-A/ SMISO000-A/ SSCL000/ RXD001-A/ SMISO001-A/ SSCL001/ MISO1-C	ET1_CRS		IRQ1		

Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (3/10)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
36	TDO	P302	PIO_026		TMRI3	GTCPPO12	TXD000-A/ SMOSI000-A/ SSDA000/ TXDA000/ TXD001-A/ SMOSI001-A/ SSDA001/ TXDA001/ MOSI1-C	ET1_COL		IRQ4		
37	TCK/ SWCLK	P301	PIO_025		TMCI3	GTCPPO11	SCK000-A/ CTS000#/ TXDB000/ SCK001-A/ CTS001#/ TXDB001/ RSPCK1-C	ET1_WOL		IRQ7		
38	TMS/ SWDIO	P300	PIO_024		TMO1	GTCPPO10	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000/ CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001/ SSL10-C	ET0_WOL		IRQ6		
39		P201	PIO_017		TMCI0	GTIW/ GTIOC3B/ GTIOC14B	SCK006-A/ CTS006#/ TXDB006/ MISO0-C/ SCLHS1-A/ USB0_EXICEN/SSILRCK0	ET0_RX_ER-B/ RMII0_RX_ER-B/ CAT0_RX_ER-B	SD0_CLK-C/PIXD5	IRQ9		PCINZ0
40		P200	PIO_016		TMRI0	GTETRGA/ GTIOC3A/ GTIOC14A	CTS006#/ RTS006#/ SS006#/ DE006/ TXDB006/ MOSI0-C/ SDAHS1-A/ USB0_ID/ SSIRXD0	ET0_TX_EN-B/ RMII0_TX_EN-B/ CAT0_TX_EN-B	SD0_CMD-C/PIXD4	IRQ8	ADTRG2#	PCINZ1
41		P107	PIO_015		TMO1	GTIV/ GTIOC15B/ POEGA	TXD003-B/ SMOSI003-B/ SSDA003/ TXDA003/ SDAHS2-A/ SSITXD0	ET0_TXD3-B/ CAT0_ETXD3-B/ CATI2CDATA-B	SD0_DAT3-C/PIXD3	IRQ31-DS	ADTRG1#	PCINB1
42	CLKOUT	P106	PIO_014		TMO2/ RTCOUT	GTIU/ GTIOC15A/ POEGB	RXD003-B/ SMISO003-B/ SSCL003/ SCLHS2-A	ET0_TXD2-B/ CAT0_ETXD2-B/ CATI2CCLK-B	SD0_DAT2-C/PIXD2	IRQ30-DS	ADTRG0#	PCINA1
43		P105	PIO_013		TMCI2	GTIV/ GTIOC14B	TXD002-B/ SMOSI002-B/ SSDA002/ TXDA002/ SCK003-B/ CTS003#/ TXDB003/ CRX2/ USB0_VBUS/ SSILRCK1	ET0_TXD1-B/ RMII0_TXD1-B/ CAT0_ETXD1-B/ CATLEDRUN	PIXD1	IRQ29-DS	ADST1	DSM0_DAT1-C/ PCINB0

Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (4/10)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
44		P104	PIO_012		TMRI2	GTIW/ GTIOC14A	RXD002-B/ SMISO002-B/ SSCL002/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ CTX2/ USB0_OVRC URA-DS	ET0_TXD0-B/ RMII0_TXD 0-B/ CAT0_ETX D0-B/ CATLEDST ER	PIXD0	IRQ4	ADST0	DSM0_CL K1-C/ PCINA0
45	VCL											
46	VSS											
47	VCC											
48		P103	PIO_011		TMO3	GTADSM1/ GTIOC13B	CTS002#/ SDA00-A	ET0_CRS/ CATI2CDAT A-A		IRQ3		
49		P102	PIO_010		TMCI1	GTADSM0/ GTIOC13A	SCL00-A	ET0_COL/ CATI2CCLK -A		IRQ2		
50		P101	PIO_009	CS0#-A/ ALE-B	TMCI3	GTETRGC/ GTADSM1/ GTIOC12B	SCK002-B/ CTS002#/ TXDB002/ USB0_VBUS-DS	ET0_TX_CL K-B/ CAT0_TX_C LK-B/ CAT0_LINK STA		IRQ1	ADTRG1 #	DSM0_DA T0-C
51		P100	PIO_008	CS1#-B/ WAIT#-A	TMRI3/ CACREF	GTIU/ GTADSM0/ GTIOC12A	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS005#/ USB0_OVRC URB-DS	ET0_TX_ER -B/ CATLINKAC T0/ CATLEDER R		IRQ0	ADTRG2 #	DSM0_CL K0-C
52	VCC_DCD C											
53	VCC_DCD C											
54	VLO											
55	VLO											
56	VSS_DCD C											
57	VSS_DCD C											
58		P803	PIO_059	CS3#-A/ WR1#-B/ BC1#-B		GTIOC1B/ POEGA	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ CTX2/ USB0_ID	ET0_MDC-B/ CAT0_MDC-B		IRQ3	ADSYNC	DSM1_DA T0-C
59		P802	PIO_058	CS2#-A/ WR#-B/ WR0#-B		GTIW/ GTIOC1A/ POEGB	SCK010-B/ CTS010#/ TXDB010/ CRX2/ USB0_EXICE N	ET0_MDIO-B/ CAT0_MDIO -B		IRQ2	ADCNV2	DSM1_CL K0-C
60	VCL											
61	VSS											
62	VCC											

Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (5/10)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
63	CLKOUT	P801	PIO_057	EBCLK-A		GTIV/ GTIOC0B/ POEGC	TXD010-B/ SMOSI010-B/ SSDA010/ TXDA010	ET0_CRS/ CATSYNC0		IRQ9	ADCNV1	DSM1_DAT1-C
64		P800	PIO_056	CS1#-A/ DQM0-B		GTIU/ GTIOC0A/ POEGD	RXD010-B/ SMISO010-B/ SSCL010	ET0_COL/ CATLATCH0		IRQ8	ADCNV0	DSM1_CLK1-C
65	ETHPHYCLK	PC07	PIO_031	D0-A	TMO2/ TOC0/ CACREF	GTETRGD/ GTADSM1/ GTIOC15B/ POEGA	TXD008-A/ SMOSI008-A/ SSDA008/ TXDA008/ MISO0-A/ SSITXD0	CATRESTOUT	SD0_CD	IRQ14		DSM1_DAT2-C/ PDMDAT0
66		PC06	PIO_030	D1-A	TMCI2/ TIC0	GTETRGC/ GTCPPO7/ GTIOC15A/ POEGB	RXD008-A/ SMISO008-A/ SSCL008/ MOSI0-A/ SSILRCK0	ET0_TX_ER-A/ CATLINKACT0	SD0_WP	IRQ13		DSM1_CLK2-C/ PDMCLK0
67		PC05	PIO_029	D2-A	TMRI2	GTOWLO/ GTIOC9B	SCK008-A/ CTS008#/ TXDB008/ RSPCK0-A/ SSIBCK0	ET0_TX_EN-A/ RMII0_TX_EN-A/ CAT0_TX_EN-A	SD0_DAT1-A	IRQ5		PCOUTZ1
68		PC04	PIO_028	D3-A	TMCI1	GTOWUP/ GTIOC9A	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008/ CTS011#/ SSL00-A/ AUDIO_CLK	ET0_TXD3-A/ CAT0_ETXD3-A	SD0_DAT0-A	IRQ12		PCOUTB1
69		PC03	PIO_027	D4-A		GTOVLO/ GTIOC8B	TXD011-A/ SMOSI011-A/ SSDA011/ TXDA011/ SDAHS1-C	ET0_TXD2-A/ CAT0_ETXD2-A	SD0_CLK-A	IRQ11		PCOUTA1
70		PC02	PIO_026	D5-A		GTOVUP/ GTIOC8A	RXD011-A/ SMISO011-A/ SSCL011/ SSL03-A/ SCLHS1-C	ET0_TXD1-A/ RMII0_TXD1-A/ CAT0_ETXD1-A	SD0_CMD-A	IRQ10		PCOUTZ0
71		PC01	PIO_025	D6-A		GTOULO/ GTIOC7B	SCK011-A/ CTS011#/ TXDB011/ SSL02-A/ SDA00-C	ET0_TXD0-A/ RMII0_TXD0-A/ CAT0_ETXD0-A	SD0_DAT3-A	IRQ12		PCOUTB0
72		PC00	PIO_024	D7-A		GTOUUP/ GTIOC7A	CTS011#/ RTS011#/ SS011#/ DE011/ TXDB011/ SSL01-A/ SCL00-C	ET0_TX_CLK-A/ CAT0_TX_CLK-A	SD0_DAT2-A	IRQ14		PCOUTA0
73		PB07	PIO_023	D8-A		GTOWLO/ GTIOC6B	TXD009-A/ SMOSI009-A/ SSDA009/ TXDA009	ET0_LINKSTA/ CAT0_LINKSTA		IRQ15		
74		PB06	PIO_022	D9-A		GTOWUP/ GTIOC6A	RXD009-A/ SMISO009-A/ SSCL009	ET0_RX_ER-A/ RMII0_RX_ER-A/ CAT0_RX_ER-A		IRQ6		

Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (6/10)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
75		PB05	PIO_021	D10-A	TMRI1	GTOVLO/ GTIOC5B	SCK009-A/ CTS009#/ TXDB009	ET0_RX_DV-A/ RMII0_CRS_DV-A/ CAT0_RX_DV-A		IRQ13		
76		PB04	PIO_020	D11-A		GTOVUP/ GTIOC5A	CTS004#/ CTS009#/ RTS009#/ SS009#/ DE009/ TXDB009	ET0_RX_CLK-A/ RMII0_REF50CK-A/ CAT0_RX_CLK-A		IRQ4		
77	VCC											
78	VSS											
79	VCL											
80		PB03	PIO_019	D12-A	TMO0	GTOULO/ GTIOC4B	SCK004-A/ CTS004#/ TXDB004	ET0_RXD3-A/ CAT0_ERXD3-A		IRQ3		
81		PB02	PIO_018	D13-A		GTOUUP/ GTIOC4A	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004/ CTS009#	ET0_RXD2-A/ CAT0_ERXD2-A		IRQ2		
82		PB01	PIO_017	D14-A	TMCI0	GTETRGB/ GTCPPO4/ GTIOC14B/ POEGA	TXD004-A/ SMOSI004-A/ SSDA004/ TXDA004	ET0_RXD1-A/ RMII0_RXD1-A/ CAT0_ERXD1-A		IRQ4-DS		DSM0_DAT2-A/ PCINB1
83		PB00	PIO_016	D15-A		GTETRGA/ GTADSM0/ GTIOC14A/ POEGC	RXD004-A/ SMISO004-A/ SSCL004	ET0_RXD0-A/ RMII0_RXD0-A/ CAT0_ERXD0-A		IRQ12	ADST2	DSM0_CLK2-A/ PCINA1
84	ETHPHYCLK	PA07	PIO_015	A0-A/ BC0#-A/ DQM1-B		GTIOC3B/ GTIOC13B	RXD010-A/ SMISO010-A/ SSCL010/ MISO0-B	ET1_TX_ER-A/ CATLINKACT1		IRQ7		PCINB0
85		PA06	PIO_014	A1-A	TMCI3	GTIOC3A/ GTIOC13A	TXD010-A/ SMOSI010-A/ SSDA010/ TXDA010/ MOSI0-B	ET1_TXD3-A/ CAT1_ETXD3-A		IRQ14		PCINZ1
86		PA05	PIO_013	A2-A		GTIOC2B/ GTIOC12B	SCK010-A/ CTS010#/ TXDB010/ RSPCK0-B	ET1_TXD2-A/ CAT1_ETXD2-A		IRQ5		PCINA0
87		PA04	PIO_012	A3-A	TMRI0	GTIOC2A/ GTIOC12A	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ SSL00-B	ET1_TXD1-A/ RMII1_TXD1-A/ CAT1_ETXD1-A		IRQ5-DS		PCINZ0
88	VCC											
89	VSS											
90	VCL											
91		PA03	PIO_011	A4-A		GTIOC1B/ GTIOC11B	RXD005-A/ SMISO005-A/ SSCL005	ET1_TXD0-A/ RMII1_TXD0-A/ CAT1_ETXD0-A		IRQ6-DS	ADSYNC	DSM0_DAT1-A

Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (7/10)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
92		PA02	PIO_010	A5-A		GTIW/ GTIOC1A/ GTIOC11A	TXD005-A/ SMOSI005-A/ SSDA005/ TXDA005/ SSL03-B	ET1_TX_CLK-A/ CAT1_TX_CLK-A		IRQ10	ADCNV2	DSM0_CLK1-A
93		PA01	PIO_009	A6-A		GTIV/ GTIOC0B/ GTIOC10B	SCK005-A/ CTS005#/ TXDB005/ SSL02-B	ET1_TX_EN-A/ RMII1_TX_EN-A/ CAT1_TX_EN-A		IRQ11	ADCNV1	DSM0_DAT0-A
94	ETHPHYCLK	PA00	PIO_008	A7-A	CACREF	GTIU/ GTIOC0A/ GTIOC10A	CTS010#/ CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ SSL01-B	CATIRQ		IRQ1-DS	ADCNV0	DSM0_CLK0-A
95		P702	PIO_050	RD#-A		GTETRGA/ GTIOC11A	SCK004-B/ CTS004#/ TXDB004	ET1_CRS/ CATSYNC1	XSPI1_WP0#/ XSPI1_RESET1#/ HSYNC	IRQ10	ADST2	DSM1_CLK1-D
96		P701	PIO_049	CKE-A		GTIOC10B	RXD004-B/ SMISO004-B/ SSCL004	ET1_COL/ CATLATCH1	XSPI1_RSTO0#/ XSPI1_RESET0#/ VSYNC	IRQ1	ADST1	DSM1_DAT0-D
97	ETHPHYCLK	P700	PIO_048	SDCLK-A		GTIOC10A	TXD004-B/ SMOSI004-B/ SSDA004/ TXDA004	ET1_INT/ CATRESTOUT	XSPI1_INT0#/ XSPI1_ECS0#/PIXCLK	IRQ0	ADST0	DSM1_CLK0-D
98	VCC											
99	VSS											
100	VCL											
101		PE07	PIO_047	A8-B/A20-D	TOC1	GTETRGD/ GTCPPO7/ GTIOC10B/ POEGD		ET1_LINKSTA/ CAT1_LINKSTA/ CATRESTOUT	XSPI1_CS0#/PIXD7	IRQ7		
102		PE06	PIO_046	A9-B/A21-D	TIC1	GTETRGC/ GTADSM1/ GTIOC10A/ POEGB	SSL13-A	ET1_RX_CLK-D/ RMII1_REF50CK-D/ CAT1_RX_CLK-D/ CATLEDER R	XSPI1_DS/ PIXD6	IRQ6		
103		PE05	PIO_045	A10-B/ A22-D		GTOWLO/ GTIOC9B	SSL12-A	ET1_RXD3-D/ CAT1_ERXD3-D/ CATLEDRUN	XSPI1_IO3/ PIXD5	IRQ5		
104		PE04	PIO_044	A11-B/ A23-D		GTOWUP/ GTIOC9A	CTS012#/ SSL11-A	ET1_RXD2-D/ CAT1_ERXD2-D/ CATLEDSTER	XSPI1_IO2/ XSPI1_WP0#/PIXD4	IRQ12		
105		PE03	PIO_043	A12-B	TOC3	GTOVLO/ GTIOC8B	CTS012#/ RTS012#/ SS012#/ DE012/ TXDB012/ MISO1-A	ET1_RXD1-D/ RMII1_RXD1-D/ CAT1_ERXD1-D	SD0_DAT7-B/ XSPI1_IO1/ PIXD3	IRQ11		

Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (8/10)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
106		PE02	PIO_042	A13-B	TIC3	GTOVUP/ GTIOC8A	RXD012-A/ SMISO012-A/ SSCL012/ MOSI1-A	ET1_RXD0-D/ RMII1_RXD0-D/ CAT1_ERXD0-D	SD0_DAT6-B/ XSPI1_IO0/ PIXD2	IRQ7-DS		
107	CLKOUT	PE01	PIO_041	A14-B		GTOULO/ GTIOC7B	TXD012-A/ SMOSI012-A/ SSDA012/ TXDA012/ RSPCK1-A	ET1_RX_DV-D/ RMII1_CRS_DV-D/ CAT1_RX_DV-D	SD0_DAT5-B/ XSPI1_CK/ PIXD1	IRQ9		
108	ETHPHYCLK	PE00	PIO_040	A15-B		GTOUUP/ GTIOC7A	SCK012-A/ CTS012#/ TXDB012/ SSL10-A	ET1_RX_ER-D/ RMII1_RX_ER-D/ CAT1_RX_ER-D	SD0_DAT4-B/ XSPI1_CKN#/ XSPI1_CS1#/PIXD0	IRQ8		
109		P605	PIO_013	CS2#-C		GTIOC6B	RXD009-B/ SMISO009-B/ SSCL009/ SSL02-D	ET1_TXD3-B/ ET_TAS_STA1/ CAT1_ETXD3-B	XSPI0_INT0#/ XSPI0_ECS0#	IRQ13		DSM1_DAT1-A
110		P604	PIO_012	CS3#-C		GTIOC6A	TXD009-B/ SMOSI009-B/ SSDA009/ TXDA009/ SSL01-D	ET1_TXD2-B/ ET_TAS_STA0/ CAT1_ETXD2-B	XSPI0_CS1#/ XSPI0_RSTO0#	IRQ4		DSM1_CLK1-A
111		P603	PIO_011	WE#-B		GTIOC5B	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008/ CTS009#/ MISO0-D	ET1_TXD1-B/ RMII1_TXD1-B/ GPTP_PTPOUT3/ CAT1_ETXD1-B/ CATSYNC0	XSPI0_IO7/ PCKO	IRQ3		DSM1_DAT0-A
112		P602	PIO_010	CAS#-B		GTIOC5A	SCK008-B/ CTS008#/ TXDB008/ MOSI0-D	ET1_TXD0-B/ RMII1_TXD0-B/ GPTP_PTPOUT2/ CAT1_ETXD0-B/ CATLATCH0	XSPI0_IO6/ HSYNC	IRQ2	ADTRG2#	DSM1_CLK0-A
113		P601	PIO_009	RAS#-B		GTIOC4B	RXD008-B/ SMISO008-B/ SSCL008/ RSPCK0-D	ET1_TX_EN-B/ RMII1_TX_EN-B/ GPTP_PTPOUT1/ CAT1_TX_EN-B/ CATSYNC1	XSPI0_IO5/ VSYNC	IRQ1	ADTRG1#	
114		P600	PIO_008	SDCS#-B		GTIOC4A	TXD008-B/ SMOSI008-B/ SSDA008/ TXDA008/ SSL00-D	ET1_TX_CLK-B/ GPTP_PTPOUT0/ CAT1_TX_CLK-B/ CATLATCH1	XSPI0_IO4/ PIXCLK	IRQ0	ADTRG0#	
115	VCC2											
116	VSS											

Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (9/10)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
117		PD07	PIO_039	A16-B		GTIW/ GTIOC3B/ POEGA	TXD003-A/ SMOSI003-A/ SSDA003/ TXDA003/ CTX1	ET1_LINKSTA/ CAT1_LINKSTA	SD0_CD/ XSPI0_CS0#/ XSPI0_RESET1#/PIXD7	IRQ7	AN031	
118		PD06	PIO_038	A17-B		GTIV/ GTIOC3A/ POEGB	RXD003-A/ SMISO003-A/ SSCL003/ SSL23-A/ CRX1	ET1_RX_ER-B/ RMII1_RX_ER-B/ CAT1_RX_ER-B/ CATLEDER R	SD0_WP/ XSPI0_DS/ PIXD6	IRQ6	AN030	
119		PD05	PIO_037	A18-B		GTIU/ GTIOC2B/ POEGD	SCK003-A/ CTS003#/ TXDB003/ SSL22-A/ CTX0	ET1_RX_DV-B/ RMII1_CRS_DV-B/ CAT1_RX_DV-B/ CATLEDSTER	SD0_DAT1-B/ XSPI0_IO3/ PIXD5	IRQ5	AN029	
120		PD04	PIO_036	A19-B		GTETRGA/ GTIOC2A/ POEGC	CTS002#/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ SSL21-A/ CRX0	ET1_RX_CLK-B/ RMII1_REF50CK-B/ CAT1_RX_CLK-B/ CATLEDRUN	SD0_DAT0-B/ XSPI0_IO2/ XSPI0_WP0#/PIXD4	IRQ4	AN028	
121		PD03	PIO_035	A20-B	TOC2	GTIOC1B/ POEGA	TXD002-A/ SMOSI002-A/ SSDA002/ TXDA002/ MISO2-A	ET1_RXD3-B/ CAT1_ERXD3-B/ CAT0_MDIO-D	SD0_CLK-B/ XSPI0_IO1/ PIXD3	IRQ3	AN027	
122		PD02	PIO_034	A21-B	TIC2	GTETRGB/ GTIOC1A/ POEGB	RXD002-A/ SMISO002-A/ SSCL002/ MOSI2-A	ET1_RXD2-B/ CAT1_ERXD2-B/ CAT0_MDC-D	SD0_CMD-B/ XSPI0_IO0/ PIXD2	IRQ2	AN026	
123		PD01	PIO_033	A22-B		GTETRGC/ GTIOC0B/ POEGC	SCK002-A/ CTS002#/ TXDB002/ RSPCK2-A	ET1_RXD1-B/ RMII1_RXD1-B/ CAT1_ERXD1-B/ CATSYNC0	SD0_DAT3-B/ XSPI0_CK/ PIXD1	IRQ1	AN025	
124		PD00	PIO_032	A23-B		GTETRGD/ GTIOC0A/ POEGD	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS003#/ SSL20-A	ET1_RXD0-B/ RMII1_RXD0-B/ CAT1_ERXD0-B/ CATLATCH0	SD0_DAT2-B/ XSPI0_CKN#/ XSPI0_CS1#/PIXD0	IRQ0	AN024	
125	VSS											
126	VCL											
127		P901	PIO_001			GTETRGB/ GTCPPO6	TXD001-C/ SMOSI001-C/ SSDA001/ TXDA001	ET1_CRS/ ET_TAS_STA1/ CATLATCH1	XSPI0_RSTO1#/ XSPI0_RESET0#	IRQ9	AN033	
128		P900	PIO_000			GTETRGA/ GTCPPO5	RXD001-C/ SMISO001-C/ SSCL001	ET1_COL/ ET_TAS_STA0/ CATSYNC1	XSPI0_INT1#/ XSPI0_ECS1#	IRQ0	AN032	
129	AVCC0											

Table 1.9 List of Pin and Pin Functions (144-Pin LFQFP) (10/10)

Pin Number					Timer		Communication		Memory I/F Camera I/F			Others
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	Bus EXDMAC SDRAMC	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI, PDC)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
130	AVSS0											
131	VREFL0											
132	VREFH0											
133		P405	PIO_053							IRQ13-DS	AN005	
134		P404	PIO_052							IRQ12-DS	AN004	
135		P403	PIO_051							IRQ11-DS	AN003	
136		P402	PIO_050							IRQ10-DS	AN002	
137		P401	PIO_049							IRQ9-DS	AN001	
138		P400	PIO_048							IRQ8-DS	AN000	
139		P415	PIO_063							IRQ31	AN015/ DA1	
140		P414	PIO_062							IRQ30	AN014/ DA0	
141		P007	PIO_007			GTCPPO6/ GTIOC13B/ POEGA	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000	ET1_INT/ CATIRQ		IRQ23-DS	ADTRG0 #/AN023	PDMDAT0
142		P006	PIO_006			GTCPPO5/ GTIOC13A/ GTIOC9B	SCK000-B/ CTS000#/ TXDB000	ET1_LINKS TA/ CAT1_LINK STA		IRQ22-DS	ADTRG1 #/AN022	PDMCLK0 / PCOUTZ1
143		P005	PIO_005			GTCPPO4/ GTIOC12B/ GTIOC9A	RXD000-B/ SMISO000-B/ SSCL000/ SSILRCK1	ET1_MDIO-D/ CATLATCH 0		IRQ21-DS	ADTRG2 #/AN021	DSM0_DA T2-B/ PCOUTB1
144		P004	PIO_004			GTCPPO3/ GTIOC12A/ GTIOC8B	TXD000-B/ SMOSI000-B/ SSDA000/ TXDA000/ SSITXD1	ET1_MDC-D/ CATSYNC0		IRQ20-DS	AN020	DSM0_CL K2-B/ PCOUTA1

1.6.6 100-Pin LFQFP

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (1/7)

Pin Number				Timer		Communication		Memory I/F Camera I/F			Others
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
1		P003	PIO_003		GTCPPO2/ GTIOC11B/ GTIOC8A	RXD007-A/ SMISO007-A/ SSCL007/ SSIRXD1	ET0_MDIO-D/ CAT0_MDIO-E		IRQ19-DS	AN019	DSM0_DAT1-B/ PCOUTB0
2		P002	PIO_002	TMCI1	GTCPPO1/ GTIOC11A/ GTIOC7B	TXD007-A/ SMOSI007-A/ SSDA007/ TXDA007/ SSIBCK1	ET0_MDC-D/ CAT0_MDC-E		IRQ18-DS	AN018	DSM0_CLK1-B/ PCOUTA0
3		P001	PIO_001	TMCI0	GTCPPO0/ GTIOC10B/ GTIOC7A	SCK007-A/ CTS007#/ TXDB007/ SSIBCK0	ET0_LINKSTA/ CAT0_LINKSTA		IRQ17-DS	AN017	DSM0_DAT0-B/ PCOUTZ0
4	VSS										
5	VCL										
6	RES#										
7	MD/FINED	P315									
8		P312	PIO_060	RTCIC2	GTETRGD/ GTCPPO15/ POEGA	SSL13-B/ SSILRCK0	ET1_WOL		IRQ20	ADTRG2#	DSM0_DAT2-C/ TAMPI2
9		P311	PIO_059	RTCIC1	GTETRGC/ GTCPPO14/ POEGD	CTS007#/ SSL12-B/ SSIRXD0	ET0_WOL		IRQ19	ADTRG1#	DSM0_CLK2-C/ TAMPI1
10		P310	PIO_058	RTCIC0/ CACREF	GTETRGB/ GTCPPO1/ POEGC	CTS000#/ CTS001#/ SSL11-B/ SSITXD0	ET1_INT/ CATIRQ		IRQ18	ADTRG0#	TAMPI0
11	VBATT/ VCC										
12	XCIN/ EXCIN	P309									
13	XCOUT	P308									
14	VSS										
15	XTAL	P307									
16	EXTAL	P306									
17	VCC										
18		P305							NMI/IRQ0		
19	VCC_USB										
20		PF01	PIO_049		GTCPPO15	USB0_DM			IRQ1		
21		PF00	PIO_048		GTCPPO14	USB0_DP			IRQ0		
22	VSS_USB										
23	ETHPHYCLK	P304	PIO_028	TMCI3	GTETRGD/ GTCPPO0/ POEGA	CTS000#/ CTS001#/ USB0_VBUSEN	ET0_INT/ CATRESTOUT		IRQ0-DS	ADTRG0#	
24	TDI	P303	PIO_027	TMCI2	GTCPPO13	RXD000-A/ SMISO000-A/ SSCL000/ RXD001-A/ SMISO001-A/ SSCL001/ MISO1-C	ET1_CRS		IRQ1		

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (2/7)

Pin Number				Timer		Communication		Memory I/F Camera I/F			Others
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
25	TDO	P302	PIO_026	TMRI3	GTCPPO12	TXD000-A/ SMOSI000-A/ SSDA000/ TXDA000/ TXD001-A/ SMOSI001-A/ SSDA001/ TXDA001/ MOSI1-C	ET1_COL		IRQ4		
26	TCK/ SWCLK	P301	PIO_025	TMCI3	GTCPPO11	SCK000-A/ CTS000#/ TXDB000/ SCK001-A/ CTS001#/ TXDB001/ RSPCK1-C	ET1_WOL		IRQ7		
27	TMS/ SWDIO	P300	PIO_024	TMO1	GTCPPO10	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000/ CTS001#/ RTS001#/ SS001#/ DE001/ TXDB001/ SSL10-C	ET0_WOL		IRQ6		
28		P201	PIO_017	TMCI0	GTIW/ GTIOC3B/ GTIOC14B	MISO0-C/ SCLHS1-A/ USB0_EXICEN/SSILRCK0	ET0_RX_ER-B/ RMII0_RX_ER-B/ CAT0_RX_ER-B	SD0_CLK-C	IRQ9		PCINZ0
29		P200	PIO_016	TMRI0	GTETRGA/ GTIOC3A/ GTIOC14A	MOSI0-C/ SDAHS1-A/ USB0_ID/ SSIRXD0	ET0_TX_EN-B/ RMII0_TX_EN-B/ CAT0_TX_EN-B	SD0_CMD-C	IRQ8	ADTRG2#	PCINZ1
30		P107	PIO_015	TMO1	GTIV/ GTIOC15B/ POEGA	TXD003-B/ SMOSI003-B/ SSDA003/ TXDA003/ SDAHS2-A/ SSITXD0	ET0_TXD3-B/ CAT0_ETXD3-B/ CATI2CDATA-B	SD0_DAT3-C	IRQ31-DS	ADTRG1#	PCINB1
31	CLKOUT	P106	PIO_014	TMO2/ RTCOUT	GTIU/ GTIOC15A/ POEGB	RXD003-B/ SMISO003-B/ SSCL003/ SCLHS2-A	ET0_TXD2-B/ CAT0_ETXD2-B/ CATI2CCLK-B	SD0_DAT2-C	IRQ30-DS	ADTRG0#	PCINA1
32		P105	PIO_013	TMCI2	GTIV/ GTIOC14B	TXD002-B/ SMOSI002-B/ SSDA002/ TXDA002/ SCK003-B/ CTS003#/ TXDB003/ CRX2/ USB0_VBUS/ SSILRCK1	ET0_TXD1-B/ RMII0_TXD1-B/ CAT0_ETXD1-B/ CATLEDRUN		IRQ29-DS	ADST1	DSM0_DAT1-C/ PCINB0

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (3/7)

Pin Number				Timer		Communication		Memory I/F Camera I/F			Others
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
33		P104	PIO_012	TMRI2	GTIW/ GTIOC14A	RXD002-B/ SMISO002-B/ SSCL002/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ CTX2/ USB0_OVRCURA-DS	ET0_TXD0-B/ RMII0_TXD0-B/ CAT0_ETXD0-B/ CATLEDSTER		IRQ4	ADST0	DSM0_CLK1-C/ PCINA0
34	VCL										
35	VSS										
36	VCC										
37		P103	PIO_011	TMO3	GTADSM1/ GTIOC13B	CTS002#/ SDA00-A	ET0_CRS/ CATI2CDATA-A		IRQ3		
38		P102	PIO_010	TMCI1	GTADSM0/ GTIOC13A	SCL00-A	ET0_COL/ CATI2CCLK-A		IRQ2		
39		P101	PIO_009	TMCI3	GTETRGC/ GTADSM1/ GTIOC12B	SCK002-B/ CTS002#/ TXDB002/ USB0_VBUS-DS	ET0_TX_CLK-B/ CAT0_TX_CLK-B/ CAT0_LINKSTA		IRQ1	ADTRG1#	DSM0_DAT0-C
40	VCC_DCDC										
41	VLO										
42	VSS_DCDC										
43	VSS										
44		PC06	PIO_030	TMCI2	GTETRGC/ GTCPPO7/ GTIOC15A/ POEGB	RXD008-A/ SMISO008-A/ SSCL008/ MOSI0-A/ SSILRCK0	ET0_TX_ER-A/ CATLINKACT0	SD0_WP	IRQ13		PDMCLK0
45		PC05	PIO_029	TMRI2	GTOWLO/ GTIOC9B	SCK008-A/ CTS008#/ TXDB008/ RSPCK0-A/ SSIBCK0	ET0_TX_EN-A/ RMII0_TX_EN-A/ CAT0_TX_EN-A	SD0_DAT1-A	IRQ5		PCOUTZ1
46		PC04	PIO_028	TMCI1	GTOWUP/ GTIOC9A	CTS008#/ RTS008#/ SS008#/ DE008/ TXDB008/ CTS011#/ SSL00-A/ AUDIO_CLK	ET0_TXD3-A/ CAT0_ETXD3-A	SD0_DAT0-A	IRQ12		PCOUTB1
47		PC03	PIO_027		GTOVLO/ GTIOC8B	TXD011-A/ SMOSI011-A/ SSDA011/ TXDA011/ SDAHS1-C	ET0_TXD2-A/ CAT0_ETXD2-A	SD0_CLK-A	IRQ11		PCOUTA1
48		PC02	PIO_026		GTOVUP/ GTIOC8A	RXD011-A/ SMISO011-A/ SSCL011/ SSL03-A/ SCLHS1-C	ET0_TXD1-A/ RMII0_TXD1-A/ CAT0_ETXD1-A	SD0_CMD-A	IRQ10		PCOUTZ0

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (4/7)

Pin Number				Timer		Communication		Memory I/F Camera I/F			Others
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
49		PC01	PIO_025		GTOULO/ GTIOC7B	SCK011-A/ CTS011#/ TXDB011/ SSL02-A/ SDA00-C	ET0_TXD0-A/ RMII0_TXD0-A/ CAT0_ETXD0-A	SD0_DAT3-A	IRQ12		PCOUTB0
50		PC00	PIO_024		GTOUUP/ GTIOC7A	CTS011#/ RTS011#/ SS011#/ DE011/ TXDB011/ SSL01-A/ SCL00-C	ET0_TX_CLK-A/ CAT0_TX_CLK-A	SD0_DAT2-A	IRQ14		PCOUTA0
51		PB06	PIO_022		GTOWUP/ GTIOC6A		ET0_RX_ER-A/ RMII0_RX_ER-A/ CAT0_RX_ER-A		IRQ6		
52		PB05	PIO_021	TMRI1	GTOVLO/ GTIOC5B		ET0_RX_DV-A/ RMII0_CRS_DV-A/ CAT0_RX_DV-A		IRQ13		
53		PB04	PIO_020		GTOVUP/ GTIOC5A	CTS004#	ET0_RX_CLK-A/ RMII0_REF50CK-A/ CAT0_RX_CLK-A		IRQ4		
54		PB03	PIO_019	TMO0	GTOULO/ GTIOC4B	SCK004-A/ CTS004#/ TXDB004	ET0_RXD3-A/ CAT0_ERXD3-A		IRQ3		
55		PB02	PIO_018		GTOUUP/ GTIOC4A	CTS004#/ RTS004#/ SS004#/ DE004/ TXDB004	ET0_RXD2-A/ CAT0_ERXD2-A		IRQ2		
56		PB01	PIO_017	TMCI0	GTETRGB/ GTCPPO4/ GTIOC14B/ POEGA	TXD004-A/ SMOSI004-A/ SSDA004/ TXDA004	ET0_RXD1-A/ RMII0_RXD1-A/ CAT0_ERXD1-A		IRQ4-DS		DSM0_DAT2-A/ PCINB1
57		PB00	PIO_016		GTETRGA/ GTADSM0/ GTIOC14A/ POEGC	RXD004-A/ SMISO004-A/ SSCL004	ET0_RXD0-A/ RMII0_RXD0-A/ CAT0_ERXD0-A		IRQ12	ADST2	DSM0_CLK2-A/ PCINA1
58	ETHPHYCLK	PA07	PIO_015		GTIOC3B/ GTIOC13B	RXD010-A/ SMISO010-A/ SSCL010/ MISO0-B	ET1_TX_ER-A/ CATLINKACT1		IRQ7		PCINB0
59		PA06	PIO_014	TMCI3	GTIOC3A/ GTIOC13A	TXD010-A/ SMOSI010-A/ SSDA010/ TXDA010/ MOSI0-B	ET1_TXD3-A/ CAT1_ETXD3-A		IRQ14		PCINZ1
60		PA05	PIO_013		GTIOC2B/ GTIOC12B	SCK010-A/ CTS010#/ TXDB010/ RSPCK0-B	ET1_TXD2-A/ CAT1_ETXD2-A		IRQ5		PCINA0

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (5/7)

Pin Number				Timer		Communication		Memory I/F Camera I/F			Others
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
61		PA04	PIO_012	TMRI0	GTIOC2A/ GTIOC12A	CTS010#/ RTS010#/ SS010#/ DE010/ TXDB010/ SSL00-B	ET1_TXD1-A/ RMII1_TXD1-A/ CAT1_ETXD1-A		IRQ5-DS		PCINZ0
62	VCC										
63	VSS										
64	VCL										
65		PA03	PIO_011		GTIOC1B/ GTIOC11B	RXD005-A/ SMISO005-A/ SSCL005	ET1_TXD0-A/ RMII1_TXD0-A/ CAT1_ETXD0-A		IRQ6-DS	ADSYNC	DSM0_DAT1-A
66		PA02	PIO_010		GTIW/ GTIOC1A/ GTIOC11A	TXD005-A/ SMOSI005-A/ SSDA005/ TXDA005/ SSL03-B	ET1_TX_CLK-A/ CAT1_TX_CLK-A		IRQ10	ADCNV2	DSM0_CLK1-A
67		PA01	PIO_009		GTIV/ GTIOC0B/ GTIOC10B	SCK005-A/ CTS005#/ TXDB005/ SSL02-B	ET1_TX_EN-A/ RMII1_TX_EN-A/ CAT1_TX_EN-A		IRQ11	ADCNV1	DSM0_DAT0-A
68	ETHPHYCLK	PA00	PIO_008	CACREF	GTIU/ GTIOC0A/ GTIOC10A	CTS010#/ CTS005#/ RTS005#/ SS005#/ DE005/ TXDB005/ SSL01-B	CATIRQ		IRQ1-DS	ADCNV0	DSM0_CLK0-A
69		PE06	PIO_046		GTETRGC/ GTADSM1/ GTIOC10A/ POEGB	SSL13-A	ET1_RX_CLK-D/ RMII1_REF50CK-D/ CAT1_RX_CLK-D/ CATLEDERR	XSPI1_DS	IRQ6		
70		PE05	PIO_045		GTOWLO/ GTIOC9B	SSL12-A	ET1_RXD3-D/ CAT1_ERXD3-D/ CATLEDRUN	XSPI1_IO3	IRQ5		
71		PE04	PIO_044		GTOWUP/ GTIOC9A	CTS012#/ SSL11-A	ET1_RXD2-D/ CAT1_ERXD2-D/ CATLEDSTER	XSPI1_IO2/ XSPI1_WP0#	IRQ12		
72		PE03	PIO_043	TOC3	GTOVLO/ GTIOC8B	CTS012#/ RTS012#/ SS012#/ DE012/ TXDB012/ MISO1-A	ET1_RXD1-D/ RMII1_RXD1-D/ CAT1_ERXD1-D	SD0_DAT7-B/XSPI1_IO1	IRQ11		
73		PE02	PIO_042	TIC3	GTOVUP/ GTIOC8A	RXD012-A/ SMISO012-A/ SSCL012/ MOSI1-A	ET1_RXD0-D/ RMII1_RXD0-D/ CAT1_ERXD0-D	SD0_DAT6-B/XSPI1_IO0	IRQ7-DS		

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (6/7)

Pin Number				Timer		Communication		Memory I/F Camera I/F			Others
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
74	CLKOUT	PE01	PIO_041		GTOULO/ GTIOC7B	TXD012-A/ SMOSI012-A/ SSDA012/ TXDA012/ RSPCK1-A	ET1_RX_DV-D/ RMII1_CRS_DV-D/ CAT1_RX_DV-D	SD0_DAT5-B/XSPI1_CK	IRQ9		
75	ETHPHYCLK	PE00	PIO_040		GTOUUP/ GTIOC7A	SCK012-A/ CTS012#/ TXDB012/ SSL10-A	ET1_RX_ER-D/ RMII1_RX_ER-D/ CAT1_RX_ER-D	SD0_DAT4-B/ XSPI1_CKN#/ XSPI1_CS1#	IRQ8		
76		P601	PIO_009		GTIOC4B	RXD008-B/ SMISO008-B/ SSCL008/ RSPCK0-D	ET1_TX_EN-B/ RMII1_TX_EN-B/ GPTP_PTPOUT1/ CAT1_TX_EN-B/ CATSYNC1		IRQ1	ADTRG1#	
77		P600	PIO_008		GTIOC4A	TXD008-B/ SMOSI008-B/ SSDA008/ TXDA008/ SSL00-D	ET1_TX_CLK-B/ GPTP_PTPOUT0/ CAT1_TX_CLK-B/ CATLATCH1		IRQ0	ADTRG0#	
78		PD07	PIO_039		GTIW/ GTIOC3B/ POEGA	TXD003-A/ SMOSI003-A/ SSDA003/ TXDA003/ CTX1	ET1_LINKSTA/ CAT1_LINKSTA	SD0_CD/ XSPI0_CS0#/ XSPI0_RESET1#	IRQ7	AN031	
79		PD06	PIO_038		GTIV/ GTIOC3A/ POEGB	RXD003-A/ SMISO003-A/ SSCL003/ SSL23-A/ CRX1	ET1_RX_ER-B/ RMII1_RX_ER-B/ CAT1_RX_ER-B/ CATLEDERR	SD0_WP/ XSPI0_DS	IRQ6	AN030	
80		PD05	PIO_037		GTIU/ GTIOC2B/ POEGD	SCK003-A/ CTS003#/ TXDB003/ SSL22-A/ CTX0	ET1_RX_DV-B/ RMII1_CRS_DV-B/ CAT1_RX_DV-B/ CATLEDSTER	SD0_DAT1-B/XSPI0_IO3	IRQ5	AN029	
81		PD04	PIO_036		GTETRGA/ GTIOC2A/ POEGC	CTS002#/ CTS003#/ RTS003#/ SS003#/ DE003/ TXDB003/ SSL21-A/ CRX0	ET1_RX_CLK-B/ RMII1_REF50CK-B/ CAT1_RX_CLK-B/ CATLEDRUN	SD0_DAT0-B/ XSPI0_IO2/ XSPI0_WP0#	IRQ4	AN028	
82		PD03	PIO_035	TOC2	GTIOC1B/ POEGA	TXD002-A/ SMOSI002-A/ SSDA002/ TXDA002/ MISO2-A	ET1_RXD3-B/ CAT1_ERXD3-B/ CAT0_MDIO-D	SD0_CLK-B/ XSPI0_IO1	IRQ3	AN027	

Table 1.10 List of Pin and Pin Functions (100-Pin LFQFP) (7/7)

Pin Number				Timer		Communication		Memory I/F Camera I/F			Others
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	PIO	(TMR, CMTW, RTC, CAC)	(GPTW, POEG)	(RSCI, RSPIA, RI3C, RIICHS, CANFD, USB, SSIE)	(ESWM, ESC)	(XSPI, SDHI)	Interrupt	A/D D/A	(DSMIF, PDMIF, PCIF, Tamper detection)
83		PD02	PIO_034	TIC2	GTETRGB/ GTIOC1A/ POEGB	RXD002-A/ SMISO002-A/ SSCL002/ MOSI2-A	ET1_RXD2-B/ CAT1_ERXD2-B/ CAT0_MDC-D	SD0_CMD-B/ XSPI0_IO0	IRQ2	AN026	
84		PD01	PIO_033		GTETRGC/ GTIOC0B/ POEGC	SCK002-A/ CTS002#/ TXDB002/ RSPCK2-A	ET1_RXD1-B/ RMII1_RXD1-B/ CAT1_ERXD1-B/ CATSYNC0	SD0_DAT3-B/XSPI0_CK	IRQ1	AN025	
85		PD00	PIO_032		GTETRGD/ GTIOC0A/ POEGD	CTS002#/ RTS002#/ SS002#/ DE002/ TXDB002/ CTS003#/ SSL20-A	ET1_RXD0-B/ RMII1_RXD0-B/ CAT1_ERXD0-B/ CATLATCH0	SD0_DAT2-B/ XSPI0_CKN#/ XSPI0_CS1#	IRQ0	AN024	
86	VCC2										
87	VSS										
88	VCL										
89	AVCC0										
90	AVSS0										
91	VREFL0										
92	VREFH0										
93		P404	PIO_052						IRQ12-DS	AN004	
94		P402	PIO_050						IRQ10-DS	AN002	
95		P400	PIO_048						IRQ8-DS	AN000	
96		P414	PIO_062						IRQ30	AN014/ DA0	
97		P007	PIO_007		GTCPPO6/ GTIOC13B/ POEGA	CTS000#/ RTS000#/ SS000#/ DE000/ TXDB000	ET1_INT/ CATIRQ		IRQ23-DS	ADTRG0#/ AN023	PDMDAT0
98		P006	PIO_006		GTCPPO5/ GTIOC13A/ GTIOC9B	SCK000-B/ CTS000#/ TXDB000	ET1_LINKSTA/ CAT1_LINKSTA		IRQ22-DS	ADTRG1#/ AN022	PDMCLK0/ PCOUTZ1
99		P005	PIO_005		GTCPPO4/ GTIOC12B/ GTIOC9A	RXD000-B/ SMISO000-B/ SSCL000/ SSILRCK1	ET1_MDIO-D/ CATLATCH0		IRQ21-DS	ADTRG2#/ AN021	DSM0_DAT2-B/ PCOUTB1
100		P004	PIO_004		GTCPPO3/ GTIOC12A/ GTIOC8B	TXD000-B/ SMOSI000-B/ SSDA000/ TXDA000/ SSITXD1	ET1_MDC-D/ CATSYNC0		IRQ20-DS	AN020	DSM0_CLK2-B/ PCOUTA1

2. Electrical Characteristics

2.1 Test Conditions

The supported peripheral functions and pins vary depending on the product model.
Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

- VCC = VCC_DCDC = VBATT = 1.62 to 3.63 V
- VCC2 = 1.62 to 3.63 V
- AVCC0 = 1.62 to 3.63 V
- VCC_USB = VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
- VREFH00/VREFH01/VREFH02/VREFH0 = 1.62 V to AVCC0
- VSS = VSS_DCDC = AVSS0 = VREFL00/VREFL01/VREFL02/VREFL0 = VSS_USB = VSS_USBHS = AVSS_USBHS = 0 V
- VCC voltage is lower than 2.7 V : LVOCR.LVO0E = 1, otherwise LVOCR.LVO0E = 0
- Tj = Topj
- V_{OH} = 0.7 × VCC/VCC2, V_{OL} = 0.3 ×VCC/VCC2
- V_{IH} = 0.7 × VCC/VCC2, V_{IL} = 0.3 ×VCC/VCC2
- Capacitive load C = 30 pF

2.1.1 Maximum and Minimum Values (Max./Min.)

Unless otherwise specified, minimum and maximum values are guaranteed by either design simulation, characterization results or test in production.

2.1.2 Typical Values (Typ.)

Unless otherwise specified, the following conditions were used in obtaining the typical (Typ.) values:

- Room temperature of 25°C
- VCC/VCC2 = VCC_DCDC = VCC_USB = VBATT = VCC_USBHS = AVCC_USBHS = AVCC0 = VREFH00/VREFH01/VREFH02/VREFH0 = 3.3 V

2.2 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Item			Symbol	Value	Unit
Power supply voltage			VCC, VCC2, VCC_DCDC	–0.3 to +4.0	V
External power supply voltage			VCL	–0.3 to +1.2	V
VBATT power supply voltage			V_{BATT}	–0.3 to +4.0	V
USB power supply voltage			VCC_USB	–0.3 to +4.0	V
USBHS power supply voltage			VCC_USBHS	–0.3 to +4.0	V
USBHS analog power supply voltage			AVCC_USBHS	–0.3 to +4.0	V
Analog power supply voltage			AVCC0	–0.3 to +4.0	V
Reference power supply voltage			VREFH00, VREFH01, VREFH02, VREFH0	–0.3 to AVCC0 + 0.3	V
Input voltage for port pins that are not 5-V tolerant	P000 to P015, P108 to P115, P208 to P215, P300 to P307, P315, P500 to P515, P700 to P715, P800 to P807, PA00 to PA07, PB00 to PB07, PC00 to PC07, PE00 to PE07, PF02 to PF09, PG00 to PG15		V_{in}	–0.3 to VCC + 0.3	V
	P309	EXCIN (when the VCC power supply is selected)		–0.3 to VCC + 0.3	
		EXCIN (when the VBATT power supply is selected)		–0.3 to VBATT + 0.3	
		Other than above		–0.3 to VCC + 0.3	
	P310, P311, P312	RTCICn (n = 0 to 2)		–0.3 to +3.9	
		Other than above		–0.3 to VCC + 0.3 (up to 3.9)	
	P600 to P607, P900 to P907, PD00 to PD07			–0.3 to VCC2 + 0.3	
	P400 to P415			–0.3 to AVCC0 + 0.3	
	PF00, PF01			–0.3 to VCC_USB + 0.3	
	USBHS_DP, USBHS_DM			–0.3 to VCC_USBHS + 0.3	
Input voltage for port pins that are 5-V tolerant	P100 to P107, P200 to P207		V_{in}	–0.3 to VCC + 3.6 (up to 5.8)	V
Analog input voltage	P400 to P415		V_{AN}	–0.3 to AVCC0 + 0.3	V
	P000 to P007	AVCC0 ≤ VCC		–0.3 to AVCC0 + 0.3	
		VCC < AVCC0		–0.3 to VCC + 0.3	
	P900 to P903, PD00 to PD07	AVCC0 ≤ VCC2		–0.3 to AVCC0 + 0.3	
		VCC2 < AVCC0		–0.3 to VCC2 + 0.3	
Junction temperature			T_j	–40 to +125	°C
Storage temperature			T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

2.3 Recommended Operating Conditions

Table 2.2 Recommended Operating Conditions (1)

Item			Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	When ESWM and SDRAM are not in use		VCC, VCC_DCDC	1.62	—	3.63	V
	When ESWM is in use			2.30	—	3.63	
	When SDRAM is in use			3.00	—	3.63	
	When ESWM and SDRAM are not in use		VCC2	1.62	—	3.63	
	When ESWM is in use*1			2.30	—	3.63	
	When SDRAM is in use*2			3.00	—	3.63	
	When external VDD is in use*3	Voltage range 1	VCL	0.920	0.950	0.990	
		Voltage range 2		0.870	0.925	0.990	
	When DCDC is in use	VSCR_1		—	0.950	—	
		VSCR_2		—	0.925	—	
		SVSCR_1		—	0.950	—	
		SVSCR_2		—	0.925	—	
		SVSCR_3		—	0.825	—	
		SVSCR_4		—	0.765		
		SVSCR_5		—	0.715	—	
			VSS, VSS_DCDC	—	0	—	
VBATT power supply voltage			V_{BATT}	1.62	—	3.63	V
USB power supply voltage	When USB is not in use		VCC_USB, VCC_USBHS, AVCC_USBHS	1.62	—	3.63	V
	When USB is in use			3.00	—	3.60	
			VSS_USB, VSS_USBHS, AVSS_USBHS	—	0	—	
Analog power supply voltage	Other than the following		AVCC0*4	1.62	—	3.63	V
	When sample-and-hold circuit is in use			2.70	—	3.63	
			AVSS0	—	0	—	

Note 1. When the pins for the ESWM with the VCC2 power supply are not in use, the voltage conditions differ from those when the ESWM is in use.
Note 2. When the pins for the SDRAM with the VCC2 power supply are not in use, the voltage conditions differ from those when the SDRAM is in use.
Note 3. Ensure that the VCL voltage is no higher than the VCC voltage.
Note 4. When the A/D converter, the D/A converter and the comparator are not in use, connect the AVCC0 and VREFH0 pins to VCC, and the AVSS0 and VREFL pins to VSS, respectively.

Table 2.3 Recommended Operating Conditions (2)

Item	Package	Symbol	Value	Required number of capacitors
Capacitance of a decoupling capacitor for stabilizing the internal voltage	BGA320	C_{VCL}	0.22 μF ± 30%	Nine or more
	BGA224			
	BGA176			
	LQFP176			Nine
	LQFP144			Eight
	LQFP100		0.47 μF ± 30%	Four

Note: Use a multilayer ceramic capacitor with a stated capacitance of 0.22 μF or 0.47μF and a capacitance tolerance within the range ±30%.

2.4 DC Characteristics

2.4.1 Characteristics of the Input Voltage of the I/O Pins

Table 2.4 Characteristics of the Input Voltage of the I/O Pins (V_{IH}/V_{IL}) (1/2)

Item		VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min.	Typ.	Max.	Unit
High- and low-level input voltage (except for Schmitt trigger input pins)	EXTAL (excluding usage with external clock input)	1.62 V or higher	V_{IH}	0.8 × VCC	—	—	V
			V_{IL}	—	—	0.2 × VCC	
	RSPI (excluding usage with RSPCK)*1	1.62 V or higher	V_{IH}	0.8 × VCC	—	—	
			V_{IL}	—	—	0.2 × VCC	
			V_{IH}	0.8 × VCC2	—	—	
			V_{IL}	—	—	0.2 × VCC2	
	XSPI*2	2.70 V or higher	V_{IH}	0.8 × VCC	—	—	
			V_{IL}	—	—	0.2 × VCC	
			V_{IH}	0.8 × VCC2	—	—	
			V_{IL}	—	—	0.2 × VCC2	
		1.70 V to 1.95 V	V_{IH}	0.7 × VCC	—	—	
			V_{IL}	—	—	0.3 × VCC	
			V_{IH}	0.7 × VCC2	—	—	
			V_{IL}	—	—	0.3 × VCC2	
	SDHI	2.70 V or higher	V_{IH}	0.625 × VCC	—	—	
			V_{IL}	—	—	0.25 × VCC	
			V_{IH}	0.625 × VCC2	—	—	
			V_{IL}	—	—	0.25 × VCC2	
		1.70 V to 1.95 V	V_{IH}	1.27	—	2	
			V_{IL}	—	—	0.58	
	MMC	2.70 V or higher	V_{IH}	0.625 × VCC	—	—	
			V_{IL}	—	—	0.25 × VCC	
			V_{IH}	0.625 × VCC2	—	—	
			V_{IL}	—	—	0.25 × VCC2	
		1.70 V to 1.95 V	V_{IH}	0.65 × VCC	—	—	
			V_{IL}	—	—	0.35 × VCC	
			V_{IH}	0.65 × VCC2	—	—	
			V_{IL}	—	—	0.35 × VCC2	
	D0 to D31, BREQ#, WAIT#	3.00 V or higher	V_{IH}	0.7 × VCC	—	—	
			V_{IL}	—	—	0.3 × VCC	
			V_{IH}	0.7 × VCC2	—	—	
			V_{IL}	—	—	0.3 × VCC2	
	RIICHS (SMBus)*3	2.70 V or higher	V_{IH}	2.3	—	—	
			V_{IL}	—	—	0.8	
	RI3C (SMBus)*4	2.70 V or higher	V_{IH}	2.3	—	—	
			V_{IL}	—	—	0.8	
	ESWM(MII*5), ESWM(RMII*6), ESC*7	2.70 V to 3.60 V	V_{IH}	2.3	—	—	
			V_{IL}	—	—	0.2 × VCC	
			V_{IH}	2.3	—	—	
			V_{IL}	—	—	0.2 × VCC2	
	ESWM(GMII*8), ESWM(RGMII*9)	3.00 V to 3.60 V	V_{IH}	2	—	—	
			V_{IL}	—	—	0.8	
		2.30 V to 2.70 V	V_{IH}	1.7	—	—	
			V_{IL}	—	—	0.7	

Table 2.4 Characteristics of the Input Voltage of the I/O Pins (V_{IH}/V_{IL}) (2/2)

Item		VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min.	Typ.	Max.	Unit
High- and low-level input voltage (except for Schmitt trigger input pins)	ESWM*10, ESC*11	2.30 V to 3.60 V	V_{IH}	0.7 × VCC	—	—	V
			V_{IL}	—	—	0.3 × VCC	
			V_{IH}	0.7 × VCC2	—	—	
			V_{IL}	—	—	0.3 × VCC2	
	RTCIC0, RTCIC1, RTCIC2 (when the VCC power supply is selected)	1.62 V or higher	V_{IH}	0.9	—	—	
			V_{IL}	—	—	0.3	
	RTCIC0, RTCIC1, RTCIC2 (when the VBATT power supply is selected)		V_{IH}	0.9	—	—	
			V_{IL}	—	—	0.3	
	EXCIN (when the VCC power supply is selected)	1.62 V or higher	V_{IH}	0.9	—	—	
			V_{IL}	—	—	0.3	
	EXCIN (when the VBATT power supply is selected)		V_{IH}	0.9	—	—	
			V_{IL}	—	—	0.3	
Schmitt trigger input voltage (for the peripheral function pins)	RIICHS input pins (except for SMBus)*3	1.62 V or higher	V_{IH}	0.7 × VCC	—	—	V
			V_{IL}	—	—	0.3 × VCC	
			ΔV_T	0.05 × VCC	—	—	
	RI3C input pins (I3C mode)*4	1.65 V to 1.95 V 2.97 V to 3.63 V	V_{IH}	0.7 × VCC	—	—	
			V_{IL}	—	—	0.3 × VCC	
			ΔV_T	0.1 × VCC	—	—	
	RI3C input pins (I^2C mode excluding SMBus operation)*4	1.62 V or higher	V_{IH}	0.7 × VCC	—	—	
			V_{IL}	—	—	0.3 × VCC	
			ΔV_T	0.1 × VCC	—	—	
	5-V tolerant port pins*12	1.62 V or higher	V_{IH}	0.8 × VCC	—	—	
			V_{IL}	—	—	0.2 × VCC	
			ΔV_T	0.05 × VCC	—	—	
	Other pins in the VCC power domain	1.62 V or higher	V_{IH}	0.8 × VCC	—	—	
			V_{IL}	—	—	0.2 × VCC	
			ΔV_T	0.05 × VCC	—	—	
	Other pins in the VCC2 power domain	1.62 V or higher	V_{IH}	0.8 × VCC2	—	—	
			V_{IL}	—	—	0.2 × VCC2	
			ΔV_T	0.05 × VCC2	—	—	
	Other pins in the AVCC0 power domain	1.62 V or higher	V_{IH}	0.8 × AVCC0	—	—	
			V_{IL}	—	—	0.2 × AVCC0	
			ΔV_T	0.05 × AVCC0	—	—	
	Other pins in the VCC_USB power domain	1.62 V or higher	V_{IH}	0.8 × VCC_USB	—	—	
			V_{IL}	—	—	0.2 × VCC_USB	
			ΔV_T	0.05 × VCC_USB	—	—	
Schmitt trigger input voltage (for the port pins)	5-V tolerant port pins*12	1.62 V or higher	V_{IH}	0.8 × VCC	—	—	V
			V_{IL}	—	—	0.2 × VCC	
	Other pins in the VCC power domain	1.62 V or higher	V_{IH}	0.8 × VCC	—	—	
			V_{IL}	—	—	0.2 × VCC	
	Other pins in the VCC2 power domain	1.62 V or higher	V_{IH}	0.8 × VCC2	—	—	
			V_{IL}	—	—	0.2 × VCC2	
	Other pins in the AVCC0 power domain	1.62 V or higher	V_{IH}	0.8 × AVCC0	—	—	
			V_{IL}	—	—	0.2 × AVCC0	
	Other pins in the VCC_USB power domain	1.62 V or higher	V_{IH}	0.8 × VCC_USB	—	—	
			V_{IL}	—	—	0.2 × VCC_USB	
	Other pins in the VBATT power domain	1.62 V or higher	V_{IH}	0.8 × VCC	—	VCC	
			V_{IL}	—	—	0.2 × VCC	

Note 1. MOSIn, MISOn, SSLn0 (n = A, B, C)
Note 2. XSPIn_IOx, XSPIn_DS, XSPIn_CK, XSPIn_CS0# (n = 0, 1; x = 0 to 7)
Note 3. SDAHSn-A, SCLHSn-A (n = 1, 2)
Note 4. SDA00-A, SCL00-A
Note 5. ETn_RX_CLK, ETn_RX_DV, ETn_RXD0, ETn_RXD1, ETn_RXD2, ETn_RXD3, ETn_RX_ER, ETn_TX_CLK, ETn_CRS, ETn_COL (n = 0, 1)
Note 6. RMIIn_REF50CK, RMIIn_CRS_DV, RMIIn_RXD0, RMIIn_RXD1, RMIIn_RX_ER (n = 0, 1)
Note 7. CATn_RX_CLK, CATn_RX_DV, CATn_ERXD0, CATn_ERXD1, CATn_ERXD2, CATn_ERXD3, CATn_RX_ER, CATn_TX_CLK (n = 0, 1)
Note 8. ETn_RX_CLK-A, ETn_RX_DV-A, ETn_RX_ER-A, ETn_RXD0-A, ETn_RXD1-A, ETn_RXD2-A, ETn_RXD3-A, ETn_RXD4-A, ETn_RXD5-A, ETn_RXD6-A, ETn_RXD7-A, ETn_TX_CLK-A (n = 0, 1)
Note 9. RGMIIn_RX_CTL-A, RGMIIn_RXC-A, RGMIIn_RXD0-A, RGMIIn_RXD1-A, RGMIIn_RXD2-A, RGMIIn_RXD3-A (n = 0, 1)
Note 10. GPTP_CAPTUREn, ETn_LINKSTA, ETn_MDIO, ETn_INT (n = 0, 1)
Note 11. CATn_LINKSTA, CAT0_MDIO, CATI2CDATA, CATLATCHn (n = 0, 1)
Note 12. P100 to P107 and P200 to P207 are 5-V tolerant.

2.4.2 Characteristics of the Output Voltage of the I/O Pins

Table 2.5 Characteristics of the Output Voltage of the I/O Pins (V_{OH}/V_{OL}) (1) (1/3)

Item		VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
High-level output voltage	RI3C*1	2.97 V to 3.63 V	V_{OH}	VCC – 0.27	—	—	V	I_{OH} = 3.0 mA (PRTS.PRTMD = 0, BFCTL.FMPE = 0, BFCTL.HSME = 0)
		1.65 V to 1.95 V		VCC – 0.27	—	—		
	ESWM	2.70 V to 3.60 V	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1.0 mA
				VCC2 – 0.5	—	—		
		2.30 V to 2.70 V		2	—	—		
	SDHI	2.70 V or higher	V_{OH}	0.75 × VCC	—	—	V	I_{OH} = –2.0 mA
				0.75 × VCC2	—	—		
		1.70 V to 1.95 V		1.4	—	—		
	MMC	2.70 V or higher	V_{OH}	0.75 × VCC	—	—	V	I_{OH} = –0.1 mA
				0.75 × VCC2	—	—		
		1.70 V to 1.95 V		VCC – 0.45	—	—		I_{OH} = –2.0 mA
				VCC2 – 0.45	—	—		
	Other output pins		V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1.0 mA
				VCC2 – 0.5	—	—		
				AVCC0 – 0.5	—	—		
				VCC_USB – 0.5	—	—		
Low-level output voltage	RIICHS output pins*2	2.70 V or higher	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA (ICFER.FMPE = 0, ICFER.HSME = 0)
				—	—	0.6		I_{OL} = 6 mA (ICFER.FMPE = 0, ICFER.HSME = 0)
				—	—	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
				—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
		1.62 V to 1.95 V		—	—	0.2 × VCC		I_{OL} = 2 mA (ICFER.FMPE = 0, ICFER.HSME = 0)
				—	—	0.4		I_{OL} = 3 mA (ICFER.FMPE = 0, ICFER.HSME = 0)
				—	—	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1, ICFER.HSME = 0)
				—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1, ICFER.HSME = 0)
				—	—	0.2 × VCC		I_{OL} = 3 mA (ICFER.FMPE = 0, ICFER.HSME = 1)

Table 2.5 Characteristics of the Output Voltage of the I/O Pins (V_{OH}/V_{OL}) (1) (2/3)

Item		VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Low-level output voltage	RI3C*1	2.97 V or higher	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA (ICMR.OMS = 1, ICFER.FMPE = 0, ICFER.HSME = 1)
				—	—	0.27		I_{OL} = 3.0 mA (ICMR.OMS = 0, ICFER.FMPE = 0, ICFER.HSME = 0)
		2.70 V or higher		—	—	0.4	V	I_{OL} = 3.0 mA (ICMR.OMS = 1, ICFER.FMPE = 0, ICFER.HSME = 0)
				—	—	0.6		I_{OL} = 6.0 mA (ICMR.OMS = 1, ICFER.FMPE = 0, ICFER.HSME = 0)
				—	—	0.4		I_{OL} = 15.0 mA (ICMR.OMS = 1, ICFER.FMPE = 1, ICFER.HSME = 0)
				—	0.4	—		I_{OL} = 20.0 mA (ICMR.OMS = 1, ICFER.FMPE = 1, ICFER.HSME = 0)
		1.62 V to 1.95 V		—	—	0.2 × VCC	V	I_{OL} = 2.0 mA (ICMR.OMS = 1, ICFER.FMPE = 0, ICFER.HSME = 0)
				—	—	0.4		I_{OL} = 3.0 mA (ICMR.OMS = 1, ICFER.FMPE = 0, ICFER.HSME = 0)
				—	—	0.6		I_{OL} = 6.0 mA (ICMR.OMS = 1, ICFER.FMPE = 0, ICFER.HSME = 0)
				—	—	0.2 × VCC		I_{OL} = 2.0 mA (ICMR.OMS = 1, ICFER.FMPE = 1, ICFER.HSME = 0)
				—	—	0.4		I_{OL} = 15.0 mA (ICMR.OMS = 1, ICFER.FMPE = 1, ICFER.HSME = 0)
				—	0.4	—		I_{OL} = 20.0 mA (ICMR.OMS = 1, ICFER.FMPE = 1, ICFER.HSME = 0)
				—	—	0.2 × VCC		I_{OL} = 3.0 mA (ICMR.OMS = 1, ICFER.FMPE = 0, ICFER.HSME = 1)
		1.65 V to 1.95 V		—	—	0.27		I_{OL} = 3.0 mA (ICMR.OMS = 0, ICFER.FMPE = 0, ICFER.HSME = 0)
	ESWM		V_{OL}	—	—	0.4	V	I_{OL} = 1.0 mA

Table 2.5 Characteristics of the Output Voltage of the I/O Pins (V_{OH}/V_{OL}) (1) (3/3)

Item		VCC/VCC2/ AVCC0/ VCC_USB	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Low-level output voltage	SDHI	2.70 V or higher	V_{OL}	—	—	0.125 × VCC	V	I_{OL} = 2.0 mA
				—	—	0.125 × VCC2		
		1.70 V to 1.95 V		—	—	0.45		I_{OL} = 2.0 mA
	MMC	2.70 V or higher	V_{OL}	—	—	0.125 × VCC	V	I_{OL} = 0.1 mA
				—	—	0.125 × VCC2		I_{OL} = 0.1 mA
		1.70 V to 1.95 V		—	—	0.45		I_{OL} = 2.0 mA
	Other output pins		V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
				—	—	0.5		
				—	—	0.5		
				—	—	0.5		

Note 1. This specification applies to SDA00-A and SCL00-A.
Note 2. This specification applies to SCLHS1-A, SDAHS1-A, SCLHS2-A, and SDAHS2-A.

Table 2.6 Characteristics of the Output Voltage of the I/O Pins (V_{OH}/V_{OL}) (2) (1/3)

Item		Power supply voltage	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
High-level output voltage	DRV1*1	3.3 V	V_{OH}	—	3.15	—	V	I_{OH} = –1 mA
				—	3.00	—		I_{OH} = –2 mA
				—	2.70	—		I_{OH} = –4 mA
				—	2.10	—		I_{OH} = –8 mA
				—	1.05	—		I_{OH} = –15 mA
	DRV2*1	3.3 V	V_{OH}	—	3.23	—	V	I_{OH} = –1 mA
				—	3.15	—		I_{OH} = –2 mA
				—	3.00	—		I_{OH} = –4 mA
				—	2.70	—		I_{OH} = –8 mA
				—	2.18	—		I_{OH} = –15 mA
	DRV3*1	3.3 V	V_{OH}	—	3.25	—	V	I_{OH} = –1 mA
				—	3.20	—		I_{OH} = –2 mA
				—	3.10	—		I_{OH} = –4 mA
				—	2.90	—		I_{OH} = –8 mA
				—	2.55	—		I_{OH} = –15 mA
	DRV4*1	3.3 V	V_{OH}	—	3.27	—	V	I_{OH} = –1 mA
				—	3.24	—		I_{OH} = –2 mA
				—	3.18	—		I_{OH} = –4 mA
				—	3.06	—		I_{OH} = –8 mA
				—	2.85	—		I_{OH} = –15 mA
		1.8 V		—	1.75	—		I_{OH} = –1 mA
				—	1.70	—		I_{OH} = –2 mA
				—	1.60	—		I_{OH} = –4 mA
				—	1.40	—		I_{OH} = –8 mA
				—	1.05	—		I_{OH} = –15 mA
	DRV5*1	3.3 V	V_{OH}	—	3.26	—	V	I_{OH} = –1 mA
				—	3.23	—		I_{OH} = –2 mA
				—	3.16	—		I_{OH} = –4 mA
				—	3.01	—		I_{OH} = –8 mA
				—	2.76	—		I_{OH} = –15 mA

Table 2.6 Characteristics of the Output Voltage of the I/O Pins (V_{OH}/V_{OL}) (2) (2/3)

Item		Power supply voltage	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
High-level output voltage	DRV6*1	3.3 V	V_{OH}	—	3.28	—	V	I_{OH} = –1 mA
				—	3.25	—		I_{OH} = –2 mA
				—	3.20	—		I_{OH} = –4 mA
				—	3.11	—		I_{OH} = –8 mA
				—	2.94	—		I_{OH} = –15 mA
	DRV7*1	3.3 V	V_{OH}	—	3.28	—	V	I_{OH} = –1 mA
				—	3.26	—		I_{OH} = –2 mA
				—	3.22	—		I_{OH} = –4 mA
				—	3.14	—		I_{OH} = –8 mA
				—	3.00	—		I_{OH} = –15 mA
		2.5 V		—	2.45	—		I_{OH} = –1 mA
				—	2.40	—		I_{OH} = –2 mA
				—	2.30	—		I_{OH} = –4 mA
				—	2.10	—		I_{OH} = –8 mA
				—	1.75	—		I_{OH} = –15 mA
	DRV8*1	3.3 V	V_{OH}	—	3.28	—	V	I_{OH} = –1 mA
				—	3.25	—		I_{OH} = –2 mA
				—	3.20	—		I_{OH} = –4 mA
				—	3.11	—		I_{OH} = –8 mA
				—	2.94	—		I_{OH} = –15 mA
		1.8 V		—	1.79	—		I_{OH} = –1 mA
				—	1.77	—		I_{OH} = –2 mA
				—	1.75	—		I_{OH} = –4 mA
				—	1.70	—		I_{OH} = –8 mA
				—	1.61	—		I_{OH} = –15 mA
Low-level output voltage	DRV1*1	3.3 V	V_{OL}	—	0.15	—	V	I_{OL} = 1 mA
				—	0.30	—		I_{OL} = 2 mA
				—	0.60	—		I_{OL} = 4 mA
				—	1.20	—		I_{OL} = 8 mA
				—	2.25	—		I_{OL} = 15 mA
	DRV2*1	3.3 V	V_{OL}	—	0.08	—	V	I_{OL} = 1 mA
				—	0.15	—		I_{OL} = 2 mA
				—	0.30	—		I_{OL} = 4 mA
				—	0.60	—		I_{OL} = 8 mA
				—	1.13	—		I_{OL} = 15 mA
	DRV3*1	3.3 V	V_{OL}	—	0.05	—	V	I_{OL} = 1 mA
				—	0.10	—		I_{OL} = 2 mA
				—	0.20	—		I_{OL} = 4 mA
				—	0.40	—		I_{OL} = 8 mA
				—	0.75	—		I_{OL} = 15 mA
	DRV4*1	3.3 V	V_{OL}	—	0.03	—	V	I_{OL} = 1 mA
				—	0.06	—		I_{OL} = 2 mA
				—	0.12	—		I_{OL} = 4 mA
				—	0.24	—		I_{OL} = 8 mA
				—	0.45	—		I_{OL} = 15 mA
		1.8 V		—	0.05	—		I_{OL} = 1 mA
				—	0.10	—		I_{OL} = 2 mA
				—	0.20	—		I_{OL} = 4 mA
				—	0.40	—		I_{OL} = 8 mA
				—	0.75	—		I_{OL} = 15 mA

Table 2.6 Characteristics of the Output Voltage of the I/O Pins (V_{OH}/V_{OL}) (2) (3/3)

Item		Power supply voltage	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Low-level output voltage	DRV5*1	3.3 V	V_{OL}	—	0.04	—	V	I_{OL} = 1 mA
				—	0.07	—		I_{OL} = 2 mA
				—	0.14	—		I_{OL} = 4 mA
				—	0.29	—		I_{OL} = 8 mA
				—	0.54	—		I_{OL} = 15 mA
	DRV6*1	3.3 V	V_{OL}	—	0.02	—	V	I_{OL} = 1 mA
				—	0.05	—		I_{OL} = 2 mA
				—	0.10	—		I_{OL} = 4 mA
				—	0.19	—		I_{OL} = 8 mA
				—	0.36	—		I_{OL} = 15 mA
	DRV7*1	3.3 V	V_{OL}	—	0.02	—	V	I_{OL} = 1 mA
				—	0.04	—		I_{OL} = 2 mA
				—	0.08	—		I_{OL} = 4 mA
				—	0.16	—		I_{OL} = 8 mA
				—	0.30	—		I_{OL} = 15 mA
		2.5 V		—	0.05	—		I_{OL} = 1 mA
				—	0.10	—		I_{OL} = 2 mA
				—	0.20	—		I_{OL} = 4 mA
				—	0.40	—		I_{OL} = 8 mA
				—	0.75	—		I_{OL} = 15 mA
	DRV8*1	3.3 V	V_{OL}	—	0.02	—	V	I_{OL} = 1 mA
				—	0.05	—		I_{OL} = 2 mA
				—	0.10	—		I_{OL} = 4 mA
				—	0.19	—		I_{OL} = 8 mA
				—	0.36	—		I_{OL} = 15 mA
		1.8 V		—	0.01	—		I_{OL} = 1 mA
				—	0.03	—		I_{OL} = 2 mA
				—	0.05	—		I_{OL} = 4 mA
				—	0.10	—		I_{OL} = 8 mA
				—	0.20	—		I_{OL} = 15 mA

Note 1. This is the driving ability as selected by the setting of the driving ability select (PmnPFS.DSCR[3:0]) bits.

2.4.3 Characteristics of the Other I/O Pins

Table 2.7 Characteristics of the Other I/O Pins

Item		Power supply voltage	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES# pin		$\lvert I_{in} \rvert$	—	—	5	μA	V_{in} = 0 V, V_{in} = 5.5 V
	NMI, XCIN, and XCOUT pins			—	—	1		V_{in} = 0 V, V_{in} = VCC
Three-state leakage current (off state)	Other than ports for 5-V tolerant		$\lvert I_{TSI} \rvert$	—	—	1	μA	V_{in} = 0 V, V_{in} = VCC, VCC2, AVCC0, VCC_USB
	Ports for 5-V tolerant*1			—	—	5		V_{in} = 0 V, V_{in} = 5.5 V
Input pull-up resistor current*2		2.70 V or higher	I_p	–300	—	–10	μA	VCC, VCC2, AVCC0, VCC_USB = 2.7 to 3.63 V V_{in} = 0 V
		1.62 V or higher		–300	—	–5		VCC, VCC2, AVCC0, VCC_USB = 1.62 to 3.63 V V_{in} = 0 V
Input capacitance	P414, P415		C_{in}	—	—	16	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	PF00, PF01, USB_DP, USB_DM			—	—	12		
	P102, P103, P106, P107, P200, P201			—	—	10		
	USBHS_DP, USBHS_DM			—	—	10		
	Other input pins			—	—	8		

Note 1. P100 to P107 and P200 to P207 are 5-V tolerant.
Note 2. The values are for pins excluding USB_DP, USB_DM, USBHS_DP, USBHS_DM, SDA00-A, SCL00-A, SDAHSn-A, and SCLHSn-A (n = 1, 2).

2.4.4 Operating and Standby Currents

The operating current and standby current depend on the product part number.
For the current characteristics of the products with part numbers of the form R5K574Mxy4xx (y = A, B, C, D, T, U, V, W), see section 2.4.4.1, Operating and Standby Currents for Product Part No. R5K574Mxy4xx (y = A, B, C, D, T, U, V, W).
For the current characteristics of the products with part numbers of the form R5K574Mxy4xx (y = E, F), see section 2.4.4.2, Operating and Standby Currents for Product Part No. R5K574Mxy4xx (y = E, F).
Unless otherwise specified, the supply current values were measured with all output pins load-free and all input pull-up resistors disabled.
The values for current given or used in this section do not include the current supplied for background operation (BGO).
The VCC current includes the VCC2 power supply current.

The currents were measured with the operating frequencies specified as shown in Table 2.8.

Table 2.8 Frequency Settings for the Individual Clocks

Item		ICLK	MRICLK	MRPCLK	BCLK	PCLKA	PCLKB, PCLKC	PCLKD	PCLKE	Unit
When the peripheral clock supplies are stopped*1	Frequency setting 1 (CPUCLK0 = 600 MHz)	300	300	150	Stopped	Stopped	Stopped	Stopped	Stopped	MHz
	Frequency setting 2 (CPUCLK0 = 480 MHz)	240	240	120	Stopped	Stopped	Stopped	Stopped	Stopped	
	Frequency setting 3 (CPUCLK0 = 300 MHz)	300	300	150	Stopped	Stopped	Stopped	Stopped	Stopped	
Other cases	Frequency setting 1 (CPUCLK0 = 600 MHz)	300	300	150	150	150	75	150	300	
	Frequency setting 2 (CPUCLK0 = 480 MHz)	240	240	120	120	120	60	120	240	
	Frequency setting 3 (CPUCLK0 = 300 MHz)	300	300	150	150	150	75	150	300	

Note 1. The frequencies of the clocks in the table are set for division by 64 in the SCKDIVCR register when the peripheral clock supplies are stopped.

The symbols shown in Figure 2.1, Supply Current Measurement Diagram (DCDC Mode), and Figure 2.2, Supply Current Measurement Diagram (LDO Mode), are used in the tables that follow the figures.

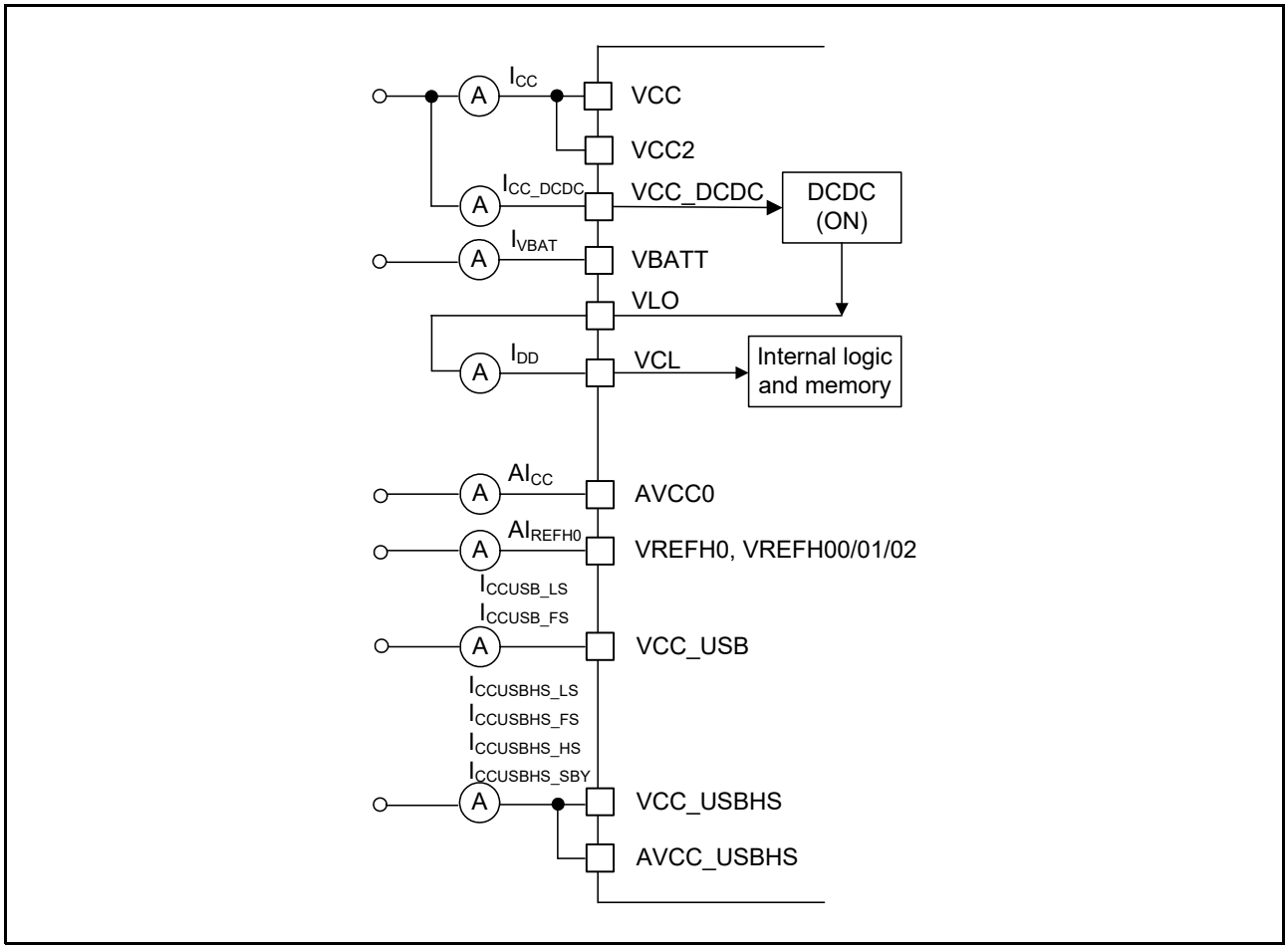


Figure 2.1 Supply Current Measurement Diagram (DCDC Mode)

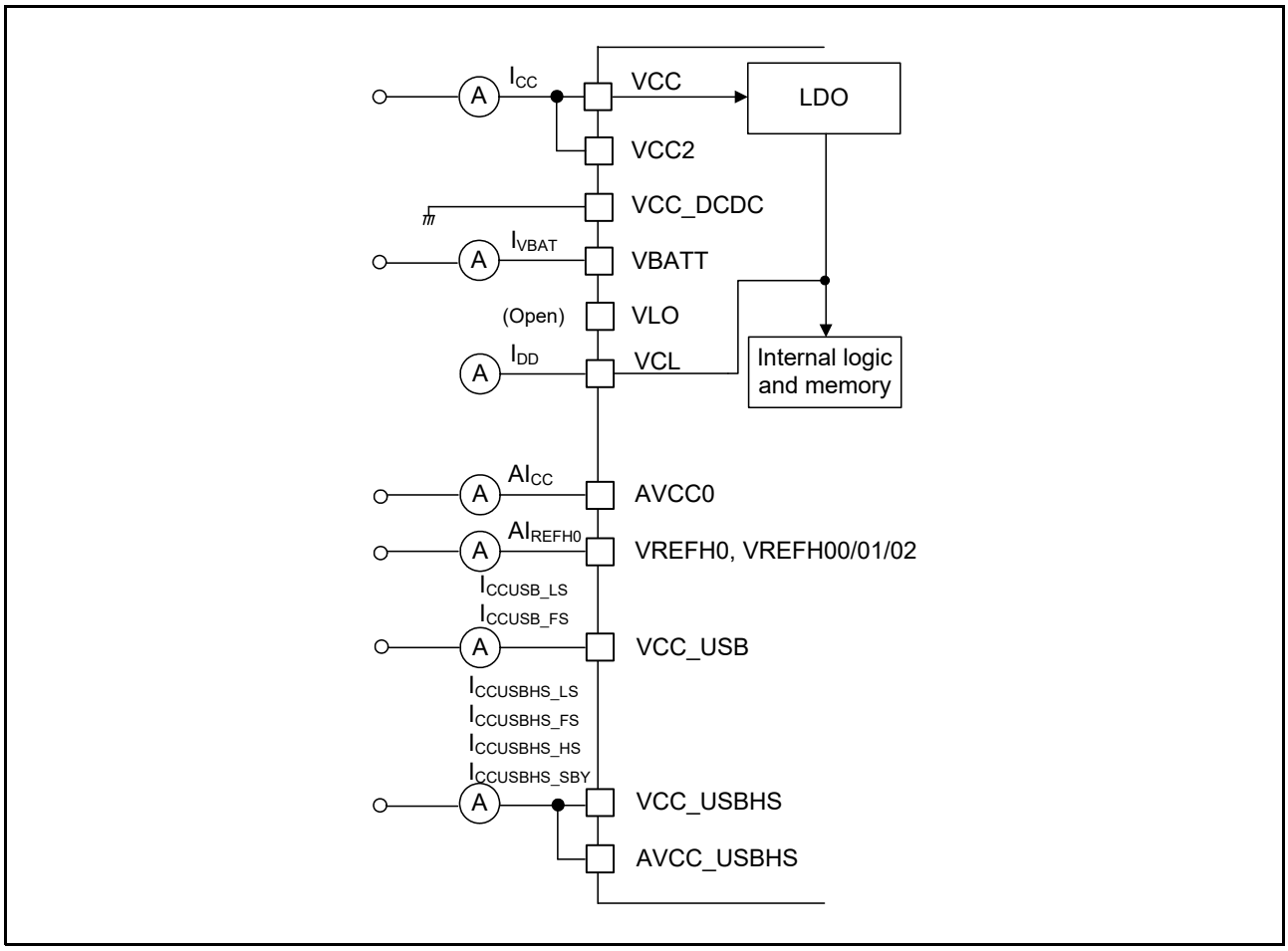


Figure 2.2 Supply Current Measurement Diagram (LDO Mode)

When the DCDC is in use, the efficiency of power conversion depends on the load currents, temperature, and VCC voltage. For reference, the results of conversion efficiency simulation are shown in Figure 2.3 to Figure 2.5.

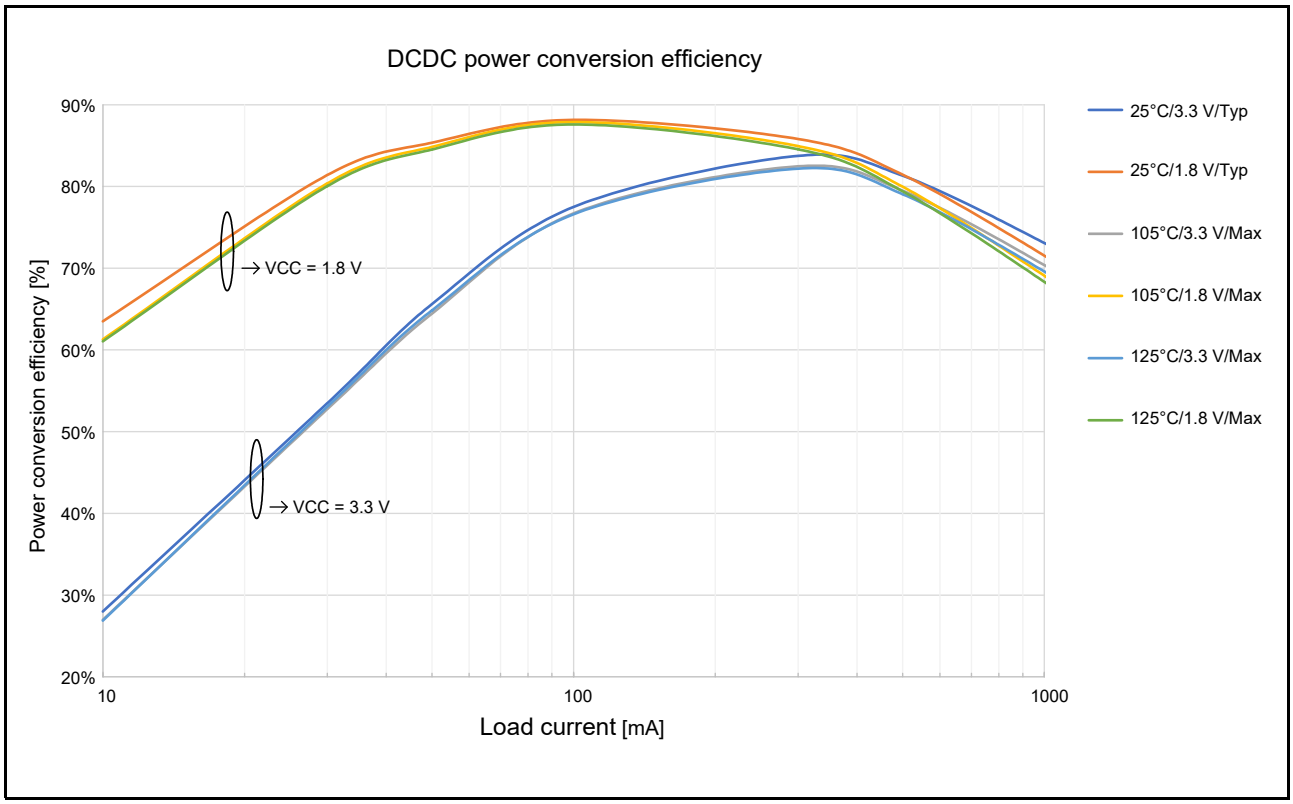


Figure 2.3 DCDC Power Conversion Efficiency in Normal Mode and Software Standby Mode (SSCR1.SS2LP = SS2LP_0) (Reference: Simulated Values)

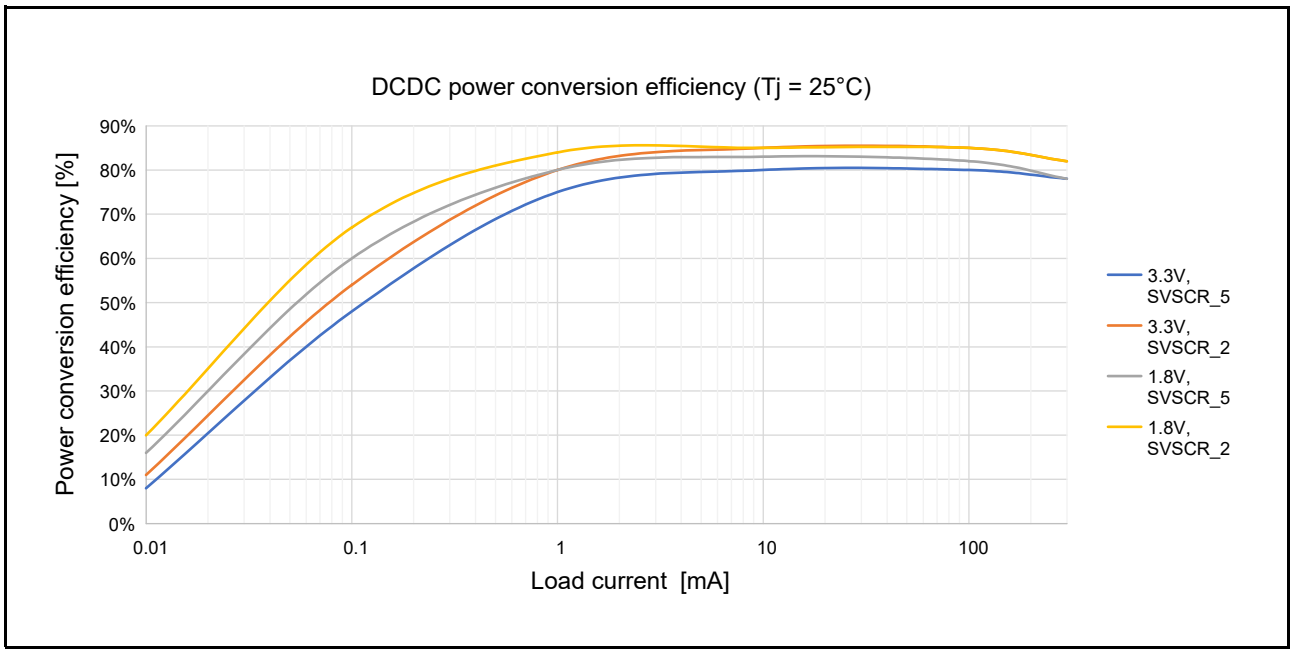


Figure 2.4 DCDC Power Conversion Efficiency in Software Standby Mode (SSCR1.SS2LP = SS2LP_1) at Tj = 25°C (Reference: Simulated Values)

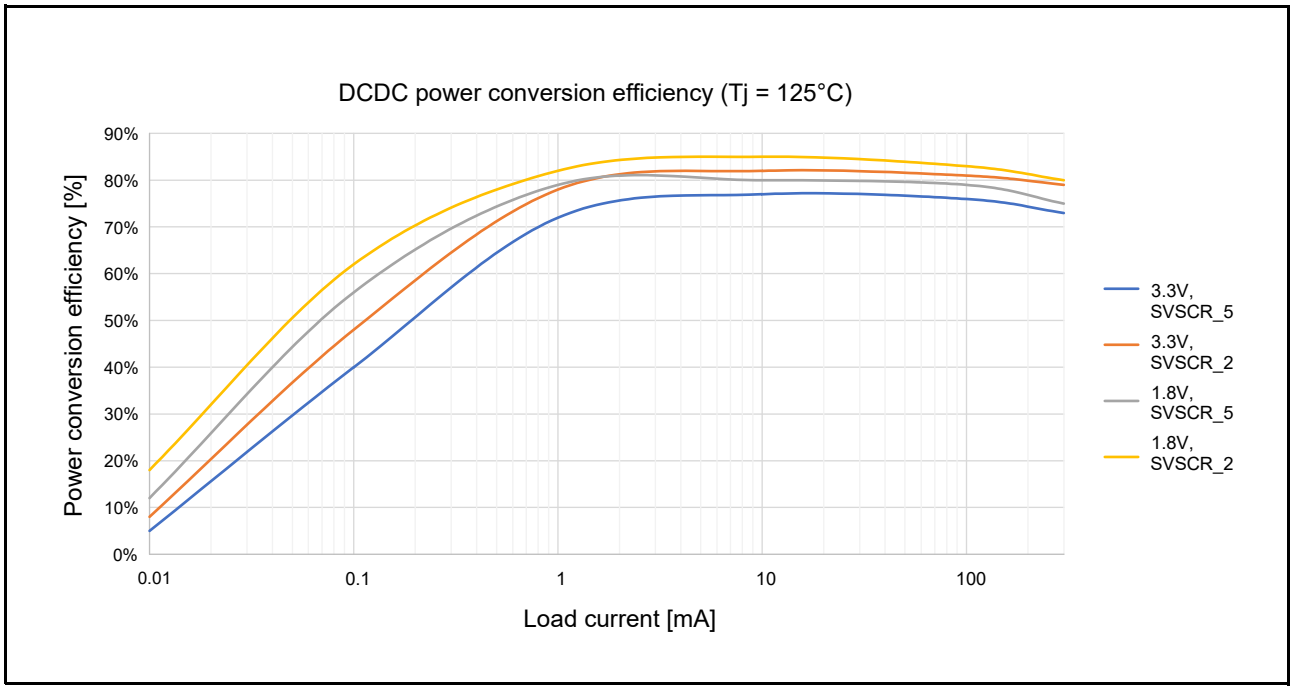


Figure 2.5 DCDC Power Conversion Efficiency in Software Standby Mode (SSCR1.SS2LP = SS2LP_1) at Tj = 125°C (Reference: Simulated Values)

2.4.4.1 Operating and Standby Currents for Product Part No. R5K574Mxy4xx (y = A, B, C, D, T, U, V, W)

Table 2.9 Supply Currents for Full Operation (DCDC Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max.*2 (Tj = 125°C)	Unit	Test Conditions
Supply current (full operation)	VCC_DCDC ≥ 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{CC_DCDC} *1	88	217	307	mA	VSCR_1 (VCL = 0.95 V) VCC_DCDC = 3.3 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		68	181	262		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		68	180	261		
	VCC_DCDC < 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)		153	396	568		VSCR_1 (VCL = 0.95 V) VCC_DCDC = 1.8 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		116	329	482		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		115	329	482		
	VCC current		I_{CC}	11	15	17		VCC = 3.3 V

Note: This table lists the values for current under the following operating conditions.
- The internal memory (SRAM and MRAM) is configured with wait settings that suit the operating frequency and kept as active as is possible through data transfer by the DMAC.
- The peripheral functions are supplied with clocks and kept as active as is possible.
- Unless otherwise specified, the clocks are set to the states that maximize the supply currents within the limits imposed by the specifications.
- The program is placed in the LRAM, the cache is enabled, and the CPU repeatedly executes multiply-and-accumulate instructions.
- Power to the ESWM domain is turned on.

Note 1. Value for I_{CC_DCDC} can be estimated by using the following formulae (units: I_{CC_DCDC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).

[When VCC_DCDC = 3.3 V]

I_{CC_DCDC} Typ.(VSCR_1) = 0.0498 × $f_{CPUCLK0}$ + 0.0895 × f_{ICLK} + 30.84
I_{CC_DCDC} Typ.(VSCR_2) = 0.0512 × $f_{CPUCLK0}$ + 0.0633 × f_{ICLK} + 28.49
I_{CC_DCDC} Max.(VSCR_1, 105°C) = 0.0654 × $f_{CPUCLK0}$ + 0.1276 × f_{ICLK} + 139.00
I_{CC_DCDC} Max.(VSCR_1, 125°C) = 0.0716 × $f_{CPUCLK0}$ + 0.1305 × f_{ICLK} + 225.16
I_{CC_DCDC} Max.(VSCR_2, 105°C) = 0.0604 × $f_{CPUCLK0}$ + 0.0810 × f_{ICLK} + 132.18
I_{CC_DCDC} Max.(VSCR_2, 125°C) = 0.0679 × $f_{CPUCLK0}$ + 0.0907 × f_{ICLK} + 207.32

[When VCC_DCDC = 1.8 V]

I_{CC_DCDC} Typ.(VSCR_1) = 0.0974 × $f_{CPUCLK0}$ + 0.1756 × f_{ICLK} + 42.07
I_{CC_DCDC} Typ.(VSCR_2) = 0.0927 × $f_{CPUCLK0}$ + 0.1180 × f_{ICLK} + 43.29
I_{CC_DCDC} Max.(VSCR_1, 105°C) = 0.1223 × $f_{CPUCLK0}$ + 0.2385 × f_{ICLK} + 251.34
I_{CC_DCDC} Max.(VSCR_1, 125°C) = 0.1363 × $f_{CPUCLK0}$ + 0.2484 × f_{ICLK} + 411.75
I_{CC_DCDC} Max.(VSCR_2, 105°C) = 0.1157 × $f_{CPUCLK0}$ + 0.1521 × f_{ICLK} + 237.43
I_{CC_DCDC} Max.(VSCR_2, 125°C) = 0.1280 × $f_{CPUCLK0}$ + 0.1714 × f_{ICLK} + 379.37

However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 2. For the LQFP100 package (products with part numbers of the form R5K574MxxxFP), control the number of peripheral functions to ensure that the maximum current does not exceed 710 mA (see section 2.4.5.2, Supply Currents for the Peripheral Functions).

Table 2.10 Supply Currents for Full Operation (External VDD Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max.*2 (Tj = 125°C)	Unit	Test Conditions
Supply current (full operation)	VCL = 0.92 to 0.99 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{DD}*1	256	597	800	mA	Voltage range 1 (VCL = 0.95 V)
	VCL = 0.87 to 0.99 V	Frequency setting 2 (CPUCLK0 = 480 MHz)		202	524	719		Voltage range 2 (VCL = 0.925 V)
		Frequency setting 3 (CPUCLK0 = 300 MHz)		201	523	718		
	VCC current		I_{CC}	11	15	17		VCC = 3.3 V

Note: This table lists the values for current under the following operating conditions.
- Unless otherwise specified, the clocks are set to the states that maximize the supply currents within the limits imposed by the specifications.
- The program is placed in the LRAM, the cache is enabled, and the CPU repeatedly executes multiply-and-accumulate instructions.
- The internal memory (SRAM and MRAM) is configured with wait settings that suit the operating frequency and kept as active as is possible through data transfer by the DMAC.
- Power to the ESWM domain is turned on.

Note 1. Value for I_{DD} can be estimated by using the following formulae (units: I_{DD} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).

I_{DD} Typ.(VCL = 0.92 to 0.99 V) = 0.1584 × $f_{CPUCLK0}$ + 0.2852 × f_{ICLK} + 75.36
I_{DD} Typ.(VCL = 0.87 to 0.99 V) = 0.1588 × $f_{CPUCLK0}$ + 0.2007 × f_{ICLK} + 77.55
I_{DD} Max.(VCL = 0.92 to 0.99 V, 105°C) = 0.1600 × $f_{CPUCLK0}$ + 0.3120 × f_{ICLK} + 407.46
I_{DD} Max.(VCL = 0.92 to 0.99 V, 125°C) = 0.1565 × $f_{CPUCLK0}$ + 0.2849 × f_{ICLK} + 620.60
I_{DD} Max.(VCL = 0.87 to 0.99 V, 105°C) = 0.1622 × $f_{CPUCLK0}$ + 0.2122 × f_{ICLK} + 394.73
I_{DD} Max.(VCL = 0.87 to 0.99 V, 125°C) = 0.1615 × $f_{CPUCLK0}$ + 0.2126 × f_{ICLK} + 590.17

However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 2. For the LQFP100 package (products with part numbers of the form R5K574MxxxFP), control the number of peripheral functions to ensure that the maximum current does not exceed 718 mA (see section 2.4.5.2, Supply Currents for the Peripheral Functions).

Table 2.11 Supply Currents for Maximum Data Processing with the Peripheral Clock Supplies Stopped (DCDC Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
Supply current (maximum data processing with the peripheral clock supplies stopped)	VCC_DCDC ≥ 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{CC_DCDC} *1	41	165	254	mA	VSCR_1 (VCL = 0.95 V) VCC_DCDC = 3.3 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		33	144	225		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		28	138	218		
	VCC_DCDC < 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)		66	299	467		VSCR_1 (VCL = 0.95 V) VCC_DCDC = 1.8 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		52	260	412		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		42	248	399		
	VCC current		I_{CC}	3.9	7.1	9.7		VCC = 3.3 V

Note: This table lists the values for current under the following operating conditions.
- Unless otherwise specified, the clocks are set to the states that maximize the supply currents within the limits imposed by the specifications.
- The program is placed in the LRAM, the cache is enabled, and the CPU repeatedly executes multiply-and-accumulate instructions.
- The clock-signal supplies to the peripheral functions are stopped.
- Power to the ESWM domain is turned off.

Note 1. Value for I_{CC_DCDC} can be estimated by using the following formulae (units: I_{CC_DCDC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When VCC_DCDC = 3.3 V]
I_{CC_DCDC} Typ.(VSCR_1) = 0.0352 × $f_{CPUCLK0}$ + 0.0163 × f_{ICLK} + 14.69
I_{CC_DCDC} Typ.(VSCR_2) = 0.0369 × $f_{CPUCLK0}$ + 0.0119 × f_{ICLK} + 12.17
I_{CC_DCDC} Max.(VSCR_1, 105°C) = 0.0454 × $f_{CPUCLK0}$ + 0.0180 × f_{ICLK} + 132.14
I_{CC_DCDC} Max.(VSCR_1, 125°C) = 0.0496 × $f_{CPUCLK0}$ + 0.0190 × f_{ICLK} + 218.27
I_{CC_DCDC} Max.(VSCR_2, 105°C) = 0.0443 × $f_{CPUCLK0}$ + 0.0162 × f_{ICLK} + 119.62
I_{CC_DCDC} Max.(VSCR_2, 125°C) = 0.0479 × $f_{CPUCLK0}$ + 0.0183 × f_{ICLK} + 197.45
[When VCC_DCDC = 1.8 V]
I_{CC_DCDC} Typ.(VSCR_1) = 0.0674 × $f_{CPUCLK0}$ + 0.0279 × f_{ICLK} + 17.22
I_{CC_DCDC} Typ.(VSCR_2) = 0.0646 × $f_{CPUCLK0}$ + 0.0223 × f_{ICLK} + 15.14
I_{CC_DCDC} Max.(VSCR_1, 105°C) = 0.0863 × $f_{CPUCLK0}$ + 0.0343 × f_{ICLK} + 237.02
I_{CC_DCDC} Max.(VSCR_1, 125°C) = 0.0935 × $f_{CPUCLK0}$ + 0.0359 × f_{ICLK} + 399.63
I_{CC_DCDC} Max.(VSCR_2, 105°C) = 0.0806 × $f_{CPUCLK0}$ + 0.0305 × f_{ICLK} + 214.33
I_{CC_DCDC} Max.(VSCR_2, 125°C) = 0.0897 × $f_{CPUCLK0}$ + 0.0343 × f_{ICLK} + 361.19
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Table 2.12 Supply Currents for Maximum Data Processing with the Peripheral Clock Supplies Stopped (External VDD Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
Supply current (maximum data processing with the peripheral clock supplies stopped)	VCL = 0.92 to 0.99 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{DD}*1	112	468	681	mA	Voltage range 1 (VCL = 0.95 V)
	VCL = 0.87 to 0.99 V	Frequency setting 2 (CPUCLK0 = 480 MHz)		90	426	631		Voltage range 2 (VCL = 0.925 V)
		Frequency setting 3 (CPUCLK0 = 300 MHz)		73	408	614		
	VCC current		I_{CC}	3.9	7.1	9.7		VCC = 3.3 V

Note: This table lists the values for current under the following operating conditions.
- Unless otherwise specified, the clocks are set to the states that maximize the supply currents within the limits imposed by the specifications.
- The program is placed in the LRAM, the cache is enabled, and the CPU repeatedly executes multiply-and-accumulate instructions.
- The clock-signal supplies to the peripheral functions are stopped.
- Power to the ESWM domain is turned off.
- The values given were measured with all output pins load-free and all input pull-up resistors disabled.
- The values given do not include the supply current for background operation (BGO).

Note 1. Value for I_{DD} can be estimated by using the following formulae (units: I_{DD} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
I_{DD} Typ.(VCL = 0.92 to 0.99 V) = 0.1181 × $f_{CPUCLK0}$ + 0.0469 × f_{ICLK} + 27.55
I_{DD} Typ.(VCL = 0.87 to 0.99 V) = 0.1153 × $f_{CPUCLK0}$ + 0.0405 × f_{ICLK} + 25.17
I_{DD} Max.(VCL = 0.92 to 0.99 V, 105°C) = 0.1192 × $f_{CPUCLK0}$ + 0.0469 × f_{ICLK} + 381.95
I_{DD} Max.(VCL = 0.92 to 0.99 V, 125°C) = 0.1148 × $f_{CPUCLK0}$ + 0.0437 × f_{ICLK} + 598.85
I_{DD} Max.(VCL = 0.87 to 0.99 V, 105°C) = 0.1192 × $f_{CPUCLK0}$ + 0.0448 × f_{ICLK} + 357.95
I_{DD} Max.(VCL = 0.87 to 0.99 V, 125°C) = 0.1182 × $f_{CPUCLK0}$ + 0.0449 × f_{ICLK} + 563.65
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Table 2.13 Supply Currents for while(1) Operation by the CPU with the Peripheral Clock Supplies Stopped and the ESWM Domain Turned Off

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Supply current (DCDC mode)	VCC_DCDC ≥ 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{CC_DCDC} *1	28	—	mA	VSCR_1 (VCL = 0.95 V) VCC_DCDC = 3.3 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		23	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		22	—		
	VCC_DCDC < 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)		41	—		VSCR_1 (VCL = 0.95 V) VCC_DCDC = 1.8 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		33	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		30	—		
Supply current (external VDD mode)	VCL = 0.92 to 0.99 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{DD}*2	68	—	mA	Voltage range 1 (VCL = 0.95 V)
	VCL = 0.87 to 0.99 V	Frequency setting 2 (CPUCLK0 = 480 MHz)		56	—		Voltage range 2 (VCL = 0.925 V)
		Frequency setting 3 (CPUCLK0 = 300 MHz)		52	—		

Note: This table lists the values for current under the following operating condition.
- The program is placed in the LRAM, the cache is enabled, and the CPU executes a while(1) loop.

Note 1. Value for I_{CC_DCDC} can be estimated by using the following formulae (units: I_{CC_DCDC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When VCC_DCDC = 3.3 V]
I_{CC_DCDC} Typ.(VSCR_1) = 0.0145 × $f_{CPUCLK0}$ + 0.0149 × f_{ICLK} + 14.35
I_{CC_DCDC} Typ.(VSCR_2) = 0.0113 × $f_{CPUCLK0}$ + 0.0109 × f_{ICLK} + 14.76
[When VCC_DCDC = 1.8 V]
I_{CC_DCDC} Typ.(VSCR_1) = 0.0259 × $f_{CPUCLK0}$ + 0.0269 × f_{ICLK} + 17.25
I_{CC_DCDC} Typ.(VSCR_2) = 0.0236 × $f_{CPUCLK0}$ + 0.0218 × f_{ICLK} + 16.14
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 2. Value for I_{DD} can be estimated by using the following formulae (units: I_{DD} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
I_{DD} Typ.(VCL = 0.92 to 0.99 V) = 0.0448 × $f_{CPUCLK0}$ + 0.0469 × f_{ICLK} + 27.37
I_{DD} Typ.(VCL = 0.87 to 0.99 V) = 0.0440 × $f_{CPUCLK0}$ + 0.0406 × f_{ICLK} + 25.19
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Table 2.14 Supply Currents for Coremark Execution with the Peripheral Clock Supplies Stopped and the ESWM Domain Turned Off (DCDC Mode)

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Cache enabled	VCC_DCDC ≥ 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{CC_DCDC}	36	—	mA	VSCR_1 (VCL = 0.95 V) VCC_DCDC = 3.3 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		29	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		25	—		
	VCC_DCDC < 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)		58	—		VSCR_1 (VCL = 0.95 V) VCC_DCDC = 1.8 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		46	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		38	—		
Cache disabled, code executed in LRAM	VCC_DCDC ≥ 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{CC_DCDC}	29	—	mA	VSCR_1 (VCL = 0.95 V) VCC_DCDC = 3.3 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		24	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		22	—		
	VCC_DCDC < 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)		45	—		VSCR_1 (VCL = 0.95 V) VCC_DCDC = 1.8 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		36	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		31	—		
Cache disabled, code executed in SRAM	VCC_DCDC ≥ 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{CC_DCDC}	23	—	mA	VSCR_1 (VCL = 0.95 V) VCC_DCDC = 3.3 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		21	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		20	—		
	VCC_DCDC < 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)		34	—		VSCR_1 (VCL = 0.95 V) VCC_DCDC = 1.8 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		29	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		27	—		
Cache disabled, code executed in MRAM	VCC_DCDC ≥ 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{CC_DCDC}	26	—	mA	VSCR_1 (VCL = 0.95 V) VCC_DCDC = 3.3 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		22	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		22	—		
	VCC_DCDC < 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)		40	—		VSCR_1 (VCL = 0.95 V) VCC_DCDC = 1.8 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		32	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		32	—		

Table 2.15 Supply Currents for Coremark Execution with the Peripheral Clock Supplies Stopped and the ESWM Domain Turned Off (External VDD Mode)

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Cache enabled	VCL = 0.92 to 0.99 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{DD}	97	—	mA	Voltage range 1 (VCL = 0.95 V)
	VCL = 0.87 to 0.99 V	Frequency setting 2 (CPUCLK0 = 480 MHz)		78	—		Voltage range 2 (VCL = 0.925 V)
		Frequency setting 3 (CPUCLK0 = 300 MHz)		63	—		
Cache disabled, code executed in LRAM	VCL = 0.92 to 0.99 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{DD}	75	—	mA	Voltage range 1 (VCL = 0.95 V)
	VCL = 0.87 to 0.99 V	Frequency setting 2 (CPUCLK0 = 480 MHz)		60	—		Voltage range 2 (VCL = 0.925 V)
		Frequency setting 3 (CPUCLK0 = 300 MHz)		52	—		
Cache disabled, code executed in SRAM	VCL = 0.92 to 0.99 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{DD}	55	—	mA	Voltage range 1 (VCL = 0.95 V)
	VCL = 0.87 to 0.99 V	Frequency setting 2 (CPUCLK0 = 480 MHz)		45	—		Voltage range 2 (VCL = 0.925 V)
		Frequency setting 3 (CPUCLK0 = 300 MHz)		45	—		
Cache disabled, code executed in MRAM	VCL = 0.92 to 0.99 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{DD}	65	—	mA	Voltage range 1 (VCL = 0.95 V)
	VCL = 0.87 to 0.99 V	Frequency setting 2 (CPUCLK0 = 480 MHz)		53	—		Voltage range 2 (VCL = 0.925 V)
		Frequency setting 3 (CPUCLK0 = 300 MHz)		53	—		

Table 2.16 Supply Currents in CPU Sleep Mode with the Peripheral Clock Supplies Stopped and the ESWM Domain Turned Off

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Supply current (DCDC Mode)	VCC_DCDC ≥ 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{CC_DCDC} *1	22	227	mA	VSCR_1 (VCL = 0.95 V) VCC_DCDC = 3.3 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		19	205		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		19	205		
	VCC_DCDC < 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)		31	416		VSCR_1 (VCL = 0.95 V) VCC_DCDC = 1.8 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		26	375		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		26	375		
Supply current (External VDD Mode)	VCL = 0.92 to 0.99 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{DD}*2	52	618	mA	Voltage range 1 (VCL = 0.95 V)
	VCL = 0.87 to 0.99 V	Frequency setting 2 (CPUCLK0 = 480 MHz)		43	582		Voltage range 2 (VCL = 0.925 V)
		Frequency setting 3 (CPUCLK0 = 300 MHz)		44	582		

Note 1. Value for I_{CC_DCDC} can be estimated by using the following formulae (units: I_{CC_DCDC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When VCC_DCDC = 3.3 V]
I_{CC_DCDC} Typ.(VSCR_1) = 0.0049 × $f_{CPUCLK0}$ + 0.0128 × f_{ICLK} + 15.37
I_{CC_DCDC} Typ.(VSCR_2) = 0.0051 × $f_{CPUCLK0}$ + 0.0109 × f_{ICLK} + 14.14
[When VCC_DCDC = 1.8 V]
I_{CC_DCDC} Typ.(VSCR_1) = 0.0098 × $f_{CPUCLK0}$ + 0.0260 × f_{ICLK} + 17.72

I_{CC_DCDC} Typ.(VSCR_2) = 0.0096 × $f_{CPUCLK0}$ + 0.0221 × f_{ICLK} + 15.88
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 2. Value for I_{DD} can be estimated by using the following formulae (units: I_{DD} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
I_{DD} Typ.(VCL = 0.92 to 0.99 V) = 0.0176 × $f_{CPUCLK0}$ + 0.0471 × f_{ICLK} + 27.25
I_{DD} Typ.(VCL = 0.87 to 0.99 V) = 0.0175 × $f_{CPUCLK0}$ + 0.0409 × f_{ICLK} + 25.14
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Table 2.17 Supply Currents in CPU Deep Sleep Mode with the Peripheral Clock Supplies Stopped and the ESWM Domain Turned Off

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Supply current (DCDC Mode)	VCC_DCDC ≥ 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{CC_DCDC} *1	20	186	mA	VSCR_1 (VCL = 0.95 V) VCC_DCDC = 3.3 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		17	168		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		18	169		
	VCC_DCDC < 2.5 V	Frequency setting 1 (CPUCLK0 = 600 MHz)		27	340		VSCR_1 (VCL = 0.95 V) VCC_DCDC = 1.8 V
		Frequency setting 2 (CPUCLK0 = 480 MHz)		22	307		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
		Frequency setting 3 (CPUCLK0 = 300 MHz)		23	308		
Supply current (External VDD Mode)	VCL = 0.92 to 0.99 V	Frequency setting 1 (CPUCLK0 = 600 MHz)	I_{DD}*2	43	520	mA	Voltage range 1 (VCL = 0.95 V)
	VCL = 0.87 to 0.99 V	Frequency setting 2 (CPUCLK0 = 480 MHz)		36	489		Voltage range 2 (VCL = 0.925 V)
		Frequency setting 3 (CPUCLK0 = 300 MHz)		38	491		

Note 1. Value for I_{CC_DCDC} can be estimated by using the following formulae (units: I_{CC_DCDC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When VCC_DCDC = 3.3 V]
I_{CC_DCDC} Typ.(VSCR_1) = 0.0024 × $f_{CPUCLK0}$ + 0.0134 × f_{ICLK} + 14.33
I_{CC_DCDC} Typ.(VSCR_2) = 0.0029 × $f_{CPUCLK0}$ + 0.0122 × f_{ICLK} + 12.87
[When VCC_DCDC = 1.8 V]
I_{CC_DCDC} Typ.(VSCR_1) = 0.0049 × $f_{CPUCLK0}$ + 0.0265 × f_{ICLK} + 15.67
I_{CC_DCDC} Typ.(VSCR_2) = 0.0050 × $f_{CPUCLK0}$ + 0.0226 × f_{ICLK} + 13.98
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 2. Value for I_{DD} can be estimated by using the following formulae (units: I_{DD} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
I_{DD} Typ.(VCL = 0.92 to 0.99 V) = 0.0089 × $f_{CPUCLK0}$ + 0.0472 × f_{ICLK} + 23.68
I_{DD} Typ.(VCL = 0.87 to 0.99 V) = 0.0089 × $f_{CPUCLK0}$ + 0.0406 × f_{ICLK} + 22.00
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Table 2.18 Increases in Supply Currents during BGO Programming of MRAM-OTP in the Case of Maximal Operation

Item		Symbol	Typ.	Max.	Unit	Test Conditions
Supply current	Normal speed write mode	I_{CC}	—	20	mA	VCC ≥ 1.62 V
		I_{DD}	—	0.5		
	High speed write mode 0	I_{CC}	—	25		VCC ≥ 2.5 V
		I_{DD}	—	5		
	High speed write mode 1	I_{CC}	—	80		VCC ≥ 3.0 V
		I_{DD}	—	0.5		

Note: The MWMCR register is used to select the mode for writing data to MRAM-OTP.

Table 2.19 Currents in Software Standby Mode 1 (DCDC Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
VCC current			I_{CC}	0.20	0.41	0.62	mA	VCC = 3.3 V
VCC_DCDC current	The SRAM and LRAM data are retained.*1, *2	VSCR_1 (VCL = 0.95 V)	I_{CC_DCDC}	10.5	86.3	135	mA	VCC_DCDC = 3.3 V
		VSCR_2 (VCL = 0.925 V)		9.76	79.2	124		
	The SRAM and LRAM data are not retained. *1, *2	VSCR_1 (VCL = 0.95 V)		10.3	85.7	134		
		VSCR_2 (VCL = 0.925 V)		9.63	78.7	123		

Note 1. When the PDRAMSCR0 register is set to 7FFFh, data in the SRAM are retained; when the register is set to 7000h, data in the SRAM are not retained.

Note 2. When the PDRAMSCR2.RKEEP0 bit is set to 1, data in the LRAM are retained; when the bit is set to 0, data in the LRAM are not retained.

Table 2.20 Currents in Software Standby Mode 2 (DCDC Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
VCC current	For SS2LP_0		I_{CC}	0.20	0.41	0.62	mA	VCC = 3.3 V
	For SS2LP_1			0.04	0.27	0.48		
SS2LP_0*1	SVSCR_1*2	The SRAM and LRAM data are retained.*3, *4	I_{CC_DCDC}	8.95	26.8	39.2	mA	VCC_DCDC = 3.3 V
		The SRAM and LRAM data are not retained.*3, *4		8.88	26.0	37.8		
	SVSCR_2*2	The SRAM and LRAM data are retained.*3, *4		8.89	24.7	36.0		
		The SRAM and LRAM data are not retained.*3, *4		8.74	24.2	35.1		
	SVSCR_3*2	The SRAM and LRAM data are retained.*3, *4		8.69	18.7	27.9		
		The SRAM and LRAM data are not retained.*3, *4		8.68	18.4	27.3		
	SVSCR_4*2	The SRAM and LRAM data are retained.*3, *4		8.62	16.6	24.7		
		The SRAM and LRAM data are not retained.*3, *4		8.59	16.1	23.6		
	SVSCR_5*2	The SRAM and LRAM data are retained.*3, *4		8.39	14.6	21.5		
		The SRAM and LRAM data are not retained.*3, *4		8.37	14.2	20.6		
SS2LP_1*1	SVSCR_2*2	The SRAM and LRAM data are retained.*3, *4	I_{CC_DCDC}	1.06	20.3	34.1	mA	VCC_DCDC = 3.3 V
		The SRAM and LRAM data are not retained.*3, *4		0.96	19.8	33.0		
	SVSCR_3*2	The SRAM and LRAM data are retained.*3, *4		0.69	14.9	25.5		
		The SRAM and LRAM data are not retained.*3, *4		0.65	14.6	24.8		
	SVSCR_4*2	The SRAM and LRAM data are retained.*3, *4		0.56	13.0	22.6		
		The SRAM and LRAM data are not retained.*3, *4		0.52	12.4	21.3		
	SVSCR_5*2	The SRAM and LRAM data are retained.*3, *4		0.46	11.2	19.6		
		The SRAM and LRAM data are not retained.*3, *4		0.43	10.7	18.5		

Note 1. Setting of the SS2LP[1:0] bits in the SSCR1 register: SS2LP_0 = default mode, SS2LP_1 = low power setting 1

Note 2. SVSCR_n (n = 1 to 5) is the target VDD voltage specified in the SVSCR register.
Note 3. When the PDRAMSCR0 register is set to 7FFFh, data in the SRAM are retained; when the register is set to 7000h, data in the SRAM are not retained.
Note 4. When the PDRAMSCR2.RKEEP0 bit is set to 1, data in the LRAM are retained; when the bit is set to 0, data in the LRAM are not retained.

2.4.4.2 Operating and Standby Currents for Product Part No. R5K574Mxy4xx (y = E, F)

Table 2.21 Supply Currents for Full Operation (DCDC Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
Supply current (full operation	VCC_DCDC ≥ 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{CC_DCDC} *1	62	144	210	mA	VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
	VCC_DCDC < 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)		104	260	384		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
	VCC current		I_{CC}	10	13	15		VCC = 3.3 V

Note: This table lists the values for current under the following operating conditions.
- The internal memory (SRAM and MRAM) is configured with wait settings that suit the operating frequency and kept as active as is possible through data transfer by the DMAC.
- The peripheral functions are supplied with clocks and kept as active as is possible.
- Unless otherwise specified, the clocks are set to the states that maximize the supply currents within the limits imposed by the specifications.
- The program is placed in the LRAM, the cache is enabled, and the CPU repeatedly executes multiply-and-accumulate instructions.
- Power to the ESWM domain is turned on.

Note 1. Value for I_{CC_DCDC} can be estimated by using the following formulae (units: I_{CC_DCDC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When VCC_DCDC = 3.3 V]
I_{CC_DCDC} Typ. = 0.0460 × $f_{CPUCLK0}$ + 0.0622 × f_{ICLK} + 29.28
I_{CC_DCDC} Max.(VSCR_2, 105°C) = 0.0456 × $f_{CPUCLK0}$ + 0.0702 × f_{ICLK} + 109.07
I_{CC_DCDC} Max.(VSCR_2, 125°C) = 0.0477 × $f_{CPUCLK0}$ + 0.0723 × f_{ICLK} + 173.67
[When VCC_DCDC = 1.8 V]
I_{CC_DCDC} Typ. = 0.0818 × $f_{CPUCLK0}$ + 0.1136 × f_{ICLK} + 45.27
I_{CC_DCDC} Max.(VSCR_2, 105°C) = 0.0854 × $f_{CPUCLK0}$ + 0.1322 × f_{ICLK} + 194.42
I_{CC_DCDC} Max.(VSCR_2, 125°C) = 0.0890 × $f_{CPUCLK0}$ + 0.1352 × f_{ICLK} + 316.79
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Table 2.22 Supply Currents for Full Operation (External VDD Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
Supply current (full operation	VCL = 0.87 to 0.99 V	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{DD}*1	181	425	594	mA	Voltage range 2 (VCL = 0.925 V)
	VCC current		I_{CC}	10	13	15		VCC = 3.3 V

Note: This table lists the values for current under the following operating conditions.
- The internal memory (SRAM and MRAM) is configured with wait settings that suit the operating frequency and kept as active as is possible through data transfer by the DMAC.
- The peripheral functions are supplied with clocks and kept as active as is possible.
- Unless otherwise specified, the clocks are set to the states that maximize the supply currents within the limits imposed by the specifications.
- The program is placed in the LRAM, the cache is enabled, and the CPU repeatedly executes multiply-and-accumulate instructions.
- Power to the ESWM domain is turned on.

Note 1. Value for I_{DD} can be estimated by using the following formulae (units: I_{DD} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
I_{DD} Typ. = 0.1408 × $f_{CPUCLK0}$ + 0.1942 × f_{ICLK} + 80.70
I_{DD} Max.(VCL = 0.87 to 0.99 V, 105°C) = 0.1267 × $f_{CPUCLK0}$ + 0.1933 × f_{ICLK} + 329.00
I_{DD} Max.(VCL = 0.87 to 0.99 V, 125°C) = 0.1200 × $f_{CPUCLK0}$ + 0.1800 × f_{ICLK} + 504.00
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Table 2.23 Supply Currents for Full Operation (LDO Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
Supply current (full operation)	LDO efficiency improvement function is disabled*2	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{CC}*1	192	432	600	mA	VCC = 3.3 V
	LDO efficiency improvement function is enabled*2, *3	Frequency setting 3 (CPUCLK0 = 300 MHz)		175	352*4	477*4		
				230	487*4	666*4		VCC = 1.8 V

Note: This table lists the values for current under the following operating conditions.
- The internal memory (SRAM and MRAM) is configured with wait settings that suit the operating frequency and kept as active as is possible through data transfer by the DMAC.
- The peripheral functions are supplied with clocks and kept as active as is possible.
- Unless otherwise specified, the clocks are set to the states that maximize the supply currents within the limits imposed by the specifications.
- The program is placed in the LRAM, the cache is enabled, and the CPU repeatedly executes multiply-and-accumulate instructions.
- Power to the ESWM domain is turned on.

Note 1. Value for I_{CC} can be estimated by using the following formulae (units: I_{CC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).

[When LDO efficiency improvement function is disabled (LDOECR.EFUPE = 0)]

I_{CC} Typ. = 0.1431 × $f_{CPUCLK0}$ + 0.2051 × f_{ICLK} + 87.95

I_{CC} Max.(VSCR_2, 105°C) = 0.1333 × $f_{CPUCLK0}$ + 0.2000 × f_{ICLK} + 332.01

I_{CC} Max.(VSCR_2, 125°C) = 0.1400 × $f_{CPUCLK0}$ + 0.2000 × f_{ICLK} + 498.00

[When LDO efficiency improvement function is enabled (LDOECR.EFUPE = 1)] (VCC = 3.3 V)

I_{CC} Typ. = (0.0856 × $f_{CPUCLK0}$ + 0.1260 × f_{ICLK} + 95.97) × (correction coefficients 1.1)

I_{CC} Max.(VSCR_2, 105°C) = (0.1133 × $f_{CPUCLK0}$ + 0.1333 × f_{ICLK} + 246.02) × (correction coefficients 1.1)

I_{CC} Max.(VSCR_2, 125°C) = (0.0867 × $f_{CPUCLK0}$ + 0.1400 × f_{ICLK} + 365.99) × (correction coefficients 1.1)

[When LDO efficiency improvement function is enabled (LDOECR.EFUPE = 1)] (VCC = 1.8 V)

I_{CC} Typ. = (0.1456 × $f_{CPUCLK0}$ + 0.2042 × f_{ICLK} + 103.76) × (correction coefficients 1.1)

I_{CC} Max.(VSCR_2, 105°C) = (0.1267 × $f_{CPUCLK0}$ + 0.1867 × f_{ICLK} + 348.98) × (correction coefficients 1.1)

I_{CC} Max.(VSCR_2, 125°C) = (0.1000 × $f_{CPUCLK0}$ + 0.1733 × f_{ICLK} + 523.01) × (correction coefficients 1.1)

However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 2. LDOECR.EFUPE = 0 (disabled) or LDOECR.EFUPE = 1 (enabled)

Note 3. When the LDO efficiency improvement function is enabled, the efficiency deteriorates and the supply current increases as the VCC voltage decreases. See Figure 2.6.

Note 4. The values are reference values.

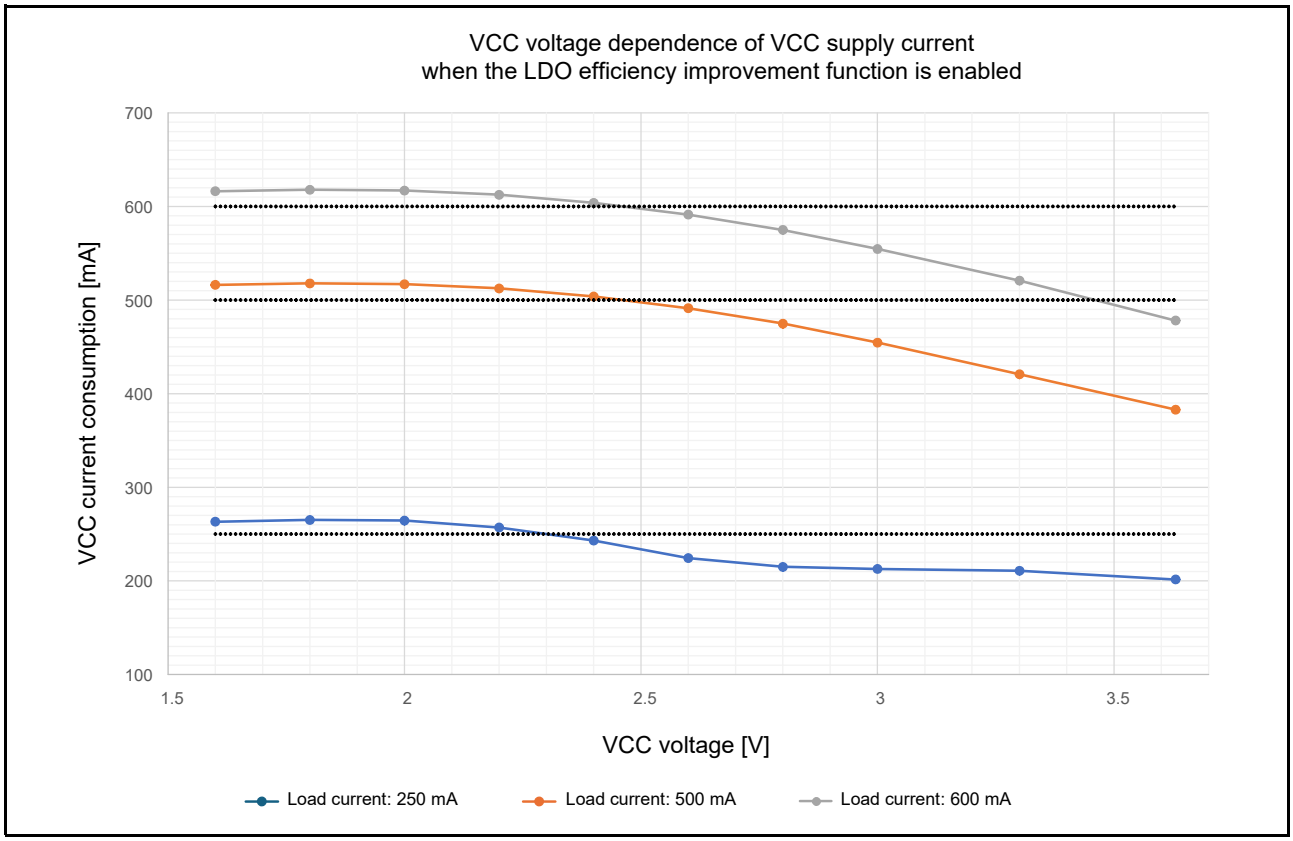


Figure 2.6 VCC Voltage Dependence of VCC Supply Current when the LDO Efficiency Improvement Function is Enabled

Table 2.24 Supply Currents for Maximum Data Processing with the Peripheral Clock Supplies Stopped (DCDC Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
Supply current	VCC_DCDC ≥ 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{CC_DCDC} *1	25	106	173	mA	VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
	VCC_DCDC < 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)		36	189	315		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
	VCC current		I_{CC}	3.9	6.2	8.3		VCC = 3.3 V

Note: This table lists the values for current under the following operating conditions.
- Unless otherwise specified, the clocks are set to the states that maximize the supply currents within the limits imposed by the specifications.
- The program is placed in the LRAM, the cache is enabled, and the CPU repeatedly executes multiply-and-accumulate instructions.
- The clock-signal supplies to the peripheral functions are stopped.
- Power to the ESWM domain is turned off.

Note 1. Value for I_{CC_DCDC} can be estimated by using the following formulae (units: I_{CC_DCDC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).

[When VCC_DCDC = 3.3 V]

I_{CC_DCDC} Typ. = 0.0318 × $f_{CPUCLK0}$ + 0.0111 × f_{ICLK} + 12.00

I_{CC_DCDC} Max.(VSCR_2, 105°C) = 0.0210 × $f_{CPUCLK0}$ + 0.0070 × f_{ICLK} + 97.82

I_{CC_DCDC} Max.(VSCR_2, 125°C) = 0.0126 × $f_{CPUCLK0}$ + 0.0026 × f_{ICLK} + 168.35

[When VCC_DCDC = 1.8 V]

I_{CC_DCDC} Typ. = 0.0612 × $f_{CPUCLK0}$ + 0.0197 × f_{ICLK} + 12.07

I_{CC_DCDC} Max.(VSCR_2, 105°C) = 0.0387 × $f_{CPUCLK0}$ + 0.0129 × f_{ICLK} + 174.02

I_{CC_DCDC} Max.(VSCR_2, 125°C) = 0.0243 × $f_{CPUCLK0}$ + 0.0048 × f_{ICLK} + 306.77

However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Table 2.25 Supply Currents for Maximum Data Processing with the Peripheral Clock Supplies Stopped (External VDD Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
Supply current	VCL = 0.87 to 0.99 V	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{DD}*1	62.5	320	501	mA	Voltage range 2 (VCL = 0.925 V)
	VCC current		I_{CC}	3.9	6.2	8.3		VCC = 3.3 V

Note: This table lists the values for current under the following operating conditions.
- Unless otherwise specified, the clocks are set to the states that maximize the supply currents within the limits imposed by the specifications.
- The program is placed in the LRAM, the cache is enabled, and the CPU repeatedly executes multiply-and-accumulate instructions.
- The clock-signal supplies to the peripheral functions are stopped.
- Power to the ESWM domain is turned off.
- The values given were measured with all output pins load-free and all input pull-up resistors disabled.
- The values given do not include the supply current for background operation (BGO).

Note 1. Value for I_{DD} can be estimated by using the following formulae (units: I_{DD} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
I_{DD} Typ. = $0.1124 \times f_{CPUCLK0} + 0.0351 \times f_{ICLK} + 18.30$
I_{DD} Max.(VCL = 0.87 to 0.99 V, 105°C) = $0.0600 \times f_{CPUCLK0} + 0.0200 \times f_{ICLK} + 296.00$
I_{DD} Max.(VCL = 0.87 to 0.99 V, 125°C) = $0.0333 \times f_{CPUCLK0} + 0.0067 \times f_{ICLK} + 489.00$
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Table 2.26 Supply Currents for Maximum Data Processing with the Peripheral Clock Supplies Stopped (LDO Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
Supply current	LDO efficiency improvement function is disabled*2	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{CC}*1	68.1	323	503	mA	VCC = 3.3 V
	LDO efficiency improvement function is enabled*2	Frequency setting 3 (CPUCLK0 = 300 MHz)		68.0	256*3	424*3		
				68.2	373*3	554*3		VCC = 1.8 V

Note: This table lists the values for current under the following operating conditions.
- The internal memory (SRAM and MRAM) is configured with wait settings that suit the operating frequency and kept as active as is possible through data transfer by the DMAC.
- The peripheral functions are supplied with clocks and kept as active as is possible.
- Unless otherwise specified, the clocks are set to the states that maximize the supply currents within the limits imposed by the specifications.
- The program is placed in the LRAM, the cache is enabled, and the CPU repeatedly executes multiply-and-accumulate instructions.
- Power to the ESWM domain is turned on.

Note 1. Value for I_{CC} can be estimated by using the following formulae (units: I_{CC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When LDO efficiency improvement function is disabled (LDOECR.EFUPE = 0)]
I_{CC} Typ. = $0.1115 \times f_{CPUCLK0} + 0.0349 \times f_{ICLK} + 24.16$
I_{CC} Max.(VSCR_2, 105°C) = $0.0800 \times f_{CPUCLK0} + 0.0333 \times f_{ICLK} + 289.01$
I_{CC} Max.(VSCR_2, 125°C) = $0.0800 \times f_{CPUCLK0} + 0.0400 \times f_{ICLK} + 467.00$
[When LDO efficiency improvement function is enabled (LDOECR.EFUPE = 1)] (VCC = 3.3 V)
I_{CC} Typ. = $0.1115 \times f_{CPUCLK0} + 0.0349 \times f_{ICLK} + 24.08$
I_{CC} Max.(VSCR_2, 105°C) = $(0.0400 \times f_{CPUCLK0} + 0.0200 \times f_{ICLK} + 215.00)$ × (correction coefficients 1.1)
I_{CC} Max.(VSCR_2, 125°C) = $(0.0733 \times f_{CPUCLK0} + 0.2200 \times f_{ICLK} + 297.01)$ × (correction coefficients 1.1)
[When LDO efficiency improvement function is enabled (LDOECR.EFUPE = 1)] (VCC = 1.8 V)
I_{CC} Typ. = $0.1115 \times f_{CPUCLK0} + 0.0349 \times f_{ICLK} + 24.25$
I_{CC} Max.(VSCR_2, 105°C) = $(0.0327 \times f_{CPUCLK0} + 0.1029 \times f_{ICLK} + 298.32)$ × (correction coefficients 1.1)
I_{CC} Max.(VSCR_2, 125°C) = $(0.0333 \times f_{CPUCLK0} + 0.0200 \times f_{ICLK} + 488.01)$ × (correction coefficients 1.1)
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 2. LDOECR.EFUPE = 0 (disabled) or LDOECR.EFUPE = 1 (enabled)

Note 3. The values are reference values.

Table 2.27 Supply Currents for while(1) Operation by the CPU with the Peripheral Clock Supplies Stopped and the ESWM Domain Turned Off

Item			Symbol	Typ.	Max.	Unit	Test Conditions
DCDC mode	VCC_DCDC ≥ 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{CC_DCDC} *2	16	—	mA	VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
	VCC_DCDC < 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)		24	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
External VDD mode	VCL = 0.87 to 0.99 V	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{DD}*3	41	—	mA	Voltage range 2 (VCL = 0.925 V)
LDO mode	LDO efficiency improvement function is disabled*1	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{CC}*4	47	—	mA	VCC = 3.3 V
	LDO efficiency improvement function is enabled*1	Frequency setting 3 (CPUCLK0 = 300 MHz)		47	—		

Note 1. LDOECR.EFUPE = 0 (disabled) or LDOECR.EFUPE = 1 (enabled)

Note 2. Value for I_{CC_DCDC} can be estimated by using the following formulae (units: I_{CC_DCDC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When VCC_DCDC = 3.3 V]
I_{CC_DCDC} Typ.(VSCR_2) = 0.0069 × $f_{CPUCLK0}$ + 0.0122 × f_{ICLK} + 10.71
[When VCC_DCDC = 1.8 V]
I_{CC_DCDC} Typ.(VSCR_2) = 0.0213 × $f_{CPUCLK0}$ + 0.0200 × f_{ICLK} + 11.63
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 3. Value for I_{DD} can be estimated by using the following formula (units: I_{DD} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
I_{DD} Typ.(VCL = 0.87 to 0.99 V) = 0.0420 × $f_{CPUCLK0}$ + 0.0353 × f_{ICLK} + 18.16
However, note that the above formula is only for use in estimation and values from it do not guarantee the actual supply currents.

Note 4. Value for I_{CC} can be estimated by using the following formulae (units: I_{CC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When LDO efficiency improvement function is disabled (LDOECR.EFUPE = 0)]
I_{CC} Typ. = 0.0425 × $f_{CPUCLK0}$ + 0.0351 × f_{ICLK} + 24.05
[When LDO efficiency improvement function is enabled (LDOECR.EFUPE = 1)]
I_{CC} Typ. = 0.0423 × $f_{CPUCLK0}$ + 0.0351 × f_{ICLK} + 23.78
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Table 2.28 Supply Currents for Coremark Execution with the Peripheral Clock Supplies Stopped and the ESWM Domain Turned Off (DCDC Mode)

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Cache enabled	VCC_DCDC ≥ 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{CC_DCDC}	23	—	mA	VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
	VCC_DCDC < 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)		34	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
Cache disabled, code executed in LRAM	VCC_DCDC ≥ 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{CC_DCDC}	20	—	mA	VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
	VCC_DCDC < 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)		27	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
Cache disabled, code executed in SRAM	VCC_DCDC ≥ 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{CC_DCDC}	18	—	mA	VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
	VCC_DCDC < 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)		23	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
Cache disabled, code executed in MRAM	VCC_DCDC ≥ 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{CC_DCDC}	20	—	mA	VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
	VCC_DCDC < 2.5 V	Frequency setting 3 (CPUCLK0 = 300 MHz)		28	—		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V

Table 2.29 Supply Currents for Coremark Execution with the Peripheral Clock Supplies Stopped and the ESWM Domain Turned Off (External VDD Mode)

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Cache enabled	VCL = 0.87 to 0.99 V	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{DD}	56	—	mA	Voltage range 2 (VCL = 0.925 V)
Cache disabled, code executed in LRAM			I_{DD}	45	—	mA	
Cache disabled, code executed in SRAM			I_{DD}	38	—	mA	
Cache disabled, code executed in MRAM			I_{DD}	45	—	mA	

Table 2.30 Supply Currents for Coremark Execution with the Peripheral Clock Supplies Stopped and the ESWM Domain Turned Off (LDO Mode)

Item		Symbol	Typ.	Max.	Unit	Test Conditions
Cache enabled	Frequency setting 3 (CPUCLK0 = 300 MHz)	I_{DD}	62	—	mA	VCC = 3.3 V
Cache disabled, code executed in LRAM		I_{DD}	51	—	mA	
Cache disabled, code executed in SRAM		I_{DD}	44	—	mA	
Cache disabled, code executed in MRAM		I_{DD}	58	—	mA	

Table 2.31 Supply Currents in CPU Sleep Mode with the Peripheral Clock Supplies Stopped and the ESWM Domain Turned Off

Item		Symbol	Typ.	Max.	Unit	Test Conditions
DCDC mode	VCC_DCDC ≥ 2.5 V	I_{CC_DCDC} *2	17	188	mA	VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
	VCC_DCDC < 2.5 V		21	344		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
External VDD mode	VCL = 0.87 to 0.99 V	I_{DD}*3	34	540	mA	Voltage range 2 (VCL = 0.925 V)
LDO mode	LDO efficiency improvement function is disabled*1	I_{CC}*4	40	542	mA	VCC = 3.3 V
	LDO efficiency improvement function is enabled*1		40	406*5		
			40	595*5		VCC = 1.8 V

Note 1. LDOECR.EFUPE = 0 (disabled) or LDOECR.EFUPE = 1 (enabled)

Note 2. Value for I_{CC_DCDC} can be estimated by using the following formulae (units: I_{CC_DCDC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When VCC_DCDC = 3.3 V]
I_{CC_DCDC} Typ. = 0.0028 × $f_{CPUCLK0}$ + 0.0096 × f_{ICLK} + 12.80
[When VCC_DCDC = 1.8 V]
I_{CC_DCDC} Typ. = 0.0074 × $f_{CPUCLK0}$ + 0.0184 × f_{ICLK} + 12.82
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 3. Value for I_{DD} can be estimated by using the following formula (units: I_{DD} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
I_{DD} Typ.(VCL = 0.87 to 0.99 V) = 0.0169 × $f_{CPUCLK0}$ + 0.0351 × f_{ICLK} + 18.18
However, note that the above formula is only for use in estimation and values from it do not guarantee the actual supply currents.

Note 4. Value for I_{CC} can be estimated by using the following formulae (units: I_{CC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When LDO efficiency improvement function is disabled (LDOECR.EFUPE = 0)]
I_{CC} Typ. = 0.0171 × $f_{CPUCLK0}$ + 0.0352 × f_{ICLK} + 24.02
[When LDO efficiency improvement function is enabled (LDOECR.EFUPE = 1)]
I_{CC} Typ. = 0.0170 × $f_{CPUCLK0}$ + 0.0351 × f_{ICLK} + 24.50
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 5. The values are reference values.

Table 2.32 Supply Currents in CPU Deep Sleep Mode with the Peripheral Clock Supplies Stopped and the ESWM Domain Turned Off

Item		Symbol	Typ.	Max.	Unit	Test Conditions
DCDC mode	VCC_DCDC ≥ 2.5 V	I_{CC_DCDC} *2	15	154	mA	VSCR_2 (VCL = 0.925 V) VCC_DCDC = 3.3 V
	VCC_DCDC < 2.5 V		19	279		VSCR_2 (VCL = 0.925 V) VCC_DCDC = 1.8 V
External VDD mode	VCL = 0.87 to 0.99 V	I_{DD}*3	30	450	mA	Voltage range 2 (VCL = 0.925 V)
LDO mode	LDO efficiency improvement function is disabled*1	I_{CC}*4	36	453	mA	VCC = 3.3 V
	LDO efficiency improvement function is enabled*1		36	347*5		
			36	506*5		VCC = 1.8 V

Note 1. LDOECR.EFUPE = 0 (disabled) or LDOECR.EFUPE = 1 (enabled)

Note 2. Value for I_{CC_DCDC} can be estimated by using the following formulae (units: I_{CC_DCDC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When VCC_DCDC = 3.3 V]
I_{CC_DCDC} Typ.(VSCR_2) = 0.0016 × $f_{CPUCLK0}$ + 0.0062 × f_{ICLK} + 13.10
[When VCC_DCDC = 1.8 V]
I_{CC_DCDC} Typ.(VSCR_2) = 0.0039 × $f_{CPUCLK0}$ + 0.0156 × f_{ICLK} + 12.82
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 3. Value for I_{DD} can be estimated by using the following formula (units: I_{DD} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
I_{DD} Typ.(VCL = 0.87 to 0.99 V) = 0.0085 × $f_{CPUCLK0}$ + 0.0350 × f_{ICLK} + 17.37
However, note that the above formula is only for use in estimation and values from it do not guarantee the actual supply currents.

Note 4. Value for I_{CC} can be estimated by using the following formulae (units: I_{CC} = mA, $f_{CPUCLK0}$ = MHz, f_{ICLK} = MHz).
[When LDO efficiency improvement function is disabled (LDOECR.EFUPE = 0)]
I_{CC} Typ. = 0.0086 × $f_{CPUCLK0}$ + 0.0351 × f_{ICLK} + 23.25
[When LDO efficiency improvement function is enabled (LDOECR.EFUPE = 1)]
I_{CC} Typ. = 0.0085 × $f_{CPUCLK0}$ + 0.0352 × f_{ICLK} + 22.89
However, note that the above formulae are only for use in estimation and values from them do not guarantee the actual supply currents.

Note 5. The values are reference values.

Table 2.33 Increases in Supply Currents during BGO Programming of MRAM-OTP in the Case of Maximal Operation

Item		Symbol	Typ.	Max.	Unit	Test Conditions
Supply current	Normal speed write mode	I_{CC}	—	20	mA	VCC ≥ 1.62 V
		I_{DD}	—	0.5		
	High speed write mode 0	I_{CC}	—	25		VCC ≥ 2.5 V
		I_{DD}	—	5		
	High speed write mode 1	I_{CC}	—	80		VCC ≥ 3.0 V
		I_{DD}	—	0.5		

Note: The MWMCR register is used to select the mode for writing data to MRAM-OTP.

Table 2.34 Currents in Software Standby Mode 1 (DCDC Mode)

Item		Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
VCC current		I_{CC}	0.18	0.39	0.62	mA	VCC = 3.3 V
VCC_DCDC current	The SRAM and LRAM data are retained. *1, *2	I_{CC_DCDC}	9.76	77.4	122	mA	VCC_DCDC = 3.3 V
	The SRAM and LRAM data are not retained.*1, *2		9.63	76.7	121		

Note 1. When the PDRAMSCR0 register is set to 7FFFh, data in the SRAM are retained; when the register is set to 7000h, data in the SRAM are not retained.
Note 2. When the PDRAMSCR2.RKEEP0 bit is set to 1, data in the LRAM are retained; when the bit is set to 0, data in the LRAM are not retained.

Table 2.35 Currents in Software Standby Mode 1 (LDO Mode)

Item		Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
VCC current	The SRAM and LRAM data are retained.*1, *2	I_{CC}	9.94	223	353	mA	VCC = 3.3 V
	The SRAM and LRAM data are not retained. *1, *2		9.81	223	353		

Note: In software standby mode 1, disable the LDO efficiency improvement function (LDOECR.EFUPE = 0).
Note 1. When the PDRAMSCR0 register is set to 7FFFh, data in the SRAM are retained; when the register is set to 7000h, data in the SRAM are not retained.
Note 2. When the PDRAMSCR2.RKEEP0 bit is set to 1, data in the LRAM are retained; when the bit is set to 0, data in the LRAM are not retained.

Table 2.36 Currents in Software Standby Mode 2 (DCDC Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
VCC current	For SS2LP_0		I_{CC}	0.18	0.39	0.62	mA	VCC = 3.3 V
	For SS2LP_1			0.04	0.26	0.49		
SS2LP_0*1	SVSCR_2*2	The SRAM and LRAM data are retained.*3, *4	I_{CC_DCDC}	8.34	23.2	34.1	mA	VCC_DCDC = 3.3 V
		The SRAM and LRAM data are not retained.*3, *4		8.25	22.8	33.3		
	SVSCR_3*2	The SRAM and LRAM data are retained.*3, *4		7.99	17.8	26.2		
		The SRAM and LRAM data are not retained.*3, *4		7.94	17.6	25.7		
	SVSCR_4*2	The SRAM and LRAM data are retained.*3, *4		7.87	15.6	22.9		
		The SRAM and LRAM data are not retained.*3, *4		7.84	15.3	22.0		
	SVSCR_5*2	The SRAM and LRAM data are retained.*3, *4		7.79	13.6	19.8		
		The SRAM and LRAM data are not retained.*3, *4		7.77	13.4	19.1		
SS2LP_1*1	SVSCR_2*2	The SRAM and LRAM data are retained.*3, *4	I_{CC_DCDC}	0.84	18.7	31.5	mA	VCC_DCDC = 3.3 V
		The SRAM and LRAM data are not retained.*3, *4		0.73	18.3	30.5		
	SVSCR_3*2	The SRAM and LRAM data are retained.*3, *4		0.53	13.6	23.3		
		The SRAM and LRAM data are not retained.*3, *4		0.48	13.4	22.7		
	SVSCR_4*2	The SRAM and LRAM data are retained.*3, *4		0.42	11.7	20.3		
		The SRAM and LRAM data are not retained.*3, *4		0.39	11.3	19.4		
	SVSCR_5*2	The SRAM and LRAM data are retained.*3, *4		0.34	10.0	17.6		
		The SRAM and LRAM data are not retained.*3, *4		0.32	9.70	16.8		

Note 1. Setting of the SS2LP[1:0] bits in the SSCR1 register: SS2LP_0 = default mode, SS2LP_1 = low power setting 1
Note 2. SVSCR_n (n = 2 to 5) is the target VDD voltage specified in the SVSCR register.
Note 3. When the PDRAMSCR0 register is set to 7FFFh, data in the SRAM are retained; when the register is set to 7000h, data in the SRAM are not retained.
Note 4. When the PDRAMSCR2.RKEEP0 bit is set to 1, data in the LRAM are retained; when the bit is set to 0, data in the LRAM are not retained.

Table 2.37 Currents in Software Standby Mode 2 (LDO Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
SS2LP_0*1	SVSCR_2*2	The SRAM and LRAM data are retained.*3, *4	I_{CC}	4.46	57.2	95.9	mA	VCC = 3.3 V
		The SRAM and LRAM data are not retained.*3, *4		4.11	56.3	94.0		
	SVSCR_3*2	The SRAM and LRAM data are retained.*3, *4		3.66	47.2	80.3		
		The SRAM and LRAM data are not retained.*3, *4		3.49	46.5	78.7		
	SVSCR_4*2	The SRAM and LRAM data are retained.*3, *4		3.39	42.7	73.8		
		The SRAM and LRAM data are not retained.*3, *4		3.26	41.2	70.6		
	SVSCR_5*2	The SRAM and LRAM data are retained.*3, *4		3.14	38.6	67.3		
		The SRAM and LRAM data are not retained.*3, *4		3.05	37.3	64.4		
SS2LP_1*1	SVSCR_2*2	The SRAM and LRAM data are retained.*3, *4	I_{CC}	2.85	56.4	94.9	mA	VCC = 3.3 V
		The SRAM and LRAM data are not retained.*3, *4		2.51	55.6	93.1		
	SVSCR_3*2	The SRAM and LRAM data are retained.*3, *4		2.09	46.3	79.3		
		The SRAM and LRAM data are not retained.*3, *4		1.92	45.6	77.8		
	SVSCR_4*2	The SRAM and LRAM data are retained.*3, *4		1.78	41.6	72.6		
		The SRAM and LRAM data are not retained.*3, *4		1.65	40.4	69.6		
	SVSCR_5*2	The SRAM and LRAM data are retained.*3, *4		1.54	37.5	66.1		
		The SRAM and LRAM data are not retained.*3, *4		1.45	36.4	63.3		

Note: In software standby mode 2, disable the LDO efficiency improvement function (LDOECR.EFUPE = 0).
Note 1. Setting of the SS2LP[1:0] bits in the SSCR1 register: SS2LP_0 = default mode, SS2LP_1 = low power setting 1
Note 2. SVSCR_n (n = 2 to 5) is the target VDD voltage specified in the SVSCR register.
Note 3. When the PDRAMSCR0 register is set to 7FFFh, data in the SRAM are retained; when the register is set to 7000h, data in the SRAM are not retained.
Note 4. When the PDRAMSCR2.RKEEP0 bit is set to 1, data in the LRAM are retained; when the bit is set to 0, data in the LRAM are not retained.

2.4.4.3 Currents in Deep Software Standby Mode

Table 2.38 Currents in Deep Software Standby Mode (DCDC Mode or LDO Mode)

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
DSTBY1	VCC_DCDC current		I_{CC_DCDC}	0.16	1.24	2.45	μA	Condition for the Max. values: VCC = VCC_DCDC = 3.63 V Condition for the Typ. values: VCC = VCC_DCDC = 3.3 V
	VCC current		I_{CC}	7.10	185	332		
		Increase in the current when PVDn or VBATT power switching is enabled*1		See Table 2.40				
		Increase in the current when the LOCO is in use*2		3.42	4.50	5.20		
		Increase in the current during SOSC and RTC operation		See Table 2.41				
		Increase in the current during IWDT operation		0.01	0.02	0.02		
DSTBY2	VCC_DCDC current		I_{CC_DCDC}	0.16	1.24	2.45	μA	
	VCC current		I_{CC}	4.90	108	195		
		Increase in the current when PVDn or VBATT power switching is enabled*1		See Table 2.40				
		Increase in the current during SOSC and RTC operation		See Table 2.41				
DSTBY3	VCC_DCDC current		I_{CC_DCDC}	0.16	1.24	2.45	μA	
	VCC current		I_{CC}	4.40	106	193		
		Increase in the current during SOSC and RTC operation		See Table 2.41				
Increase in the current when the LDO regulator is in use			I_{CC}	0.10	7.42	26.1	μA	VCC = 3.3 V

DSTBY1: Deep software standby mode 1
DSTBY2: Deep software standby mode 2
DSTBY3: Deep software standby mode 3
PVDn: Programmable voltage detection module (n = 0, 1, 2, 4, 5)
LOCO: Low-speed on-chip oscillator
SOSC: Sub-clock oscillator
RTC: Realtime clock
Note 1. When the VBATTCR1.PSWDIS bit = 0 (initial value), VBATT power switching is enabled.
Note 2. The maximum value for this item is the result measured at VCC = VCC_DCDC = 3.3 V.

Table 2.39 RTC Operating Current with VCC Off (VCC = 0 V) and Only the RTC Operating through the Battery Backup Function

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
VBATT supply current	When a crystal resonator is in use	Low-power mode 2 (7 pF) *1	I_{VBAT}	0.57	—	—	μA	VBATT = 1.8 V
				0.98	—	—		VBATT = 3.3 V
		Low-power mode 1 (9 pF) *1		0.67	—	—		VBATT = 1.8 V
				1.08	—	—		VBATT = 3.3 V
		Standard mode (12.5 pF) *1		0.92	—	—		VBATT = 1.8 V
				1.34	—	—		VBATT = 3.3 V
	When the external sub-clock input pin (EXCIN) is in use			0.23	—	—		VBATT = 1.8 V
				0.57	—	—		VBATT = 3.3 V
	Increased in the current per channel when the RTCICn (n = 0 to 2) input is in use			0.01	—	—		VBATT = 1.8 V
				0.01	—	—		VBATT = 3.3 V

Note 1. This mode is selected by the SOMCR.SODRV[1:0] bits.

Table 2.40 Increases in the Current when the PVDn or VBATT Function is Enabled in DSTBY1 and DSTBY2

Item		Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
Increase in VCC current	Current in the common circuit of PVDn in DSTBY1*1	I_{CC}	3.60	—	—	μA	VCC = VCC_DCDC = 3.3 V
	Current in the common circuit of PVDn in DSTBY2*1		3.60	—	—		
	PVD1 is enabled		1.70	—	—		
	PVD2 is enabled		1.70	—	—		
	PVD4 is enabled		1.70	—	—		
	PVD5 is enabled		1.70	—	—		
	When VBATT power switching is enabled*2		1.70	—	—		

n = 0, 1, 2, 4, 5

Note 1. When PVDn is enabled and the low power consumption function of PVD0 is disabled (OFS1.DSBYLPSEL = 1)

Note 2. When the VBATTCR1.PSWDIS bit = 0 and PVD0 is not in use for VBATT voltage detection (OFS1.DSBYLPSEL = 1)

Table 2.41 Increase in the Current during Sub-Clock Oscillator and RTC Operation in DSTBY Mode

Item			Symbol	Typ.	Max. (Tj = 105°C)	Max. (Tj = 125°C)	Unit	Test Conditions
Increase in VCC current	When a crystal resonator is in use	Low-power mode 2 (7 pF) *1	I_{CC}	0.47	—	—	μA	VCC = VCC_DCDC = 3.3 V
		Low-power mode 1 (9 pF) *1		0.57	—	—		
		Standard mode (12.5 pF) *1		0.83	—	—		
	During RTC Operation			0.05	—	—		

Note 1. This mode is selected by the SOMCR.SODRV[1:0] bits.

Table 2.42 Inrush Currents

Item		Product Part No. (R5K574Mxy4zz)	DPSBYCR Register	Symbol	Typ.	Max.	Unit	Test Conditions
Inrush current of VCC_DCDC	Inrush current on power-on	y = A, B, C, D, T, U, V, W	—	I_{RUSH}	—	1200	mA	—
		y = E, F	—		—	1050		
	Inrush current on return from deep software standby mode	y = A, B, C, D, T, U, V, W	DCSSMODE[1:0] = 01b		—	1150		
			DCSSMODE[1:0] = 10b		—	1050		
			DCSSMODE[1:0] = 11b		—	1050		
		y = E, F	DCSSMODE[1:0] = 01b		—	1000		
			DCSSMODE[1:0] = 10b		—	900		
			DCSSMODE[1:0] = 11b		—	800		
Inrush current of VCC	Inrush current on power-on	zz = FP (LQFP100)		I_{RUSH}	—	495	mA	—
		zz = FB (LQFP144)			—	490		
		zz = FC (LQFP176)			—	500		
		zz = BG (BGA176)			—	500		
		zz = BD (BGA224)			—	500		
		zz = AE (BGA320)			—	511		*1
	Inrush current on return from deep software standby mode	zz = FP (LQFP100)	LDOSSMODE[1:0] = 01b		—	615		—
		zz = FB (LQFP144)			—	602		
		zz = FC (LQFP176)			—	626		
		zz = BG (BGA176)			—	626		
		zz = BD (BGA224)			—	626		
		zz = AE (BGA320)			—	650		*1
		zz = FP (LQFP100)	LDOSSMODE[1:0] = 10b		—	541		—
		zz = FB (LQFP144)			—	532		
		zz = FC (LQFP176)			—	548		
		zz = BG (BGA176)			—	548		
		zz = BD (BGA224)			—	548		
		zz = AE (BGA320)			—	563		*1
		zz = FP (LQFP100)	LDOSSMODE[1:0] = 11b		—	495		—
		zz = FB (LQFP144)			—	490		
		zz = FC (LQFP176)			—	500		
		zz = BG (BGA176)			—	500		
		zz = BD (BGA224)			—	500		
		zz = AE (BGA320)			—	511		*1

Note: The values are reference values.

Note 1. The VCL pins must be connected to the VSS pins via multilayer ceramic capacitors and no more than ten multilayer ceramic capacitors should be connected in LDO mode.
The values for the BGA320 package are for the case with ten multilayer ceramic capacitors connected.

2.4.4.4 Other Operating Currents

Table 2.43 Main Clock Oscillator Operating Current

Item		Symbol	Typ.	Max.	Unit
Main clock oscillator operating current	MOMCR.MODRV0[2:0] = 000b	I_{CC}	0.65	—	mA
	MOMCR.MODRV0[2:0] = 011b		0.76	—	
	MOMCR.MODRV0[2:0] = 101b		0.88	—	

Table 2.44 Analog Operating Currents

Item	A/D Unit 0	S&H (3ch.)	A/D Unit 1	A/D Unit 2	D/A*1 AMP ON	D/A*2 AMP OFF	TEMPS	Symbol	Typ.	Max.	Unit
Analog power supply current	Converting	Sleep	Sleep	Sleep	Stopped	Stopped	Stopped	AI_{CC}	2.4	3.2	mA
	Converting	Converting	Sleep	Sleep	Stopped	Stopped	Stopped		6.6	8.7	
	Waiting	Sleep	Sleep	Sleep	Stopped	Stopped	Stopped		1.6	2.0	
	Sleep	Sleep	Converting	Sleep	Stopped	Stopped	Stopped		2.4	3.2	
	Sleep	Sleep	Waiting	Sleep	Stopped	Stopped	Stopped		1.6	2.0	
	Sleep	Sleep	Sleep	Converting	Stopped	Stopped	Stopped		2.4	3.2	
	Sleep	Sleep	Sleep	Waiting	Stopped	Stopped	Stopped		1.6	2.0	
	Stopped	Stopped	Stopped	Stopped	Converting	Stopped	Stopped		0.5	1.5	
	Stopped	Stopped	Stopped	Stopped	Stopped	Converting	Stopped		0.1	0.2	
	Stopped	Stopped	Stopped	Stopped	Stopped	Stopped	Converting		0.1	0.2	
	Standby mode								0.3	7.3	μA
Reference power supply current	A/D conversion is in progress in all ADC16H units.			SAR mode				AI_{REFH0}	220	370	μA
				Oversampling mode or hybrid mode					580	880	
	All ADC16H units waiting for the start of A/D conversion								8.2	14	
	All ADC16H units in standby mode								0.1	0.5	

Stopped: The module is stopped.
Waiting: The module is operating but not performing A/D conversion.
Sleep: The module is in sleep mode. (ADUSLPCRn.ADUSLPn = 1 (n = 0, 1, or 2))
S&H: Channel-dedicated sample-and-hold circuit
Note 1. The load resistance is 5 kΩ when the amplifier is on.
Note 2. The load resistance is 2 MΩ when the amplifier is off.

Table 2.45 USB Operating Currents

Item				Symbol	Typ.	Max.	Unit
USB operating current	Low-speed operation	USBf		I_{CCUSB_LS}	2.90	4.00	mA
		USBHS	Classic-only mode is disabled	$I_{CCUSBHS_LS}$	11.5	14.6	
			Classic-only mode is enabled		5.04	6.80	
	Full-speed operation	USBf		I_{CCUSB_FS}	4.00	4.70	
		USBHS	Classic-only mode is disabled	$I_{CCUSBHS_FS}$	12.5	14.7	
			Classic-only mode is enabled		5.98	6.90	
	High-speed operation	USBHS		$I_{CCUSBHS_HS}$	45.7	55.3	
	Standby mode	USBHS		$I_{CCUSBHS_SBY}$	0.89	11.4	μA

Note: The power supplies to the USBHS are set as VCC_USBHS = AVCC_USBHS.
Note: Classic-only mode is disabled when the PHYSET.HSEB bit is 0 and enabled when the PHYSET.HSEB bit is 1.

2.4.4.5 Permissible Output Currents

Table 2.46 Permissible Output Currents (1/6)

Item				Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	I3C*1	I3C protocol mode*5	LVO0E = 0	I_{OL}	—	—	20	mA
			LVO0E = 1		—	—	25	
		I^2C (Sm)			—	—	25	
		I^2C (Fm)			—	—	25	
		I^2C (Fm+)			—	—	25	
		I^2C (Hs)			—	—	25	
	RIICHS*2	I^2C (Sm)			—	—	25	
		I^2C (Fm)			—	—	25	
		I^2C (Fm+)			—	—	25	
		I^2C (Hs)			—	—	25	
	Other than above*3, *4	DRV1			—	—	7.5	
		DRV2			—	—	15	
		DRV3			—	—	20	
		DRV4			—	—	25	
		DRV5			—	—	25	
		DRV6			—	—	25	
		DRV7			—	—	25	
		DRV8			—	—	25	
Permissible output low current (max. value per pin)	I3C*1	I3C protocol mode*5	LVO0E = 0	I_{OL}	—	—	40	mA
			LVO0E = 1		—	—	50	
		I^2C (Sm)			—	—	50	
		I^2C (Fm)			—	—	50	
		I^2C (Fm+)			—	—	50	
		I^2C (Hs)			—	—	50	
	RIICHS*2	I^2C (Sm)			—	—	50	
		I^2C (Fm)			—	—	50	
		I^2C (Fm+)			—	—	50	
		I^2C (Hs)			—	—	50	
	Other than above*3, *4	DRV1			—	—	15	
		DRV2			—	—	30	
		DRV3			—	—	40	
		DRV4			—	—	50	
		DRV5			—	—	50	
		DRV6			—	—	50	
		DRV7			—	—	50	
		DRV8			—	—	50	
Permissible output low current (total)	VCC IO (LQFP100)	P001 to P007, P306, P307, P310 to P312, P315 (Total of 13 pins)		ΣI_{OL}	—	—	80	mA
		P101 to P107, P200, P201, P300 to P304 (Total of 14 pins)			—	—	80	
		PA04 to PA07, PB00 to PB06, PC00 to PC06 (Total of 18 pins)			—	—	80	
		PA00 to PA03, PE00 to PE06 (Total of 11 pins)			—	—	80	

Table 2.46 Permissible Output Currents (2/6)

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (total)	VCC IO (LQFP144)	P000 to P007, P306, P307, P310 to P312, P315 (Total of 14 pins)	ΣI_{OL}	—	—	80	mA
		P202 to P207, P302 to P304 (Total of 9 pins)		—	—	80	
		P100 to P107, P200, P201, P300, P301 (Total of 12 pins)		—	—	80	
		P800 to P803, PC00 to PC07 (Total of 12 pins)		—	—	80	
		PB00 to PB07 (Total of 8 pins)		—	—	80	
		PA00 to PA07 (Total of 8 pins)		—	—	80	
		P700 to P702, PE00 to PE07 (Total of 11 pins)		—	—	80	
	VCC IO (LQFP176, BGA176)	P000 to P007, P306, P307, P310 to P312, P315 (Total of 14 pins)	ΣI_{OL}	—	—	80	mA
		P202 to P207, P302 to P304 (Total of 9 pins)		—	—	80	
		P100 to P107, P200, P201, P300, P301, P804, P805 (Total of 14 pins)		—	—	80	
		P500 to P503, P800 to P803, PC00 to PC07 (Total of 16 pins)		—	—	80	
		PA04 to PA07, PB00 to PB07, PG00 to PG02 (Total of 15 pins)		—	—	80	
		P700 to P707, PA00 to PA03 (Total of 12 pins)		—	—	80	
		PE00 to PE07 (Total of 8 pins)		—	—	80	
	VCC IO (BGA224)	P000 to P007, P214, P215 (Total of 10 pins)	ΣI_{OL}	—	—	80	mA
		P306, P307, P310 to P312, P315, P208 to P213 (Total of 12 pins)		—	—	80	
		P112 to P115, P202 to P207, PF02 to PF05 (Total of 14 pins)		—	—	80	
		P108 to P111, P300 to P304, P804 to P807 (Total of 13 pins)		—	—	80	
		P100 to P107, P200, P201, P504 to P507 (Total of 14 pins)		—	—	80	
		P500 to P503, P800 to P803, PC05 to PC07 (Total of 11 pins)		—	—	80	
		PB04 to PB07, PC00 to PC04 (Total of 9 pins)		—	—	80	
		PB00 to PB03, PG04 to PG07 (Total of 8 pins)		—	—	80	
		PA04 to PA07, PG00 to PG03 (Total of 8 pins)		—	—	80	
		P700 to P707, PA00 to PA03 (Total of 12 pins)		—	—	80	
		PE00 to PE07, PF06 to PF09 (Total of 12 pins)		—	—	80	

Table 2.46 Permissible Output Currents (3/6)

Item				Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (total)	VCC IO (BGA320)	P000 to P015, P214, P215 (Total of 18 pins)		ΣI_{OL}	—	—	80	mA
		P306, P307, P310 to P312, P315, P208 to P213 (Total of 12 pins)			—	—	80	
		P112 to P115, P202 to P207, PF02 to PF05 (Total of 14 pins)			—	—	80	
		P108 to P111, P300 to P304, P804 to P807 (Total of 13 pins)			—	—	80	
		P100 to P107, P200, P201, P504 to P507 (Total of 14 pins)			—	—	80	
		P500 to P503, P800 to P803, PC05 to PC07(Total of 11 pins)			—	—	80	
		P512 to P515, PB04 to PB07, PC00 to PC04 (Total of 13 pins)			—	—	80	
		P510, P511, PB00 to PB03, PG04 to PG07 (Total of 10 pins)			—	—	80	
		P508, P509, PA04 to PA07, PG00 to PG03 (Total of 10 pins)			—	—	80	
		P704 to P707, PA00 to PA03, PG12 to PG15 (Total of 12 pins)			—	—	80	
		P700 to P703, P712 to P715, PG08 to PG11 (Total of 12 pins)			—	—	80	
		P708 to P711, PE00 to PE07, PF06 to PF09 (Total of 16 pins)			—	—	80	
	VCC2 IO	P600 to P607, P900 to P907, PD00 to PD07 (Total of 24 pins)		ΣI_{OL_VCC2}	—	—	80	mA
	AVCC0 IO	P400 to P415 (Total of 16 pins)		ΣI_{OL_AVCC0}	—	—	33	mA
	VCC_USB IO	PF00, PF01 (Total of 2 pins)*6		ΣI_{OL_VCCUSB}	—	—	33	mA
Permissible output high current (average value per pin)	I3C*1	I3C protocol mode*5, *7	LVO0E = 0	I_{OH}	—	—	–20	mA
			LVO0E = 1		—	—	–25	
	Other than above*3, *4	DRV1			—	—	–7.5	
		DRV2			—	—	–15	
		DRV3			—	—	–20	
		DRV4			—	—	–25	
		DRV5			—	—	–25	
		DRV6			—	—	–25	
		DRV7			—	—	–25	
		DRV8			—	—	–25	

Table 2.46 Permissible Output Currents (4/6)

Item				Symbol	Min.	Typ.	Max.	Unit
Permissible output high current (max. value per pin)	I3C*1	I3C protocol mode*5, *7	LVO0E = 0	I_{OH}	—	—	–40	mA
			LVO0E = 1		—	—	–50	
	Other than above*3, *4	DRV1			—	—	–15	
		DRV2			—	—	–30	
		DRV3			—	—	–40	
		DRV4			—	—	–50	
		DRV5			—	—	–50	
		DRV6			—	—	–50	
		DRV7			—	—	–50	
		DRV8			—	—	–50	
Permissible output high current (total)	VCC IO (LQFP100)	P001 to P007, P306, P307, P310 to P312, P315 (Total of 13 pins)		ΣI_{OH}	—	—	–80	mA
		P101 to P107, P200, P201, P300 to P304 (Total of 14 pins)			—	—	–80	
		PA04 to PA07, PB00 to PB06, PC00 to PC06 (Total of 18 pins)			—	—	–80	
		PA00 to PA03, PE00 to PE06 (Total of 11 pins)			—	—	–80	
	VCC IO (LQFP144)	P000 to P007, P306, P307, P310 to P312, P315 (Total of 14 pins)		ΣI_{OH}	—	—	–80	mA
		P202 to P207, P302 to P304 (Total of 9 pins)			—	—	–80	
		P100 to P107, P200, P201, P300, P301 (Total of 12 pins)			—	—	–80	
		P800 to P803, PC00 to PC07 (Total of 12 pins)			—	—	–80	
		PB00 to PB07 (Total of 8 pins)			—	—	–80	
		PA00 to PA07 (Total of 8 pins)			—	—	–80	
		P700 to P702, PE00 to PE07 (Total of 11 pins)			—	—	–80	
	VCC IO (LQFP176, BGA176)	P000 to P007, P306, P307, P310 to P312, P315 (Total of 14 pins)		ΣI_{OH}	—	—	–80	mA
		P202 to P207, P302 to P304 (Total of 9 pins)			—	—	–80	
		P100 to P107, P200, P201, P300, P301, P804, P805 (Total of 14 pins)			—	—	–80	
		P500 to P503, P800 to P803, PC00 to PC07 (Total of 16 pins)			—	—	–80	
		PA04 to PA07, PB00 to PB07, PG00 to PG02 (Total of 15 pins)			—	—	–80	
		P700 to P707, PA00 to PA03 (Total of 12 pins)			—	—	–80	
		PE00 to PE07 (Total of 8 pins)			—	—	–80	

Table 2.46 Permissible Output Currents (5/6)

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output high current (total)	VCC IO (BGA224)	P000 to P007, P214, P215 (Total of 10 pins)	ΣI_{OH}	—	—	–80	mA
		P306, P307, P310 to P312, P315, P208 to P213 (Total of 12 pins)		—	—	–80	
		P112 to P115, P202 to P207, PF02 to PF05 (Total of 14 pins)		—	—	–80	
		P108 to P111, P300 to P304, P804 to P807 (Total of 13 pins)		—	—	–80	
		P100 to P107, P200, P201, P504 to P507 (Total of 14 pins)		—	—	–80	
		P500 to P503, P800 to P803, PC05 to PC07 (Total of 11 pins)		—	—	–80	
		PB04 to PB07, PC00 to PC04 (Total of 9 pins)		—	—	–80	
		PB00 to PB03, PG04 to PG07 (Total of 8 pins)		—	—	–80	
		PA04 to PA07, PG00 to PG03 (Total of 8 pins)		—	—	–80	
		P700 to P707, PA00 to PA03 (Total of 12 pins)		—	—	–80	
		PE00 to PE07, PF06 to PF09 (Total of 12 pins)		—	—	–80	
	VCC IO (BGA320)	P000 to P015, P214, P215 (Total of 18 pins)	ΣI_{OH}	—	—	–80	mA
		P306, P307, P310 to P312, P315, P208 to P213 (Total of 12 pins)		—	—	–80	
		P112 to P115, P202 to P207, PF02 to PF05 (Total of 14 pins)		—	—	–80	
		P108 to P111, P300 to P304, P804 to P807 (Total of 13 pins)		—	—	–80	
		P100 to P107, P200, P201, P504 to P507 (Total of 14 pins)		—	—	–80	
		P500 to P503, P800 to P803, PC05 to PC07(Total of 11 pins)		—	—	–80	
		P512 to P515, PB04 to PB07, PC00 to PC04 (Total of 13 pins)		—	—	–80	
		P510, P511, PB00 to PB03, PG04 to PG07 (Total of 10 pins)		—	—	–80	
		P508, P509, PA04 to PA07, PG00 to PG03 (Total of 10 pins)		—	—	–80	
		P704 to P707, PA00 to PA03, PG12 to PG15 (Total of 12 pins)		—	—	–80	
		P700 to P703, P712 to P715, PG08 to PG11 (Total of 12 pins)		—	—	–80	
		P708 to P711, PE00 to PE07, PF06 to PF09 (Total of 16 pins)		—	—	–80	

Table 2.46 Permissible Output Currents (6/6)

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output high current (total)	VCC2 IO	P600 to P607, P900 to P907, PD00 to PD07 (Total of 24 pins)	ΣI_{OH_VCC2}	—	—	–80	mA
	AVCC0 IO	P400 to P415 (Total of 16 pins)	ΣI_{OH_AVCC0}	—	—	–33	mA
	VCC_USB IO	PF00, PF01 (Total of 2 pins)*6	ΣI_{OH_VCCUSB}	—	—	–33	mA

Caution: To protect the MCU's reliability, the output current values should not exceed the values in Table 2.46.
The average output current is obtained from the values for current measured over a period of 100 μs.

Note 1. When SDA00-A and SCL00-A are selected for the P102 and P103 pins.
Note 2. When SDAHSn-A and SCLHSn-A (n = 1, 2) are selected for the P106, P107, P200, and P201 pins.
Note 3. This is the driving ability as selected by the setting of the driving ability select (PmnPFS.DSCR[3:0]) bits.
Note 4. The values are for pins excluding USB0_DP, USB0_DM, USBHS_DP, and USBHS_DM.
Note 5. This characteristics depends on the setting of the LVO0E bit in the low-voltage operating characteristics control register (LVOCR).
Note 6. When a function other than USB0_DP or USB0_DM is selected.
Note 7. When the module operates in Push-Pull mode

2.4.5 Thermal Characteristics

2.4.5.1 Thermal Resistance Value

Table 2.47 Thermal Resistance Value (Reference)

Item	Package	Symbol	Max.	Unit	Test Conditions
Thermal resistance	176-pin LQFP (PLQP0176KJ-A)	θ_{ja}	29.6	°C/W	JESD51-2 and JESD51-7 compliant
	144-pin LQFP (PLQP0144KA-B)		34.3		
	100-pin LQFP (PLQP0100KP-A)		31.6		
	320-pin BGA (PLBG0320GD-A)		20.3		JESD51-2 and JESD51-9 compliant
	224-pin BGA (PLBG0224GE-A)		20.4		
	176-pin BGA (PLBG0176GG-A)		24.7		
	176-pin LQFP (PLQP0176KJ-A)	Ψ_{jt}	0.45	°C/W	JESD51-2 and JESD51-7 compliant
	144-pin LQFP (PLQP0144KA-B)		0.36		
	100-pin LQFP (PLQP0100KP-A)		0.45		
	320-pin BGA (PLBG0320GD-A)		0.17		JESD51-2 and JESD51-9 compliant
	224-pin BGA (PLBG0224GE-A)		0.19		
	176-pin BGA (PLBG0176GG-A)		0.21		

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

2.4.5.2 Supply Currents for the Peripheral Functions

Table 2.48 Operating Currents for the Peripheral Functions (Load Currents inside the Chip after Release from Module Stop State)

Item		Symbol	Max.	Unit	Register
SRAM1		I_{DD}	23.1	mA	MSTPCRA.MSTPA1
DMAC, DTC	DMACAa (8 channels), DTC	I_{DD}	7.04	mA	MSTPCRA.MSTPA22
	EXDMACAa (2 channels)		6.56		MSTPCRA.MSTPA29
Timers	GPTW (16 channels)	I_{DD}	5.54	mA	MSTPCRE.MSTPE31
	HRPWMb		0.09		MSTPCRD.MSTPD6
	TMRa (2 units)		0.07		MSTPCRF.MSTPF7, MSTPCRF.MSTPF6
	CMT (2 units)		0.06		MSTPCRF.MSTPF15, MSTPCRF.MSTPF14
	CMTW (2 units)		0.05		MSTPCRF.MSTPF13, MSTPCRF.MSTPF12
Communication interface	ESWM	I_{DD}	24.5	mA	MSTPCRC.MSTPC30
	ESC		1.25		MSTPCRC.MSTPC28, MSTPCRC.MSTPC29
	USB		0.25		MSTPCRB.MSTPB11
	USBHS		0.35		MSTPCRB.MSTPB12
	RSCI (13 channels)		5.34		MSTPCRB.MSTPB31 to MSTPCRB.MSTPB20, MSTPCRB.MSTPB0
	RI3C		0.21		MSTPCRB.MSTPB4
	RIICHS (2 channels)		0.40		MSTPCRB.MSTPB8, MSTPCRB.MSTPB7
	CANFDG (2 channels)		0.30		MSTPCRC.MSTPC25
	CANFD		0.14		MSTPCRC.MSTPC27
	RSPIA (3 channels)		0.67		MSTPCRB.MSTPB19, MSTPCRB.MSTPB18, MSTPCRC.MSTPC23
	SDHIc		0.08		MSTPCRC.MSTPC12
	PDMIF		0.03		MSTPCRC.MSTPC24
	DSMIFA (6 channels)		1.89		MSTPCRD.MSTPD9, MSTPCRD.MSTPD8
	XSPI (2 units), DOTF		9.37		MSTPCRB.MSTPB17, MSTPCRB.MSTPB16
	PCIF (2 units)		0.44		MSTPCRF.MSTPF31, MSTPCRF.MSTPF30
	SSIE (2 channels)		0.08		MSTPCRC.MSTPC8, MSTPCRC.MSTPC7
Analog	ADC16H	I_{DD}	4.73	mA	MSTPCRD.MSTPD21
	R12DAB		0.02		MSTPCRD.MSTPD20, MSTPCRD.MSTPD19
	Temperature sensor		0.01		MSTPCRD.MSTPD22
Safety, security function	CRCA	I_{DD}	0.01	mA	MSTPCRC.MSTPC1
	DOCA		0.01		MSTPCRC.MSTPC13
	RSIP		0.67		MSTPCRC.MSTPC31
	POEGd (4 channels)		0.22		MSTPCRD.MSTPD14, MSTPCRD.MSTPD13, MSTPCRD.MSTPD12, MSTPCRD.MSTPD11
Image processing	PDC	I_{DD}	0.04	mA	MSTPCRC.MSTPC2

Note: This table lists the internal load currents flowing inside the chip; they are not the I_{CC_DCDC} current supplied to the DCDC.
Note: The values listed are the increases in the currents after release from the module stop state.

Table 2.49 Leakage Current of the Peripheral Functions (Load Current inside the Chip)

Item	Tj = 105°C	Tj = 125°C	Unit	Control register
ESWM	9.48	18.3	mA	PDCTRESWM.PDDE

Note: The value given is the leakage current when the ESWM power domain is turned on.

2.4.5.3 Example of Calculation of T_a

The estimated maximum operating temperature (i.e., maximum ambient temperature) can be calculated from the maximum junction temperature and the thermal resistance value by using the following formula.

Tamax = Tjmax – (Iccmax × VCC × θja)

- Tamax: Maximum ambient temperature (maximum operating temperature) [°C]
- Tjmax: Maximum junction temperature [°C]
- Iccmax: Maximum operating current [A]
- θja: Thermal resistance value

For example, for the BGA320 package, when the LDO efficiency improvement function is enabled and the ICC current in maximal operation is 211 mA (typ) with VCC = 3.3 V, the calculation can proceed as shown below. In this case, the MCU can operate at ambient temperatures up to 111°C.

Tamax = 125°C – (0.211 A × 3.3 V × 20.3°C/W) = Approximately 111°C

Figure 2.7 shows the VCC voltage dependence of the maximum ambient temperature with a load current of 250 mA when the LDO efficiency improvement function is disabled.

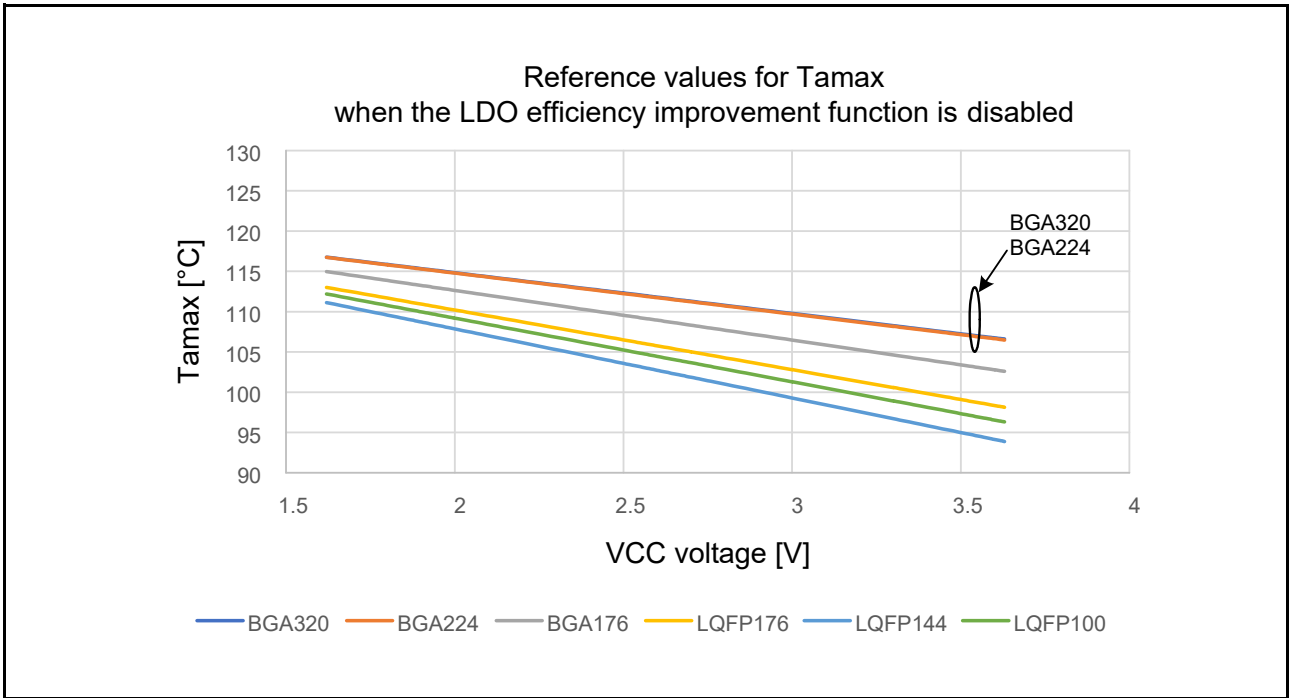


Figure 2.7 VCC Voltage Dependence of the Maximum Ambient Temperature with a Load Current of 250 mA When the LDO Efficiency Improvement Function Is Disabled

Figure 2.8 shows the VCC voltage dependence of the maximum ambient temperature with a load current of 250 mA when the LDO efficiency improvement function is enabled.

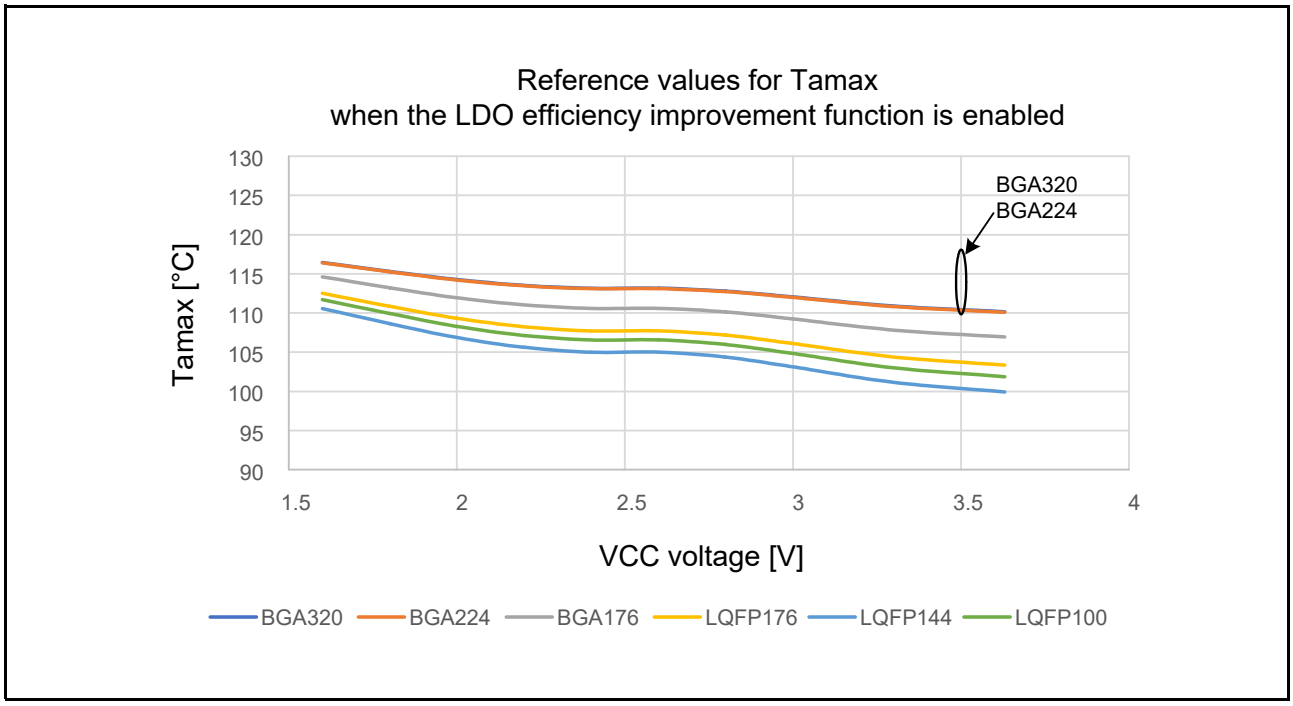


Figure 2.8 VCC Voltage Dependence of the Maximum Ambient Temperature with a Load Current of 250 mA When the LDO Efficiency Improvement Function Is Enabled

Figure 2.9 shows the VCC voltage dependence of the maximum ambient temperature with a load current of 200 mA when the DCDC supply is in use. Since the ICC current and power conversion efficiency of the DCDC supply vary with the VCC voltage, the values shown are only for reference and were calculated assuming a power conversion efficiency of approximately 70% at higher VCC voltages and approximately 85% at lower VCC voltages.

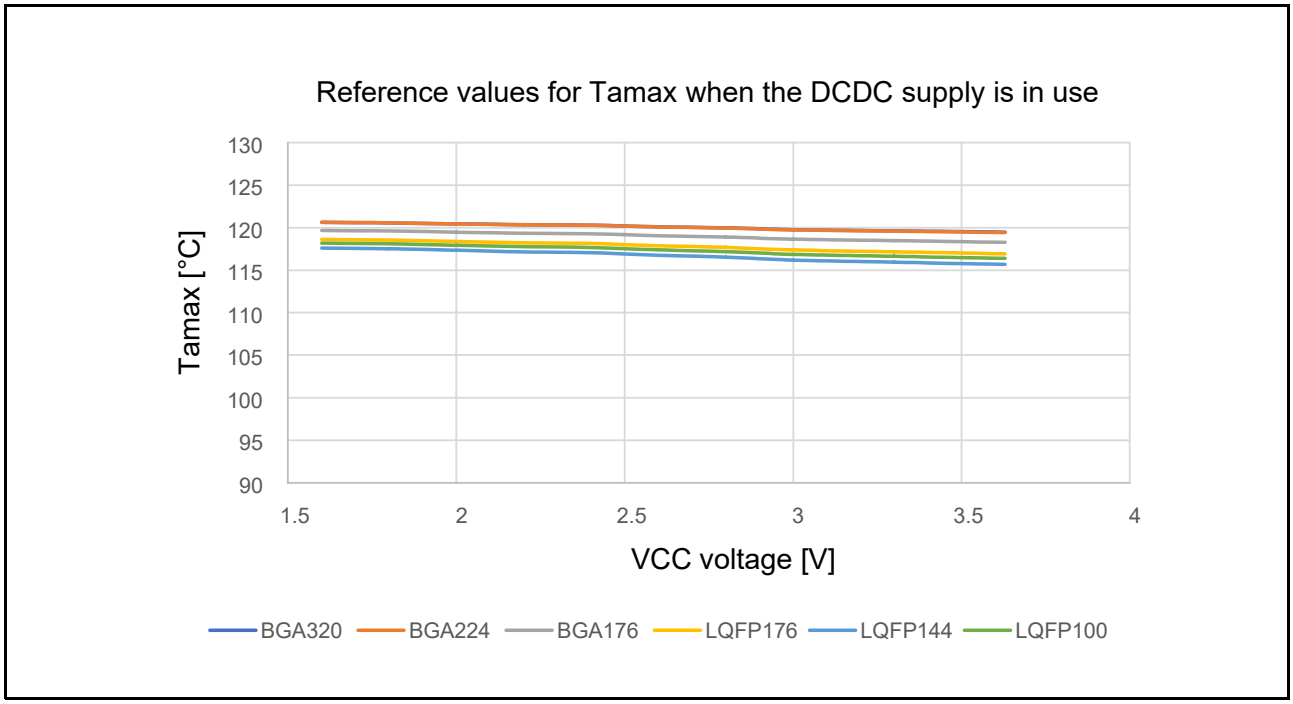


Figure 2.9 VCC Voltage Dependence of the Maximum Ambient Temperature with a Load Current of 200 mA When the DCDC Supply Is in Use

2.4.6 VCC Rising and Falling Slopes and Ripple Frequency

Table 2.50 Characteristics of VCC Rising and Falling Slopes When Power is Switched On and Off

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
VCC rising slope at power on*1		SrVCC	0.0084	—	4	ms/V	Figure 2.10
VCC falling slope at power off*2	VBATT function is disabled	SfVCC1	0.0084	—	—		
	VBATT function is enabled	SfVCC2	1.0000	—	—		

Note 1. When the VCC voltage changes from below V_{POR1} to above V_{POR1}
Note 2. When the VCC voltage changes from above V_{POR1} to below V_{POR1}

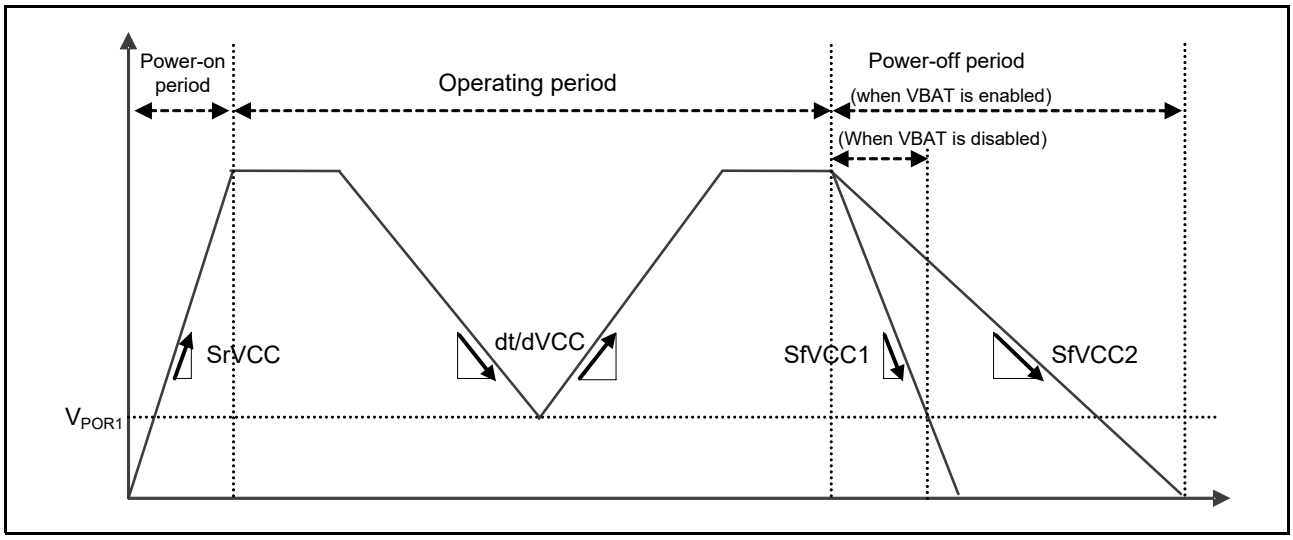


Figure 2.10 VCC Rising and Falling Slopes

Table 2.51 Characteristics of VCC Ripple Frequency and Rising and Falling Slope during Operation

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 2.11 $V_{r(VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.11 $V_{r(VCC)} \leq VCC \times 0.08$
		—	—	10		Figure 2.11 $V_{r(VCC)} \leq VCC \times 0.06$
Allowable voltage fluctuation rising and falling slope*1	dt/dVCC	1	—	—	ms/V	When the fluctuation in VCC exceeds VCC ± 10%

Note: The ripple voltage must be within the range between the upper (3.63 V) and lower (1.62 V) limits of VCC and satisfy the condition for allowable ripple frequency $f_{r(VCC)}$.
Note: When the fluctuation in VCC exceeds VCC ± 10%, the rate of change must be within the allowable voltage fluctuation rising and falling slope dt/dVCC.
Note 1. When the VCC voltage does not drop below V_{POR1}.

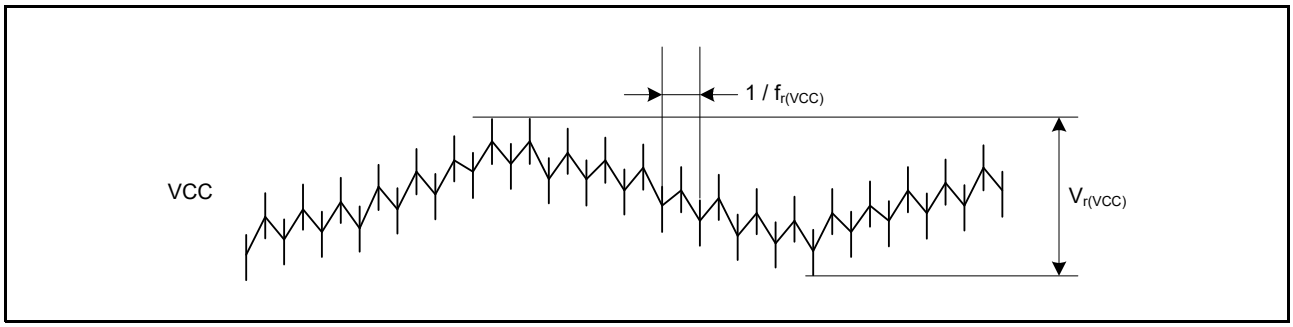


Figure 2.11 Ripple Waveform

2.5 AC Characteristics

2.5.1 Operating Frequency

Table 2.52 Operating Frequency

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Operating frequency	CPU clock (CPUCLK0)	For product part no. R5K574Mxy4xx (y = A, B, T, U)	f	—	—	600	MHz	VSCR_1 (DCDC mode) Voltage range 1 (external VDD mode)
				—	—	480		VSCR_2 (DCDC mode) Voltage range 2 (external VDD mode)
		For product part no. R5K574Mxy4xx (y = C, D, V, W)		—	—	480		VSCR_2 (DCDC mode) Voltage range 2 (external VDD mode)
		For product part no. R5K574Mxy4xx (y = E, F)		—	—	300		
	System clock (ICLK)			—	—	300		
	Peripheral module clock (PCLKA)*1			—	—	150		
	Peripheral module clock (PCLKB)			—	—	75		
	Peripheral module clock (PCLKC)			—	—	75		
	Peripheral module clock (PCLKD)			—	—	150		
	Peripheral module clock (PCLKE)			—	—	300		
	MRAM code bus clock (MRICLK)			—	—	300		
	MRAM peripheral bus clock (MRPCLK)			—	—	150		
	External bus clock	Synchronous clock (BCLK)		—	—	150		
		Asynchronous clock (BCLKA)		—	—	133		
	EBCLK pin output*2	3.0 V ≤ VCC ≤ 3.6 V		—	—	100		
		2.7 V ≤ VCC < 3.0 V		—	—	60		
	SDCLK pin output*2	3.0 V ≤ VCC ≤ 3.6 V		—	—	133		
		2.7 V ≤ VCC < 3.0 V		—	—	60		
	SCI clock (SCICLK)			—	—	120		
	SPI clock (SPICLK)			—	—	100		
	XSPI clock (XSPICLK)			—	—	266		
	CANFD core clock (CANFDCLK)			—	—	80		
	ADC clock (ADCCLK)			25	—	60		
	GPT clock (GPTCLK)*1			—	—	300		
	USB clock (USBCLK)			—	—	48		
	USBHS-PHY clock (USB60CLK)			—	—	60		
	I3C clock (I3CCLK)			—	—	100		
	ESWM clock (ESWCLK)			—	—	250		
	ESWM-PHY clock (ESWPHYCLK)			—	—	500		
	ESC clock (ESCCLK)			—	—	100		
	Ethernet-PHY clock (ETHPHYCLK)			—	—	50		
	DSMIF clock (DSMIFCLK)			—	—	200		

Note 1. When using PCLKA or GPTCLK at frequencies of and below 25 MHz or of and above 120 MHz, select the ADC clock (ADCCLK) as the A/D conversion clock (ADCLK).

Note 2. This is the case when the setting of the port drive capability bits in the PmnPFS register is for DRV7.

2.5.2 Clock Timing

Table 2.53 Timing of the EBCLK and SDCLK Pins Output

Conditions: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV7.

Item	VCC	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
ECLK pin output cycle time	3.0 V or higher	t_{Bcyc}	10.0	—	—	ns	Figure 2.12
	2.7 V or higher		16.6	—	—		
EBCLK pin output high pulse width	3.0 V or higher	t_{CH}	2.0	—	—	ns	
	2.7 V or higher		3.3	—	—		
EBCLK pin output low pulse width	3.0 V or higher	t_{CL}	2.0	—	—	ns	
	2.7 V or higher		3.3	—	—		
EBCLK pin output rising time	3.0 V or higher	t_{Cr}	—	—	3.0	ns	
	2.7 V or higher		—	—	5.0		
EBCLK pin output falling time	3.0 V or higher	t_{Cf}	—	—	3.0	ns	
	2.7 V or higher		—	—	5.0		
SDCLK pin output cycle time	3.0 V or higher	t_{SDcyc}	7.52	—	—	ns	
	2.7 V or higher		16.6	—	—		
SDCLK pin output high pulse width	3.0 V or higher	t_{CH}	1.0	—	—	ns	
	2.7 V or higher		2.2	—	—		
SDCLK pin output low pulse width	3.0 V or higher	t_{CL}	1.0	—	—	ns	
	2.7 V or higher		2.2	—	—		
SDCLK pin output rising time	3.0 V or higher	t_{Cr}	—	—	2.7	ns	
	2.7 V or higher		—	—	2.7		
SDCLK pin output falling time	3.0 V or higher	t_{Cf}	—	—	2.7	ns	
	2.7 V or higher		—	—	2.7		

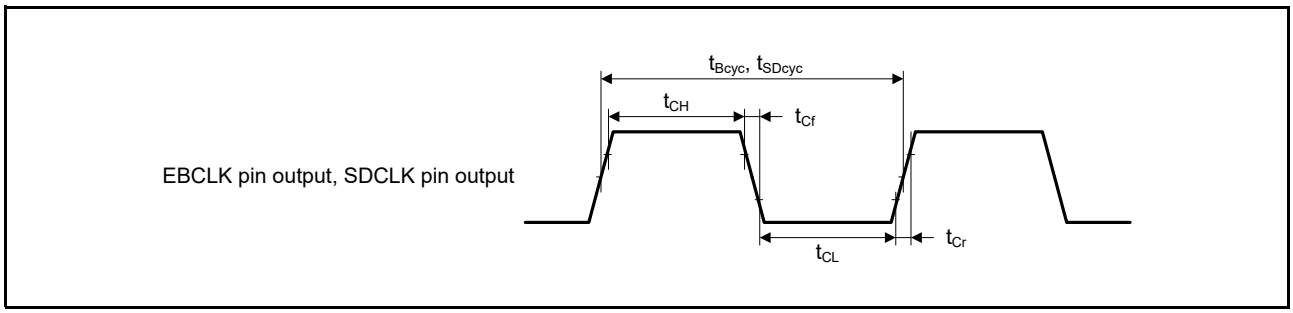


Figure 2.12 EBCLK and SDCLK Pins Output Timing

Table 2.54 EXTAL Clock Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{EXcyc}	20.80	—	—	ns	Figure 2.13
EXTAL external clock input high pulse width	t_{EXH}	5.30	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	5.30	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	3.0	ns	
EXTAL external clock falling time	t_{EXf}	—	—	3.0	ns	

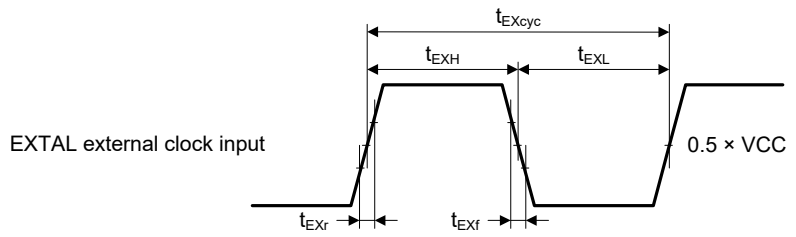


Figure 2.13 EXTAL External Clock Input Timing

Table 2.55 Main Clock Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	48	MHz	
Main clock oscillation stabilization wait time (crystal)*1	$t_{MAINOSCWT}$	—	—	—	ms	Figure 2.14

Note 1. When using the main clock, request evaluation by the manufacturer of the oscillator. For the time until the oscillation is stabilized, confirm the evaluation result by the manufacturer and set a value in the MOSCWTCR register that exceeds the manufacturer's recommended value. After having set the MOSCCR.MOSTP bit to start the main clock operation, wait until the oscillation is stabilized before using the main clock.

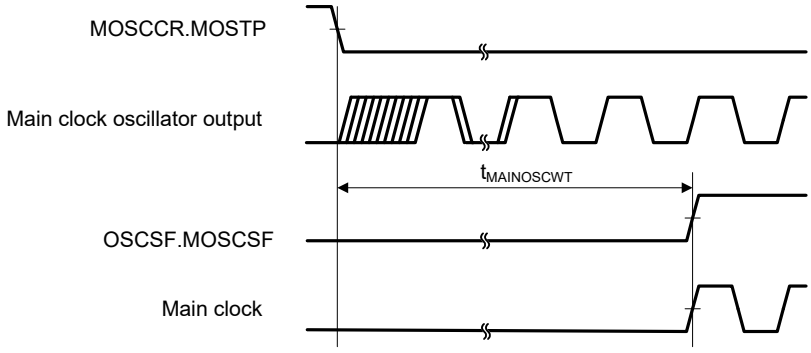


Figure 2.14 Main Clock Oscillator Start Timing

Table 2.56 LOCO and MOCO Clock Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock oscillation frequency	f_{LOCO}	29.4912	32.768	36.0448	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	26.0	μs	Figure 2.15
MOCO clock oscillation frequency	f_{MOCO}	7.2	8.0	8.8	MHz	
MOCO clock oscillation stabilization wait time	t_{MOCOWT}	—	—	3.5	μs	Figure 2.16

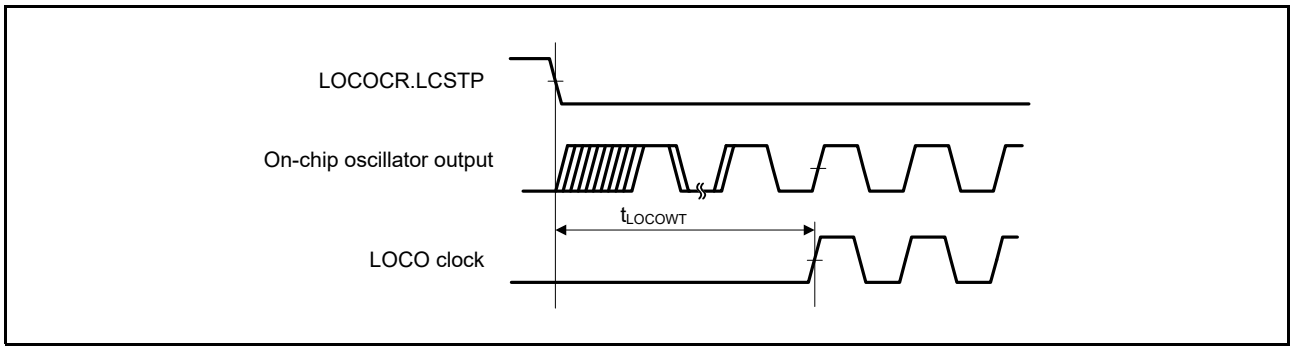


Figure 2.15 LOCO Clock Oscillation Start Timing

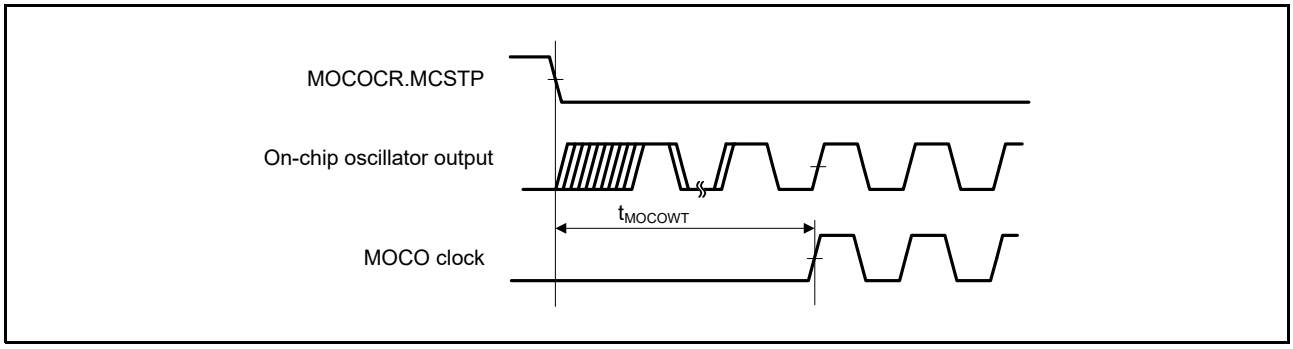


Figure 2.16 MOCO Clock Oscillation Start Timing

Table 2.57 HOCO Clock Timing

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	Without FLL	f_{HOCO16}	15.776	16.000	16.224	MHz	–20°C ≤ T_j ≤ 105°C
		f_{HOCO18}	17.748	18.000	18.252		
		f_{HOCO20}	19.720	20.000	20.280		
		f_{HOCO32}	31.552	32.000	32.448		
		f_{HOCO48}	47.328	48.000	48.672		
		f_{HOCO16}	15.712	16.000	16.288		–40°C ≤ T_j ≤ 125°C
		f_{HOCO18}	17.676	18.000	18.324		
		f_{HOCO20}	19.640	20.000	20.360		
		f_{HOCO32}	31.424	32.000	32.576		
		f_{HOCO48}	47.136	48.000	48.864		
	With FLL	f_{HOCO16}	15.960	16.000	16.040		–40°C ≤ T_j ≤ 125°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.955	18.000	18.045		
		f_{HOCO20}	19.950	20.000	20.050		
		f_{HOCO32}	31.920	32.000	32.080		
		f_{HOCO48}	47.880	48.000	48.120		
HOCO clock oscillation stabilization wait time*1		t_{HOCOWT}	—	—	15.0	μs	Figure 2.17
HOCO stop width time		$t_{HOCOSTP}$	1.0	—	—	μs	Figure 2.18
HOCO period jitter		—	–3.0	—	3.0	ps	
FLL stabilization wait time		t_{FLLWT}	—	—	1.92	ms	

Note 1. This value indicates the time that is required for the HOCO oscillation frequency (f_{HOCO}) to fall within the corresponding guaranteed range of error in the above table after release from the reset state.

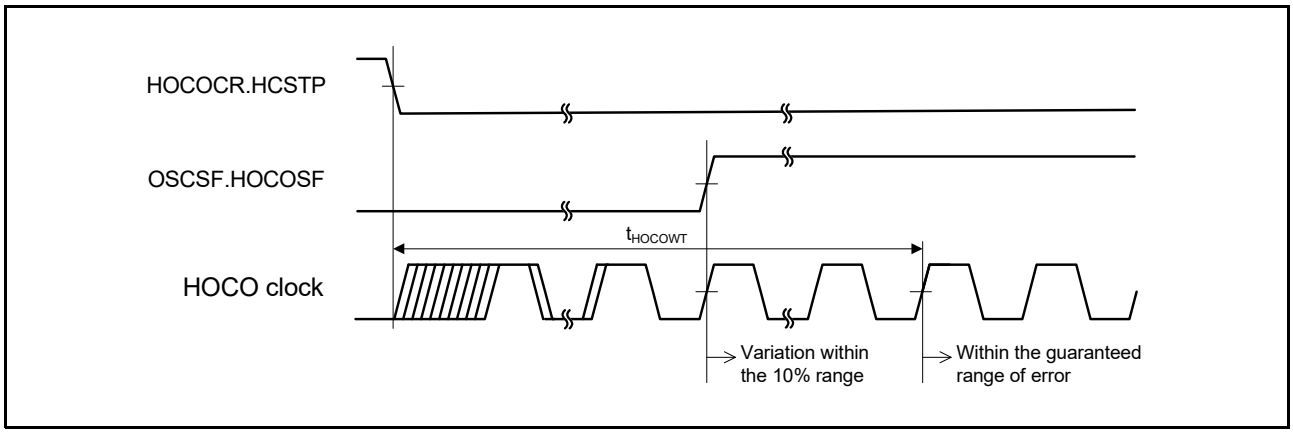


Figure 2.17 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

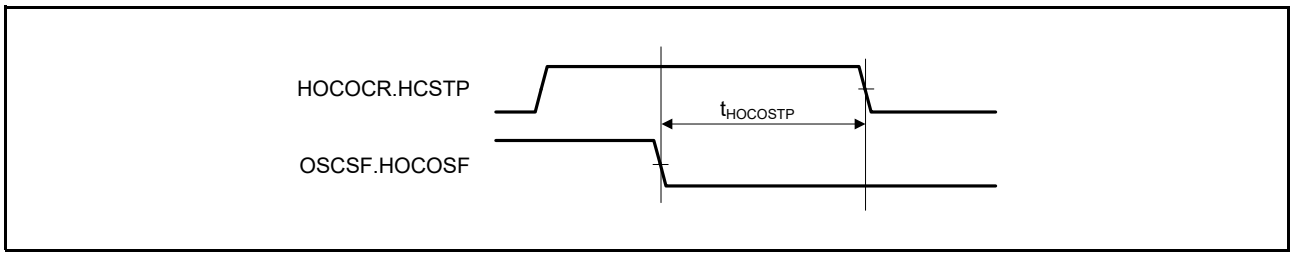
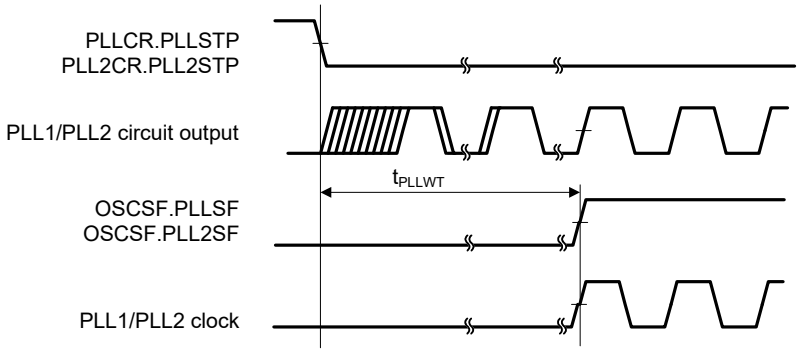


Figure 2.18 HOCO Stop Width Time

Table 2.58 PLL Clock Timing

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL1 clock oscillation frequency	VCO frequency		f_{PLL_VCO}	960	—	2400	MHz	—
	PLL output clock P	Part no. type 1	f_{PLL_P}	60	—	600		VSCR_1 (DCDC mode) Voltage range 1 (external VDD mode)
				60	—	480		VSCR_2 (DCDC mode) Voltage range 2 (external VDD mode)
		Part no. type 2		60	—	480		VSCR_2 (DCDC mode) Voltage range 2 (external VDD mode)
		Part no. type 3		60	—	300		
	PLL output clock Q	Part no. types 1 and 2	f_{PLL_Q}	106.6	—	500		—
		Part no. type 3		106.6	—	300		—
	PLL output clock R		f_{PLL_R}	106.6	—	500		—
PLL2 clock oscillation frequency	VCO frequency		f_{PLL_VCO}	960	—	2400	MHz	—
	PLL output clock P	Part no. types 1 and 2	f_{PLL_P}	60	—	500		—
		Part no. type 3		60	—	300		—
	PLL output clock Q	Part no. types 1 and 2	f_{PLL_Q}	106.6	—	500		—
		Part no. type 3		106.6	—	300		—
	PLL output clock R		f_{PLL_R}	106.6	—	500		—
PLL1/PLL2 clock oscillation stabilization wait time			t_{PLLWT}	—	—	50	μs	Figure 2.19
PLL1/PLL2 period jitter			—	—	±52	—	ps	—
PLL1/PLL2 long term jitter			—	—	±300	—	ps	Term: 1 μs, 10 μs

Part no. type 1: Products with part numbers of the form R5K574Mxy4xx (y = A, B, T, U)
Part no. type 2: Products with part numbers of the form R5K574Mxy4xx (y = C, D, V, W)
Part no. type 3: Products with part numbers of the form R5K574Mxy4xx (y = E, F)



Note 1. The PLL only starts operation after the main clock oscillation is stabilized.

Figure 2.19 PLL1/PLL2 Clock Oscillation Start Timing

Table 2.59 Sub-Clock Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillation frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization wait time*1	$t_{SUBOSCWT}$	—	—	—	s	Figure 2.20

Note 1. When using the sub-clock, request evaluation by the manufacturer of the oscillator. Regarding the oscillation stabilization wait time, refer to the resonator manufacturer's evaluation results and wait in the program for a time longer than the value recommended by the resonator manufacturer. After having set the SOSCCR.SOSTP bit to start the sub-clock operation, wait until the oscillation is stabilized before using the sub-clock.

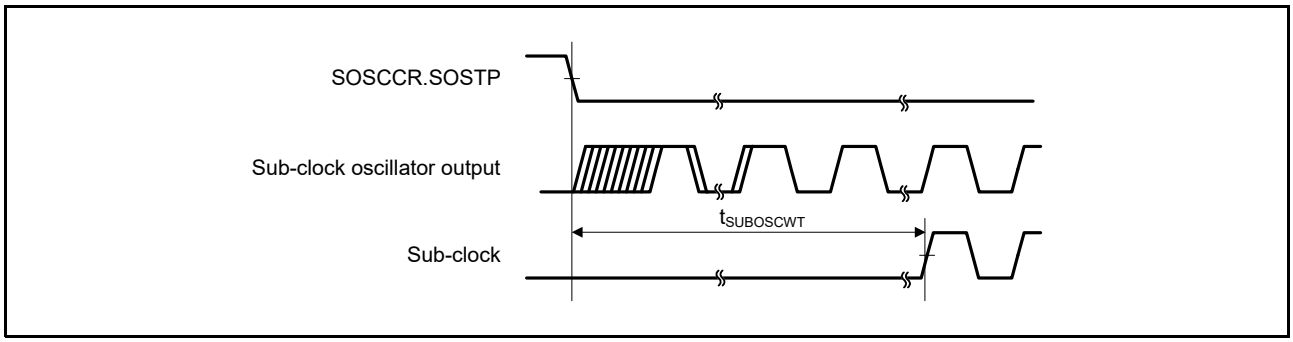


Figure 2.20 Sub-Clock Oscillation Start Timing

Table 2.60 EXCIN External Clock Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXCIN external clock input cycle time	t_{EXcyc}	27.7	—	—	μs	Figure 2.21
EXCIN external clock input frequency	t_{EXCIN}	—	—	36	kHz	
EXCIN external clock input high pulse width	t_{EXH}	11.08	—	—	μs	
EXCIN external clock input low pulse width	t_{EXL}	11.08	—	—	μs	
EXCIN external clock rising time	t_{EXr}	—	—	200	ns/V	
EXCIN external clock falling time	t_{EXf}	—	—	200	ns/V	

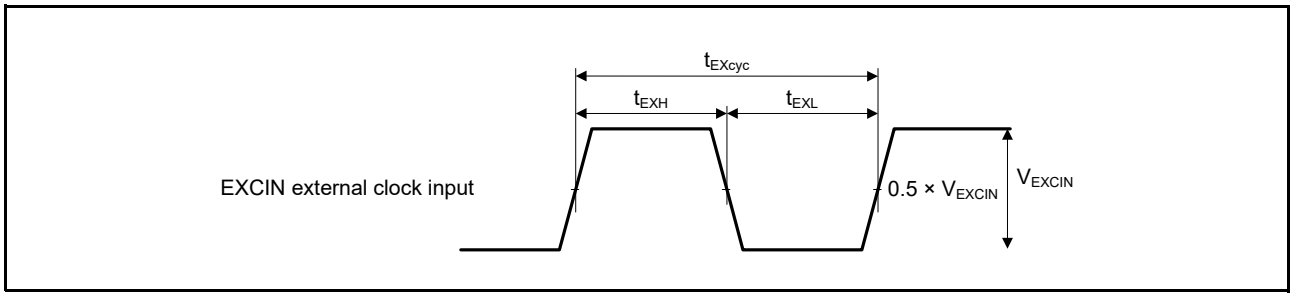
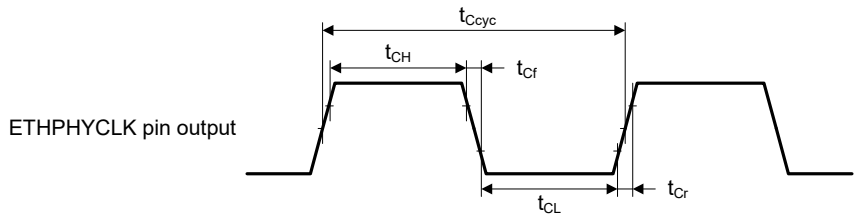


Figure 2.21 EXCIN External Clock Input Timing

Table 2.61 ETHPHYCLK Pin Output Timing

Conditions: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV3.
VCC = 2.70 to 3.63 V
Capacitive load C_L = 30 pF (during operation at 25 MHz), C_L = 15 pF (during operation at 50 MHz)

Item	Output Frequency	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
ETHPHYCLK pin output cycle time	25 MHz	t_{Ccyc}	—	40	—	ns	Figure 2.22
	50 MHz		—	20	—		
ETHPHYCLK pin high pulse width	25 MHz	t_{CH}	13	—	—	ns	
	50 MHz		6.5	—	—		
ETHPHYCLK pin low pulse width	25 MHz	t_{CL}	13	—	—	ns	
	50 MHz		6.5	—	—		
ETHPHYCLK pin rising time	25 MHz	t_{Cr}	—	—	3.3	ns	
	50 MHz		—	—	1.66		
ETHPHYCLK pin falling time	25 MHz	t_{Cf}	—	—	3.3	ns	
	50 MHz		—	—	1.66		



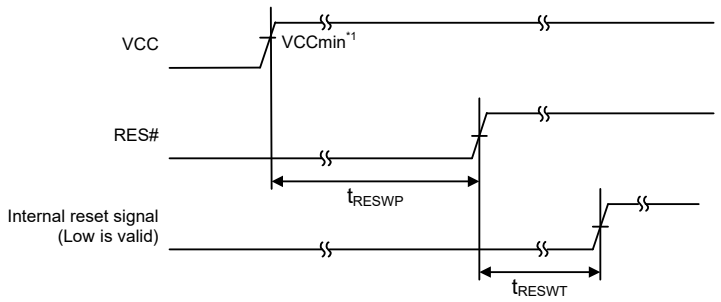
Test conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C_L = 30 pF or 15 pF

Figure 2.22 ETHPHYCLK Pin Output Timing

2.5.3 Reset Timing

Table 2.62 Reset Timing

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on		t_{RESWP}	2.40	—	—	ms	Figure 2.23
	Deep software standby mode 1	DPSBYCR.DCSSMODE = 01b	t_{RESWD}	0.51	—	—		Figure 2.24
		DPSBYCR.DCSSMODE = 10b		0.67	—	—		
		DPSBYCR.DCSSMODE = 11b		1.00	—	—		
		DPSBYCR.LDOSSMODE = 01b		0.51	—	—		
		DPSBYCR.LDOSSMODE = 10b		0.67	—	—		
		DPSBYCR.LDOSSMODE = 11b		1.00	—	—		
	Deep software standby mode 2	DPSBYCR.DCSSMODE = 01b		0.51	—	—		
		DPSBYCR.DCSSMODE = 10b		0.67	—	—		
		DPSBYCR.DCSSMODE = 11b		1.00	—	—		
		DPSBYCR.LDOSSMODE = 01b		0.51	—	—		
		DPSBYCR.LDOSSMODE = 10b		0.67	—	—		
		DPSBYCR.LDOSSMODE = 11b		1.00	—	—		
	Deep software standby mode 3	DPSBYCR.DCSSMODE = 01b		0.68	—	—		
		DPSBYCR.DCSSMODE = 10b		0.84	—	—		
		DPSBYCR.DCSSMODE = 11b		1.20	—	—		
		DPSBYCR.LDOSSMODE = 01b		0.68	—	—		
		DPSBYCR.LDOSSMODE = 10b		0.84	—	—		
		DPSBYCR.LDOSSMODE = 11b		1.20	—	—		
	Software standby mode		t_{RESWS}	0.55	—	—		
	CPU deep sleep mode (SCKSCR.CKSEL[2:0] = 100b)		$t_{RESWSODS}$	0.16	—	—		
	CPU deep sleep mode (Any setting for SCKSCR.CKSEL[2:0] other than 100b)		t_{RESWDS}	0.04	—	—		
Waiting time after release from the RES# pin reset			t_{RESWT}	—	78.7	79.1	μs	Figure 2.23
Waiting time after release from internal reset time (independent watchdog timer reset, watchdog timer reset, bus error reset, common memory error reset, software reset, local memory error reset)			t_{RESWT2}	—	78.7	79.1	μs	
RESOUT# output pulse width		OFS1.ROWSEL[2:0] = 000b	t_{ROUT}	0.25	0.28	0.31	ms	Figure 2.25
		OFS1.ROWSEL[2:0] = 100b		0.50	0.55	0.62		
		OFS1.ROWSEL[2:0] = 101b		1.00	1.10	1.23		
		OFS1.ROWSEL[2:0] = 110b		5.00	5.50	6.12		
		OFS1.ROWSEL[2:0] = 111b		10.0	11.0	12.2		



Note 1. VCCmin is the minimum guaranteed voltage of the MCU.

Figure 2.23 Reset Input Timing at Power-On

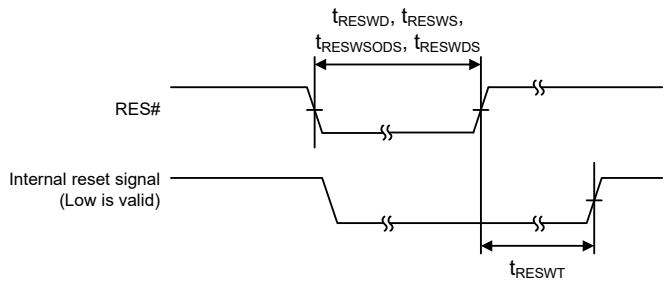
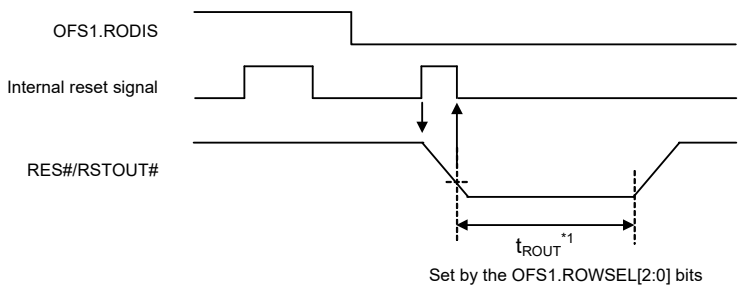


Figure 2.24 Reset Input Timing



Note 1. t_{ROUT} is the value counted for the time set by OFS1.ROWSEL[2:0] after the internal reset is released. After the count ends, the RSTOUT# output is released.

Figure 2.25 RSTOUT# Output Operation

2.5.4 Timing of Return from Low Power Consumption Modes

The following symbols are used in this section to represent the frequencies of the individual clocks.

f_{MOCO}: MOCO clock (8 MHz)
$f_{MOCOmin}$: Minimum frequency of the MOCO clock (7.2 MHz)
f_{SRCCLK}: System clock shown in Table 2.64 to Table 2.67
f_{PLL}: PLL1 circuit clock
f_{ICLK}: System clock ICLK
f_{MOSC}: MOSC clock
f_{HOCO}: HOCO clock
f_{SOSC}: SOSC clock (32.768 kHz)

Table 2.63 Time to Return from CPU Deep Sleep Mode

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Time to return from CPU deep sleep mode	t_{DSLP}	—	6.13	9.44	μs	ICLK = 300 MHz

Note: To calculate the time to return at a frequency that differs from the condition in testing, use the following formula.
t_{DSLP} (typ.) = 44 / f_{MOCO} + 9 / f_{ICLK} + 0.6 [μs], t_{DSLP} (max.) = 44 / $f_{MOCOmin}$ + 9 / f_{ICLK} + 3.3 [μs]
(f_{MOCO}: MOCO frequency [MHz], $f_{MOCOmin}$: Minimum frequency of MOCO [MHz], f_{ICLK}: ICLK frequency [MHz])

Table 2.64 Time to Return from Software Standby Mode 1

Item	Input Clock Source		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL1 output clock P	MOSC (Crystal resonator is connected.)	Oscillation continues.*1	t_{SBYPC}	—	132	194	μs	PLL1P = 300 MHz ICLK = MRICLK = PCLKE = 300 MHz PCLKA = PCLKD = MRPCLK = BCLK = 150 MHz PCLKB = 75 MHz (divide-by-4)
		Oscillation stops.*1		—	2209	2499		
	MOSC (External clock is connected.)		t_{SBYPE}	—	132.5	194		
	HOCO	Oscillation continues.*2	t_{SBYPH}	—	132.5	194		
		Oscillation stops.*2		—	142.7	205		
Main clock oscillator (MOSC)	Crystal resonator	Oscillation continues.*1	t_{SBYMC}	—	24.3	62.4	μs	Main clock = 48 MHz ICLK = 48 MHz
		Oscillation stops.*1		—	2091	2368		
	External clock		t_{SBYEX}	—	24.3	62.4		
High-speed on-chip oscillator (HOCO)		Oscillation continues.*2	t_{SBYHO}	—	22.9	25.7	μs	High-speed clock = 48 MHz ICLK = 48 MHz
		Oscillation stops.*2		—	25.4	70.1		
Sub-clock oscillator (SOSC)			t_{SBYSC}	—	569	569	μs	Sub-clock = 32.768 kHz ICLK = 32.768 kHz
Middle-speed on-chip oscillator (MOCO)			t_{SBYMO}	—	23.9	26.7	μs	Middle-speed clock = 8 MHz ICLK = 8 MHz

Note 1. The setting of the MOSCSOKP bit in the main clock oscillator standby control register (MOSCSCR) determines this. When MOSCSOKP = 1, oscillation will be continuing. When MOSCSOKP = 0, oscillation will be stopped.
Note 2. The setting of the HCSTP bit in the high-speed on-chip oscillator control register (HOCOCR) determines this. When HCSTP = 0, oscillation will be continuing. When HCSTP = 1, oscillation will be stopped.

Table 2.65 Formula for Calculating the Time to Return from Software Standby Mode 1

Item	Input Clock Source		Symbol	Formula (Typ.)	Formula (Max.)
PLL1 output clock P	MOSC (Crystal resonator is connected.)	Oscillation continues.*1	t_{SBYPC}	FG + MAX (oscillation stabilization time (129.8), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (oscillation stabilization time (190.7), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
		Oscillation stops.*1		FG + MAX (($t_{MAINOSCWT}$ + 118.3), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (($t_{MAINOSCWT}$ + 178), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
	MOSC (External clock is connected.)		t_{SBYPE}	FG + MAX (oscillation stabilization time (129.8), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (oscillation stabilization time (190.7), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
	HOCO	Oscillation continues.*2	t_{SBYPH}	FG + MAX (oscillation stabilization time (129.8), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (oscillation stabilization time (190.7), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
		Oscillation stops.*2		FG + MAX (140, B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (202, B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
Main clock oscillator (MOSC)	Crystal resonator	Oscillation continues.*1	t_{SBYMC}	FG + MAX (oscillation stabilization time (11.5), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{MOSC}))	FG + MAX (oscillation stabilization time (59.3), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{MOSC}))
		Oscillation stops.*1		FG + MAX ($t_{MAINOSCWT}$, B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (($t_{MAINOSCWT}$ + 46.6), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
	External clock		t_{SBYEX}	FG + MAX (oscillation stabilization time (11.5), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{MOSC}))	FG + MAX (oscillation stabilization time (59.3), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{MOSC}))
High-speed on-chip oscillator (HOCO)		Oscillation continues.*2	t_{SBYHO}	FG + MAX (oscillation stabilization time (0), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{HOCO}))	
		Oscillation stops.*2		FG + MAX (20, B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (67, B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
Sub-clock oscillator (SOSC)			t_{SBYSC}	FG + MAX (oscillation stabilization time (0), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{SOSC}))	
Middle-speed on-chip oscillator (MOCO)			t_{SBYMO}	FG + MAX (oscillation stabilization time (0), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{MOCO}))	

The symbols used in the table above represent the following value and calculation results.

n: The larger of the frequency division values set by the SCKDIVCR and SCKDIVCR2 registers.
Typ. value: FG = 14/f_{MOCO} + 2/f_{ICLK}
Max. value: FG = 14/$f_{MOCOmin}$ + 2/f_{ICLK}
Typ. value: B = Oscillation stabilization time/f_{MOCO} + 158/f_{MOCO} + 0.3
Max. value: B = Oscillation stabilization time/$f_{MOCOmin}$ + 158/f_{MOCO} + 0.59
Typ. value: C = (10.5 + 2.5n)/f_{MOCO} + 2.5/f_{SRCCLK} + 2/f_{ICLK}
Max. value: C is obtained by the same formula as for the typ. value.
Typ. value: D = 7/f_{MOCO} + 8/f_{ICLK}
Max. value: D = 7/$f_{MOCOmin}$ + 8/f_{ICLK}
Typ. value: H = 2/f_{ICLK}
Max. value: H is obtained by the same formula as for the typ. value.

$t_{MAINOSCWT}$: Main clock oscillation stabilization wait time

Note: In the formulae above, when no distinction is made between Typ. and Max., use the same formula for the calculation.

Note 1. The setting of the MOSCSOKP bit in the main clock oscillator standby control register (MOSCSCR) determines this. When MOSCSOKP = 1, oscillation will be continuing. When MOSCSOKP = 0, oscillation will be stopped.

Note 2. The setting of the HCSTP bit in the high-speed on-chip oscillator control register (HOCOCR) determines this. When HCSTP = 0, oscillation will be continuing. When HCSTP = 1, oscillation will be stopped.

Table 2.66 Time to Return from Software Standby Mode 2

Conditions: The SS2FR bit in software standby control register 1 (SSCR1) is set to 1 (fast return function is enabled) and the SS2LP[1:0] bits are set to SS2LP_1 (low power setting 1).
The VSCM[2:0] bits in the voltage scaling control register (VSCR) are set to 010b (0.90 V).
The SVMCM[2:0] bits in the SSTBY voltage scaling control register (SVSCR) are set to 010b (0.90 V).
The LDOSTP bits in both of the PLLn-LDO control registers (PLLnLDOCR, n = 1, 2) are set to 1 (LDO is stopped).

Item	Input Clock Source		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL1 output clock P	MOSC (Crystal resonator is connected.)	Oscillation continues.*1	t_{SBYPC}	—	294	355	μs	PLL1P = 300 MHz ICLK = MRICLK = PCLKE = 300 MHz PCLKA = PCLKD = MRPCLK = BCLK = 150 MHz PCLKB = 75 MHz (divide-by-4)
		Oscillation stops.*1		—	2370	2660		
	MOSC (External clock is connected.)		t_{SBYPE}	—	294	355		
	HOCO	Oscillation continues.*2	t_{SBYPH}	—	294	355		
		Oscillation stops.*2		—	304	367		
Main clock oscillator (MOSC)	Crystal resonator	Oscillation continues.*1	t_{SBYMC}	—	202	251	μs	Main clock = 48 MHz ICLK = 48 MHz
		Oscillation stops.*1		—	2252	2529		
	External clock		t_{SBYEX}	—	202	251		
High-speed on-chip oscillator (HOCO)		Oscillation continues.*2	t_{SBYHO}	—	200	243	μs	High-speed clock = 48 MHz ICLK = 48 MHz
		Oscillation stops.*2		—	203	252		
Sub-clock oscillator (SOSC)			t_{SBYSC}	—	729	729	μs	Sub-clock = 32.768 kHz ICLK = 32.768 kHz
Middle-speed on-chip oscillator (MOCO)			t_{SBYMO}	—	201	244	μs	Middle-speed clock = 8 MHz ICLK = 8 MHz

Note 1. The setting of the MOSCSOKP bit in the main clock oscillator standby control register (MOSCSCR) determines this. When MOSCSOKP = 1, oscillation will be continuing. When MOSCSOKP = 0, oscillation will be stopped.
Note 2. The setting of the HCSTP bit in the high-speed on-chip oscillator control register (HOCOCR) determines this. When HCSTP = 0, oscillation will be continuing. When HCSTP = 1, oscillation will be stopped.

Table 2.67 Formula for Calculating the Time to Return from Software Standby Mode 2

Item	Input Clock Source		Symbol	Formula (Typ.)	Formula (Max.)
PLL1 output clock P	MOSC (Crystal resonator is connected.)	Oscillation continues.*1	t_{SBYPC}	FG + MAX (oscillation stabilization time (129.8), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (oscillation stabilization time (190.7), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
		Oscillation stops.*1		FG + MAX (($t_{MAINOSCWT}$ + 118.3), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (($t_{MAINOSCWT}$ + 178), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
	MOSC (External clock is connected.)		t_{SBYPE}	FG + MAX (oscillation stabilization time (129.8), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (oscillation stabilization time (190.7), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
	HOCO	Oscillation continues.*2	t_{SBYPH}	FG + MAX (oscillation stabilization time (129.8), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (oscillation stabilization time (190.7), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
		Oscillation stops.*2		FG + MAX (140, B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (202, B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
Main clock oscillator (MOSC)	Crystal resonator	Oscillation continues.*1	t_{SBYMC}	FG + MAX (oscillation stabilization time (11.5), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{MOSC}))	FG + MAX (oscillation stabilization time (59.3), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{MOSC}))
		Oscillation stops.*1		FG + MAX ($t_{MAINOSCWT}$, B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (($t_{MAINOSCWT}$ + 46.6), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
	External clock		t_{SBYEX}	FG + MAX (oscillation stabilization time (11.5), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{MOSC}))	FG + MAX (oscillation stabilization time (59.3), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{MOSC}))
High-speed on-chip oscillator (HOCO)		Oscillation continues.*2	t_{SBYHO}	FG + MAX (oscillation stabilization time (0), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{HOCO}))	
		Oscillation stops.*2		FG + MAX (20, B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))	FG + MAX (67, B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{PLL}))
Sub-clock oscillator (SOSC)			t_{SBYSC}	FG + MAX (oscillation stabilization time (0), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{SOSC}))	
Middle-speed on-chip oscillator (MOCO)			t_{SBYMO}	FG + MAX (oscillation stabilization time (0), B, C) + MAX (D, H + (2/f_{ICLK} + 2n/f_{MOCO}))	

The symbols used in the table above represent the following value and calculation results.

n: The larger of the frequency division values set by the SCKDIVCR and SCKDIVCR2 registers.
Typ. value: FG = CYC + 2/f_{ICLK}
Max. value: FG = CYC + 2/f_{ICLK} (See Table 2.68 for CYC values.)
Typ. value: B = Oscillation stabilization time/f_{MOCO} + 193/f_{MOCO} + 11.6
Max. value: B = Oscillation stabilization time/$f_{MOCOmin}$ + 193/f_{MOCO} + 51
Typ. value: C = (10.5 + 2.5n)/f_{MOCO} + 2.5/f_{SRCCLK} + 2/f_{ICLK}
Max. value: C is obtained by the same formula as for the typ. value.
Typ. value: D = 18/f_{MOCO} + 9/f_{ICLK}
Max. value: D = 18/$f_{MOCOmin}$ + 9/f_{ICLK}
Typ. value: H = 2/f_{ICLK}
Max. value: H is obtained by the same formula as for the typ. value.

$t_{MAINOSCWT}$: Main clock oscillation stabilization wait time

Note: In the formulae above, when no distinction is made between Typ. and Max., use the same formula for the calculation.

Note 1. The setting of the MOSCSOKP bit in the main clock oscillator standby control register (MOSCSCR) determines this. When MOSCSOKP = 1, oscillation will be continuing. When MOSCSOKP = 0, oscillation will be stopped.

Note 2. The setting of the HCSTP bit in the high-speed on-chip oscillator control register (HOCOCR) determines this. When HCSTP = 0, oscillation will be continuing. When HCSTP = 1, oscillation will be stopped.

Table 2.68 CYC Value

SSCR1.SS2LP[1:0]	VSCR.VSCM[2:0]	SVSCR.SVSCM[2:0]	CYC	Unit	Remarks
SS2LP_0	VSCR_1	SVSCR_1	237	Cycles	*1
		SVSCR_2	379		—
		SVSCR_3	591		
		SVSCR_4	696		
		SVSCR_5	802		
	VSCR_2	SVSCR_1	379		—
		SVSCR_2	237		*1
		SVSCR_3	538		—
		SVSCR_4	643		
		SVSCR_5	749		
SS2LP_1	VSCR_1	SVSCR_2	514	Cycles	—
		SVSCR_3	726		
		SVSCR_4	831		
		SVSCR_5	937		
	VSCR_2	SVSCR_2	459		*2
		SVSCR_3	673		—
		SVSCR_4	778		
		SVSCR_5	884		

Note 1. When the LDOSTP bits in both of the PLLn-LDO control registers (PLLnLDOCR, n = 1, 2) are set to 1 (LDO is stopped) or the SKEEP bits in both registers are set to 1 (the PLLn-LDO state before software standby mode 2 is retained), CYC is 56 if both the LDOSTP bit and SKEEP bit in the HOCO/LCO control register (HOCOLDOCR) are set to 0; CYC is 27 if either of the bits is set to1.

Note 2. When the SS2FR bit in software standby control register 1 (SSCR1) is set to 1 (fast return function is enabled), CYC is 162 if the LDOSTP bits in both of the PLLn-LDO control registers (PLLnLDOCR, n = 1, 2) are set to 1 (LDO is stopped) or the SKEEP bits in both registers are set to 1 (the PLLn-LDO state before software standby mode 2 is retained); otherwise, CYC is 327.

Table 2.69 Time to Return from Deep Software Standby Mode

Item		DPSBYCR Setting	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
DCDC mode	DSTBY1	DCSSMODE = 01b	t_{DBSY}	—	296	346	μs	Figure 2.27
		DCSSMODE = 10b		—	456	506		
		DCSSMODE = 11b		—	776	826		
	DSTBY2	DCSSMODE = 01b		—	296	346		
		DCSSMODE = 10b		—	456	506		
		DCSSMODE = 11b		—	776	826		
	DSTBY3	DCSSMODE = 01b		—	483	604		
		DCSSMODE = 10b		—	643	764		
		DCSSMODE = 11b		—	963	1084		
LDO mode	DSTBY1	LDOSSMODE = 01b	t_{DBSY}	—	208	268	μs	Figure 2.27
		LDOSSMODE = 10b		—	226	307		
		LDOSSMODE = 11b		—	250	353		
	DSTBY2	LDOSSMODE = 01b		—	262	291		
		LDOSSMODE = 10b		—	262	307		
		LDOSSMODE = 11b		—	262	353		
	DSTBY3	LDOSSMODE = 01b		—	449	549		
		LDOSSMODE = 10b		—	449	565		
		LDOSSMODE = 11b		—	449	611		
Waiting time after release from the deep software standby mode			t_{DBSYWT}	22.2	—	33.6	μs	

DSTBY1: Deep software standby mode 1
DSTBY2: Deep software standby mode 2
DSTBY3: Deep software standby mode 3

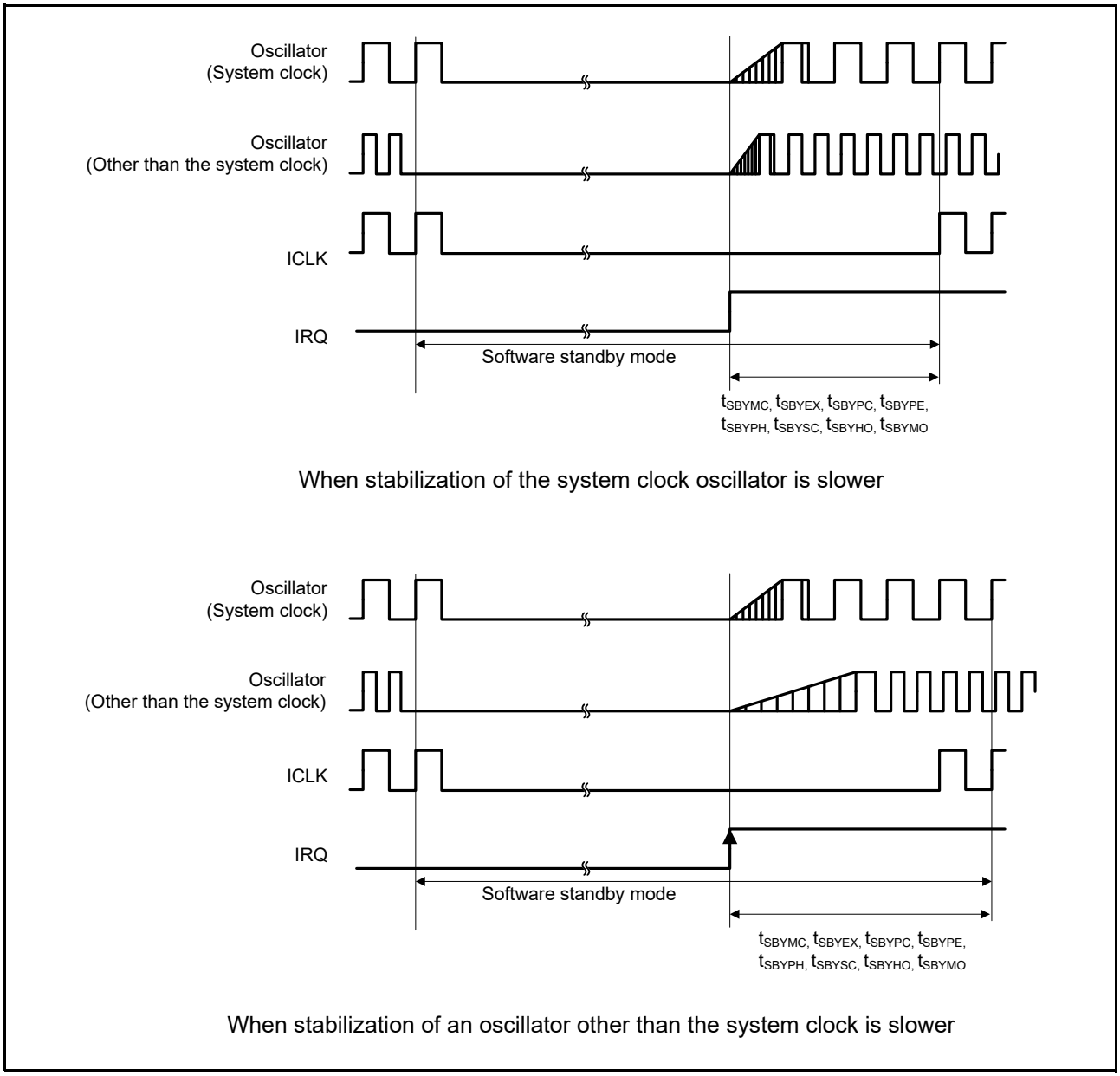


Figure 2.26 Timing of Return from Software Standby Mode

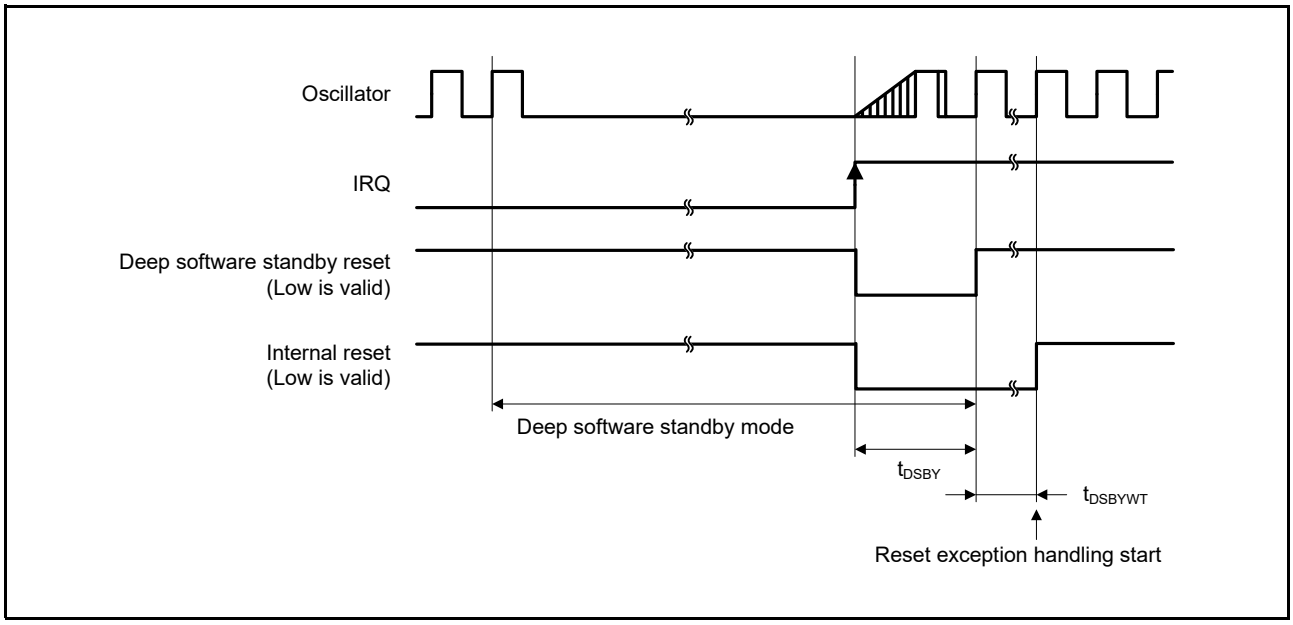


Figure 2.27 Timing of Return from Deep Software Standby Mode

2.5.5 Control Signal Timing

Table 2.70 Control Signal Timing

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	NMI digital filter disabled	$t_{PBcyc} \times 2 \leq 200$ ns	t_{NMIW}	200	—	—	ns	Figure 2.28
		$t_{PBcyc} \times 2 > 200$ ns		$t_{PBcyc} \times 2$*1	—	—		
	NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns		200	—	—		
		$t_{NMICK} \times 3 > 200$ ns		$t_{NMICK} \times 3.5$*2	—	—		
IRQ pulse width	IRQ digital filter disabled	$t_{PBcyc} \times 2 \leq 200$ ns	t_{IRQW}	200	—	—	ns	Figure 2.29
		$t_{PBcyc} \times 2 > 200$ ns		$t_{PBcyc} \times 2$*1	—	—		
	IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns		200	—	—		
		$t_{IRQCK} \times 3 > 200$ ns		$t_{IRQCK} \times 3.5$*3	—	—		

Note: In software standby mode, the minimum value is 200 ns.
Note: When switching system clock sources, add 4 clock cycles of the clock source you are switching to.
Note 1. t_{PBcyc}: PCLKB cycle
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

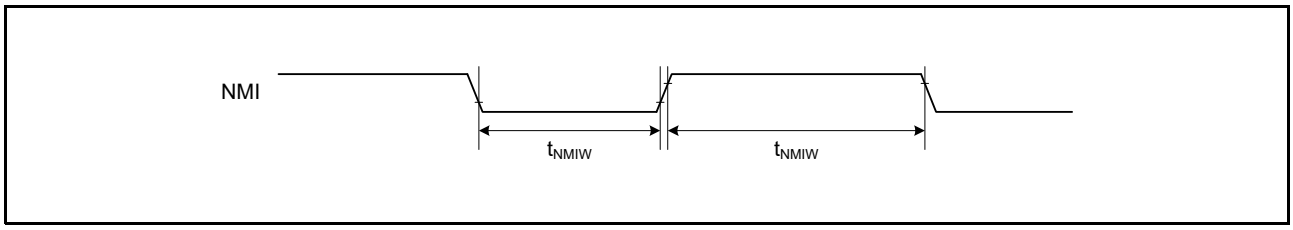


Figure 2.28 NMI Interrupt Input Timing

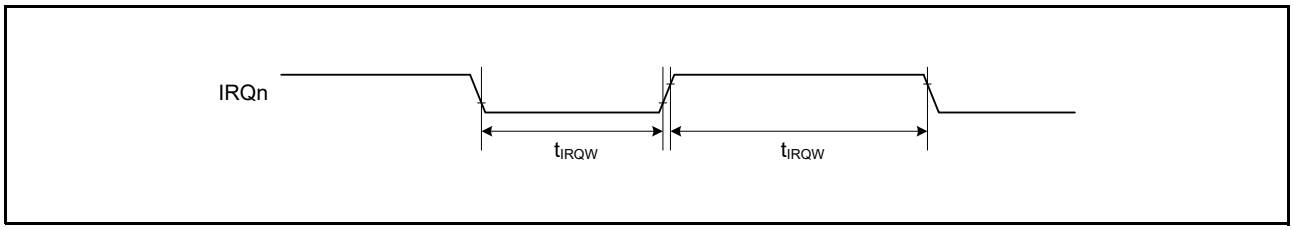


Figure 2.29 IRQ Interrupt Input Timing

2.5.6 Bus Timing

Table 2.71 Bus Timing (1)

Conditions: With the CS area controller in use
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the EBCLK pin are set for DRV7.
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to pins other than the EBCLK pin are set for DRV3.
EBCLK = 100 MHz,
VCC = VCC2 = 3.0 to 3.63 V, C = 15 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	0.5	10.8	ns	Figure 2.30 to Figure 2.37
Byte control delay time	t_{BCD}	0.5	10.8	ns	
CS# delay time	t_{CSD}	0.5	10.8	ns	
ALE delay time	t_{ALED}	0.5	10.8	ns	
RD# delay time	t_{RSD}	0.5	10.8	ns	
Read data setup time	t_{RDS}	10.8	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	0.5	10.8	ns	
Write data delay time	t_{WDD}	0.5	10.8	ns	
Write data hold time	t_{WDH}	0.5	—	ns	
WAIT# setup time	t_{WTS}	10.8	—	ns	
WAIT# hold time	t_{WTH}	0	—	ns	
BREQ# setup time	t_{BRS}	12.5	—	ns	
BREQ# hold time	t_{BRH}	0	—	ns	
BACK# delay time	t_{BAC}	0.5	12.5	ns	
Bus release time	t_{BRL}	—	12.5	ns	
Bus acquisition time	t_{BAQ}	—	12.5	ns	

Note: This table only applies when pins with the suffix -A, indicating the group name, as part of the pin name are in use.
Note: The above characteristics are only guaranteed for products with part numbers of the form R5K574Mxx4yy (yy = BG, BD, AE).

Table 2.72 Bus Timing (2)

Conditions: With the CS area controller in use
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the EBCLK pin are set for DRV7.
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to pins other than the EBCLK pin are set for DRV3.
EBCLK = 60 MHz,
VCC = VCC2 = 2.7 to 3.63 V, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	0.5	12.5	ns	Figure 2.30 to Figure 2.37
Byte control delay time	t_{BCD}	0.5	12.5	ns	
CS# delay time	t_{CSD}	0.5	12.5	ns	
ALE delay time	t_{ALED}	0.5	12.5	ns	
RD# delay time	t_{RSD}	0.5	12.5	ns	
Read data setup time	t_{RDS}	12.5	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	0.5	12.5	ns	
Write data delay time	t_{WDD}	0.5	12.5	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	12.5	—	ns	
WAIT# hold time	t_{WTH}	0	—	ns	
BREQ# setup time	t_{BRS}	12.5	—	ns	
BREQ# hold time	t_{BRH}	0	—	ns	
BACK# delay time	t_{BAC}	—	12.5	ns	
Bus release time	t_{BRL}	—	12.5	ns	
Bus acquisition time	t_{BAQ}	—	12.5	ns	

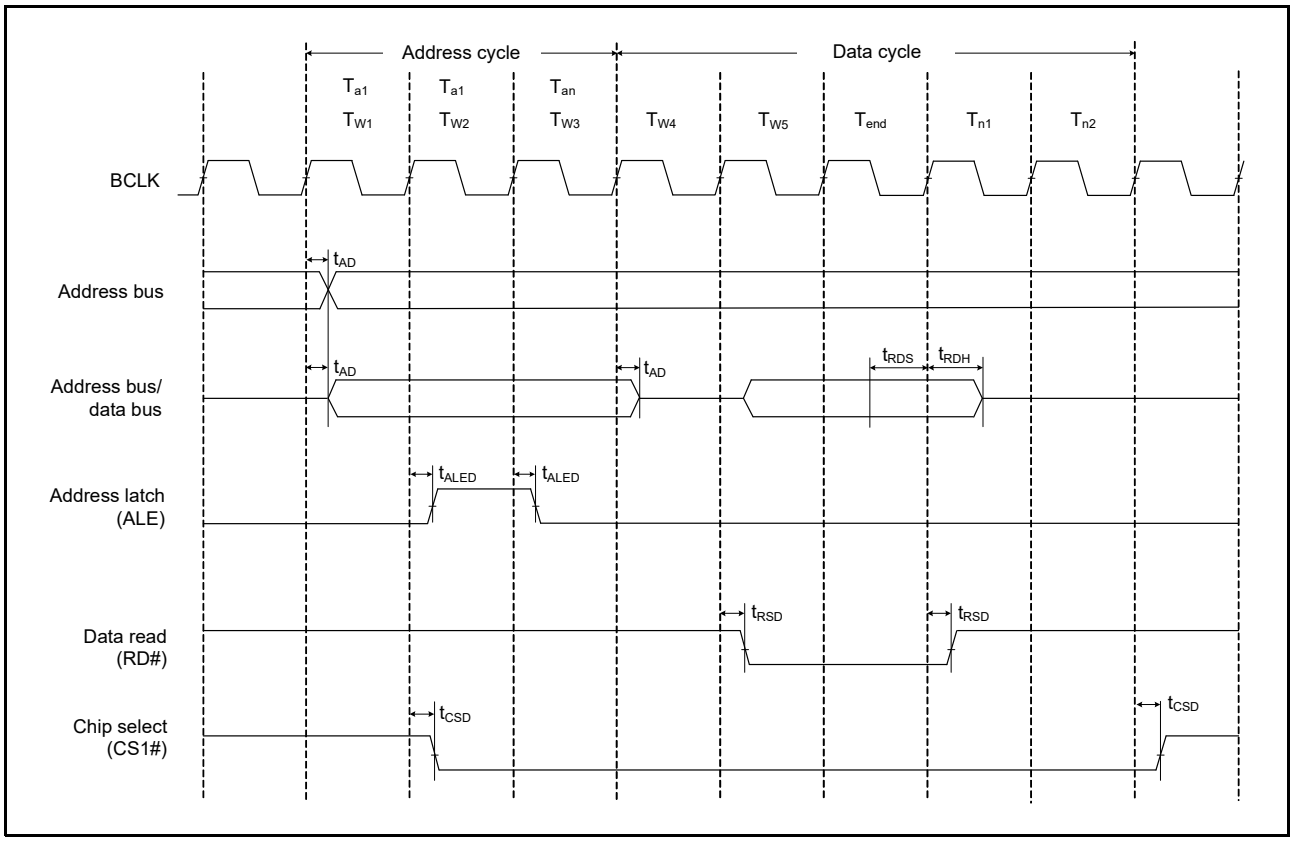


Figure 2.30 Address/Data Multiplexed Bus Read Access Timing

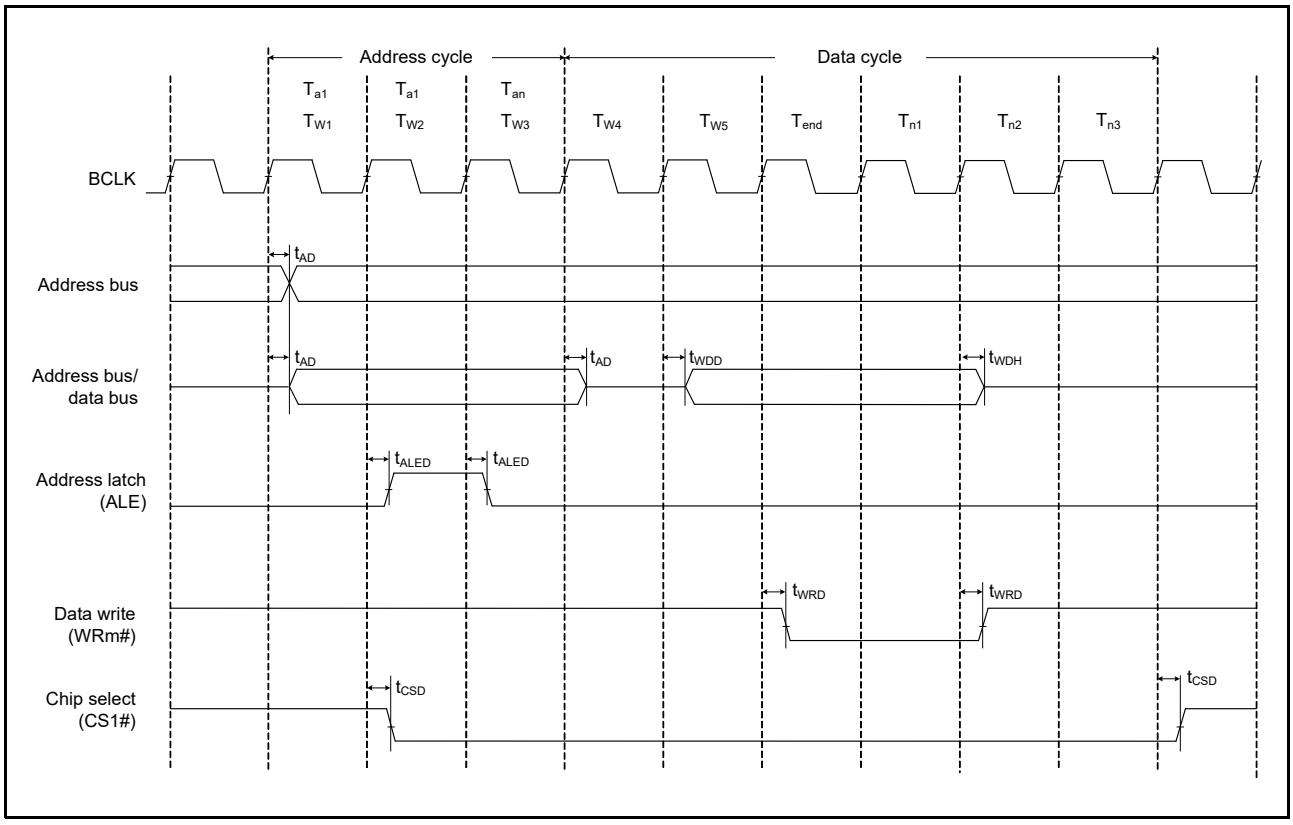


Figure 2.31 Address/Data Multiplexed Bus Write Access Timing

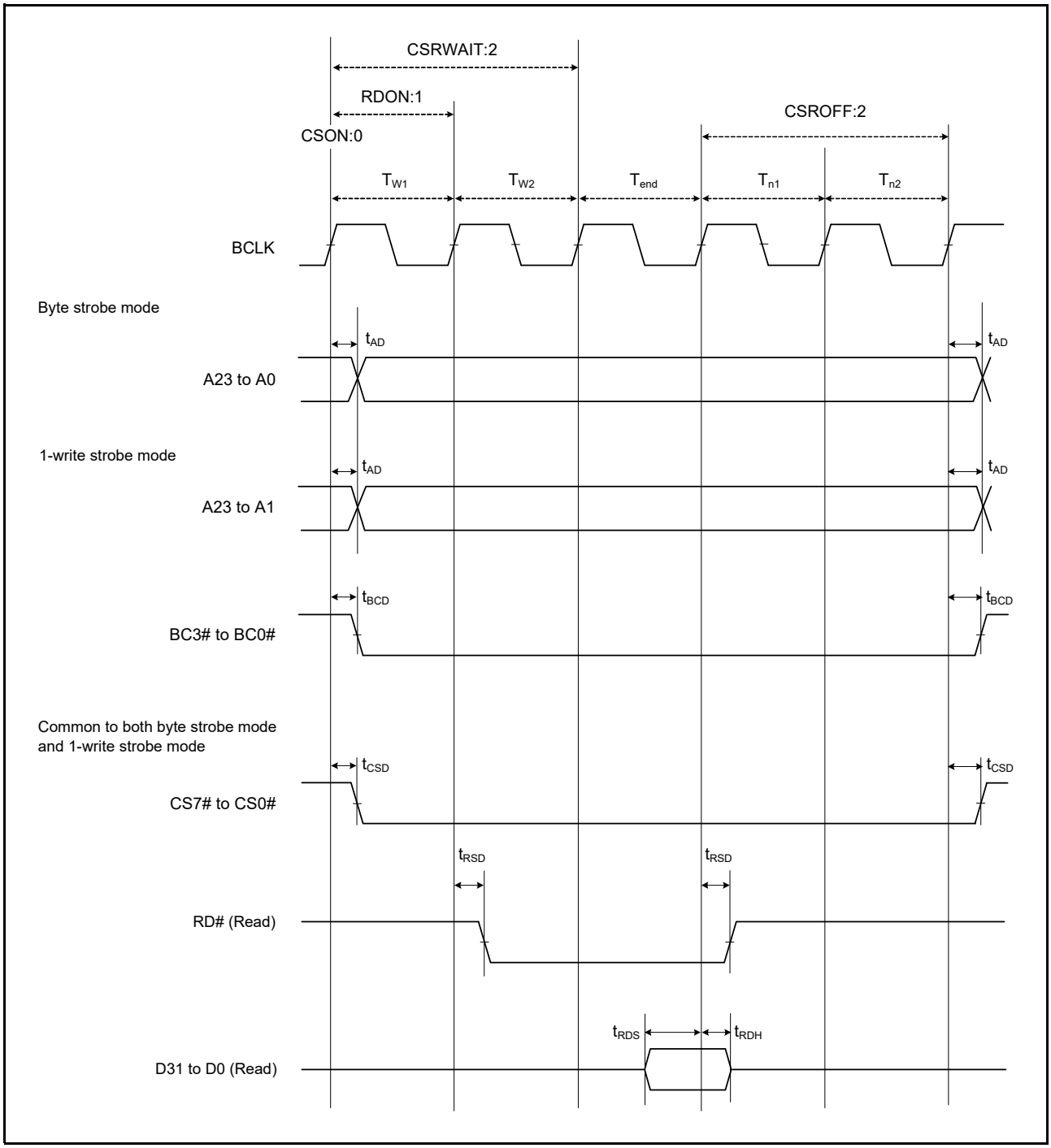
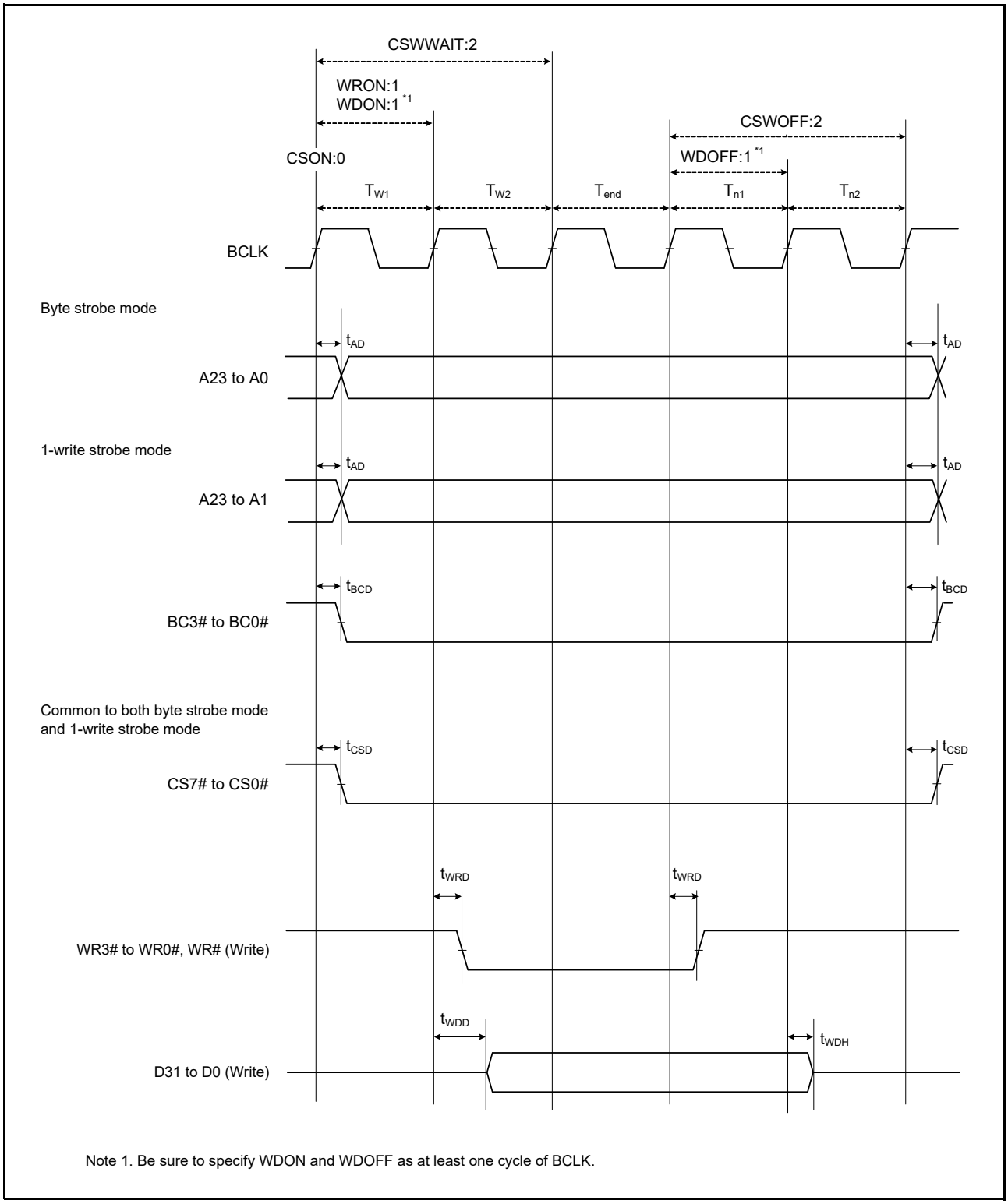


Figure 2.32 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 2.33 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

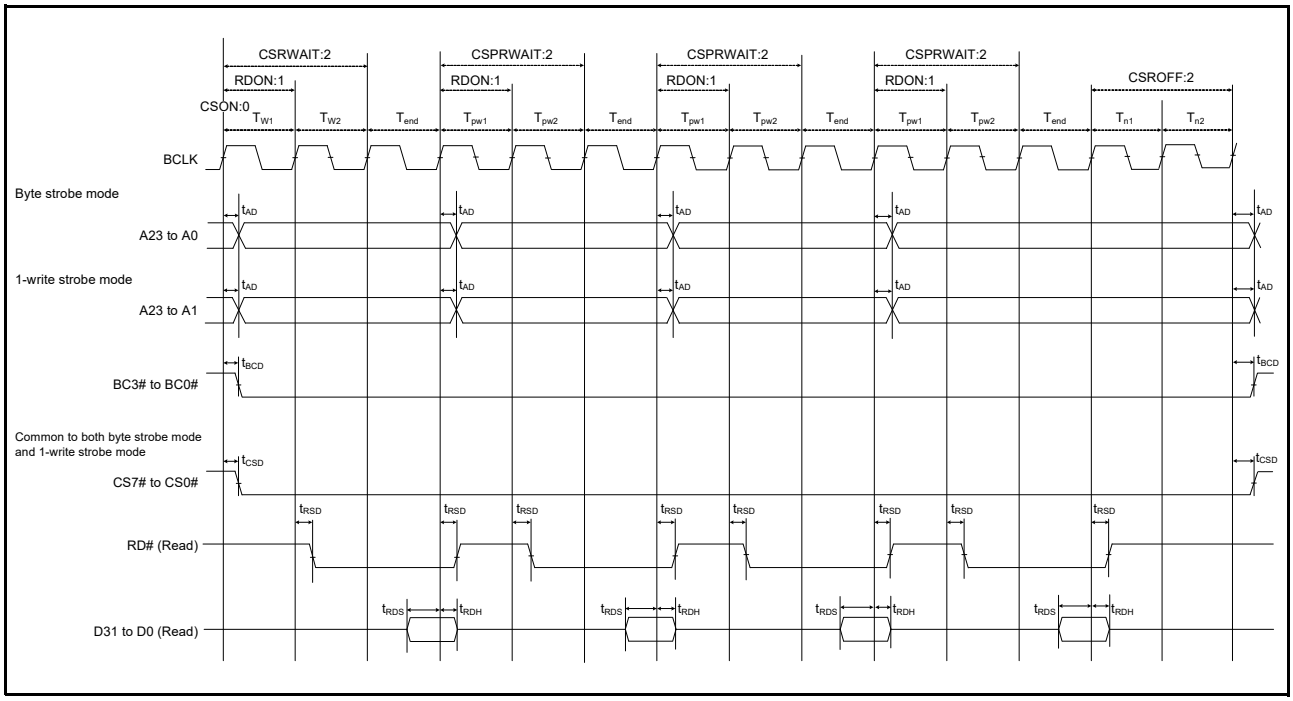


Figure 2.34 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

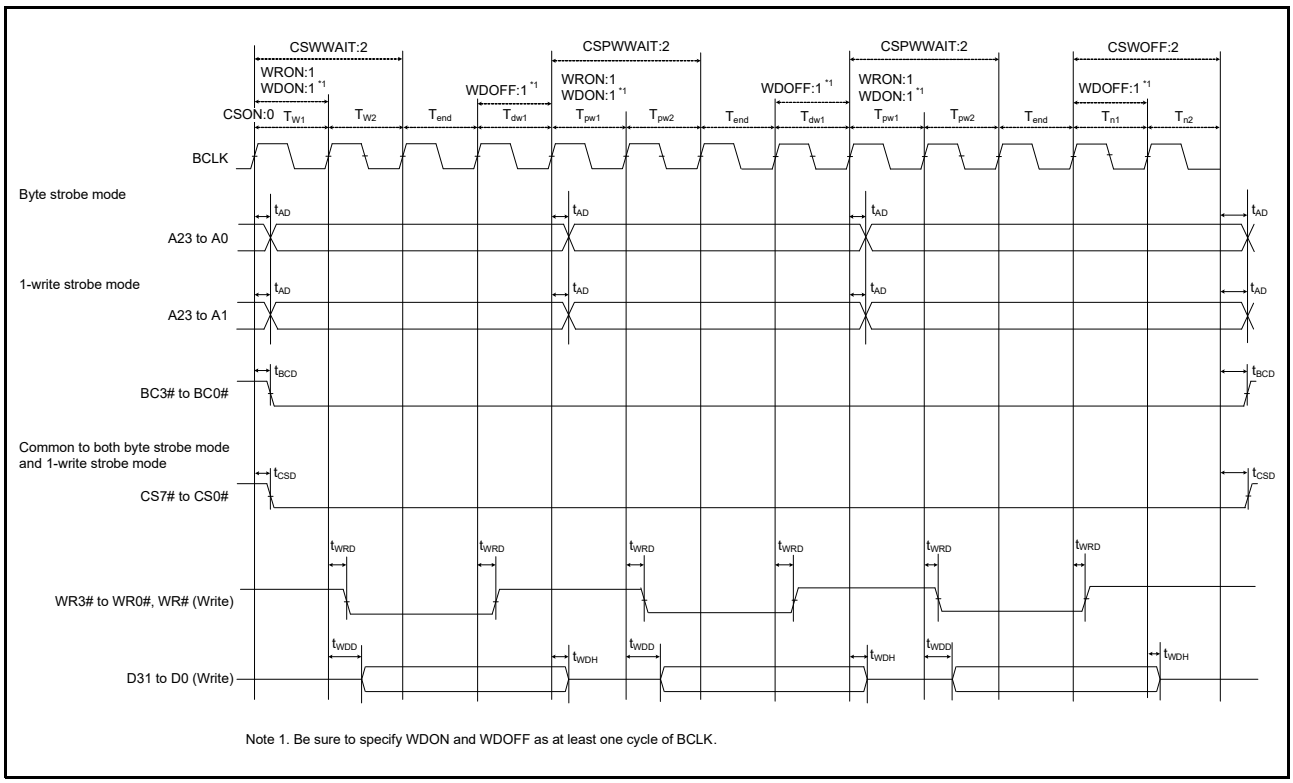


Figure 2.35 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

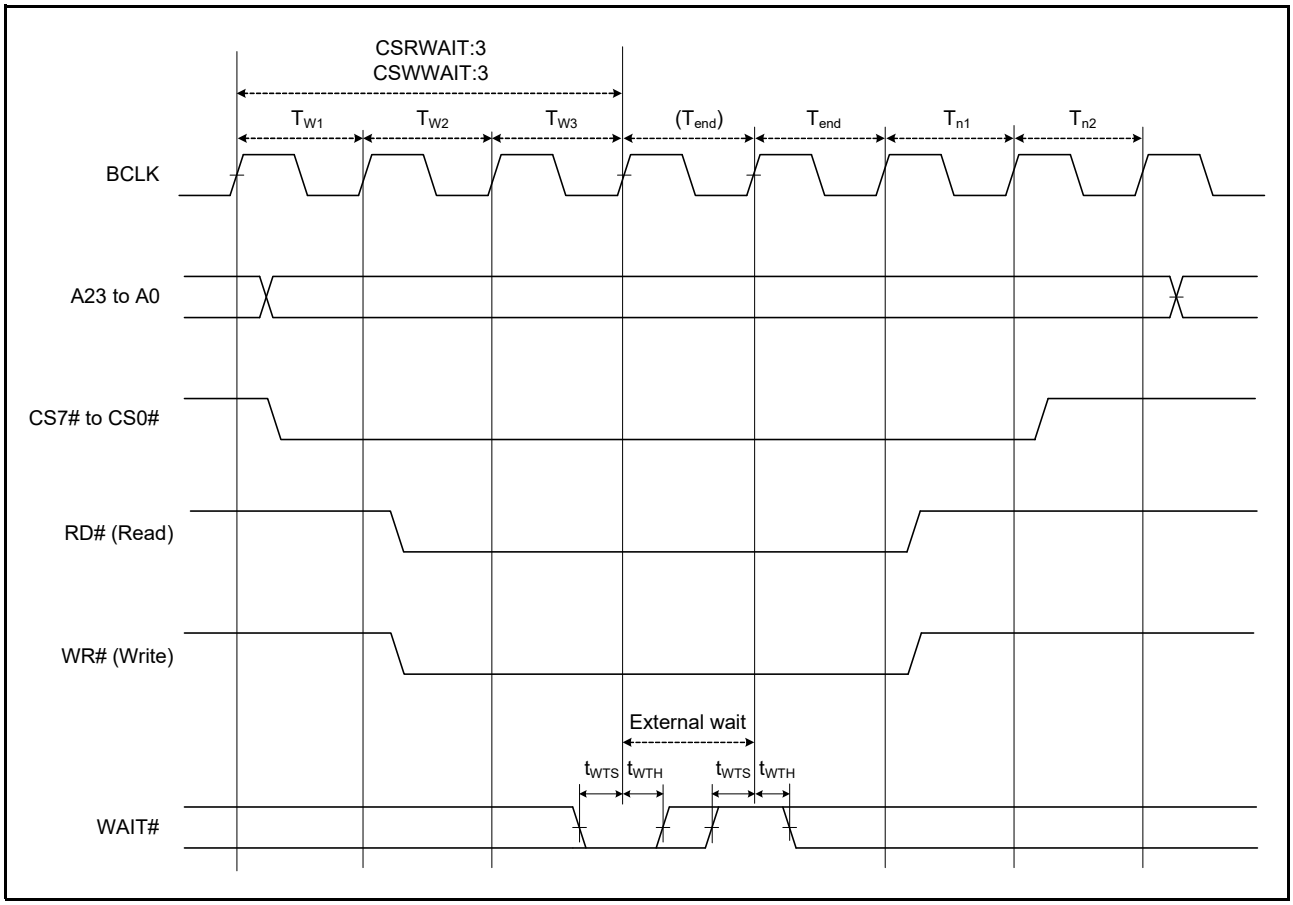


Figure 2.36 External Bus Timing/External Wait Control

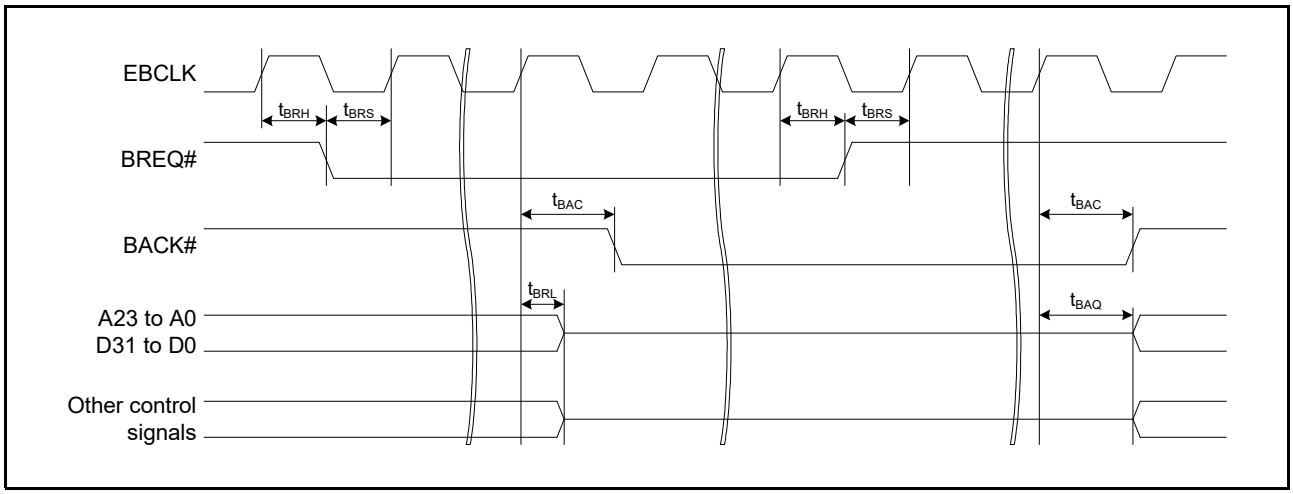


Figure 2.37 External Bus Timing/BREQ, BACK

Table 2.73 Bus Timing (3)

Conditions: With the SDRAM area controller in use
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the SDCLK pin are set for DRV7.
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to pins other than SDCLK pin are set for DRV3.
SDCLK = 133 MHz,
VCC = VCC2 = 3.0 to 3.63 V, C = 15 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time 2 (SDRAM)	t_{AD2}	0.8	6	ns	Figure 2.38 to Figure 2.45
CS# delay time 2 (SDRAM)	t_{CSD2}	0.8	6	ns	
DQM delay time (SDRAM)	t_{DQMD}	0.8	6	ns	
CKE delay time (SDRAM)	t_{CKED}	0.8	6	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	2.1	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	6	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	0.8	—	ns	
WE# delay time (SDRAM)	t_{WED}	0.8	6	ns	
RAS# delay time (SDRAM)	t_{RASD}	0.8	6	ns	
CAS# delay time (SDRAM)	t_{CASD}	0.8	6	ns	
BREQ# setup time 2 (SDRAM)	t_{BRS2}	12.5	—	ns	
BREQ# hold time 2 (SDRAM)	t_{BRH2}	0.8	—	ns	
BACK# delay time 2 (SDRAM)	t_{BAC2}	0.8	12.5	ns	
Bus release time 2 (SDRAM)	t_{BRL2}	0.8	12.5	ns	
Bus acquisition time 2 (SDRAM)	t_{BAQ2}	0	12.5	ns	

Note: This table only applies when pins with the suffix -A, indicating the group name, as part of the pin name are in use.
Note: The above characteristics are only guaranteed for products with part numbers of the form R5K574Mxx4yy (yy = BG, BD, AE).

Table 2.74 Bus Timing (4)

Conditions: With the SDRAM area controller in use
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the SDCLK pin are set for DRV7.
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to pins other than SDCLK pin are set for DRV3.
SDCLK = 100 MHz,
VCC = VCC2 = 3.0 to 3.63 V, C = 15 pF

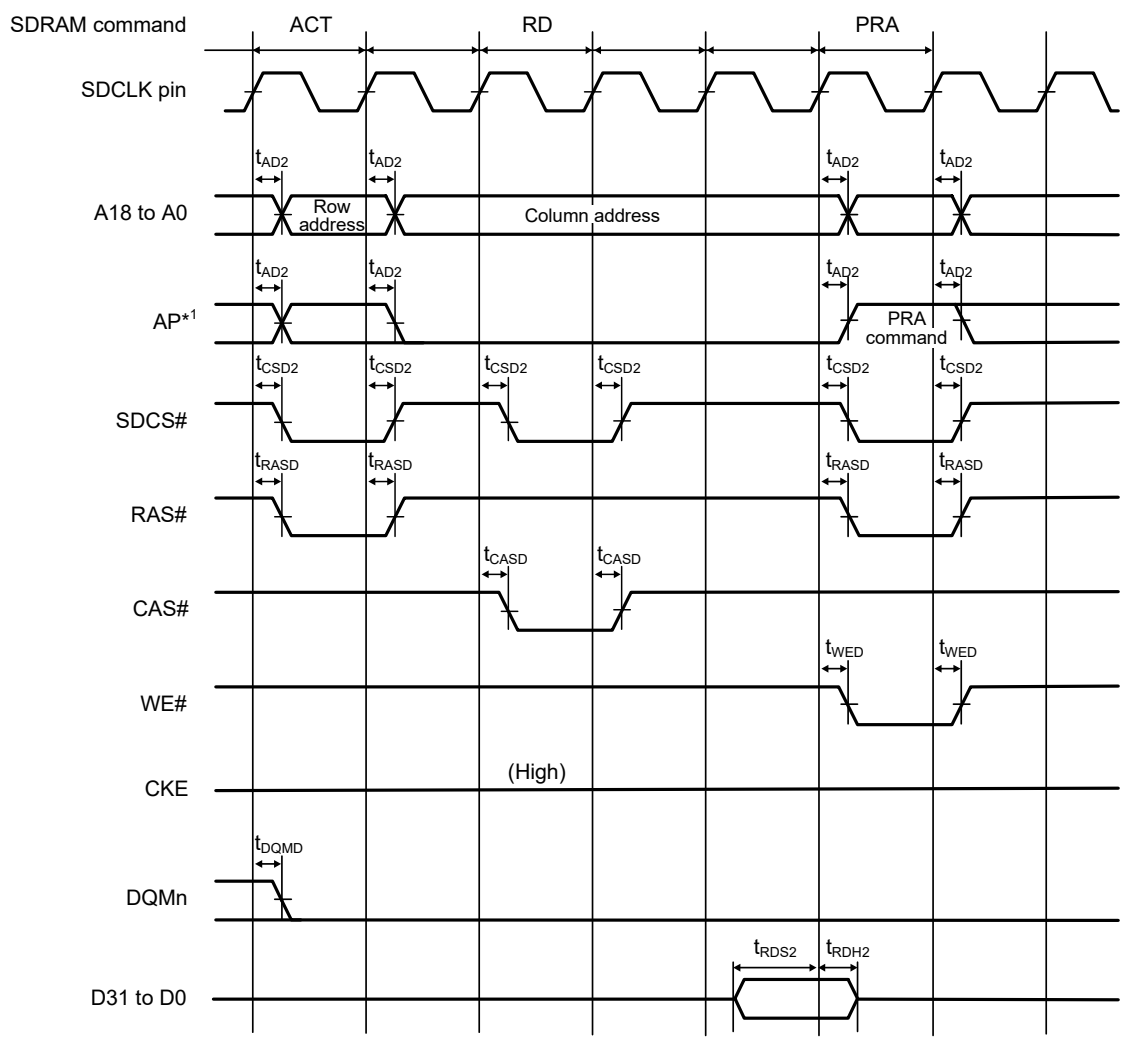
Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time 2 (SDRAM)	t_{AD2}	0.8	8.5	ns	Figure 2.38 to Figure 2.45
CS# delay time 2 (SDRAM)	t_{CSD2}	0.8	8.5	ns	
DQM delay time (SDRAM)	t_{DQMD}	0.8	8.5	ns	
CKE delay time (SDRAM)	t_{CKED}	0.8	8.5	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	4	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	8.5	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	0.8	—	ns	
WE# delay time (SDRAM)	t_{WED}	0.8	8.5	ns	
RAS# delay time (SDRAM)	t_{RASD}	0.8	8.5	ns	
CAS# delay time (SDRAM)	t_{CASD}	0.8	8.5	ns	
BREQ# setup time 2 (SDRAM)	t_{BRS2}	12.5	—	ns	
BREQ# hold time 2 (SDRAM)	t_{BRH2}	0.8	—	ns	
BACK# delay time 2 (SDRAM)	t_{BAC2}	0.8	12.5	ns	
Bus release time 2 (SDRAM)	t_{BRL2}	0.8	12.5	ns	
Bus acquisition time 2 (SDRAM)	t_{BAQ2}	0	12.5	ns	

Note: The above characteristics are only guaranteed for products with part numbers of the form R5K574Mxx4yy (yy = BG, BD, AE).

Table 2.75 Bus Timing (5)

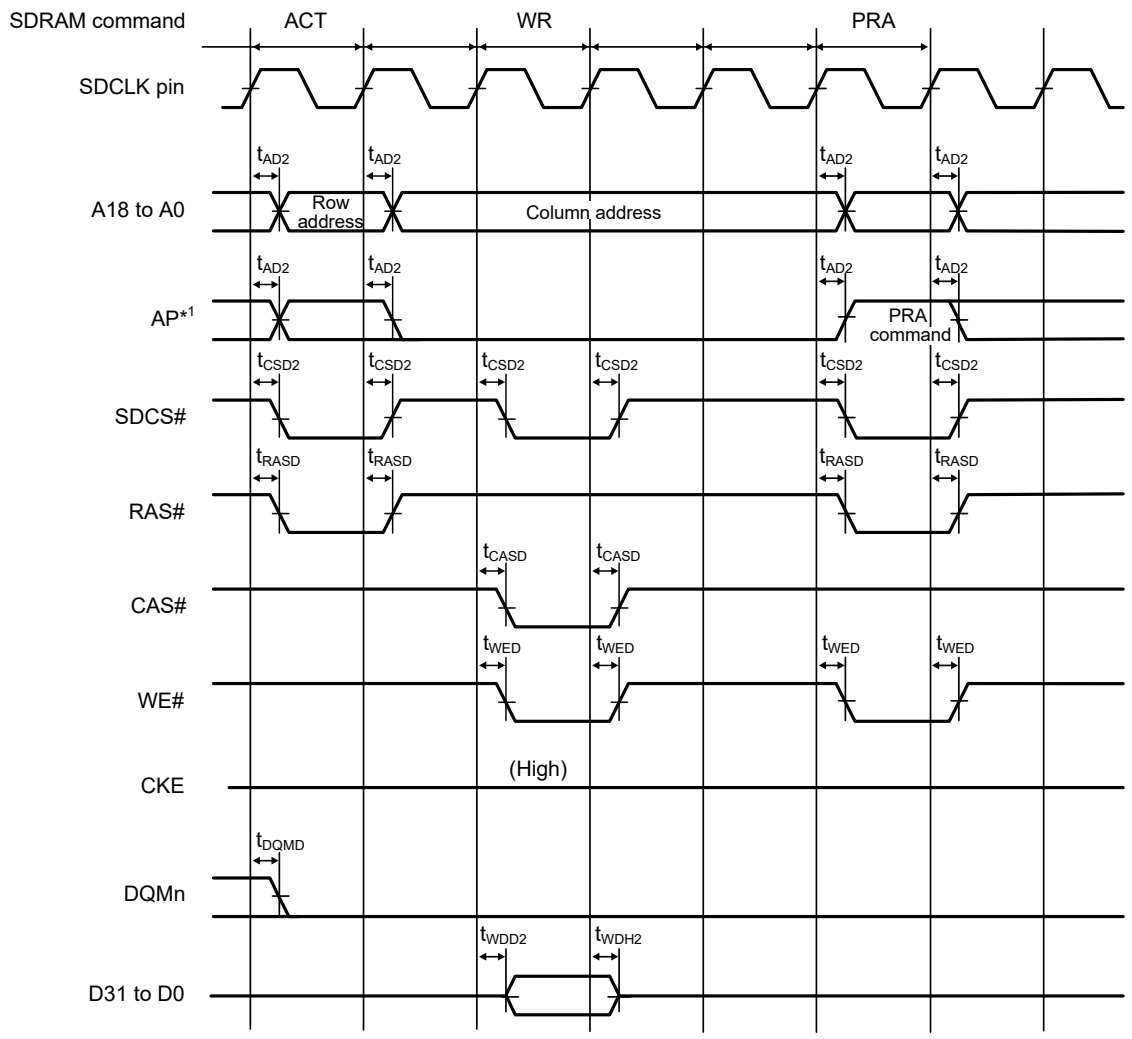
Conditions: With the SDRAM area controller in use
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the SDCLK pin are set for DRV7.
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to pins other than SDCLK pin are set for DRV3.
SDCLK = 60 MHz,
VCC = VCC2 = 2.70 to 3.63 V, C = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time 2 (SDRAM)	t_{AD2}	0.8	12.5	ns	Figure 2.38 to Figure 2.45
CS# delay time 2 (SDRAM)	t_{CSD2}	0.8	12.5	ns	
DQM delay time (SDRAM)	t_{DQMD}	0.8	12.5	ns	
CKE delay time (SDRAM)	t_{CKED}	0.8	12.5	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	10	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	12.5	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	0.8	—	ns	
WE# delay time (SDRAM)	t_{WED}	0.8	12.5	ns	
RAS# delay time (SDRAM)	t_{RASD}	0.8	12.5	ns	
CAS# delay time (SDRAM)	t_{CASD}	0.8	12.5	ns	
BREQ# setup time 2 (SDRAM)	t_{BRS2}	12.5	—	ns	
BREQ# hold time 2 (SDRAM)	t_{BRH2}	0.8	—	ns	
BACK# delay time 2 (SDRAM)	t_{BAC2}	0.8	12.5	ns	
Bus release time 2 (SDRAM)	t_{BRL2}	0.8	12.5	ns	
Bus acquisition time 2 (SDRAM)	t_{BAQ2}	0	12.5	ns	



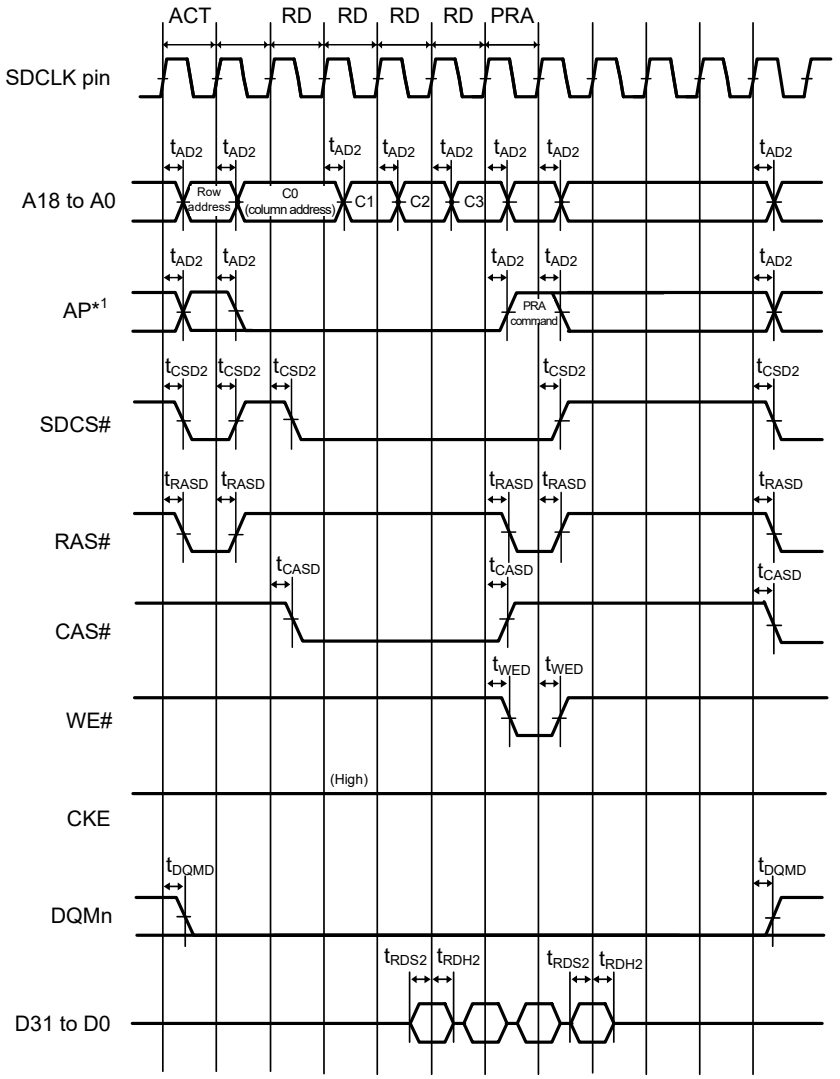
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.38 SDRAM Space Single Read Bus Timing



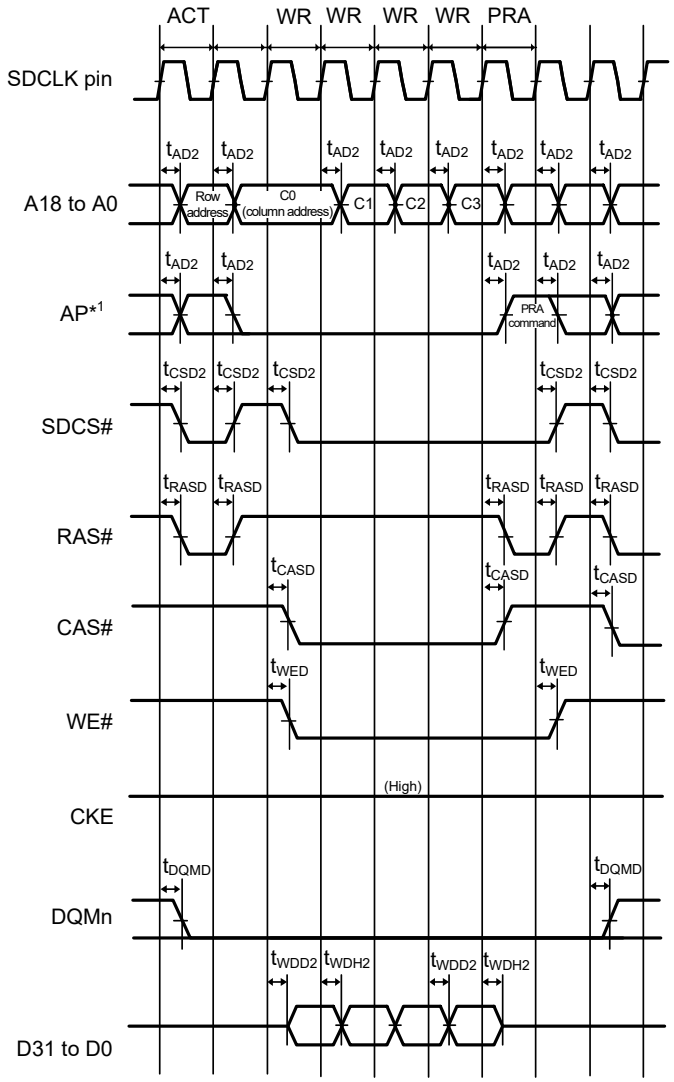
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.39 SDRAM Space Single Write Bus Timing



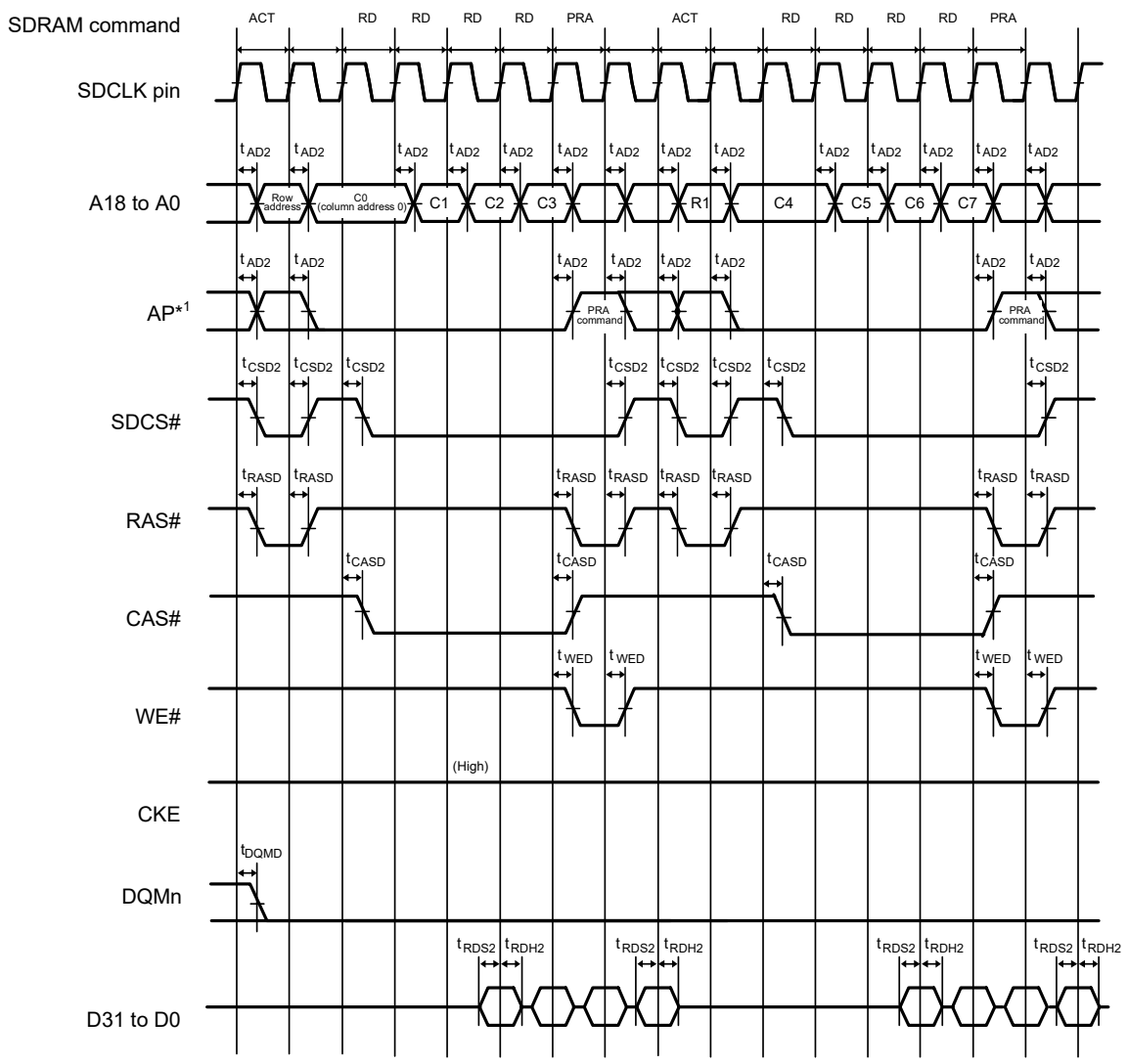
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.40 SDRAM Space Multiple Read Bus Timing



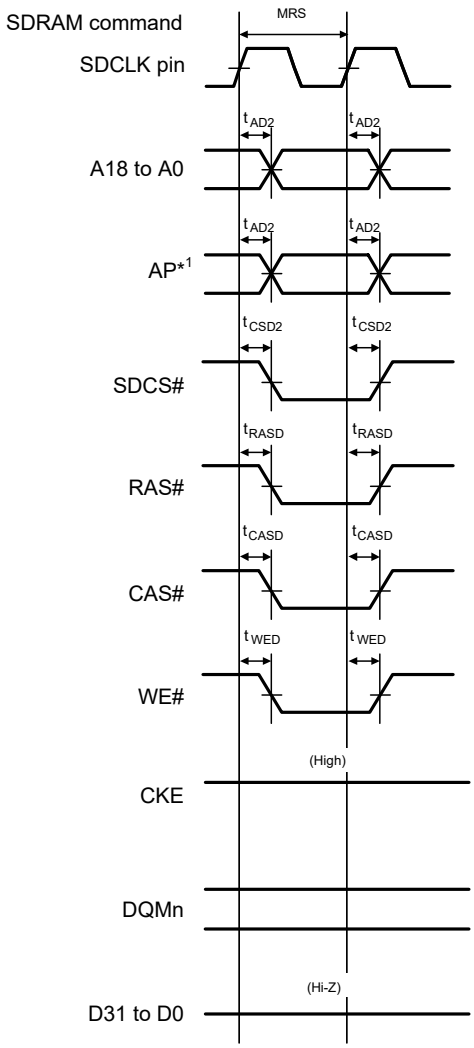
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.41 SDRAM Space Multiple Write Bus Timing



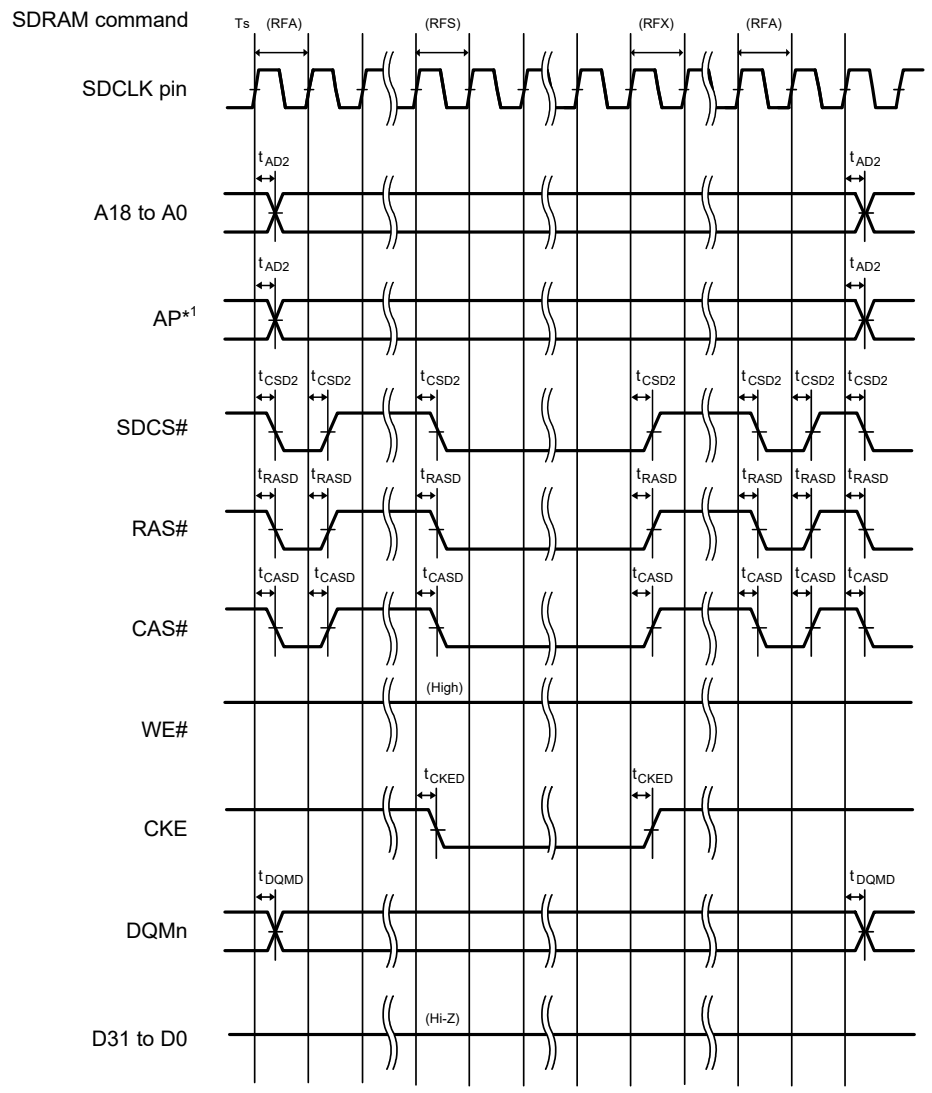
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.42 SDRAM Space Multiple Read Line Stride Bus Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.43 SDRAM Space Mode Register Set Bus Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.44 SDRAM Space Self-Refresh Bus Timing

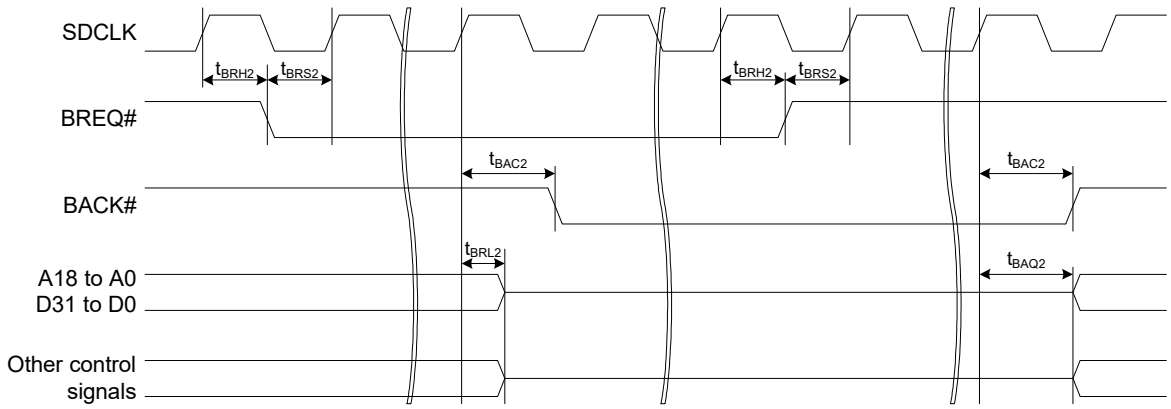


Figure 2.45 External Bus Timing/BREQ, BACK

2.5.7 Timing of On-Chip Peripheral Modules

2.5.7.1 I/O Port

Table 2.76 I/O Port Timing

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	7.5	—	t_{Icyc}	Figure 2.46

Note 1. t_{Icyc}: ICLK cycle

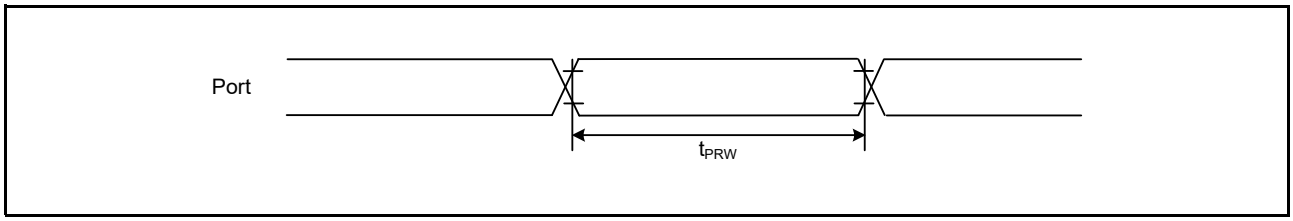


Figure 2.46 I/O Port Input Timing

2.5.7.2 TMR

Table 2.77 TMR Timing

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 2.47
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

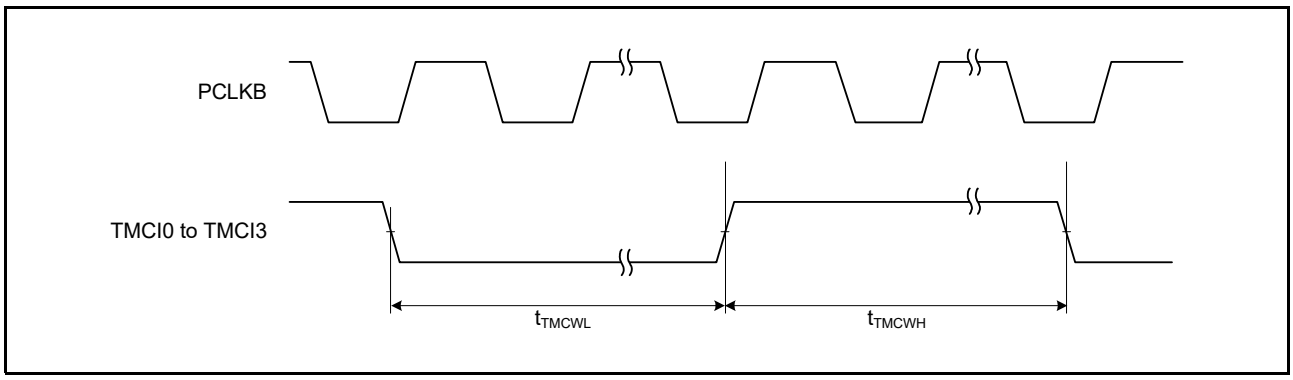


Figure 2.47 TMR Clock Input Timing

2.5.7.3 CMTW

Table 2.78 CMTW Timing

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWTICW}$	1.5	—	t_{PBcyc}	Figure 2.48
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

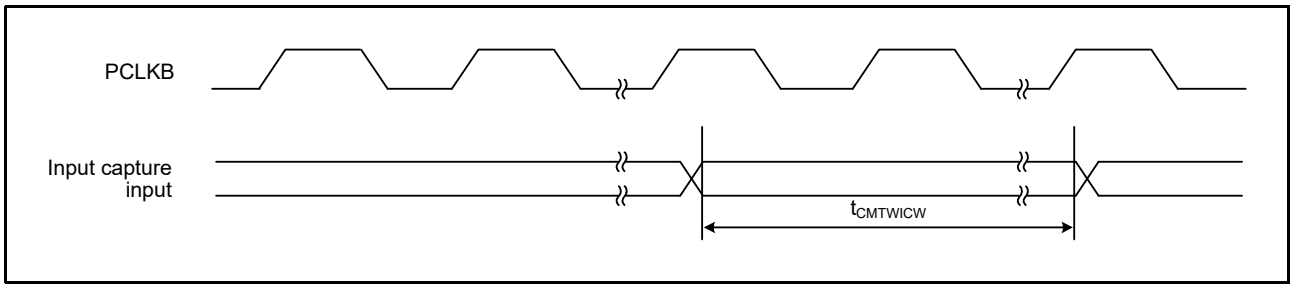


Figure 2.48 CMTW Input Capture Input Timing

2.5.7.4 POEG

Table 2.79 POEG Timing

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
POEG	GTETRGn input pulse width (n = A to D)		t_{POEGW}	1.5	—	t_{PAcyc}	
	POEGn input pulse width (n = A to D)		t_{POEGW2}	1.5	—	t_{PAcyc}	
	Output disable time	Input level detection of the GTETRGn pin (via flag)	t_{POEGDI}	—	3 PCLKA + 0.34	μs	When the digital noise filter is not in use (POEGGn.NFEN = 0 (n = A to D))
		Input level detection of the POEGn pin (via flag)	$t_{POEGDI2}$	—	3 PCLKA + 0.34		When the digital noise filter is not in use (POEGG2n.NFEN = 0 (n = A to D))
		Change of the POEGn signal level	$t_{POEGDI3}$	—	4 PCLKA + 0.34		Detection of a rising or falling edge (POEGG2n.PIDM[1:0] = 01b or 10b)
		Detection of the output stopping signal from GPTW (deadtime error, simultaneous high output, or simultaneous low output)	t_{POEGDE}	—	0.5		
		Detection of the output stopping signal from DSMIF	t_{POEGDD}	—	0.5		
		Register setting	t_{POEGDS}	—	1 PCLKA + 0.3		Time for access to the register is not included.
		Detection of the main clock oscillation stop	$t_{POEGDOS}$	—	2		

Note 1. t_{PAcyc}: PCLKA cycle

2.5.7.5 GPTW

Table 2.80 GPTW Timing

Item			Symbol	Min.	Max.	Unit*1, *2	Test Conditions
GPTW	Input capture input pulse width (cycle)	Single-edge setting	t_{GTICW}	1.5	—	t_{GTcyc}	
		Both-edge setting		2.5	—		
	External trigger input pulse width (cycle)	Single-edge setting	t_{GTEW}	1.5	—	t_{PAcyc}	
		Both-edge setting		2.5	—		
	Timer clock pulse width		t_{GTCKWH}, t_{GTCKWL}	1.5	—	t_{PAcyc}	

Note 1. t_{GTcyc}: GTCLK cycle
Note 2. t_{PAcyc}: PCLKA cycle

2.5.7.6 RSCI

Table 2.81 RSCI Timing (Asynchronous Mode)

Condition: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV3.

Item		VCC/VCC2	Symbol	Min.	Max.	Unit*1	Test Conditions
RSCI (Asynchronous)	Input clock cycle		t_{Scyc}	4	—	t_{PAcyc}	Figure 2.49
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	0.1	ns	
	Input clock fall time		t_{SCKf}	—	0.1	ns	
	Output clock cycle		t_{Scyc}	6	—	t_{PAcyc}	
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time	2.70 V or higher	t_{SCKr}	—	3.3	ns	
		1.62 V or higher		—	6.6		
	Output clock fall time	2.70 V or higher	t_{SCKf}	—	3.3	ns	
		1.62 V or higher		—	6.6		

Note 1. t_{PAcyc}: PCLKA cycle

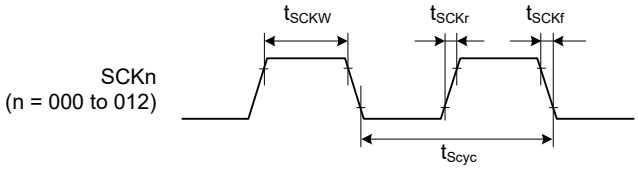


Figure 2.49 SCK Clock Input Timing

Table 2.82 RSCI Timing (Clock Synchronous Mode)

Condition: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV3.

Item			VCC/VCC2	Symbol	Min.	Max.	Unit*1	Test Conditions
RSCI (clock synchronous)	Output clock cycle	Master	2.70 V or higher	t_{Scyc}	2 (TCLK ≤ 120 MHz)	—	t_{Tcyc}	Figure 2.50
					4 (TCLK > 120 MHz)	—		
			1.62 V or higher		2 (TCLK ≤ 60 MHz)	—		
					4 (TCLK ≤ 120 MHz)	—		
					8 (TCLK > 120 MHz)	—		
	Input clock cycle	Slave	2.70 V or higher		2	—	t_{Tcyc}	
			1.62 V or higher		2 (TCLK ≤ 100 MHz)	—		
					4 (TCLK > 100 MHz)	—		
	Clock high pulse width	Master		t_{SCKWH}	0.4	0.6	t_{Scyc}	
		Slave			0.4	0.6		
	Clock low pulse width	Master		t_{SCKWL}	0.4	0.6	t_{Scyc}	
		Slave			0.4	0.6		
	Clock rise/fall time	Output	2.70 V or higher	t_{SCKr}, t_{SCKf}	—	3.3	ns	
			1.62 V or higher		—	6.6		
		Input	1.62 V or higher		—	1.0	μs	
	Data input setup time	Master (high-speed pins)*2		t_{SU}	2.6	—	ns	
		Master			2.8	—		
		Slave	2.70 V or higher		3.3	—		
			1.62 V or higher		5.3	—		
	Data input hold time	Master	2.70 V or higher	t_H	7.5	—	ns	
			1.62 V or higher		9.5	—		
		Slave	2.70 V or higher		3.0	—		
			1.62 V or higher		5.0	—		
	Data output delay time	Master (high-speed pins)*2		t_{OD}	—	5.0	ns	
		Master			—	5.0		
		Slave (high speed pins)*2	2.70 V or higher		—	15		
			1.62 V or higher		—	23		
		Slave	2.70 V or higher		—	21		
			1.62 V or higher		—	29		
	Data rise/fall time	Output	2.70 V or higher	t_{Dr}, t_{Df}	—	3.3	ns	
			1.62 V or higher		—	6.6		
		Input			—	1.0	μs	

Note 1. t_{Tcyc}: TCLK (PCLKA or SCICLK) cycle
Note 2. The listed value applies when the pins with -A appended to their names are in use.

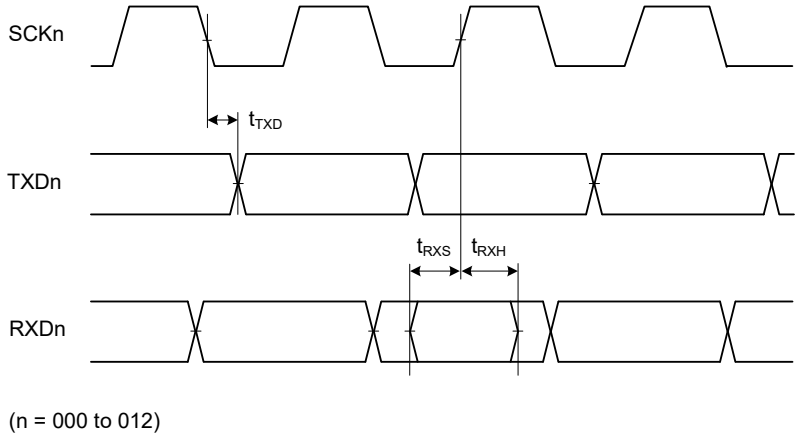


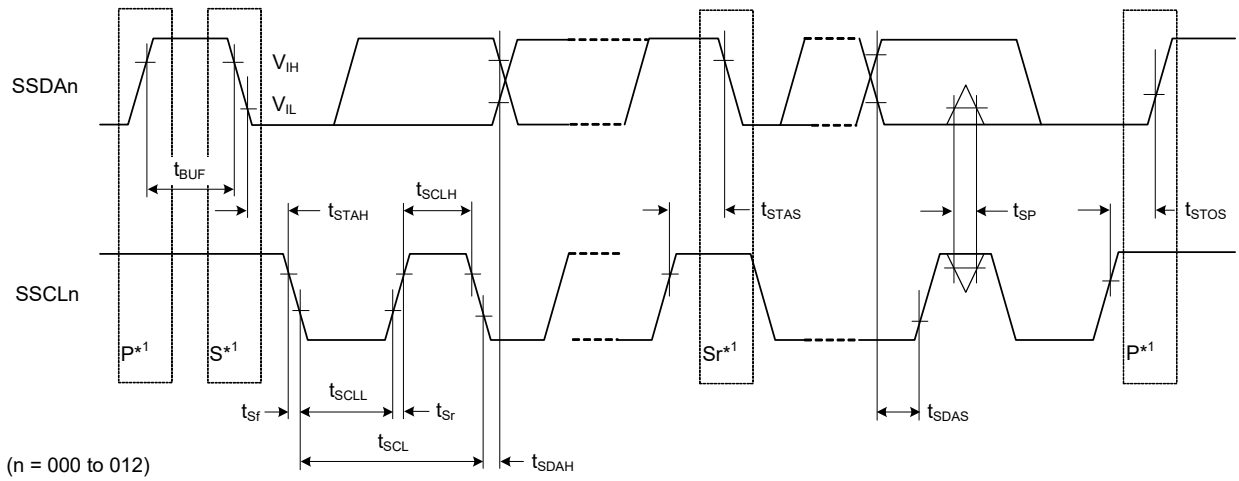
Figure 2.50 RSCI Input/Output Timing: Clock Synchronous Mode

Table 2.83 Simple IIC Timing

Condition: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV3.

Item		Symbol	Min.	Max.*1	Unit	Test Conditions
Simple IIC (Standard-mode)	SSCL and SSDA input rise time	t_{Sr}	—	1000	ns	Figure 2.51
	SSCL and SSDA input fall time	t_{Sf}	—	300		
	SSCL and SSDA input spike pulse removal time	t_{SP}	0	4 × t_{PAcyc}		
	Data input setup time	t_{SDAS}	250	—		
	Data input hold time	t_{SDAH}	0	—		
	SSCL and SSDA capacitive load	C_b*2	—	400	pF	
Simple IIC (Fast-mode)	SSCL and SSDA input rise time	t_{Sr}	—	300	ns	
	SSCL and SSDA input fall time	t_{Sf}	—	300		
	SSCL and SSDA input spike pulse removal time	t_{SP}	0	4 × t_{PAcyc}		
	Data input setup time	t_{SDAS}	100	—		
	Data input hold time	t_{SDAH}	0	—		
	SSCL and SSDA capacitive load	C_b*2	—	400	pF	

Note 1. t_{PAcyc}: PCLKA cycle
Note 2. Cb is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
V_{IH} = 0.7 × VCC or 0.7 × VCC2,
V_{IL} = 0.3 × VCC or 0.3 × VCC2,
V_{OL} = 0.6 V, I_{OL} = 6 mA

Figure 2.51 Simple IIC Bus Interface Input/Output Timing

Table 2.84 Simple SPI Timing (1/2)

Condition: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV3.

Item			VCC/VCC2	Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	Output clock cycle	Master	2.70 V or higher	t_{Scyc}	2 (TCLK ≤ 120 MHz)	65536	t_{Tcyc}	Figure 2.52
					4 (TCLK > 120 MHz)	65536		
			1.62 V or higher		2 (TCLK ≤ 60 MHz)	65536		
					4 (TCLK ≤ 120 MHz)	65536		
					8 (TCLK > 120 MHz)	65536		
	Input clock cycle	Slave	2.70 V or higher		2	—	t_{Tcyc}	
			1.62 V or higher		2 (TCLK ≤ 100 MHz)	—		
					4 (TCLK > 100 MHz)	—		
	Clock high pulse width			t_{SCKWH}	0.4	0.6	t_{SPcyc}	
	Clock low pulse width			t_{SCKWL}	0.4	0.6		
	Clock rise/fall time	Output	2.70 V or higher	t_{SCKr}, t_{SCKf}	—	3.3	ns	
			1.62 V or higher		—	6.6		
		Input			—	1.0	μs	
	Data input setup time	Master (high-speed pins)*2		t_{SU}	–1.5	—	ns	Figure 2.53, Figure 2.54
		Master			2.0	—		
		Slave	2.70 V or higher		2.5	—		
			1.62 V or higher		4.5	—		
	Data input hold time	Master	2.70 V or higher	t_H	7.5	—	ns	
			1.62 V or higher		9.5	—		
		Slave	2.70 V or higher		2.5	—		
			1.62 V or higher		4.5	—		
	Data output delay time	Master (high-speed pins)*2	2.70 V or higher	t_{OD}	—	3.0	ns	
			1.62 V or higher		—	4.5		
		Master	2.70 V or higher		—	3.5		
			1.62 V or higher		—	5.5		
		Slave (high-speed pins)*2	2.70 V or higher		—	15		
			1.62 V or higher		—	23		
		Slave	2.70 V or higher		—	21		
			1.62 V or higher		—	29		
	Data output hold time	Master (high-speed pins)*2	2.70 V or higher	t_{OH}	–3.0	—	ns	
			1.62 V or higher		–4.5	—		
		Master	2.70 V or higher		–3.5	—		
			1.62 V or higher		–5.5	—		
		Slave			0	—		
	Data rise/fall time	Output	2.70 V or higher	t_{Dr}, t_{Df}	—	3.3	ns	
			1.62 V or higher		—	6.6		
		Input			—	1.0		
	SS input setup time			t_{LEAD}	1.0	—	t_{SPcyc}	Figure 2.55, Figure 2.56
	SS input hold time			t_{LAG}	1.0	—		
	SS data rise/fall time			t_{SSLr}, t_{SSLf}	—	1.0	μs	

Table 2.84 Simple SPI Timing (2/2)

Condition: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV3.

Item		VCC/VCC2	Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	Slave access time	2.70 V or higher	t_{SA}	—	$3 \times t_{Tcyc} + 25$*1	ns	Figure 2.55, Figure 2.56
		1.62 V or higher		—	$3 \times t_{Tcyc} + 32$*1		
	Slave output release time	2.70 V or higher	t_{REL}	—	$3 \times t_{Tcyc} + 25$*1	ns	
		1.62 V or higher		—	$3 \times t_{Tcyc} + 32$*1		

Note 1. t_{Tcyc}: TCLK (PCLKA or SCICLK) cycle
Note 2. The listed value applies when the pins with -A appended to their names are in use.

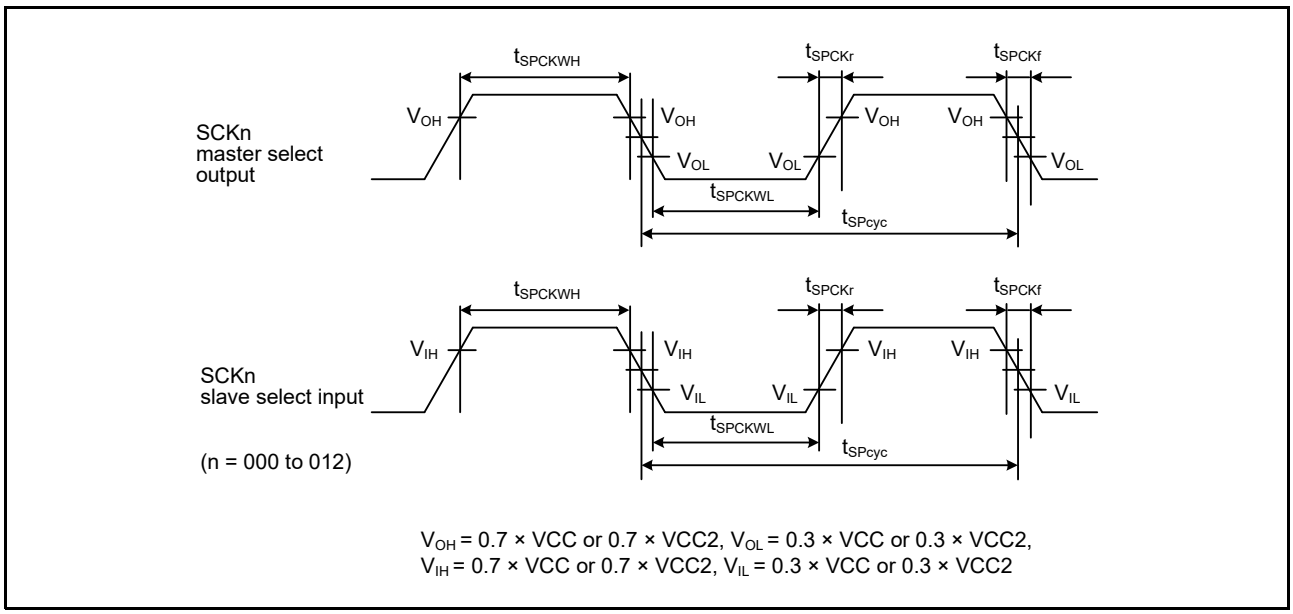


Figure 2.52 Simple SPI Clock Timing

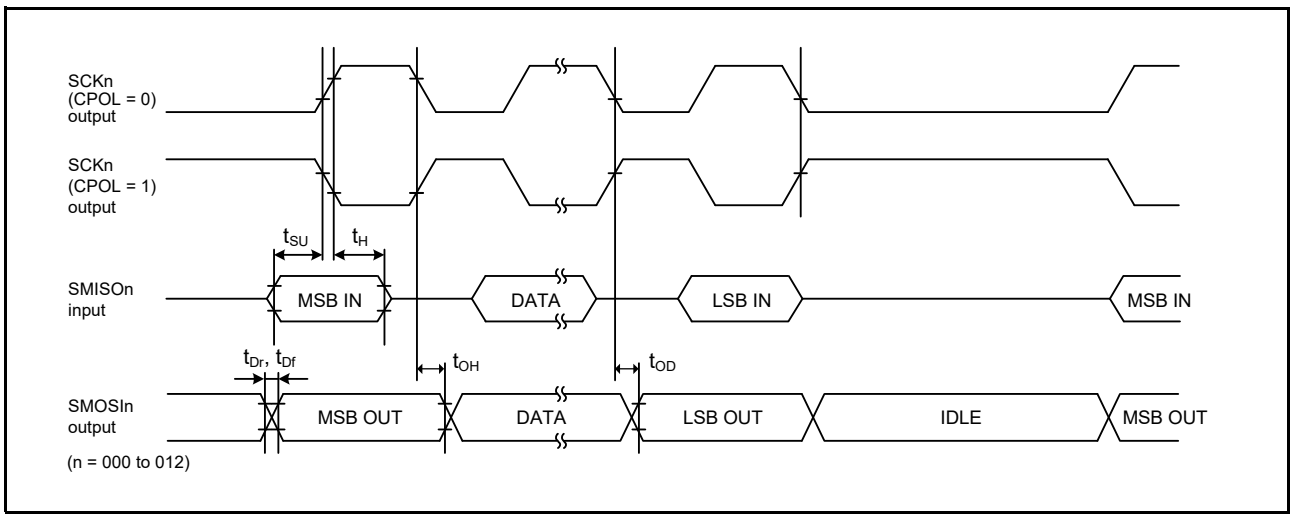


Figure 2.53 Simple SPI Timing (Master, CPHA = 0)

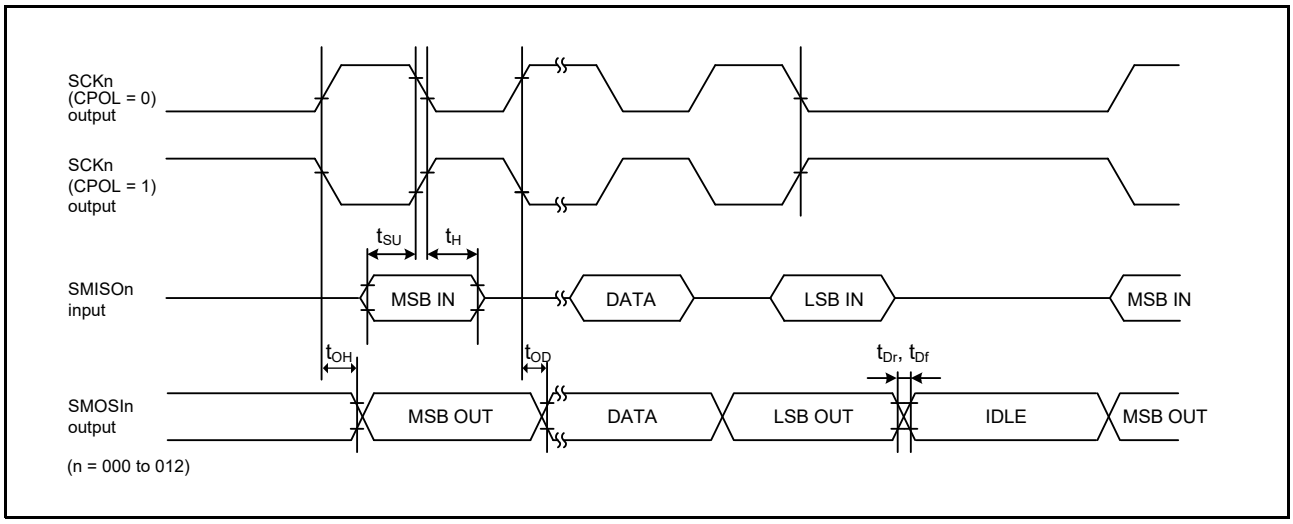


Figure 2.54 Simple SPI Timing (Master, CPHA = 1)

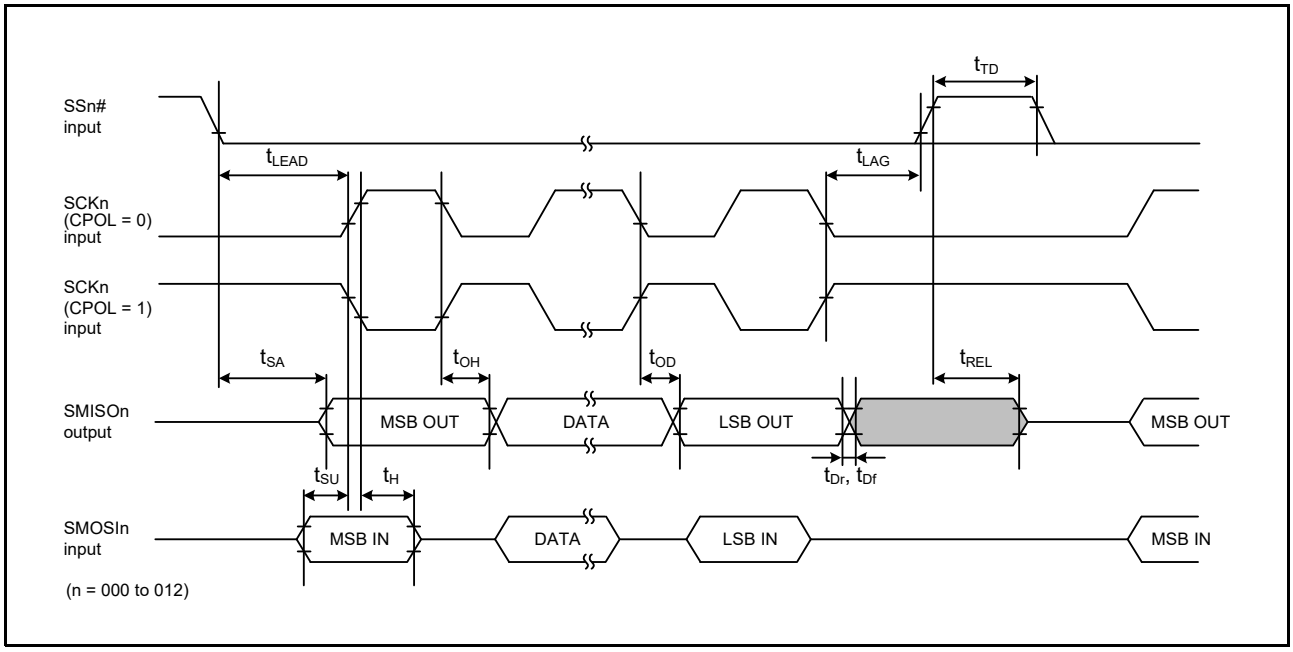


Figure 2.55 Simple SPI Timing (Slave, CPHA = 0)

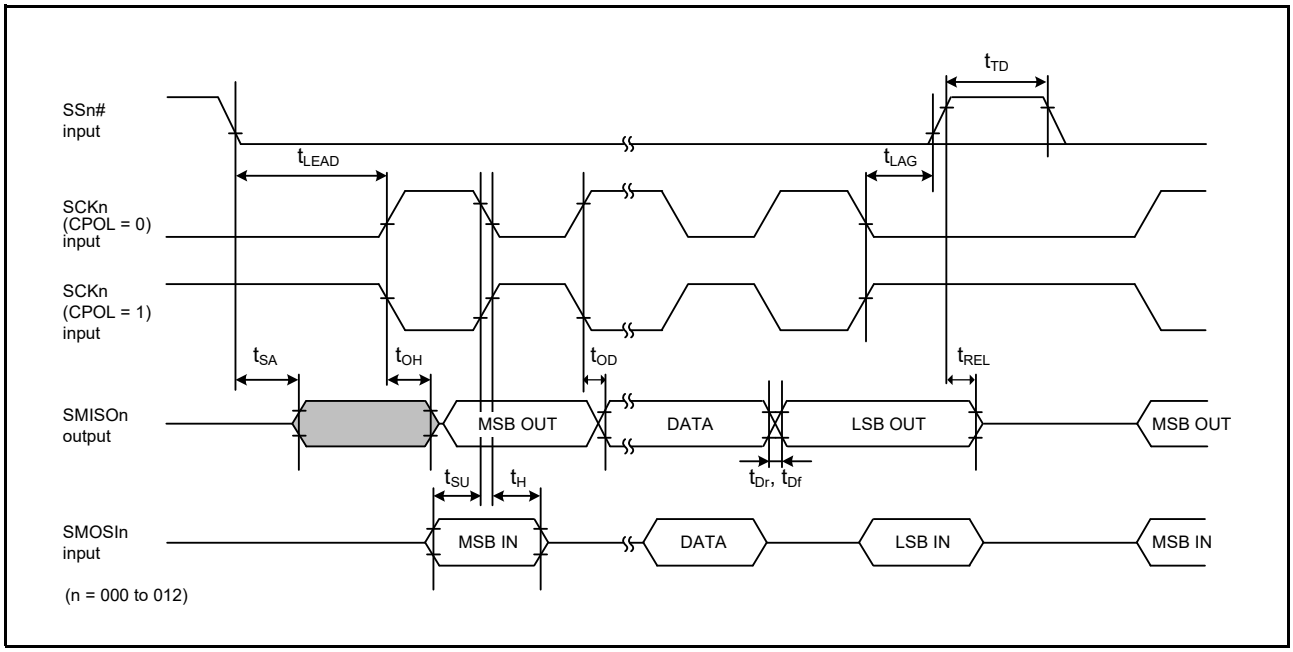


Figure 2.56 Simple SPI Timing (Slave, CPHA = 1)

2.5.7.7 RSPIA

Table 2.85 RSPIA Timing (1/2)

Condition: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV3.

Item			VCC/VCC2	Symbol	Min.*1	Max.*1	Unit*1	Test Conditions
RSPIA	Clock cycle	Master	3.00 V or higher	t_{SPcyc}	2	4096	t_{Tcyc}	Figure 2.57
			2.70 V or higher		2	4096		
			1.62 V or higher		2 (TCLK ≤ 60 MHz)	4096		
					4 (TCLK > 60 MHz)	4096		
		Slave	3.00 V or higher		2	—		
			2.70 V or higher		2	—		
			1.62 V or higher		2 (TCLK ≤ 60 MHz)	—		
					4 (TCLK > 60 MHz)	—		
	Clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			0.4	—	t_{SPcyc}	
	Clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			0.4	—	t_{SPcyc}	
	Clock rise/fall time	Output	3.00 V or higher	t_{SPCKr}, t_{SPCKf}	—	1.66	ns	
			2.70 V or higher		—	3.30		
			1.62 V or higher		—	6.60		
		Input			—	0.1	μs	
	Data input setup time	Master	3.00 V or higher	t_{SU}	–1.5	—	ns	Figure 2.58, Figure 2.59
			2.70 V or higher		0.0	—		
			1.62 V or higher		0.0	—		
		Slave			2.5	—		
	Data input hold time	Master	3.00 V or higher	t_H	7.5	—	ns	
			2.70 V or higher		7.5	—		
			1.62 V or higher		9.5	—		
		Slave	3.00 V or higher		2.5	—		
			2.70 V or higher		2.5	—		
			1.62 V or higher		5.5	—		
	SSL setup time	Master		t_{LEAD}	$1 \times t_{SPcyc} - 10$	$8 \times t_{SPcyc} + 10$	ns	
		Slave			5.0	—	t_{Tcyc}	
	SSL hold time	Master		t_{LAG}	$1 \times t_{SPcyc} - 10$	$8 \times t_{SPcyc} + 10$	ns	
		Slave			5.0	—	t_{Tcyc}	
	TI SSP SS input setup time	Slave		t_{TISS}	2.5	—	ns	Figure 2.63, Figure 2.64
	TI SSP SS input hold time	Slave	3.00 V or higher	t_{TISH}	2.5	—	ns	
			2.70 V or higher		2.5	—		
			1.62 V or higher		5.5	—		
	TI SSP next-access time	Slave		t_{TIND}	$2 \times t_{Tcyc} + S_{LNDL} \times t_{Tcyc}$	—	ns	
	TI SSP master SS output delay time	Master	3.00 V or higher	t_{TISSOD}	—	4.0	ns	Figure 2.60
			2.70 V or higher		—	8.0		
			1.62 V or higher		—	8.0		

Table 2.85 RSPIA Timing (2/2)

Condition: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV3.

Item			VCC/VCC2	Symbol	Min.*1	Max.*1	Unit*1	Test Conditions
RSPIA	Data output delay time	Master	3.00 V or higher	t_{OD1}	—	2.5	ns	Figure 2.58, Figure 2.59
			2.70 V or higher		—	3.0		
			1.62 V or higher		—	6.0		
		Master	3.00 V or higher	t_{OD2}	—	2.5		
			2.70 V or higher		—	2.5		
			1.62 V or higher		—	5.0		
		Slave	3.00 V or higher	t_{OD}	—	11.5*2 13.0*3		
			2.70 V or higher		—	16		
			1.62 V or higher		—	24		
	Data output hold time	Master	3.00 V or higher	t_{OH}	–2.5	—	ns	
			2.70 V or higher		–2.5	—		
			1.62 V or higher		–4.5	—		
		Slave			0.0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Tcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Tcyc}$	ns	
		Slave			t_{Tcyc}	—		
	MOSI and MISO rise/fall time	Output	3.00 V or higher	t_{Dr}, t_{Df}	—	1.66	ns	
			2.70 V or higher		—	3.30		
			1.62 V or higher		—	6.60		
		Input			—	1.00	μs	
	SSL rise/fall time	Output	3.00 V or higher	t_{SSLr}, t_{SSLf}	—	1.66	ns	
			2.70 V or higher		—	3.30		
			1.62 V or higher		—	6.60		
		Input			—	1.00	μs	
	Slave access time	Slave	3.00 V or higher	t_{SA}	—	20.0	ns	Figure 2.61, Figure 2.62
			2.70 V or higher		—	20.0		
			1.62 V or higher		—	25.0		
	Slave output release time	Slave	3.00 V or higher	t_{REL}	—	20.0	ns	
			2.70 V or higher		—	20.0		
			1.62 V or higher		—	25.0		

Note: The pin names include either -A or -B as a suffix to indicate the group to which the given pin belongs. Make sure that pins to be used for a given RSPIA interface are from the same group.

Note 1. t_{Tcyc}: TCLK (PCLKA or SPICLK) cycle

Note 2. When the pin in use is a group-A pin

Note 3. When the pin in use is not a group-A pin

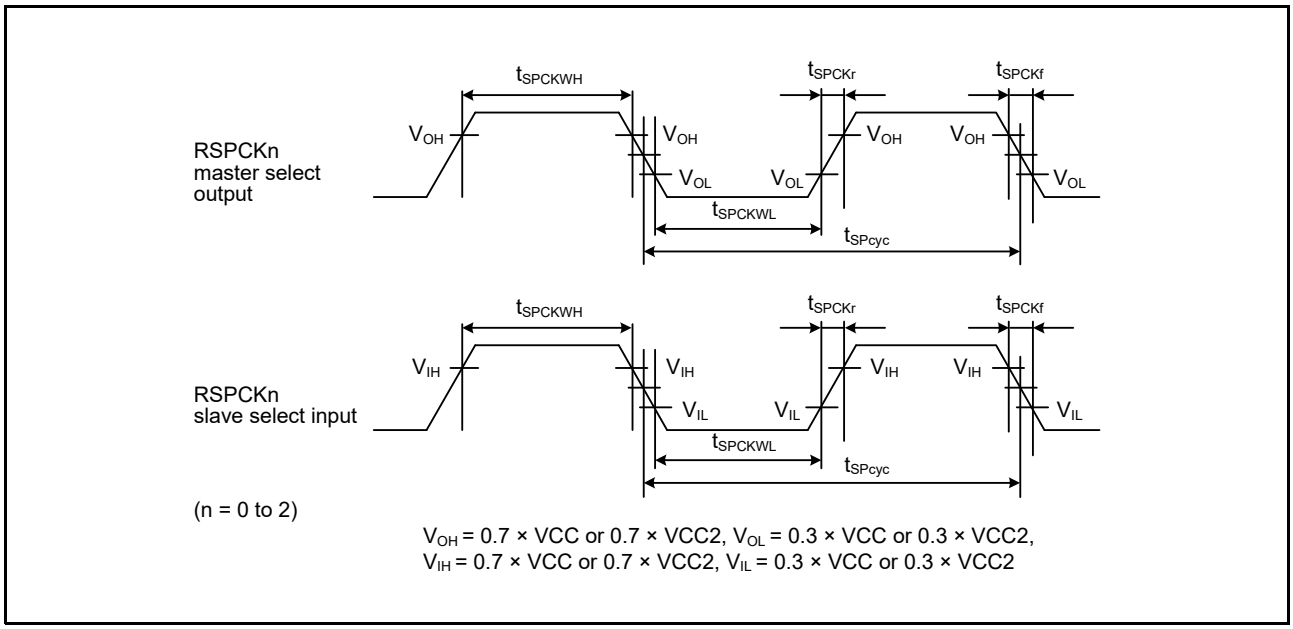


Figure 2.57 RSPIA Clock Timing

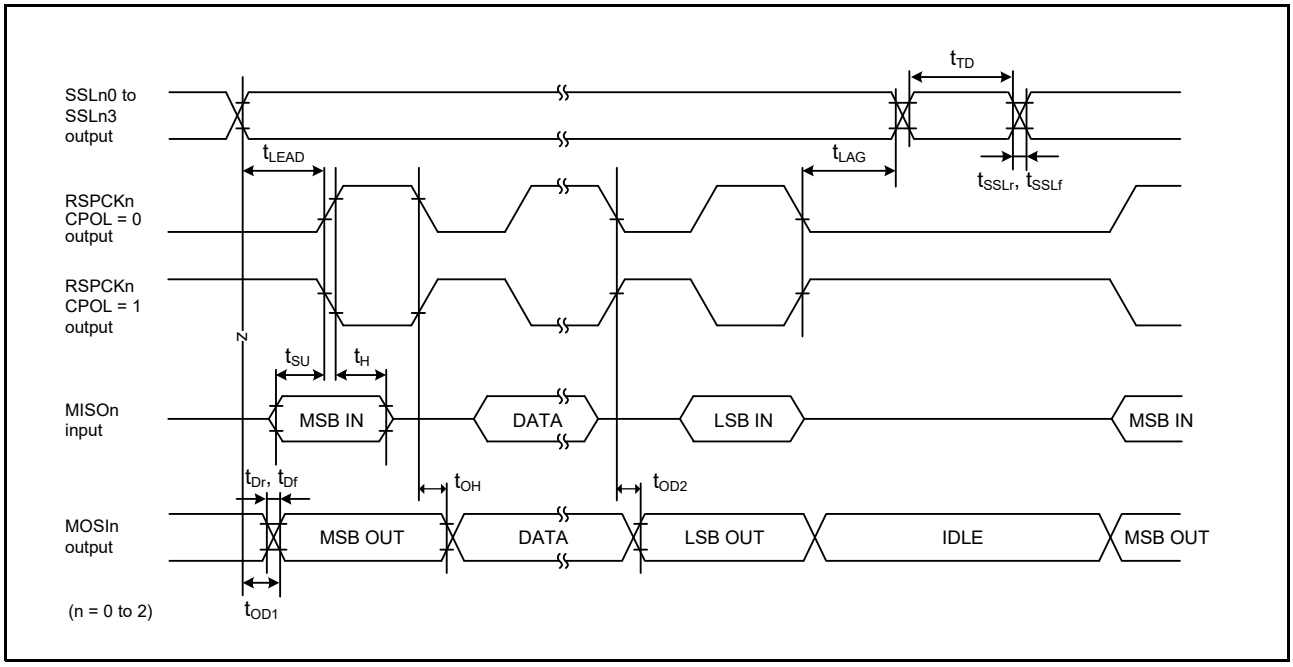


Figure 2.58 RSPIA Timing (Master, Motorola SPI, CPHA = 0)

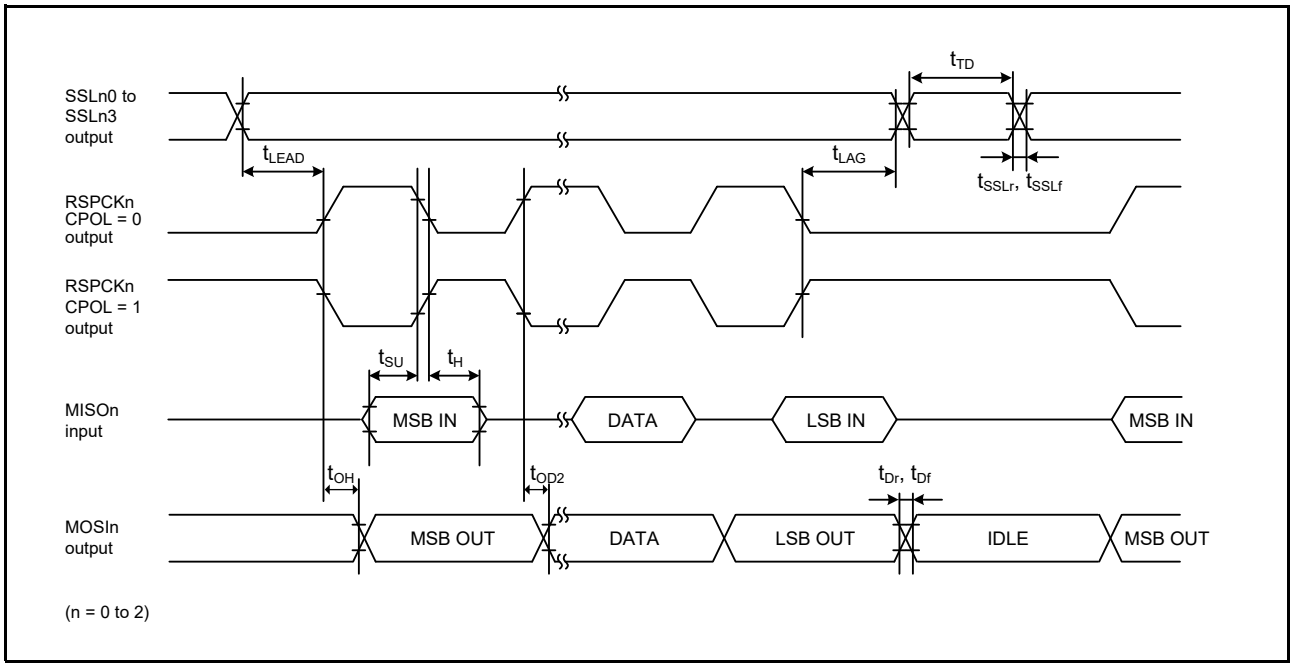


Figure 2.59 RSPIA Timing (Master, Motorola SPI, CPHA = 1)

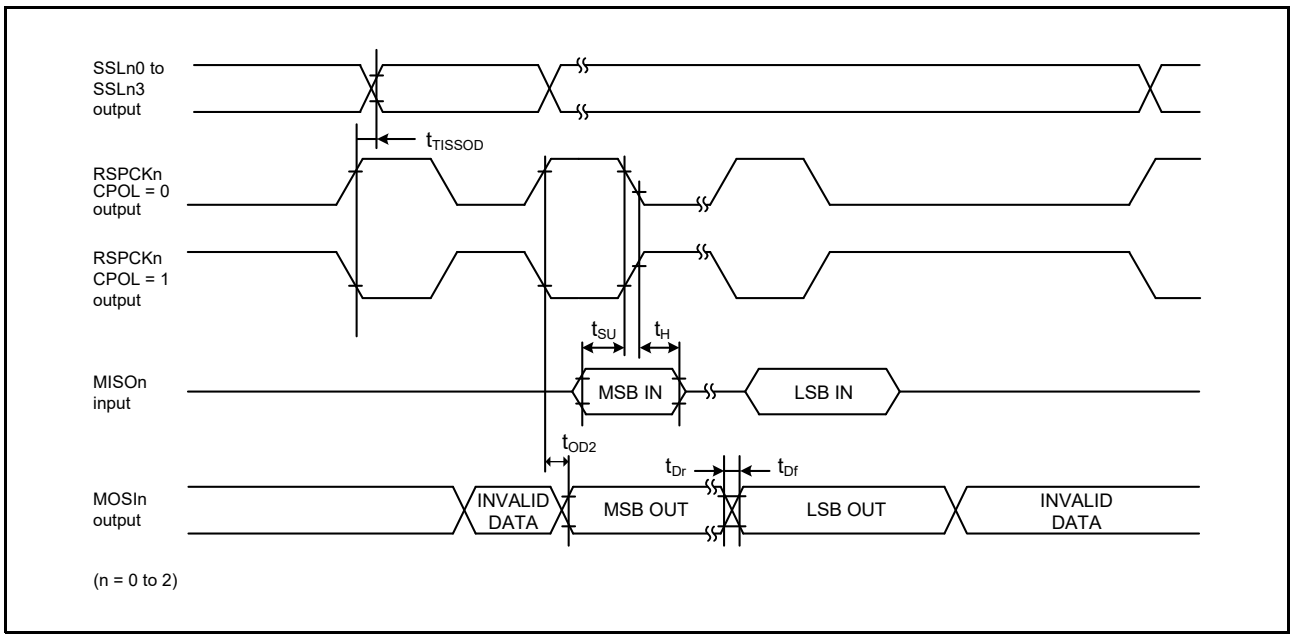


Figure 2.60 RSPIA Timing (Master, TI SSP)

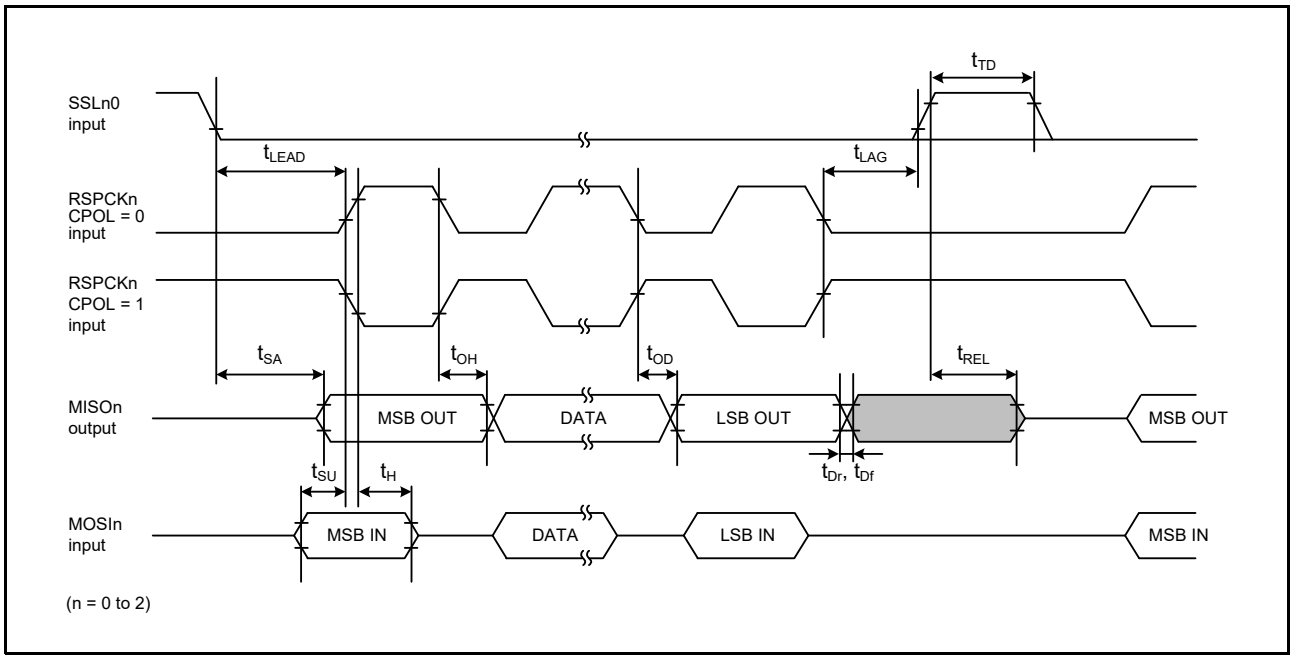


Figure 2.61 RSPIA Timing (Slave, Motorola SPI, CPHA = 0)

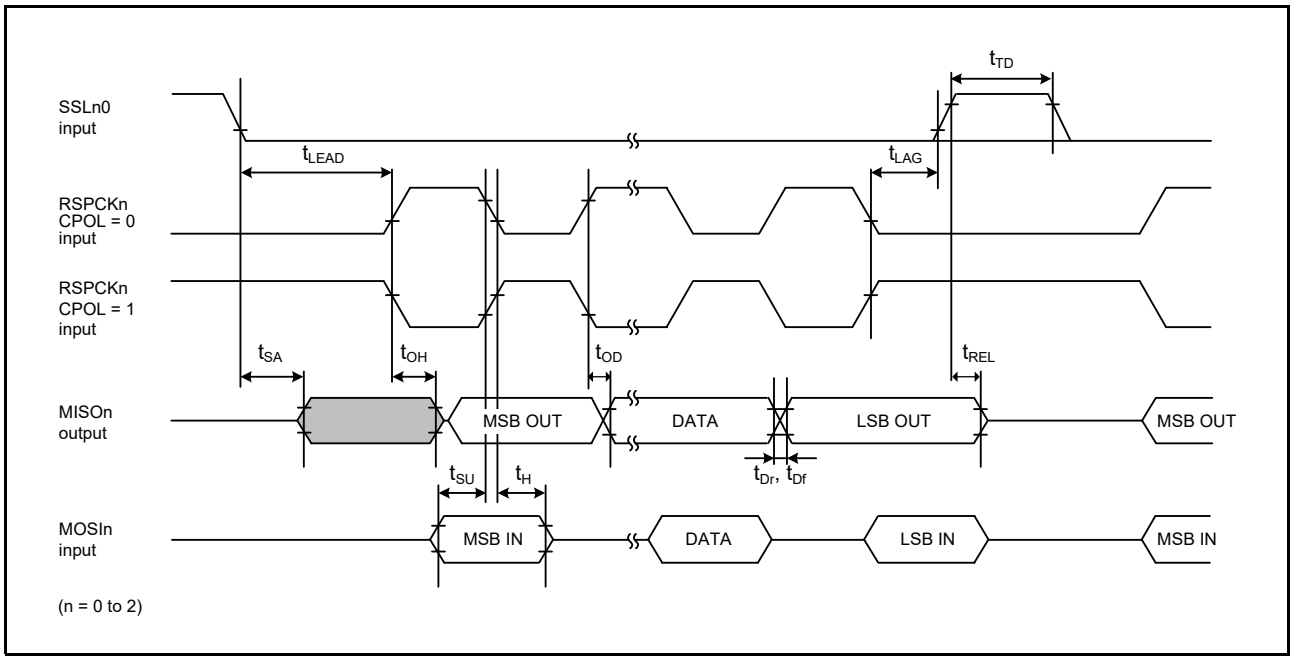


Figure 2.62 RSPIA Timing (Slave, Motorola SPI, CPHA = 1)

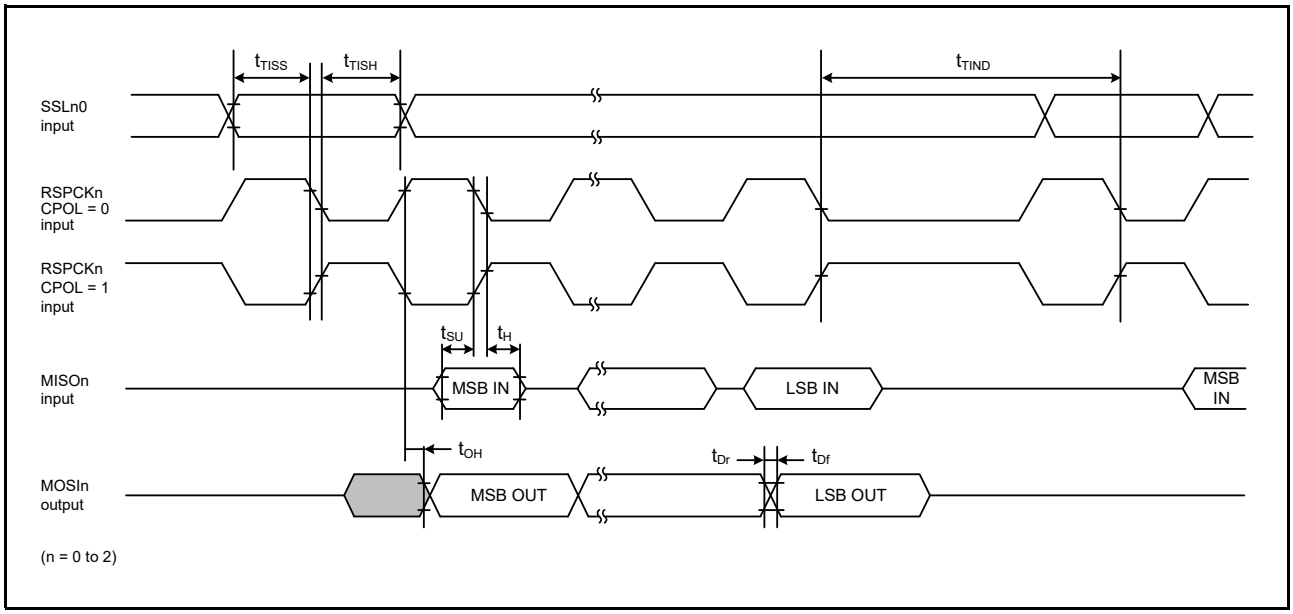


Figure 2.63 RSPIA Timing (Slave, TI SSP, with Inter-Frame Delay)

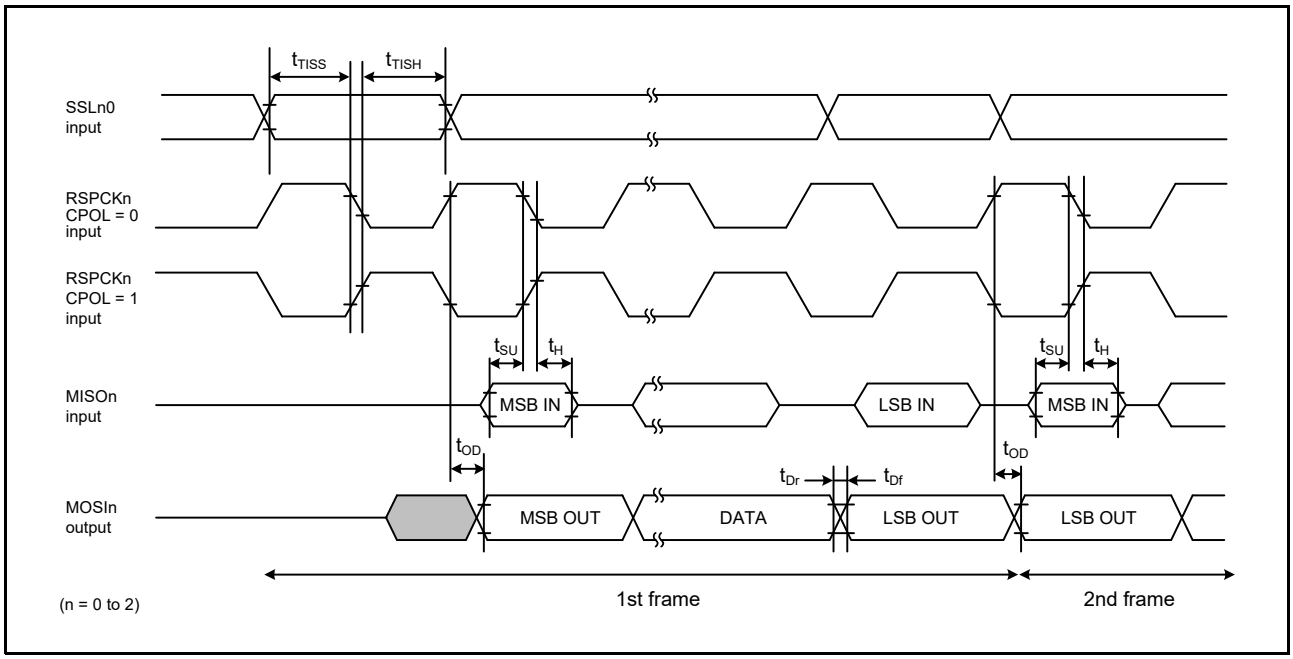


Figure 2.64 RSPIA Timing (Slave, TI SSP, with No Inter-Frame Delay)

2.5.7.8 XSPI

Table 2.86 XSPI Master Timing

Conditions: Capacitive load C = 15 pF,
When VCC/VCC2 ≥ 2.7 V: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the XSPIn_CK, XSPIn_DS, and XSPIn_IO0 to XSPIn_IO7 pins are set for DRV6.
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the XSPIn_CS0# and XSPIn_CS1# pins are set for DRV3.
When VCC/VCC2 < 2.0 V: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the XSPIn_CK, XSPIn_DS, and XSPIn_IO0 to XSPIn_IO7 pins are set for DRV8.
The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the XSPIn_CS0# and XSPIn_CS1# pins are set for DRV4.

Item			VCC/VCC2	Symbol	Min.	Max.	Unit	Test Conditions
XSPI master	Cycle time	SDR without the XSPIn_DS pin	2.70 V or higher	t_{PERIOD}	16.67	—	ns	Figure 2.65
			Less than 2.00 V		20.00	—		
		DDR with the XSPIn_DS pin*1			7.5	—		
	Clock output slew rate			t_{SRck}	0.75	—	V/ns	
	Clock duty cycle-distortion			t_{CKDCD}	0	0.375	ns	
	Clock minimum pulse width			t_{CKMPW}	3.375	—	ns	
	DS Duty cycle distortion			t_{DSDCD}	0	0.3	ns	
	DS minimum pulse width			t_{DSMPW}	3.075	—	ns	
	Data input/output slew rate			t_{SR}	1.37	—	ns	
	Data input setup time	SDR without the XSPIn_DS pin	2.70 V or higher	t_{SU}	8.17	—	ns	Figure 2.66
			Less than 2.00 V		13.0	—		
	Data input hold time	SDR without the XSPIn_DS pin		t_H	0.5	—	ns	
	Data output valid time*2	SDR without the XSPIn_DS pin		t_{OV}	—	5.4	ns	
	Data output hold time	SDR without the XSPIn_DS pin		t_{OH}	–5.4	—	ns	
	Data output buffer off time	SDR without the XSPIn_DS pin		t_{BOFF}	–5.4	—	ns	
	Data input setup time	DDR with the XSPIn_DS pin*1		t_{SU}	–0.7	—	ns	Figure 2.67, Figure 2.68
	Data input hold time	DDR with the XSPIn_DS pin*1		t_H	2.375	—	ns	
	Data output valid time*2	DDR with the XSPIn_DS pin*1		t_{OV}	—	$t_{PERIOD}/4 + 0.6$	ns	
	Data output hold time	DDR with the XSPIn_DS pin*1		t_{OH}	0.9	—	ns	
	Data output buffer off time	DDR with the XSPIn_DS pin*1		t_{BOFF}	0.9	—	ns	
	Time from clock low to XSPIn_CSi# low			t_{CKLCSL}	6	—	ns	Figure 2.66, Figure 2.67, Figure 2.68
	Time from XSPIn_CSi# low to clock high*3			t_{CSLCKH}	6	—	ns	
	Time from clock low to XSPIn_CSi# high			t_{CKLCSH}	6	—	ns	
	Time from XSPIn_CSi# high to clock high			t_{CSHCKH}	6	—	ns	
	Time from XSPIn_DS low to XSPIn_CSi# high			t_{DSLCSH}	$0.8 \times t_{PERIOD}$	—	ns	Figure 2.69
	Time from XSPIn_CSi# high to XSPIn_DS tristate			t_{CSHDST}	—	t_{PERIOD}	ns	
	Time when XSPIn_CSi# low to XSPIn_DS low input *3, *4			t_{CSLDSL}	0	12.5	ns	
	Time from XSPIn_DS tristate to XSPIn_CSi# low			t_{DSTCSL}	0	—	ns	

n = 0, 1; i = 0, 1

Note 1. For products with part numbers of the form R5K574Mxx4Fx, only use this value for reference.
Note 2. COMCFG.OEASTEX = 1
Note 3. LIOCFGCSx.CSASTEX = 1
Note 4. When using a JESD251 Profile 1.0 memory with an external pull-down connected to the XSPIn_DS pin, you do not need to follow this restriction.

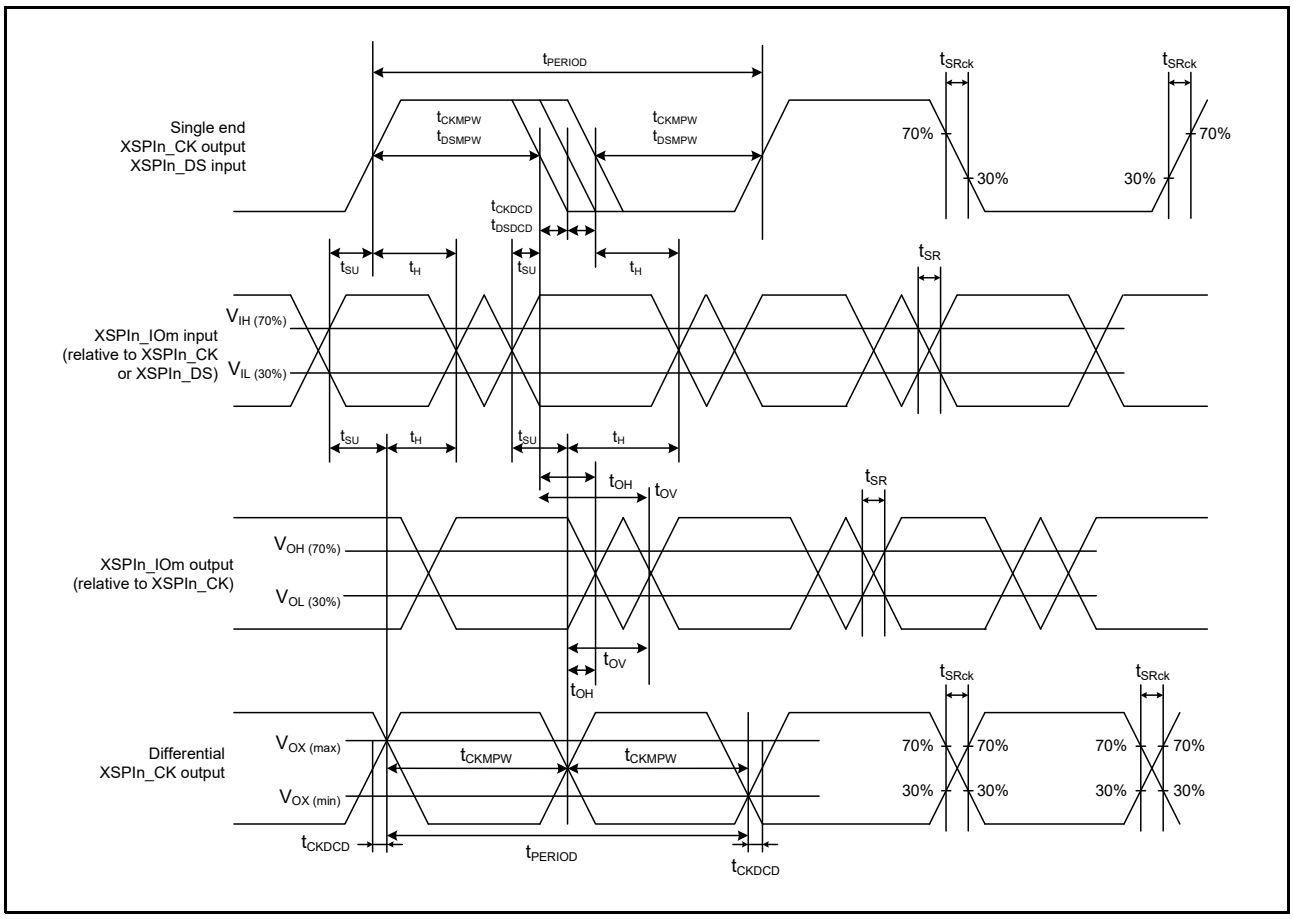


Figure 2.65 XSPI Clock/DS Timing (n = 0, 1; m = 0 to 7)

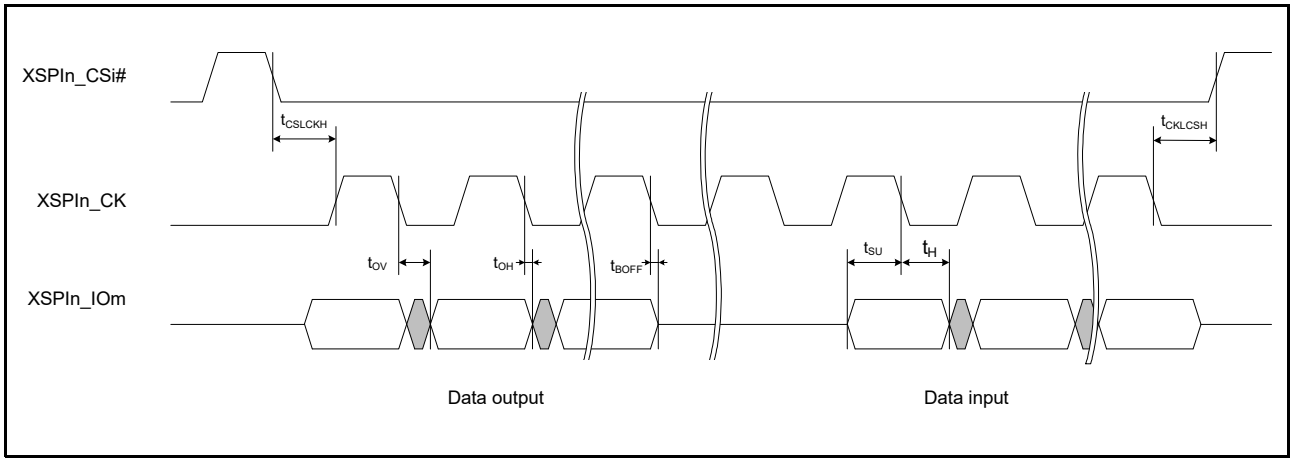


Figure 2.66 SDR Transmit/Receive Timing (1S-1S-1S, 1S-2S-2S, 2S-2S-2S, 1S-4S-4S, 4S-4S-4S) (n = 0, 1; m = 0 to 7; i = 0, 1)

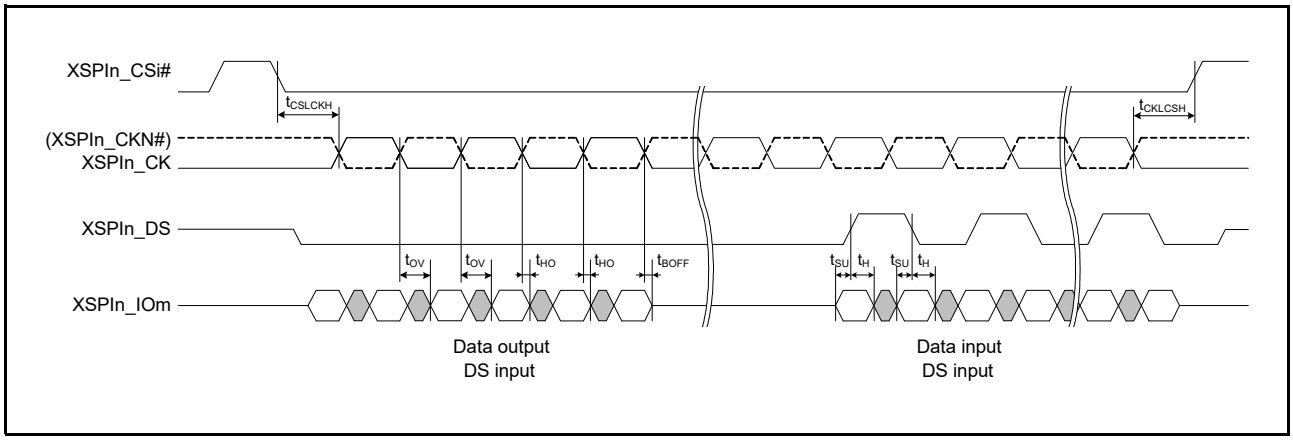


Figure 2.67 DDR Transmit/Receive Timing (4S-4D-4D, 8D-8D-8D) (n = 0, 1; m = 0 to 7; i = 0, 1)

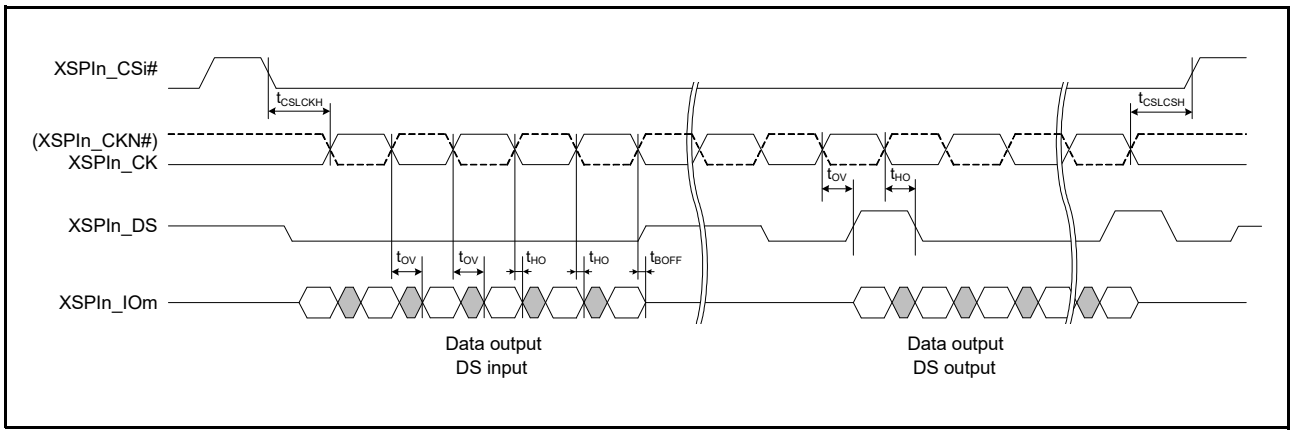


Figure 2.68 DDR Transmit/Receive Timing (HyperRAM write) (n = 0, 1; m = 0 to 7; i = 0, 1)

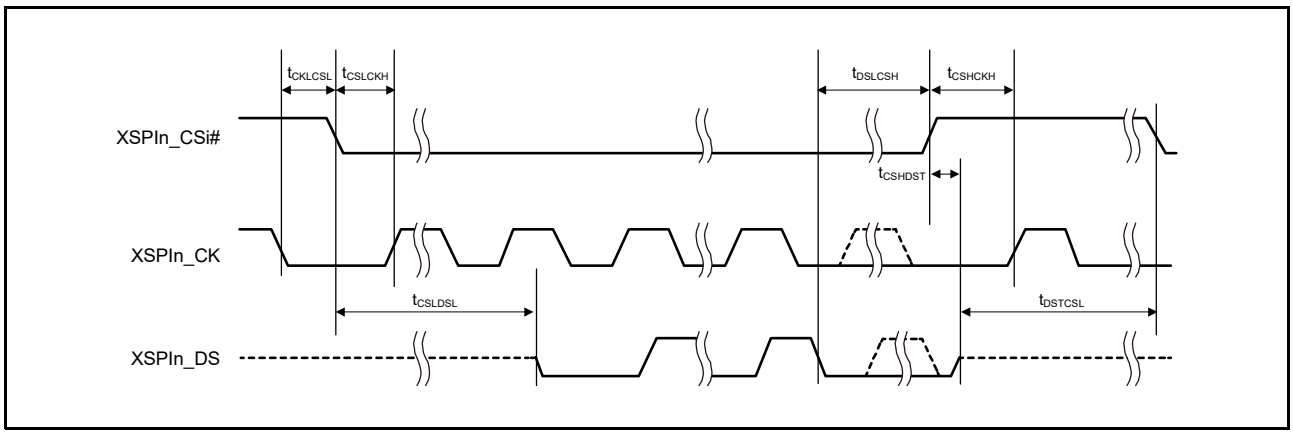


Figure 2.69 DS to CS Signal Timing (n = 0, 1; i = 0, 1)

Table 2.87 XSPI Slave Timing

Conditions: Capacitive load C = 15 pF,
When VCC/VCC2 ≥ 2.7 V: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV6.
When VCC/VCC2 < 2.0 V: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV8.

Item			VCC/VCC2	Symbol	Min.	Max.	Unit	Test Conditions
XSPI slave	Cycle time	SDR without the XSPIn_DS pin		t_{PERIOD}	40	—	ns	Figure 2.70
		DDR with the XSPIn_DS pin*1			10	—		
	Clock output slew rate			t_{SRck}	0.56	—	V/ns	
	Clock duty cycle-distortion			t_{CKDCD}	0	0.5	ns	
	Clock minimum pulse width			t_{CKMPW}	4.5	—	ns	
	DS Duty cycle distortion			t_{DSDCD}	0	0.4	ns	
	DS minimum pulse width			t_{DSMPW}	4.1	—	ns	
	Data input/output slew rate		2.70 V or higher	t_{SR}	1.03	—	ns	
			Less than 2.00 V		0.56	—		
	Data input setup time	SDR without the XSPIn_DS pin		t_{SU}	2.5	—	ns	Figure 2.71
	Data input hold time	SDR without the XSPIn_DS pin		t_{H}	2.5	—	ns	
	Data output valid time	SDR without the XSPIn_DS pin		t_{OV}	—	14	ns	
	Data output hold time	SDR without the XSPIn_DS pin		t_{OH}	0	—	ns	
	Data output buffer off time	SDR without the XSPIn_DS pin		t_{BOFF}	—	2 × t_{PERIOD}	ns	
	Data input setup time	DDR with the XSPIn_DS pin*1		t_{SU}	1	—	ns	Figure 2.72, Figure 2.73
	Data input hold time	DDR with the XSPIn_DS pin*1		t_{H}	1	—	ns	
	Data output skew time*2	DDR with the XSPIn_DS pin*1		t_{RQ}	0.8	—	ns	
	Data output skew hold time	DDR with the XSPIn_DS pin*1		t_{RQH}	0.8	—	ns	
	Data output buffer off time	DDR with the XSPIn_DS pin*1		t_{BOFF}	—	2 × t_{PERIOD}	ns	
	Time from clock low to XSPIn_CSi# low			t_{CKLCSL}	6	—	ns	Figure 2.71, Figure 2.72, Figure 2.73
	Time from XSPIn_CSi# low to clock high			t_{CSLCKH}	6	—	ns	
	Time from clock low to XSPIn_CSi# high			t_{CKLCSH}	6	—	ns	
	Time from XSPIn_CSi# high to clock high			t_{CSHCKH}	6	—	ns	
	Time from XSPIn_DS low to XSPIn_CSi# high			t_{DSLCSH}	0.8 × t_{PERIOD}	—	ns	Figure 2.74
	Time from XSPIn_CSi# high to XSPIn_DS tristate			t_{CSHDST}	—	2 × t_{PERIOD}	ns	
	Time when XSPIn_CSi# low to XSPIn_DS low input*3		2.70 V or higher	t_{CSLDSL}	0	15	ns	
			Less than 2.00 V		0	19		
	Time from XSPIn_DS tristate to XSPIn_CSi# low			t_{DSTCSL}	0	—	ns	

n = 0, 1; i = 0, 1

Note 1. For products with part numbers of the form R5K574Mxx4Fx, only use this value for reference.

Note 2. L15CFG0.OEASTEX = 1

Note 3. When using a JESD251 Profile 1.0 memory with an external pull-down connected to the XSPIn_DS pin, you do not need to follow this restriction.

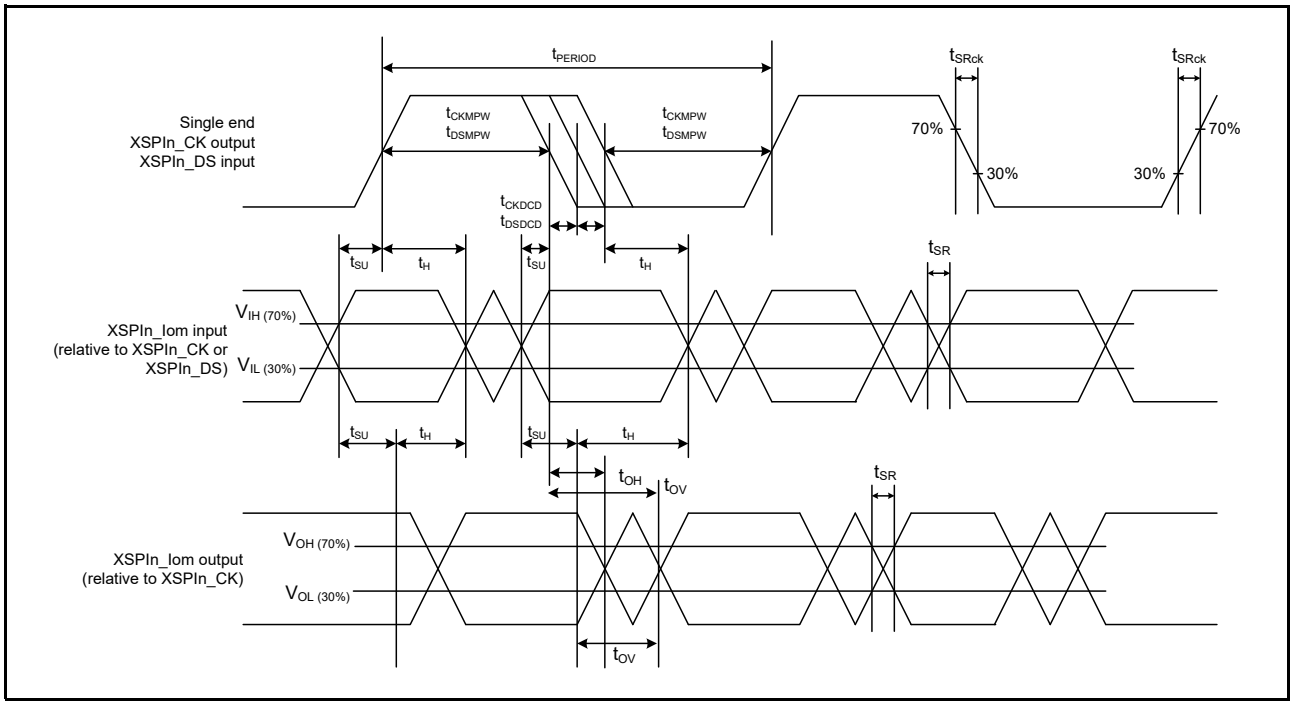


Figure 2.70 XSPI Clock/DS Timing (n = 0, 1; m = 0 to 7)

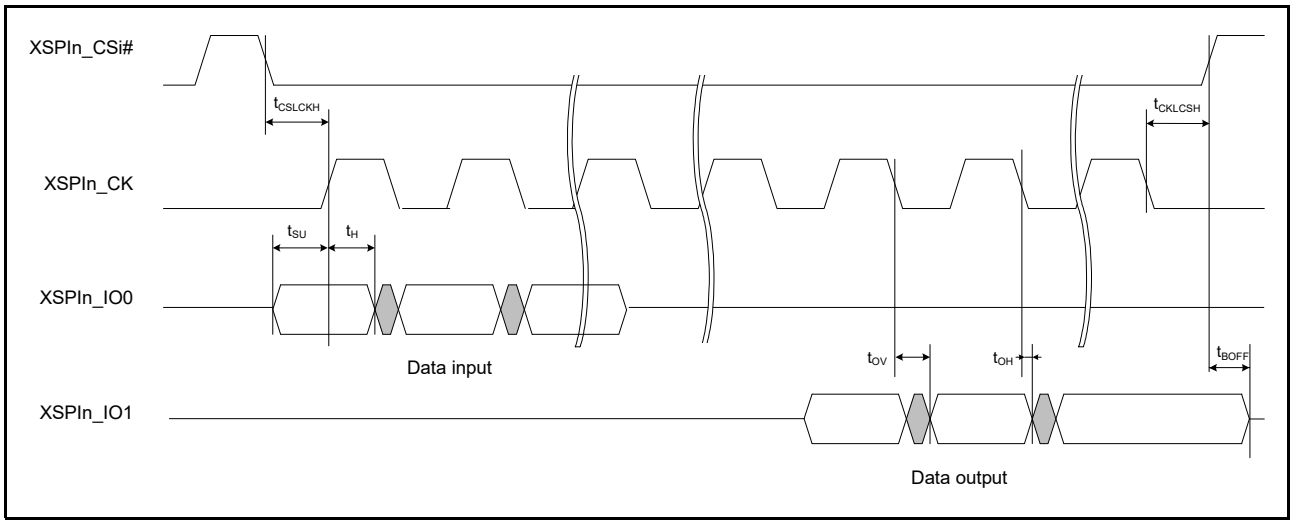


Figure 2.71 SDR Transmit/Receive Timing (1S-1S-1S) (n = 0, 1; i = 0, 1)

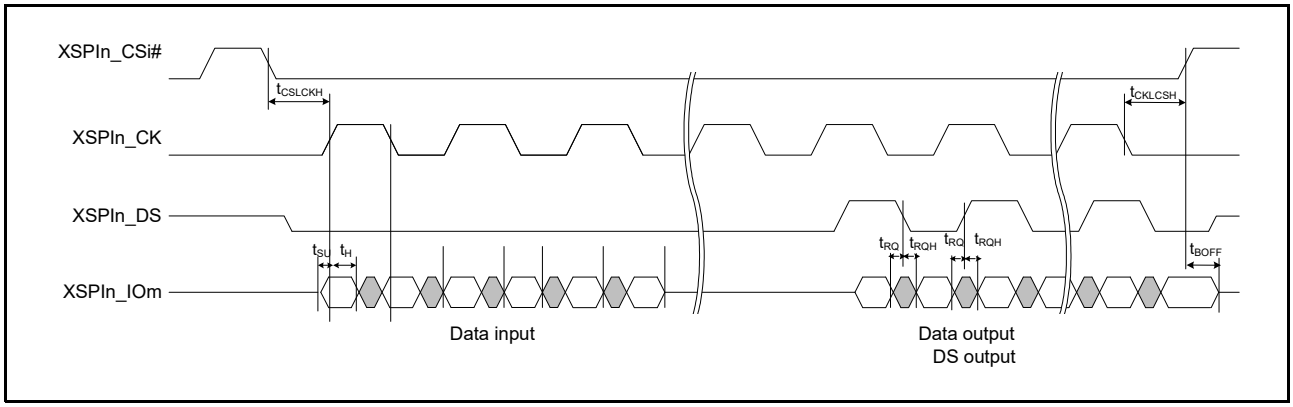


Figure 2.72 DDR Transmit/Receive Timing (4S-4D-4D, 8D-8D-8D) (n = 0, 1; m = 0 to 7; i = 0, 1)

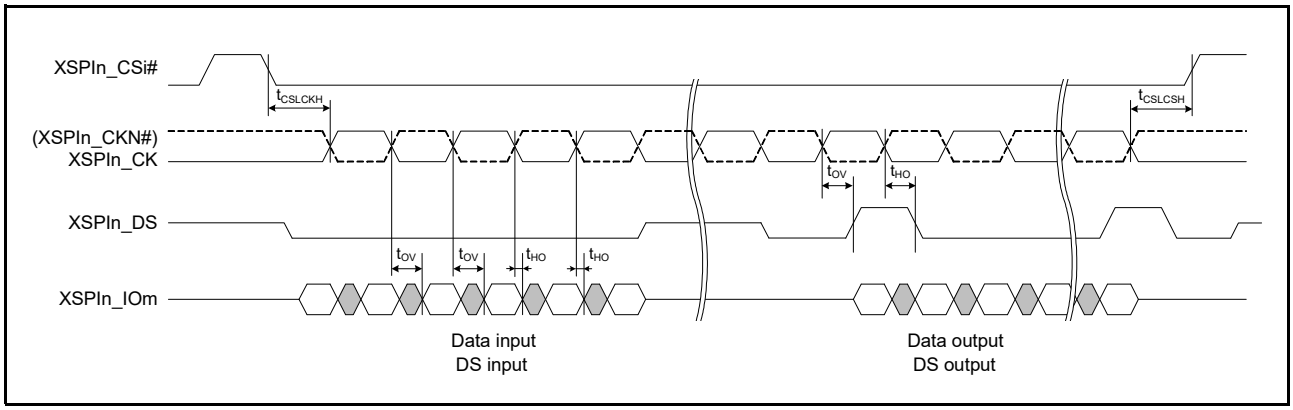


Figure 2.73 DDR Transmit/Receive Timing (HyperRAM write) (n = 0, 1; m = 0 to 7; i = 0, 1)

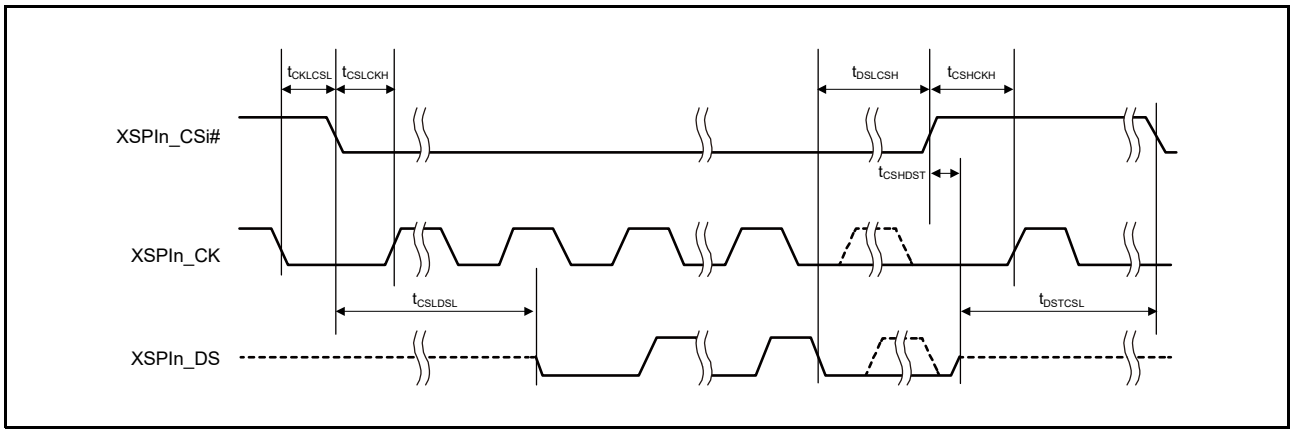


Figure 2.74 DS to CS Signal Timing (n = 0, 1; i = 0, 1)

2.5.7.9 RIICHS

Table 2.88 RIICHS Timing (1) (1/2)

Conditions: VCC = 1.62 to 1.98 V or VCC = 2.70 to 3.63 V,
Evaluation was with either of the following driving ability settings for the target pins, depending on the VCC voltage.
When VCC = 1.62 to 1.98 V: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV3.
When VCC = 2.70 to 3.63 V: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV2.

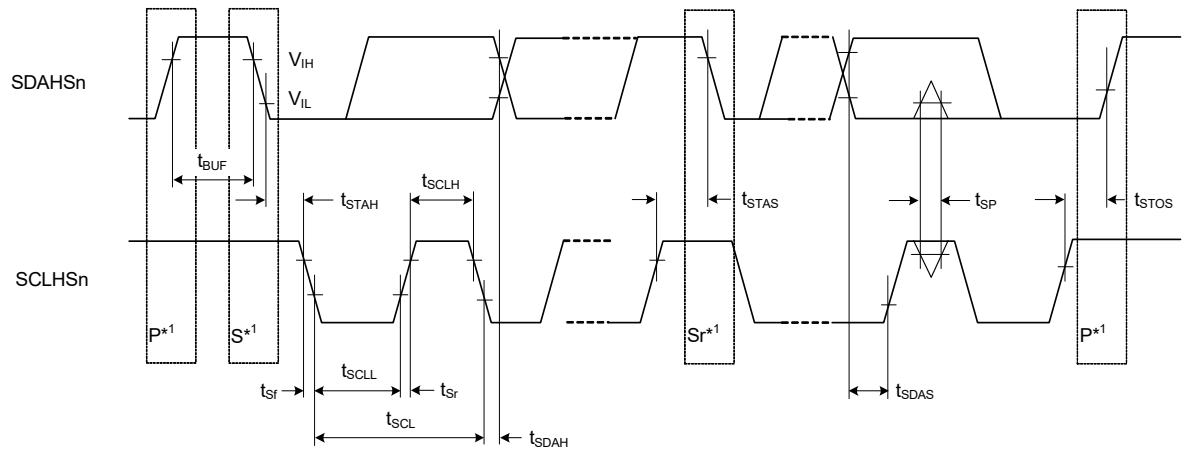
Item		Wakeup Function	Symbol	Min.*1	Max.*1	Unit	Test Conditions
RIICHS (Standard-mode, SMBus) ICFER.FMPE = 0	SCLHS input cycle time		t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.75
	SCLHS input high pulse width		t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCLHS input low pulse width		t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCLHS, SDAHS input rise time		t_{Sr}	—	1000	ns	
	SCLHS, SDAHS input fall time		t_{Sf}	—	300	ns	
	SCLHS, SDAHS input spike pulse removal time		t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDAHS input bus free time	Enabled	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
		Disabled		3(6) × t_{IICcyc} + 4 × t_{PAcyc} + 300	—		
	Start condition input hold time	Enabled	t_{STAH}	t_{IICcyc} + 300	—	ns	
		Disabled		1(5) × t_{IICcyc} + t_{PAcyc} + 300	—		
	Restart condition input setup time		t_{STAS}	1000	—	ns	
	Stop condition input setup time		t_{STOS}	1000	—	ns	
	Data input setup time		t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time		t_{SDAH}	0	—	ns	
	SCLHS, SDAHS capacitive load		C_b*2	—	400	pF	
RIICHS (Fast-mode)*3 ICFER.FMPE = 0	SCLHS input cycle time		t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	Figure 2.75
	SCLHS input high pulse width		t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCLHS input low pulse width		t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCLHS, SDAHS input rise time		t_{Sr}	20 × (External pull-up voltage/5.5 V)	300	ns	
	SCLHS, SDAHS input fall time		t_{Sf}	20 × (External pull-up voltage/5.5 V)	300	ns	
	SCLHS, SDAHS input spike pulse removal time		t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDAHS input bus free time	Enabled	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
		Disabled		3(6) × t_{IICcyc} + 4 × t_{PAcyc} + 300	—		
	Start condition input hold time	Enabled	t_{STAH}	t_{IICcyc} + 300	—	ns	
		Disabled		1(5) × t_{IICcyc} + t_{PAcyc} + 300	—		
	Restart condition input setup time		t_{STAS}	300	—	ns	
	Stop condition input setup time		t_{STOS}	300	—	ns	
	Data input setup time		t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time		t_{SDAH}	0	—	ns	
	SCLHS, SDAHS capacitive load		C_b*2	—	400	pF	

Table 2.88 RIICHS Timing (1) (2/2)

Conditions: VCC = 1.62 to 1.98 V or VCC = 2.70 to 3.63 V,
Evaluation was with either of the following driving ability settings for the target pins, depending on the VCC voltage.
When VCC = 1.62 to 1.98 V: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV3.
When VCC = 2.70 to 3.63 V: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV2.

Item		Wakeup Function	Symbol	Min.*1	Max.*1	Unit	Test Conditions
RIICHS (Fast-mode Plus) *3 ICFER.FMPE = 1	SCLHS input cycle time		t_{SCL}	$6(12) \times t_{IICcyc} + 240$	—	ns	Figure 2.75
	SCLHS input high pulse width		t_{SCLH}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCLHS input low pulse width		t_{SCLL}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCLHS, SDAHS input rise time		t_{Sr}	—	120	ns	
	SCLHS, SDAHS input fall time		t_{Sf}	—	120	ns	
	SCLHS, SDAHS input spike pulse removal time		t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDAHS input bus free time	Enabled	t_{BUF}	$3(6) \times t_{IICcyc} + 120$	—	ns	
		Disabled		$3(6) \times t_{IICcyc} + 4 \times t_{PAcyc} + 120$	—		
	Start condition input hold time	Enabled	t_{STAH}	$t_{IICcyc} + 120$	—	ns	
		Disabled		$1(5) \times t_{IICcyc} + t_{PAcyc} + 120$	—		
	Restart condition input setup time		t_{STAS}	120	—	ns	
	Stop condition input setup time		t_{STOS}	120	—	ns	
	Data input setup time		t_{SDAS}	$t_{IICcyc} + 30$	—	ns	
	Data input hold time		t_{SDAH}	0	—	ns	
	SCLHS, SDAHS capacitive load		C_b*2	—	550	pF	

Note: The pin names include either -A or -B as a suffix to indicate the group to which the given pin belongs. Make sure that pins to be used for a given RIICHS interface are from the same group.
Note: t_{IICcyc}: RIICHS internal reference clock (IICφ) cycle; t_{PAcyc}: PCLKA cycle
Note 1. Numbers enclosed in parentheses are for the case where the ICFER.NFE bit is set to 1, enabling the digital filter, and the ICMR3.NF[1:0] bits are set to 11b.
Note 2. C_b is the total capacitance of the bus lines.
Note 3. These electrical characteristics are only guaranteed when pins with the suffix -A, indicating the group name, as part of the pin name are in use.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
$V_{IH} = 0.7 \times VCC$, $V_{IL} = 0.3 \times VCC$
$V_{OL} = 0.6$ V, $I_{OL} = 6$ mA

Figure 2.75 RIICHS Bus Interface Input/Output Timing (n = 1, 2)

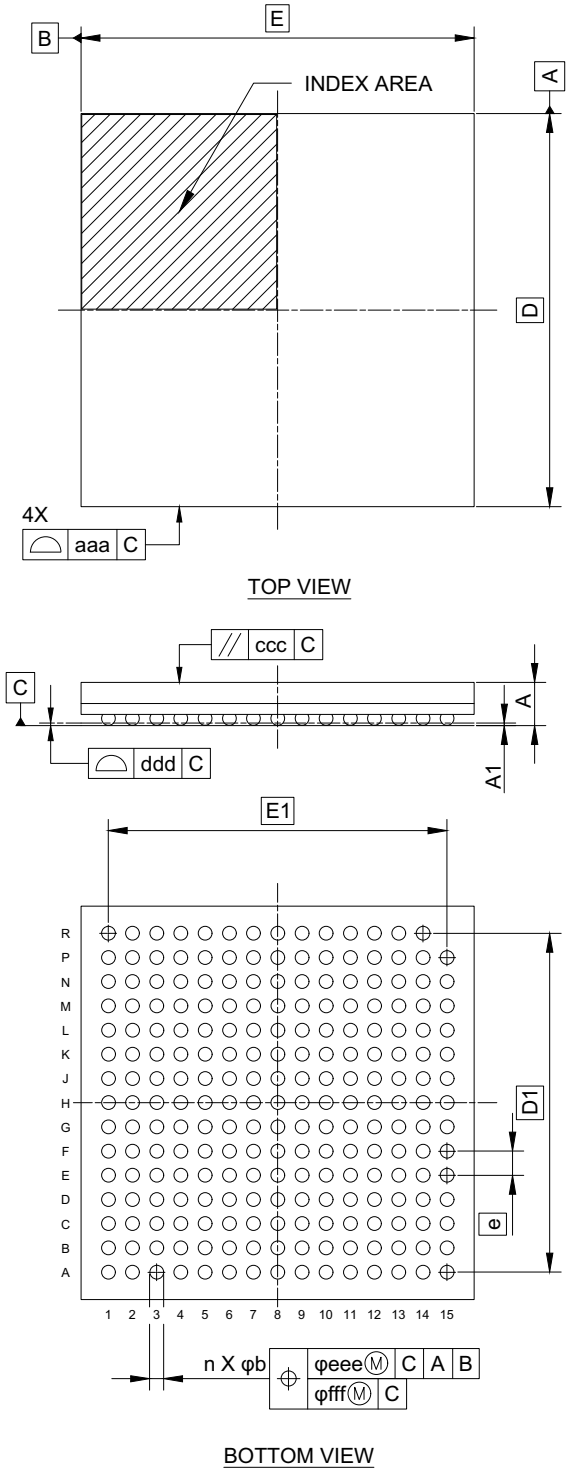
Table 2.89 RIICHS Timing (2)

Conditions: VCC = 1.65 to 1.95 V or VCC = 2.97 to 3.63 V,
Evaluation was with either of the following driving ability settings for the target pins, depending on the VCC voltage.
When VCC = 1.65 to 1.95 V: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV3.
When VCC = 2.97 to 3.63 V: The driving ability select bits (PmnPFS.DSCR[3:0]) corresponding to the target pins are set for DRV2.

Item		Load capacitance*2	Symbol	Min.*1	Max.*1	Unit	Test Conditions
RIICHS (Hs-mode) ICFER.HSME = 1	SCLHS input cycle time		t_{SCL}	46(48) × t_{IICcyc}	—	ns	Figure 2.76
	SCLHS input high pulse width	C_b = 400 pF	t_{SCLH}	29(30) × t_{IICcyc}	—	ns	
		C_b = 100 pF		13(14) × t_{IICcyc}	—		
	SCLHS input low pulse width	C_b = 400 pF	t_{SCLL}	69(70) × t_{IICcyc}	—	ns	
		C_b = 100 pF		33(34) × t_{IICcyc}	—		
	SCLHS input rise time	C_b = 400 pF	t_{SrCL}	—	80	ns	
		C_b = 100 pF		—	40		
	SDAHS input rise time	C_b = 400 pF	t_{SrDA}	—	160	ns	
		C_b = 100 pF		—	80		
	SCLHS input fall time	C_b = 400 pF	t_{SfCL}	—	80	ns	
		C_b = 100 pF		—	40		
	SDAHS input fall time	C_b = 400 pF	t_{SfDA}	—	160	ns	
		C_b = 100 pF		—	80		
	SCLHS, SDAHS input spike pulse removal time		t_{SP}	0	1(1) × t_{IICcyc}	ns	
	Restart condition input setup time		t_{STAS}	40	—	ns	
	Stop condition input setup time		t_{STOS}	40	—	ns	
	Data input setup time		t_{SDAS}	10	—	ns	
	Data input hold time	C_b = 400 pF	t_{SDAH}	0	150	ns	
		C_b = 100 pF		0	70		
	SCLHS, SDAHS capacitive load		C_b*2	—	400	pF	

Note: The pin names include either -A or -B as a suffix to indicate the group to which the given pin belongs. Make sure that pins to be used for a given RIICHS interface are from the same group.
Note: t_{IICcyc}: RIICHS internal reference clock (IICφ) cycle
Note 1. Numbers enclosed in parentheses are for the case where the ICFER.NFE bit is set to 1, enabling the digital filter, and the ICMR3.NF[1:0] bits are set to 11b.
Note 2. C_b is the total capacitance of the bus lines.

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA224-13x13-0.80	PLBG0224GE-A	-



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	13.00	—
E	—	13.00	—
D1	—	11.20	—
E1	—	11.20	—
A	—	—	1.60
A1	0.31	—	—
b	0.41	0.46	0.51
e	—	0.80	—
aaa	—	—	0.15
ccc	—	—	0.20
ddd	—	—	0.20
eee	—	—	0.15
fff	—	—	0.08
N	—	224	—

Figure B 224-Pin LFBGA (PLBG0224GE-A)