

Radiation-Tolerant Non-Isolated DC-to-DC Point of Load Converter

POL-05-20S-T



Introduction

The POL-05-20S-T is a high efficiency Point-of-Load (POL) converter using GaN power HEMTs to achieve high efficiency and increased power density. This device can deliver up to 20A of output current in a small form factor and supports an input voltage range of 4.75V to 13.2V. The POL-05-20S-T utilizes a synchronous buck topology with current mode control to achieve fast switching frequency and a robust, stable design.

The POL-05-20S-T is optimized for high current, fast transient applications, such as the core rails of FPGAs, ASICs and other high processing intensive digital loads. The device is available in a 25g, 1.51" × 1.51" × 0.45" surface mount package with adjustable output voltage.

This device is intended for harsh environments, such as space, with electrical parameters specified pre and post irradiation up to 50 krad(Si) and Single Event Effects (SEE) characterized up to a Linear Energy Transfer (LET) of 43 MeV·cm²/mg. The POL-05-20S-T operates over a temperature range of -55 °C to 100 °C at full load.

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1. Features and Applications

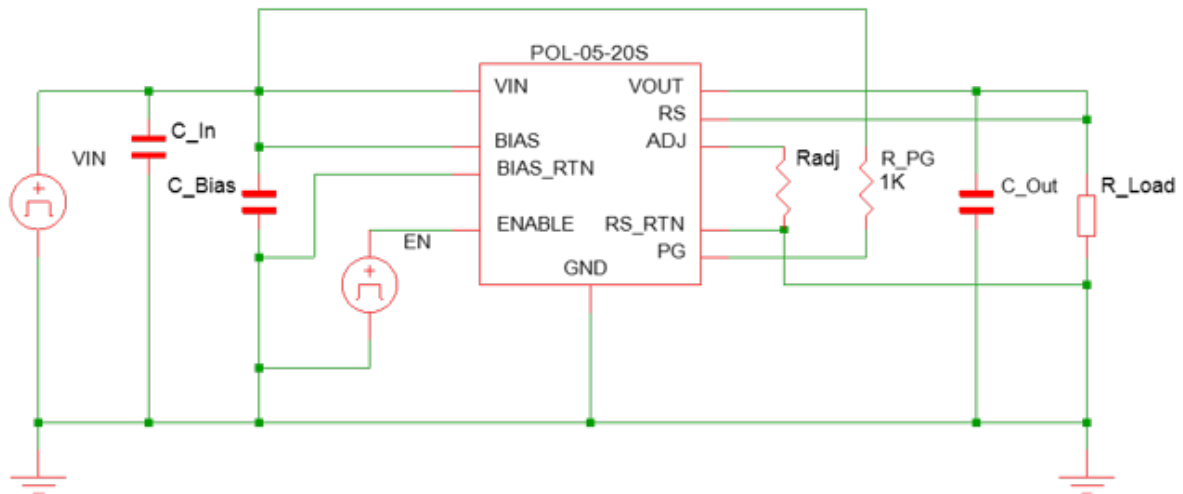
Features

- Up to 20A Continuous Output
- Wide Input Voltage Range: 4.75V–13.2V
- Adjustable Output Voltage
- GAN FETs to Achieve High Efficiency
- Tight Output Voltage Variation During Load Transient with Internal Droop Feature
- Current Mode Synchronous Back Topology
- Enable Pin for Electrical ON/OFF
- Power-Good Indicator

Applications

- High Current, Fast Transient, Space FPGAs and MCUs Application

Figure 1-1. Typical Application Connection Diagram



2. Functional Description

2.1. Operation and Topology

POL-05-20S-T is a high current, non-isolated, fixed frequency, radiation-tolerant synchronous buck converter which can step-down voltages from 4.75V to 13.2V V_{in} to as low as 0.7V output. By utilizing GAN FETs and 400 kHz switching frequency, it is optimized for high current, low voltage Point-of-Load application.

2.2. Bias Voltage

The BIAS voltage powers internal components of the converter. A BIAS voltage pin can be powered separately or tied to V_{IN} . If the bus is noisy, a separate BIAS voltage with external bypass capacitors of 1uF and 0.1uF, closely placed next to the BIAS voltage pin, is recommended.

2.3. External Components

External input capacitors are optional but recommended when operating at input voltages greater than 5V. When operating from a 12V input source, a minimum of two T598D107M025ATE050 capacitors is recommended. A minimum output capacitance of 330 uF is required. Additional low-ESR capacitance may be required to prevent OVP and UVP trips during transient load conditions.

2.4. Enable (ENABLE)

The Enable voltage threshold is 1.58V with 300 mV hysteresis, and it must be persistent at least 80 us. This pin has an internal pull-down to keep the converter off if the pin is left unconnected. A 5 K Ω resistor connected to BIAS will automatically enable the unit, and an open-collector or open-drain buffer can be implemented to disable the unit in applications where this pin is driven by microcontrollers or FPGA.

2.5. Power Good (PG)

The Power Good pin is an output indicator signaling the output is within +/-5% of regulation setpoint. It is an open-drain output capable of sinking up to 5 mA. An external buffer is needed to drive more current otherwise connect to V_{IN} through a 5 K Ω resistor. The nominal response time of PG is less than 20 uSec, except at power up or when the converter enters auto-restart mode where the nominal response time is 3 mSec.

2.6. Remote Sense (RS) and Remote Sense Return (RS_RTN)

True differential remote sensing to maintain output voltage accuracy by sensing across the load via RS and RS_RTN pins, thereby compensating for voltage drops along trace/planes carrying high current. The unit will compensate for a maximum total voltage drop of 0.25V.

2.7. Output Voltage and Adjust Pin (ADJ)

Output voltage is adjustable from 0.7V–5.0V by connecting the ADJ pin to the RS_RTN pin through a resistor or a combination of resistors. Use the equation and table below to determine the value of resistance. The suggested resistor values are for light load condition. The output voltage at high loads decreases slightly because of the Droop feature. The output voltage is 0.7V by default with the ADJ pin unconnected.

$$R_{ADJ(K\Omega)} = 4.32 \times \frac{5.098 - V_{out}(V)}{V_{out}(V) - 0.70897}$$

Where: $0.8 \leq V_{out}(V) \leq 5.0V$

$V_{out} = 0.70V$ and $5.09V$ if $R_{ADJ(K\Omega)}$ is open and short respectively

Table 2-1. ADJ Resistance Value

Output Voltage(V)	Target Trimming Resistance
0.8V	204 k Ω
1.0V	60.8 k Ω
1.2V	34.4 k Ω
1.5V	19.6 k Ω
1.8V	13.0 k Ω
2.0V	10.4 k Ω
2.5V	6.26 k Ω
3.3V	2.98 k Ω
5.0V	98.8 Ω

2.8. Soft-start and Output Voltage

The internal soft-start circuit ramps up the voltage in a controlled manner to limit inrush current and overshoot during startup. The output voltage rise time is approximately 5 ms.

2.9. Droop Regulation

Internal droop regulation is implemented to minimize output variation during load transients by changing the output voltage inversely to the output load current. As the load increases, the output voltage decreases. It is recommended to trim the output voltage at minimum load to the highest acceptable voltage.

2.10. Overvoltage (OVP) and Undervoltage (UVP) Protection

Overvoltage/undervoltage protection is triggered when the output voltage exceeds (V_{OVP}) or (V_{UVP}) respectively. The PG pin goes low, and the output voltage drops, but the unit does not shut down. The unit will continuously attempt to restart until the fault conditions are removed.

3. Absolute Maximum Ratings

Rating	Value
V _{IN} and V _{BIAS} range	0 VDC to 16 VDC
Output current	20A
Output power	50W
Operating temperature	–55 °C to 100 °C
Storage temperature	–55 °C to 125 °C
Shock	1500 gpk, 0.5 ms, ½ sine
Constant acceleration	50g
Random vibration	24.06 grms, 50 Hz to 2000 Hz

4. Electrical Parameters

This section shows the electrical parameters of the POL-05-20S-T Single Series device under the following conditions unless otherwise specified: $T_J = -40\text{ }^{\circ}\text{C}$ to $+100\text{ }^{\circ}\text{C}$, $V_{IN} = +5\text{V}$ or $+12\text{V}$, Full Load

Parameter	Output	Conditions	Min	Nom	Max	Units	
Input Voltage							
V _{IN}	—	—	0	5	13.2	V	
BIAS Voltage							
V _{BIAS}	—	—	4.75	5	13.2	V	
Undervoltage Lockout, Note 1							
V _{BIAS_UVLO_ON}	—	Enable = V _{BIAS}	4.05	4.2	4.4	V	
V _{BIAS_UVLO_OFF}	—	Enable = V _{BIAS}	3.85	4.0	4.1	V	
H _{YSTERESIS}	—	Enable = V _{BIAS}	150	220	300	mV	
No Load Input Current							
I _{IN}	—	I _{OUT} =0,ENABLE High	—	85	90	mA	
		ENABLE Low	—	7	15		
Adjustable Output Voltage Range							
V _{OUT}	—	V _{IN} = 5V	0.7	—	4.2	V	
	—	V _{IN} = 12V	1.2	—	5.0	V	
Output Power							
P _{OUT}	0.7V	V _{IN} = 5V	0	—	14	W	
	1.0V				20		
	1.2V				24		
	1.5V				30		
	2.0V	V _{IN} = 5V or 12V			40		
	2.5V				50		
	3.3V				50		
	5.0V				V _{IN} = 12V		50
Output Current							
I _{OUT}	All	Output Power Limited to 50W maximum	0	—	20	A	
Output Voltage, Line Regulation, Remote Sense Connected							
VR _{LINE}	All	V _{IN} = 5V to 12V	—	—	0.75	% V _{out}	
Output Voltage, Load Regulation, Remote Sense Connected							
VR _{LOAD}	All	No Load to Full Load	—	—	0.75	% V _{out}	
Output Voltage Ripple, Note 2							
V _{RIP}	0.7V–1.5V	V _{IN} = 5V, I _{OUT} = 20A	—	15	—	mVp-p	
	1.8V–2.5V						
	3.3V	V _{IN} = 5V, I _{OUT} = 15A					30
	1.2V–2.5V	V _{IN} = 12V, I _{OUT} = 20A					25
	3.3V	V _{IN} = 12V, I _{OUT} = 15A					65
	5.0V	V _{IN} = 12V, I _{OUT} = 10A					80
Transient Load Response, Note 2							
T _{TLD}	All	V _{IN} = 5V, V _{IN} = 12V	—	40	—	uSec	

Electrical Parameters (continued)									
Parameter	Output	Conditions	Min	Nom	Max	Units			
V _{TLN}	0.7V	V _{IN} = 5V, I _{OUT} = 50% to 100% Load	—	25	—	mVpk			
	2.5V			60					
	3.3V			60					
	1.2V	V _{IN} = 12V, I _{OUT} = 50% TO 100% Load		55					
	3.3V			70					
	5.0V			70					
Turn-on Response: Overshoot, Notes 2 and 3									
V _{OS}	All	0% to 100% rated load	—	0	10	mV			
Turn-on Response: Turn-on Delay, Note 2 and 3									
T _{DLY}	All	Maximum Load	—	8.5	10	mSec			
Efficiency									
E _{FF}	0.7V	V _{IN} = 5V, I _{OUT} = 20A	—	82	—	%			
	0.8V			83					
	1.0V	V _{IN} = 5V, I _{OUT} = 20A V _{IN} = 12V, I _{OUT} = 20A	—	86 84	—				
	1.2V			89 87					
	1.8V			91 89					
	2.5V			93 91					
	3.3V			V _{IN} = 5V, I _{OUT} = 15A V _{IN} = 12V, I _{OUT} = 15A			—	95 93	—
	5.0V			V _{IN} = 12V, I _{OUT} = 10A			—	93	—
	Enable Input, Note 1								
ON Threshold	—	—	1.74	1.8	—	V			
OFF Threshold	—	—	—	1.0	1.2				
Switching Frequency									
F _S	—	—	375	—	425	kHz			
Output Overvoltage Protection, Note 1									
V _{OV} P	—	Relative to output voltage	110	115	120	%			
Output Undervoltage Protection, Note 1									
V _{UV} P	—	Relative to output voltage	80	85	90	%			
General									
Capacitive Load	—	—	330	—	5000	uF			
Mass	—	—	—	—	25	g			
MTBF	—	MIL-HDBK-217F2, S _F , 35 °C	—	2.13×10 ⁶	—	hrs			

Notes:

1. Parameter not 100% tested an only assured by design
2. Tested and verified using a 20 kHz to 20 MHz bandwidth. Measured across tantalum capacitor load (3 ea. T530X337M010AHE004) on test fixture.
3. Turn-on delay time from either a step application of input power or a logic low to a logic high transition on the Enable pin to the point where V_{OUT} = 90% of nominal

4.1. Radiation Specification (Note 1)

Environment	Conditions	Min	Unit
TID (gamma)	MIL-STD-883, method 1019 Bias applied during exposure	50	krad(Si)
SEE SEU, SEL, SEGR, SEB	Heavy ions [LET] Bias applied during exposure	43	MeV·cm ² /mg

Note:

1. The “-T” configuration incorporates GaN FET technology providing a >43 MeV·cm²/mg SEE capability to the design

5. Typical Performance Curves

Figure 5-1. POL-05-20S Efficiency $V_{IN} = 5V$

(Typical: +25°C, Bias = 5V, 990 μF external output capacitance)

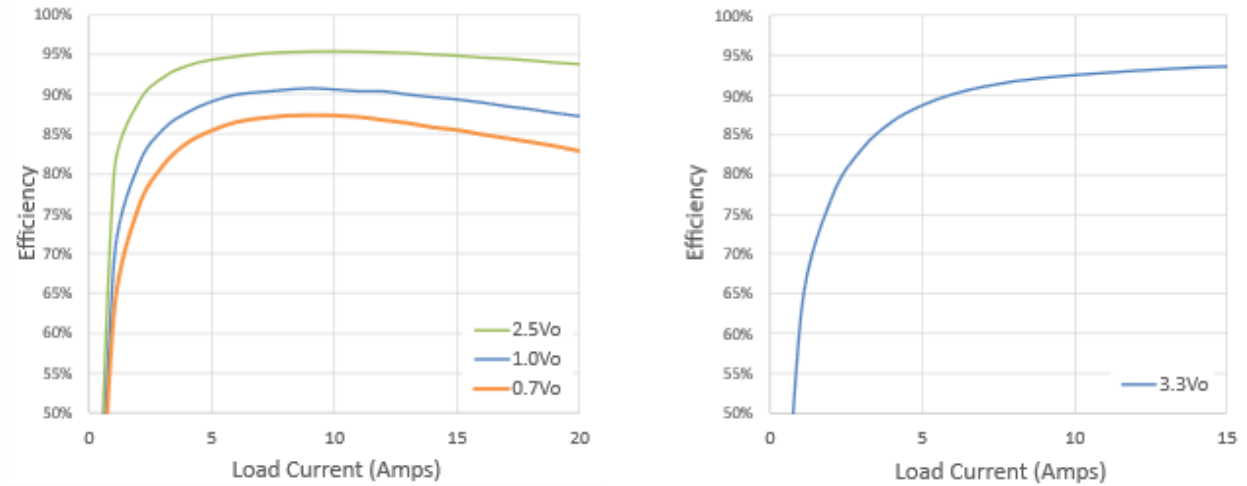


Figure 5-2. POL-05-20S Efficiency $V_{IN} = 5V$ vs Temperature
(Typical: Bias = 5V, 990 μF external output capacitance)

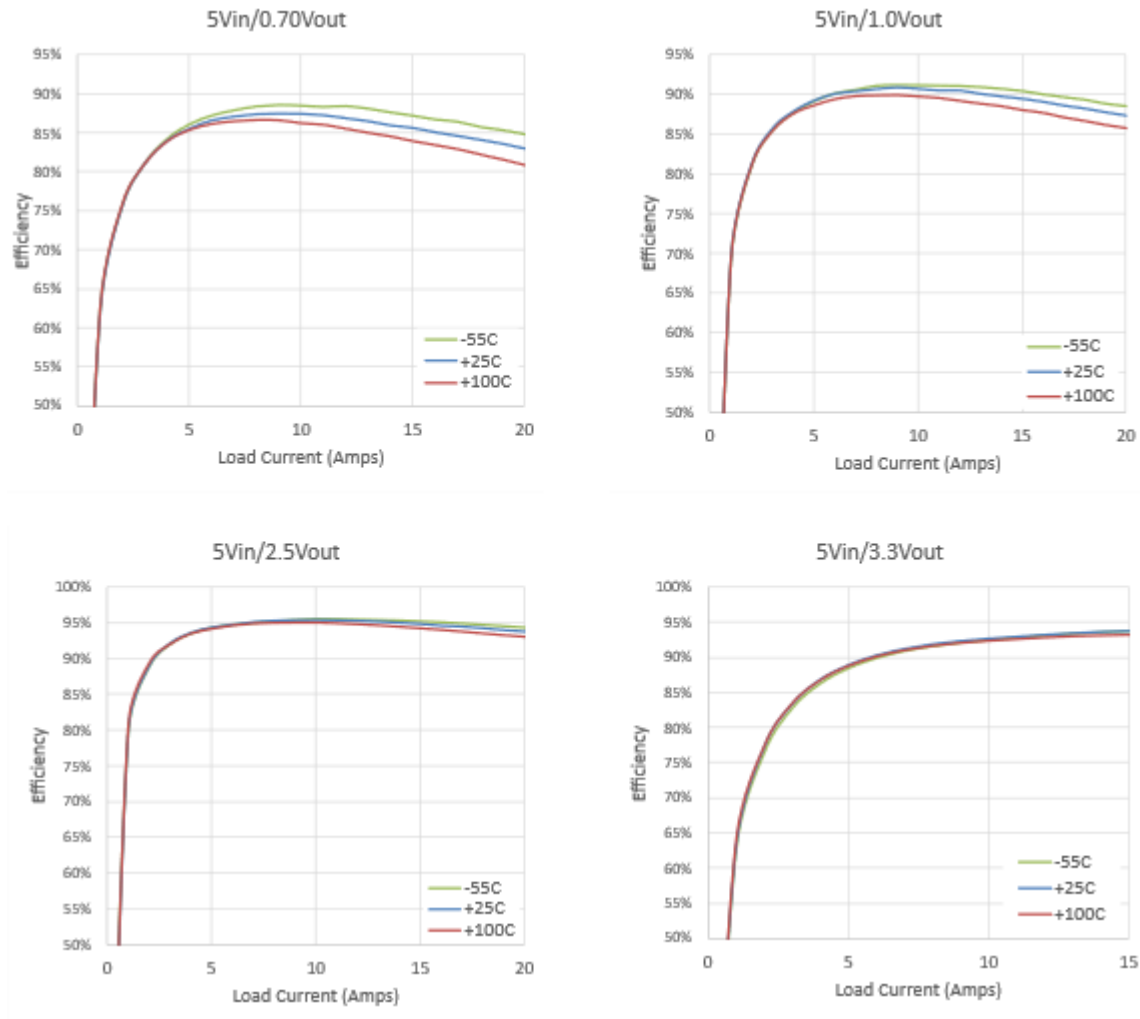


Figure 5-3. POL-05-20S Efficiency $V_{IN} = 12V$
(Typical: $+25^{\circ}C$, Bias = 12V, 990 μF external output capacitance)

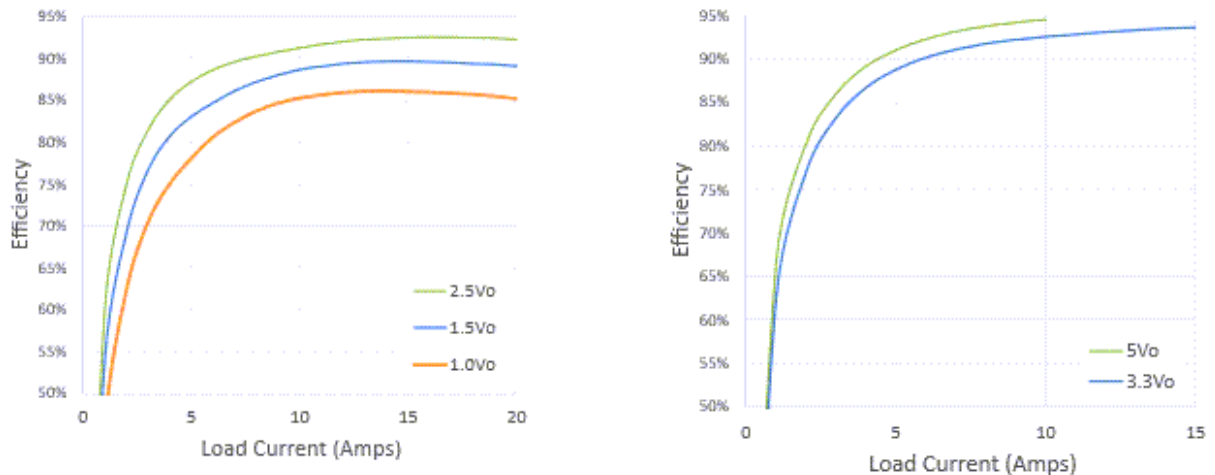


Figure 5-4. POL-05-20S Efficiency $V_{IN} = 12V$ vs Temperature
 (Typical: Bias = 12V, 990 μF external output capacitance)

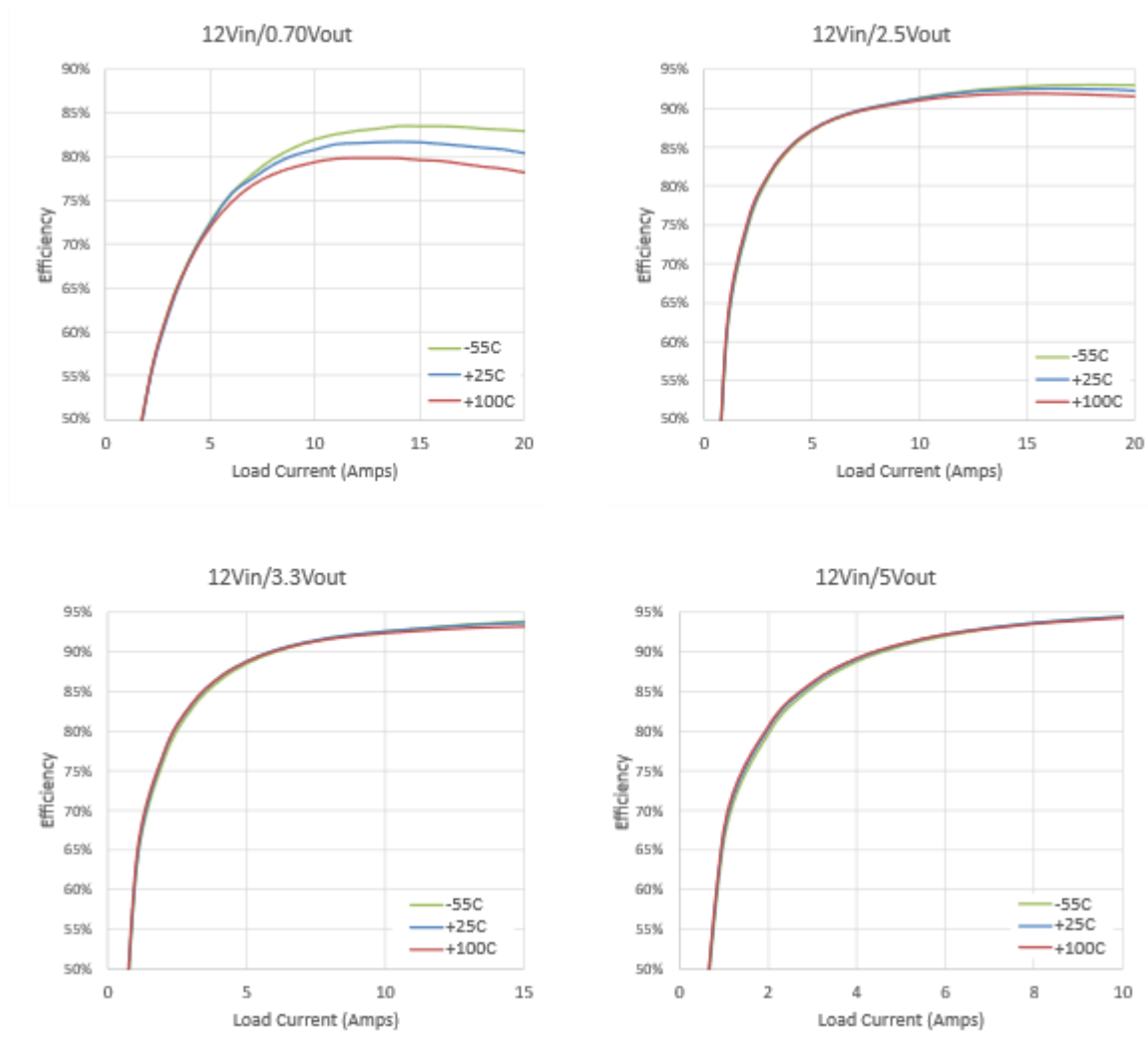


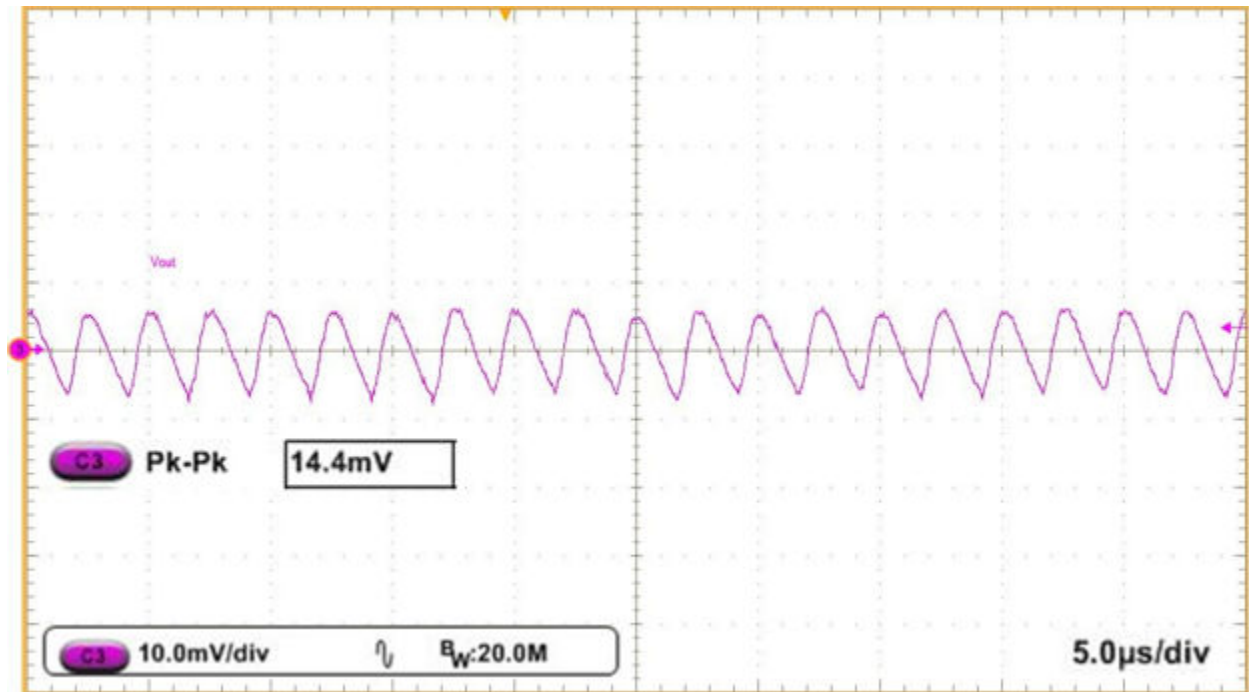
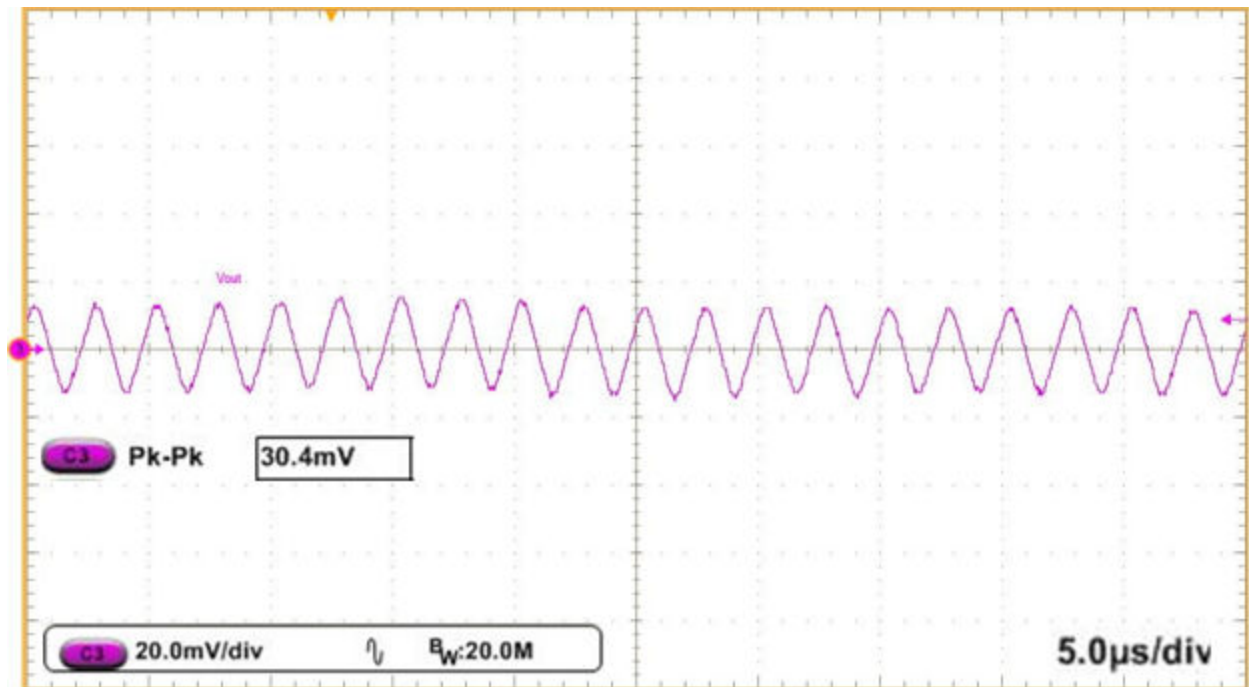
Figure 5-5. Typical Output Ripple at $V_{IN} = 5V$, $V_{OUT} = 0.7V$ *(Bias = 5V, $I_{OUT} = 20A$, 3* 330 uF external tantalum capacitors)***Figure 5-6.** Typical Output Ripple at $V_{IN} = 5V$, $V_{OUT} = 2.5V$ *(Bias = 5V, $I_{OUT} = 20A$, 3* 330 uF external tant output caps)*

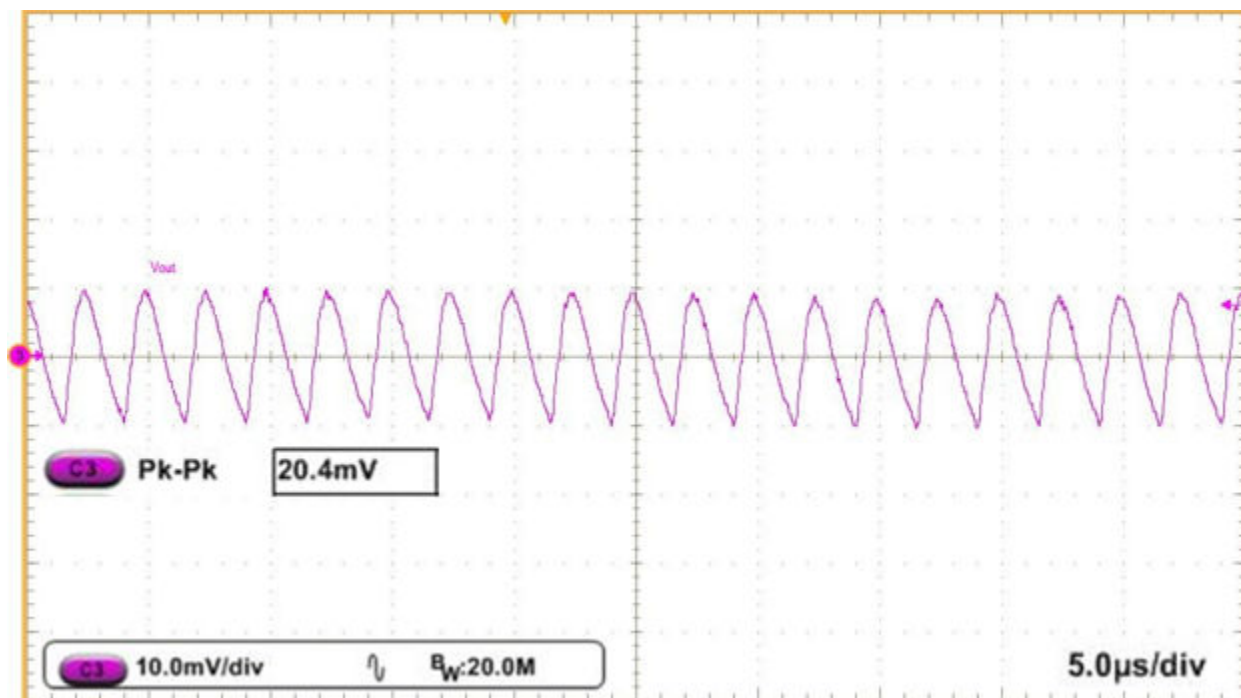
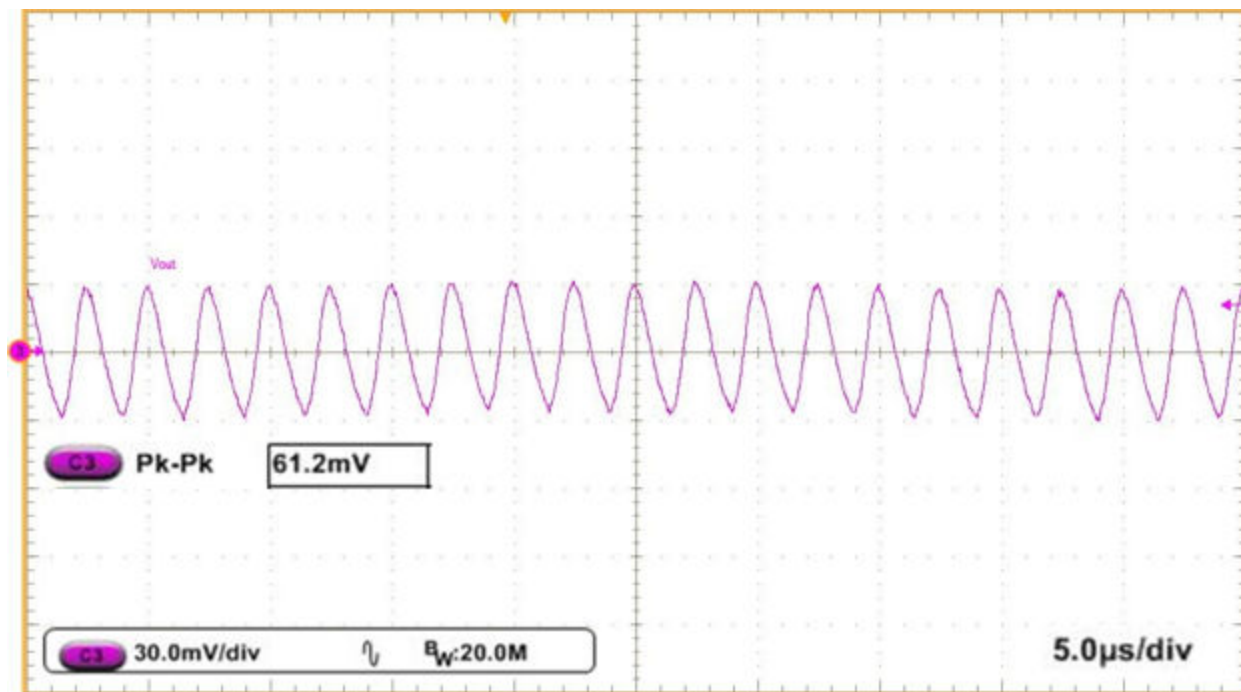
Figure 5-7. Typical Output Ripple at $V_{IN} = 12V$, $V_{OUT} = 1.2V$ *(Bias = 12V, $I_{OUT} = 20A$, 3*330 μF external tantalum capacitors)***Figure 5-8.** Typical Output Ripple at $V_{IN} = 12V$, $V_{OUT} = 3.3V$ *(Bias = 12V, $I_{OUT} = 15A$, 3* 330 μF external tant output caps)*

Figure 5-9. Step Load Transient Response at $V_{IN} = 5V$, $V_{OUT} = 0.7V$ Output
 (Bias = 5V, $I_{OUT} = 10A-20A$ (1 A/us), 3* 330 uF external tant output caps)

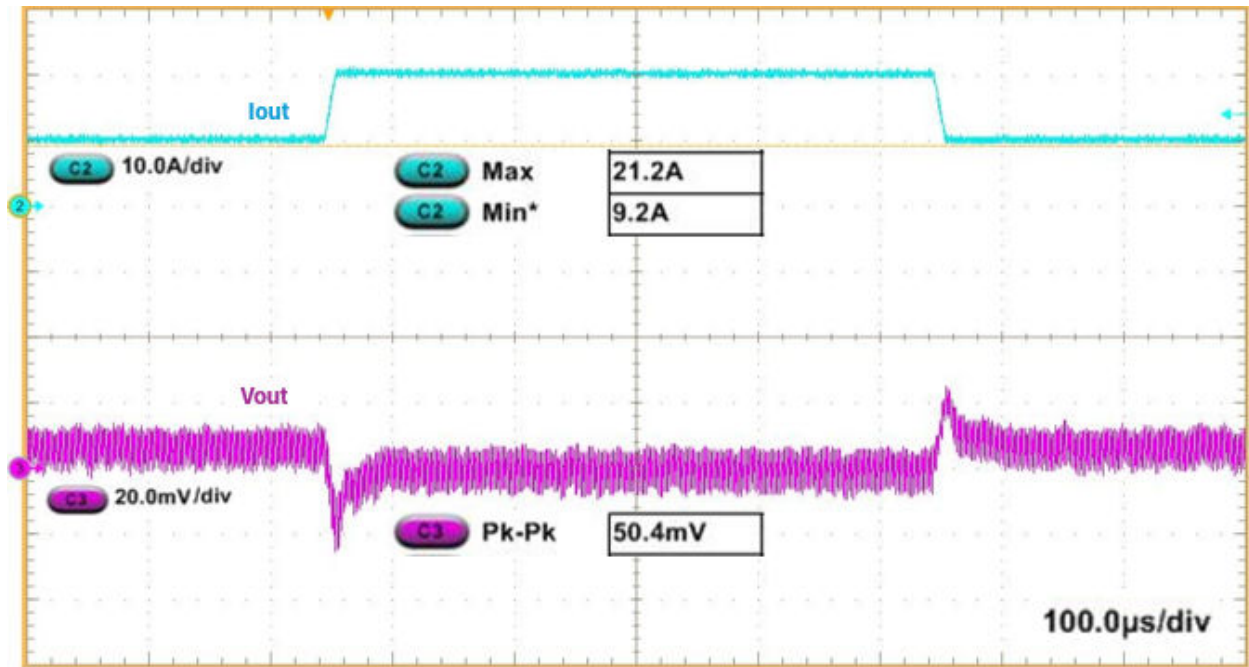


Figure 5-10. Step Load Transient Response at $V_{IN} = 5V$, $V_{OUT} = 2.5V$ Output
 (Bias = 5V, $I_{OUT} = 10A-20A-10A$ (1 A/us), 3* 330 uF external tant output caps)



Figure 5-11. Step Load Transient Response at $V_{IN} = 12V$, $V_{OUT} = 1.2V$ Output
 (Bias = 12V, $I_{OUT} = 10A-20A-10A$ (1 A/us), 3*330 uF external tant output caps)

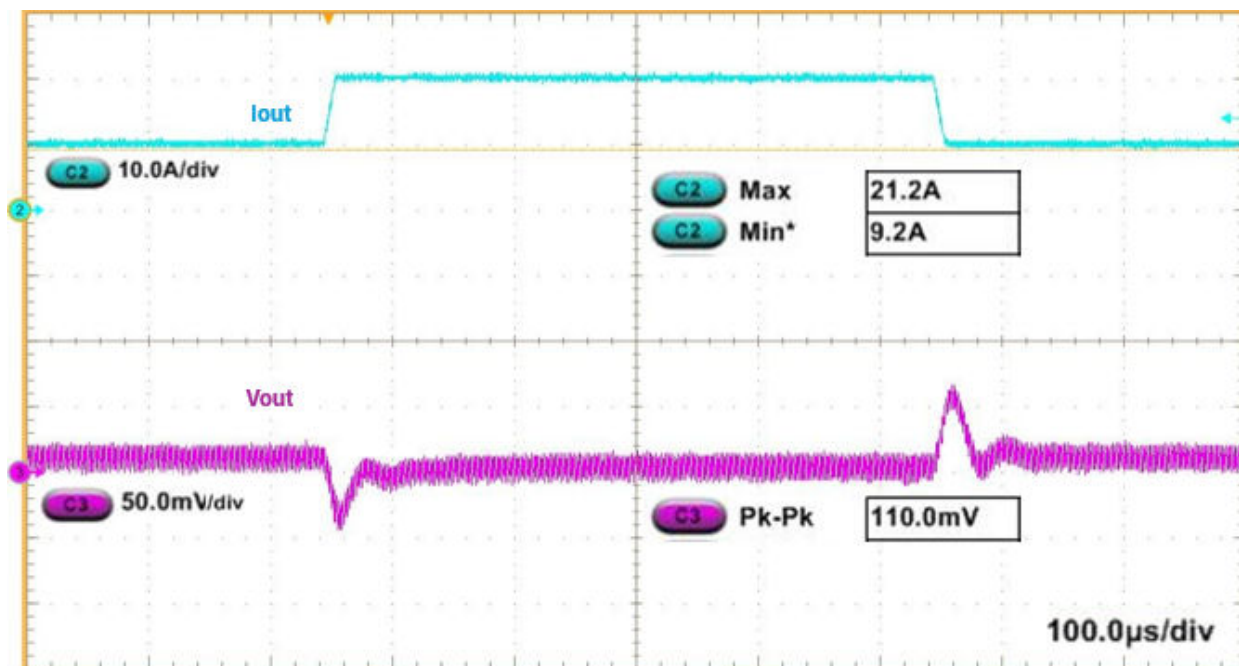


Figure 5-12. Step Load Transient Response at $V_{IN} = 12V$, $V_{OUT} = 3.3V$ Output
 (Bias = 12V, $I_{OUT} = 7.5A-15A-7.5A$ (1A/us), 3*330 uF external tant output caps)

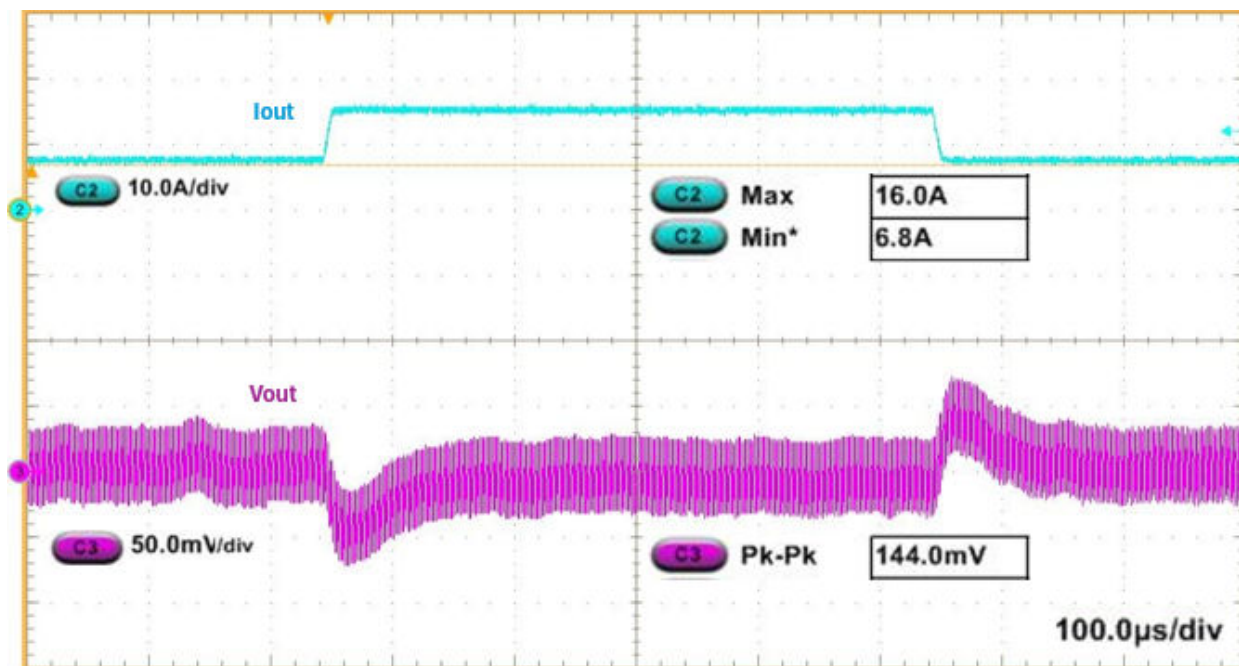


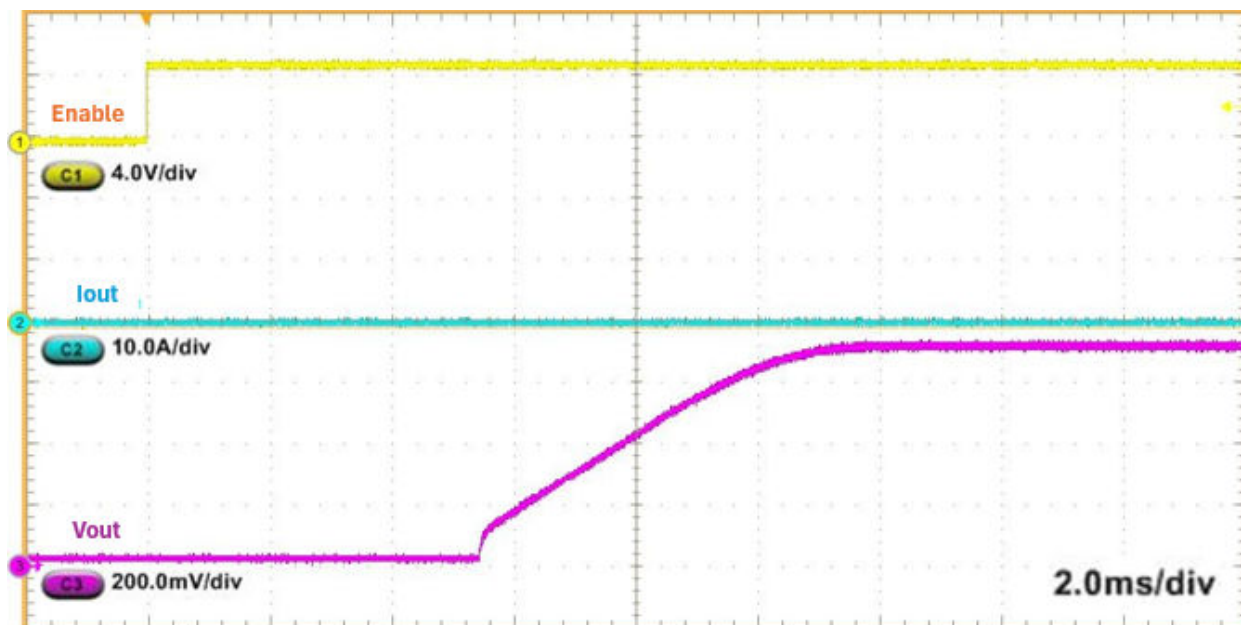
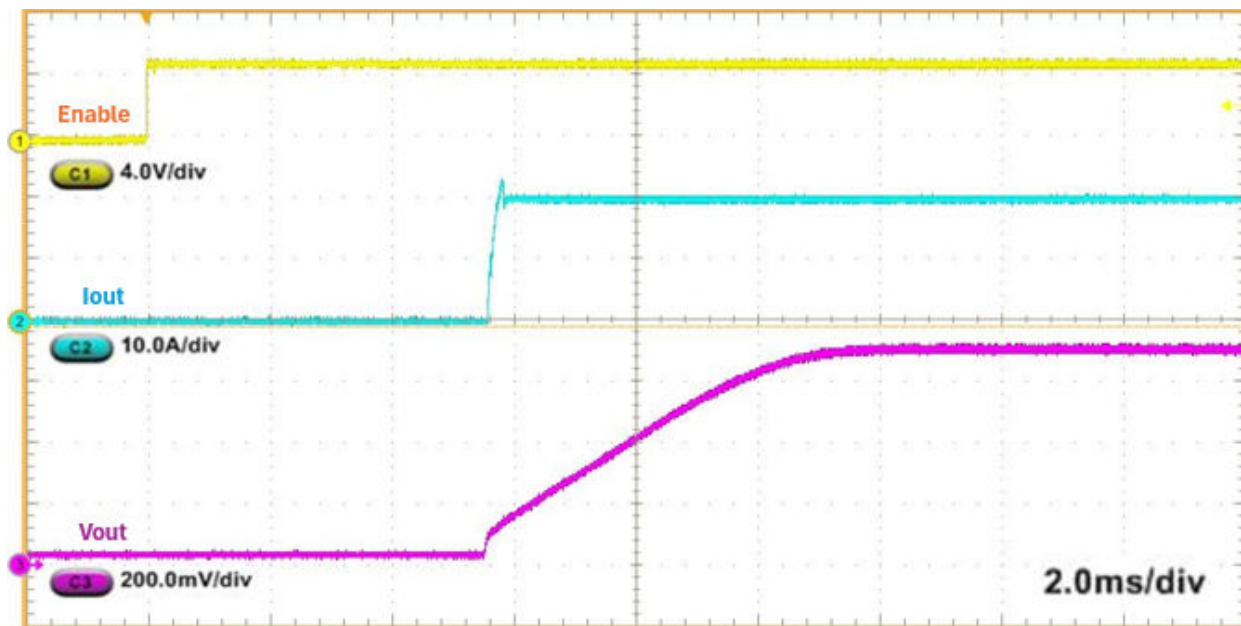
Figure 5-13. Startup by Enable, No Load, $V_{IN} = 5V$, $V_{OUT} = 0.7V$ *(Typical, 3*330 μF external tant output caps)***Figure 5-14.** Startup by Enable, 20A Load, $V_{IN} = 5V$, $V_{OUT} = 0.7V$ *(Typical, 3*330 μF external tant output caps)*

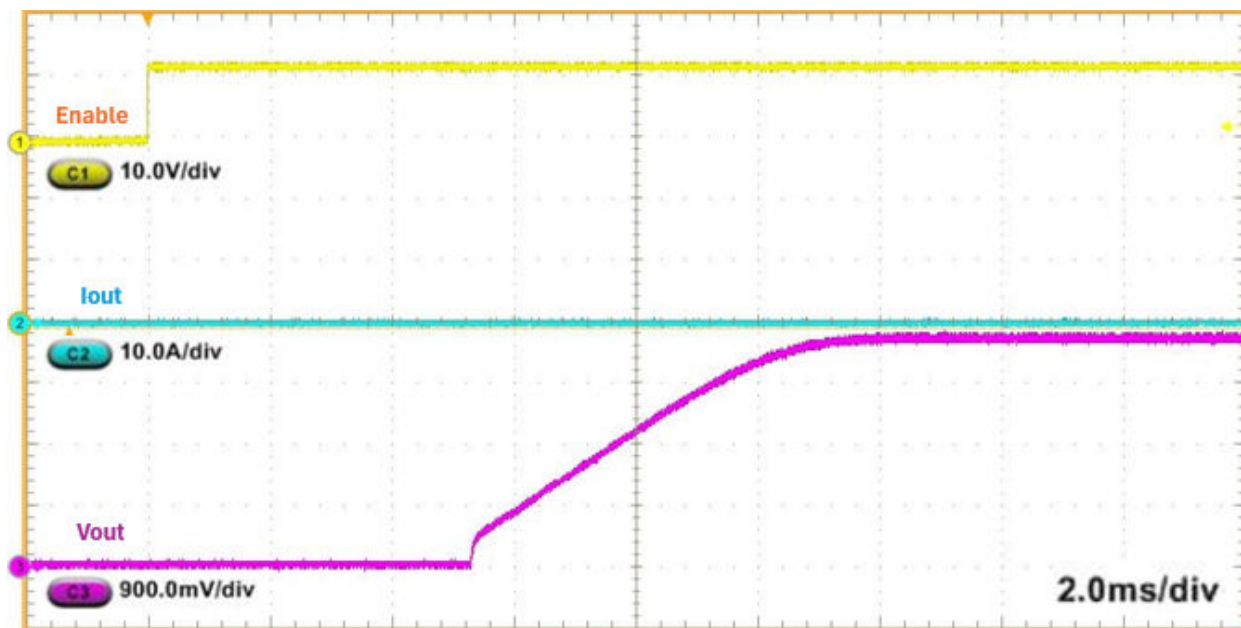
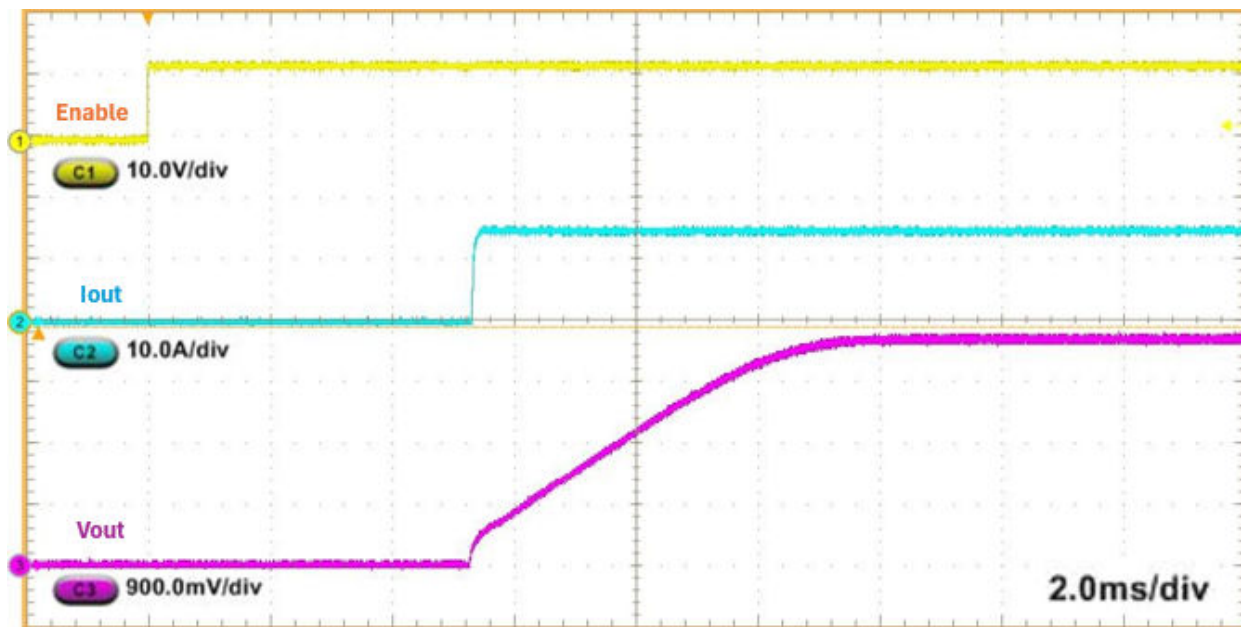
Figure 5-15. Startup by Enable, No Load, $V_{IN} = 12V$, $V_{OUT} = 3.3V$ *(Typical, 3*330 μF external tant output caps)***Figure 5-16.** Startup by Enable, 15A Load, $V_{IN} = 12V$, $V_{OUT} = 3.3V$ *(Typical, 3*330 μF external tant output caps)*

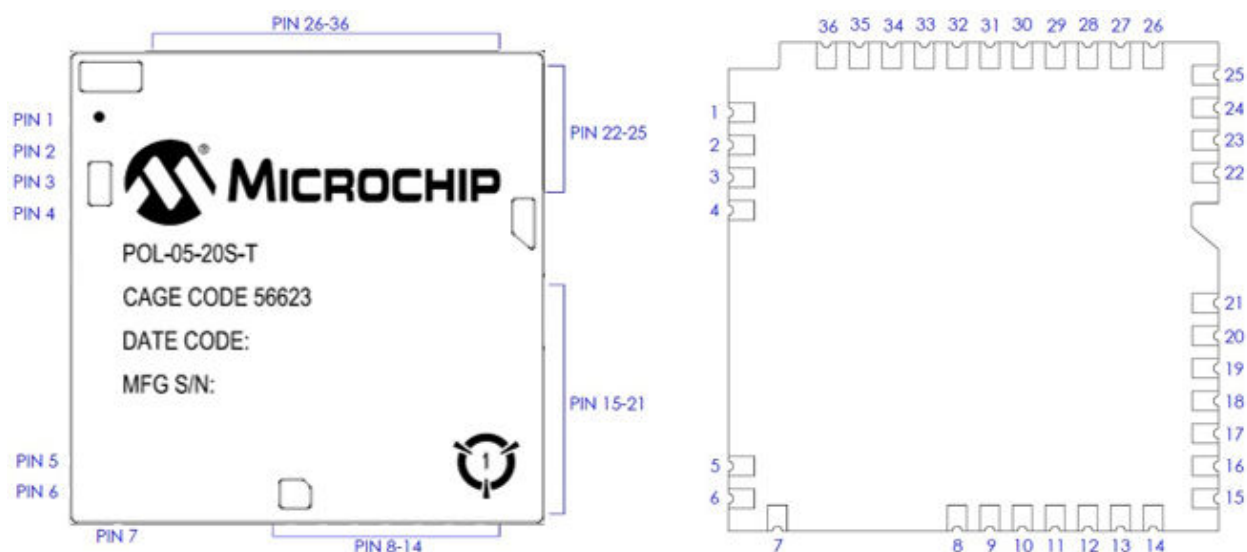
Figure 5-17. Stability Measurement: (Phase/Gain) Margin = 68 deg/22.5 dB, Cross-Over = 57 KHz

$V_{in} = 5V$, $V_{OUT} = 0.7V$, Load = -1A/5A/10A/15A/20A, 3*330 μF external output cap



6. Pin Configuration

Figure 6-1. Pin Configuration

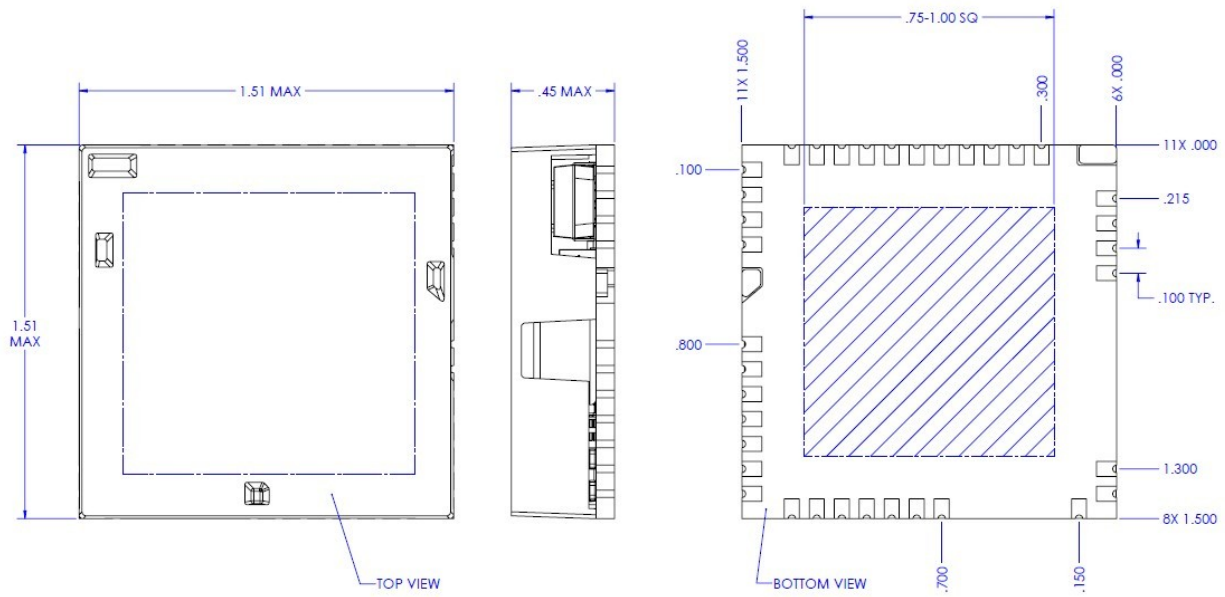


7. Pin Description

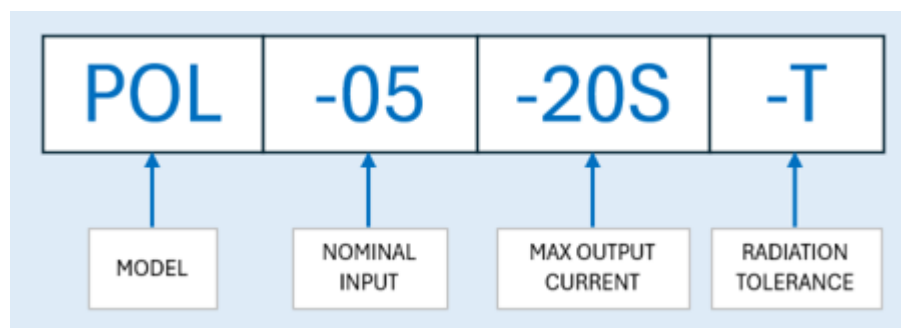
Pin	Name	Description
1	BIAS_RTN	Signal Ground, Bias Return
2	BIAS	Bias Input Voltage, Input supply for the internal circuits
3	PG	Power Good Indicator (Open Drain)
4	ENABLE	Power Supply ENABLE, Active High, Internal pull-down
5	RS_RTN	Remote Sense Return, Connect as close to load terminal (-) as possible
6	ADJ	Remote Adjust Pin to Adjust Output Voltage
7	RS	Remote Sense, Connect as close to load terminal (+) as possible
8-14	PWR GND	Power Ground, Connect to the application power ground plane
15-21	VOUT	Output Voltage
22-25	VIN	Power Input Voltage, Power input for the power switching stage
26-36	GND	Power Ground, Connect to the application power ground plane

8. Mechanical Outline Package

Figure 8-1. Castellated edges (Top, Bottom and Side View, Dimension in inches)



9. Ordering Information



Model	POL	Point of Load	
Nominal Input	-05	5.0V	Nominal Line Input Voltage
Max Output Current	-20	20A	Maximum Output Current (Power Limited)
Radiation Tolerance	-T	Tolerant	Radiation Tolerant. Contact factory for a radiation hardened design.

10. Revision History

Revision	Date	Description
A	09/2026	X3 Preliminary

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