
MTCH 24 Channel Controller

Functional Safety

- UL/IEC 60730 Class B ready
- Self diagnostics at power-on and as periodic tests during operation

MTCH Sensing Technology

- Choice of configurable key arrangements using mutual or self capacitance measurements
- Up to 32 mutual capacitance keys
- Up to 24 self capacitance keys
- Keys can be grouped to form up to 6 sliders or wheels
- Adjacent Key Suppression (AKS) technology is supported for false key touch prevention

Front Panel Material

- A wide variety of non-conductive materials is possible, subject to a high E_r
- Glass up to 6 mm (dependent on screen size, touch size, configuration and stack-up)
- Plastic up to 3 mm (dependent on screen size, touch size, configuration and stack-up)

Touch Performance

- Configurable acquisition schemes for robust and sensitive multi-touch sensing, including:
 - Single-ended Mutual capacitance measurements
 - P2P Mutual Capacitance measurements
 - Single-ended Self Capacitance measurements
 - P2P Self Capacitance measurements
- Noise suppression technology to combat ambient and power-line noise
 - Up to 240 V_{PP} between 1 Hz and 1 kHz sinusoidal waveform (no touches)
 - IEC 61000-4-6, 10 V_{rms}, Class A (normal touch operation) conducted noise immunity
- Touch panel failure detection
 - Automatic touch sensor diagnostics to support the implementation of safety critical features
 - Diagnostics reported using dedicated output pin or by standard Object Protocol messages
 - Configurable test limits

Data Store

- 64-byte data area for user's custom data (not CRC checksummed)

Device Security

- Encrypted configuration parameters and touch coordinate reports (OBP messages) using customer's own security key
- Firmware Authentication mechanism to ensure the authenticity of the application firmware in the device

Power Saving

- Programmable timeout for automatic transition from Active to Idle state
- Pipelined analog sensing detection and digital processing to optimize system power efficiency
- Low power idle mode during which the device detects touches before entering active mode to perform full measurement and touch processing

Application Interface

- I²C client interface for main communication between the system host and the device
 - Standard mode (up to 100 kHz)
 - Fast mode (up to 400 kHz)
 - Fast-mode Plus (up to 1 MHz)
- Interrupt to indicate when a message is available

Power Supply

- Digital (V_{dd}) 3.3V nominal
- Digital I/O (V_{ddIO}) 1.8 to 3.3V nominal

Package

- 38-pin XQFN 4 × 4 × 0.35 mm, 0.35 mm pitch

Operating Temperature

- -40°C to +105°C

Design Services

- Review of device configuration, stack-up and sensor patterns (contact your Microchip representative)
- Specific design and tuning tools available as MTCH Studio plug-ins

MTCH3240P

PIN CONFIGURATION

38-pin XQFN

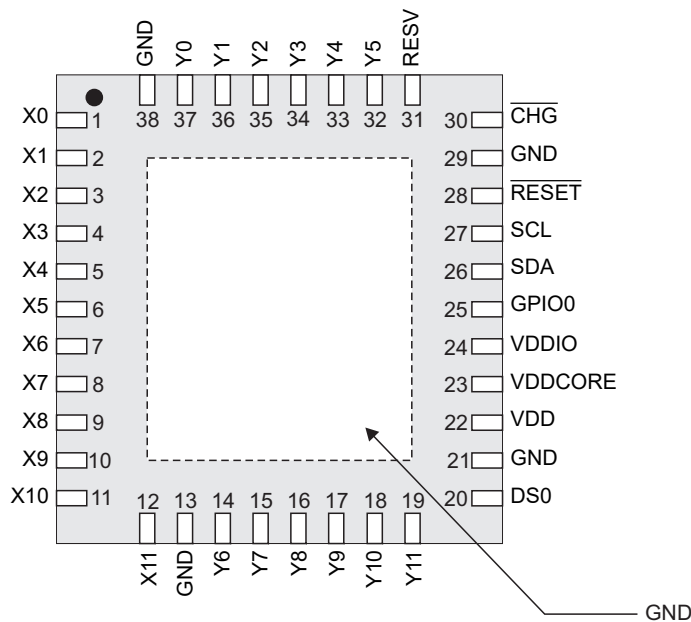


TABLE 1: PIN LISTING – 38-PIN XQFN

Pin	Name	Type	Description	If Unused...
1	X0	S	X line connection	Leave open
2	X1	S	X line connection	Leave open
3	X2	S	X line connection	Leave open
4	X3	S	X line connection	Leave open
5	X4	S	X line connection	Leave open
6	X5	S	X line connection	Leave open
7	X6	S	X line connection	Leave open
8	X7	S	X line connection	Leave open
9	X8	S	X line connection	Leave open
10	X9	S	X line connection	Leave open
11	X10	S	X line connection	Leave open
12	X11	S	X line connection	Leave open
13	GND	P	Ground	—
14	Y6	S	Y line connection	Leave open

TABLE 1: PIN LISTING – 38-PIN XQFN (CONTINUED)

Pin	Name	Type	Description	If Unused...
15	Y7	S	Y line connection	Leave open
16	Y8	S	Y line connection	Leave open
17	Y9	S	Y line connection	Leave open
18	Y10	S	Y line connection	Leave open
19	Y11	S	Y line connection	Leave open
20	DS0	S	Driven Shield signal; used as guard track between X/Y signals and ground	Leave open
21	GND	P	Ground	–
22	VDD	P	Digital and analog power	–
23	VDDCORE	P	Digital core power	–
24	VDDIO	P	Digital IO interface power	–
25	GPIO0	O	General Purpose Output; see Section 2.1.6 “GPIO Pin”	Leave open; configure as output high
26	SDA	OD	I ² C Serial Interface Data	–
27	SCL	OD	I ² C Serial Interface Clock	–
28	$\overline{\text{RESET}}$	I	Reset low. Connection to host system is recommended	Pull up to VddIO
29	GND	P	Ground	–
30	$\overline{\text{CHG}}$	OD	State change interrupt Note: Briefly set (~100 ms) as an input after power-up/reset for diagnostic purposes	Pull up to VddIO
31	RESV	O	Reserved for future use	Leave open
32	Y5	S	Y line connection	Leave open
33	Y4	S	Y line connection	Leave open
34	Y3	S	Y line connection	Leave open
35	Y2	S	Y line connection	Leave open
36	Y1	S	Y line connection	Leave open
37	Y0	S	Y line connection	Leave open
38	GND	P	Ground	–
Pad	GND	P	Exposed pad must be connected to GND	–

Note 1: Use of the GPIO pin is not supported for functional safety purposes under UL/IEC 60730 Class B.

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

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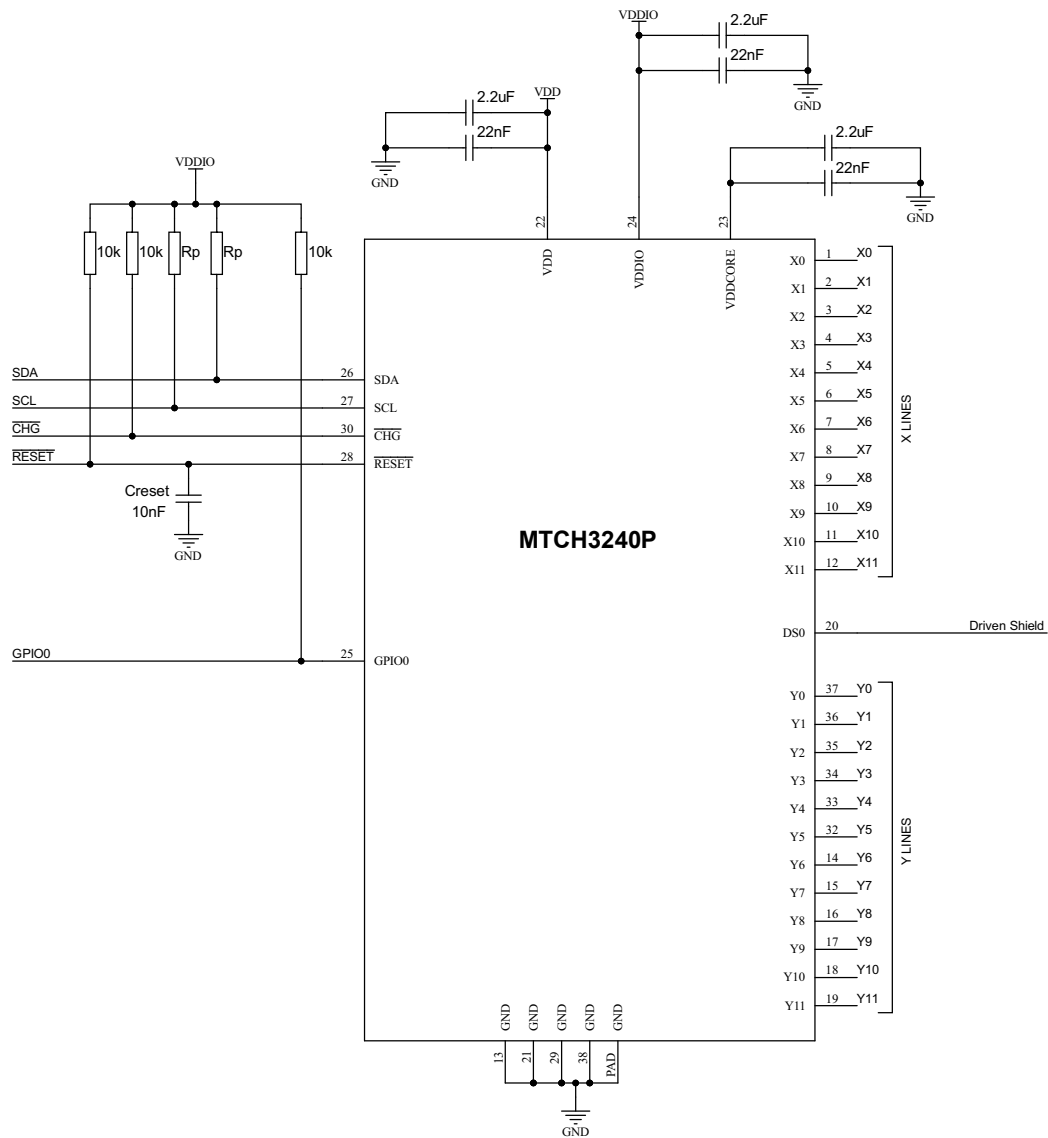
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1.0 OVERVIEW OF MTCH3240P

The Microchip MTCH series of capacitive sensing controllers brings industry-leading capacitive touch performance to customer's button-based capacitive user interfaces. The MTCH3240P features the latest generation of Microchip sensing technology that can be configured to use either a choice of a mutual or self capacitive sensing system in order to deliver unparalleled touch features and a robust user experience.

- **Functional Safety** – The device is designed with functional safety applications in mind (for example, for the home appliance market). Specifically, the device is UL/IEC 60730 Class B ready. See [Section 6.8 “Functional Safety – UL/IEC 60730 Class B Ready”](#) for more information.
- **Patented capacitive sensing method** – The MTCH3240P uses a unique charge-transfer acquisition engine to implement Microchip's patented capacitive sensing method. Coupled with a state-of-the-art CPU, the entire sensor sensing solution can measure, classify and report a number of individual finger touches in the shortest response time even in the presence of electrical noise.
- **Capacitive Touch Engine (CTE)** – The MTCH3240P features an acquisition engine that uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver input lines. The engine includes sufficient dynamic range to cope with anticipated sensor self and mutual capacitances, which allows great flexibility in sensor design, shape and material.
- **Touch detection** – The MTCH3240P allows for either mutual or self capacitance single-ended measurements. Self-capacitive measurements allow operation in the presence of moisture, whereas mutual capacitance measurements allow a larger number of button elements to be configured, and/or a more compact interface design.
- **Noise Cancellation** – A combination of analog circuitry, hardware noise processing, and firmware combats noise without requiring additional listening channels..
- **Noise filtering** – Hardware noise processing in the capacitive touch engine provides enhanced autonomous filtering and allows a broad range of noise profiles to be handled. The result is good performance in the presence of electrical noise.
- **Processing power** – The main CPU has two low-power companion microsequencer coprocessors under its control. This system allows the signal acquisition, preprocessing and postprocessing to be partitioned in an efficient and flexible way.

2.0 SCHEMATIC



See [Section 2.1 "Schematic Notes"](#)

2.1 Schematic Notes

2.1.1 POWER SUPPLY

2.1.1.1 VDDCORE

VddCore is internally generated from the Vdd power supply. To guarantee stability of the internal voltage regulator, one or more external decoupling capacitors are required.

2.1.2 DECOUPLING CAPACITORS

All decoupling capacitors must be X7R or X5R and placed less than 5 mm away from the pins for which they act as bypass capacitors. Pins of the same type can share a capacitor provided no pin is more than 10 mm from the capacitor.

The schematics on the previous pages show the capacitors required. The parallel combination of capacitors is recommended to give high and low frequency filtering, which is beneficial if the voltage regulators are likely to be some distance from the device (for example, if an active tail design is used). Note that this requires that the voltage regulator supplies (Vdd, VddIO) are clean and noise free. It also assumes that the track length between the capacitors and on-board power supplies is less than 50 mm.

The number of base capacitors can be reduced if the pinout configuration means that sharing a bypass capacitor is possible (subject to the distance between the pins satisfying the conditions above and there being no routing difficulties).

2.1.3 PULL-UP RESISTORS

The pull-up resistors shown in the schematic are suggested typical values and may be modified to meet the requirements of an individual customer design.

This applies, in particular, to the pull-up resistors on the I²C SDA and SCL lines (shown on the schematic), as the values of these resistors depend on the voltage and the speed of the I²C interface. See [Section 11.9 "I2C Specification"](#) for the specification of the I²C interface on the MTCH3240P.

Note that if a VddIO supply at the low end of the allowable range is used, the I²C pull-up resistor values may need to be reduced.

2.1.4 $\overline{\text{CHG}}$ LINE

The $\overline{\text{CHG}}$ line is an active-low, open-drain output that is used as an interrupt to alert the system host that an OBP message is pending and ready to be read.

See [Section 7.8 "CHG Line"](#) for more information.

2.1.5 DRIVEN SHIELD LINE

The driven shield line (DS0) should be used to shield the X/Y sense lines. Specifically, the driven shield line acts as a driven shield in self capacitance operation. See [Section 8.4 "Driven Shield Line"](#) for more details.

2.1.6 GPIO PIN

MTCH3240P has one GPIO pin (GPIO0). This pin is an output only pin, and is configured using the GPIO Configuration T19 object.

IMPORTANT! Use of the GPIO0 pin is not considered UL/IEC 60730 Class B ready.
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By default, the GPIO Configuration T19 object configures the GPIO0 pin as an input, so it must be configured as an output pin for use. If the GPIO0 pin is unused, it should be set as an output high using the GPIO Configuration T19 object.

If the GPIO Configuration T19 object is not enabled for use, the GPIO0 pin cannot be used.

3.0 SENSOR BASICS

3.1 Sensor Construction

The physical capacitive user interface is a custom design to suit each application and is constructed from a number of button elements. If desired, these can be logically combined to operate as a group of buttons, or as a slider or wheel.

The enhanced configurability of the MTCH system allows for great flexibility in the size, shape and materials used for making these physical sensing elements. Guidelines for the design of the sensing elements can be found in the following document available from the Microchip website:

- AN2934 – *Capacitive Touch Sensor Design Guide*

See [Section 4.0 “Sensor Layout”](#) for more details on the various configurations of electrodes supported by the device.

3.2 Scanning Sequence

All nodes are scanned in a defined sequence by the device. Where possible, parallelism is used in the scanning sequence to improve overall response time. With mutual capacitance scanning, the nodes are scanned by measuring capacitive changes at the intersections formed between the first drive (X) line and all the receive (Y) lines. Then the intersections between the next drive line and all the receive lines are scanned, and so on, until all X and Y combinations have been measured. With self capacitance scanning, the entire X axis and the entire Y axis are scanned in turn.

The device can be configured in various ways to suit individual application requirements. It is possible to disable unused keys (nodes) so that they are not scanned. Disabling a key disables its processing and may reduce scan time.

3.3 Sensor Sensitivity

3.3.1 ADJUSTMENT

The materials and stack-up used for a sensor affect the overall sensitivity of the design. A global sensitivity adjustment is available to tune the sensor to the correct level of sensitivity.

Individual sensor elements can vary in sensitivity, however, based on the underlying mechanics of the design and the size and shape of each element. The MTCH parts therefore incorporate features to adjust the sensitivity for each sensing node in the design to allow for this.

3.3.2 MECHANICAL STACKUP

The mechanical stack-up refers to the arrangement of material layers that exist above and below a sensor. The arrangement of the sensor in relation to other parts of the mechanical stack-up has an effect on the overall sensitivity of the screen. The MTCH technology has an excellent ability to operate in the presence of ground planes close to the sensor. Front panel dielectric material also has a direct bearing on sensitivity: the thicker the front panel, the lower the signal-to-noise ratio of the measured capacitive changes and hence the lower the sensitivity of the sensor. Glass front panels are preferred as they have higher relative permittivity than most plastics, which improves capacitive coupling, but final performance depends on material grade, thickness, electrode geometry, and stack-up. A wide range of other front panel materials are also usable with MTCH sensors (see AN2934 referenced above for details).

4.0 SENSOR LAYOUT

4.1 Electrodes

The MTCH3240P is designed to operate with a sensor that consists of an array of keys (nodes). The keys are measured using either mutual or self capacitance measurements (but not both), and can be grouped together to form the following:

- **Keys** – Up to 32 mutual capacitance keys, or 24 self capacitance keys, are allowed. The keys can be configured to operate in groups or individually.
- **Sliders or Wheels** – Consecutive keys can be configured to form a slider or wheel. Up to 6 sliders and/or wheels are allowed in addition to any individual keys or groups of keys.

4.1.1 MUTUAL CAPACITANCE KEYS

With mutual capacitance keys, the X and Y lines form a grid with a node at each intersection of an X line with a Y line. The first 32 nodes can then be enabled as keys (each node representing a single key). If the grid contains more than 32 nodes, the additional nodes are not processed.

NOTE Where possible, the grid should contain fewer X than Y lines, as this results in faster measurement scanning. If necessary, the number of nodes can be rounded up to more than 32 nodes to make sure of a more efficient X/Y grid arrangement. For example, 3 X by 11 Y lines (33 nodes) is more efficient than a grid of 4 X by 8 Y (exactly 32 nodes). In this case, the excess node is ignored.

The keys are numbered (that is, assigned key IDs) either along the X lines or along the Y lines, as configured by the Key Array T500 object. This is shown in the following examples. Note that only the first 32 nodes can be used as keys (and are therefore numbered): the excess nodes are ignored.

EXAMPLE 4-1: MUTUAL CAPACITANCE KEYS – NUMBERED BY X LINES

In this example, the keys are formed by a 4 X by 5 Y grid, with the keys numbered along the X lines, as follows:

		Y Lines				
		Y0	Y1	Y2	Y3	Y4
X Lines	X0	Key 0	Key 1	Key 2	Key 3	Key 4
	X1	Key 5	Key 6	Key 7	Key 8	Key 9
	X2	Key 10	Key 11	Key 12	Key 13	Key 14
	X3	Key 15	Key 16	Key 17	Key 18	Key 19

Keys numbered
along X lines →

EXAMPLE 4-2: MUTUAL CAPACITANCE KEYS – NUMBERED BY Y LINES

In this example, the keys are formed by a 4 X by 5 Y grid, with the keys numbered along the Y lines, as follows:

		Y Lines				
		Y0	Y1	Y2	Y3	Y4
X Lines	X0	Key 0	Key 4	Key 8	Key 12	Key 16
	X1	Key 1	Key 5	Key 9	Key 13	Key 17
	X2	Key 2	Key 6	Key 10	Key 14	Key 18
	X3	Key 3	Key 7	Key 11	Key 15	Key 19

↓
Keys
numbered
along Y lines

4.1.2 SELF CAPACITANCE KEYS

With self capacitance keys, each X or Y line forms a key. On the MTCH3240P the maximum number of self capacitance keys that can be defined is 24 (that is, 12 X lines plus 12 Y lines). Note that for P2P self capacitance measurements, some of the X and Y lines must be assigned as reference channels, so this will reduce the number of X and Y lines available for use as keys (see [Section 4.1.2.1 “Reference Channels”](#)).

The keys are numbered (that is, assigned key IDs) either along the X lines followed by the Y lines, or along the Y lines followed by the X lines, as configured by the Key Array T500 object. This is shown in the following examples.

EXAMPLE 4-3: SELF CAPACITANCE KEYS – ARRANGED X LINES + Y LINES

In this example, there are 4 X lines followed by 5 Y lines, with the keys numbered with the X lines first, as follows:

TABLE 4-1: EXAMPLE KEY NUMBERS – SELF CAPACITANCE KEYS 4 X PLUS 5 Y LINES

X Lines				Y Lines				
X0	X1	X2	X3	Y0	Y1	Y2	Y3	Y4
Key 0	Key 1	Key 2	Key 3	Key 4	Key 5	Key 6	Key 7	Key 8

EXAMPLE 4-4: SELF CAPACITANCE KEYS – ARRANGED Y LINES + X LINES

In this example, there are 5 Y lines followed by 4 X lines, with the keys numbered with the Y lines first, as follows:

TABLE 4-2: EXAMPLE KEY NUMBERS – SELF CAPACITANCE KEYS 4 X PLUS 5 Y LINES

Y Lines					X Lines			
Y0	Y1	Y2	Y3	Y4	X0	X1	X2	X3
Key 0	Key 1	Key 2	Key 3	Key 4	Key 5	Key 6	Key 7	Key 8

4.1.2.1 Reference Channels

Using P2P self capacitance measurements allows higher gains to be used than with single-ended measurements. P2P measurements therefore require 1 or more reference channels so that a DC level is always present.

On the MTCH3240P 1 reference channel is required for the X lines. Similarly, 1 reference channel is required for the Y lines. The reference channels are assigned to the line following the last X or Y line, as appropriate, as shown in [Table 4-6 on page 14](#) and [Table 4-7 on page 14](#).

The MTCH3240P automatically considers the last line at the end of each X/Y axis as a reference channel (as shown in [Table 4-6 on page 14](#) and [Table 4-7 on page 14](#)), and the other channels are considered as keys. If additional reference channels are required (for example, to meet the required minimum number of X/Y lines), the keys corresponding to those channels must be disabled in the corresponding Key Controller T501 object.

NOTE The automatically assigned reference channels does not count as a key and is therefore not assigned a Key ID. Any other reference channels will occupy valid key channels, however, and must be disabled in the corresponding Key Controller T501 object.

4.2 Key Configurations

The recommended X/Y key configurations are shown in the following tables.

4.2.1 MUTUAL CAPACITANCE KEYS

Rules

- Both X and Y lines must be used. The maximum number of operational keys is 32, although the sensor may be larger than this (see details above).
- For single-ended mutual capacitance:
 - The minimum number of both X and Y lines is 1.
- For P2P mutual capacitance:
 - The minimum number of X lines is 1, and the minimum number of Y lines is 3.
 - The number of Y lines must be a multiple of 4, or a multiple of 4 minus 1.
- Any excess X or Y lines that are not required for use as keys must be disabled in the Key Controller T501 object.

TABLE 4-3: MUTUAL CAPACITANCE

		Number of Y Lines											
		1	2	3	4	5	6	7	8	9	10	11	12
Number of X Lines	12	S	S	S									
	11	S	S	S									
	10	S	S	K	K								
	9	S	S	K	K								
	8	S	S	K	K								
	7	S	S	K	K	K							
	6	S	S	K	K	K	K						
	5	S	S	K	K	K	K	K					
	4	S	S	K	K	K	K	K	K				
	3	S	S	K	K	K	K	K	K	K	K		
	2	S	S	K	K	K	K	K	K	K	K	K	
	1	S	S	K	K	K	K	K	K	K	K	K	K

Number of keys =
X × Y (maximum 32)×

Note: For key numbers, see [Section 4.1.1 "Mutual Capacitance Keys"](#).

Key: K Configuration supported for all mutual capacitance measurements
S Configuration supported for single-ended (non P2P) mutual capacitance measurements only
 Configuration not supported
 Configuration results in more than 32 keys; excess nodes will be ignored by the device.

4.2.2 SELF CAPACITANCE KEYS

4.2.2.1 Single-ended Self Capacitance

Rules

- Keys can be formed using X lines, Y lines, or a combination of both.
- For X lines:
 - If X lines are used (XSIZE > 0) there must be a minimum of 2 X lines.
 - If Self Capacitance Configuration T111 Low Frequency Compensation is enabled, there must be an even number of X lines.
- For Y lines:
 - If Y lines are used (YSIZE > 0) there must be a minimum of 2 Y lines.
 - If Self Capacitance Configuration T111 Low Frequency Compensation is enabled, there must be an even number of Y lines.
- Any allocated X or Y lines that are not required for use as keys must be disabled in the corresponding Key Controller T501 object.

TABLE 4-4: SINGLE-ENDED SELF CAPACITANCE – X LINES

Without Low Frequency Compensation												T500	
Key Assignment to X Line												XSIZE	
	X0	X1	X2	X3	X4	X5	X6	X7	X8	X9	X10	X11	
12	K	K	K	K	K	K	K	K	K	K	K	K	12
11	K	K	K	K	K	K	K	K	K	K	K		11
10	K	K	K	K	K	K	K	K	K	K			10
9	K	K	K	K	K	K	K	K	K				9
8	K	K	K	K	K	K	K	K					8
7	K	K	K	K	K	K	K						7
6	K	K	K	K	K	K							6
5	K	K	K	K	K								5
4	K	K	K	K									4
3	K	K	K										3
2	K	K											2
1	K	M											2

With Low Frequency Compensation												T500	
Key Assignment to X Line												XSIZE	
	X0	X1	X2	X3	X4	X5	X6	X7	X8	X9	X10	X11	
12	K	K	K	K	K	K	K	K	K	K	K	K	12
11	K	K	K	K	K	K	K	K	K	K	K	M	12
10	K	K	K	K	K	K	K	K	K	K	K		10
9	K	K	K	K	K	K	K	K	K	M			10
8	K	K	K	K	K	K	K	K					8
7	K	K	K	K	K	K	K	M					8
6	K	K	K	K	K	K							6
5	K	K	K	K	K	M							6
4	K	K	K	K									4
3	K	K	K	M									4
2	K	K											2
1	K	M											2

Key: K Key allocated to X line
 Configuration not supported.
M Excess lines to meet required number; measured but not allocated to a key. Must be disabled in Key Controller T501

TABLE 4-5: SINGLE-ENDED SELF CAPACITANCE – Y LINES

Without Low Frequency Compensation												T500	
Key Assignment to Y Line												YSIZE	
	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	
12	K	K	K	K	K	K	K	K	K	K	K	K	12
11	K	K	K	K	K	K	K	K	K	K	K		11
10	K	K	K	K	K	K	K	K	K	K			10
9	K	K	K	K	K	K	K	K					9
8	K	K	K	K	K	K	K	K					8
7	K	K	K	K	K	K	K						7
6	K	K	K	K	K	K							6
5	K	K	K	K	K								5
4	K	K	K	K									4
3	K	K	K										3
2	K	K											2
1	K	M											2

With Low Frequency Compensation												T500	
Key Assignment to Y Line												YSIZE	
	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	
12	K	K	K	K	K	K	K	K	K	K	K	K	12
11	K	K	K	K	K	K	K	K	K	K	K	M	12
10	K	K	K	K	K	K	K	K	K	K			10
9	K	K	K	K	K	K	K	K	K	M			10
8	K	K	K	K	K	K	K	K					8
7	K	K	K	K	K	K	K	M					8
6	K	K	K	K	K	K							6
5	K	K	K	K	K	M							6
4	K	K	K	K									4
3	K	K	K	M									4
2	K	K											2
1	K	M											2

Key: K Key allocated to Y line
 Configuration not supported.
M Excess lines to meet required number; measured but not allocated to a key. Must be disabled in Key Controller T501

4.2.2.2 P2P self Capacitance

Rules

- Keys can be formed using X lines, Y lines, or a combination of both.
- For X lines:
 - The minimum number of X lines allowed is 3 (including at least 1 reference channel).
 - If Self Capacitance Configuration T111 Low Frequency Compensation is enabled, there must be an even number of X lines.
 - A minimum of 1 reference channel must be used.

- For Y lines:
 - The minimum number of Y lines allowed is 3 (including at least 1 reference channel).
 - If Self Capacitance Configuration T111 Low Frequency Compensation is enabled, there must be an even number of Y lines.
 - A minimum of 1 reference channel must be used.
- Any allocated X or Y lines that are not required for use as keys must be treated as reference channels and disabled in the corresponding Key Controller T501 object.

TABLE 4-6: P2P SELF CAPACITANCE – X LINES

Without Low Frequency Compensation

Key Assignment to X Line

T500

XSIZE

Number of Keys on X Lines

X0

X1

X2

X3

X4

X5

X6

X7

X8

X9

X10

X11

12

11

10

9

8

7

6

5

4

3

2

1

—

12

11

10

9

8

7

6

5

4

3

3

With Low Frequency Compensation

Key Assignment to X Line

T500

XSIZE

Number of Keys on X Lines

X0

X1

X2

X3

X4

X5

X6

X7

X8

X9

X10

X11

12

11

10

9

8

7

6

5

4

3

2

1

—

12

12

12

10

10

8

8

6

4

4

4

4

Key:

K

R

Key allocated to X line

Reference channel allocated to X line

Excess line to meet required number. Treat as reference channel; must be disabled in Key Controller T501

Configuration not supported.

TABLE 4-7: P2P SELF CAPACITANCE – Y LINES

Without Low Frequency Compensation

Key Assignment to Y Line

Y0

Y1

Y2

Y3

Y4

Y5

Y6

Y7

Y8

Y9

Y10

Y11

T500

YSIZE

Number of Keys on Y Lines

12

11

10

9

8

7

6

5

4

3

2

1

—

12

11

10

9

8

7

6

5

4

3

3

K

R

Key allocated to Y line

Reference channel allocated to Y line

Excess line to meet required number. Treat as reference channel; must be disabled in Key Controller T501

Configuration not supported.

With Low Frequency Compensation

Key Assignment to Y Line

Y0

Y1

Y2

Y3

Y4

Y5

Y6

Y7

Y8

Y9

Y10

Y11

T500

YSIZE

Number of Keys on Y Lines

12

11

10

9

8

7

6

5

4

3

2

1

—

12

12

12

10

10

8

6

6

4

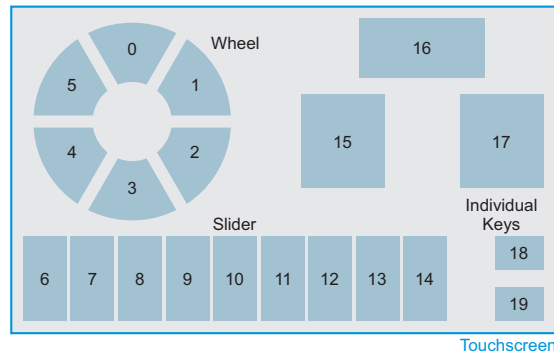
4

4

4.3 Sensor Layout

The mutual or self capacitance keys can be freely assigned to actual keys on the touchscreen. Note that the keys do not need to be arranged in a grid-like pattern, and individual keys can be of different shapes and sizes. Note, however, that this may result in different levels of capacitance (C_m ; see [Section 11.7 “Touch Sensor Characteristics”](#)) as the keys will have the same gain configured in the Key Array T500 object. If necessary, the characteristics of each individual key (such as its touch detection threshold) can be configured using the Key Controller T501 object. An example layout for 20 keys is shown in [Figure 4-1](#).

FIGURE 4-1: KEYS, SLIDERS AND WHEELS – EXAMPLE LAYOUT (20 KEYS)



4.4 Driven Shield Line

The driven shield line (DS0) should be used to shield the X/Y sense lines. See [Section 8.4 “Driven Shield Line”](#) for more details.

5.0 POWER-UP / RESET REQUIREMENTS

5.1 Power Sequencing

The MTCH3240P has a number of power rails, reflecting the power domains internal to the device. Power sequencing should be straightforward if the following rules are followed.

5.1.1 PREREQUISITES

All input signals to the device must be set to 0V (logic low) whenever the device is powered off to avoid “back-powering” the device through the input protection diodes.

Make sure that any lines connected to the device do not exceed the value of VddIO during power-up and power-down.

5.1.2 POWER-UP SEQUENCE

The power rails should be powered on in the following order:

1. Ideally, VddIO should be powered on first (see [Figure 5-1](#)), as the $\overline{\text{RESET}}$ line and $\overline{\text{CHG}}$ line are referenced to this.
2. Vdd should be powered on after, or at the same time as, VddIO.

All rails must adhere to the maximum rate-of-rise specification (see [Section 11.2.1 “DC Characteristics”](#)).

5.1.3 POWER-DOWN SEQUENCE

Powering off the chip is essentially the reverse of power-up. Again, all input signals to the device must be set to 0V (logic low) before power is removed from the device. All rails must adhere to the maximum rate-of-fall specification (see [Section 11.2.1 “DC Characteristics”](#)).

5.1.4 POWER REGULATORS

One or more power rails may be derived from the same LDO, in which case the power rails will power up and down together:

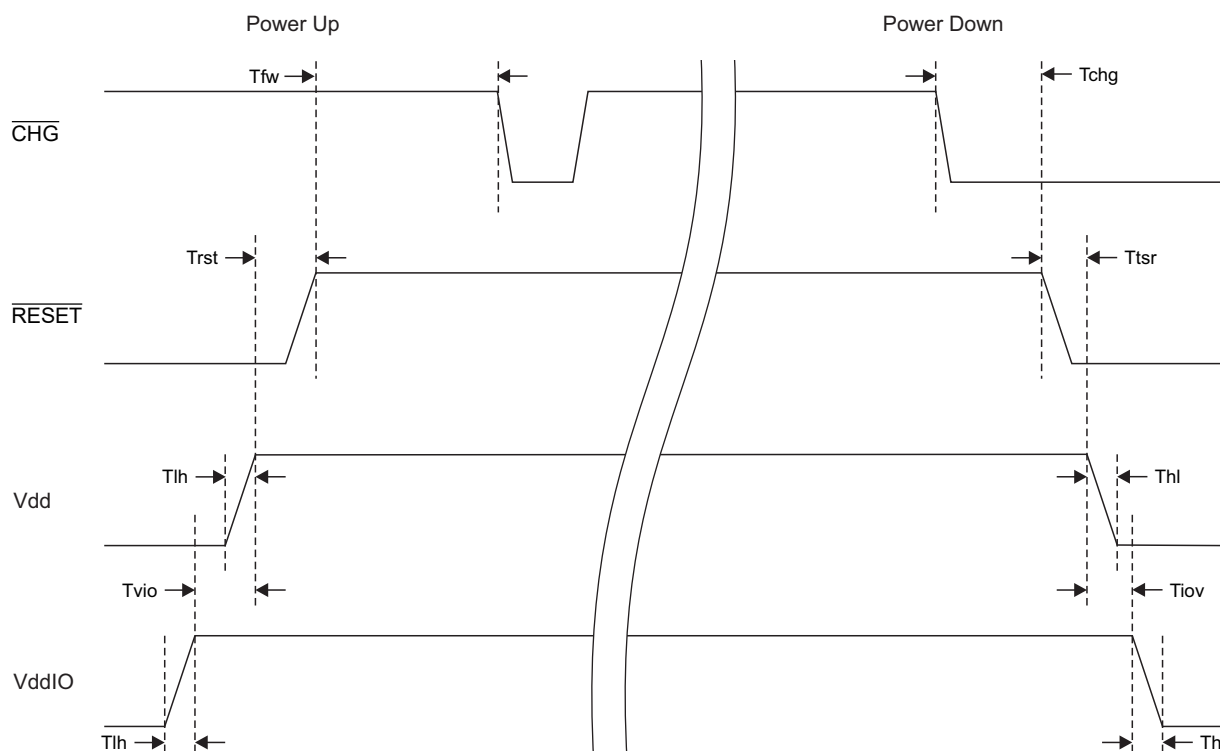
- The Vdd and VddIO rails can be shared.

If a design requires separate power rails, contact your Microchip representative for help and advice.

5.1.5 SUMMARY OF POWER SEQUENCES

[Figure 5-1](#) summarizes the power-on and power-off sequences.

FIGURE 5-1: POWER SEQUENCES



Parameter	Description	Value
Tlh	Supply Rise Rate	See Section 11.2.1 "DC Characteristics"
Tvio	VddIO to Vdd rise delay	0 ns to 10 ms
Trst	Last power rail rise to Reset	≥ 90 ns
Tfw	Reset to CHG line toggled.	Depends on configuration; see Section 11.6.2 "Reset Timings"
Tchg	CHG line to Reset asserted	Controlled by MTCH device
Ttsr	Reset asserted to first power rail fall	≥ 0 ns
Thl	Supply Fall Rate	See Section 11.2.1 "DC Characteristics"
Tiov	Vdd to VddIO fall delay	≥ 0 ns

5.2 Power-on Reset

5.2.1 INTERNAL RESET

The MTCH3240P includes a Power-on Reset (POR) function in the device. This will reset the device on the rising edge of the Vdd supply. When using this feature, the following applies:

- VddIO should either share the Vdd supply, or must be powered on before Vdd.
- The RESET pin should be pulled high to VddIO by a resistor.

The POR function will also perform a reset in the event of a power brown-out during operation.

At power-on, the device can be configured to perform self tests (using the Self Test Control T10 object) to check for faults in the device.

MTCH3240P

5.2.2 EXTERNAL RESET

It is recommended that the MTCH3240P is controlled by a $\overline{\text{RESET}}$ line from the system host, as this gives the system host full control over the timing and power state of the device. To avoid back-powering problems, the $\overline{\text{RESET}}$ line must be driven low (logic 0) whenever power is not supplied to the device. The $\overline{\text{RESET}}$ line must be held low for at least 90 ns after both the Vdd and VddIO device power supplies have reached their nominal values.

NOTE The voltage level on the $\overline{\text{RESET}}$ pin must never exceed the VddIO supply voltage.

5.3 Initialization

After power-up, the device typically takes 120 ms to 340 ms before it is ready to start scanning, depending on the configuration. The device indicates that initialization is complete by asserting the CHG line low (see [Section 5.5 "CHG Line Operation"](#)).

NOTE Device initialization will not complete until after all the power supplies are present. If any power supply is not present, internal initialization stalls and the device will not communicate with the host.

In addition, the MTCH3240P incorporates brown-out detector circuits (BODs) to initialize the device correctly once the power rails reach valid values. If the BOD initialization fails, the device will reset itself.

5.4 Reset During Operation

5.4.1 HARDWARE RESET

The hardware $\overline{\text{RESET}}$ pin can be used to reset the device during operation whenever the system host considers it necessary. It is recommended to connect the $\overline{\text{RESET}}$ pin to a host controller to allow the host to initiate a full hardware reset without requiring the MTCH3240P to be powered down.

The $\overline{\text{RESET}}$ pin must be asserted low for a minimum of 90 ns to cause a reset. Following a hardware reset, the device typically takes 120 ms to 360 ms before it restarts scanning, depending on the configuration.

WARNING The device should be reset only by using the $\overline{\text{RESET}}$ line. If an attempt is made to reset by removing the power from the device without also sending the signal lines low, power will be drawn from the communication and I/O lines and the device will not reset correctly.

NOTE The voltage level on the $\overline{\text{RESET}}$ pin of the device must never exceed VddIO (digital supply voltage).

5.4.2 SOFTWARE RESET

The host can issue a software reset command using the Command Processor T6 object at any time in order to reset the device. The device typically takes 140 ms to 380 ms before it restarts scanning, depending on the configuration.

The reset flag is set in the Command Processor T6 object message data to indicate to the host that it has just completed a reset cycle. This bit can be used by the host to detect any unexpected brownout events. This allows the host to take any necessary corrective actions, such as reconfiguration.

5.4.3 RESET INDICATION

After any reset and reinitialization, a Command Processor T6 message is generated by the device. The RESET bit in the Command Processor T6 STATUS message field is set to 1 to indicate that a reset has been performed.

5.5 $\overline{\text{CHG}}$ Line Operation

The $\overline{\text{CHG}}$ line is briefly set as an input during power-up or reset until the device has finished initializing. It is therefore particularly important that the line should be allowed to be pulled high by the $\overline{\text{CHG}}$ line pull-up resistor during this period: it should never be driven by the host.

Once the device has reset, and has completed its initialization, it pulls the $\overline{\text{CHG}}$ line low. This signals to the system host that the Command Processor T6 reset report message is available.

6.0 DETAILED OPERATION

6.1 Touch Detection

The device can be configured to use either mutual or self capacitive measurements. Both of these can be either single-ended or P2P (differential) measurements. The choice of measurement type depends on a number of design choices for any given system, for example:

- How many button elements are required
- How much water and noise robustness is required
- Whether the use of the low power mode is required
- Whether the component count should be minimized

For more assistance, please contact your Microchip representative.

6.2 Operational Modes

The device operates in two modes: **Active** (touch detected) and **Idle** (no touches detected). Both modes operate as a series of burst cycles. Each cycle consists of a short burst (during which measurements are taken) followed by an inactive sleep period. The difference between these modes is the length of the cycles. Those in idle mode typically have longer sleep periods. The cycle length is configured using the IDLEACQINT and ACTVACQINT settings in the Power Configuration T7. In addition, an Active to Idle Timeout setting is provided.

6.3 Low Power Mode

Low Power mode (Low Power Idle Configuration T126) provides the lowest power consumption whilst still maintaining touch detection capability by optimizing the power consumed by different parts of the device. A low power self capacitance scan is used to check for touch detections. When a touch is detected, the device comes out of Low Power mode and single-ended or P2P self capacitance measurements (as selected in Key Array T500) are performed.

NOTE	Low Power Idle mode is supported on the Y lines only. Therefore, when in Low Power Idle mode, only a key detection on a Y line will wake the device: key detections on the X lines have no effect. Once the device is in active mode, it will remain in that mode until the Active to Idle Timeout expires after the last touch is released. Key detection on the X lines will, however, operate as normal when the device is in active mode.
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6.4 Detection Integrator

The device features a touch detection integration mechanism. This acts to confirm a detection in a robust fashion. A counter is incremented each time a touch has exceeded its threshold and has remained above the threshold for the current acquisition. When this counter reaches a preset limit the sensor is finally declared to be touched. If, on any acquisition, the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

The detection integrator is configured using the appropriate touch object (Key Array T500).

6.5 Sensor Acquisition

The charge time for mutual capacitance measurements is set using the Acquisition Configuration T8 object. The device combines a number of factors together to arrive at the total acquisition time for one drive line (that is, one X line for mutual capacitance acquisitions or one axis for self capacitance acquisitions).

The following constraints apply on the MTCH3240P:

- The per X line mutual capacitance touch measurement and the per axis self capacitance measurement should not exceed 2 ms. Furthermore, the total acquisition time for the sensor as a whole must not exceed 250 ms. In the event of a timeout, a SIGERR may be reported.
- The high and low pulse periods must not exceed 51.26 μ s each. This means that the maximum possible burst period is 102.46 μ s (that is, a minimum frequency of 9.76 kHz). In addition, the burst period must not be less than 4 μ s (that is, a maximum frequency of 250 kHz).

Unpredictable system behavior might occur if any of the above constraints are not met.

Care should be taken to configure all the objects that can affect the measurement timing (for example, drift and noise measurement interval settings) so that these limits are not exceeded.

6.6 Calibration

Calibration is the process by which a sensor chip assesses the background capacitance on each node. Calibration occurs in a variety of circumstances, for example:

- When determined by the mutual capacitance recalibration process, as controlled by the Acquisition Configuration T8 object
- When determined by the self capacitance recalibration process, as controlled by the Self Capacitance Configuration T111 object
- Following a Self Capacitance Global Configuration T109 Tune command
- When the host issues a recalibrate command
- When certain configuration settings are changed

6.7 Digital Filtering and Noise Suppression

The MTCH3240P supports on-chip filtering of the acquisition data received from the sensor. Specifically, the Noise Suppression T72 object provides an algorithm to suppress the effects of noise (for example, from a noisy charger plugged into the user's product). This algorithm can automatically adjust some of the acquisition parameters during operation to filter the Analog-to-Digital Conversions (ADCs) received from the sensor.

NOTE	This functionality has an effect only if mutual capacitance (P2P or single-ended) or P2P self capacitance measurements are selected for use. Noise suppression cannot be used with single-ended self capacitance measurements.
-------------	--

Noise suppression is triggered when a noise source is detected.

- The host driver code can indicate when a noise source is present.
- The noise suppression is also triggered based on the noise levels detected using internal line measurements. The Noise Suppression T72 object selects the appropriate controls to suppress the noise present in the system.

6.8 Functional Safety – UL/IEC 60730 Class B Ready

- The device is designed with functional safety applications in mind (for example, for the home appliance market). Specifically, the device supports UL/IEC 60730 Class B system certification.
 - User-configurable self diagnostics to detect internal system errors (for example, CPU, memory and system clocks), power, pin fault errors and signal errors for immediate action by the host system (see [Section 10.3 "Self Test"](#)). These tests can be configured to run at power-on/reset and/or as periodic testing during operation.
 - Other built-in automatic system-level tests (for example interrupts, CTE and peripheral I/O)
 - Enhanced communications that includes sequence numbers (timing) and CRC error checking

For more details on the self tests available on the MTCH3240P, see [Section 10.3 "Self Test"](#).

6.9 Display Noise Suppression

Display noise suppression allows the device to overcome display noise simultaneously with external noise. This feature is based on filtering provided by the Lens Bending T65 object (see [Section 6.11 "Lens Bending"](#)).

6.10 Electromagnetic Interference Reduction

The MTCH3240P has the following mechanisms to help reduce Electromagnetic Interference (EMI) and other emissions and ensure that the user's product operates within the desired EMC limits:

- **Configurable Voltage Reference Mode** – Allows for the selection of voltage swing of the self capacitance measurements. This feature is configured by the Self Capacitance Global Configuration T109 object.
- **Input Buffer Power Configuration** – Controls the positive/negative drive strength of the Input Buffer for self capacitance measurements. This feature is configured by the Self Capacitance Global Configuration T109 object.
- **Configurable Input Amplifier Bias** – Controls the Input Amplifier Bias. This feature is configured by the Self Capacitance Global Configuration T109 object.

6.11 Lens Bending

The device supports algorithms to eliminate disturbances from the measured signal.

When the sensor suffers from the screen deformation (lens bending) the signal values acquired by normal procedure are corrupted by the disturbance component (bend). The amount of bend depends on:

- The mechanical and electrical characteristics of the sensor
- The amount and location of the force applied by the user touch to the sensor
- The Lens Bending T65 object measures the bend component and compensates for any distortion caused by the bend.

6.12 Device Encryption

For added security, the MTCH3240P allows for the encryption of important configuration parameters within the device, and for the encryption of messages sent by the device.

The default state of the MTCH3240P is to be unencrypted, which allows the host to interact with the device using the standard Object-based Protocol in the same manner as any other unencrypted MTCH device. However, the host can enable encryption if desired. This uses the AES 128 algorithm (Cipher Block Chaining mode) for the encryption and decryption of data. One or more of the following encryption modes are possible:

- Encrypted configuration read/write
- Encrypted Message Processor T5 messages
- Debug output can be disabled when the device is in an encrypted state

Encryption is requested by downloading the encryption parameters to the Serial Data Command T68 object. Encryption is then activated when the device is next reset. If the device has active encryption, the Variant ID is reported with bit 7 set to 1. This provides a method for the host controller to detect if encryption is in use.

The current encryption status can be read from the device using the Encryption Status T2 object.

NOTE Users are recommended to contact their Microchip representative for additional guidance on using encryption features available on this device.

6.13 Firmware Authentication

The firmware authentication mechanism ensures the authenticity of the application firmware in the device and can help detect tampering. This is of particular use in user products that need to pass Payment Card Industry (PCI) certification. The firmware authentication feature operates as follows:

1. Periodically (for example, once every 24 hours), the system host puts the MTCH3240P device into bootloader mode and then invokes the Firmware Authentication mechanism.
2. The bootloader firmware creates hashed signatures of individual memory blocks, or a segment of memory, as requested by the system host.
3. The bootloader firmware sends the signatures to the system host.

4. The system host compares the hash data against the expected value to ascertain if the firmware code has been tampered with.

7.0 I²C COMMUNICATIONS

Communication between the device and the system host is achieved using the I²C interface.

The I²C interface is used in conjunction with the $\overline{\text{CHG}}$ line. The $\overline{\text{CHG}}$ line going low signifies that a new data packet is available. This provides an interrupt-style interface and allows the device to present data packets when internal changes have occurred. See [Section 7.8 “CHG Line”](#) for more information.

7.1 Encrypted Communications

The default state of the MTCH3240P is to be in an unencrypted state. This allows the system host to interact with the device using the standard Object-based Protocol in the same manner as any other unencrypted MTCH device.

For added security, the system host can request that the data communication between the device and the system host is encrypted using mutually agreed keys. This uses the AES 128 algorithm (Cipher Block Chaining mode) for the encryption and decryption of data. One or more of the following encryption modes are possible:

- Encrypted configuration read/write – If enabled, all objects with an address above the User Data T38 object require read/write transactions to be encrypted.
- Encrypted Message Processor T5 messages – If enabled, all messages are sent from the device in encrypted format.
- All debug output disabled – When encryption is enabled, all debug data output can be disabled for additional security.

A customer key is required to encrypt or decrypt configuration settings and messages.

NOTE	Users are recommended to contact their Microchip representative for additional guidance on using encryption features available on this device.
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7.2 I²C Address

The MTCH3240P supports one fixed 7-bit I²C device address: 0x3A.

The I²C address is shifted left by one bit to form the SLA+W or SLA+R address when transmitted over the I²C interface, as shown in [Table 7-1](#).

TABLE 7-1: FORMAT OF SLA+W/SLA+R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0x3A							Read/write

7.3 Writing To the Device

An I²C WRITE cycle consists of the following bytes:

START	1 bit	I ² C START condition
SLA+W	1 byte	I ² C address of the device (see Section 7.2 “I²C Address”)
Address (LSByte, MSByte)	2 bytes	Address of the location at which the data writing starts. This address is stored as the address pointer.
Embedded Data Size (only if encryption is active)	2 bytes	If writing to an encrypted object, the size of the embedded data to be written, including the data CRC (if requested), but excluding any padding bytes; that is, these bytes specify the actual data size and not the number of bytes sent. Otherwise these bytes must be set to zero. Note that these bytes will have a non-zero value only if writing one or more bytes of actual data to an encrypted object. In all other cases the size should be set to zero, such as in the following circumstances: • The target object is not encrypted • Encryption is enabled for message reads only • The data is zero bytes in length. Note that, in this case, even if a CRC is requested for the write, the embedded data size will be 0, not 1 (that is, the CRC is ignored). These bytes are present only if encryption is active; they are not present if encryption is not active.

Data	0 or more bytes	The actual data to be written. The data is written to the device, starting at the location of the address pointer. The address pointer returns to its starting value when the I ² C STOP condition is detected.
CRC (optional)	1 byte	An optional 8-bit CRC that includes all the bytes that have been sent, including the two address bytes and the embedded data size bytes (if encryption is active), but not the SLA+W byte. If the device detects an error in the CRC during a write transfer, a COMSERR fault is reported by the Command Processor T6 object. See Section 7.4 "I2C Writes in Checksum Mode" for more details
Padding to 16 bytes (only if encrypted writes are enabled)	Maximum 15 bytes	If writing to an encrypted object, and there are one or more bytes of data (excluding the CRC), the data block (including the CRC, if present) must be padded to 16 bytes. If the data is zero bytes in size, the padding is not necessary and the data block will consist of the CRC only (if present).
STOP	1 bit	I ² C STOP condition

Figure 7-1 and Figure 7-2 show examples of writing four bytes of data to contiguous addresses starting at 0x1234.

FIGURE 7-1: EXAMPLE OF A FOUR-BYTE WRITE – ENCRYPTION NOT ACTIVE

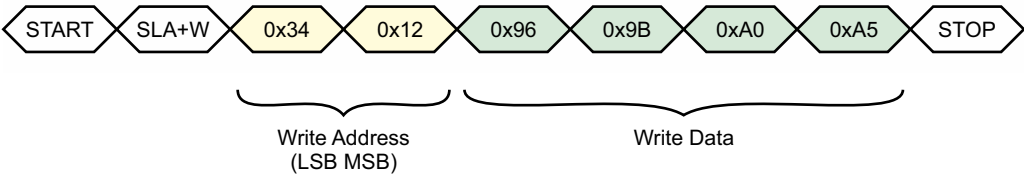
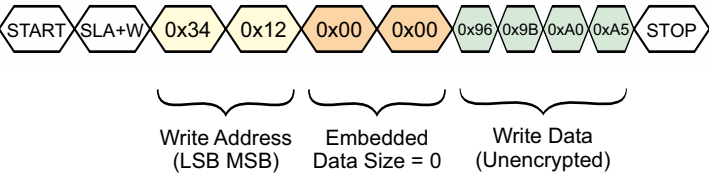
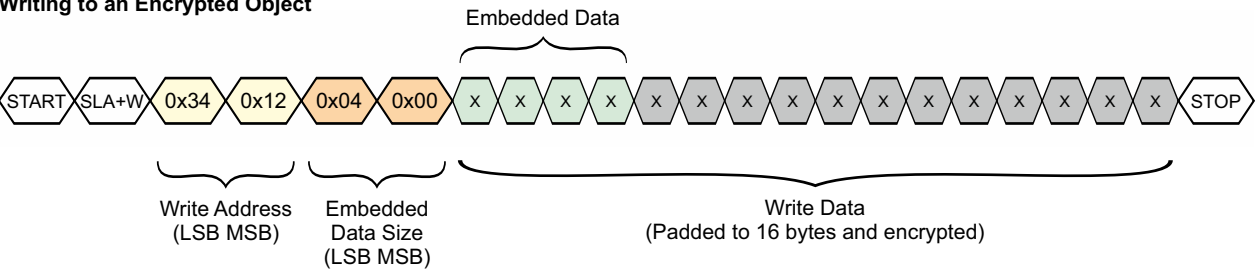


FIGURE 7-2: EXAMPLE OF A FOUR-BYTE WRITE – ENCRYPTION ACTIVE

Writing to an Unencrypted Object



Writing to an Encrypted Object

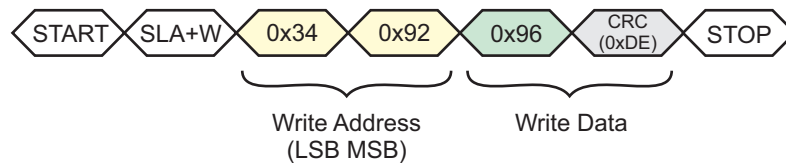


7.4 I²C Writes in Checksum Mode

In I²C checksum mode an 8-bit CRC is added to all I²C writes. The CRC is sent following the last data byte. All the bytes sent are included in the CRC, including the two address bytes and the two embedded data size bytes (if encryption is active). Any command or data sent to the device is processed even if the CRC fails.

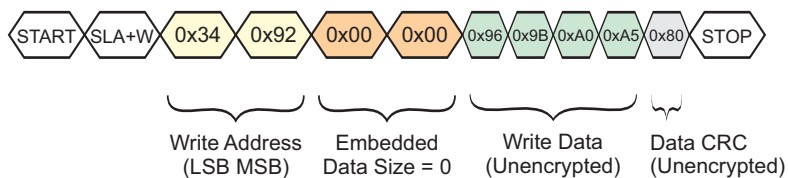
To indicate that a checksum is to be sent in the write, the most significant bit of the MSByte of the write address is set to 1. For example, the I²C command shown in Figure 7-3 writes a value of 150 (0x96) to address 0x1234 with a checksum. The address is changed to 0x9234 to indicate checksum mode.

FIGURE 7-3: EXAMPLE OF A WRITE TO ADDRESS 0x1234 WITH A CHECKSUM – ENCRYPTION NOT ACTIVE

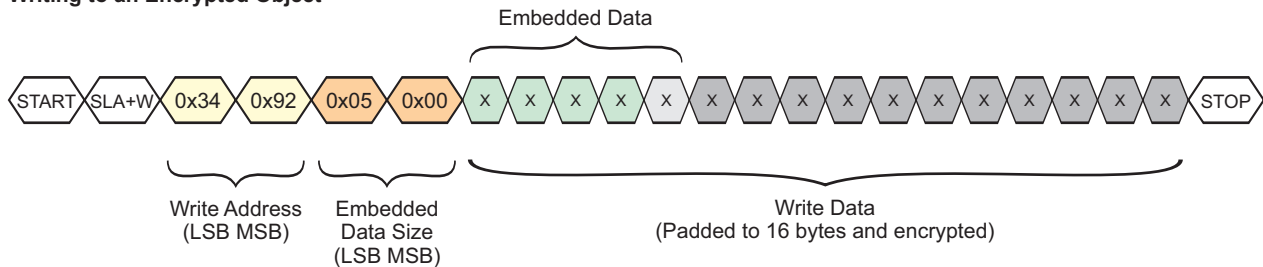


EXAMPLE OF A WRITE TO ADDRESS 0x1234 WITH A CHECKSUM – ENCRYPTION ACTIVE

Writing to an Unencrypted Object



Writing to an Encrypted Object



Note: When writing to an encrypted object, and data is present, the Embedded Data Size includes CRC byte (see [Section 7.3 "Writing To the Device"](#)).

7.5 Reading From the Device

Two I²C bus activities must take place to read from the device. The first activity is an I²C write to set the address pointer (LSByte then MSByte). The second activity is the actual I²C read to receive the data. The address pointer returns to its starting value when the read cycle NACK or STOP is detected.

It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation. The address pointer will be correct if the reads occur in order. In particular, when reading multiple messages from the Message Processor T5 object, the address pointer is automatically reset to the address of the Message Processor T5 object, in order to allow continuous reads (see [Section 7.7.1 "Reading Status Messages with DMA"](#)).

NOTE Encryption functionality on the MTCH3240P means that if the host read request falls within the Message Processor T5 address space, but not at its start address, the device considers it a valid Message Processor T5 message read. The device therefore sends the entire Message Processor T5 message. Note that the message may be encrypted or unencrypted, depending on the message encryption setting.

The WRITE and READ cycles consist of a START condition followed by the I²C address of the device (SLA+W or SLA+R respectively).

Figure 7-4 and Figure 7-5 show the I²C commands to read four bytes starting at address 0x1234.

FIGURE 7-4: EXAMPLE OF A FOUR-BYTE READ – ENCRYPTION NOT ACTIVE

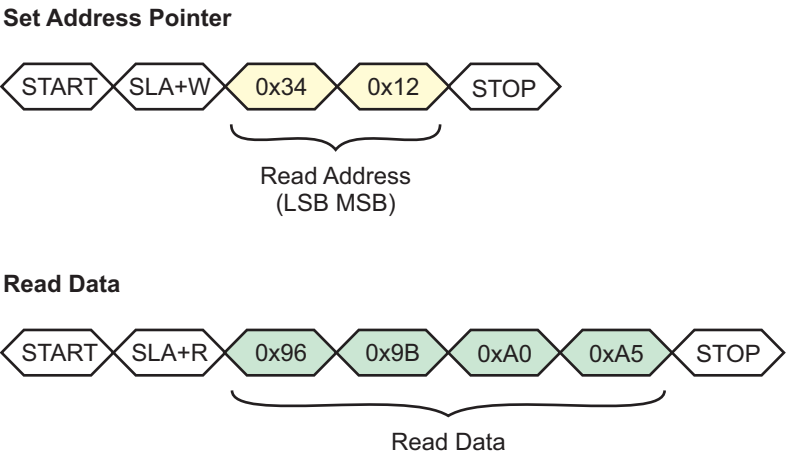
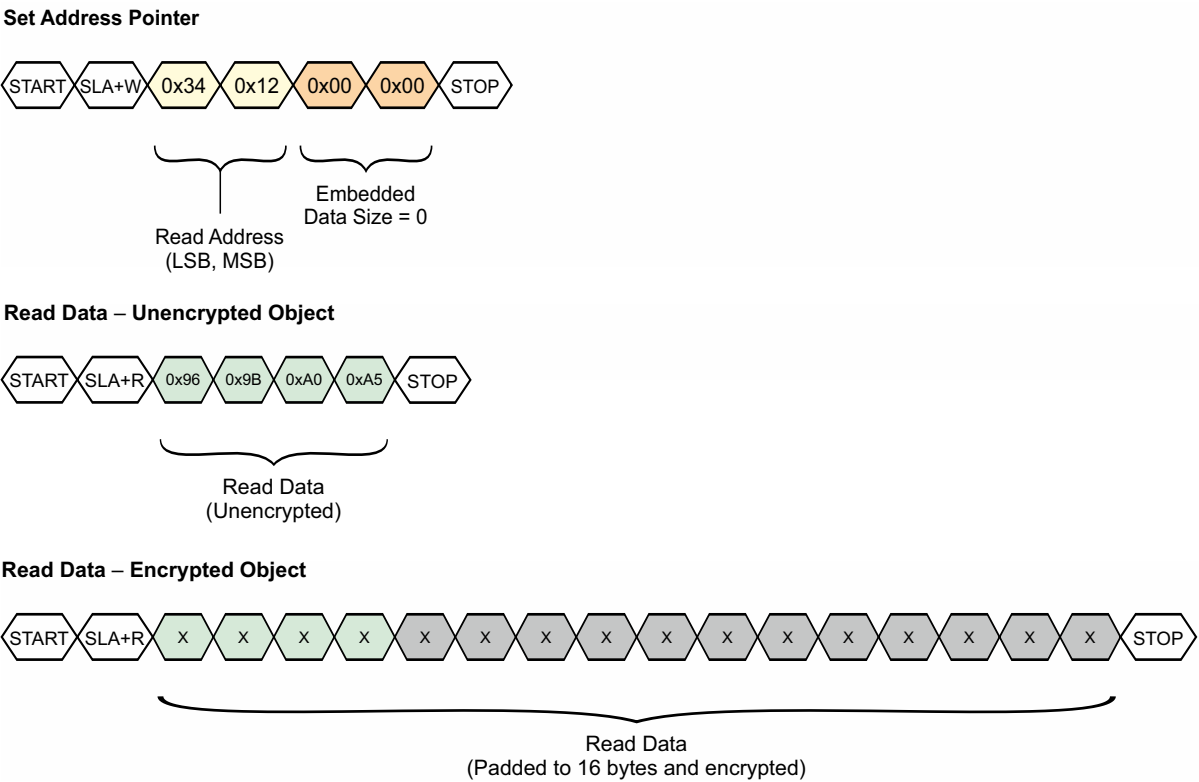


FIGURE 7-5: EXAMPLE OF A FOUR-BYTE READ – ENCRYPTION ACTIVE



NOTE At least one data byte must be read during an I²C READ transaction; it is illegal to abort the transaction with an I²C STOP condition without reading any data.

7.6 I²C Reads in Checksum Mode

In I²C checksum mode an 8-bit CRC is added to all I²C reads. The CRC is sent following the last data byte. The CRC includes the Report Id and the data bytes.

To indicate that a checksum is to be sent in the read response, the most significant bit of the MSByte of the write address is set to 1. For example, to read from address 0x1234 with a checksum, the address is changed to 0x9234 to indicate checksum mode.

7.7 Reading a Message from the Message Processor T5 Object

An I²C read of the Message Processor T5 object contains the following bytes:

START	1 bit	I ² C START condition.
SLA+R	1 byte	I ² C address of the device (see Section 7.2 "I2C Address"). If a checksum is requested, the MSBit of the address is set to 1.
Report ID	1 byte	Message report ID.
Data	7 bytes	The message data (that is, the Message Processor T5 MESSAGE field).
CRC (optional)	1 byte	An 8-bit CRC (if requested) for the Message Processor T5 report ID and message data. See Section 7.6 "I2C Reads in Checksum Mode" for more details on how to request a checksum.
Padding to 16 bytes (only if encrypted messages enabled)	5 or 6 bytes	If the encryption of Message Processor T5 messages is enabled, the data block (including the CRC, if present) is padded to 16 bytes.
STOP	1 bit	I ² C STOP condition.

[Figure 7-6](#) shows an example read from the Message Processor T5 object with a checksum. To read multiple messages using Direct Memory Access, see [Section 7.7.1 "Reading Status Messages with DMA"](#).

FIGURE 7-6: EXAMPLE READ FROM MESSAGE PROCESSOR T5 WITH A CHECKSUM – ENCRYPTION NOT ACTIVE

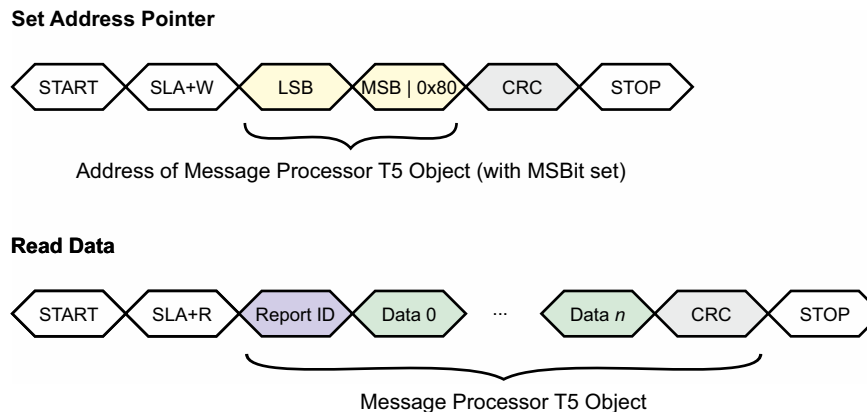
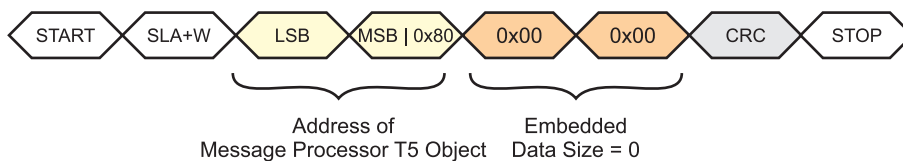
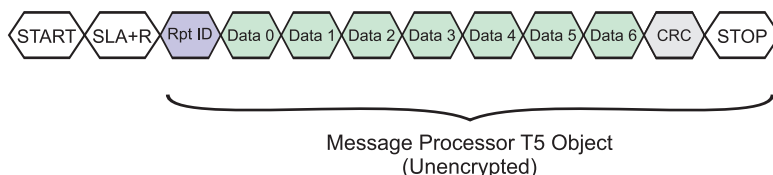


FIGURE 7-7: EXAMPLE READ FROM MESSAGE PROCESSOR T5 WITH A CHECKSUM – ENCRYPTION ACTIVE

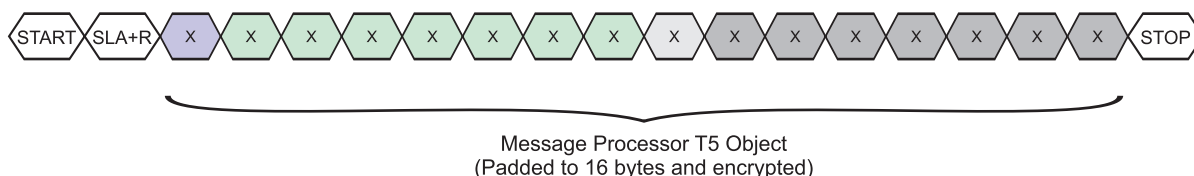
Set Address Pointer



Read Data – Unencrypted Message



Read Data – Encrypted Message



7.7.1 READING STATUS MESSAGES WITH DMA

The device facilitates the easy reading of multiple messages using a single continuous read operation. This allows the system host hardware to use a Direct Memory Access (DMA) controller for the fast reading of messages, as follows:

1. The system host uses a write operation to set the address pointer to the start of the Message Count T44 object, if necessary. Note that the STOP condition at the end of the read resets the address pointer to its initial location, so it may already be pointing at the Message Count T44 object following a previous message read. If a checksum is required on each message, the most significant bit of the MSByte of the read address must be set to 1.
2. The system host starts the read operation of the message by sending a START condition.
3. The system host reads the Message Count T44 object (one byte) to retrieve a count of the pending messages.
4. The system host calculates the number of bytes to read, as follows:
 - If encryption is not enabled, by multiplying the message count by the size of the Message Processor T5 object. Note that the system host should have already read the size of the Message Processor T5 object in its initialization code.
 - If encryption is enabled, by multiplying the message count by 16. Note that, in order to decrypt the message data, the system host will still need to know the size of the Message Processor T5 object.

Note that the size of the Message Processor T5 object as recorded in the Object Table includes the checksum. If a checksum has not been requested, one byte should be deducted from the size of the object.
That is: number of bytes = count × (size – 1).
5. The system host reads the calculated number of message bytes. It is important that the system host does *not* send a STOP condition during the message reads, as this will terminate the continuous read operation and reset the address pointer. No START and STOP conditions must be sent between the messages.
6. The system host sends a STOP condition at the end of the read operation after the last message has been read. The NACK condition immediately before the STOP condition resets the address pointer to the start of the Message Count T44 object.

Figure 7-8 shows an example of using a continuous read operation to read three messages from the device without a checksum. Figure 7-9 shows the same example with a checksum.

FIGURE 7-8: CONTINUOUS MESSAGE READ – NO CHECKSUM

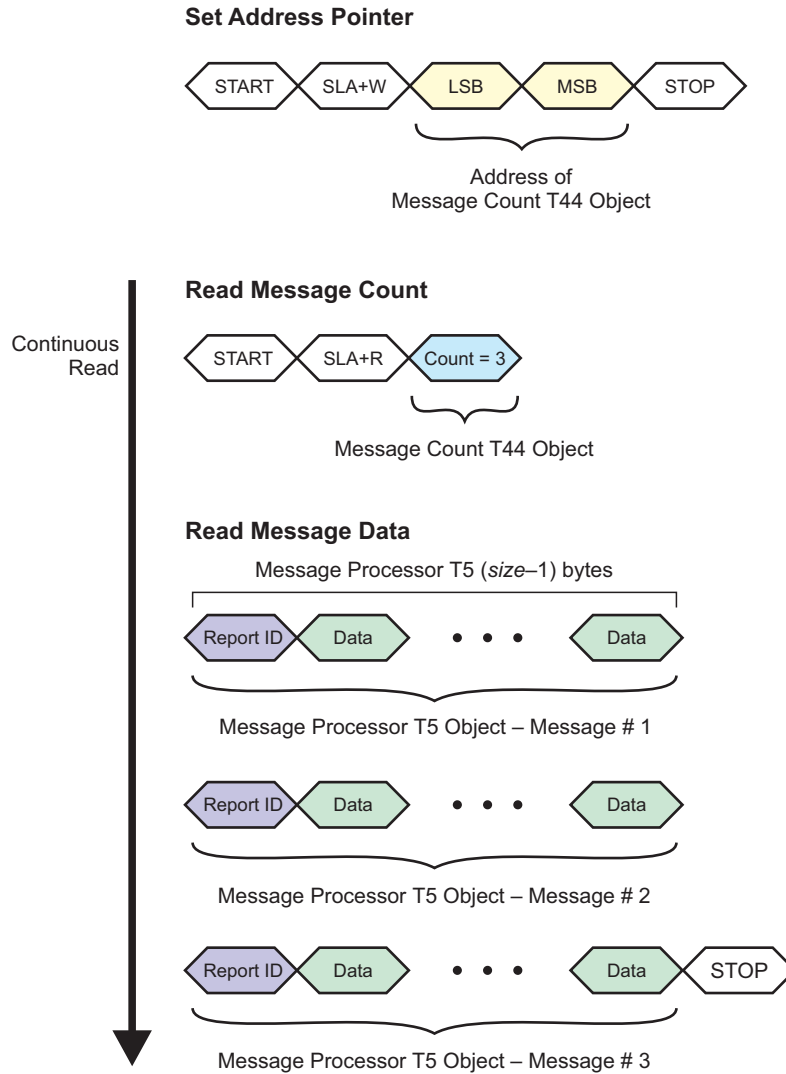
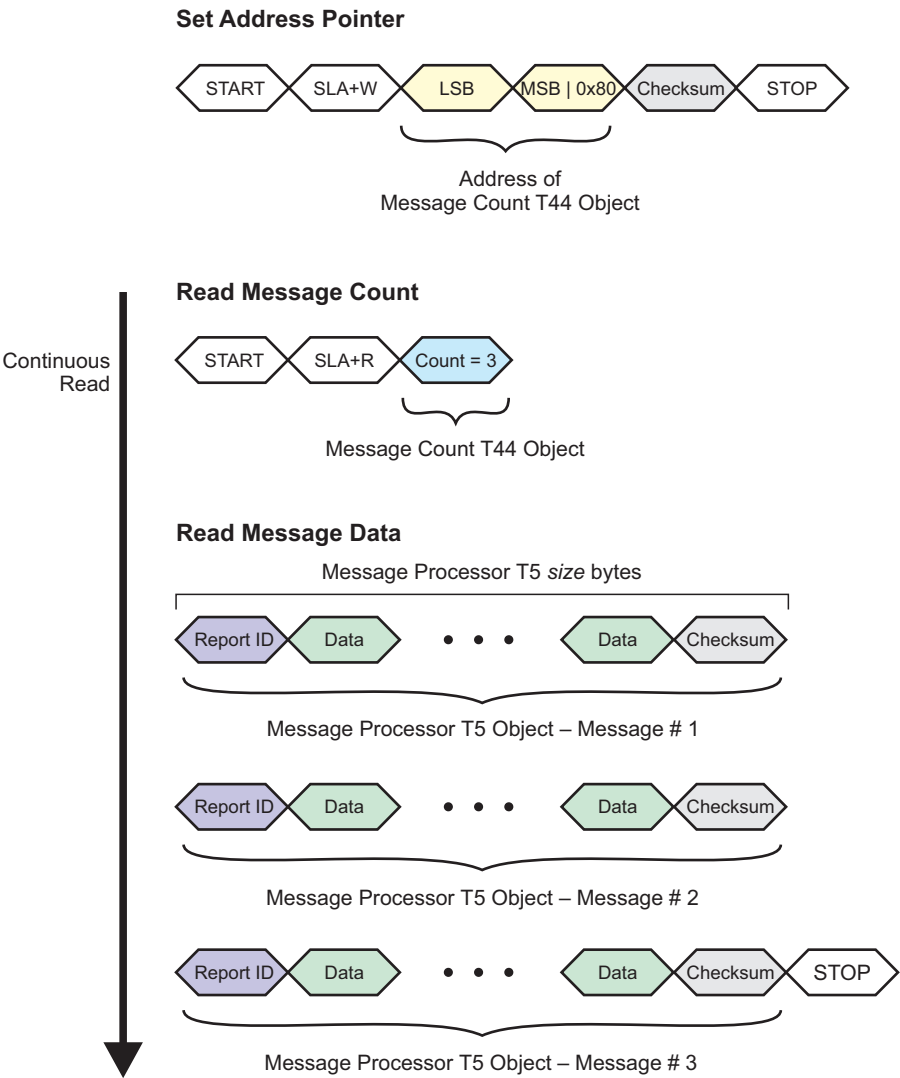
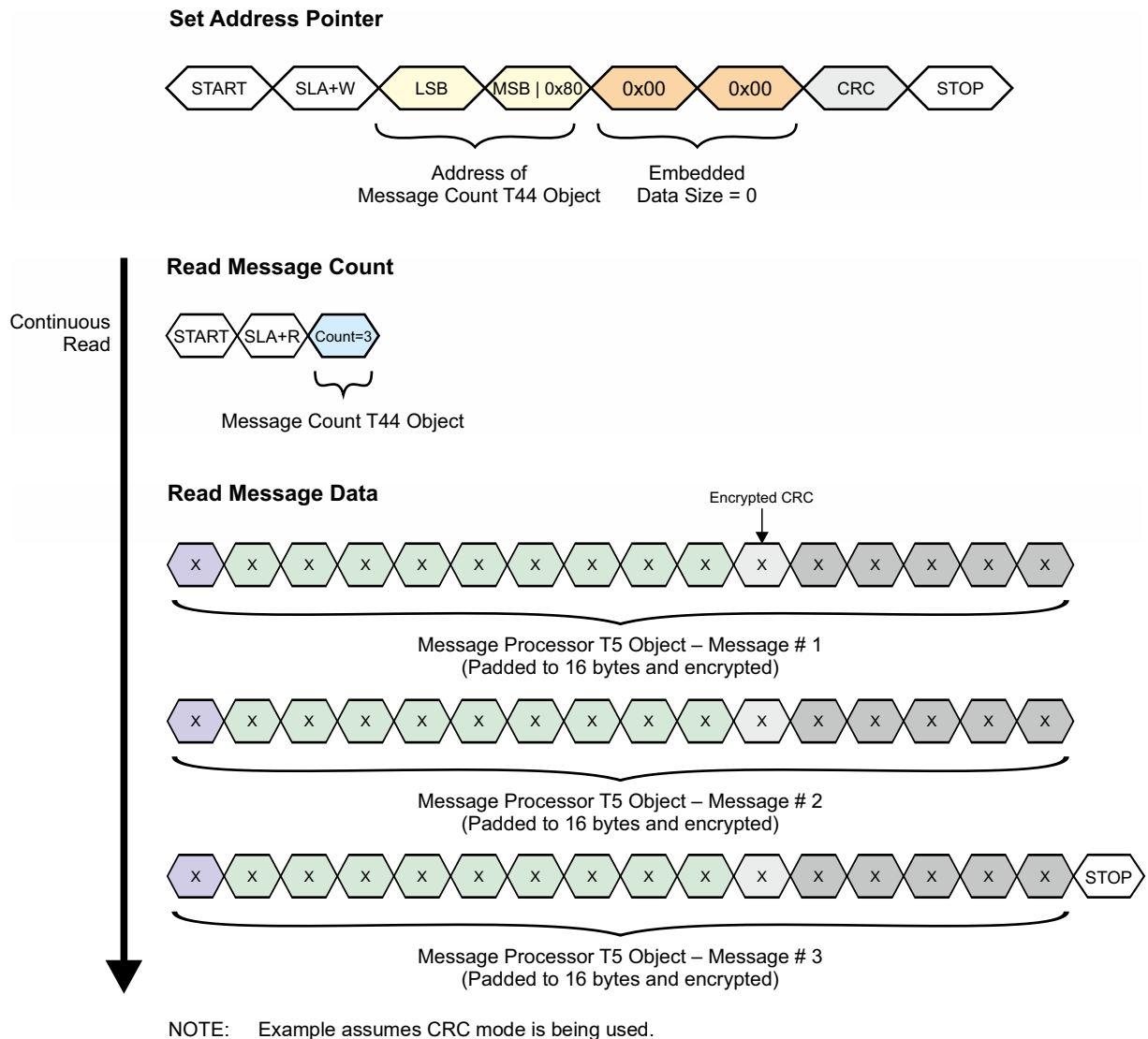


FIGURE 7-9: EXAMPLE CONTINUOUS MESSAGE READ – I²C CHECKSUM MODE



If encryption is enabled for Message Processor T5 message reads, then each message read using DMA will need to be decrypted. An example of this is shown in [Figure 7-10](#). Note that this example also assumes the use of a CRC on the message reads, although this is not necessary.

FIGURE 7-10: EXAMPLE CONTINUOUS READ FROM MESSAGE PROCESSOR T5 – ENCRYPTION ACTIVE



7.8 $\overline{\text{CHG}}$ Line

The $\overline{\text{CHG}}$ line is an active-low, open-drain output that is used as an interrupt to alert the system host that the device is ready to send a response, or that an OBP message is pending and ready to be read by the system host. This provides the system host with an interrupt-style interface with the potential for fast response times. It reduces the need for wasteful I²C communications.

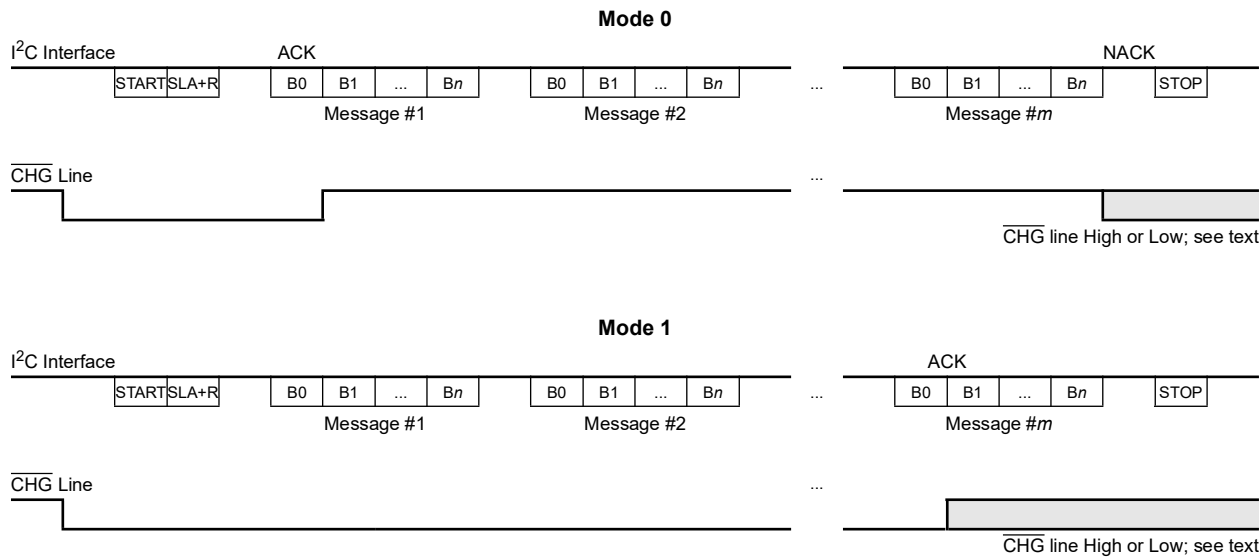
NOTE The system host should always use the $\overline{\text{CHG}}$ line as an indication that a message is ready to be read from the Message Processor T5 object; the system host should never poll the device for messages.

The $\overline{\text{CHG}}$ line should always be configured as an input on the system host during normal usage. This is particularly important after power-up or reset (see [Section 5.0 “Power-up / Reset Requirements”](#)).

A pull-up resistor is required to VddIO (see [Section 2.0 “Schematic”](#)).

The $\overline{\text{CHG}}$ line operates in two modes when it is used with I²C communications, as defined by the Communications Configuration T18 object.

FIGURE 7-11: CHG LINE MODES FOR I²C-COMPATIBLE TRANSFERS



In Mode 0 (edge-triggered operation):

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line goes high when the first byte of the first message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the buffer.
3. The STOP condition at the end of an I²C transfer causes the $\overline{\text{CHG}}$ line to stay high if there are no more messages. Otherwise the $\overline{\text{CHG}}$ line goes low to indicate a further message.

Note that Mode 0 also allows the system host to continually read messages by simply continuing to read bytes back without issuing a STOP condition. Message reading should end when a report ID of 255 ("invalid message") is received. Alternatively the system host ends the transfer by sending a NACK after receiving the last byte of a message, followed by a STOP condition. If there is another message present, the $\overline{\text{CHG}}$ line goes low again, as in step 1. In this mode the state of the $\overline{\text{CHG}}$ line does not need to be checked during the I²C read.

NOTE If functional safety implementation is required (that is, the user's product is to comply with UL/IEC 60730 Class B), a report ID of 255 is assumed to be an error. A report ID of 255, therefore, should not be used as an indication of the end of message reading.

In Mode 1 (level-triggered operation):

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line remains low while there are further messages to be sent after the current message.
3. The $\overline{\text{CHG}}$ line goes high again only once the first byte of the last message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the output buffer.

Mode 1 allows the system host to continually read the messages until the $\overline{\text{CHG}}$ line goes high, and the state of the $\overline{\text{CHG}}$ line determines whether or not the system host should continue receiving messages from the device.

NOTE The state of the $\overline{\text{CHG}}$ line should be checked only between messages and not between the bytes of a message. The precise point at which the $\overline{\text{CHG}}$ line changes state cannot be predicted and so the state of the $\overline{\text{CHG}}$ line cannot be guaranteed between bytes.

The Communications Configuration T18 object can be used to configure the behavior of the $\overline{\text{CHG}}$ line. In addition to the $\overline{\text{CHG}}$ line operation modes described above, this object allows direct control over the state of the $\overline{\text{CHG}}$ line.

7.9 SDA and SCL

The I²C bus transmits data and clock with SDA and SCL respectively. These are open-drain. The device can only drive these lines low or leave them open. The termination resistors (Rp) pull the line up to VddIO if no I²C device is pulling it down.

The termination resistors should be chosen so that the rise times on SDA and SCL meet the I²C specifications for the interface speed being used, bearing in mind other loads on the bus. For best latency performance, it is recommended that no other devices share the I²C bus with the MTCH3240P.

7.10 Clock Stretching

The MTCH3240P supports clock stretching in accordance with the I²C specification. It may also instigate a clock stretch if a communications event happens during a period when the MTCH3240P is busy internally. The maximum clock stretch is 2 ms and typically less than 350 µs.

8.0 PCB DESIGN CONSIDERATIONS

8.1 Introduction

The following sections give the design considerations that should be adhered to when designing a PCB layout for use with the MTCH3240P. Of these, power supply and ground tracking considerations are the most critical.

By observing the following design rules, and with careful preparation for the PCB layout exercise, designers will be assured of a far better chance of success and a correctly functioning product.

8.2 Printed Circuit Board

Microchip recommends the use of a four-layer printed circuit board for MTCH3240P applications. This, together with careful layout, will ensure that the board meets relevant EMC requirements for both noise radiation and susceptibility, as laid down by the various national and international standards agencies.

8.2.1 PCB CLEANLINESS

Modern no-clean-flux is generally compatible with capacitive sensing circuits.

CAUTION! If a PCB is reworked to correct soldering faults relating to any device, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

8.3 Power Supply

8.3.1 SUPPLY QUALITY

While the device has good Power Supply Rejection Ratio properties, poorly regulated and/or noisy power supplies can significantly reduce performance.

8.3.2 SUPPLY RAILS AND GROUND TRACKING

Power supply and clock distribution are the most critical parts of any board layout. Because of this, it is advisable that these be completed before any other tracking is undertaken. After these, supply decoupling, and analog and high speed digital signals should be addressed. Track widths for all signals, especially power rails should be kept as wide as possible in order to reduce inductance.

The Power and Ground planes themselves can form a useful capacitor. Flood filling for either or both of these supply rails, therefore, should be used where possible. It is important to ensure that there are no floating copper areas remaining on the board: all such areas should be connected to the ground plane. The flood filling should be done on the outside layers of the board.

8.3.3 POWER SUPPLY DECOUPLING

Decoupling capacitors should be fitted as specified in [Section 2.1 “Schematic Notes”](#).

The decoupling capacitors must be placed as close as possible to the pin being decoupled. The traces from these capacitors to the respective device pins should be wide and take a straight route. They should be routed over a ground plane as much as possible. The capacitor ground pins should also be connected directly to a ground plane.

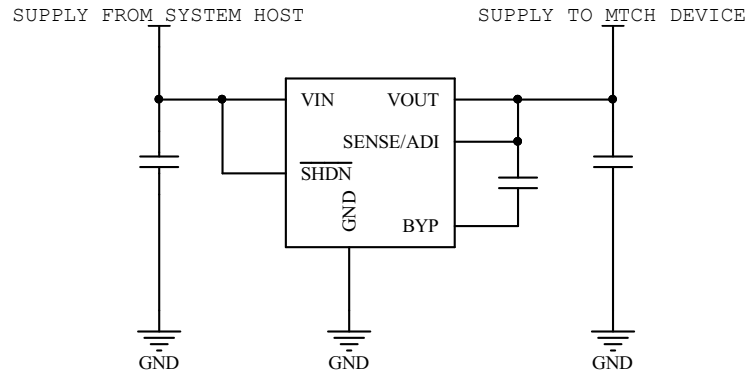
Surface mounting capacitors are preferred over wire-leaded types due to their lower ESR and ESL. It is often possible to fit these decoupling capacitors underneath and on the opposite side of the PCB to the digital ICs. This will provide the shortest tracking, and most effective decoupling possible.

8.3.4 VOLTAGE REGULATORS

The supply rails require a Low Drop-Out (LDO) voltage regulator that is shared between the rails (if the supply rails have different voltage levels separate LDOs are required).

Figure 8-1 shows an example circuit for an LDO.

FIGURE 8-1: EXAMPLE LDO CIRCUIT



An LDO regulator should be chosen that provides adequate output capability, low noise, no-load stability, good load regulation and step response. The MTCH3240P has been qualified for use only with the Microchip LDOs listed in Table 8-1 and Microchip cannot guarantee the functionality or performance of this MTCH controller with any other LDO. If an alternative LDO is needed in the user's product, please check with your local Microchip representative concerning its suitability.

NOTE Microchip recommends that a minimum of a 1.0 μF ceramic, low ESR capacitor at the input and output of these devices is always used. The datasheet for the device should always be referred to when selecting capacitors and the typical recommended values, types and dielectrics adhered to.

Sufficient output capacitance should be provided such that the output rate of rise is compatible with the MTCH3240P power rail specifications (see Section 11.2.1 "DC Characteristics"). This can be achieved by a combination of output capacitance on the pins of the LDO and bulk capacitance at the inputs to the MTCH3240P.

TABLE 8-1: LDO REGULATORS – QUALIFIED FOR USE

Manufacturer	Device	Current Rating (mA)
Microchip Technology Inc.	MCP1824	300
Microchip Technology Inc.	MIC5504	300
Microchip Technology Inc.	MIC5514	300

When designing a PCB for an application using a single LDO, extra care should be taken to ensure short, low inductance traces between the supply and the touch controller supply input pins. Ideally, tracking for the individual supplies should be arranged in a star configuration, with the LDO at the junction of the star. This will ensure that supply current variations or noise in one supply rail will have minimum effect on the other supplies. In applications where a ground plane is not practical, this same star layout should also apply to the power supply ground returns.

Only regulators with a 300 mA or greater rating can be used in a single-supply design.

Refer to the following application note for more information:

- Application Note: AN6564 – *Design Guide for PCB Layouts for MTCH Touch Controllers*

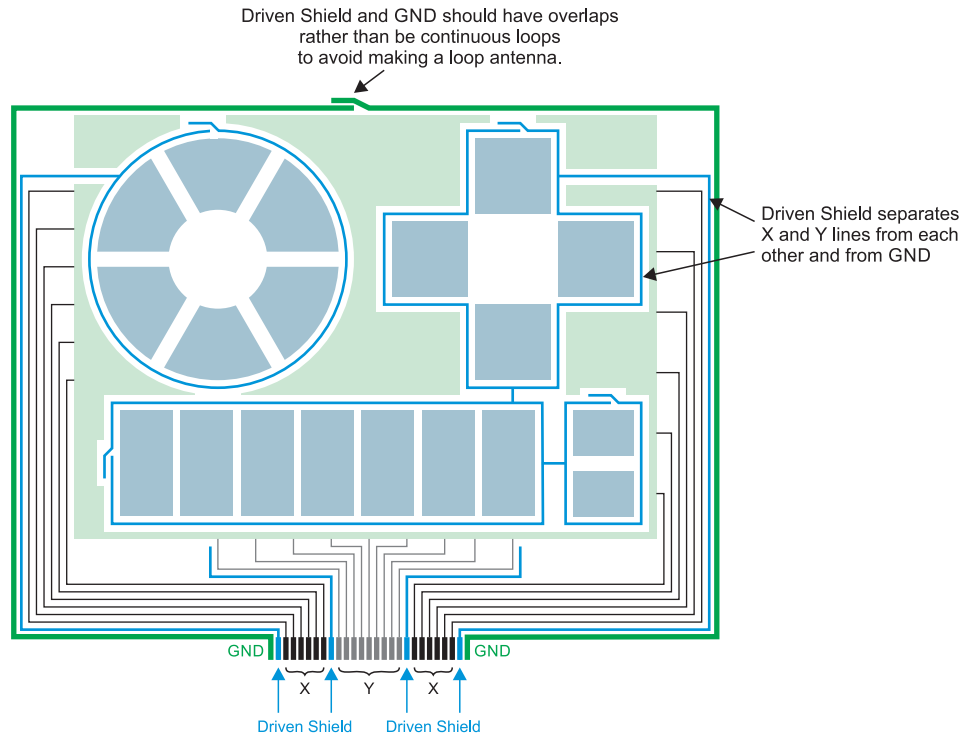
8.4 Driven Shield Line

The driven shield line is used to provide a guard track around the sensor panel that serves as Ground in mutual capacitance operation and as a driven shield in self capacitance operation.

The guard track must be routed between the groups of X tracks and the groups of Y tracks, as well as between the combined group of X/Y tracks and Ground. It should be fairly wide to avoid X-to-Y coupling in mutual capacitance operation, as the guard track will act as Ground in this circumstance.

A guard track is also needed between any self capacitance X/Y lines and mutual capacitance only X/Y lines.

FIGURE 8-2: EXAMPLE DRIVEN SHIELD ROUTING



NOTE Sample touchscreen for illustrative purposes only. In addition, the routing of the X/Y lines shown should not be taken as indicative of any preferred layout and the user's layout may vary.

8.5 ESD Ground Routing

To avoid damage due to ESD strikes, the outermost track on the sensor should be an ESD ground (see [Figure 8-2](#)). This should completely surround the sensor, but with an overlap at the top rather than forming a complete loop (similar to the driven shield).

To avoid electromagnetic induction of currents into the driven shield trace, a minimum separation of 0.3 mm should be maintained between the ESD GND trace and the Driven Shield.

The ESD ground traces should be connected to a dedicated ground trace in the PCB, and routed such that ESD strike currents do not flow under or close to the touch controller or the connecting wiring between it and the sensor array. The ESD ground should be connected in to the main system ground at a star point at the main GND connection to the PCB.

See also:

- Application Note: AN6564 – *Design Guide for PCB Layouts for MTCH Touch Controllers*

8.6 Analog I/O

In general, tracking for the analog I/O signals from the device should be kept as short as possible. These normally go to a connector which interfaces directly to the sensor.

Ensure that adequate ground-planes are used. An analog ground plane should be used in addition to a digital one. Care should be taken to ensure that both ground planes are kept separate and are connected together only at the point of entry for the power to the PCB. This is usually at the input connector.

8.7 Component Placement and Tracking

It is important to orient all devices so that the tracking for important signals (such as power and clocks) are kept as short as possible.

8.7.1 DIGITAL SIGNALS

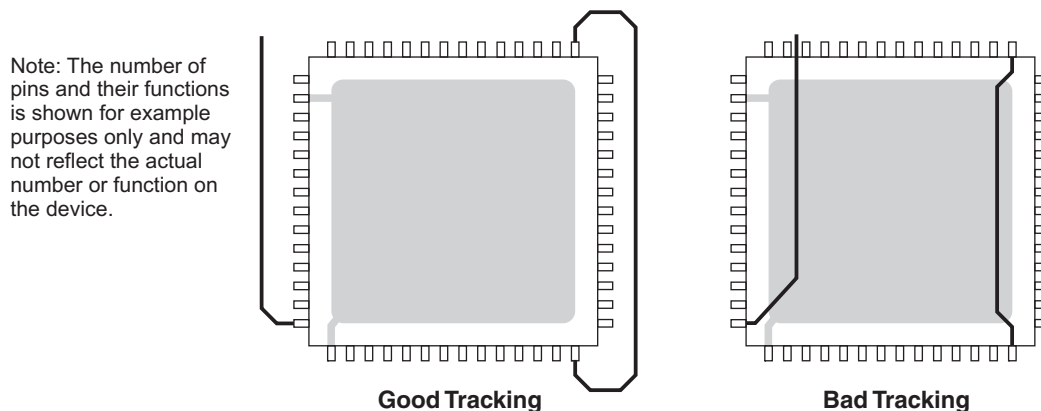
In general, when tracking digital signals, it is advisable to avoid sharp directional changes on sensitive signal tracks (such as analog I/O) and any clock tracking.

A good ground return path for all signals should be provided, where possible, to ensure that there are no discontinuities.

8.7.2 QFN PACKAGE RESTRICTIONS

The central pad on the underside of the QFN device should be connected to ground. Do not run any tracks underneath the body of the device on the top layer of the PCB, only ground. [Figure 8-3](#) shows examples of good and bad tracking.

FIGURE 8-3: EXAMPLES OF GOOD AND BAD TRACKING



8.8 EMC and Other Observations

The following recommendations are not mandatory, but may help in situations where particularly difficult EMC or other problems are present:

- Try to keep as many signals as possible on the inside layers of the board. If suitable ground flood fills are used on the top and bottom layers, these will provide a good level of screening for noisy signals, both into and out of the PCB.
- Ensure that the on-board regulators have sufficient tracking around and underneath the devices to act as a heatsink. This heatsink will normally be connected to the 0 V or ground supply pin. Increasing the width of the copper tracking to any of the device pins will aid in removing heat. There should be no solder mask over the copper track underneath the body of the regulators.
- Ensure that the decoupling capacitors, especially high capacity ceramic type, have the requisite low ESR, ESL and good stability/temperature properties. Refer to the regulator manufacturer's datasheet for more information.

9.0 GETTING STARTED WITH MTCH3240P

9.1 Establishing Contact

9.1.1 COMMUNICATION WITH THE SYSTEM HOST

The system host can use the following interface to communicate with the device:

- I²C interface (see [Section 7.0 “I2C Communications”](#))

9.1.2 POWER-UP SEQUENCE

The power-up sequence is as follows:

1. After the device has reset, the $\overline{\text{CHG}}$ line goes low to indicate to the system host that a message is available. If the $\overline{\text{CHG}}$ line does not go low within a suitable timeout, there is a problem with the device. The timeout should be chosen to be, for example, three times the relevant typical values for the system as defined in [Section 11.6.2 “Reset Timings”](#) (for example, 1 second if all POST tests are performed).
2. Once the device is ready, the system host should attempt to read the ID Information portion of the Information Block in the device to establish that the device is present and running following power-up. See [Section 9.1.3 “Initialization procedure”](#) for more details.
3. The device performs a checksum on the configuration settings held in the non-volatile memory. If the checksum does not match a stored copy of the last checksum, then this indicates that the settings have become corrupted. For compliance with UL/IEC 60730 Class B, the system host should make the system safe if the read checksum does not match the expected checksum, or if the configuration error bit in the message data from the Command Processor T6 object is set.

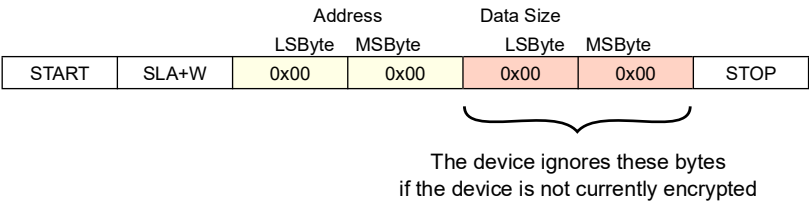
9.1.3 INITIALIZATION PROCEDURE

Once the device has powered up, the system host should perform the following initialization steps so that it can communicate with the device:

1. Immediately after start-up, the system host should attempt to read the ID Information portion of the Information Block). This will also be used to determine whether the device is encrypted or not, and therefore which communications protocol to use. A successful read will also confirm that the device is present and running following power-up. The ID Information forms the first 7 bytes of memory in the device at address 0x0000.

The write transfer to set the address pointer to 0x0000 must be sent using the encryption communications protocol, even if the device is currently unencrypted. If the device is expecting an encrypted format write transfer, it will expect, and accept, the entire write transfer. If, however, the device is not currently encrypted it will simply ignore the extra bytes in the write transfer (see [Figure 9-1](#)).

FIGURE 9-1: WRITE TRANSFER



2. Once the system host has read the Information Block, the system host should examine the Variant ID and use it to determine if encrypted communications are active. The Variant ID is the second byte in the Information Block (read in [Step 1](#)).
- If encryption is not active (default), the most significant bit will be set to 0 (that is, the Variant ID is 0x01).
- If encryption is active, the most significant bit will be set to 1 (that is, the Variant ID is 0x81).
3. The system host can now read the start positions of all the objects in the device from the Object Table and build up a list of the object addresses. Note that the number of Object Table elements was read by the system host at start-up as part of the ID Information bytes. If encryption is active:
 - a) Record the start position of the User Data T38 object (found in [Step 3](#)).

- b) If encrypted configuration read/writes are enabled, use the address of the User Data T38 object to determine which objects will use encryption. These are the objects that are located after the User Data T38 object (that is, they have higher addresses).
4. Read the Encryption Status T2 object to determine which mode of encryption is enabled (that is, encrypted configuration read/writes and/or encrypted messages). This will determine the communications protocol to use to read or write configuration parameters and to read messages from the device.
5. Use the Object Table to calculate the report IDs so that messages from the device can be correctly interpreted.
6. Read any pending messages generated during the start-up process. Note that [Step 4.](#) will have determined the communications protocol to use for reading messages.

IMPORTANT! No assumption should be made concerning the order of the messages received by the system host from the device, particularly on start-up. For example, on start-up the first messages will be the Command Processor T6 Reset message and any Self Test Control T10 POST failure message (if Self Test Control T10 POST tests are enabled and an error occurs) in either order.

9.2 Using the Object-based Protocol

The device has an object-based protocol (OBP) that is used to communicate with the device. Typical communication includes configuring the device, sending commands to the device, and receiving messages from the device.

9.2.1 CLASSES OF OBJECTS

The MTCH3240P contains the following classes of objects:

- **Debug objects** – provide a raw data output method for development and testing.
- **General objects** – required for global configuration, transmitting messages and receiving commands.
- **Touch objects** – operate on measured signals from the touch sensor and report touch data.
- **Signal processing objects** – process data from other objects (typically signal filtering operations).
- **Support objects** – provide additional functionality on the device.

9.2.2 OBJECT INSTANCES

TABLE 9-1: OBJECTS ON THE MTCH3240P

Object	Description	Number of Instances	Usage
Debug Objects			
Diagnostic Debug T37	Allows access to diagnostic debug data to aid development.	1	Debug commands only; Read-only object. No configuration or tuning is necessary. Not for use in production. Debug data is not encrypted.
General Objects			
Encryption Status T2	Provides information on the configuration encryption status.	1	Read-only object; no configuration is necessary. Object is not encrypted.
Message Processor T5	Handles the transmission of messages. This object holds a message in its memory space for the host to read.	1	Read-only object; no configuration is necessary. Messages can be encrypted.
Command Processor T6	Performs a command when written to. Commands include reset, calibrate and backup settings.	1	No configuration is necessary. Object is not encrypted.
Power Configuration T7	Controls the sleep mode of the device. Power consumption can be lowered by controlling the acquisition frequency and the sleep time between acquisitions.	1	Must be configured before use. Configuration read/writes may be encrypted.
Acquisition Configuration T8	Controls how the device takes each capacitive measurement.	1	Must be configured before use. Configuration read/writes may be encrypted.

TABLE 9-1: OBJECTS ON THE MTCH3240P (CONTINUED)

Object	Description	Number of Instances	Usage
Extended Object Table T254	Extends the Information Block at the start of the memory map to allow 16-bit type codes.	1	Read-only object; no configuration is necessary. Object is not encrypted.
Touch Objects			
Key Array T500	Configures the measurement type for an array of touch sensor nodes that act as keys.	1	Configure as required. Configuration read/writes may be encrypted.
Signal Processing Objects			
Lens Bending T65	Compensates for lens deformation (lens bending) by attempting to eliminate the disturbance signal from the reported deltas.	3	Enable and configure as required. Configuration read/writes may be encrypted.
Noise Suppression T72	Performs various noise reduction techniques during sensor signal acquisition.	1	Enable and configure as required. Configuration read/writes may be encrypted.
Support Objects			
Self Test Control T10	Controls the self-test routines to find faults on the touch sensor.	1	Enable and configure as required. Configuration read/writes may be encrypted.
Self Test Pin Faults T11	Specifies the configuration settings for the Pin Fault self tests.	1	Configure as required. Configuration read/writes may be encrypted.
Self Test Signal Limits T12	Specifies the configuration settings for the Signal Limit self tests.	1	Configure as required. Configuration read/writes may be encrypted.
Communications Configuration T18	Configures additional communications behavior for the device.	1	Check and configure as necessary. Configuration read/writes may be encrypted.
GPIO Configuration T19	Allows the host controller to configure and use the general purpose I/O pins on the device.	1	Enable and configure as required. Configuration read/writes may be encrypted.
User Data T38	Provides a data storage area for user data.	1	Configure as required. Object is not encrypted.
Message Count T44	Provides a count of pending messages.	1	Read-only object; no configuration is necessary. Object is not encrypted.
CTE Configuration T46	Controls the capacitive touch engine for the device.	1	Must be configured. Configuration read/writes may be encrypted.
Timer T61	Provides control of a timer.	6	Enable and configure as required. Configuration read/writes may be encrypted.
Serial Data Command T68	Provides an interface for the host driver to deliver various data sets to the device.	1	Enable and configure as required. Object is not encrypted.
Dynamic Configuration Controller T70	Allows rules to be defined that respond to system events.	20	Enable and configure as required. Configuration read/writes may be encrypted.
Dynamic Configuration Container T71	Allows the storage of user configuration on the device that can be selected at runtime based on rules defined in the Dynamic Configuration Controller T70 object.	1	Configure if Dynamic Configuration Controller T70 is in use. Configuration read/writes may be encrypted.
Self Capacitance Global Configuration T109	Provides configuration for self capacitance measurements employed on the device.	1	Check and configure as required (if using self capacitance measurements). Configuration read/writes may be encrypted.

TABLE 9-1: OBJECTS ON THE MTCH3240P (CONTINUED)

Object	Description	Number of Instances	Usage
Self Capacitance Tuning Parameters T110	Provides configuration space for a generic set of settings for self capacitance measurements.	4	Use under the guidance of Microchip field engineers only. Configuration read/writes may be encrypted.
Self Capacitance Configuration T111	Provides configuration for self capacitance measurements employed on the device.	2	Check and configure as required (if using self capacitance measurements). Configuration read/writes may be encrypted.
Low Power Idle Configuration T126	Configures the overall behavior of the low power mode.	1	Enable and configure as required. Configuration read/writes may be encrypted.
Key Controller T501	Controls an individual key.	32	Enable and configure as required. Configuration read/writes may be encrypted.
Slider Controller T502	Configures a continuous group of keys to operate as either a linear slider or a circular wheel.	6	Enable and configure as required. Configuration read/writes may be encrypted.

9.2.3 CONFIGURING AND TUNING THE DEVICE

The objects are designed such that a default value of zero in their fields is a “safe” value that typically disables functionality. The objects must be configured before use and the settings written to the non-volatile memory using the Command Processor T6 object.

Perform the following actions for each object:

1. Enable the object, if the object requires it.
2. Configure the fields in the object, as required.
3. Enable reporting, if the object supports messages, to receive messages from the object.

9.3 Writing to the Device

Communication with the device is achieved using an I²C write operation (see [Section 7.3 “Writing To the Device”](#)) to write to the appropriate object:

- To send a command to the device, an appropriate command is written to the Command Processor T6 object.
- To configure the device, a configuration parameter is written to the appropriate object. For example, writing to the Power Configuration T7 configures the power consumption for the device and writing to the Key Array T500 object sets up the sensor.
- Some objects are optional and need to be enabled before use.

Any modifications to the configuration in the device can be backed up to non-volatile memory (NVM). The stored configuration settings will then be loaded automatically on the subsequent start-up of the device.

IMPORTANT! When performing an NVM write, it is important that a Hardware Reset or a power down does not take place before the NVM write process is complete.

To determine if the NVM write has completed, the $\overline{\text{CHG}}$ line can be monitored. If the $\overline{\text{CHG}}$ line is asserted, the message's Report ID should be checked to verify that the $\overline{\text{CHG}}$ line assertion is caused by a message from the target object and not from some other source. Note that the CTRL RPTEN control bit of the target object should be set to 1 (if the object has reporting capabilities) to ensure that the object will assert the $\overline{\text{CHG}}$ line as expected.

9.3.1 WRITING A CONFIGURATION TO THE DEVICE

During a configuration download, device operation may be based upon only part of that configuration because it is yet to finish downloading. In rare circumstances, the total processing time might exceed the WDT reset time. This is more likely to happen when measurements take a long time to perform due to the partial configuration.

To ensure that the configuration is written safely, follow these steps:

1. Use the Command Processor T6 Freeze command (BACKUPNV = 0x22) to suspend device operations.
2. Write the configuration to the device using the Command Processor T6 Backup command (BACKUPNV = 0x55).
3. Finally, use the Command Processor T6 Unfreeze command (BACKUPNV = 0x11) to resume device operations.

9.4 Reading from the Device

Reading a configuration from the device is described in [Section 7.5 “Reading From the Device”](#).

Status information is stored in the Message Processor T5 object. This object can be read to receive any status information from the device. For compliance with UL/IEC 60730 Class B, the system host should monitor the sequence number and take appropriate action if it detects a missing or repeated message, or if a message is received out of sequence. The following mechanisms can be used to read messages:

- The $\overline{\text{CHG}}$ line is asserted whenever a new message is available in the Message Processor T5 object. The system host should read the available message. See the sections for each interface for more information. See [Section 7.8 “CHG Line”](#) for more information.
- Direct Memory Access (DMA) reads can be used to read multiple Message Processor T5 messages using a single continuous read operation. See [Section 7.7.1 “Reading Status Messages with DMA”](#) for more information.

NOTE	The system host should always wait to be notified of messages; the system host should not poll the device for messages, either by polling the Message Processor T5 object or by polling the CHG line.
-------------	---

10.0 DEBUGGING AND TUNING

10.1 Object-based Protocol

The device provides a mechanism for obtaining debug data for development and testing purposes by reading data from the Diagnostic Debug T37 object.

10.2 Debug Data and Encryption

It is possible to disable all debug data output from all sources if encryption is active. This is achieved by setting the STATUS DISDBG parameter in the Encryption Status T2 object.

This feature disables debug data from the following sources:

- The Diagnostic Debug T37 object

10.3 Self Test

The Self Test Control T10, Self Test Pin Faults T11 and Self Test Signal Limits T12 objects run self-test routines in the device to find hardware faults in the device both at power-on/reset and during normal operation. These self-test routines can be configured to check the CPU, clock, memory and power supplies of the devices, as well as CTE operation and the signal levels. The tests can also check for pin shorts between sensor X and Y pins, and between the sensor lines and DS0, power or GND pins.

The Self Test Control T10 object can also provide continuous monitoring of the health of the device while it is in operation. A periodic Built-In Self Test (BIST) test can be run at a user-specified interval to monitor the global pass and specific fail status (as determined by the device configuration). Reporting is achieved by standard Self Test Control T10 object protocol messages.

IMPORTANT! For compliance with UL/IEC 60730 Class B, reporting should be achieved using Self Test Control T10 object protocol messages and not by a hardware GPIO pin.

For a list of the self tests available on the MTCH3240P, see [Table 10-1](#).

TABLE 10-1: SELF TESTS

Self Test Group	Run as...		
	Pre-Operation Self Test (POST)	Built-In Self Test (BIST)	On Demand Test
CPU	Automatically tested at start-up	Yes	–
Internal Interrupts	Yes	Yes	–
Clock	Yes	Yes	–
Flash Memory	Yes	Yes	–
NVM Settings ⁽²⁾	Automatically tested at start-up	No	Yes
RAM	CTE RAM: Yes AVR RAM: Automatically tested at start-up	Yes	–
Power	Yes	Yes	Yes
CTE (Capacitive Touch Engine)	Yes	Yes	–
Pin Faults	Yes	Yes	Yes
Signal Limits	Yes	Yes	Yes

} Internal System

} CTE and Touch System

Note 1: If the Driven Shield Signal Limit test is enabled in Self Test Signal Limits T12, the Signal Limit tests include additional tests on the Driven Shield (DS0) pin.

Note 2: This is the region in the non volatile memory (NVM) to which the device backs up the OBP configuration settings and stores the payload data.

MTCH3240P

11.0 SPECIFICATIONS

11.1 Absolute Maximum Specifications

Vdd	3.6V
VddIO	3.6V
Maximum continuous combined pin current, all GPIO pins	40 mA
Voltage forced onto any pin	−0.3V to + 0.3V (Vdd or VddIO)
Configuration parameters maximum writes	10,000
Maximum junction temperature	125°C

CAUTION! Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.

11.2 Recommended Operating Conditions

Operating temperature	−40°C to +105°C
Storage temperature	−60°C to +150°C
Vdd	3.3 V
VddIO	1.8 V to 3.3 V
Temperature slew rate	10°C/min

11.2.1 DC CHARACTERISTICS

11.2.1.1 Digital Voltage Supply – VddIO, Vdd

Parameter	Min	Typ	Max	Units	Notes
VddIO					
Operating limits – Normal Voltage	2.7	3.3	3.47	V	
Operating limits – Low Voltage	1.71	1.8	1.89	V	
Supply Rise Rate	–	–	0.036	V/μs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 μs to rise
Vdd					
Operating limits	2.7	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/μs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 μs to rise
Supply Fall Rate	–	–	0.05	V/μs	For example, for a 3.3 V rail, the voltage should take a minimum of 66 μs to fall

11.2.2 POWER SUPPLY RIPPLE AND NOISE

Parameter	Min	Typ	Max	Units	Notes
Vdd, VddIO	–	–	±50	mV	Across frequency range 1 Hz to 1 MHz

11.3 Test Configuration

The configuration values listed below were used in the reference unit to validate the interfaces and derive the characterization data provided in the following sections. Where the values differ, this is noted.

TABLE 11-1: TEST CONFIGURATION – Mutual Capacitance

Object/Parameter	Description/Setting (Numbers in Decimal)
Power Configuration T7	
CFG2	0 (Power Monitor Enabled)
Acquisition Configuration T8	
CHRGTIME	9
CTE Configuration T46	
IDLESYNCSPERX	8
ACTVSYNCSPERX	8
Lens Bending T65 Instance 0	Object Instance Enabled
Noise Suppression T72	Object Enabled
Slider Controller T502 Instance 0	Object Instance Enabled
Key Array T500	Object Enabled; Reporting Enabled
CTRL	MEASTYPE = 0 (Mutual Capacitance – Single Ended)) KEYORDER = 0 (keys ordered along X lines)
XSIZE	4
YSIZE	7
Key Controller T501 Instance 0 to Instance 27	Object Instance Enabled

TABLE 11-2: TEST CONFIGURATION – Self Capacitance

Object/Parameter	Description/Setting (Numbers in Decimal)
Power Configuration T7	
CFG2	0 (Power Monitor Enabled)
Acquisition Configuration T8	
MEASALLOW	10
CTE Configuration T46	
IDLESYNCSPERX	8
ACTVSYNCSPERX	8
Lens Bending T65 Instance 1	Object Instance Enabled
Lens Bending T65 Instance 2	Object Instance Enabled
Noise Suppression T72	Object Enabled
Self Capacitance Configuration T111 Instance 0	
INTTIME	27
IDLESYNCSPERL	24
ACTVSYNCSPERL	24
Self Capacitance Configuration T111 Instance 1	
INTTIME	27
IDLESYNCSPERL	24
ACTVSYNCSPERL	24
Low Power Idle Configuration T126	Object Enabled; Reporting Enabled

TABLE 11-2: TEST CONFIGURATION – Self Capacitance (CONTINUED)

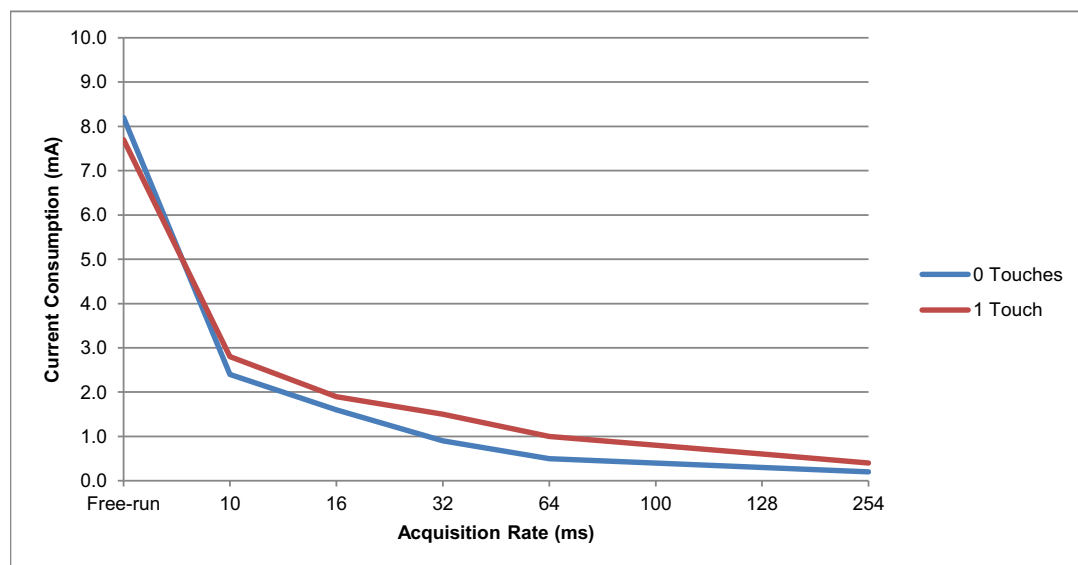
Object/Parameter	Description/Setting (Numbers in Decimal)
Key Array T500	Object Enabled; Reporting Enabled
CTRL	MEASTYPE = 3 (Self Capacitance – P2P) KEYORDER = 1 (X lines followed by Y lines)
XSIZE	12
YSIZE	12
Key Controller T501 Instance 0 to Instance 21	Object Instance Enabled; Reporting Enabled
Slider Controller T502 Instance 0	Object Instance Enabled; Reporting Enabled
Slider Controller T502 Instance 1	Object Instance Enabled; Reporting Enabled

11.4 Current Consumption – Mutual Capacitance

NOTE The characterization charts show typical values based on the configuration in [Table 11-1](#). In particular, BIST processing has been disabled. Actual power consumption in the user's application will depend on the circumstances of that particular project and will vary from that shown here. Further tuning will be required to achieve an optimal performance.

11.4.1 VDD

Acquisition Rate (ms)	Current Consumption (mA)	
	0 Touches	1 Touch
Free-run	8.2	7.7
10	2.4	2.8
16	1.6	1.9
32	0.9	1.5
64	0.5	1
100	0.4	0.8
128	0.3	0.6
254	0.2	0.4



11.4.2 VDDIO

Current Consumption (mA)	
0 Touches	1 Touch
0.02	0.02

11.4.3 DEEP SLEEP

Power Monitor On, Sampling mode; $T_A = 25^\circ\text{C}$

Parameter	Value	Units	Notes
Deep Sleep Current	0.3	mA	Vdd = 3.3V VddIO = 3.3V
Deep Sleep Power	1.0	mW	

Power Monitor Off; $T_A = 25^\circ\text{C}$

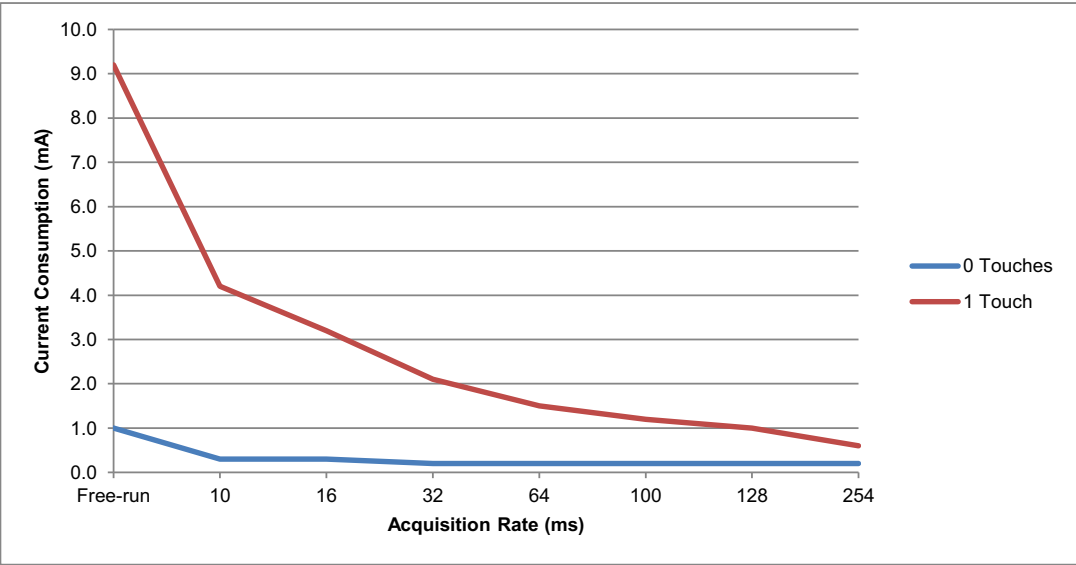
Parameter	Value	Units	Notes
Deep Sleep Current	0.2	mA	Vdd = 3.3V VddIO = 3.3V
Deep Sleep Power	0.5	mW	

11.5 Current Consumption – Self Capacitance

NOTE The characterization charts show typical values based on the configuration in [Table 11-2 on page 45](#). In particular, BIST processing has been disabled. Actual power consumption in the user's application will depend on the circumstances of that particular project and will vary from that shown here. Further tuning will be required to achieve an optimal performance.

11.5.1 VDD

Acquisition Rate (ms)	Current Consumption (mA)	
	0 Touches	1 Touch
Free-run	1	9.2
10	0.3	4.2
16	0.3	3.2
32	0.2	2.1
64	0.2	1.5
100	0.2	1.2
128	0.2	1
254	0.2	0.6



11.5.2 VDDIO

Acquisition Rate (ms)	Current Consumption (mA)	
	0 Touches	1 Touch
Free-run	0.016	0.017
10	0.016	0.016
16	0.016	0.016
32	0.016	0.016
64	0.016	0.016
100	0.016	0.016
128	0.016	0.016
254	0.016	0.016

11.5.3 DEEP SLEEP

Power Monitor On, Sampling mode; $T_A = 25^\circ\text{C}$

Parameter	Value	Units	Notes
Deep Sleep Current	0.3	mA	Vdd = 3.3V VddIO = 3.3V
Deep Sleep Power	1.0	mW	

Power Monitor Off; $T_A = 25^\circ\text{C}$

Parameter	Value	Units	Notes
Deep Sleep Current	0.2	mA	Vdd = 3.3V VddIO = 3.3V
Deep Sleep Power	0.5	mW	

11.6 Timing Specifications

NOTE The figures below show typical values based on the test configuration. Actual timings in the user's application will depend on the circumstances of that particular project and will vary from those shown below. Further tuning will be required to achieve an optimal performance.

11.6.1 TOUCH LATENCY

Mutual Capacitance

Conditions: XSIZE = 4; YSIZE = 7; CHRGTIME = 9;
IDLESYNCSPEX = 8; ACTVSYNCSPEX = 8;
T = ambient temperature; Reporting off (except T500)

T500 TCHDIDOWN	Pipelining Off			Pipelining On			Units
	Min	Typ	Max	Min	Typ	Max	
1	1.6	6.4	11.7	6.6	11.9	16.7	ms

Self Capacitance

Conditions: XSIZE = 12; YSIZE = 12; INTTIME = 27; DELAYTIME = 19;
IDLESYNCSPEX = 24; ACTVSYNCSPEX = 24;
T = ambient temperature; Reporting off (except T500)

T500 TCHDIDOWN	Pipelining Off			Pipelining On			Units
	Min	Typ	Max	Min	Typ	Max	
1	1.5	2.7	3.8	4.5	5.5	6.3	ms

11.6.2 RESET TIMINGS

Parameter	Power-on Features (Typ) ⁽²⁾		Units	Notes
	Disabled	Enabled		
Power on to $\overline{\text{CHG}}$ line low ⁽¹⁾	120	340	ms	Triggered by Vdd supply at start up
Hardware reset to $\overline{\text{CHG}}$ line low ⁽¹⁾	120	360	ms	Triggered by $\overline{\text{RESET}}$
Software reset to $\overline{\text{CHG}}$ line low ⁽¹⁾	140	380	ms	Triggered by Command Processor T6 Reset command

Note 1: Any $\overline{\text{CHG}}$ line activity before the power-on or reset period has expired should be ignored by the host. Operation of this signal cannot be guaranteed before the power-on/reset periods have expired.

Note 2: Power-on features include POST self tests and device encryption. Figures show typical values for extreme cases; that is, with all features disabled and with all features enabled.

11.7 Touch Sensor Characteristics

Parameter	Description	Value
Cm	Mutual capacitance	Typical value is between 1.7 pF and 10 pF on a single node.
Cpx	Mutual capacitance load to X	Microchip recommends a maximum load of 300 pF on each X line. ⁽¹⁾
Cpy	Mutual capacitance load to Y	Microchip recommends a maximum load of 300 pF on each Y line. ⁽¹⁾
Cpx	Self capacitance load to X	Microchip recommends a maximum load of 130 pF on each X or Y line. ⁽¹⁾
Cpy	Self capacitance load to Y	
ΔCpx	Self capacitance imbalance on X	Nominal value is 14.8 pF at 100 pF
ΔCpy	Self capacitance imbalance on Y	Value increases by 1 pF for every 45 pF reduction in Cpx/Cpy (based on 100 pF load)
Cpds0	Self capacitance load to Driven Shield	Microchip recommends a maximum load of 130 pF on the Driven Shield line. ⁽¹⁾

Note 1: Please contact your Microchip representative for advice if you intend to use higher values.

11.8 Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Notes
Input (All input pins connected to the VddIO power rail)						
Vil	Low input logic level	-0.3	—	$0.3 \times \text{VddIO}$	V	VddIO = 1.8 V to Vdd
Vih	High input logic level	$0.7 \times \text{VddIO}$	—	VddIO	V	VddIO = 1.8 V to Vdd
Iil	Input leakage current	—	—	1	μA	
$\overline{\text{RESET}}$	Internal pull-up resistor	9	10	16	k Ω	
GPIOs	Internal pull-up/pull-down resistor	20	40	60	k Ω	
Input (All input pins connected to the Vdd power rail)						
Vil	Low input logic level	-0.3	—	$0.3 \times \text{Vdd}$	V	
Vih	High input logic level	$0.7 \times \text{Vdd}$	—	Vdd	V	
Iil	Input leakage current	—	—	1	μA	Pull-up resistors disabled

Parameter	Description	Min	Typ	Max	Units	Notes
Output (All output pins connected to the VddIO power rail)						
Vol	Low output voltage	0	–	$0.2 \times V_{ddIO}$	V	$V_{ddIO} = 1.8 \text{ V to } V_{dd}$ $I_{ol} = \text{max } 0.4 \text{ mA}$
Voh	High output voltage	$0.8 \times V_{ddIO}$	–	V_{ddIO}	V	$V_{ddIO} = 1.8 \text{ V to } V_{dd}$ $I_{oh} = 0.4 \text{ mA}$
Output (All output pins connected to the Vdd power rail)						
Vol	Low output voltage	0	–	$0.2 \times V_{dd}$	V	$I_{ol} = \text{max } 0.4 \text{ mA}$
Voh	High output voltage	$0.8 \times V_{dd}$	–	V_{dd}	V	$I_{oh} = 0.4 \text{ mA}$

11.9 I²C Specification

Parameter	Value
Address	0x3A
I ² C specification ⁽¹⁾	Revision 7.0
Maximum bus speed (SCL) ⁽²⁾	1 MHz
Standard Mode ⁽³⁾	100 kHz
Fast Mode ⁽³⁾	400 kHz
Fast Mode Plus ⁽³⁾	1 MHz

- Note 1:** More detailed information on I²C operation is available from UM10204, *I²C bus specification and user manual*, available from NXP.
- Note 2:** In systems with heavily laden I²C lines, even with minimum pull-up resistor values, bus speed may be limited by capacitive loading to less than the theoretical maximum.
- Note 3:** The values of pull-up resistors should be chosen to ensure SCL and SDA rise and fall times meet the I²C specification. The value required will depend on the amount of capacitance loading on the lines.

11.10 Firmware Authentication

Operation	Typical	Unit
T6 Reset command to bootloader command mode	33.04	ms
Receive authentication parameters from system host	10.4	μs
Process single 64-byte flash block in device	867.32	μs
Process Bootloader segment	61.75	ms
Process Firmware Application segment	794	ms
Process NVM segment	12.7	ms
Host reads signature (I ² C at 600 kbps)	1.5	ms

11.11 Thermal Packaging

11.11.1 THERMAL DATA

Parameter	Description	Typ	Unit	Condition	Package
θ_{JA}	Junction to ambient thermal resistance	43.9	°C/W	Still air	38-pin XQFN 4 × 4 × 0.35 mm
θ_{JC}	Junction to case thermal resistance	14.0	°C/W		38-pin XQFN 4 × 4 × 0.35 mm

11.11.2 JUNCTION TEMPERATURE

The maximum junction temperature allowed on this device is 125°C.

The average junction temperature in °C (T_J) for this device can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA})$$

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If a cooling device is required, use this equation:

$$T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$$

where:

- θ_{JA} = package thermal resistance, Junction to ambient (°C/W) (see [Section 11.11.1 “Thermal Data”](#))
- θ_{JC} = package thermal resistance, Junction to case thermal resistance (°C/W) (see [Section 11.11.1 “Thermal Data”](#))
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the cooling device datasheet
- P_D = device power consumption (W)
- T_A is the ambient temperature (°C)

11.12 ESD Information

Parameter	Value	Reference Standard
Human Body Model (HBM)	±2000V	JEDEC JS-001
Charge Device Model (CDM)	±250V	JEDEC JS-002

11.13 Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150 – 200°C
Time Maintained Above 217°C	60 – 150 seconds
Time within 5°C of Actual Peak Temperature	30 seconds
Peak Temperature Range	260°C
Ramp down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

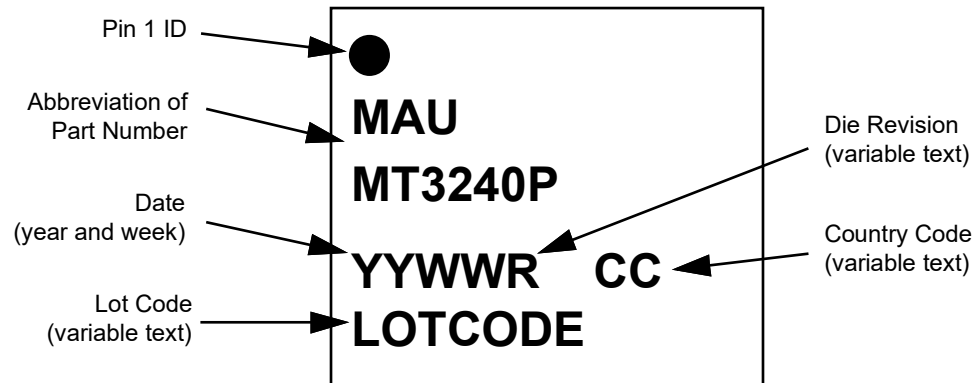
11.14 Moisture Sensitivity Level (MSL)

MSL Rating	Package Type(s)	Peak Body Temperature	Specifications
MSL3	38-pin XQFN	260°C	IPC/JEDEC J-STD-020

12.0 PACKAGING INFORMATION

12.1 Package Marking Information

12.1.1 38-PIN XQFN



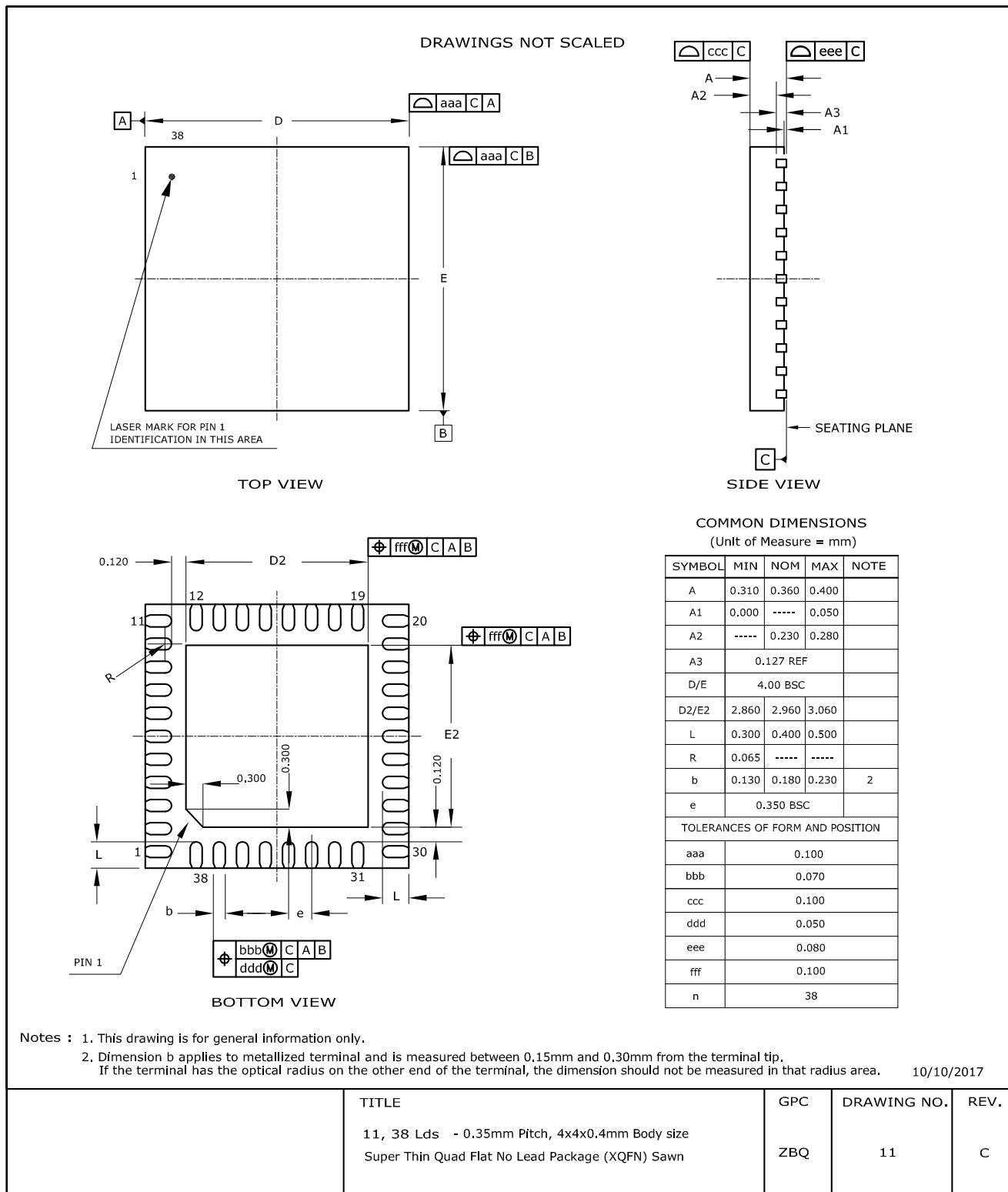
12.1.2 ORDERABLE PART NUMBERS

The product identification system for MTCH devices is described in [“Product Identification System” on page 59](#). That section also lists example part numbers for the MTCH3240P device.

MTCH3240P

12.2 Package Details

12.2.1 38-PIN XQFN 4 × 4 × 0.35 MM



APPENDIX A: ASSOCIATED DOCUMENTS

Microchip MTCH Web Site

For general information on the MTCH3240P, please visit the following:

- <https://www.microchip.com/en-us/product/MTCH3240P>

Microchip Documents

The following documents are available on the Microchip website.

Sensor Design and PCB/FPCB Layout Guidelines

- Application Note: AN6564 – *Design Guide for PCB Layouts for MTCH Touch Controllers*
- Application Note: AN2934 – *Capacitive Touch Sensor Design*

Configuring and Tuning the Device

- Application Note: AN6566 – *Interfacing with MTCH Touchscreen Controllers*

Tools Documentation

- *MTCH Studio User Guide* (accessible as help pages from within MTCH Studio)

External Documents

The following documents are not supplied by Microchip. To obtain any of the following documents, please contact the relevant organization.

Standards

- IEC 60730-1, *Automatic electrical controls – Part 1: General requirement*, Edition 5.1, 2015-12
- UL 60730-1, *Automatic Electrical Controls – Part 1: General Requirements*, Edition 5, 2016-08-03

Communication Interface

- UM10204, *I²C bus specification and user manual*, Rev. 7.0 — 1 October 2021
Available from NXP

APPENDIX B: REVISION HISTORY

Revision A (August 2026)

Initial edition for firmware revision 1.0.AA – Release

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PRODUCT IDENTIFICATION SYSTEM

The table below gives details on the product identification system for MTCH devices. See [“Orderable Part Numbers”](#) below for example part numbers for the MTCH3240P.

To order or obtain information, for example on pricing or delivery, refer to the factory or the listed sales office.

<u>PART-NO.</u>	<u>-XXX</u>	<u>X</u>	<u>[X]</u>	<u>[XXX]</u>
Device	Package	Temperature Range	Tape and Reel Option	Pattern
Device:	Base device name			
Package:	MA	=	XQFN (Super Thin Quad Flat No Lead Sawn)	
	MA5	=	XQFN (Super Thin Quad Flat No Lead Sawn)	
Temperature Range:	U	=	–40°C to +105°C (Grade 2)	
Tape and Reel Option: ⁽¹⁾	Blank	=	Standard Packaging (Tube or Tray)	
	R	=	Tape and Reel	
Pattern:	Text	=	Extension, Version, Code or Special Requirements (Blank Otherwise)	

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. See [“Orderable Part Numbers”](#) below or check with your Microchip Sales Office for package availability with the Tape and Reel option.

Orderable Part Numbers

Orderable Part Number	Firmware Revision	Family ID	Variant ID	Description
MTCH3240P-MAU001 (Supplied in trays)	1.0.AA	0xA9	0x01	38-pin XQFN 4 × 4 × 0.35 mm, RoHS compliant Industrial grade; not suitable for automotive characterization
MTCH3240P-MAUR001 (Supplied in tape and reel)				

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Datasheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

For information on the MTCH3240P, visit <https://www.microchip.com/en-us/product/MTCH3240P>.

THE MTCH WEB SITE

Information on Microchip's MTCH product line can be accessed via the microchip web site at www.microchip.com.

The MTCH web pages contain the following information:

- **Product Information** – Product specifications, brochures, datasheets, protocol guides
- **Tools and Software** – Evaluation kits, MTCH Studio, software libraries for individual MTCH touch controllers
- **Training and Support** – Generic application notes and training material for the MTCH product range

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CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers.

Technical support is available through the web site at: <http://microchip.com/support>

NOTES:

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