

Features

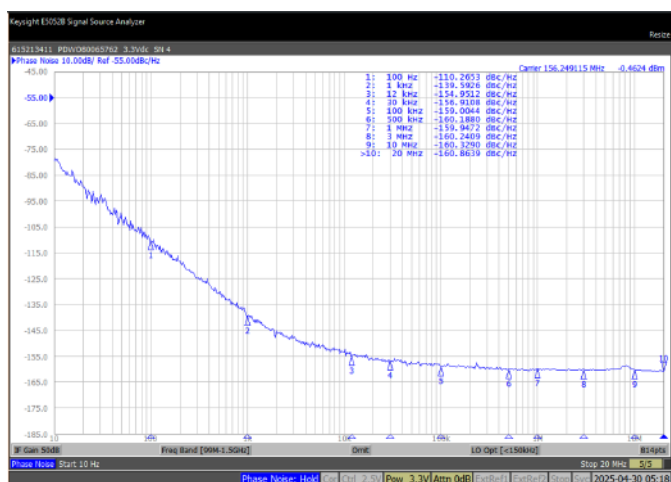
- 3.2mm × 2.5mm surface-mount package
- TID: 50krad (Si) Total Ionizing Dose (TID)
- Single Event Latchup (SEL): 40MeV-cm²/mg
- MIL-PRF-55310 Class B-Screening option
- CMOS frequency range of 1.25MHz to 135MHz
- LVDS frequency range of 100MHz to 250MHz
- Operating temperature range of -55°C to +125°C



Applications

- New Space Programs
- LEO Constellations
- Cube Satellites
- Small Satellites
- Broadband Internet, Earth Observation, Tracking

Figure 1-2. LX-820: 156.25MHz, LVDS Output, 3.3V - Typical Performance



Phase Noise to Jitter Calculation

i	Offset Frequency (Hz)	Phase Noise L(f) (dBc/Hz)	Phase Jitter per segment (ps rms)
1	100	-110	
2	1,000	-139	0.033
3	12,000	-154	0.006
4	30,000	-156	0.003
5	100,000	-159	0.005
6	500,000	-160	0.010
7	1,000,000	-159	0.011
8	3,000,000	-160	0.021
9	10,000,000	-160	0.038
10	20,000,000	-160	0.046
11			
12			
13			
14			
15			
Total Jitter =			0.073

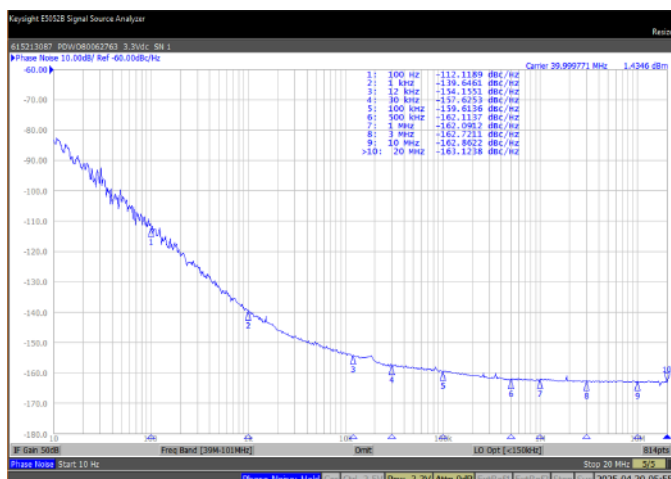
+25°C at
3.3Vdc

(Root Sum-of-Squares)

Fc	156.25	MHz
BW	12,000	Hz
BW Jitter	0.065	ps rms

<-- Enter Carrier Frequency
<-- Enter Offset Frequency 1
<-- Enter Offset Frequency 2

Figure 1-3. LX-820: 40MHz, CMOS Output, 3.3V - Typical Performance



Phase Noise to Jitter Calculation

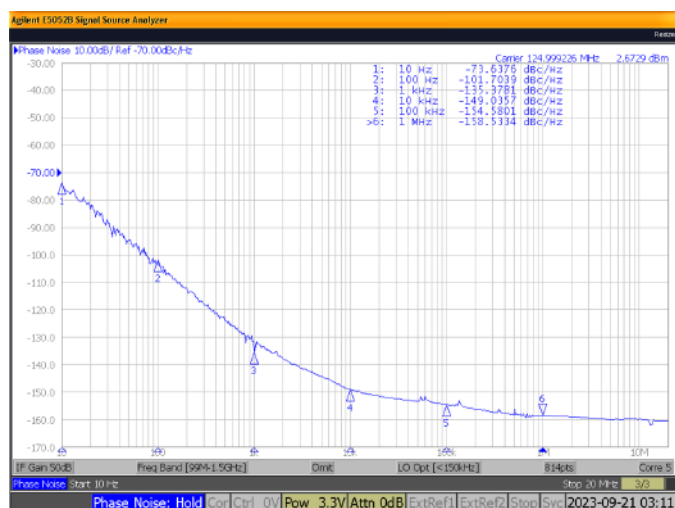
i	Offset Frequency (Hz)	Phase Noise L(f) (dBc/Hz)	Phase Jitter per segment (ps rms)
1	100	-109	
2	1,000	-137	0.148
3	12,000	-154	0.029
4	50,000	-160	0.015
5	100,000	-160	0.013
6	500,000	-162	0.031
7	1,000,000	-162	0.032
8	3,000,000	-163	0.059
9	10,000,000	-162	0.113
10	20,000,000	-162	0.141
11			
12			
13			
14			
15			
Total Jitter =			0.247

(Root Sum-of-Squares)

Fc	40	MHz
BW	12,000	Hz
BW Jitter	0.196	ps rms

<-- Enter Carrier Frequency
<-- Enter Offset Frequency 1
<-- Enter Offset Frequency 2

Figure 1-4. LX-820: 125MHz, CMOS Output, 3.3V - Typical Performance



Phase Noise to Jitter Calculation

i	Offset Frequency (Hz)	Phase Noise L(f) (dBc/Hz)	Phase Jitter per segment (ps rms)
1	100	-104	
2	1,000	-132	0.084
3	12,000	-150	0.016
4	50,000	-153	0.009
5	100,000	-155	0.008
6	500,000	-158	0.016
7	1,000,000	-158	0.016
8	3,000,000	-159	0.030
9	10,000,000	-161	0.047
10	20,000,000	-162	0.048
11			
12			
13			
14			
15			
Total Jitter =			0.115 (Root Sum-of-Squares)

Fc	125	MHz	<-- Enter Carrier Frequency
BW	12,000	Hz	<-- Enter Offset Frequency 1
	20,000,000	Hz	<-- Enter Offset Frequency 2
BW Jitter	0.078	ps rms	

Table 1-6. Additional Parameters

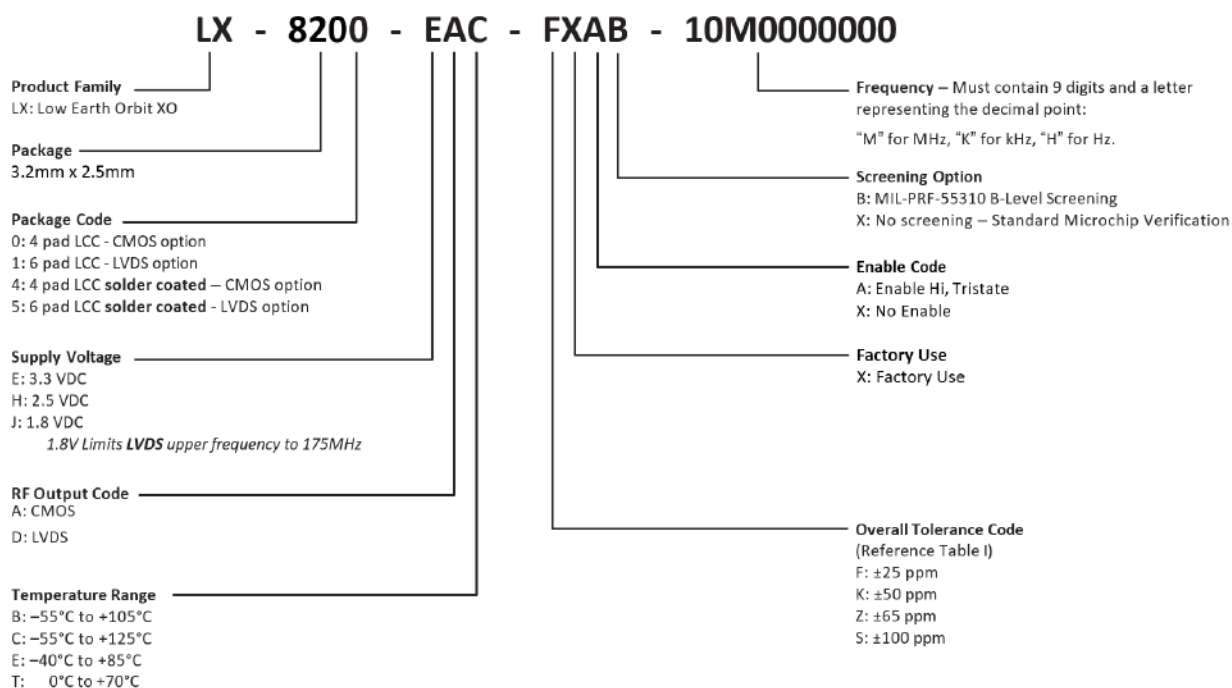
Parameter	Conditions	Additional Notes
Screening	Microchip Verification (Standard "X")	See the following table for Tests
	Class B, MIL-PRF-55310 (Optional)	See the following table for Tests
Output Enable	Logic "0" input == Output disabled (Tri-state)	—
	Logic "1" or floating input == Output enabled	
Weight	< 2 grams	—
Processing and Packing	Tape and Reel	—
RoHS Compliance	RoHS 6	Unless Sn/Pb solder coated
REACH Compliance	Yes	—
Solder Coated Pads	Sn63/Pb37 Solder (Optional)	See Package Code in Part Number
Moisture Sensitivity Level (MSL)	1	Ceramic package, Seam sealed
MTBF/FIT (Generic)	480,000,000 Hours	MIL-HBK-217, Hybrid, Space Flight, Commercial Contact Factory for Custom MTBF/FIT
ECCN	EAR99	—
Software 3D Model	IGS/STEP file	Contact VOP-Support@microchip.com

Table 1-7. Standard Microchip Verification "X" in Screening Option

Test	Test Conditions
Internal Visual Inspection	MIL-STD-883, Methods 2017, 2032
Stabilization Bake	MIL-STD-883, Method 1008, Condition C, 150°C, 24 hours minimum
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
High-Temperature Reflow	2 cycles of solder reflow profile, SnPb Standard, See Section 4 for profile
Seal Test (Fine Leak)	MIL-STD-883, Method 1014, Condition A2, Class B
Seal Test (Gross Leak)	MIL-STD-883, Method 1014, Condition C

2. Product Identification System

Figure 2-1. Ordering Information



Note: The full part number does not have spaces and should contain dashes as indicated.

Example 1: LX-8200-EAC-FXAB-10M0000000

Table 2-1. Overall Tolerance Codes

Table I: Overall Tolerance Code	
Temperature Range	Overall Tolerance
C: -55°C to +125°C	Z: ±65ppm
	S: ±100ppm
B: -55°C to +105°C E: -40°C to +85°C	K: ±50ppm
	Z: ±65ppm
	S: ±100ppm
T: 0°C to +70°C	F: ±25ppm
	K: ±50ppm
	Z: ±65ppm
	S: ±100ppm

3. Packaging Information

CMOS Package

Figure 3-1. CMOS Package Outline/Enclosure

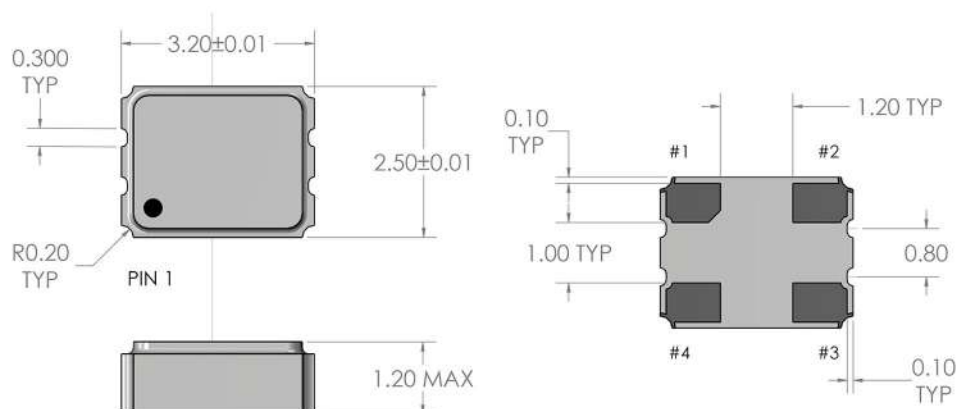


Table 3-1. Type LCC (CMOS)

Package Code	Length "L"	Width "W"	Height "H"
0	3.2mm ±0.2mm	2.5mm ±0.2mm	1.2mm max.

Table 3-2. CMOS Pin Connections

Pin Number	Pin Description
1	Enable/Disable or N/C <i>Output active = Floating or Voltage Applied</i>
2	Ground (Case)
3	RF Output
4	Supply

Note: Package standard termination finish: Au 12-39 microinches over Nickel 50 microinches minimum.

➔ Important: Overall package thickness **tolerance** will be increased from ± 0.007 to ± 0.015 inches when pads are solder coated.

LVDS Package

Figure 3-2. LVDS Package Outline/Enclosure

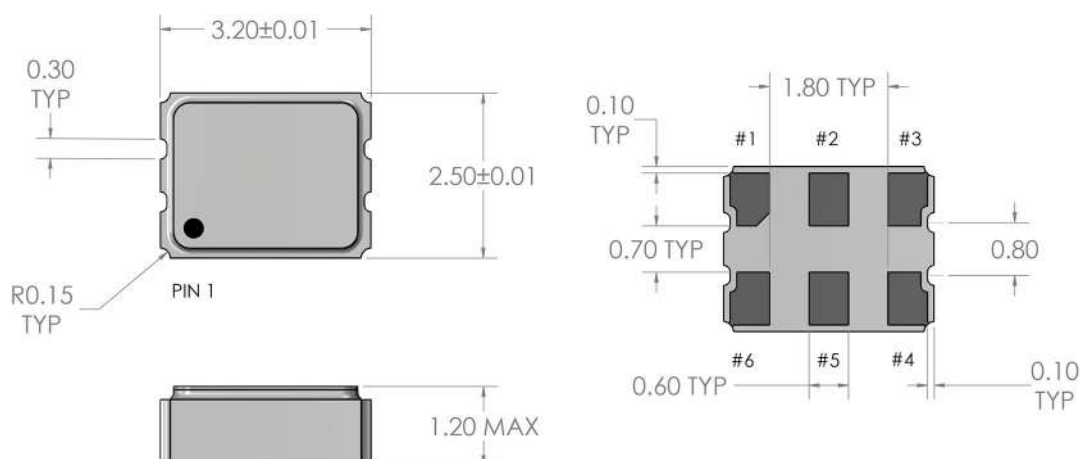


Table 3-3. Type LCC (LVDS)

Package Code	Length "L"	Width "W"	Height "H"
1	3.2mm ±0.2mm	2.5mm ±0.2mm	1.2mm max.

Table 3-4. Pin Connections

Pin Number	Pin Description
1	Enable/Disable or N/C <i>Output active = Floating or Voltage Applied</i>
2	N/C
3	Ground (Case)
4	LVDS+
5	LVDS-
6	Supply

Note: Package standard termination finish: Au 12-39 microinches over Nickel 50 microinches minimum.

➔ Important: Overall package thickness **tolerance** will be increased from ±.007 to ±.015 inches when pads are solder coated.

4. Recommended Reflow Profiles

Figure 4-1. Recommended Reflow Profiles for Pb-Free and Sn-Pb

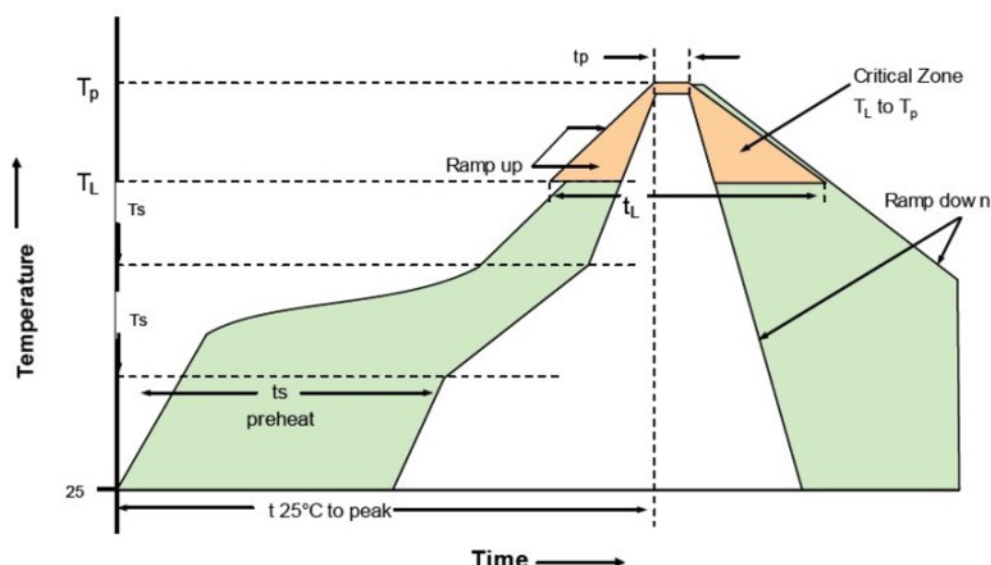


Table 4-1. 230°C Reflow Profile

All temperatures refer to top side of the package, measured on the package body surface.

Profile Feature	Sn-Pb Assembly	Profile Feature	Sn-Pb Assembly
Average ramp-up rate (t_L to t_P)	3°C/second max.	Time 25°C to Peak Temperature	4 minutes max.
Preheat		Time maintained above Temperature (T_L)	183°C
Temperature min. $T_{S(MIN)}$	135°C	Time (t_L)	45-60 seconds
Temperature min. $T_{S(MAX)}$	155°C		
Time (min. to max.) (t_S)	60-90 seconds		
$T_{S(MAX)}$ to T_L ramp-up rate	3°C/second max.	—	—
Time maintained above Temperature (T_L)	183°C	Time within 5°C of actual Peak Temperature (t_P)	10-20 seconds max.
Time (t_L)	40-60 seconds		
Peak Temperature (T_P)	230°C max.	Ramp-down Rate	6°C/second max.

Table 4-2. 260°C Reflow Profile

All temperatures refer to top side of the package, measured on the package body surface.

Profile Feature	Pb-Free Assembly	Profile Feature	Pb-Free Assembly
Average ramp-up rate (t_L to t_P)	3°C/second max.	Time 25°C to Peak Temperature	8 minutes max.
Preheat		Time maintained above Temperature (T_L)	217°C
Temperature min. $T_{S(MIN)}$	150°C	Time (t_L)	60-150 seconds
Temperature min. $T_{S(MAX)}$	200°C		
Time (min. to max.) (t_S)	60-180 seconds		
$T_{S(MAX)}$ to T_L ramp-up rate	3°C/second max.	—	—
Time maintained above Temperature (T_L)	217°C	Time within 5°C of actual Peak Temperature (T_P)	20-40 seconds max.
Time (t_L)	60-150 seconds		
Peak Temperature (T_P)	260°C max.	Ramp-down Rate	6°C/second max.