LPS27DEWO

Datasheet

Dual full-scale, 1260 hPa and 6060 hPa, absolute digital output barometer in a water-resistant package

LGA-11L
2.7 x 2.7 x 1.85 mm

Product status link
LPS27DEWO

Product summary	
Order code	LPS27DEWOTR
Temperature range [°C]	-40 to +85
Package	LGA-11L
Packing	Tape and reel

Product resources
AN6516 (device application note)
AN6541 (guidelines for system integration)
TN0018 (handling, mounting, and soldering guidelines)

Features

- Dual full-scale absolute pressure sensor in a water-resistant package
  - Mode 1: 260 ~ 1260 hPa
  - Mode 2: 260 ~ 6060 hPa
- Supply current down to 1.7 µA
- Absolute pressure accuracy: 0.3 hPa
- Low pressure sensor noise: 0.32 Pa
- Embedded temperature compensation
- 24-bit pressure data output
- ODR from 1 Hz to 200 Hz
- SPI, I²C, or MIPI I3C® interface
- Embedded FIFO
- Interrupt functions: data-ready, FIFO flags, pressure thresholds
- Supply voltage: 1.7 to 3.6 V and 1.2 V VDDIO
- Easily sealed package with O-ring
- ECOPACK lead-free compliant

Applications

- Wearables
- Altimeters and barometers for portable devices
- GPS applications
- Weather station equipment
- Sport watches
- e-cigarettes
- Water depth monitoring

Description

The LPS27DEWO is an ultracompact piezoresistive absolute pressure sensor that functions as a digital output barometer. The device comprises a sensing element and a digital interface, which communicates over the I²C, MIPI I3C®, or SPI interface from the sensing element to the application. The LPS27DEWO provides lower power consumption, achieving lower pressure noise than its predecessor.

The LPS27DEWO is available in an LGA package with a metal lid. It is guaranteed to operate over a temperature range extending from -40°C to +85°C. The package is holed to allow external pressure to reach the sensing element. Gel inside the IC protects the electrical components from water and the metal cap is, optionally, connected to ground or left floating electrically in the application PCB layout. The connection of the metal cap is determined according to the customer's target application.

This device has been designed to meet the requirements and mission profile for personal electronics and consumer applications.

1 Block diagrams

Figure 1. Device architecture block diagram

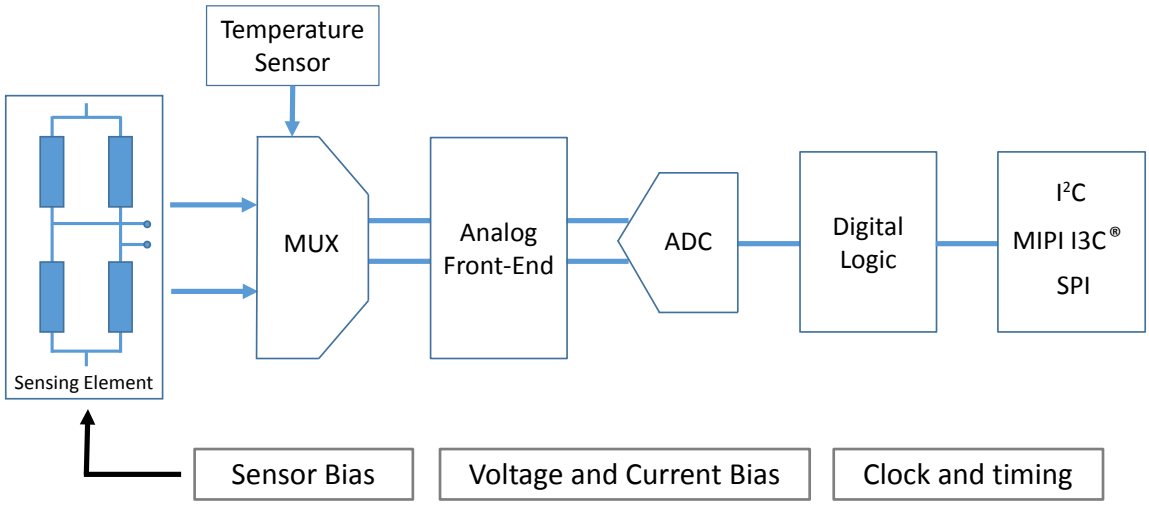
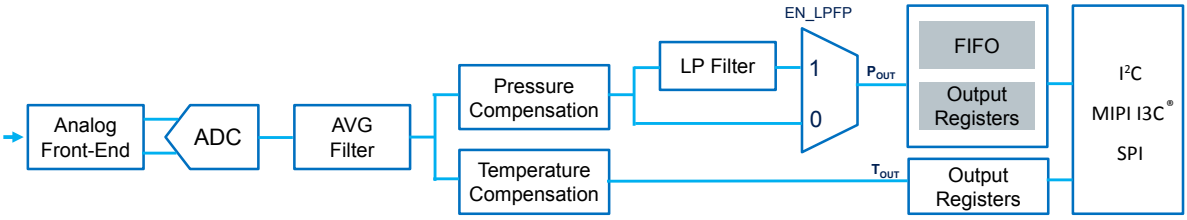


Figure 2. Digital logic



2 Pin description

Figure 3. Pin connections (bottom view)

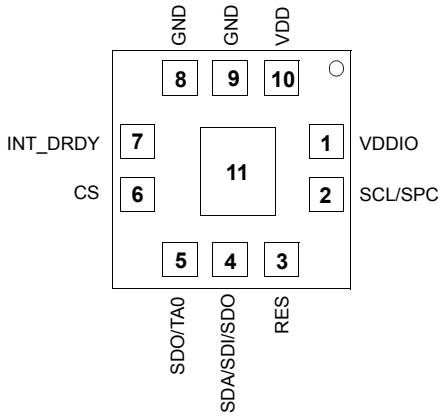


Table 1. Pin description

Pin number	Name	Function
1	VDDIO	Power supply for I/O pins
2	SCL SPC	I²C / MIPI I3C® serial clock (SCL) SPI serial port clock (SPC)
3	RES	Connect to GND
4	SDA SDI SDI/SDO	I²C / MIPI I3C® serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input/output (SDI/SDO)
5	SDO TA0	4-wire SPI serial data output (SDO) I²C least significant bit of the device address (TA0) MIPI I3C® least significant bit of the static address (TA0)
6	CS	Enables SPI I²C and MIPI I3C® / SPI mode selection (1: SPI idle mode / I²C and MIPI I3C® communication enabled; 0: SPI communication mode / I²C and MIPI I3C® disabled)
7	INT_DRDY	Interrupt or data-ready
8	GND	0 V supply
9	GND	0 V supply
10	VDD	Power supply
11	PAD2LID	Pad connection to metal lid

3 Mechanical and electrical specifications

3.1 Mechanical characteristics

VDD = 1.8 V, T = 25°C, unless otherwise noted.

Table 2. Pressure and temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
Pressure sensor characteristics						
PT_{op}	Operating temperature range		-40		+85	°C
P_{op}	Operating pressure range Mode 1 Mode 2		 260 260		 1260 6060	hPa
P_{bits}	Pressure output data			24		bits
P_{sens}	Pressure sensitivity Mode 1 Mode 2			 2700 1350		LSB/hPa
P_{AccRel}	Relative pressure accuracy[2] Mode 1 Mode 2	T =25°C P = 800 ~ 1100 hPa P= 2060 ~ 6060 hPa		 ±0.02 ±1		hPa
P_{AccT}	Absolute pressure accuracy Mode 1 Mode 2 Refer to Table 3 for more details.	T = 0 ~ 65°C P = 860 ~ 1160 hPA P = 260 ~ 1260 hPA T = 0 ~ 45°C P = 1260 ~ 6060 hPA		 ±0.3 ±0.7 ±0.5%[3]		hPa
P_{noise}	RMS pressure noise[4] Mode 1 Mode 2 Refer to Table 23 for more details.	T = 25°C		 0.32 0.6		Pa
ODR_{Pres}	Pressure output data rate			1 4 10 25 50 75 100 200		Hz
P_longterm	Pressure accuracy, long-term stability[5]			±0.2		hPa/year
P_drift	Soldering drift	drift after 4h soldering		±1		hPa
Temperature sensor characteristics						
T_{op}	Operating temperature range		-40		+85	°C
T_{sens}	Temperature sensitivity			100		LSB/°C

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
T_{acc}	Temperature absolute accuracy	T = 25 to 65°C		±1.5		°C
ODR_T	Output temperature data rate			1 4 10 25 50 75 100 200		Hz

1. *Typical specifications are not guaranteed.*
2. *The typ. value is defined based on characterization data with 10 hPa pressure interval in mode 1 and 100 hPa pressure interval in mode 2.*
3. *With extra nonlinear compensation*
4. *Pressure noise RMS evaluated in a controlled environment, based on the average standard deviation of 50 measurements with AVG = 512, BW = ODR/9.*
5. *Typ. value based on HTOL 1000 hr reliability test result.*

Table 3. Absolute pressure accuracy at different full-scale modes

Full-scale mode	Condition	Typ. absolute pressure accuracy [hPa]
Mode 1 (full scale up to 1260 hPa)	P = 860 ~ 1160 & T = 0 ~ 65°C	±0.3 hPa
Mode 2 (full scale up to 6060 hPa)[1]	P = 1260 ~ 2060 & T = 0 ~ 45°C	±0.1% of input pressure
	P = 2060 ~ 3060 & T = 0 ~ 45°C	±0.2% of input pressure
	P = 3060 ~ 4060 & T = 0 ~ 45°C	±0.3% of input pressure
	P = 4060 ~ 5060 & T = 0 ~ 45°C	±0.4% of input pressure
	P = 5060 ~ 6060 & T = 0 ~ 45°C	±0.5% of input pressure

1. *Typ. absolute pressure accuracy is considered with extra nonlinear compensation.*

3.2 Electrical characteristics

VDD = 1.8 V, T = 25°C, unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
VDD	Supply voltage		1.7		3.6	V
VDDIO	I/O supply voltage		1.08		3.6	V
Idd	Supply current Refer to Table 22 for more information.	AVG = 4 and ODR = 1 Hz		1.7		µA
		AVG = 128 and ODR = 1 Hz		9.4		
IddPdn	Supply current in power-down mode			0.9		µA

1. *Typical specifications are not guaranteed.*

Table 5. DC characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC input characteristics						
Vil	Low-level input voltage (Schmitt buffer)	VDDIO ≥ 1.8 V (typ)	-	-	0.3 * VDDIO	V
		VDDIO = 1.2 V (typ)	-	-	0.2 * VDDIO	
Vih	High-level input voltage (Schmitt buffer)	VDDIO ≥ 1.8 V (typ)	0.7 * VDDIO	-	-	V
		VDDIO = 1.2 V (typ)	0.8 * VDDIO	-	-	
DC output characteristics						
Vol	Low-level output voltage		-	-	0.2	V
Voh	High-level output voltage		VDDIO - 0.2	-	-	V

3.3 Communication interface characteristics

3.3.1 I²C - inter-IC control interface

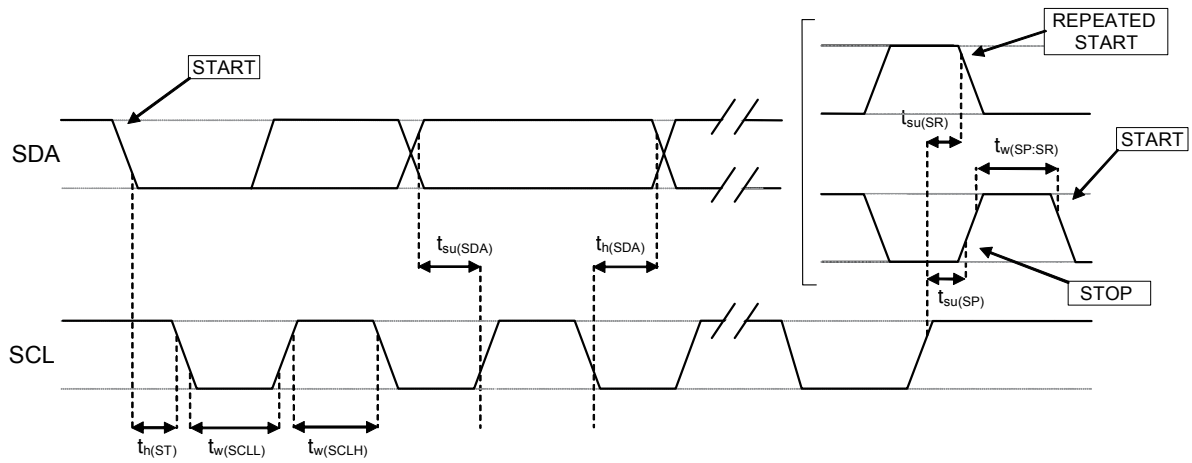
Subject to general operating conditions for VDD and T_{OP}.

Table 6. I²C target timing values

Symbol	Parameter	I²C fast mode(1)(2)		I²C fast mode+(1)(2)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	400	0	1000	kHz
$t_{w(SCLL)}$	SCL clock low time	1.3		0.5		µs
$t_{w(SCLH)}$	SCL clock high time	0.6		0.26		
$t_{su(SDA)}$	SDA setup time	100		50		ns
$t_{h(SDA)}$	SDA data hold time	0	0.9	0		µs
$t_{h(ST)}$	START/REPEATED START condition hold time	0.6		0.26		
$t_{su(SR)}$	REPEATED START condition setup time	0.6		0.26		
$t_{su(SP)}$	STOP condition setup time	0.6		0.26		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	1.3		0.5		
	Data valid time		0.9		0.45	
	Data valid acknowledge time		0.9		0.45	
C_B	Capacitive load for each bus line		400		550	pF

1. *Data based on standard I²C protocol requirements, not tested in production.*
2. *Data for I²C fast mode and I²C fast mode+ have been validated by characterization, not tested in production.*

Figure 4. I²C target timing diagram



Note: Measurement points are done at 0.3·VDDIO and 0.7·VDDIO for both ports.

3.3.2 SPI - serial peripheral interface

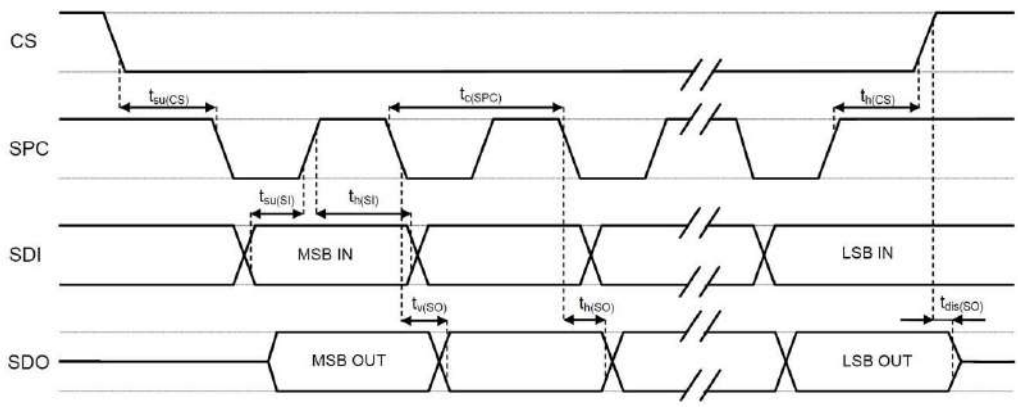
Subject to general operating conditions for VDD and T_{OP}.

Table 7. SPI target timing values

Symbol	Parameter	Value[1]		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10[2]	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. *Values are evaluated at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.*
2. *Recommended to set max SPI clock 8 MHz to ≤50 Hz ODR.*

Figure 5. SPI target timing diagram



Note: Measurement points are done at 0.3·VDDIO and 0.7·VDDIO for both ports.

3.4 Absolute maximum ratings

Stress above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximumvalue	Unit
VDD	Supply voltage	-0.3 to +4.8	V
VDDIO	I/O pins supply voltage	-0.3 to +4.8	V
Vin	Input voltage on any control pin	-0.3 to VDDIO +0.3	V
P_{water}	Overpressure[1]	1.25	MPa
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

1. *Based on characterization result of 12.5 bar pressure for 2hr.*

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4 Functionality

The LPS27DEWO is a high-resolution, digital output pressure sensor packaged in an LGA package with metal lid. The complete device includes a sensing element based on a piezoresistive Wheatstone bridge approach and an IC interface which communicates a digital signal from the sensing element to the application.

4.1 Sensing element

An ST proprietary process is used to obtain a silicon membrane for MEMS pressure sensors. When pressure is applied, the membrane deflection induces an imbalance in the Wheatstone bridge piezoresistances whose output signal is converted by the IC interface.

4.2 IC interface

The complete measurement chain is composed of a low-noise amplifier which converts the resistance unbalance of the MEMS sensors (pressure and temperature) into an analog voltage using an analog-to-digital converter.

The pressure and temperature data may be accessed through an I²C/MIPI I3C®/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LPS27DEWO features a data-ready signal which indicates when a new set of measured pressure and temperature data are available, thus simplifying data synchronization in the digital system that uses the device.

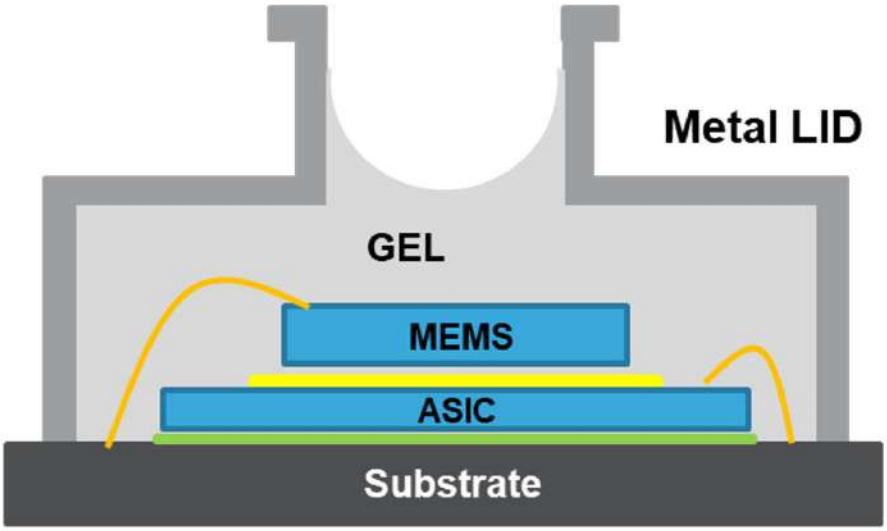
4.3 Factory calibration

The trimming values are stored inside the device in a non-volatile structure. When the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation which allows the device to be used without requiring any further calibration.

4.4 Device structure

The LPS27DEWO has a unique cylindrical package solution with a full metal lid assembled on a substrate and this cylindrical package provides an easy assembly with O-rings in the end user's application.

Figure 6. LPS27DEWO internal structure



This structure (Figure 6) is designed and verified to resist water pressure up to 12.5 Bar and the potting gel in the LPS27DEWO has been proven to protect electronic components from long-term exposure to harsh environments such as water mixed with chlorine, bromine, or commercial washing detergent. Based on potting gel properties, it has also robustness to fuels, solvents, and chemical compounds. It also provides excellent low-stress encapsulation performance for sensitive electronic components from severe environmental conditions such as high temperature and humidity, refer to the properties of the gel, which are given in the following table.

Table 9. Potting gel properties

Properties	Potting gel
Permeability g/m²·24 hr	7
Hardness (penetration) based on ASTM D1403	70
Ultra-low Young's modulus	Less than 0.01 GPa
TCE (thermal coefficient of expansion)	300 ppm/°C

4.5 Interpreting pressure readings

The pressure data are stored in three registers: PRESS_OUT_H (2Ah), PRESS_OUT_L (29h), and PRESS_OUT_XL (28h). The value is expressed as a 24-bit signed number (in two's complement).

To obtain the pressure in hPa, take the complete 24-bit word and then divide by the sensitivity 2700 LSB/hPa when the FS_MODE bit is 0 (in mode 1, full scale is up to 1260 hPa) or divide by the sensitivity 1350 LSB/hPa when the FS_MODE bit is 1 (in mode 2, full scale is up to 6060 hPa). This same interpretation is applied to pressure readings when FIFO is enabled and the pressure data are stored in three registers: FIFO_DATA_OUT_PRESS_XL (78h), FIFO_DATA_OUT_PRESS_L (79h), and FIFO_DATA_OUT_PRESS_H (7Ah).

Figure 7. Pressure readings

PRESS_OUT_H								PRESS_OUT_L								PRESS_OUT_XL							
0	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	0	0	0	1	1	0	1

$$Pressure\ Value = PRESS_OUT_H(2Ah)\ \&\ PRESS_OUT_L(29h)\ \&\ PRESS_OUT_XL(28h) = 30F58Dh = 3208589\ LSB\ (signed\ decimal) \quad (1)$$

(2)

When FS_MODE bit = 0, (CTRL_REG2 (11h)) for full scale up to 1260 hPa:

$$Pressure\ (hPA) = \frac{Pressure\ value\ (LSB)}{Sensitivity} = \frac{3208589\ LSB}{2700\ LSB/hPA} = 1188.3\ hPA$$

When FS_MODE bit = 1, (CTRL_REG2 (11h)) for full scale up to 6060 hPa:

$$Pressure\ (hPA) = \frac{Pressure\ value\ (LSB)}{Sensitivity} = \frac{3208589\ LSB}{1350\ LSB/hPA} = 2376.7\ hPA$$

4.6 Nonlinearity compensation of pressure sensor after reading data

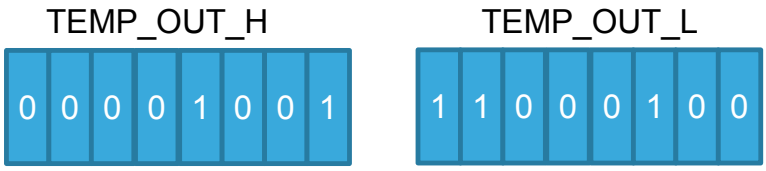
The LPS27DEWO disables the nonlinearity embedded compensation as the default setting and needs to use additional software nonlinearity compensation, which is provided in the reference driver to achieve precise pressure accuracy, covering the extended full scale up to 6060 hPa (refer to application note AN6516.

4.7 Interpreting temperature readings

The temperature data are stored in two registers: TEMP_OUT_H (2Ch) and TEMP_OUT_L (2Bh).

The value is expressed as two's complement. To obtain the temperature in °C, take the two's complement of the complete 16-bit word and then divide by the sensitivity 100 LSB/°C.

Figure 8. Temperature readings



$$\text{Temperature value (LSB)} = \text{TEMP_OUT_H (2Ch) \& TEMP_OUT_L (2Bh)}$$
$$= \text{09C4} = 2500 \text{ LSB (decimal signed)}$$

$$\text{Temperature (°C)} = \frac{\text{Temperature value (LSB)}}{\text{Sensitivity}} = \frac{2500 \text{ LSB}}{100 \text{ LSB/°C}} = 25.00\text{°C}$$

5 FIFO

The LPS27DEWO embeds 128 slots of 24-bit data FIFO to store the pressure output values. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to six different modes:

- Bypass mode
- FIFO mode
- Continuous (dynamic-stream) mode
- Continuous (dynamic-stream)-to-FIFO mode
- Bypass-to-continuous (dynamic-stream)
- Bypass-to-FIFO mode

The FIFO buffer is enabled when a configuration different from all bits 0 are written in FIFO_CTRL (14h) and each mode is selected by the TRIG_MODES bit and F_MODE[1:0] bits in FIFO_CTRL (14h). Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the FIFO_STATUS1 (25h) and FIFO_STATUS2 (26h) registers and can be set to generate dedicated interrupts on the INT_DRDY pin using the CTRL_REG3 (12h) register.

FIFO_STATUS2 (26h)(FIFO_WTM_IA) goes to 1 when the number of unread samples (FIFO_STATUS1 (25h) (FSS[7:0]) is greater than or equal to WTM[6:0] in FIFO_WTM (15h). If FIFO_WTM (15h)(WTM[6:0]) is equal to 0, FIFO_STATUS2 (26h)(FIFO_WTM_IA) stays at 0.

FIFO_STATUS2 (26h)(FIFO_OVR_IA) is equal to 1 if a FIFO slot is overwritten.

FIFO_STATUS1 (25h)(FSS[7:0]) contains stored data levels of unread samples; when FSS[7:0] is equal to 00000000, FIFO is empty; when FSS[7:0] is equal to 10000000, FIFO is full and the unread samples are 128.

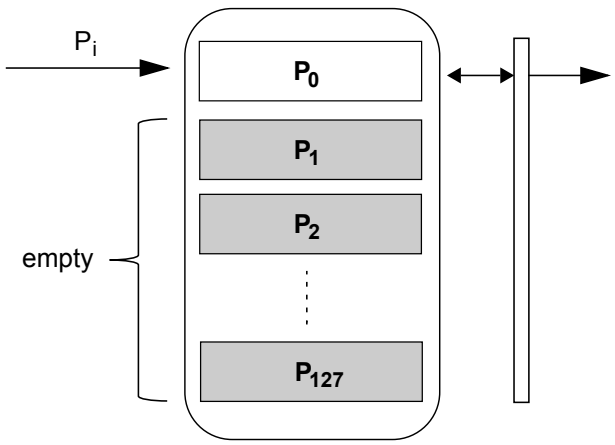
5.1 Bypass mode

In bypass mode (FIFO_CTRL (14h)(TRIG_MODES and F_MODE[1:0] = 000 or 100), the FIFO is not operational and it remains empty.

Switching to bypass mode is also used to reset the FIFO. Passing through bypass mode is mandatory when switching between different FIFO buffer operating modes.

As described in the next figure, for each channel only the first address is used. When new data is available, the older data is overwritten.

Figure 9. Bypass mode



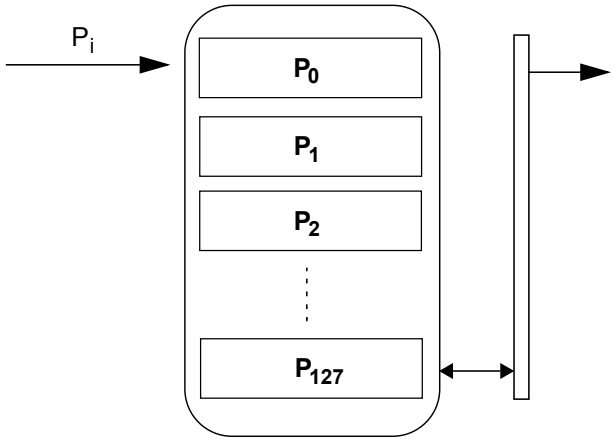
5.2 FIFO mode

In FIFO mode (FIFO_CTRL (14h)(TRIG_MODES and F_MODE[1:0] = 001) data from the output PRESS_OUT_XL (28h), PRESS_OUT_L (29h), and PRESS_OUT_H (2Ah) are stored in the FIFO until it is full.

To reset FIFO content, in order to select bypass mode the value 000 must be written in FIFO_CTRL (14h) (TRIG_MODE & F_MODE[1:0]). After this reset command it is possible to restart FIFO mode by writing the value 001 in FIFO_CTRL (14h)(TRIG_MODE & F_MODE[1:0]).

The FIFO buffer memorizes 128 levels of data, but the depth of the FIFO can be resized/reduced by setting the FIFO_CTRL (14h)(STOP_ON_WTM) bit. If the STOP_ON_WTM bit is set to 1, FIFO depth is limited to FIFO_WTM (15h)(WTM[6:0]) data.

Figure 10. FIFO mode



5.3 Continuous (dynamic-stream) mode

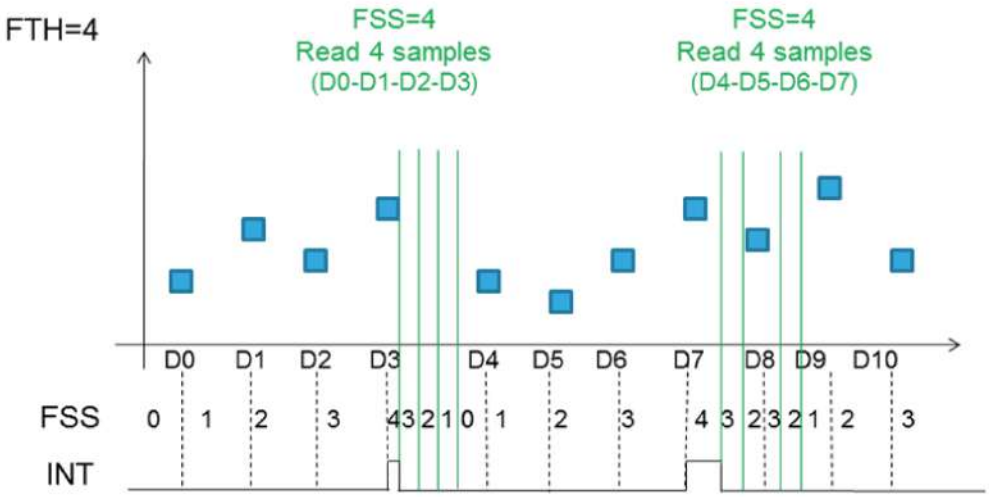
In continuous (dynamic-stream) mode (FIFO_CTRL (14h)(TRIG_MODES and F_MODE[1:0] = 011) after emptying the FIFO, the first new sample that arrives becomes the first to be read in a subsequent read burst. In this way, the number of new data available in FIFO does not depend on the previous read.

In continuous (dynamic-stream) mode FIFO_STATUS1 (25h)(FSS[7:0]) is the number of new pressure and temperature samples available in the FIFO buffer.

Continuous (dynamic-stream) is intended to be used to read FIFO_STATUS1 (25h)(FSS[7:0]) samples when it is not possible to guarantee reading data within 1/ODR time period.

Also, a FIFO threshold interrupt on the INT_DRDY pin through CTRL_REG3 (12h)(INT_F_WTM) can be enabled in order to read data from the FIFO and leave free memory slots for incoming data.

Figure 11. Continuous (dynamic-stream) mode

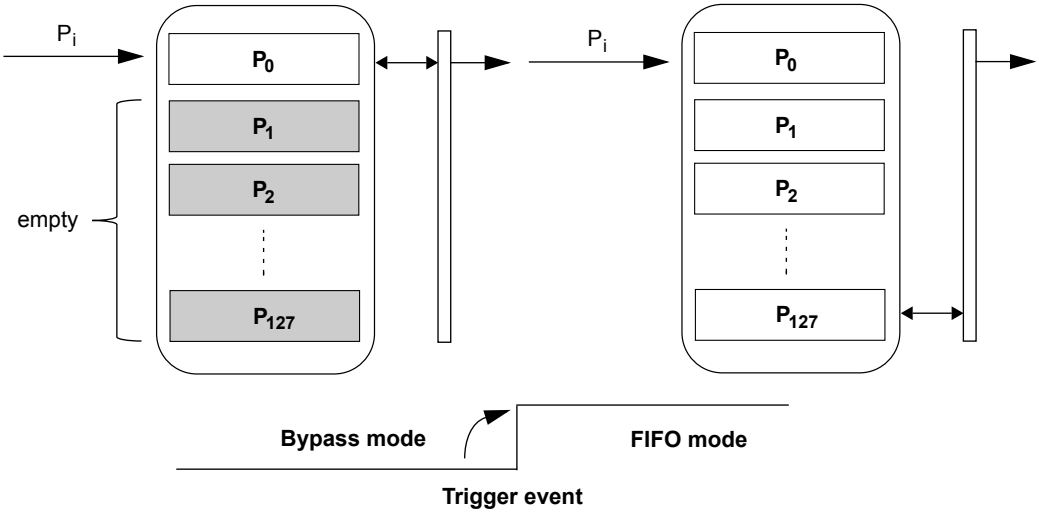


5.4 Bypass-to-FIFO mode

In bypass-to-FIFO mode (FIFO_CTRL (14h))(TRIG_MODES and F_MODE[1:0] = 101), FIFO behavior switches when the INT_SOURCE (24h)(IA) bit rises for the first time. When the INT_SOURCE (24h)(IA) bit is equal to 0, FIFO behaves like in bypass mode. Once the INT_SOURCE (24h)(IA) bit rises to 1, FIFO behavior switches and keeps behaving like in FIFO mode.

An interrupt generator has to be set to the desired configuration through INTERRUPT_CFG (0Bh).

Figure 12. Bypass-to-FIFO mode

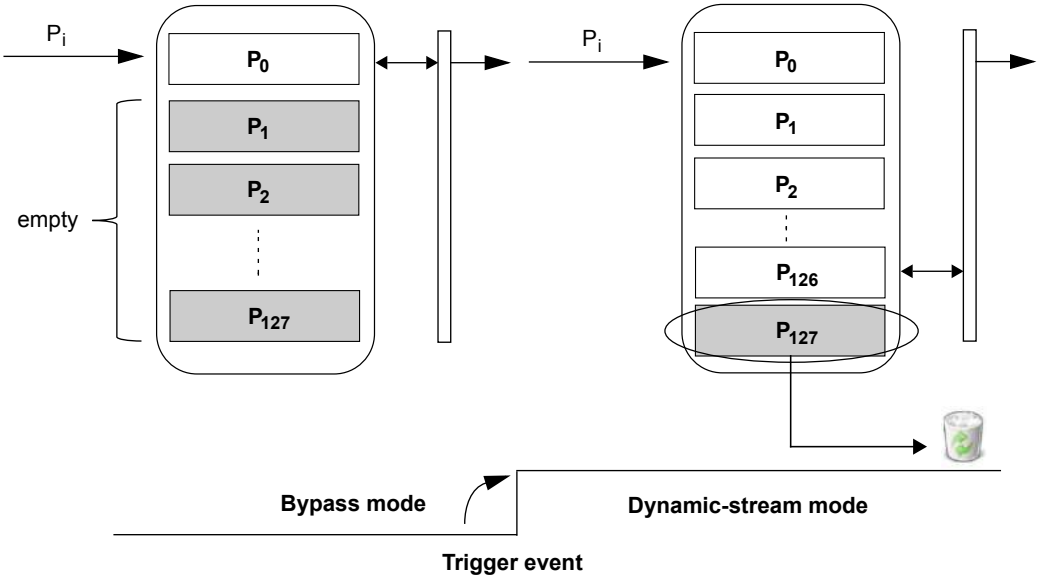


5.5 Bypass-to-continuous (dynamic-stream) mode

In bypass-to-continuous (dynamic-stream) mode (FIFO_CTRL (14h)(TRIG_MODES and F_MODE[1:0] = 110), FIFO operates in Bypass mode until it switches to continuous (dynamic-stream) mode behavior when INT_SOURCE (24h)(IA) rises to 1, then FIFO behavior keeps behaving like in continuous (dynamic-stream) mode.

An interrupt generator has to be set to the desired configuration through INTERRUPT_CFG (0Bh).

Figure 13. Bypass-to-continuous (dynamic-stream) mode

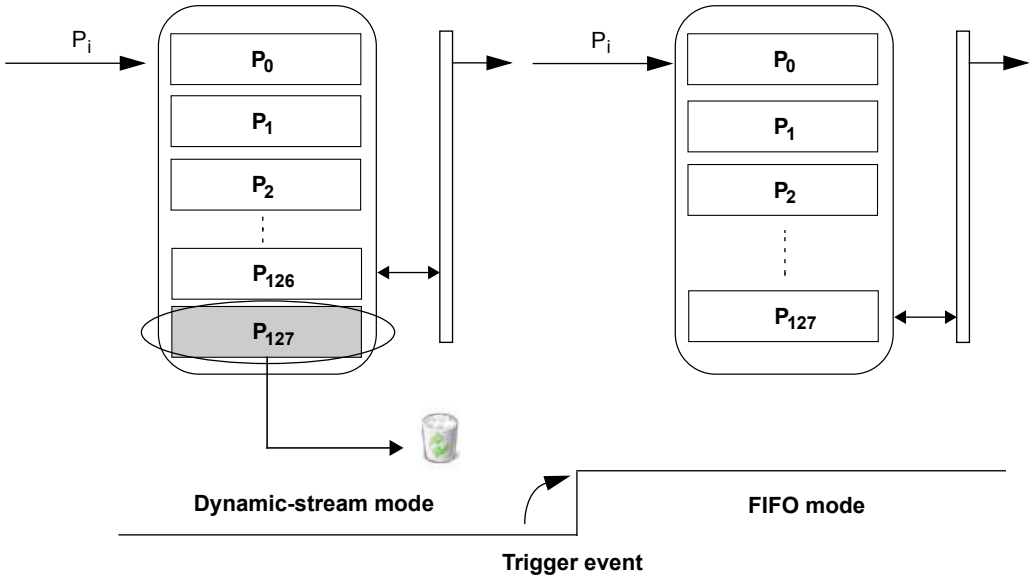


5.6 Continuous (dynamic-stream)-to-FIFO mode

In continuous (dynamic-stream)-to-FIFO mode (FIFO_CTRL (14h)(TRIG_MODES and F_MODE[1:0] = 111), data are stored in FIFO and FIFO operates in continuous (dynamic-stream) mode behavior until it switches to FIFO mode behavior when INT_SOURCE (24h)(IA) rises to 1.

An interrupt generator has to be set to the desired configuration through INTERRUPT_CFG (0Bh).

Figure 14. Continuous (dynamic-dtream)-to-FIFO mode



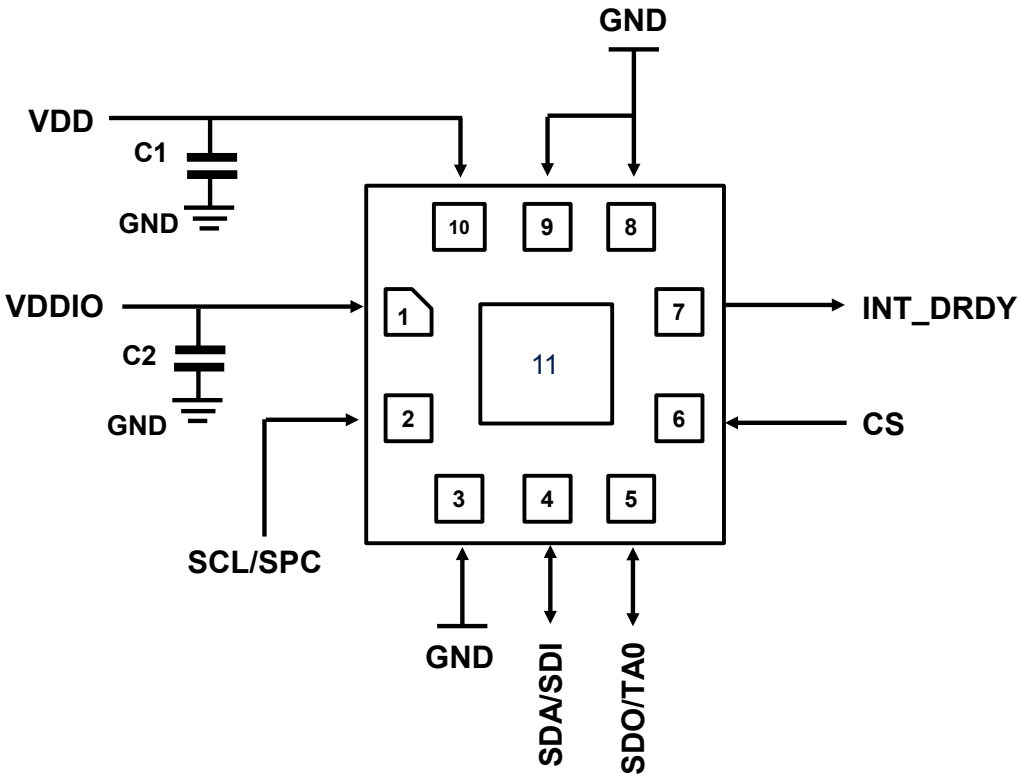
5.7 Retrieving data from FIFO

FIFO data is read through FIFO_DATA_OUT_PRESS (78h, 79h and 7Ah).

The read address is automatically updated by the device and it rolls back to 78h when register 7Ah is reached. In order to read all FIFO levels in a multiple byte read, 384 bytes (3 output registers with 128 levels) must be read.

6 Application hints

Figure 15. **LPS27DEWO electrical connections (top view)**



The device power supply must be provided through the VDD line; power supply decoupling capacitors C1, C2 (100 nF) must be placed as near as possible to the supply pads of the device. Depending on the application, an additional capacitor of 4.7 µF could be placed on the VDD line.

The functionality of the device and the measured data outputs are selectable and accessible through the I²C, MIPI I3C®, or SPI interface.

The metal lid is physically connected to pin 11 at component level and pin 11 can be used to connect the metal lid either to GND or left unconnected (floating) on the PCB of the application. The following table indicates the two cases of the metal lid connection. It is highly recommended that pin 11 be soldered to the PCB (left unconnected electrically) or soldered to GND to enhance solderability of the device.

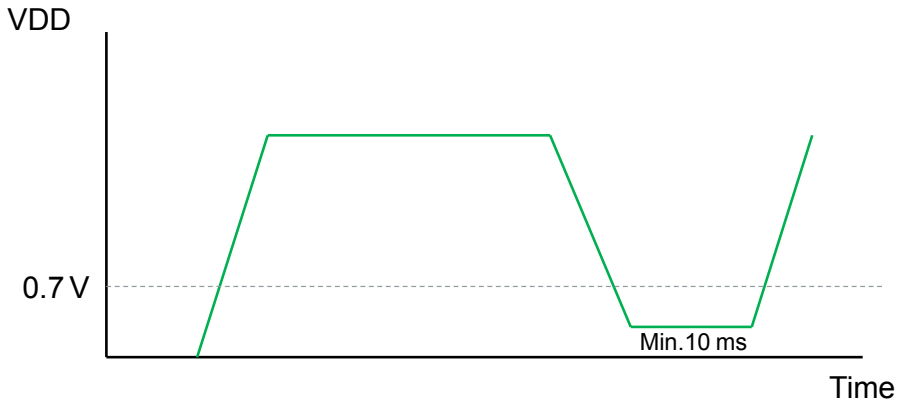
Table 10. **Metal lid and pin 11 connections**

Metal lid	Pin 11 connection to PCB(1)
Leave unconnected (floating)	Electrically leave unconnected (floating)
Connect to GND	Electrically connect to GND

1. *Pin 11 should be soldered to the PCB to improve solderability of the device.*

Note: *To guarantee proper power-off of the device, it is recommended to maintain the duration of the VDD line to GND for at least 10 ms.*

Figure 16. **LPS27DEWO power-off sequence**



- VDD Rising / Falling time : 10 µs ~ 100 ms
- VDD must be lower than 0.7 V for at least 10 ms during power-off sequence for correct POR

6.1 Soldering information

The LGA package is compliant with the ECOPACK standard and it is qualified for soldering heat resistance according to JEDEC J-STD-020.

For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

7 Digital interfaces

7.1 Serial interfaces

The registers embedded in the LPS27DEWO may be accessed through the I²C, MIPI I3C®, or SPI serial interfaces. The latter may be software configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I²C interface, the CS line must be tied high (that is, connected to VDDIO).

Table 11. Serial interface pin description

Pin name	Pin description
CS	Enables SPI I²C and MIPI I3C® / SPI mode selection (1: SPI idle mode / I²C and MIPI I3C®communication enabled; 0: SPI communication mode / I²C and MIPI I3C® disabled)
SCL/SPC	I²C / MIPI I3C® serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDI/SDO	I²C / MIPI I3C® serial data (SDA) 4-wire SPI serial data input (SDI) 3-wire serial data input/output (SDI/SDO)
SDO TA0	4-wire SPI serial data output (SDO) I²C least significant bit of the device address (TA0) MIPI I3C® least significant bit of the static address (TA0)

7.2 I²C serial interface (CS = high)

The LPS27DEWO I²C is a bus target. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in the following table.

Table 12. I²C terminology

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Controller	The device that initiates a transfer, generates clock signals, and terminates a transfer
Target	The device addressed by the controller

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines have to be connected to VDDIO through pull-up resistors.

The I²C interface is compliant with fast mode plus (1 MHz) I²C standards as well as with normal mode.

7.2.1 I²C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After the controller has transmitted this, the bus is considered busy. The next data byte transmitted after the start condition contains the address of the target in the first 7 bits and the eighth bit tells whether the controller is receiving data from the target or transmitting data to the target. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the controller.

The 7-bit target address (TAD) associated with the LPS27DEWO is 101110xb. The SDO/TA0 pin can be used to modify the less significant bit of the device address. If the TA0 pin is connected to the voltage supply, LSb is 1 (7-bit address 1011101b=5Dh), otherwise if the TA0 pin is connected to ground, the LSb value is 0 (7-bit address 1011100b=5Ch). This solution permits connecting and addressing two different LPS27DEWO devices to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver that has been addressed is obliged to generate an acknowledgment after each byte of data received.

The I²C embedded inside the ASIC behaves like a target device and the following protocol must be adhered to. After the start condition (ST) a target address is sent, once a target acknowledge has been returned (TAK), an 8-bit subaddress is transmitted (SUB). The IF_ADD_INC bit in CTRL_REG3 (12h) enables subaddress auto increment (IF_ADD_INC is 1 by default), so if IF_ADD_INC = 1 the SUB (subaddress) is automatically increased to allow multiple data read/write.

The target address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write) the controller transmits to the target with direction unchanged. Table 13 explains how the TAD+read/write bit pattern is composed, listing all the possible configurations.

Table 13. TAD+read/write patterns

Command	TAD[6:1]	TAD[0] = TA0	R/W	TAD+R/W
Read	101110	0	1	10111001(B9h)
Write	101110	0	0	10111000(B8h)
Read	101110	1	1	10111011(BBh)
Write	101110	1	0	10111010(BAh)

Table 14. Transfer when controller is writing one byte to target

Controller	ST	TAD+W		SUB		DATA		SP
Target			TAK		TAK		TAK	

Table 15. Transfer when controller is writing multiple bytes to target

Controller	ST	TAD+W		SUB		DATA		DATA		SP
Target			TAK		TAK		TAK		TAK	

Table 16. Transfer when controller is receiving (reading) one byte of data from target

Controller	ST	TAD+W		SUB		SR	TAD+R			NCAK	SP
Target			TAK		TAK			TAK	DATA		

Table 17. Transfer when controller is receiving (reading) multiple bytes of data from target

Controller	ST	TAD+W		SUB		SR	TAD+R			CAK		CAK		NCAK	SP
Target			TAK		TAK			TAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a target receiver does not acknowledge the target address (that is, it is not able to receive because it is performing some real-time function), the data line must be kept high by the target. The controller can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

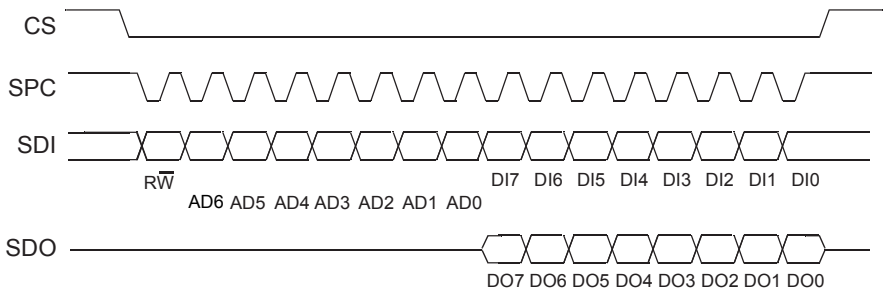
In the presented communication format CAK is controller acknowledge and NCAK is no controller acknowledge.

7.3 SPI bus interface (CS = low)

The LPS27DEWO SPI is a bus target. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the application using four wires: **CS**, **SPC**, **SDI**, and **SDO**.

Figure 17. Read and write protocol



CS enables the serial port and it is controlled by the SPI controller. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and it is controlled by the SPI controller. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or multiples of 8 in the case of multiple read/write bytes. Bit duration is the time between the two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23,...) starts at the last falling edge of SPC just before the rising edge of CS.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

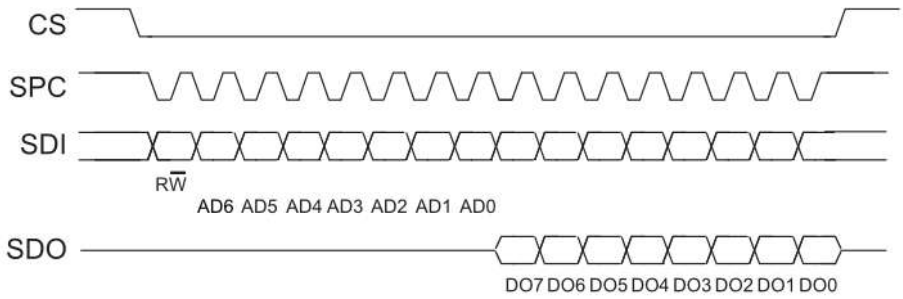
bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first). bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first). In multiple read/write commands further blocks of 8 clock periods are added. When the IF_ADD_INC bit is 0, the address used to read/write data remains the same for every block. When the IF_ADD_INC bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

7.3.1 SPI read

Figure 18. **SPI read protocol**



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

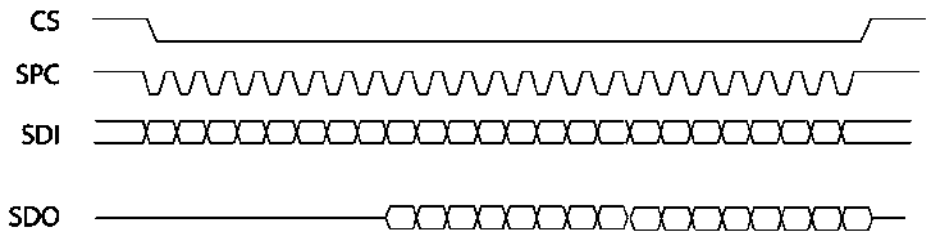
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

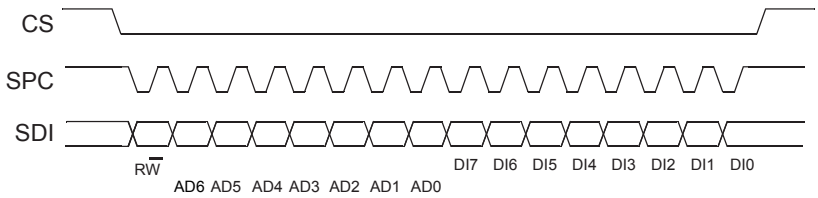
bit 16-...: data DO(...-8). Further data in multiple byte reads.

Figure 19. **Multiple byte SPI read protocol (2-byte example)**



7.3.2 SPI write

Figure 20. **SPI write protocol**



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

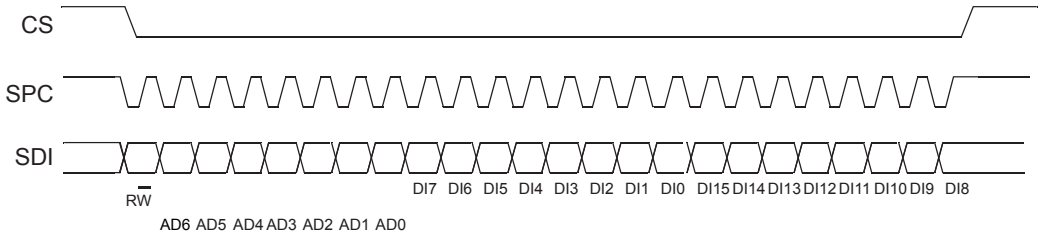
bit 0: WRITE bit. The value is 0.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written in the device (MSb first).

bit 16-...: data DI(...-8). Further data in multiple byte writes.

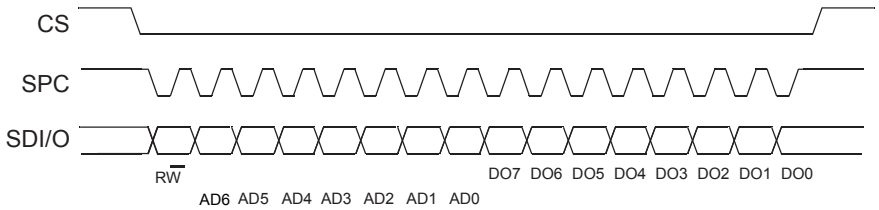
Figure 21. **Multiple byte SPI write protocol (2-byte example)**



7.3.3 SPI read in 3-wire mode

A 3-wire mode is entered by setting the SIM bit to 1 (SPI serial interface mode selection) in CTRL_REG1 (10h).

Figure 22. **SPI read protocol in 3-wire mode**



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first). A multiple read command is also available in 3-wire mode.

7.4 MIPI I3C® target interface

The LPS27DEWO interface includes a MIPI I3C® SDR only target interface (compliant with release 1.1 of the specification) with MIPI I3C® SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- In-band interrupt request
- Target reset pattern
- Group address
- Asynchronous modes 0 and 1
- Synchronous mode
- Error detection and recovery methods (S0-S6)

7.4.1 MIPI I3C® CCC supported commands

The list of MIPI I3C® CCC commands supported by the device is detailed in the following table.

Table 18. MIPI I3C® CCC commands

Command	Command code	Default	Description
ENTDAA	0x07		DAA procedure
SETDASA	0x87		Assign dynamic address using static address 0x5C/0x5D depending on TA0 pin
ENEC	0x80 / 0x00		Target activity control (direct and broadcast)
DISEC	0x81/ 0x01		Target activity control (direct and broadcast)
ENTAS0	0x82 / 0x02		Enter activity state (direct and broadcast)
SETXTIME	0x98 / 0x28		Timing information exchange
GETXTIME	0x99	0x07 0x00 0x0C 0x92	Timing information exchange
RSTDAA	0x06		Reset the assigned dynamic address (broadcast only)
SETMWL	0x89 / 0x08		Define maximum write length during private write (direct and broadcast)
SETMRL	0x8A / 0x09		Define maximum read length during private read (direct and broadcast)
SETNEWDA	0x88		Change dynamic address
GETMWL	0x8B	0x00 0x08 (2 byte)	Get maximum write length during private write
GETMRL	0x8C	0x00 0x10 0x05 (3 byte)	Get maximum read length during private read
GETPID	0x8D	0x02 0x08 0x00	TA0 = 1

Command	Command code	Default	Description
GETPID	0x8D	0xB4 0x90 0x0B	
		0x02 0x08 0x00 0xB4 0x10 0x0B	TA0 = 0
GETBCR	0x8E	0x07 (1 byte)	Bus characteristics register
GETDCR	0x8F	0x62 default	MIPI I3C® device characteristics register
GETSTATUS	0x90	0x00 0x00 (2 byte)	Status register
GETMXDS	0x94	0x08 0x60	Return maximum write and read speed
GETCAPS	0x95	0x00 0x11 0x18 0x00	Provide information about device capabilities and supported extended features
SETGRPA	0x9B		Group address assignment command
RSTGRPA	0x2C/0x9C		Reset the group address
RSTACT	0x9A/0x2A		Configure target reset action

7.4.2 Overview of antispike filter management

The device acts as a standard I²C target as long as it has an I²C static address. The device is capable of detecting and disabling the I²C antispike filter after detecting the broadcast address (7'h7E/W). In order to guarantee proper behavior of the device, the I3C controller must emit the first START, 7'h7E/W at open-drain speed using I²C fast mode plus reference timing.

After detecting the broadcast address, the device can receive the I3C dynamic address following the I3C push-pull timing. If the device is not assigned a dynamic address, then the device continues to operate as an I²C device with no antispike filter. For the case in which the host decides to keep the device as I²C with an antispike filter, there is a configuration required to keep the antispike filter active. This configuration is done by writing the ASF_ON bit to 1 in the I3C_IF_CTRL (19h) register. This configuration forces the antispike filter to always be turned on instead of being managed by the communication on the bus.

8 Register mapping

The following table provides a quick overview of the 8-bit registers embedded in the device.

Table 19. Registers address map

Name	Type	Register address	Default	Function and comment
		Hex	Hex	
Reserved		00 – 0A	-	Reserved
INTERRUPT_CFG	R/W	0B	00h	Interrupt register
THS_P_L	R/W	0C	00h	Pressure threshold registers
THS_P_H	R/W	0D	00h	
IF_CTRL	R/W	0E	00h	Interface control register
WHO_AM_I	R	0F	B4h	Who am I
CTRL_REG1	R/W	10	00h	Control registers
CTRL_REG2	R/W	11	00h	
CTRL_REG3	R/W	12	01h	
CTRL_REG4	R/W	13	00h	
FIFO_CTRL	R/W	14	00h	FIFO configuration registers
FIFO_WTM	R/W	15	00h	
REF_P_L	R	16	00h	Reference pressure registers
REF_P_H	R	17	00h	
Reserved		18	-	Reserved
I3C_IF_CTRL	R/W	19	80h	Interface configuration register
RPDS_L	R/W	1A	00h	Pressure offset registers
RPDS_H	R/W	1B	00h	
Reserved		1C-23	-	Reserved
INT_SOURCE	R	24	Output	Interrupt register
FIFO_STATUS1	R	25	Output	FIFO status registers
FIFO_STATUS2	R	26	Output	
STATUS	R	27	Output	Status register
PRESSURE_OUT_XL	R	28	Output	Pressure output registers
PRESSURE_OUT_L	R	29	Output	
PRESSURE_OUT_H	R	2A	Output	
TEMP_OUT_L	R	2B	Output	Temperature output registers
TEMP_OUT_H	R	2C	Output	
Reserved		2D - 6F	-	Reserved
ID_FS	R	70	Output	ID
Reserved		71 - 77	-	Reserved
FIFO_DATA_OUT_PRESS_XL	R	78	Output	FIFO pressure output registers
FIFO_DATA_OUT_PRESS_L	R	79	Output	
FIFO_DATA_OUT_PRESS_H	R	7A	Output	

Registers marked as Reserved must not be changed. Writing to those registers may cause permanent damage to the device.

To guarantee the proper behavior of the device, all register addresses not listed in the above table must not be accessed and the content stored in those registers must not be changed.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The register address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

9.1 INTERRUPT_CFG (0Bh)

Interrupt mode for pressure acquisition configuration (R/W)

7	6	5	4	3	2	1	0
AUTOREFP	RESET_ARP	AUTOZERO	RESET_AZ	-	LIR	PLE	PHE

AUTOREFP	Enable the AUTOREFP function. Default value: 0 (0: normal mode; 1: AUTOREFP enabled)
RESET_ARP	Reset the AUTOREFP function. Default value: 0 (0: normal mode; 1: reset AUTOREFP function)
AUTOZERO	Enable the AUTOZERO function. Default value: 0 (0: normal mode; 1: AUTOZERO enabled)
RESET_AZ	Reset the AUTOZERO function. Default value: 0 (0: normal mode; 1: reset AUTOZERO function)
LIR	Latch interrupt request to the INT_SOURCE (24h) register. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
PLE	Enable interrupt generation on low pressure event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on the pressure value lower than the preset threshold)
PHE	Enable interrupt generation on high pressure event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on the pressure value higher than the preset threshold)

Referring to Figure 23. “Threshold-based” interrupt event, the LPS27DEWO can be set by the user to support the interrupt function when P_DIFF_IN (defined below) is higher or lower than the threshold value stored in THS_P_L (0Ch) and THS_P_H (0Dh).

It is enabled when either the PHE bit or PLE bit (or both bits) = 1. Then, the differential pressure can be compared to a user-defined threshold stored in the 15-bit THS_P (0Ch and 0Dh) registers.

The threshold pressure value defined by the user is a 15-bit unsigned value in a 16-bit register composed of THS_P_L (0Ch) and THS_P_H (0Dh). The value is:

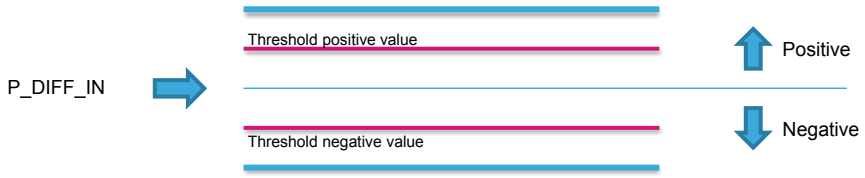
THS_P (15-bit unsigned) = desired interrupt threshold (hPa) x $\frac{2700}{256}$ for FS_mode 1 (up to 1260 hPa)

THS_P (15-bit unsigned) = desired interrupt threshold (hPa) x $\frac{1350}{256}$ for FS_mode 2 (up to 6060 hPa)

The PHE and PLE bits in INTERRUPT_CFG (0Bh) enable the differential pressure interrupt generation on the positive or negative event respectively.

The differential interrupt must be used with AUTOREFP or AUTOZERO mode.

Figure 23. "Threshold-based" interrupt event



To enable **AUTOZERO** mode, the AUTOZERO bit must be set to 1 and then the measured pressure value is used as the reference and stored in the register REF_P (REF_P_L (16h), REF_P_H (17h)). From this point on, the output pressure value (PRESS_OUT_XL (28h), PRESS_OUT_L (29h), PRESS_OUT_H (2Ah)) is updated with the difference between the measured pressure and REF_P.

- P_DIFF_IN = measured pressure - REF_P
- PRESS_OUT = measured pressure - REF_P

After the first conversion, the AUTOZERO bit is automatically set back to 0. In order to return back to normal mode, the RESET_AZ bit in the INTERRUPT_CFG (0Bh) register has to be set to 1. This also resets the content of the REF_P register to 0.

AUTOREFP mode allows using the pressure differential for the generation of the interrupt keeping the output pressure registers PRESS_OUT (PRESS_OUT_XL (28h), PRESS_OUT_L (29h), PRESS_OUT_L (29h)) without comparing REF_P. If the AUTOREFP bit is set to 1, the measured output pressure is used as the reference in the register REF_P (REF_P_L (16h), REF_P_H (17h)) for interrupt generation with the following:

- P_DIFF_IN = measured pressure - REF_P

The output registers PRESS_OUT (28h, 29h, and 2Ah) are not changed by REF_P and shows as follows.

- PRESS_OUT = measured pressure

After the first conversion, the AUTOREFP bit is automatically set to 0. In order to return back to normal mode, the RESET_ARP bit has to be set to 1.

9.2 THS_P_L (0Ch)

User-defined threshold value for pressure interrupt event (least significant bits) (R/W)

7	6	5	4	3	2	1	0
THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

THS[7:0]	This register contains the low part of the threshold value for pressure interrupt generation. Default value: 00h

The threshold value for pressure interrupt generation is a 15-bit unsigned right-justified value composed of THS_P_H (0Dh) and THS_P_L (0Ch). The value is expressed as:

THS_P (15-bit unsigned) = desired interrupt threshold (hPa) x $\frac{2700}{256}$ for FS_mode 1 (up to 1260 hPa)

THS_P (15-bit unsigned) = desired interrupt threshold (hPa) x $\frac{1350}{256}$ for FS_mode 2 (up to 6060 hPa)

To enable the interrupt event based on this user-defined threshold, the PHE bit or PLE bit (or both bits) in INTERRUPT_CFG (0Bh) has to be enabled.

9.3 THS_P_H (0Dh)

User-defined threshold value for pressure interrupt event (most significant bits) (R/W)

7	6	5	4	3	2	1	0
-	THS14	THS13	THS12	THS11	THS10	THS9	THS8

THS[14:8]	This register contains the high part of the threshold value for pressure interrupt generation. Default value: 00h Refer to THS_P_L (0Ch).

9.4 IF_CTRL (0Eh)

Interface control register (R/W)

7	6	5	4	3	2	1	0
INT_EN_I3C	I2C_I3C_DIS	SIM	SDA_PU_EN	SDO_PU_EN	INT_PD_DIS	CS_PU_DIS	-

INT_EN_I3C	Enable INT pin with MIPI I3C®. If the INT_EN_I3C bit is set, the INT pin is polarized as OUT. Default value: 0 (0: INT disabled with MIPI I3C®; 1: INT enabled with MIPI I3C®)
I2C_I3C_DIS	Disable I²C and I3C digital interfaces. Default value: 0 (0: enable I²C and I3C digital interfaces; 1: disable I²C and I3C digital interfaces)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
SDA_PU_EN	Enable pull-up on the SDA pin. Default value: 0 (0: SDA pin pull-up disconnected; 1: SDA pin with pull-up)
SDO_PU_EN	Enable pull-up on the SDO pin. Default value: 0 (0: SDO pin pull-up disconnected; 1: SDO pin with pull-up)
INT_PD_DIS	Disable pull-down on the INT pin. Default value: 0 (0: INT pin with pull-down; 1: INT pin pull-down disconnected)
CS_PU_DIS	Disable pull-up on the CS pin. Default value: 0 (0: CS pin with pull-up; 1: CS pin pull-up disconnected)

9.5 WHO_AM_I (0Fh)

Device Who am I

7	6	5	4	3	2	1	0
1	0	1	1	0	1	0	0

9.6 CTRL_REG1 (10h)

Control register 1 (R/W)

7	6	5	4	3	2	1	0
0	ODR3	ODR2	ODR1	ODR0	AVG2	AVG1	AVG0

ODR[3:0]	Output data rate selection. Default value: 0000 Refer to Table 20.
AVG[2:0]	Average selection. Default value: 000 Refer to Table 21.

Table 20. Output data rate bit configurations

ODR[3:0]	ODR of pressure, temperature
0000	One-shot
0001	1 Hz
0010	4 Hz
0011	10 Hz
0100	25 Hz
0101	50 Hz
0110	75 Hz
0111	100 Hz
1xxx	200 Hz

Table 21. Averaging selection

AVG[2:0]	Averaging of pressure and temperature
000	4
001	8
010	16
011	32
100	64
101	128
111	512

The power consumption of the LPS27DEWO mainly depends on the selected ODR (output data rate) and on the selected resolution. The user can select the desired ODR and the oversampling frequency for pressure measurements in the CTRL_REG1 (10h) register. The ODR[6:3] bits are dedicated to the ODR selection, while the AVG[2:0] bits are used to configure the resolution.

The following table summarizes the supply current at different ODRs and AVG resolution.

Table 22. Power consumption

AVG	One-shot mode		Continuous mode – supply current (µA) vs. ODR							
	Supply current (µA) @ 1 Hz	ODR Max	1 Hz	4 Hz	10 Hz	25 Hz	50 Hz	75 Hz	100 Hz	200 Hz
512	32.2	25	32.8	126.8	314.4	783.8	-	-	-	-
128	9.4	75	10	35.6	86.7	214.3	427	639.8	-	-
64	5.6	100	6.3	20.4	48.7	119.4	237.2	355	472.8	-
32	3.7	200	4.4	12.8	29.8	71.9	142.2	212.6	282.9	564.4
16	2.7	300	3.5	9	20.2	48.2	94.8	141.4	188	374
8	2	400	2.7	6	12.6	29.1	56.5	84.2	111.5	221.7
4	1.7	500	2.5	5	10.2	23.2	44.7	66.2	87.8	174

The noise performance of LPS27DEWO is also defined as depending on the ODR and selected resolution and its performance is a trade-off between the power consumption and resolution. The noise performance is indicated in the following table.

Table 23. Noise performance

AVG	FS = 1260 hPa			FS = 6060 hPa		
	Pressure noise (Pa_{rms})			Pressure noise (Pa_{rms})		
	ODR/2	ODR/4	ODR/9	ODR/2	ODR/4	ODR/9
512	0.56	0.42	0.32	1.22	0.81	0.60
128	0.86	0.63	0.46	2.15	1.52	1.08
64	1.14	0.83	0.58	2.94	2.07	1.53
32	1.50	1.10	0.80	4.01	2.94	2.10
16	2.10	1.54	1.03	5.67	4.07	2.98
8	2.88	2.05	1.45	7.89	5.59	4.07
4	3.80	2.76	1.95	10.84	7.77	5.60

When the ODR bits are set to 0000, the device is in **power-down mode**. When the device is in power-down mode, almost all internal blocks of the device are switched off to minimize power consumption. The digital interface is still active to allow communication with the device. The content of the configuration registers is preserved and the output data registers are not updated, therefore keeping the last data sampled in memory before going into power-down mode.

If the ONESHOT bit in CTRL_REG2 (11h) is set to 1, **one-shot mode** is triggered and a new acquisition starts when it is required. Enabling this mode is possible only if the device was previously in power-down mode (ODR bits set to 0000). Once the acquisition is completed and the output registers updated, the device automatically enters in power-down mode. The ONESHOT bit self-clears itself.

When the ODR bits are set to a value different than 0000, the device is in **continuous mode** and automatically acquires a set of data (pressure and temperature) at the frequency selected through the ODR[3:0] bits.

9.7 CTRL_REG2 (11h)

Control register 2 (R/W)

7	6	5	4	3	2	1	0
BOOT	FS_MODE	LFPF_CFG	EN_LPFP	BDU	SWRESET	-	ONESHOT

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FS_MODE	Full-scale selection. Default value: 0 (0: mode 1, full scale up to 1260 hPa; 1: mode 2, full scale up to 6060 hPa)
LFPF_CFG	Low-pass filter configuration. Default value: 0 (0: ODR/4; 1: ODR/9)
EN_LPFP	Enable low-pass filter on pressure data. Default value: 0 (0: disable; 1: enable)
BDU[(1)]	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
SWRESET	Software reset. Default value: 0 (0: normal mode; 1: software reset). The bit is self-cleared when the reset is completed.
ONESHOT	Enable one-shot mode. Default value: 0 (0: idle mode; 1: a new dataset is acquired)

1. *To guarantee the correct behavior of the BDU feature, PRESS_OUT_H (2Ah) must be the last address read.*

The BOOT bit is used to refresh the content of the internal registers stored in the nonvolatile memory block. At device power-up, the content of the nonvolatile memory block is transferred to the internal registers related to the trimming functions to allow correct behavior of the device itself. If for any reason the content of the trimming registers is modified, it is sufficient to use this bit to restore the correct values. When the BOOT bit is set to 1, the content of the internal nonvolatile memory block is copied into the corresponding internal registers and is used to calibrate the device. These values are factory trimmed and they are different for every device. They allow the correct behavior of the device and normally they should not be changed. At the end of the boot process, the BOOT bit is set again to 0 by hardware. The BOOT bit takes effect immediately after it is set to 1.

The SWRESET bit resets the volatile registers to the default value. It returns to 0 by hardware.

The ONESHOT bit is used to start a new conversion when the ODR[3:0] bits in CTRL_REG1 (10h) are set to 0000. Writing a 1 to ONESHOT triggers a single measurement of pressure and temperature. Once the measurement is done, the ONESHOT bit self-clears, the new data are available in the output registers, and the STATUS (27h) bits are updated.

9.8 CTRL_REG3 (12h)

Control register 3 (R/W)

7	6	5	4	3	2	1	0
0	0	0	0	INT_H_L	0	PP_OD	IF_ADD_INC

INT_H_L	Select interrupt active-high, active-low. Default value: 0 (0: active-high; 1: active-low)
PP_OD	Push-pull/open-drain selection on interrupt pin. Default value: 0 (0: push-pull; 1: open-drain)
IF_ADD_INC	Register address automatically incremented during a multiple byte access with a serial interface (I²C, I3C, or SPI). Default value: 1 (0: disable, 1: enable)

The INT_H_L bit selects an interrupt active-high/low value.

The PP_OD bit selects push-pull/open-drain on the interrupt pin.

The IF_ADD_INC bit enables the address to be automatically incremented during a multiple byte access with a serial interface (I²C, I3C, or SPI).

9.9 CTRL_REG4 (13h)

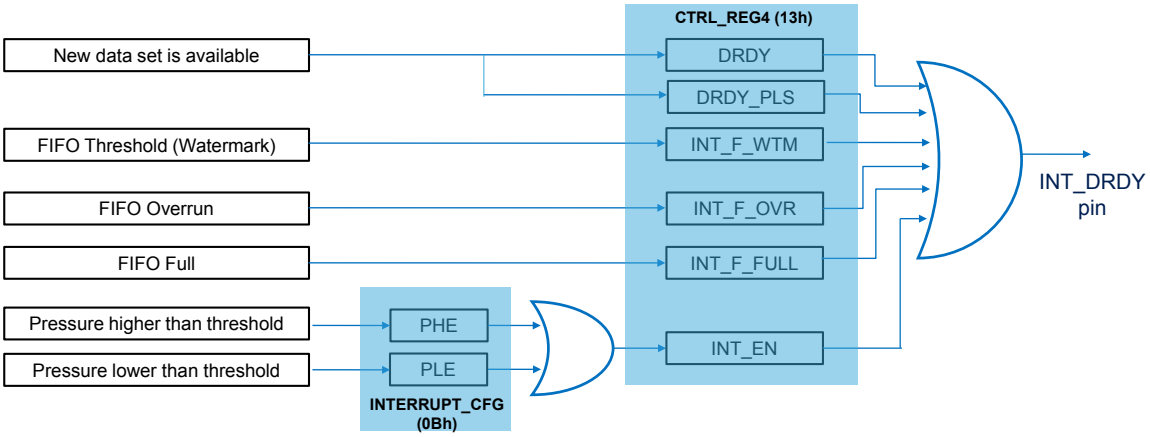
Control register 4 (R/W)

7	6	5	4	3	2	1	0
0	DRDY_PLS	DRDY	INT_EN	-	INT_F_FULL	INT_F_WTM	INT_F_OVR

DRDY_PLS[1]	Data-ready pulsed on INT_DRDY pin. Default value: 0 (0: disable; 1: enable data-ready pulsed on INT_DRDY pin, pulse width around 5 µs)
DRDY	Date-ready signal on INT_DRDY pin. Default value: 0 (0: disable; 1: enable)
INT_EN	Interrupt signal on INT_DRDY pin. Default value: 0 (0: disable; 1: enable)
INT_F_FULL	FIFO full flag on INT_DRDY pin. Default value: 0 (0: FIFO empty; 1: FIFO full with 128 unread samples)
INT_F_WTM	FIFO threshold (watermark) status on INT_DRDY pin. Default value: 0 (0: FIFO is lower than WTM level; 1: FIFO is equal to or higher than WTM level)
INT_F_OVR	FIFO overrun status on INT_DRDY pin. Default value: 0 (0: not overwritten; 1: at least one sample in the FIFO has been overwritten)

1. *This bit is used together with the DRDY bit and it can be ignored if DRDY=0.*

Figure 24. Interrupt events on INT_DRDY pin



9.10 FIFO_CTRL (14h)

FIFO control register (R/W)

7	6	5	4	3	2	1	0
0	0	0	0	STOP_ON_WTM	TRIG_MODES	F_MODE1	F_MODE0

STOP_ON_WTM	Stop-on-FIFO watermark. Enables FIFO watermark level use. Default value: 0 (0: disable; 1: enable)
TRIG_MODES	Enables triggered FIFO modes. Default value: 0
F_MODE[1:0]	Selects triggered FIFO modes. Default value: 00 Refer to Table 24.

Table 24. FIFO mode selection

TRIG_MODES	F_MODE[1:0]	Mode
x	00	Bypass
0	01	FIFO mode
0	1x	Continuous (dynamic-stream)
1	01	Bypass-to-FIFO
1	10	Bypass-to-continuous (dynamic-stream)
1	11	Continuous (dynamic-stream)-to-FIFO

The STOP_ON_WTM bit enables the use of the FIFO watermark level: when the number of samples in FIFO is equal to the watermark level (set using the WTM[4:0] bits in FIFO_WTM (15h)) then FIFO is full.

The TRIG_MODES bit enables the triggered FIFO modes.

The F_MODE[1:0] bits are used to select one of the FIFO modes, as described in Table 24.

Output pressure data are read through FIFO_DATA_OUT_PRESS_XL (78h), FIFO_DATA_OUT_PRESS_L (79h) and FIFO_DATA_OUT_PRESS_H (7Ah); both single read and multiple read operations can be used.

9.11 FIFO_WTM (15h)

FIFO threshold setting register (R/W)

7	6	5	4	3	2	1	0
0	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

WTM[6:0]	FIFO threshold. Watermark level setting. Default value: 0000000

9.12 REF_P_L (16h)

Reference pressure LSB data (R)

7	6	5	4	3	2	1	0
REFP7	REFP6	REFP5	REFP4	REFP3	REFP2	REFP1	REFP0

REFP[7:0]	This register contains the low part of the reference pressure value. Default value: 00000000

The reference pressure value is 16-bit data and it is composed of REF_P_H (17h) and REF_P_L (16h). The value is expressed as two's complement.

The reference pressure value is stored and used when the AUTOZERO or AUTOREFP function is enabled. Refer to the INTERRUPT_CFG (0Bh) register description.

9.13 REF_P_H (17h)

Reference pressure MSB data (R)

7	6	5	4	3	2	1	0
REFP15	REFP14	REFP13	REFP12	REFP11	REFP10	REFP9	REFP8

REFP[15:8]	This register contains the high part of the reference pressure value. Default value: 00000000

9.14 I3C_IF_CTRL (19h)

Control register (R/W)

7	6	5	4	3	2	1	0
1	0	ASF_ON	0	0	0	I3C_Bus_ Avb_Sel1	I3C_Bus_ Avb_Sel0

ASF_ON	Enable antispike filters. Default value: 0 (0: antispike filters are managed by protocol and turned off after the broadcast address; 1: antispike filters on SCL and SDA lines are always enabled)
I3C_Bus_Avb_Sel[1:0]	These bits are used to select the bus available time when I3C IBI is used. Default value: 00 (00: bus available time equal to 50 µsec; 01: bus available time equal to 2 µsec; 10: bus available time equal to 1 msec; 11: bus available time equal to 25 msec)

9.15 RPDS_L (1Ah)

Pressure offset (LSB data)

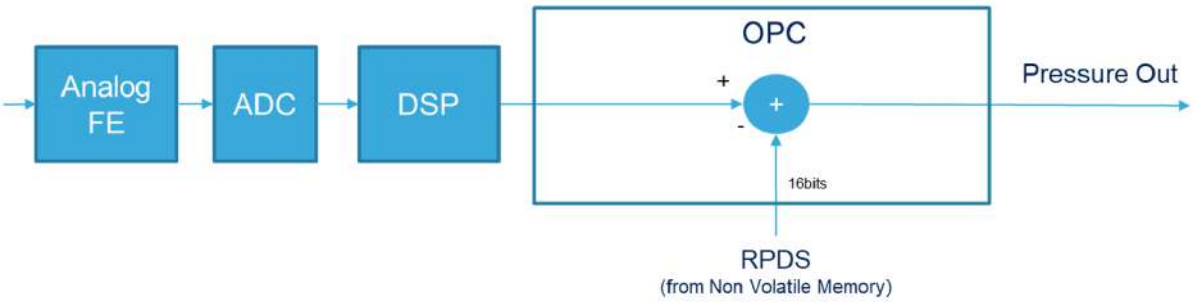
7	6	5	4	3	2	1	0
RPDS7	RPDS6	RPDS5	RPDS4	RPDS3	RPDS2	RPDS1	RPDS0

RPDS[7:0]	This register contains the low part of the pressure offset value. Default value: 00000000

The pressure offset value is 16-bit data that can be used to implement one-point calibration (OPC) after soldering. This value is composed of RPDS_H (1Bh) and RPDS_L (1Ah). The value is expressed as two's complement.

The customer can perform a one-point calibration after soldering (recommended) and the offset coefficient can be stored for OPC in register RPDS (1Ah, 1Bh). These stored offset values are directly added to the compensated pressure data in the block diagram below. To give better flexibility to the user, the OPC value can be written twice in the same register map. For further details, refer to the application note.

Figure 25. One-point calibration



9.16 RPDS_H (1Bh)

Pressure offset (MSB data)

7	6	5	4	3	2	1	0
RPDS15	RPDS14	RPDS13	RPDS12	RPDS11	RPDS10	RPDS9	RPDS8

RPDS[15:8]	This register contains the high part of the pressure offset value. Default value: 00000000

9.17 INT_SOURCE (24h)

Interrupt source (read only) register for differential pressure. A read at this address clears the INT_SOURCE register itself.

7	6	5	4	3	2	1	0
BOOT_ON	0	0	0	0	IA	PL	PH

BOOT_ON	Indication that Boot (reboot) phase is running. (0: boot phase not running; 1: boot phase is running)
IA	Interrupt active. (0: no interrupt has been generated; 1: one or more interrupt events have been generated)
PL	Differential pressure Low. (0: no interrupt has been generated; 1: low differential pressure event has occurred)
PH	Differential pressure High. (0: no interrupt has been generated; 1: high differential pressure event has occurred)

9.18 FIFO_STATUS1 (25h)

FIFO status register (read only)

7	6	5	4	3	2	1	0
FSS7	FSS6	FSS5	FSS4	FSS3	FSS2	FSS1	FSS0

FSS[7:0]	FIFO stored data level, number of unread samples stored in FIFO. (00000000: FIFO empty; 10000000: FIFO full, 128 unread samples)

9.19 FIFO_STATUS2 (26h)

FIFO status register (read only)

7	6	5	4	3	2	1	0
FIFO_WTM_IA	FIFO_OVR_IA	FIFO_FULL_IA	-	-	-	-	-

FIFO_WTM_IA	FIFO threshold (watermark) status. Default value: 0 (0: FIFO filling is lower than threshold level; 1: FIFO filling is equal or higher than threshold level)
FIFO_OVR_IA	FIFO overrun status. Default value: 0 (0: FIFO is not completely full; 1: FIFO is full and at least one sample in the FIFO has been overwritten)
FIFO_FULL_IA	FIFO full status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled, no samples overwritten)

9.20 STATUS (27h)

Status register (read only)

7	6	5	4	3	2	1	0
-	-	T_OR	P_OR	-	-	T_DA	P_DA

T_OR	Temperature data overrun. (0: no overrun has occurred; 1: new data for temperature has overwritten the previous data)
P_OR	Pressure data overrun. (0: no overrun has occurred; 1: new data for pressure has overwritten the previous data)
T_DA	Temperature data available. (0: new data for temperature is not yet available; 1: new temperature data is generated)
P_DA	Pressure data available. (0: new data for pressure is not yet available; 1: new pressure data is generated)

This register is updated every ODR cycle.

9.21 PRESS_OUT_XL (28h)

Pressure output value LSB data (read only)

7	6	5	4	3	2	1	0
POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0

POUT[7:0]	This register contains the low part of the pressure output value.

The pressure output value is a 24-bit data that contains the measured pressure. It is composed of PRESS_OUT_H (2Ah), PRESS_OUT_L (29h), and PRESS_OUT_XL (28h). The value is expressed as two's complement.

The output pressure register **PRESS_OUT** is provided as the difference between the measured pressure and the content of the register RPDS (18h, 19h).

This register contains the pressure value and the resolution is: 1 LSB = 1/2700 hPa (when FS_MODE = 0), otherwise 1 LSB = 1/1350 hPa (when FS_MODE = 1). Refer to Section 4.5: Interpreting pressure readings for additional information.

9.22 PRESS_OUT_L (29h)

Pressure output value middle data (read only)

7	6	5	4	3	2	1	0
POUT15	POUT14	POUT13	POUT12	POUT11	POUT10	POUT9	POUT8

POUT[15:8]	This register contains the mid part of the pressure output value. Refer to PRESS_OUT_XL (28h)

9.23 PRESS_OUT_H (2Ah)

Pressure output value MSB data (read only)

7	6	5	4	3	2	1	0
POUT23	POUT22	POUT21	POUT20	POUT19	POUT18	POUT17	POUT16

POUT[23:16]	This register contains the high part of the pressure output value. Refer to PRESS_OUT_XL (28h)

9.24 TEMP_OUT_L (2Bh)

Temperature output value LSB data (read only)

7	6	5	4	3	2	1	0
TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0

TOUT[7:0]	This register contains the low part of the temperature output value.

The temperature output value is 16-bit data that contains the measured temperature. It is composed of TEMP_OUT_H (2Ch), and TEMP_OUT_L (2Bh). The value is expressed as two's complement.

This register contains the temperature value and the resolution is: 1LSB = 0.01°C.

9.25 TEMP_OUT_H (2Ch)

Temperature output value MSB data (read only)

7	6	5	4	3	2	1	0
TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8

TOUT[15:8]	This register contains the high part of the temperature output value.

9.26 ID_FS (70h)

Identification of device (read only)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	1	0

ID_FS	Identification of LPS27DEWO

9.27 FIFO_DATA_OUT_PRESS_XL (78h)

FIFO pressure output LSB data (read only)

7	6	5	4	3	2	1	0
FIFO_P7	FIFO_P6	FIFO_P5	FIFO_P4	FIFO_P3	FIFO_P2	FIFO_P1	FIFO_P0

FIFO_P[7:0]	Pressure LSB data in FIFO buffer

9.28 FIFO_DATA_OUT_PRESS_L (79h)

FIFO pressure output middle data (read only)

7	6	5	4	3	2	1	0
FIFO_P15	FIFO_P14	FIFO_P13	FIFO_P12	FIFO_P11	FIFO_P10	FIFO_P9	FIFO_P8

FIFO_P[15:8]	Pressure middle data in FIFO buffer

9.29 FIFO_DATA_OUT_PRESS_H (7Ah)

FIFO pressure output MSB data (read only)

7	6	5	4	3	2	1	0
FIFO_P23	FIFO_P22	FIFO_P21	FIFO_P20	FIFO_P19	FIFO_P18	FIFO_P17	FIFO_P16

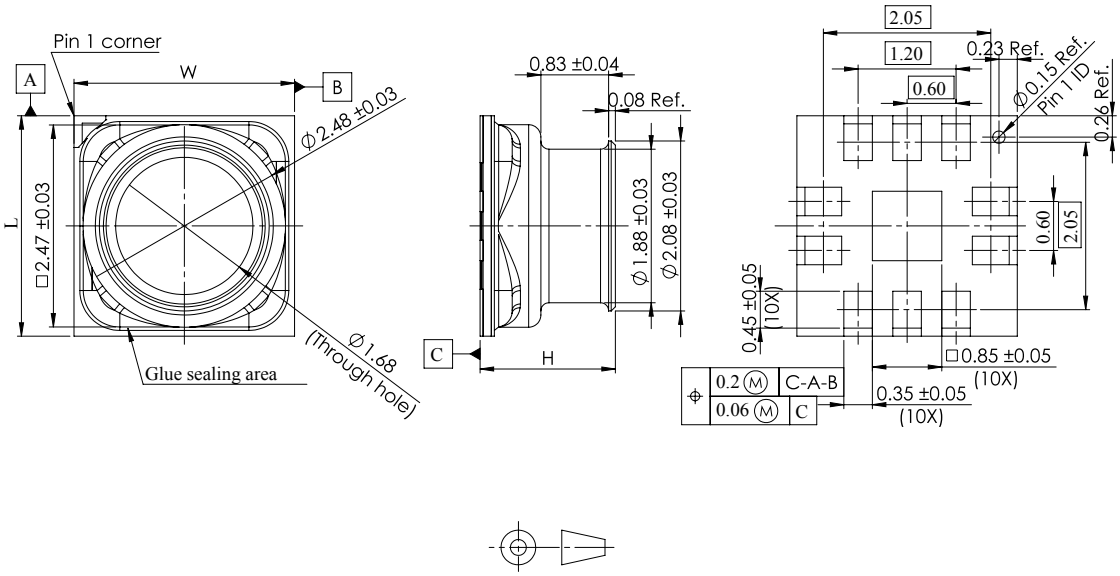
FIFO_P[23:16]	Pressure MSB data in FIFO buffer

10 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 LGA-11L package information

Figure 26. LGA-11L 2.7 x 2.7 x 1.85 mm package outline and mechanical data



Dimensions are in millimeters unless otherwise specified
General tolerance is +/-0.1mm unless otherwise specified

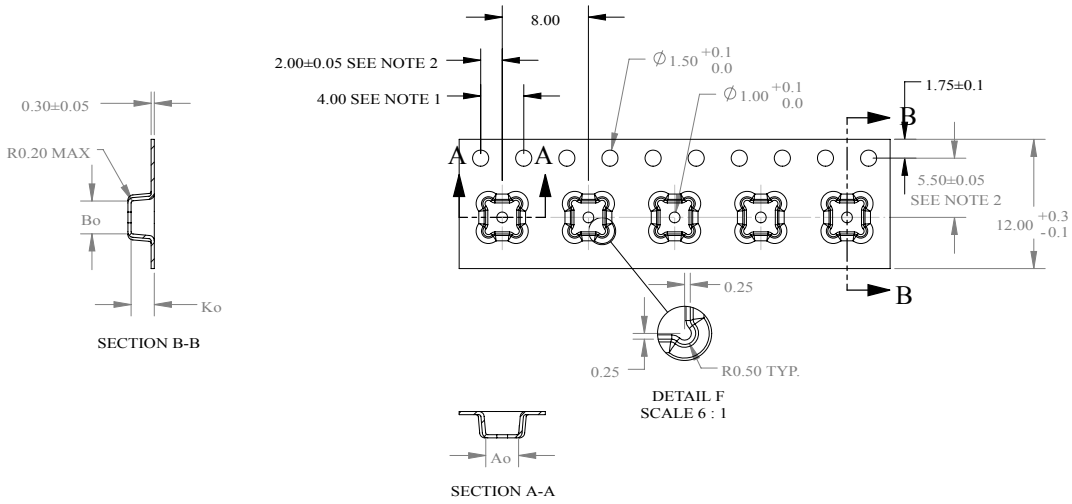
OUTER DIMENSIONS

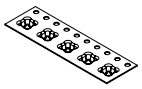
ITEM	DIMENSION (mm)	TOLERANCE (mm)
Length (L)	2.7	±0.1
Width (W)	2.7	±0.1
Height (H)	1.85 Max	/

DM01090684_3

10.2 LGA-11L packing information

Figure 27. Carrier tape information for LGA-11L package





SCALE 1:1

	DIM	±
Ao	3.05	0.05
Bo	3.05	0.05
Ko	2.15	0.10

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 28. LGA-11L package orientation in carrier tape

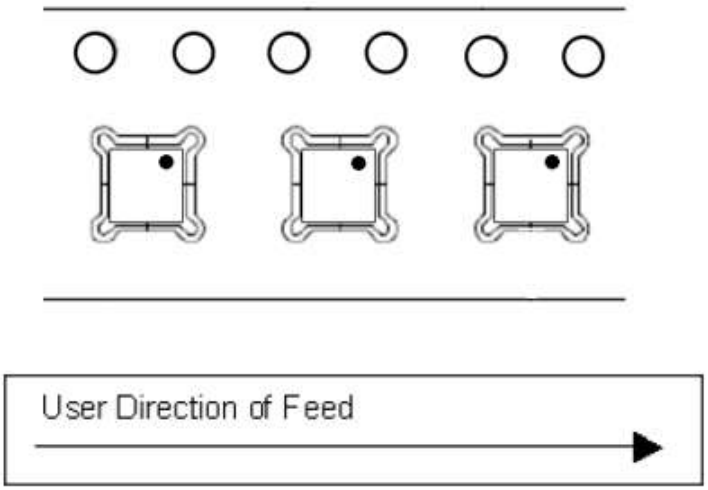


Figure 29. Reel information for carrier tape of LGA-11L package

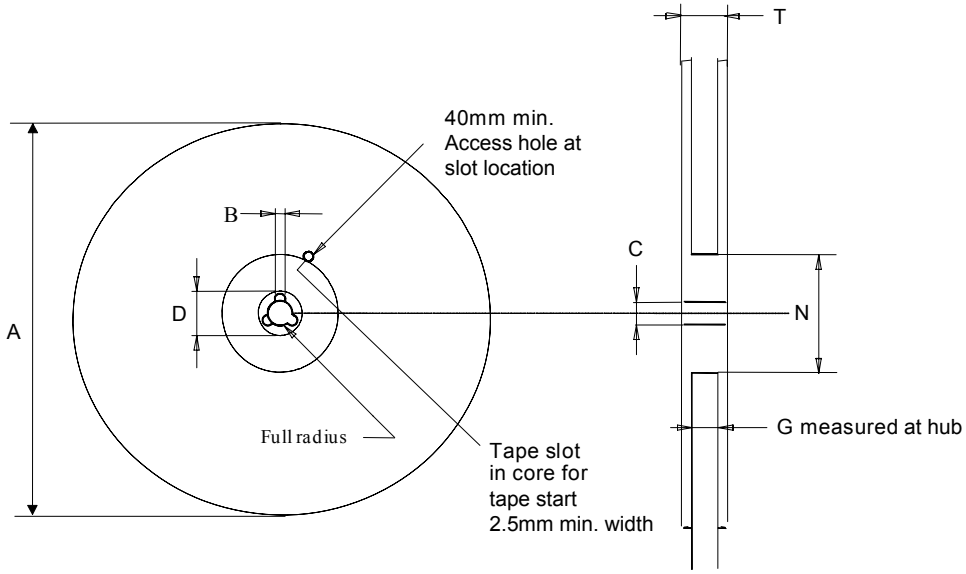


Table 25. Reel dimensions for carrier tape of LGA-11L package

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

Revision history

Table 26. **Document revision history**

Date	Version	Changes
24-Aug-2026	1	Initial release

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