L9962

Datasheet

Battery management system solution

Product status link

L9962

Product label

Features

- 2 µA SHIPMENT - DEEP SLEEP mode current and 2.5 µA standby consumption (with VREG LDO active)
- Integrated 3.3 V VREG LDO for supplying MCU and LEDs
- Measures cell voltage (4 to 10 cells), with over-/undervoltage detection as well as balance undervoltage protection
- 12-bit voltage measurement with maximum error of ±7.5 mV in the [1.5 – 4.5] V range, for -40 °C < T_J < 105 °C
- Measures stack voltage, with over/under voltage detection and plausibility check vs. sum of cells
- Measures pack temperature via NTC, with over-/undertemperature detection
- Ratiometric temperature measurement with ±0.8% max. gain error in the [0.2 – VREG] V range, for -40 °C < T_J < 105 °C
- Measures battery current, with Coulomb counting, overcurrent (both directions) and short-circuit in discharge protection.
- 16-bit signed current measurement with a maximum error of 0.25%, for -40 °C < T_J < 120 °C after customer end of line calibration with a single point
- I^2C peripheral for device programming and data transfers over the I^2C bus
- Cell balancing supporting up to 70 mA per cell
- Dual configurable HS/LS pre-driver for pack relay management
- Pack fuse management
- Embedded NVM for configuration parameters storage with lock functionality
- High hot-plug robustness

Application

- Cordless power tools
- Backup energy storage systems and UPS
- Light electric vehicles (e-bikes, scooters, etc)
- Portable and semi-portable equipment
- Medical equipment

Description

The L9962 is part of a complete battery pack monitoring, balancing, and protection system for Li-Ion and Li-Polymer cells in 4-10 series configurations. The L9962 uses a high precision ADC to provide cell voltage, stack voltage and temperature conversion via external NTC. Voltage monitoring functions are cyclically performed with a programmable loop time. Stack current is also monitored via a high-accuracy CSA, continuously running and also performing Coulomb counting. Cell balancing is available and can be simultaneously activated on all cells. IC configuration and information exchange for SOC/SOH estimation are performed via an I^2C peripheral. The IC also integrates a dual pre-driver programmable in both HS/LS configurations for driving pack relays. The L9962 also implements battery pack fuse protection to prevent fire and explosion hazards. A 3.3 V regulator with a high current capability is available for supplying the pack controller and other external circuitry in both standby and normal operation modes. The IC protects the battery pack against over-/undervoltage conditions and monitors for over-/undertemperature. It also features protection against overcurrent (both directions) and short-circuit in discharge events. Safety-relevant configurations can be stored in the internal NVM to avoid re-programming the device at each wake-up.

1 Pin description and block diagram

1.1 Device pinout

Table 1. Device Pinout

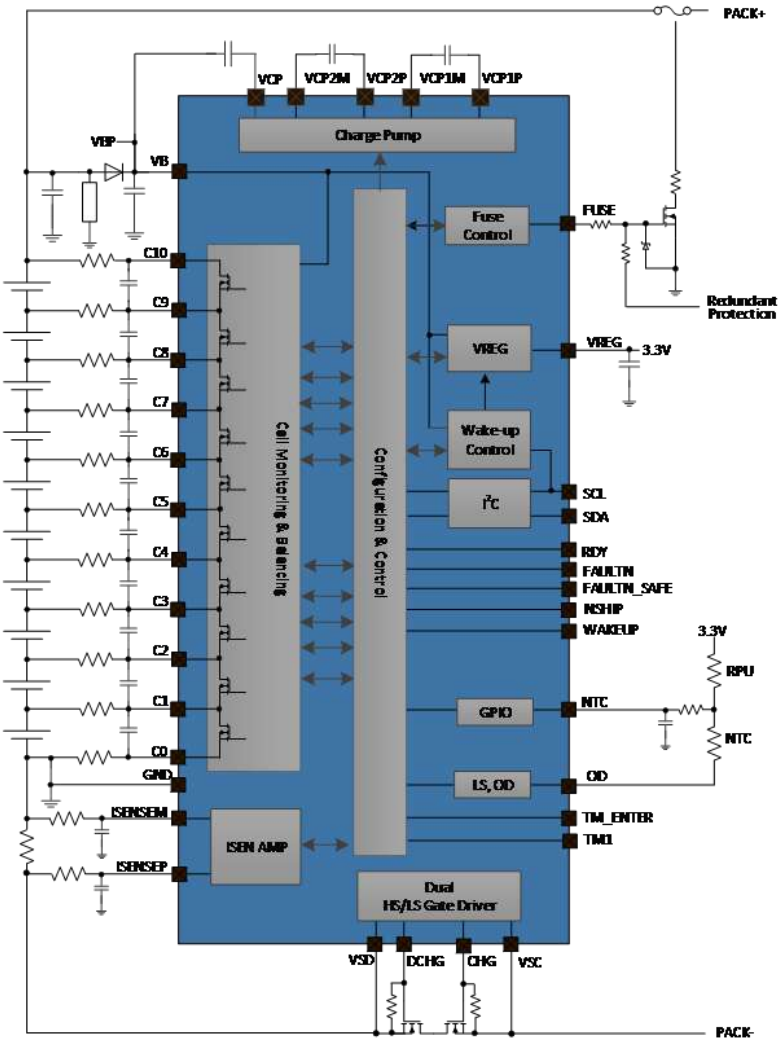
Pin #	Pin name	Pin function	Pin type	Internal PU/PD	Active
1	DNC	Do Not Connect(1)	DNC	-	-
2	DNC	Do Not Connect(1)	DNC	-	-
3	DNC	Do Not Connect(1)	DNC	-	-
4	GND	Device Ground	Ground	-	-
5	DNC	Do Not Connect(1)	DNC	-	-
6	TM1	Reserved for debug. Connect to GND.	-	PD	-
7	DNC	Do Not Connect(1)	DNC	-	-
8	ISENSEP	Current sense ADC positive input terminal	Analog In	-	-
9	ISENSEM	Current sense ADC negative input terminal	Analog In	-	-
10	DNC	Do Not Connect(1)	DNC	-	-
11	VREG	3.3V LDO output	Supply	-	-
12	DNC	Do Not Connect(1)	DNC	-	-
13	NTC	NTC sensing input	Analog In	-	-
14	OD	Open-drain switch for NTC connection to GND	Open Drain	-	Low
15	FAULTN_SAFE	Critical fault output	Open Drain	-	Low
16	FAULTN	Fault output / external CHG/DCHG shutdown trigger	Digital Input/Open Drain	-	Low
17	TM_ENTER	Reserved for debug. Connect to GND.	-	PD	-
18	RDY	Ready interrupt output	Digital output Push/ Pull	-	-
19	SDA	I2C Data line	Digital Input/Open Drain	-	Low
20	SCL	I2C Clock line	Digital Input	-	Low
21	DNC	Do Not Connect(1)	DNC	-	-
22	WAKEUP	Wake-up from STANDBY input	Digital I/O	PD	High
23	NSHIP	Wakeup from SHIPMENT - DEEP SLEEP input	Analog input	-	High
24	FUSE	Fuse input/output	Analog	-	-
25	VB	Battery input	Supply	-	-
26	DCHG	Discharge switch gate	Analog	-	-
27	VSD	Discharge switch source	Analog	-	-
28	VSC	Charge switch source	Analog	-	-
29	CHG	Charge switch gate	Analog	-	-
30	DNC	Do Not Connect(1)	DNC	-	-
31	VCP1M	Charge pump 1st stage negative flying node	Analog	-	-
32	VCP1P	Charge pump 1st stage positive flying node	Analog	-	-
33	VCP2M	Charge pump 2nd stage negative flying node	Analog	-	-

Pin #	Pin name	Pin function	Pin type	Internal PU/PD	Active
34	VCP2P	Charge pump 2nd stage positive flying node	Analog	-	-
35	VCP	Charge pump output	Supply	-	-
36	DNC	Do Not Connect(1)	DNC	-	-
37	VBCP	Battery supply input/Charge pump ground. Connect to VB on PCB	Supply	-	-
38	C10	Cell sensing/balancing terminal	Analog	-	-
39	C9	Cell sensing/balancing terminal	Analog	-	-
40	C8	Cell sensing/balancing terminal	Analog	-	-
41	C7	Cell sensing/balancing terminal	Analog	-	-
42	C6	Cell sensing/balancing terminal	Analog	-	-
43	C5	Cell sensing/balancing terminal	Analog	-	-
44	C4	Cell sensing/balancing terminal	Analog	-	-
45	C3	Cell sensing/balancing terminal	Analog	-	-
46	C2	Cell sensing/balancing terminal	Analog	-	-
47	C1	Cell sensing/balancing terminal	Analog	-	-
48	C0	Cell sensing/balancing terminal	Analog	-	-
EP	EP	Exposed pad			

1. *Do Not Connect pins are internally floating and shall be connected to GND at PCB level for enhancing EMC robustness.*

1.2 Block diagram

Figure 1. **Block diagram**



2 Product electrical ratings

2.1 Operating Range (OR)

Within the operating range, the part operates as specified and without parameter deviations. The device may not operate properly if maximum operating conditions are exceeded.

Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation, unless AMR values are exceeded.

Additional supply voltage and temperature conditions are given separately at the beginning of each electrical specification table.

Table 2. Operating ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
VB, VBCP	Battery level	5.7		50	V
VCP	Charge pump tank output pin		VB+12V		V
VCP1P, VCP2P, VCP1M, VCP2M	Charge pump flying capacitor pin	0		VCP	V
C1, C2, C3, C4, C5, C6, C7, C8	Cell terminal pins	0		VB-3	V
C9	Cell terminal pins	0		VB	V
C10	Cell terminal pins	0		VB+0.6	V
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10	Cell terminal differential voltage	1		4.7	V
VREG	3.3V regulated voltage		3.3		V
NTC	Analog input pin	0		VREG	V
OD	Open-drain pin	0		VREG	V
SDA, SCL	Digital input pins	0		VREG	V
FAULTN_SAFE, RDY, FAULTN	Digital output pin	0		VREG	V
WAKEUP	Analog input pin	0		VB	V
NSHIP	Analog input pin	0		VB	V
FUSE	Analog output pin	0		VB	V
VSD	Discharge MOS source	-1		VB+1	V
VSC	Charge MOS source	-1		VB+1	V
CHG	Charge MOS gate	VSC		Min(VCP; VSC + 12V)	
DCHG	Discharge MOS gate	VSD		Min(VCP; VSD + 12V)	
|ISENSEP – ISENSEM|	CSA input differential mode Range	-200		300	mV
(|ISENSEP + ISENSEM|) /2	CSA input common-mode Range	-200		200	mV
GND	Device ground		0		V
TM1	Device ground		0		V
TM_ENTER	Device ground		0		V
C0	Cell terminal voltage	-0.15		0.15	V

2.2 Absolute Maximum Ratings (AMR)

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

All voltages are related to the potential at substrate ground GND.

Table 3. Absolute maximum ratings

Symbol	Min.	Typ.	Max.	Unit
VREG	-0.3		4.3	V
SCL, SDA, RDY, NTC, OD, TM1	-0.3		Min(VREG+0.3;4.6)	V
ISENSEP, ISENSEM	-2		Min(VREG+0.3;4.6)	V
VB, VBCP, FUSE, NSHIP, WAKEUP	-0.3		60	V
C10	Max(-0.3;C9-0.3)		60	V
C(n), n = 1 to 9	Max(-0.3;C(n-1)-0.3)		Min(C(n+1)+0.3;60)	V
C0	-0.3		Min(C1+0.3;6)	V
VSC	-7		Min(CHG+0.3;+60)	V
VSD	-7		Min(DCHG+0.3;+60)	V
FAULTN_SAFE, FAULTN, TM_ENTER	-0.3		6	V
CHG	VSC-0.3		Min(VCP+0.3;VSC+20;80)	V
DCHG	VSD-0.3		Min(VCP+0.3;VSD+20;80)	V
VCP, VCP1P	VBCP-0.3		Min(VBCP+20;80)	V
VCP1M,VCP2M	Max(-0.3;VBCP-10)		Min(VBCP+0.3;60)	V
VCP2P	VCP1P-0.3		Min(VB+20;80)	V
GND		0		V

2.3 ESD ratings

Table 4 lists the device ESD ratings.

Table 4. ESD protection

Item	Parameter	Condition	Min.	Max.	Unit
All pins	HBM	Tested per AEC-Q100-002	-2	2	kV
All pins	CDM	Tested per AEC-Q100-011	-500	500	V
All pins	Latch-Up	Tested per AEC-Q100-004, Class-2	-100	100	mA

2.4 Thermal ratings

Table 5 lists the device thermal ratings.

Table 5. Thermal ratings

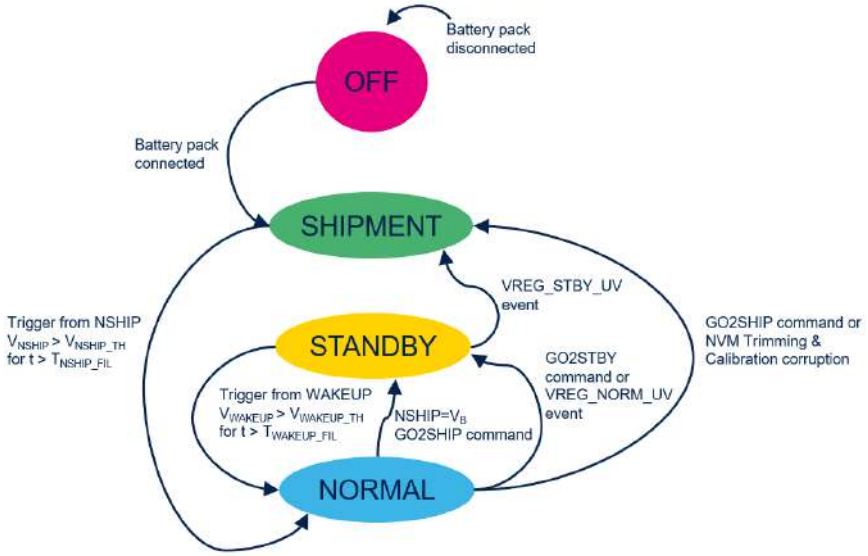
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{amb}	Operating and testing temperature		-40		85	°C
T_j	Junction temperature for all parameters		-40		120	°C
T_{stg}	Storage temperature		-55		150	°C
R_{TH_ja}	Junction to ambient thermal resistance	According to JEDEC standard on 2s2p PCB		31.1		°C/W
		On L9962 EVAL Board		TBD		°C/W

3 Functional description

3.1 Device functional states

The L9962 can operate in three different states when the battery is connected: SHIPMENT - DEEP SLEEP, STANDBY or NORMAL.

Figure 2. Device FSM



3.1.1 SHIPMENT - DEEP SLEEP

The SHIPMENT - DEEP SLEEP state is recommended for pack shipping and storage purposes. When in this state, L9962 current consumption from the VB pin is reduced to just I_{VB_SHIP}, allowing long periods of inactivity to reduce battery pack discharge.

When the battery pack is first connected (L9962 receives VB supply for the first time), the device transitions to either SHIPMENT - DEEP SLEEP state or NORMAL state depending on the NSHIP pin. If NSHIP is biased to the VB pin, the device starts in NORMAL state, otherwise the devices begins in SHIPMENT - DEEP SLEEP state.

The device can enter SHIPMENT - DEEP SLEEP from NORMAL state upon receiving a GO2SHIP command or if the VREG voltage drops below the minimum level ($V_{VREG\_STBY\_UV}$) required to supply the device.

To avoid inadvertent reactivation, the NSHIP pin shall be set low before sending the GO2SHIP command, and it shall be kept low during the transition to SHIPMENT - DEEP SLEEP.

Sending a GO2SHIP command while NSHIP is high will cause the device to enter STANDBY state.

3.1.2 STANDBY

The STANDBY state is recommended to manage short periods of inactivity, where wake-up from the MCU is needed. While in STANDBY, L9962 current consumption from the VB pin is reduced to I_{VB_STBY}.

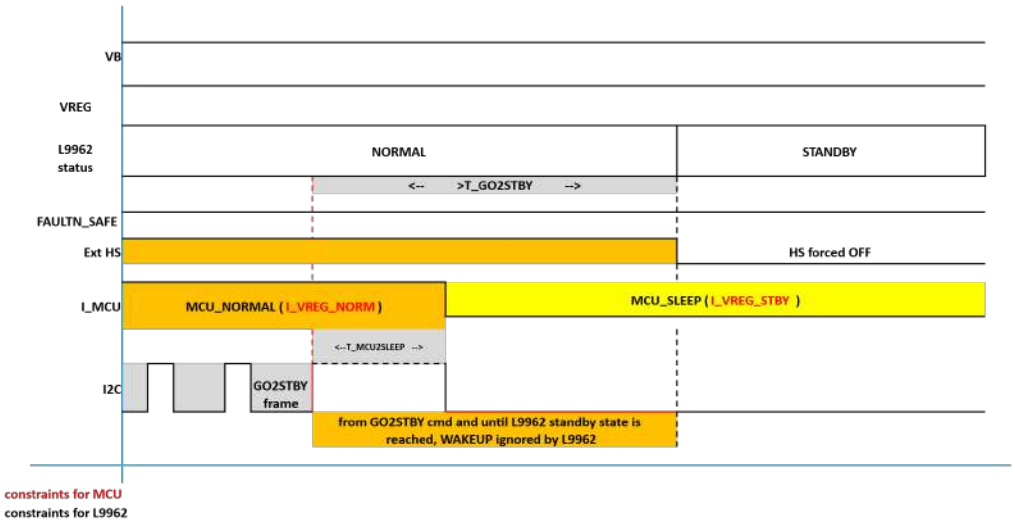
The device is powered but no system functions are available, except for WAKEUP sensing and the VREG regulator which operates with reduced performance characteristics. While VREG is operational, the FAULTN_SAFE pin is released, allowing the MCU to operate in lower power mode.

STANDBY state can be reached from NORMAL state, upon receiving a GO2STBY command through I^2C communications, or if VREG drops below the minimum level ($V_{VREG\_NORM\_UV}$) required for the L9962 to correctly perform its normal features.

Once the L9962 acknowledges the GO2STBY command, it moves to STANDBY state after $T_{GO2STBY}$. To allow a smooth transition, the MCU must move to a low-power state (where its average current consumption is less than I_{VREG_STBY}) within $T_{MCU2STBY}$ after sending a GO2STBY command to L9962.

To avoid inadvertent reactivation, the WAKEUP pin shall be set low before sending the GO2STBY command, and it shall be kept low during the transition to STANDBY state.

Figure 3. Timing diagram: transition from NORMAL to STANDBY upon GO2STBY command



3.1.3 NORMAL

The NORMAL state is recommended during system operation. All IC functions are active, including voltage/temperature/current monitoring and protection. Pack relay management and the I^2C peripheral are also available.

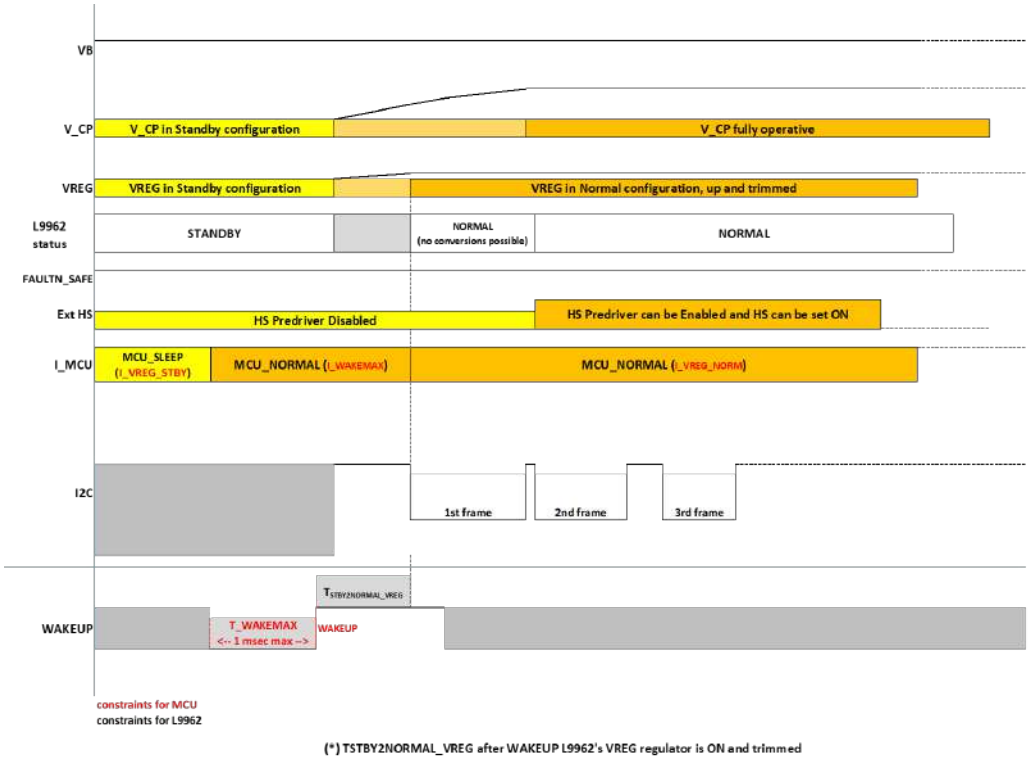
L9962 current consumption from the VB pin while in NORMAL state varies over time, due to the execution of periodical tasks, balancing activation/deactivation, and pre-driver turn on/off events.

NORMAL state can be reached:

- From STANDBY state, if the WAKEUP pin is higher than V_{WAKEUP_TH} for at least T_{WAKEUP_STBY}. Refer to Figure 4.
  - The wake-up source can be either an external stimulus (push button or other) or the system MCU asserting the WAKEUP pin via GPIO (refer to Figure 1).
  - Transition from STANDBY to NORMAL must be properly handled, as the VREG regulator needs to switch from reduced performance to full power within a defined time window. Such an operation requires $T_{STBY2NORMAL}$ from the receipt of the WAKEUP condition to be accomplished.
  - During $T_{STBY2NORMAL}$, VREG can sustain a load current up to IWAKEMAX for a maximum $T_{WAKEMAX}$ time interval, within which the MCU must wake up the L9962.
  - After $T_{STBY2NORMAL}$, the VREG regulator has reached its NORMAL state specification. An RDY pulse is generated to mark the transition to NORMAL. This allows the MCU to fully operate in its normal state, respond to watchdog, serve interrupts, and so on. The L9962 is capable of decoding I^2C commands and receiving new configurations.
  - It takes $T_{CP\_STARTUP}$ from the receipt of the WAKEUP condition for the charge pump to be ready. After $T_{CP\_STARTUP,}$ the L9962 will run monitoring/diagnostic tasks and manage the pre-driver stage.
  - Once the L9962 is in NORMAL state, the MCU is expected to set the WAKEUP pin low to reduce current consumption.
- From SHIPMENT - DEEP SLEEP state, if the NSHIP pin is higher than V_{NSHIP_TH} for at least T_{WAKEUP_NSHIP}.
  - After $T_{SHIP2NORMAL}$, the VREG regulator has reached its NORMAL state specification. An RDY pulse is generated to mark the transition to NORMAL. This allows the MCU to fully operate in its normal state, respond to watchdog, serve interrupts, and so on. The L9962 is capable of decoding I^2C commands and receiving new configurations.
  - MCU should still wait for $T_{CP\_STARTUP}$ when out of reset, before trying to operate the pre-driver stage.

Upon receipt of a wake-up condition, transitions to other states are masked until NORMAL state has been fully reached. Once the device enters NORMAL state, the logic starts a $T_{VREG\_UV\_BLK}$ blanking time on the VREG UV comparator in order to prevent erroneously flagging UV conditions that would bring the L9962 back to STANDBY state.

Figure 4. Timing diagram: transition from STANDBY to NORMAL upon WAKEUP detection



3.1.4 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise specified: VB according to the operating range in Table 2; T_j according to the operating range in Table 5

Table 6. L9962 operating states electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{VB_SHIP}	Consumption from VB pin when in SHIPMENT - DEEP SLEEP	-30°C< T_{amb}=T_j <60°C			2	uA
I_{VB_STBY}	Consumption from VB pin when in STANDBY	-30°C< T_{amb}=T_j <60°C No load on VREG		2.5	7	uA
I_{VB_NORM}	Consumption from VB pin when in NORMAL	NORMAL state, CHG/DHCG OFF, no load on VREG, no communication, Balancing OFF, FAULTN_SAFE and FAULTN released, CSA disabled.		155	190	uA
$I_{VB\_NORM\_DELTA\_CSA}$	Additional current consumption from VB when current ADC is converting	CSA_EN = 1 CC_ACC_EN = 1 OVC_EN = 1 SC_EN = 1		90	125	uA
$I_{VB\_NORM\_DELTA\_CONV}$	Additional current consumption from VB when voltage ADC is continuously converting			135	190	uA
$I_{VB\_NORM\_DELTA\_BAL\_VB}$	Additional current consumption from VB pin due to 1 Balance ON, C1 to C9	Normal condition, additional contribution for 1 Balance ON		8	12	uA
$I_{VB\_NORM\_DELTA\_BAL\_CP}$	Additional current consumption from VB pin due to 1 Balance ON, C10	Normal condition, additional contribution for 1 Balance ON		16	24	uA
$I_{VB\_NORM\_DELTA\_FET\_HS}$ (1)	Additional current consumption from VB pin due to 1 Ext HS FET ON	Normal condition, additional contribution for 1 Ext FET ON. HS Configuration No ext R mounted		9	20	uA
$I_{VB\_NORM\_DELTA\_FET\_LS}$	Additional current consumption from VB pin due to 1 Ext LS FET ON	Normal condition, additional contribution for 1 Ext FET ON. LS Configuration No ext R mounted		15	20	uA
I_{VB_DELTA}	VB pin current consumption when voltage ADC is converting, current ADC is converting, Ext FETs enabled & T_{MEAS_CYCLE} = 10ms	Application info		350	420	uA
$I_{VB\_NORM\_DELTA\_VB\_UVLO}$	Additional current consumption from VB when VB UVLO diagnostic is enabled	VB_UVLO_EN = 1		13	20	uA
$V_{VB\_TRAN\_NORM}$	Max. allowed transient slope on VB pin	Application info			1	V/us

1. *In HS case, an additional current contribution must be added to include the effect of charge pump switching activity at an increased frequency. This contribution is impacted by the external parasitic capacitances between each CP pin and GND in the range of 3 µA/pF.*

3.2 Wake-up sources (NSHIP/WAKEUP)

The L9962 can be woken up via two dedicated pins:

- NSHIP can be used as wake-up from SHIPMENT - DEEP SLEEP
- WAKEUP can be used as wake-up from STANDBY

3.2.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise noted: VB according to the operating range in Table 2; T_j according to the operating range in Table 5

Table 7. VREG electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{WAKEUP_TH}	WAKEUP wake-up threshold		0.8		1.8	V
V_{NSHIP_TH}	NSHIP wake-up threshold		1		3	V
T_{WAKEUP_FIL}	WAKEUP filter time				40	us
T_{NSHIP_FIL}	NSHIP filter time				20	us
T_{WAKEUP_NSHIP}	NSHIP assertion time to guarantee correct device wake-up from shipment		1			ms
R_{WAKEUP_PD}	WAKEUP pull-down resistor		50	100	150	kΩ
$T_{MCU2STBY}$	Maximum delay from sending GO2STBY command to MCU in low-power mode	Application info			1	ms
$T_{GO2STBY}$	Maximum delay from receipt of GO2STBY command to L9962 in STANDBY state	Application info	2		4	ms
$T_{GO2SHIP}$	Time delay for L9962 from received GO2SHIP command from MCU to enter SHIPMENT - DEEP SLEEP state	Application info	0		10	ms
$I_{WAKEMAX}$	VREG current capability in STANDBY to NORMAL state transition, during $T_{WAKEMAX}$ interval	Application info			15	mA
$T_{WAKEMAX}$	MCU time in NORMAL mode to send a WAKEUP command to L9962	Application info			1	ms
$T_{STBY2NORMAL}$	Time to complete STANDBY to NORMAL transition	From WAKEUP assertion to VREG_UV release			1	ms
$T_{SHIP2NORMAL}$	Time to complete SHIPMENT - DEEP SLEEP to NORMAL transition	From NSHIP assertion to VREG UV release. No load on VREG, 4.7uF capacitance present.			5	ms
T_{I2C_READY}	I^2C settling time	From WAKEUP/NSHIP assertion to I^2C ready			15	ms
$T_{CP\_STARTUP}$	Charge pump startup time	From VREG_UV release ($T_{VREG\_UV\_BLK}$ expired) to VCP in range			8	ms

3.3 VREG LDO

The L9962 provides a system regulator capable of providing power to the system MCU and other peripheral devices or circuits. Performances of the regulator vary according to the L9962 state:

- In STANDBY state, the regulated voltage is V_{VREG_STBY} and the average current capability is limited to I_{VREG_STBY}. Line/load regulation performances are reduced to $V_{VREG\_LIN\_REG\_STBY}$ and $V_{VREG\_LOAD\_REG\_STBY}$ respectively. The VREG current limit is still active with an $I_{VREG\_CURR\_LIM\_STBY}$ threshold.
- In NORMAL state, the regulated voltage is V_{VREG_NORM}, with an I_{VREG_NORM} average current capability. Line/load regulation performances are defined by $V_{VREG\_LIN\_REG\_NORM}$ and $V_{VREG\_LOAD\_REG\_NORM}$ respectively. The VREG current limit is active with an $I_{VREG\_CURR\_LIM}$ threshold.

3.3.1 Electrical Parameters

All parameters are tested and guaranteed in the following conditions, unless otherwise noted:
VB according to the operating range in Table 2; T_j according to the operating range in Table 5

Table 8. VREG electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{VREG_NORM}	Regulated voltage	NORMAL state 10uA<Iload<30mA	3.23	3.3	3.37	V
I_{VREG_NORM}	Current load range	NORMAL state Design info	0.01		35	mA
$I_{VREG\_CURR\_LIM}$	Current limitation	NORMAL state VREG=2.9V	40			mA
$I_{VREG\_CURR\_LIM\_STBY}$	Current limitation	STANDBY state VREG=2.6V	15			mA
$V_{VREG\_LIN\_REG\_NORM}$	Dynamic line regulation in NORMAL	NORMAL state VB from 5.7V to 50V in 100us Iload=100uA, 30mA Guaranteed by design	-150		+150	mV
$V_{VREG\_LOAD\_REG\_NORM}$	Static load regulation	NORMAL state Iload from 100uA to 30mA (both transitions), pulse 100us	-160		+160	mV
V_{VREG_STBY}	Regulated voltage	STANDBY state -30°C<T_{amb}=T_j<60°C	2.8		3.5	V
I_{VREG_STBY}	Output current	STANDBY state -30°C<T_{amb}=Tj<60°C Application info	1		300	uA
$V_{VREG\_LIN\_REG\_STBY}$	Dynamic line regulation in STANDBY	STANDBY state VB from 5.7V to 22V in 100us Iload=0, 50uAGuaranteed by design	-250		+250	mV
$V_{VREG\_LOAD\_REG\_STBY}$	Static load regulation in STANDBY	STANDBY state Iload= step 0-50uA in 100us	-400		+400	mV
$V_{VREG\_LOAD\_REG\_STBY\_OVL}$	Overload regulation in STANDBY	STANDBY state Iload= step 0-$I_{WAKEMAX}$, pulse lasting $T_{WAKEMAX}$ -30°C< Ta=Tj <60°C	2.7			V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{VREG\_NORM\_UV}$	VREG Undervoltage threshold in NORMAL state		2.6	2.7	2.9	V
$T_{VREG\_UV\_FIL}$	VREG UV filter time in NORMAL state			20		us
$T_{VREG\_UV\_BLK}$	VREG UV blanking time upon transition to NORMAL state		8			ms
$V_{VREG\_STBY\_UV}$	VREG Undervoltage threshold in STANDBY state	STANDBY state	2.1	2.5	2.8	V
C_{REG}	External LDO capacitance	Application info, required for stability	-20%	4.7	+20%	uF

3.4 Voltage conversion routine

While in NORMAL state, the L9962 cyclically executes the voltage conversion routine as shown in Figure 5. Task execution time is T_{ADCV_CONV}, which is the sum of the individual step durations:

- N_{CELL} represents the number of enabled cells. The T_{CELL_FILTER} filter time is applied to each cell conversion. At least 4 cells must be converted
- The T_{CELL_FILTER} filter time is also applied to VB pin conversion (if enabled)
- The T_{TEMP_FILTER} filter time is applied to NTC conversion (if enabled)
- The T_{TEMP_FILTER} filter time is applied to die temperature conversion, which is always performed

The task is scheduled to run every T_{MEAS_CYCLE} (programmable in TCYCLE field). Changing configuration parameters while a conversion is ongoing may result in inadvertent faults and reactions. The MCU is supposed to disable the voltage conversion routine programming T_{MEAS_CYCLE} = 0x0 before applying any new configuration set. To guarantee data integrity, in case T_{MEAS_CYCLE} = 0x0 is set while the routine is ongoing, the procedure is not halted, but runs until the last enabled step holding the previously stored configuration. Any new configuration update will be latched, if TMEAS_CYCLE != 0x0 is written, once the new measurement loop starts.

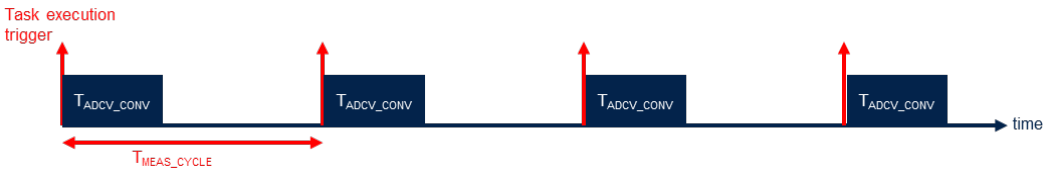
Figure 5. Voltage conversion routine steps

Table 9. Voltage conversion routine execution parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{MEAS_CYCLE}	Programmable voltage conversion routine execution period (5-bit) T_{MEAS_CYCLE}=20ms * CODE		20		620	ms

The task execution period T_{MEAS_CYCLE} must always be greater than the task duration. In case the task execution period is programmed shorter than the task duration, this will result in the task being executed at a random periodicity.

Figure 6. Correct management of the task execution periodicity



3.4.1 Cell voltage monitor (Cx)

During the cell voltage monitoring step, the voltage conversion routine measures differential voltages at the Cx pins and stores results in the VCELL<x> registers. The digital sum of cells is stored in the VCELL_SUM_MEAS register.

A cell is converted only if its corresponding VCELL<x>_EN bit is enabled. By default, all cells are disabled. At least 5 cells must be enabled in order to guarantee proper operation.

If fewer than 10 cells are used:

- Mount the cells starting from the top-most pair (C10-C9)
- A minimum of 5 cells must be connected to the L9962 and the top-most cell of the stack must be connected to the C5 pin.

Measurements are compared to programmable thresholds to detect the failures listed in Table 10.

Table 10. **Cell voltage monitor diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Cell UV	• If a cell voltage falls below VCELL_UV_TH, the corresponding UV counter is incremented by 1 • If the UV counter reaches VCELL_UV_CNT_TH, cell UV fault is acknowledged.	• The CELL<x>_UV flag is set • The Discharge FET is turned OFF • FAULTN line is asserted	• If a cell voltage rises above VCELL_UV_TH, the corresponding UV counter is decremented by 1. • If the UV counter reaches zero, the cell UV flag can be cleared by MCU	• The Discharge FET is restored to the status defined by the DCHG_ON bit • FAULTN line is released	• VCELL<x>_EN masks measurement execution. The UV flag of a disabled cell can always be cleared • CELL_UV_PRDRV_MSK masks reaction on DCHG pin • CELL_UV_FAULTN_MSK masks reaction on FAULTN pin
Cell Severe UV	• If a cell voltage falls below VCELL_SEVERE_UV_TH, a severe UV fault is acknowledged	• The CELL<x>_SEVERE_UV flag is set • The Discharge FET is turned OFF • FUSE pre-driver is enabled • FAULTN line is asserted	• If a cell voltage rises above VCELL_SEVERE_UV_TH, the cell severe UV flag can be cleared by MCU	• The Discharge FET is restored to the status defined by the DCHG_ON bit • FUSE pre-driver is disabled • FAULTN line is released	• VCELL<x>_EN masks measurement execution. The severe UV flag of a disabled cell can always be cleared • CELL_SEVERE_UV_PRDRV_MSK masks reaction on DCHG pin • CELL_SEVERE_UV_FUSE_MSK masks reaction on FUSE pin • CELL_SEVERE_UV_FAULTN_MSK masks reaction on FAULTN pin
Cell OV	• If a cell voltage rises above $V_{CELL\_OV\_TH}$, the corresponding OV counter is incremented by 1 • If the OV counter reaches VCELL_OV_CNT_TH, cell OV fault is acknowledged.	• The CELL<x>_OV flag is set • The Charge FET is turned OFF • FAULTN_SAFE is pulled low for $T_{FAULTN\_SAFE\_LOW}$ • FAULTN line is asserted	• If a cell voltage falls below VCELL_OV_TH, the corresponding OV counter is decremented by 1. • If the OV counter reaches zero, the cell OV flag can be cleared by MCU	• The Charge FET is restored to the status defined by the CHG_ON bit • FAULTN line is released	• VCELL<x>_EN masks measurement execution. The OV flag of a disabled cell can always be cleared • CELL_OV_PRDRV_MSK masks reaction on CHG pin • CELL_OV_RST_MSK masks reaction FAULTN_SAFE pin • CELL_OV_FAULTN_MSK masks reaction on FAULTN pin

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Cell Severe OV	• If a cell voltage rises above VCELL_SEVERE_OV_TH, a severe OV fault is acknowledged	• The CELL<x>_SEVERE_OV flag is set • The Charge FET is turned OFF • FUSE pre-driver is enabled • FAULTN_SAFE is pulled low for $T_{FAULTN\_SAFE\_LOW}$ • FAULTN line is asserted	• If a cell voltage falls below VCELL_SEVERE_OV_TH, the cell severe OV flag can be cleared by MCU	• The Charge FET is restored to the status defined by the CHG_ON bit • FUSE pre-driver is disabled • FAULTN line is released	• VCELL<x>_EN masks measurement execution. The severe OV flag of a disabled cell can always be cleared • CELL_SEVERE_OV_PRDRV_MSK masks reaction on CHG pin • CELL_SEVERE_OV_FUSE_MSK masks reaction on FUSE pin • CELL_SEVERE_OV_RST_MSK masks reaction FAULTN_SAFE pin • CELL_SEVERE_OV_FAULTN_MSK masks reaction on FAULTN pin
Cell Balance UV	• If a cell voltage falls below VCELL_BAL_UV_TH, the corresponding Bal UV counter is incremented by 1 • If the Bal UV counter reaches VCELL_BAL_UV_CNT_TH, it stops incrementing and the Bal UV fault is acknowledged	• The BAL<x>_UV flag is set • Any ongoing balancing is stopped on the affected cell, regardless of BAL<x>_ON bit • FAULTN line is asserted	• If a cell voltage rises above VCELL_BAL_UV_TH, the corresponding Bal UV counter is decremented by 1. • If the Bal UV counter reaches zero, the Bal UV flag can be cleared by MCU	• The Balancing FET is restored to the status defined by the corresponding BAL<x>_ON bit • FAULTN line is released	• VCELL<x>_EN masks measurement execution. The Bal UV flag of a disabled cell can always be cleared • BAL_UV_BAL_MSK masks reaction on balancing • BAL_UV_FAULTN_MSK masks reaction on FAULTN pin

3.4.1.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise specified: VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 11. Cell voltage monitor electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CELL_RANGE}	Cell voltage input measurement range	Design info	1		4.7	V
V_{CELL_RES}	Cell voltage measurement resolution	Design info		1.22		mV
N_{BIT}	ADC bit number	Design info		12		bit
V_{CELL_MEAS}	Programmable cell measurement (8 bit) $V_{CELL_{MEAS}} = V_{CELL\_RES} * CODE$	Design info				
I_{CELL_LEAK}	Cx leakage current	ADC not converting			500	nA
$V_{CELLERR1}$	ADC Total conversion error range 1	1 V ≤ V_{CELL} < 1.5 V -40°C< Tj < 120°C	-15		15	mV
$V_{CELLERR2}$	ADC Total conversion error range 2	1.5 V ≤ V_{CELL} ≤ 4.5 V -40°C< Tj < 105°C	-7.5		7.5	mV
$V_{CELLERR3}$	ADC Total conversion error range 3	4.5 V ≤ V_{CELL} ≤ 5 V -40°C< Tj < 120°C	-15		15	mV
$V_{CELLERR4}$	ADC Total conversion error range 4	1.5 V ≤ VCELL ≤ 4.5 V 105 °C < Tj < 120 °C	-25		25	mV
V_{CELL_NOISE}	Cell conversion noise			1		LSBrms
$T_{CELL\_FILTER1}$	Cell and VB acquisition filter time			0.8		ms
$T_{CELL\_FILTER2}$	Cell and VB acquisition filter time			1.31		ms
$T_{CELL\_FILTER3}$	Cell and VB acquisition filter time			4.38		ms
$T_{CELL\_FILTER4}$	Cell and VB acquisition filter time			16.67		ms
$V_{CELL\_OV\_TH}$	Programmable cell OV fault threshold (8 bit) $V_{CELL_{OVTH}} = 16V_{CELL\_RES} * CODE$		0		5	V
$N_{CELL\_OV\_CNT\_TH}$	Programmable cell OV event counter threshold (4 bit)		1		15	events
$V_{CELL\_SEVERE\_OV\_DELTA\_TH}$	Programmable cell severe OV threshold (positive delta in respect to cell OV threshold, 8 bit) $V_{CELL_{SEVERE_{OV_{TH}}}} = V_{CELL_{OV_{TH}}} + 16V_{CELL\_RES} * CODE$ In case of overflow, the $V_{CELL_{SEVERE_{OV_{TH}}}}$ is saturated to the max specified value		0		5	V
$V_{CELL\_UV\_TH}$	Programmable cell UV fault threshold (8 bit) $V_{CELL_{UVTH}} = 16V_{CELL\_RES} * CODE$		0		5	V
$N_{CELL\_UV\_CNT\_TH}$	Programmable cell UV event counter threshold (4 bit)		1		15	events

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CELL\_SEVERE\_UV\_DELTA\_TH}$	Programmable cell Severe OV threshold (negative delta in respect to cell UV threshold, 8 bit) $V_{CELL_{SEVERE_{UV_{TH}}}} = V_{CELL_{UV_{TH}}} - 16V_{CELL\_RES} * CODE$ In case of underflow, the $V_{CELL_{SEVERE_{UV_{TH}}}}$ is saturated to the min specified value		0		5	V
$V_{CELL\_BAL\_UV\_DELTA\_TH}$	Programmable Balancing UV threshold (positive delta in respect to cell UV threshold, 8 bit) $V_{CELL_{BAL_{UV_{TH}}}} = V_{CELL_{UV_{TH}}} + 16V_{CELL\_RES} * CODE$ In case of overflow, the $V_{CELL_{BAL_{UV_{TH}}}}$ is saturated to the max specified value		0		5	V
$N_{CELL\_BAL\_UV\_CNT\_TH}$	Programmable Balance UV event counter threshold (4 bit)		1		15	events
$T_{POST\_PROCESSING}$	Postprocessing time during conversion routine			40		us

3.4.2 Battery Stack Monitor (VB)

The battery stack monitor, VB, of the voltage conversion routine monitors the battery stack voltage measuring the VB pin through an internal divider.

This function is enabled by programming the corresponding VB_EN I2C bit: if disabled, this step is skipped. To limit power consumption, the internal voltage divider is connected to the VB pin at the beginning of the Voltage conversion routine and it is disconnected right after the VB measurement step is completed.

Stack voltage measurements are stored in the VB_MEAS register and compared to programmable thresholds in order to detect the failures listed in Table 12.

Besides cyclic diagnostics performed by the Voltage conversion routine, the IC implements a time-continuous VB pin monitor, which can be by enabled setting VB_UVLO_EN = 1. Aged packs at low temperatures may exhibit an abnormal increase in cell resistivity, thus leading to sudden battery voltage undershoots upon system startup or huge load current pulses. If such a condition persists, HS/LS pre-drivers (CHG/DCHG/FUSE) overdrive may decrease, thus causing pack relays overheating and possible damage. The Undervoltage lockout (UVLO) prevents transient brownouts from causing thermal issues to the system by detaching the battery from loads, shutting off the DCHG FET.

Table 12. Battery stack monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VB UV	• If VB voltage falls below VB_UV_TH, the corresponding UV counter is incremented by 1 • If the UV counter reaches VB_UV_CNT_TH, it stops incrementing and the VB UV fault is acknowledged	• The VB_UV flag is set • The Discharge FET is turned OFF • FAULTN line is asserted	• If VB voltage rises above VB_UV_TH, the corresponding UV counter is decremented by 1. • If the UV counter reaches zero, the VB_UV flag can be cleared by MCU	• The Discharge FET is restored to the status defined by the DCHG_ON bit • FAULTN line is released	• VB_EN masks measurement execution. When disabled, the VB_UV flag can always be cleared • VB_UV_PRDRV_MSK masks reaction on DCHG pin • VB_UV_FAULTN_MSK masks reaction on FAULTN pin
VB OV	• If VB voltage rises above VB_OV_TH, the corresponding OV counter is incremented by 1 • If the OV counter reaches VB_OV_CNT_TH, it stops incrementing and the VB OV fault is acknowledged	• The VB_OV flag is set • The Charge FET is turned OFF • FAULTN_SAFE is pulled low for $T_{FAULTN\_SAFE\_LOW}$ • FAULTN line is asserted	• If VB voltage falls below VB_OV_TH, the corresponding OV counter is decremented by 1. • If the OV counter reaches zero, the VB OV flag can be cleared by MCU	• The Charge FET is restored to the status defined by the corresponding I2C bit • FAULTN line is released	• VB_EN masks measurement execution. When disabled, the VB_OV flag can always be cleared • VB_OV_PRDRV_MSK masks reaction on CHG pin • VB_OV_RST_MSK masks reaction FAULTN_SAFE pin • VB_OV_FAULTN_MSK masks reaction on FAULTN pin

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
VB vs. Sum Of Cells plausibility fail	• If the absolute value of the difference between VB_MEAS and VCELL_SUM is greater than VB_VSUM_MAX_DIFF_TH, the plausibility check fail is acknowledged	• The VB_SUM_CHECK_FAIL flag is set • Both Charge and Discharge FETs are turned OFF • Balancing is interrupted on all cells • FUSE pre-driver is enabled • FAULTN line is asserted	• If the absolute value of the difference between VB_MEAS and VCELL_SUM falls below the VB_VSUM_MAX_DIFF_TH, the VB_SUM_CHECK_FAIL flag can be cleared by MCU	• The Charge FET is restored to the status defined by the CHG_ON bit • The Discharge FET is restored to the status defined by the DCHG_ON bit • FUSE pre-driver is disabled • Balancing FETs are restored to the status defined by the corresponding BAL<x>_ON bit • FAULTN line is released	• VB_EN masks measurement execution. When disabled, the VB_SUM_CHECK_FAIL flag can always be cleared • VB_SUM_CHECK_CHG_MSK masks reaction on CHG • VB_SUM_CHECK_DCHG_MSK masks reaction on DCHG • VB_SUM_CHECK_FUSE_MSK masks reaction on FUSE pin • VB_SUM_CHECK_BAL_MSK masks reaction on balancing • VB_SUM_CHECK_FAULTN_MSK masks reaction on FAULTN pin
VB UVLO	• If VB voltage falls below $V_{VB\_UVLO\_TH}$ for longer than $T_{VB\_UVLO\_FIL}$ the VB UVLO fault is acknowledged	• The VB_UVLO flag is set • The Discharge FET is turned OFF • FAULTN line is asserted	• If VB voltage rises above $V_{VB\_UVLO\_TH}$ + $V_{VB\_UVLO\_HYS}$ for longer than $T_{VB\_UVLO\_FIL}$ the VB_UVLO flag can be cleared by MCU	• The Discharge FET is restored to the status defined by the DCHG_ON bit • FAULTN line is released	• VB_UVLO_EN masks diagnostic execution. When disabled, the VB_UVLO flag can always be cleared • VB_UVLO_PRDRV_MSK masks reaction on DCHG pin • VB_UVLO_FAULTN_MSK masks reaction on FAULTN pin

3.4.2.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise specified: VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 13. Battery stack monitor external parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{B_RANGE}	VB voltage input measurement Range	Design info	5.7		50	V
V_{B_RES}	VB voltage measurement Resolution	Design info		12.2		mV
N_{BIT}	ADC bit number	Design info		12		bit
V_{B_MEAS}	Programmable VB voltage measurement (8 bit) $V_{B_{MEAS}} = V_{B\_RES} * CODE$	Design info				
V_{BERR_1}	VB voltage measurement Total	5.3V<VB<9V -40°C< Tj<105°C	-150		150	mV
V_{BERR_2}	VB voltage measurement Total	9V<VB<40V -40°C< Tj<105°C	-100		100	mV
V_{BERR_3}	VB voltage measurement Total	40V<VB< 50V -40°C< Tj<105°C	-150		150	mV
$V_{B\_OV\_TH}$	Programmable VB OV fault threshold (8 bit) $V_{B_{OV_{TH}}} = 16V_{B\_RES} * CODE$		0		50	V
$N_{VB\_OV\_CNT\_TH}$	Programmable VB OV event counter threshold (4 bit)	Tested by SCAN	1		15	events
$V_{B\_UV\_TH}$	Programmable VB UV fault threshold (8 bit) $V_{B_{UV_{TH}}} = 16V_{B\_RES} * CODE$		0		50	V
$N_{VB\_UV\_CNT\_TH}$	Programmable VB UV event counter threshold (4 bit)	Tested by SCAN	1		15	events
$V_{B\_SUM\_MAX\_DIFF\_TH}$	Programmable plausibility check threshold between VB and sum of cells (8 bit) $V_{B\_SUM_{MAX_{DIFF_{TH}}}} = \left\lvert V_B - V_{SUM} \right\rvert = 16V_{B\_RES} * CODE$		0		50	V
$V_{VB\_UVLO\_TH}$	Battery undervoltage lockout (UVLO) threshold	Tested in production	8	9	10	V
$V_{VB\_UVLO\_HYS}$	Battery undervoltage lockout (UVLO) hysteresis	Tested in production	0.8	1	1.2	V
$T_{VB\_UVLO\_FIL}$	Battery undervoltage lockout (UVLO) filter time	Tested by SCAN		100		us

3.4.3 Cell temperature monitor (NTC)

The NTC cell temperature monitoring voltage conversion routine monitors pack temperature by sensing the NTC pin. This function is enabled by programming the NTC_EN bit: if disabled, no conversion occurs.

When NTC_EN = 1, the OD open-drain is switched ON prior to the cells step execution. This allows the voltage on the NTC pin to settle before NTC acquisition is performed. Once the NTC is completed, the OD open-drain switch is released, reducing overall current consumption from VREG.

NTC measurements are stored in the NTC_MEAS register and are compared to programmable thresholds to detect the failures listed in Table 14

Table 14. **NTC temperature monitor diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
NTC OT	• If NTC voltage falls below NTC_OT_TH, the corresponding OT counter is incremented by 1 • If the OT counter reaches NTC_OT_CNT_TH, the NTC OT fault is acknowledged	• The NTC_OT flag is set • The Charge FET is turned OFF • FAULTN line is asserted	• If NTC voltage rises above NTC_OT_TH, the corresponding OT counter is decremented by 1. • If the OT counter reaches zero, the NTC OT flag can be cleared by MCU	• The Charge FET is restored to the status defined by the CHG_ON bit • FAULTN line is released	• NTC_EN masks measurement execution. The OT flag of a disabled NTC can always be cleared • NTC_OT_PRDRV_MSK masks reaction on CHG pin • NTC_OT_FAULTN_MSK masks reaction on FAULTN pin
Severe NTC OT	• If a NTC voltage falls below NTC_SEVERE_OT_TH, the severe OT fault is acknowledged	• The NTC_SEVERE_OT flag is set • Both Charge and Discharge FETs are turned OFF • Balancing is interrupted on all cells • FUSE pre-driver is enabled • FAULTN line is asserted	• If NTC voltage rises above NTC_SEVERE_OT_TH, the severe OT flag can be cleared by MCU	• The Charge FET is restored to the status defined by the CHG_ON bit • The Discharge FET is restored to the status defined by the DCHG_ON bit • FUSE pre-driver is disabled • Balancing FETs are restored to the status defined by the corresponding BAL<x>_ON bit • FAULTN line is released	• NTC_EN masks measurement execution. When disabled, the severe OT flag can always be cleared • NTC_SEVERE_OT_CHG_MSK masks reaction on CHG pin • NTC_SEVERE_OT_DCHG_MSK masks reaction on DCHG pin • NTC_SEVERE_OT_FUSE_MSK masks reaction on FUSE pin • NTC_SEVERE_OT_BAL_MSK masks reaction on balancing • NTC_SEVERE_OT_FAULTN_MSK masks reaction on FAULTN pin

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
NTC UT	• If NTC voltage rises above NTC_UT_TH, the corresponding UT counter is incremented by 1 • If the UT counter reaches NTC_UT_CNT_TH, the NTC UT fault is acknowledged	• The NTC_UT flag is set • Both Charge and Discharge FETs are turned OFF • FAULTN line is asserted	• If NTC voltage falls below NTC_UT_TH, the corresponding UT counter is decremented by 1. • If the UT counter reaches zero, the NTC_UT flag can be cleared by MCU	• The Charge FET is restored to the status defined by the CHG_ON bit • The Discharge FET is restored to the status defined by the DCHG_ON bit • FAULTN line is released	• NTC_EN masks measurement execution. The UT flag of a disabled NTC can always be cleared • NTC_UT_CHG_MSK masks reaction on CHG pin • NTC_UT_DCHG_MSK masks reaction on DCHG pin • NTC_UT_FAULTN_MSK masks reaction on FAULTN pin

3.4.3.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise specified: VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 15. NTC measurement parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{NTC_RANGE}	NTC pin voltage input measurement range	Ratiometric design info	0.2		V_{VREG}	V
V_{NTC_RES}	Cell voltage measurement resolution	Design info		$V_{VREG}/2^{12}$		mV
N_{BIT}	ADC bit number	Design info		12		bit
V_{NTC_MEAS}	Programmable NTC measurement (8 bit) $V_{NTC_{MEAS}} = V_{NTC\_RES} * CODE$	Design info				
I_{NTC_LEAK}	NTC leakage current	ADC not converting			150	nA
$V_{NTC\_GAIN\_ERR}$	NTC gain error	0.2 V ≤ VNTC ≤ VREG -40°C< Tj<105°C	-0.8		+0.8	%
$V_{NTC\_OFFSET\_ERR}$	NTC offset error		-2		+2	LSB
V_{NTC_NOISE}	NTC conversion noise			1		LSB rms
T_{TEMP_FILTER}	NTC acquisition filter time	Tested by SCAN		0.8		ms
$V_{NTC\_OT\_TH}$	Programmable NTC OT threshold (12 bit) $V_{NTC_{OT_{TH}}} = V_{NTC\_RES} * CODE$		0		V_{VREG}	V
$N_{NTC\_OT\_CNT\_TH}$	Programmable NTC OT event counter threshold (4 bit)	Tested by SCAN	1		15	events
$V_{NTC\_SEVERE\_OT\_DELTA\_TH}$	Programmable NTC severe OT threshold (negative delta in respect to NTC OT threshold, 12 bit) $V_{NTC_{SEVERE_{OT_{TH}}}} = V_{NTC_{OT_{TH}}} - V_{NTC\_RES}$ In $* CODE$ case of underflow, the $V_{NTC_{SEVERE_{OT_{TH}}}}$ is saturated to the min. specified value		0		V_{VREG}	V
$V_{NTC\_UT\_TH}$	Programmable NTC UT threshold (12 bit) $V_{NTC_{UT_{TH}}} = V_{NTC\_RES} * CODE$		0		V_{VREG}	V
$N_{NTC\_UT\_CNT\_TH}$	Programmable NTC UT event counter threshold (4 bit)	Tested by SCAN	1		15	events

3.4.4 Die temperature monitor (T_j)

The die temperature step of the voltage conversion routine monitors the L9962 junction temperature. This step is always enabled.

The die temperature is encoded according to the following formula:

$$T_j[°C] = 343.165 - 0.196 * DIE\_TEMP\_MEAS \quad (1)$$

Die temperature measurements are stored in the DIE_TEMP_MEAS register and compared to a programmable threshold in order to detect the failures listed in Table 16.

Note: In case the DIE_OT flag is asserted, the MCU is expected to move the device to a low-power state (either SHIPMENT-DEEP SLEEP or STANDBY) within 500 ms in order to prevent damage from overheating.

Table 16. Die temperature monitor diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
DIE OT	• If die temperature rises above T_{OT_TH}, the DIE_OT fault is acknowledged	• The DIE_OT flag is set • Both Charge and Discharge FETs are turned OFF • Balancing is interrupted on all cells • FAULTN line is asserted	• If die temperature falls below $T_{OT\_TH} - T_{OT\_HYST}$, the DIE_OT flag can be cleared by MCU	• Charge FET is restored to the status defined by the CHG_ON bit • The Discharge FET is restored to the status defined by the DCHG_ON bit • Balancing FETs are restored to the status defined by the corresponding BAL<x>_ON bit • FAULTN line is released	• DIE_OT_CHG_MSK masks reaction on CHG pin • DIE_OT_DCHG_MSK masks reaction on DCHG pin • DIE_OT_BAL_MSK masks reaction on balancing • DIE_OT_FAULTN_MSK masks reaction on FAULTN pin

3.4.4.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise specified: VB according to the operating range in Table 2*; T_j according to the operating range in* Table 5.

Table 17. Die temperature monitor electrical parameters

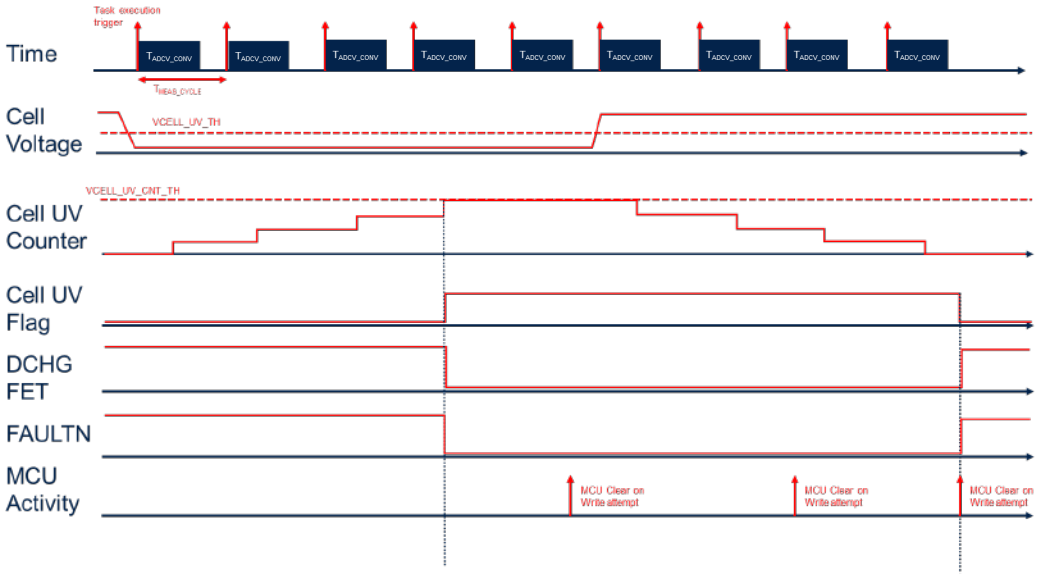
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{j_ERR}	Die temperature total conversion error		-10		10	°C
T_{OT_TH}	Overtemperature threshold		150			°C
T_{OT_HYST}	Overtemperature threshold hysteresis		5		15	°C

3.4.5 Diagnostics principle

The following example on cell UV detection applies to all diagnostics featuring a programmable event counter. The counter implements a symmetric hysteresis:

- Each fault is asserted if the corresponding threshold is exceeded. In such a case, the L9962 puts in place the programmed reactions, based on the masking bits.
- The fault counter is saturated to the programmed threshold as long as the fault is still present. During such an interval, any attempt to clear the fault status is discarded. To avoid inadvertent fault detection, the fault counter threshold is saturated to 1 on the lower bound, meaning that at least one fault event must occur for fault detection. Writing ‘0’ to any I^2C fault counter threshold will result in the internal threshold being clamped to ‘1’.
- When the fault is removed and the event counter reaches zero, the fault flag can be cleared on write by the MCU. In such a case, the system is brought back to a functional state.
- To clear a fault, a write access is necessary, which must be the value '1'.

Figure 7. **Example of cell UV detection**



3.5 Current conversion routine

The current conversion routine can be enabled by programming the CSA_EN bit: if disabled, the monitoring functions and Coulomb counting are not available.

Enabling the current conversion routine increases the VB current consumption by $I_{VB\_NORM\_DELTA\_CSA}$.

3.5.1 Current sense ADC (ISENSEP/ISENSEM)

The L9962 integrates a current sense amplifier and a fully differential sigma-delta ADC, capable of performing continuous acquisition of the pack current using an external shunt resistor connected between the ISENSEP and ISENSEM pins.

Each sample acquisition lasts for T_{CUR_FILTER} (programmable via T_CUR_FILTER field) and a new acquisition starts upon completion of the previous conversion. Being dependent on junction temperature measurements, the CSA performances are guaranteed only in case Voltage conversion routine is enabled and running (whatever the cycle period is).

The latest sample acquired by the ADC is available in the CUR_INST_MEAS register, encoded in two's complement.

The CSA comes with a native gain error of CSA_{GAIN_ERR}. To further improve the accuracy, the L9962 offers the possibility to perform end of line calibration using a single setpoint. By programming the CSA_GAIN_FACTOR register, the gain error can be reduced to $CSA_{GAIN\_ERR\_CAL}$.

The end of line calibration procedure is the following:

1. Read the CSA_GAIN_FACTOR register and store the factory correction factor $K_{GAIN\_FACTORY}$ in a temporary variable
2. Force a precise and stable V_{CSA_CAL} voltage on the ISENSEP-ISENSEM pair
3. Enable the CSA and the Coulomb counter by programming CSA_EN = 1 and CC_ACC_EN = 1
4. Let the Coulomb counter acquire at least 30 samples in order to eliminate any superimposed noise
5. Download the Coulomb counter data as described in Coulomb counting and extract the V_{CSA_MEAS} average value.
6. Calculate the gain correction factor K_{GAIN_CAL}

$$K_{GAIN_{CAL}} = \frac{V_{CSA_{CAL}}}{V_{CSA_{MEAS}}} \quad (2)$$

7. Calculate the end of line correction factor K_{GAIN_EOL} and write it into the CSA_GAIN_FACTOR register

$$K_{GAIN_{EOL}} = K_{GAIN_{FACTORY}} K_{GAINCAL} \quad (3)$$

8. Push the data into the NVM following the procedure described in Non-Volatile Memory (NVM).

3.5.2 Coulomb counting

To enable the accumulation function, the CC_ACC_EN bit must be set. When Coulomb counting is active, current samples are continuously accumulated in the CC_ACC register, while the CC_SAMPLE_CNT counts the number of samples stored in the accumulator. Disabling the Coulomb counting will cause the accumulator and sample counter to reset: to avoid loss of information, the MCU is supposed to download the Coulomb counter information before disabling it.

The MCU must periodically poll the Coulomb counter to retrieve the charge information. The following procedure has to be implemented in order to guarantee proper data synchronization between the accumulator and sample counter:

1. The MCU writes CC_ACC_MSB register with 0xFFFF data
   a. The accumulator is cleared upon write
   b. A snapshot of the internal sample counter and accumulator is loaded into CC_SAMPLE_CNT, CC_ACC_MSB and CC_ACC_LSB fields.
   c. The shadow register of the internal sample counter is meanwhile reset
2. MCU reads the CC_ACC_MSB register
3. MCU reads the CC_ACC_LSB_CNTR register

The Coulomb counting operation requires the MCU to track the charge added/subtracted from the battery pack over time. The L9962 helps track the charge variation ΔQ in the battery pack by continuously acquiring and accumulating the current. This significantly reduces the MCU reading rate, simplifying user SW.

The Coulomb counting routine may refer to a known previous charge $Q(t_0)$ and apply the following equation:

$$\begin{cases} Q(t_k) = Q_{t0} + \Delta Q = Q_{t0} + \Delta T \sum_{k=1}^{K} I_{CELL}(k) = Q_{t0} + \frac{T_{CUR\_FILTER}}{R_{SHUNT}} \sum_{k=1}^{K} V_{DIFF}(k) \\ \sum_{k=1}^{K} V_{DIFF}(k) = CC\_ACC * V_{CUR\_RES} \end{cases} \quad (4)$$

Where:

- V_{DIFF} = ISENSEP-ISENSEM
- CC_ACC is the accumulator, encoded in two's complement
- R_{SHUNT} is the external shunt resistor mounted between ISENSEP and ISENSEM

Then, the $Q(t_k)$ just evaluated becomes the $Q(t_0)$ for the next iteration.

The CC_SAT read-only flag reports the status of the accumulator and sample counter: if either of the two saturates, the CC_SAT is set to '1' and an RDY pulse is generated to inform the MCU that the register data is ready. Meanwhile, the accumulation is stopped and CC_ACC and CC_SAMPLE_CNT are frozen.

3.5.2.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise specified:

VB according to the operating range in Table 2*;* T_j *according to the operating range in* Table 5.

Table 18. Coulomb counter electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
N_{ACC}	Coulomb counter accumulator size	Design info		24		bit
N_{SAMPLE_CNT}	Coulomb counter sample counter size	Design info		8		bit

3.5.3 Overcurrent monitor

When the CSA is enabled, the L9962 can protect the battery pack from overcurrent events in both charge and discharge directions. The absolute value of each current sample is compared to a programmable digital threshold CSA.

This diagnostic can be enabled via the OVC_EN bit and covers the failures listed in Table 19.

To avoid false detections, overcurrent thresholds shall only be modified while OVC_EN = 0.

The recommended re-engagement strategy in case of persistent OVC failure detection is:

- Poll the PERSIST_OVC_<x> flags for at least 5TCUR_FILTER to check if the fault is still present
- 1. If the flag can be cleared, the fault has disappeared and the FET can be re-engaged
  2. Otherwise, re-engaging the FET is not recommended and SW should let the L9962 blow the FUSE (if not masked)

Table 19. Overcurrent diagnostics

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Overcurrent in charge	• If the ISENSEM – ISENSEP voltage rises above $V_{OVC\_CHG\_TH}$, the OVC_CHG fault is acknowledged.	• The OVC_CHG flag is set • The charge FET is turned OFF • FAULTN line is asserted	• If the ISENSEM – ISENSEP voltage falls below V_{OVC_TH}, the OVC_CHG flag can be cleared by MCU	• The Charge FET is restored to the status defined by the CHG_ON bit • FAULTN line is released	• CSA_EN masks measurement execution. When disabled, the OVC_CHG flag can always be cleared • OVC_EN masks diagnostic execution and all reactions. When disabled, the OVC_CHG flag can always be cleared • OVC_CHG_PRDRV_MSK masks reaction on CHG pin • OVC_CHG_FAULTN_MSK masks reaction on FAULTN pin
Persistent Charge current	• If the CHG FET is OFF (either commanded by user or forced by diagnostics) and the ISENSEM – ISENSEP voltage raises above $V_{PERSIST\_OVC\_TH}$, for 4 consecutive samples, the PERSIST_OVC_CHG fault is acknowledged.	• The PERSIST_OVC_CHG flag is set • FUSE pre-driver is enabled • FAULTN line is asserted	• If the ISENSEM – ISENSEP voltage falls below $V_{PERSIST\_OVC\_TH}$ for 4 consecutive samples, the PERSIST_OVC_CHG flag can be cleared by MCU	• FUSE pre-driver is disabled • FAULTN line is released	• CSA_EN masks measurement execution. When disabled, the PERSIST_OVC_CHG flag can always be cleared • OVC_EN masks diagnostic execution and all reactions. When disabled, the PERSIST_OVC_CHG flag can always be cleared • PERSIST_OVC_CHG_FUSE_MSK masks reaction on FUSE pin • PERSIST_OVC_CHG_FAULTN_MSK masks reaction on FAULTN pin
Overcurrent in discharge	• If the ISENSEP – ISENSEM voltage rises above $V_{OVC\_DCHG\_TH}$, the OVC_DCHG fault is acknowledged.	• The OVC_DCHG flag is set • The discharge FET is turned OFF • FAULTN line is asserted	• If the ISENSEP – ISENSEM voltage falls below V_{OVC_TH}, the OVC_DCHG flag can be cleared by MCU	• The discharge FET is restored to the status defined by the DCHG_ON bit • FAULTN line is released	• CSA_EN masks measurement execution. When disabled, the OVC_DCHG flag can always be cleared • OVC_EN masks diagnostic execution. When disabled, the OVC_DCHG flag can always be cleared • OVC_DCHG_PRDRV_MSK masks reaction on DCHG pin • OVC_DCHG_FAULTN_MSK masks reaction on FAULTN pin

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Persistent discharge current	• If the DCHG FET is OFF (either commanded by user or forced by diagnostics) and the ISENSEP – ISENSEM voltage rises above $V_{PERSIST\_OVC\_TH,}$ for 4 consecutive samples, the PERSIST_OVC_DCHG fault is acknowledged.	• The PERSIST_OVC_DCHG flag is set • FUSE pre-driver is enabled • FAULTN line is asserted	• If the ISENSEP – ISENSEM voltage falls below $V_{PERSIST\_OVC\_TH}$ for 4 consecutive samples, the PERSIST_OVC_DCHG flag can be cleared by MCU	• FUSE pre-driver is disabled • FAULTN line is released	• CSA_EN masks measurement execution. When disabled, the PERSIST_OVC_DCHG flag can always be cleared • OVC_EN masks diagnostic execution. When disabled, the PERSIST_OVC_DCHG flag can always be cleared • PERSIST_OVC_DCHG_FUSE_MSK masks reaction on FUSE pin • PERSIST_OVC_DCHG_FAULTN_MSK masks reaction on FAULTN pin

3.5.4 Short-circuit in discharge protection

When the CSA is enabled, the L9962 protects the battery pack from short-circuit in discharge by sensing the current through the shunt resistor with a faster filter time T_{SC_FILTER}, programmable in the SC_FILTER field. This diagnostic is enabled by using the SC_EN bit and covers the failures listed in Table 20.

Writing SC_EN = 1 enables the short-circuit monitor after a maximum delay of 528 µs.

To avoid false detections, overcurrent thresholds shall only be modified while SC_EN = 0.

Table 20. **Short-circuit in discharge diagnostics**

Fault type	Assertion condition	IC reaction to assertion	Release condition	IC reaction to flag clear	Maskable
Short-circuit in discharge	• If the (ISENSEP – ISENSEM) voltage rises above V_{SC_TH} for longer than T_{SC_FILTER}, the SC fault is acknowledged.	• The SC_DCHG flag is set • The discharge FET is turned OFF • FAULTN line is asserted	• If the (ISENSEP – ISENSEM) voltage falls below V_{SC_TH} for longer than T_{SC_FILTER}, the SC_DCHG flag can be cleared by MCU	• The discharge FET is restored to the status defined by the DCHG_ON bit • FAULTN line is released	• CSA_EN masks measurement execution. When disabled, the SC_DCHG flag can always be cleared • SC_EN masks diagnostic execution. When disabled, the SC_DCHG flag can always be cleared • SC_DCHG_PRDRV_MSK masks reaction on DCHG pin • SC_DCHG_FAULTN_MSK masks reaction on FAULTN pin
Persistent short-circuit in discharge	• If the DCHG FET is OFF (either commanded by user or forced by diagnostics) and the ISENSEP – ISENSEM voltage rises above $V_{PERSIST\_SC\_TH}$ for $N_{PERSIST\_SC}$ consecutive samples the PERSIST_SC_DCHG fault is acknowledged. Diagnostic is masked for $T_{PERSIST\_SC\_BLANK}$ starting from DCHG FET OFF event. Persistent short-circuit in discharge relies on the DCHG MOSFET status (disabled)	• The PERSIST_SC_DCHG flag is set • FUSE pre-driver is enabled • FAULTN line is asserted	• If the (ISENSEP – ISENSEM) voltage falls below $V_{PERSIST\_SC\_TH}$ for longer than T_{SC_FILTER}, the PERSIST_SC_DCHG flag can be cleared by MCU	• FUSE pre-driver is disabled • FAULTN line is released	• CSA_EN masks measurement execution. When disabled, the PERSIST_SC_DCHG flag can always be cleared • SC_EN masks diagnostic execution. When disabled, the PERSIST_SC_DCHG flag can always be cleared • PERSIST_SC_DCHG_FUSE_MSK masks reaction on FUSE pin • PERSIST_SC_DCHG_FAULTN_MSK masks reaction on FAULTN pin

3.5.4.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise specified: VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 21. Short-circuit in discharge electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{SC_FILTER}	Programmable short-circuit in discharge filter time (3 bit)	Tested by SCAN	$16\mu s*[1+2^{min(CODE,4)}]$		$16\mu s*[1+3*2^{min(CODE,4)}]$	µs
VSC_RES	Short-circuit measurement resolution	Design info		2.34 (300mv/2^7)		mV
V_{SC_TH}	Programmable short-circuit in discharge threshold (4 bit) $V_{SC_{TH}} = 49.14mV + 14.04mV * CODE$		50		275	mV
$V_{PERSIST\_SC\_TH}$	Programmable persistent short-circuit in discharge threshold (4 bit) $V_{SC_{PERSIST_{TH}}} = 49.14mV + 14.04mV * CODE$		50		275	mV
$V_{SC\_TH\_TOL}$	V_{SC_TH} gain error		-10		+10	%
$V_{SC\_TH\_OFFSET}$	V_{SC_TH} offset error		-5		+5	mV
$T_{PERSIST\_SC\_BLANK}$	Persistent short-circuit in discharge blanking time		3.1		3.65	ms

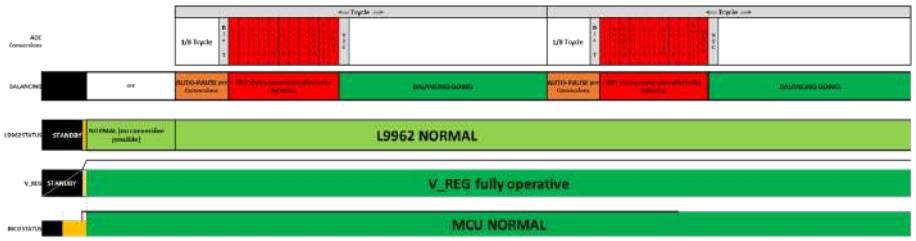
3.6 Cell balancing

The L9962 provides passive cell balancing by discharging battery cells through the Cx pins. To balance a cell, it should be enabled by using the corresponding VCELL_EN_<x> bit and to activate the balancing switch on a cell, the corresponding BAL<x>_ON bit must be set. Balancing is inhibited if cell voltage falls below the balance undervoltage threshold (refer to Cell voltage monitor (Cx)).

Balancing current must be limited to a maximum of I_{BAL_MAX} via cell filtering resistors. It is recommended to balance only non-adjacent cells. Care must be taken when balancing adjacent cells in order not to violate the I_{BAL_MAX} constraint.

To allow cell voltage relaxation, balancing is stopped for $T_{BAL\_SETTLING}$ before running the first step of the Voltage conversion routine. It is then automatically re-engaged after the VB step completion.

Figure 8. Balancing timing diagram



3.6.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise specified:
VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 22. Balancing electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{DS_ON}	Balancing FET ON resistance	I_{OUT}=70 mA			20	Ω
I_{BAL_MAX}	Maximum balancing current	For each balancing FET			70	mA
T_{ON_BAL}	Cell balance driver turn-on time	RCx=39 Ω, external Cap 470 nF From BAL<x>_ON command to 30% of VDS	1	5	12	µs
T_{OFF_BAL}	Cell balance driver turn-off time	RCx=39 Ω, external Cap 470 nF From BAL<x>_OFF command to 70% of VDS	3	9	20	µs
$T_{BAL\_SETTLING}$	Settling time before cell measurement			TMEAS_CYCLE/8		ms

3.7 HS/LS pre-drivers (CHG/DCHG/FUSE)

The L9962 integrates three pre-driver stages aimed at managing pack connection to external loads and chargers.

3.7.1 Battery pack charge/discharge relays (CHG/DCHG)

The L9962 integrates a dual pre-driver stage used to control the external charge (CHG) and discharge (DCHG) MOSFETs. Each pre-driver can be independently configured as high-side or low-side by means of the CHG_HS_LS and DCHG_HS_LS configuration bits.

For each MOSFET:

- xxx_HS_LS = 0 selects a low-side configuration.
- xxx_HS_LS = 1 selects a high-side configuration.

The default configuration after device power on is HS for both CHG and DCHG MOSFETS. The MOSFETs can be used both in a back-to-back HS/LS topology, or in a standalone HS/LS topology:

- HS back to back topology: CHG_HS_LS ="1", DCHG_HS_LS="1"
- LS back to back topology: CHG_HS_LS ="1", DCHG_HS_LS="0"
- CHG and DCHG in LS standalone topology: CHG_HS_LS ="0", DCHG_HS_LS="0"
- CHG and DCHG in HS standalone topology: CHG_HS_LS ="1", DCHG_HS_LS="1"
- CHG in standalone LS topology and DCHG in standalone HS topology: CHG_HS_LS ="0", DCHG_HS_LS="1"
- CHG in standalone HS topology and DCHG in standalone LS topology: CHG_HS_LS ="1", DCHG_HS_LS="0"

The gate driver outputs are enabled in NORMAL mode only, and are in high impedance while in STANDBY or SHIPMENT - DEEP SLEEP states.

When in NORMAL state, the CHG and DCHG FETs can be commanded ON/OFF using I^2C registers:

- DCHG_ON commands the DCHG FET
- CHG_ON commands the CHG FET

Several diagnostics may have an impact on the CHG/DCHG output state, which can be forced low by the L9962 independently of the status of the above commands.

3.7.1.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise specified:
VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 23. **Charge - Discharge gate driver electrical parameters**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
F_{PRDRV}	Pre-driver expected switching frequency	Application info		2		Hz
C_{PRDRV_LOAD}	Equivalent capacitive load on CHG/ DCGH pins	Application info		10		nF
V_{GS_ON}	CHG/DCHG ON voltage	VB > 9V	9	10.5	11.7	V
		5.7 < VB < 9V	6.5	7.5	9	V
V_{GS_OFF}	CHG/DCHG OFF voltage	I(CHG)= I(DCHG)=0.5* *IPD_MIN=0.46 mA V(VSx)=0 V			100	mV
I_{PU}	CHG/DCHG current source	V(CHG)-V(VSC)=0 V V(DCHG)-V(VSD)=0 V V(VSx)=0 V	-2.4		-0.6	mA
I_{PD}	CHG/DCHG current sink	V(CHG)-V(VSC)=5 V V(DCHG)-V(VSD)=5 V V(VSx)=0 V	12.5	70	120	mA
R_{PD}	CHG/DCHG pull-down resistance	V(CHG)-V(VSC)=0.3 V V(DCHG)-V(VSD)=0.3 V V(VSx)=0 V			35	Ω

3.7.2 FUSE pre-driver

Under certain conditions classified as permanent failures, the L9962 can be programmed to activate the FUSE pre-driver. An external NMOS can be driven to blow a fuse connected in series to the battery pack's positive terminal.

The following list of failures is classified as permanent:

- Severe cell UV: aimed at preventing copper deposition (see Cell voltage monitor (Cx))
- Severe cell OV: aimed at preventing explosion hazard (see Cell voltage monitor (Cx))
- VVB vs. sum of cells plausibility check fail: aimed at preventing BMS permanent malfunction (see Battery Stack Monitor (VB))
- Severe NTC OT: aimed at preventing fire hazard (see Cell temperature monitor (NTC))
- Persistent charge current: aimed at preventing overcharge (see Overcurrent monitor)
- Persistent discharge current: aimed at preventing overdischarge (see Overcurrent monitor)
- Persistent short circuit in discharge: aimed at preventing fire hazard (see Short-circuit in discharge protection)

In addition to the internal diagnostics, L9962 can also enable the FUSE pre-driver upon:

- User request through I2C
  1. *FUSE must start from the OFF condition (FUSE_TRIG_FIRE = 01)*
  2. *FUSE shall be first armed by writing FUSE_TRIG_ARM = 10*
  3. *The FUSE can be then fired by setting FUSE_TRIG_FIRE = 10 within $T_{FUSE\_TIMEOUT}$, otherwise the fire command will be discarded*

Note: Rewriting FUSE_TRIG_ARM = 10 while the timeout is running restarts the timer. Writing FUSE_TRIG_FIRE = 01 interrupts the FUSE activation. Writing FUSE_TRIG_ARM = 10 while FUSE_TRIG_FIRE = 10 immediately fires the FUSE.

- Secondary protector activation detection: if the FUSE voltage rises above V_{FUSE_TH} for longer than T_{FUSE_FILTER}, the FUSE pre-driver is enabled and the FUSE_EXT flag is set. Once triggered, the action can no longer be inhibited unless a GO2SHIP/GO2SLP command is issued.

3.7.2.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise specified:

VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 24. FUSE pre-driver electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{FUSE}	Fuse pre-driver pull-up current	VFUSE = 0V	50			uA
V_{FUSE_TH}	FUSE external activation detection threshold		0.8		1.8	V
V_{FUSE_HYST}	FUSE external activation detection threshold hysteresis		0.1		0.5	V
T_{FUSE_FILTER}	FUSE activation/deactivation digital filter		85	104	120	us
$T_{FUSE\_TIMEOUT}$	FUSE fire command timeout in respect to fuse arm event		1.6	2	2.3	s
R_{FUSE}	FUSE pull-down resistance		50	100	150	KΩ

3.8 Digital I/Os (RDY/SDA/SCL/FAULTN_SAFE/FAULTN/OD)

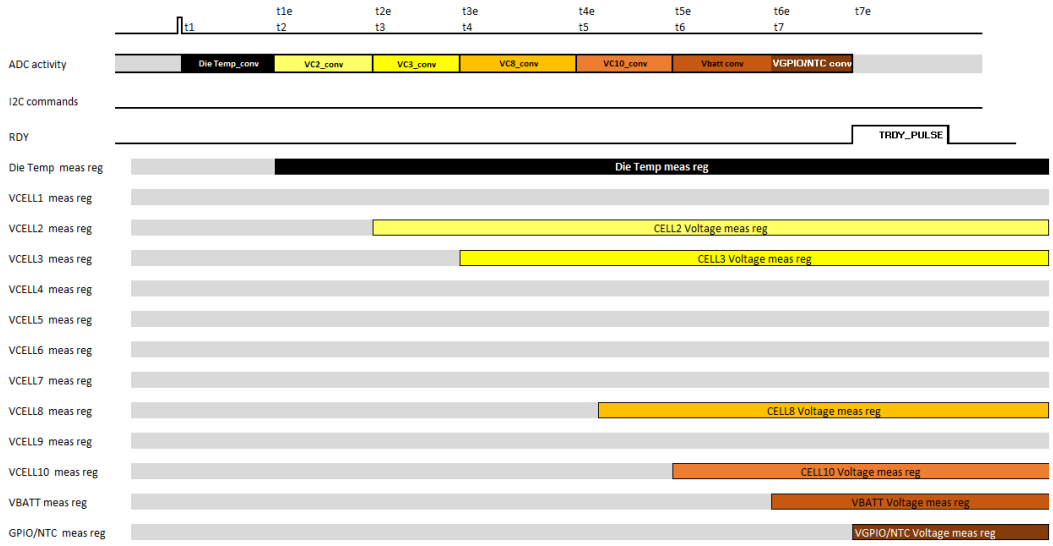
The following paragraph lists the electrical characteristics of the device digital I/Os.

3.8.1 Data-Ready Interrupt pin (RDY)

The RDY pin is used signal the system MCU when new data is available. The RDY signal is a positive pulse lasting for T_{RDY_PULSE} upon the following events:

- After each Voltage conversion routine task is completed (as shown in Figure 9)
- If the Coulomb counter saturates (upon CC_SAT flag positive edge, see Coulomb counting)
- Any time the device enters NORMAL state

Figure 9. RDY pulse generation upon voltage conversion routine task termination



3.8.1.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise specified:
VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 25. RDY interrupt pin electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{RDY_PULSE}	RDY interrupt pulse duration	Tested by SCAN	85	104	120	us

3.8.2 Fault interrupt pin (FAULTN)

The FAULTN pin indicates when a failure is detected . FAULTN is an open-drain output active low.

Several failures can be redirected to the FAULTN line depending on their masking bit. Refer to Voltage conversion routine and Current conversion routine for a list of specific failures.

FAULTN can also be used by a secondary protector in order to disconnect the battery pack from the load or the charger. When not internally pulled low, FAULTN can be externally pulled low for T_{FAULTN_LOW}: The L9962 will force the CHG/DCHG outputs low, regardless of CHG_ON and DCHG_ON commands and L9962 internal diagnostics. The event is latched by FAULTN_EXT bit. CHG/DCHG will be released upon flag clear by the MCU.

3.8.2.1 *Electrical parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise specified:
VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 26. Digital output electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{FAULTN_LOW}	FAULTN input filter time for secondary protector activation detection	Tested by SCAN	17	21	25	us

3.8.3 MCU emergency reset (FAULTN_SAFE)

The MCU should normally manage the communication with the battery charger, ensuring cells are properly charged to 100% state of charge. In case the MCU operation fails, the battery cells could be overcharged, leading to fire/explosion hazards.

The L9962 can reset the MCU should a cell overvoltage condition be detected. This is done by connecting the FAULTN_SAFE open-drain output to the MCU reset pin (active low).

When overvoltage failures are directed to the FAULTN_SAFE pin, the output will be pulled low for $T_{FAULTN\_SAFE\_LOW}$ to allow a proper reset of the MCU.

3.8.3.1 *Electrical Parameters*

All parameters are tested and guaranteed under the following conditions, unless otherwise specified:
VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 27. Digital output electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{FAULTN\_SAFE\_LOW}$	FAULTN_SAFE low interval	Tested by SCAN	85	104	120	us

3.8.4 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise specified:
VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 28. Digital output electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
V_{IN_L}	Low input level Valid for FAULTN, SDA, SCL	Slow rising ramp on input pin	0.8		1.8	V
V_{IN_HYS}	Input hysteresis Valid for FAULTN, SDA, SCL	Input considered high when VIN > VIN_L + VIN_HYS	0.1		0.8	V
V_{OUT_L}	Low output level	IOUT = 2 mA	0		0.4	V
V_{OUT_H}	High output level	IOUT = 2 mA	VREG-0.4		VREG	V
T_{OUT_RISE}	Output Rise time Valid for RDY	Cload=120pF From 20 to 80% of final value Guaranteed by design	1		35	ns
T_{OUT_FALL}	Output fall time Valid for RDY.	Cload=120pF From 80 to 20% of initial value Guaranteed by design	1		35	ns
V_{OPEN_DRAIN}	Open-drain equivalent ON resistance measurement	I_{OD}=2mA	0.01		0.15	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
	Valid for SDA, FAULTN, FAULTN_SAFE, OD					

3.9 I²C communication interface

The L9962 uses an I²C slave peripheral interface to communicate with a host MCU on an addressed I²C bus.

The I²C peripheral uses two lines to implement communication:

- SCL (serial clock): a digital input receiving clock from the master unit of the I²C bus
- SDA (serial data): a digital input/output used for sending and receiving data clocked by the master unit of the I²C bus

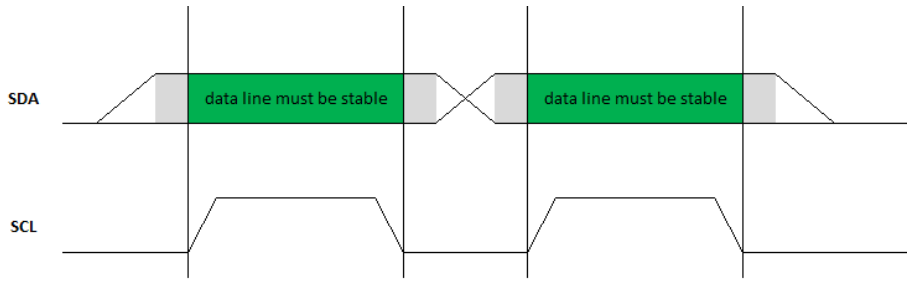
The L9962 I²C peripheral is compliant with the I²C fast standard (400 kbit/s).

3.9.1 I²C physical layer

SDA is an open-drain pin and requires an external pull-up resistor to VREG, while SCL is a digital input pin. Master/slave units can only force SDA/SCL low, while a release condition corresponds to all units not forcing a zero, thus resulting in SDA/SCL pulled high passively to VREG.

3.9.1.1 Clock polarity

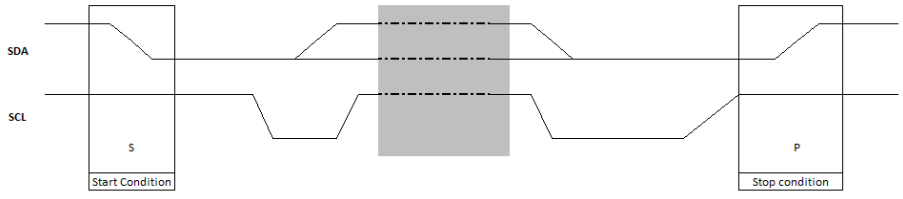
Figure 10. I2C Clock Polarity



Data on the SDA line is sampled on the SCL rising edge and must fulfil t_{SU_DAT} (setup) and t_{HD_DAT} (hold) constraints, while it is allowed to change during SCL low semi-period. A single bit is transferred per clock period.

3.9.1.2 Start/stop conditions

Figure 11. I2C Start/Stop Conditions



Every communication window is defined within the START and STOP conditions. These are always generated by the master.

- A START condition corresponds to an SDA HI→LO transition while SCL is HIGH. The SCL must verify the t_{SU_STA} (setup) and t_{HD_STA} (hold)constraints
- When a START condition is detected an internal watchdog timer is reset and started
- A STOP condition corresponds to an SDA LO→HI transition while SCL is HIGH. The SCL must verify the t_{SU_STO} (setup) and t_{HD_STO} (hold)constraints
- If the communication breaks down or any issue occurs while an I²C frame is ongoing, the IC will be able to re-engage after a TI2C_TIMEOUT time.

After the STOP condition, the bus must be left idle for at least t_{BUF} before issuing a new START condition. The L9962 resets its I²C logic upon each START/STOP condition detection.

3.9.1.3 *ACK/NACK*

In a communication window, every byte transferred over the I²C bus is followed by a 9th bit representing the Acknowledge (ACK) or Not Acknowledge (NACK) condition. For each byte, the peripheral receiving data will either confirm its availability to continue the communication (ACK) or will signal unavailability (NACK).

- An ACK is represented by SDA LOW on the 9th SCL pulse
- A NACK is represented by SDA HIGH on the 9th SCL pulse

There are five conditions leading to the generation of a NACK by a receiver:

1. *Absence of receiver*: no receiver is present on the bus with the transmitted address so there is no device to respond with an ACK
2. *Receiver busy*: the receiver is unable to receive or transmit because it is performing a real-time function and is not ready to start communication with the master
3. *Wrong data received*: during the transfer, the receiver receives data or commands that it does not understand. If the CRC check is enabled, L9962 will generate a NACK in case corrupted data is detected.
4. *Receiver buffer full*: during the transfer, the receiver cannot receive more data.
5. *Transfer completed*: a master-receiver must signal the end of the transfer to the slave transmitter.

When the L9962 generates a NACK, the error state is latched and any subsequent write operation will not be accomplished. The MCU is expected to issue a STOP condition to reset the I²C logic.

3.9.2 I²C protocol layer

3.9.2.1 *Addressing and R/W bit*

The ADDRESS byte is formed by a 7-bit address field plus a $R/\overline{W}$ bit

- By default, the ADDRESS is 0b1001001.
  - The address can be changed by programming the DEV_ADDR_ID register
  - The address can be stored in the NVM in order to allow the integration of the L9962 on a multichip bus
- The $R/\overline{W}$ bit is processed as follows
  - $R/\overline{W} = 1$ means READ
  - $R/\overline{W} = 0$ means WRITE

3.9.2.2 *CRC*

The L9962 can check data integrity by means of a CRC. By default, this feature is disabled and can be enabled by programming the CRC_EN bit.

The CRC poly is: x^8+x^2+x+1

The CRC initialization is 0.

The L9962 exploits received CRC information to validate each WRITE operation, eventually issuing a NACK and discarding data in case of corruption detection

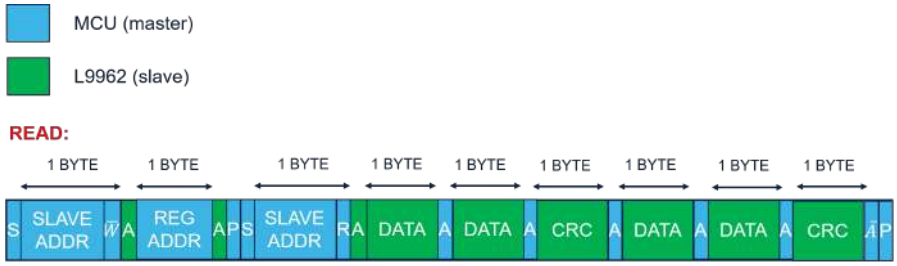
In read operations, the L9962 equips the output data with CRC to allow the MCU to validate the received data. The MCU may:

- validate data on-the-fly, generating a real-time NACK in case of corruption detection
- validate the data offline, discarding it in case of corruption detection

3.9.2.3 *Single read/block read*

The READ operation shall be used to retrieve information from the internal I²C registers. However, as the device implements a Clear-on-Write approach, it will not clear any latch.

Figure 12. I²C generic READ operation



The elementary READ operation consists of:

1. a START condition
2. the SLAVE ADDRESS byte (with $R/\overline{W} = 0$) identifying the slave device to be activated
3. the REGISTER ADDRESS byte identifying the memory address where data has to be read
4. a STOP condition

This first instruction subset loads the starting address into the memory address counter. Then the following sequence starts the download of the data:

1. a START condition
2. the SLAVE ADDRESS byte (with $R/\overline{W} = 1$) identifying the slave device to be activated
3. the L9962 will output two data bytes
4. the L9962 will output an optional CRC byte covering all the previous bytes.

In a block read, the MCU can continue reading by clocking additional packets of two data bytes (plus a third CRC byte optionally generated by the L9962). The REGISTER ADDRESS defined in step 3 will be considered as the starting address, and the memory address counter will be incremented by 1 for every 2 bytes output.

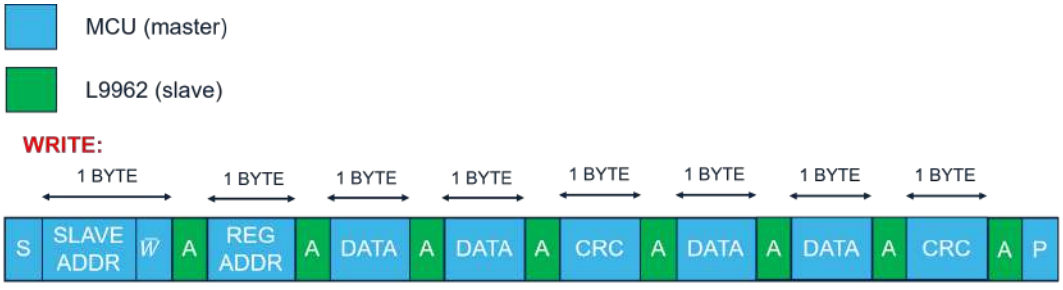
In case REGISTER ADDRESS saturates, the L9962 will output 0xFF bytes.

The READ operation terminates with a STOP condition.

3.9.2.4 *Single write/block write*

The WRITE operation shall be used to configure device parameters and send actuation commands. As the I²C peripheral implements a Clear-On-Write approach, the WRITE operation must also be used to reset any latch writing a logic '1' to the corresponding bit.

Figure 13. I²C generic WRITE operation



The elementary WRITE operation consists of:

- a START condition
- the SLAVE ADDRESS byte (with $R/\overline{W} = 0$) identifying the slave device to be activated
- the REGISTER ADDRESS byte identifying the memory address where data has to be written
- two data bytes
- an optional CRC byte covering all the previous bytes

In a block write, the operation can continue by sending other packets formed by two data bytes and an optional CRC covering the previous two bytes. The REGISTER ADDRESS defined in step 3 will be considered as the starting address, and the memory address counter will be incremented by 1 for every 2 bytes received.

In case REGISTER ADDRESS saturates, the L9962 will generate a NACK and data is be written into internal registers.

In case the received CRC is wrong, the L9962 generates a NACK and the corresponding data is not written into internal registers.

The WRITE operation terminates with a STOP condition.

3.9.2.5 *Electrical parameters*

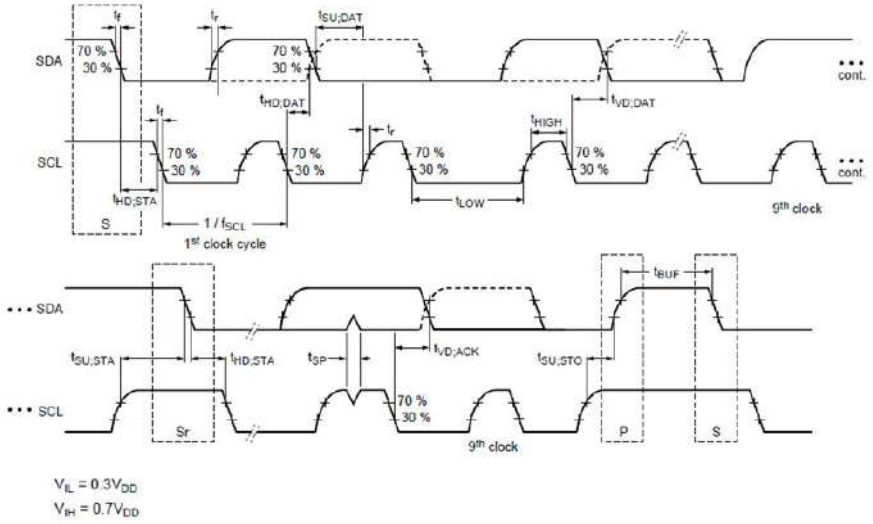
All parameters are tested and guaranteed under the following conditions, unless otherwise specified:

VB according to the operating range in Table 2*;* T_j *according to the operating range in* Table 5.

Table 29. I²C electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
F_{SCL}	Communication frequency	Guaranteed by design	80		400	kHz
t_{LOW}	LOW period of the SCL clock		1.3			us
t_{HIGH}	HIGH period of the SCL clock		0.6			us
t_{HD_STA}	SCL hold (High) time, after SDA falling edge has created the START condition, for the START condition to be correctly detected		0.6			us
t_{SU_STA}	SCL set-up time to High (SDA already High) before SDA falling edge creates the START condition sequence (by falling when SCL is steadily high)		0.6			us
t_{HD_DAT}	SDA hold time after SCL falling edge		300		-	ns
t_{SU_DAT}	SDA set-up time before SCL rising edge		100		-	ns
t_r	Rise time of SDA signal	With 4.7kΩ pull-up resistor and 40pF load	0		300	ns
t_f	Fall time of SDA signal	With 4.7kΩ pull-up resistor and 40pF load	0		300	ns
t_{rf_SCL}	Rise/fall time SCL signal		0		300	ns
t_{SU_STO}	SCL set-up time to High (SDA already Low) before SDA rising edge creates the STOP condition sequence (by rising when SCL is steadily high)		0.6			us
t_{HD_STO}	SCL hold (High) time, after SDA rising edge has created the STOP condition, for the STOP condition to be correctly detected		0.6			us
t_{BUF}	Bus free time between a STOP and START condition		1.3			us
C_b	Capacitive load for each bus line				400	pF
$T_{I2C\_TIMEOUT}$			46	50	54	ms
$t_{VD\_DAT\_ACK}$	Data (ACK) valid time				0.9	us

Figure 14. **Timing on the I²C bus**



3.10 Non-Volatile Memory (NVM)

The L9962 allows saving key I²C configuration parameters in the internal NVM. Not all I²C register are stored in the NVM: refer to the register map file attached, where a color code identifies configuration registers stored in the NVM.

The following I²C commands allow interacting with the NVM:

- NVM_WRITE_READ_CODE_CMD = 0xAAAA triggers the NVM upload fetching the data from I²C registers and moving it to the NVM sectors. The operation lasts T_{NVM_UPLOAD} and during such an interval the MCU will not be able to perform I²C R/W operations
- NVM_WRITE_READ_CODE_CMD = 0x5555 triggers the NVM download fetching the data from NVM sectors and moving it to the I²C registers. The operation lasts $T_{NVM\_DOWNLOAD}$ and during such an interval the MCU will not be able to perform I²C R/W operations.

The NVM can be written a maximum of $N_{NVM\_WRITE\_CYCLES}$. If this limit is exceeded, data retention is not guaranteed. The NVM_UPLOADS_COUNT counter stores the number of NVM write operations executed and is saturated to 31.

At each device wake-up, the NVM is autonomously re-downloaded and the related I²C configuration registers are refreshed. Thus, the MCU is not required to run configuration functions at each wake-up.

The MCU shall disable any load actuation (CHG/DCHG, Balancing and FUSE) before launching an NVM download/upload command.

Data stored in the NVM is checked against corruption:

- If the trimming & calibration data is corrupted, the CRC_TRIM_CAL_FAIL flag is set and the FAULTN pin is asserted
- If the user sectors are corrupted, the CRC_CFG_FAIL flag is set and the FAULTN pin is asserted

Whenever data corruption is detected (CRC_TRIM_CAL_FAIL or CRC_CFG_FAIL), the diagnostic routines will not be stopped and faults might be inadvertently flagged. However, all the actuations due to internal faults will be inhibited as if the corresponding masking bit (*_MSK) was set.

3.10.1 Electrical parameters

All parameters are tested and guaranteed under the following conditions, unless otherwise specified: VB according to the operating range in Table 2; T_j according to the operating range in Table 5.

Table 30. NVM electrical parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$N_{NVM\_WRITE\_CYCLES}$	NVM allowed write cycles	Guaranteed by design			16	cycles
T_{NVM_UPLOAD}	NVM upload time	Guaranteed by design			65	ms
$T_{NVM\_DOWNLOAD}$	NVM download time	Guaranteed by design			5	ms

4 Device register map

L9962 register map is available in the STSW-L9962FW software package.

5 Application information

5.1 Power supply circuit

Figure 15. **Power supply circuit**

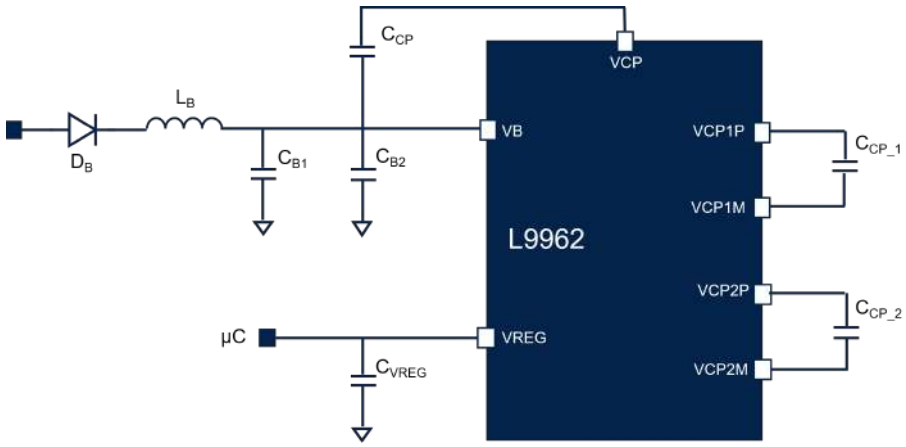


Table 31. **Recommended power supply components**

Components	Value	Unit	Max. tolerance	Rating	Comments
L_B	1	µH	20%	150mA	LPF inductance for battery path. The filter cut-off frequency is $f_C = \frac{1}{\left(2\pi\sqrt{L_B(C_{B1}+C_{B2})}\right.}$
C_{B1}	10	µF	10%	100 V	Provides battery stabilization. Filter noise on VB sense line.
C_{B2}	220	nF	10%	100 V	Filter high frequency noise on VB sense line. Place as close as possible to VB pin.
C_{CP}	68	nF	10%	25 V	Charge pump tank capacitor. Mount as close as possible to VCP pin.
C_{CP_1}	6.8	nF	10%	50 V	Charge pump flying capacitor. Mount as close as possible to VCP1P/1M pin.
C_{CP_2}	6.8	nF	10%	50 V	Charge pump flying capacitor. Mount as close as possible to VCP2P/2M pin.
C_{VREG}	4.7	µF	10%	16 V	Tank for the VREG regulator. Mount as close as possible to VREG pin.
D_{ZB}	100	V			The BAT46WJF is recommended to protect VB against reverse battery

5.2 Cell voltage sensing and balancing circuit

Figure 16. **Cell voltage sensing and balancing circuit**

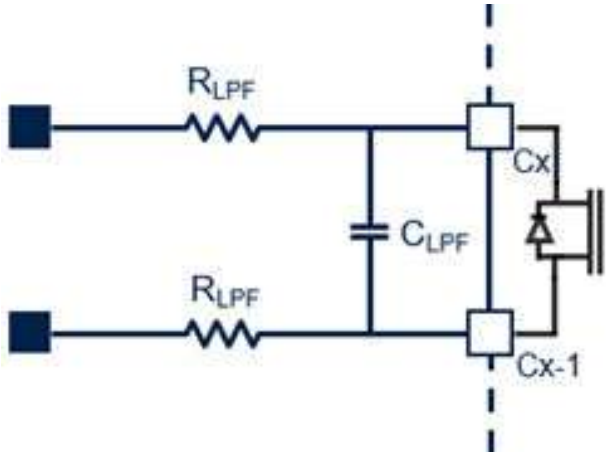


Table 32. **Typical BOM for cell voltage sensing and balancing circuit**

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{LPF}	39	Ω	10%	1/8W	LPF resistor for cell voltage measurement. It is also used to limit the balancing current. The differential filter cut-off frequency is $f_C = \frac{1}{(4\pi R_{LPF} C_{LPF})}$
C_{LPF}	470	nF	10%	16V	LPF capacitor for cell voltage measurement. The differential filter cut-off frequency is $f_C = \frac{1}{(4\pi R_{LPF} C_{LPF})}$

5.3 Current sense circuit

Figure 17. **Current sense circuit**

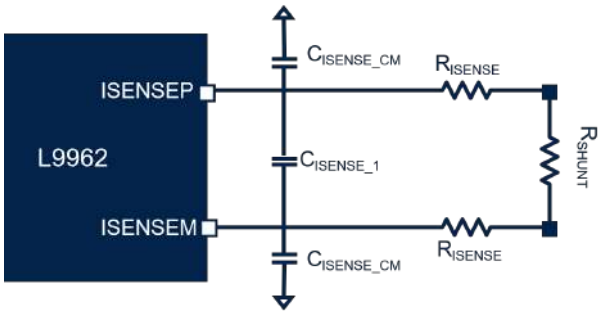


Table 33. **Typical current sense BOM**

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{ISENSE}	47	Ω	0.1%	1/10W	It is used both for filter differential and common-mode noise on the ISENSEp/ISENSEm input. The differential filter cut-off frequency is $f_C = \frac{1}{\left(4\pi R_{ISENSE}\left(C_{ISENSE\_1} + C_{ISENSE\_2} + \frac{C_{ISENSE\_CM}}{2}\right)\right.}$ The common-mode filter cut-off frequency is $f_C = \frac{1}{(2\pi R_{ISENSE} C_{ISENSE\_CM})}$
C_{ISENSE_CM}	33	nF	5%	16V	Filter common -mode noise. The common mode filter cut-off frequency is $f_C = \frac{1}{(2\pi R_{ISENSE} C_{ISENSE\_CM})}$
C_{ISENSE_1}	4.7	µF	10%	16V	Filter differential low frequency noise on the ISENSEp/ ISENSEm input. The differential filter cut-off frequency is $f_C = \frac{1}{\left(4\pi R_{ISENSE}\left(C_{ISENSE\_1} + C_{ISENSE\_2} + \frac{C_{ISENSE\_CM}}{2}\right)\right.}$

Shunt resistor is used for current sensing and coulomb counting. Rating depends on the maximum battery current (R_{SHUNT} * $I_{SENSE\_MAX}^2$). Different R_{SHUNT} values are possible as long as R_{SHUNT} * I_{SENSE} stays in the differential measurement range [-200 ; +200] mV and the ISENSEp/ISENSEm AMR are not violated.

5.4 NTC analog front end

Figure 18. **NTC measurement circuit**

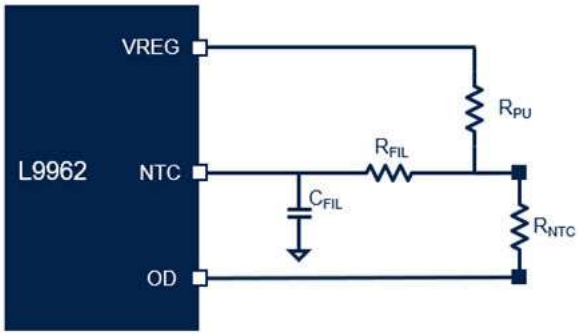


Table 34.

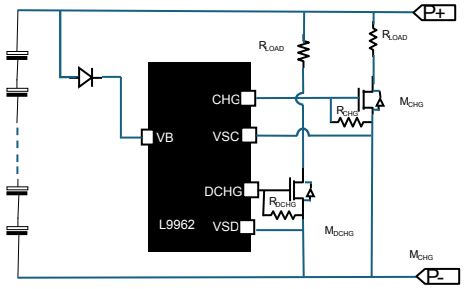
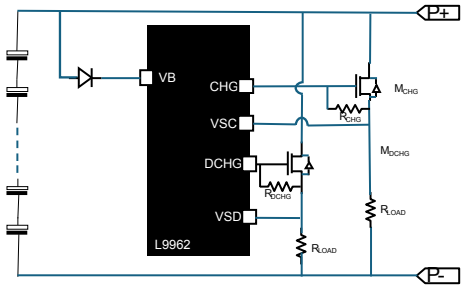
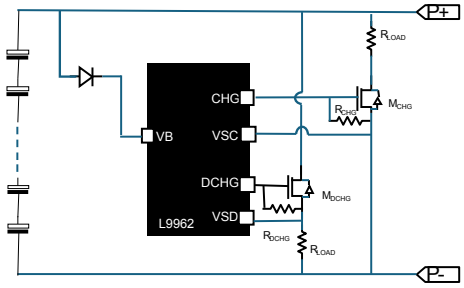
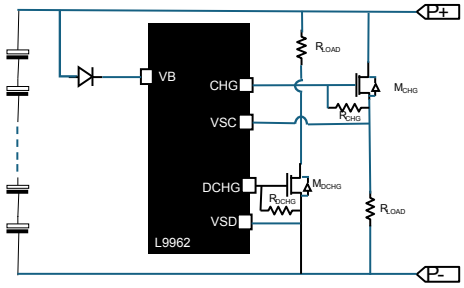
Components	Value	Unit	Max. tolerance	Rating	Comments
R_{NTC}	33	kΩ	10%	1/10W	NTC resistor
R_{PU}	33	kΩ	10%	1/10W	Provides VREG/2 polarization for NTC typical value
R_{FIL}	10	kΩ	10%	1/10W	Filters the NTC signal: cut-off frequency is $f_C = \frac{1}{(2\pi R_{FIL} C_{FIL})}$
C_{FIL}	10	nF	10%	16V	Filters the NTC signal: cut-off frequency is $f_C = \frac{1}{(2\pi R_{FIL} C_{FIL})}$

5.5 HS/LS pre-drivers circuit

L9962 Supports two pre-driver circuits fully configurable.

Each predriver can be configured to work either in LS or HS according to configurated bit.

Table 35. HS/LS predriver stand-alone topology

CHG_HS_LS	DCHG_HS_LS	
0	0	
1	1	
0	1	
1	0	

A back to back topology is also fully supported as described below:

Table 36. HS/LS predriver back to back topology

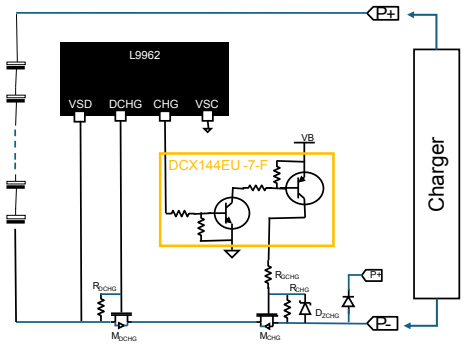
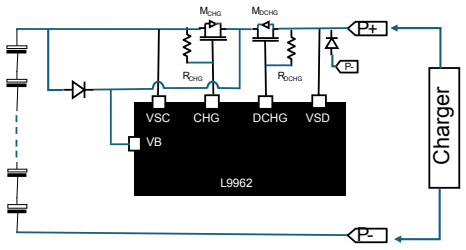
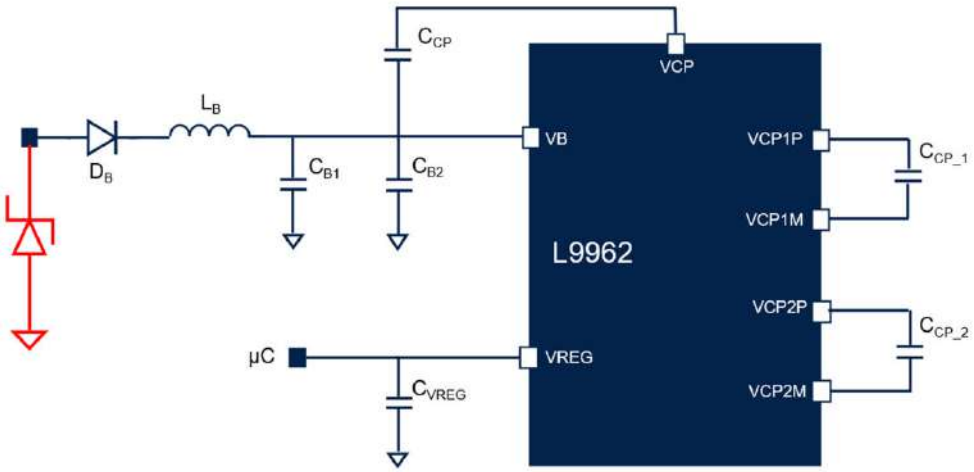
CHG_HS_LS	DCHG_HS_LS	
1	0	 LS Configuration
1	1	 HS Configuration

Table 37. Typical HS/LS pre-drivers BOM

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{CHG}	2	MΩ	10%	1/8 W	Pull-down resistor
R_{DCHG}	2	MΩ	10%	1/8 W	Pull-down resistor
M_{CHG}				60V	Battery charge FET. The STL130N6F7 is recommended
M_{DCHG}				60V	Battery discharge FET. The STL130N6F7 is recommended
D_R	44	V			(Optional) DR recirculation diode intended to protect VSD/VSC pin by recirculating the energy stored in the parasitic inductance of wires in case the charge/discharge phase is sudden interrupted by M_{CHG} / M_{DCHG} FET. The component has to be chosen with an Rdyn that guarantee to not violate the VSD AMR according to the max current surge. SMA6J40A/CA recommended for a typical scenario with a maximum DC operating VB = 44V.
C_R	100	nF	10%	60V	(Optional) Capacitance limits the maximum pin slew/rate in case of charge/discharge phase is sudden interrupted.
R_{VSC}	2.2	Ω	5%	1/8 W	Protection on VSC pin in HS configuration, to avoid AMR violation in case of hot-plug spikes
C_{VSC}	1	µF	5%	100V	

Figure 19. **Optional TVS diode**



(Optional) The SMCJ40A diode can be used to mitigate the effects of parasitic inductances on the battery lines, which can cause overshoot on the battery line when high currents are interrupted.

The diode has to be placed as close as possible to the battery and GND connector.

5.6 Fuse circuit

Figure 20. **Fuse circuit**

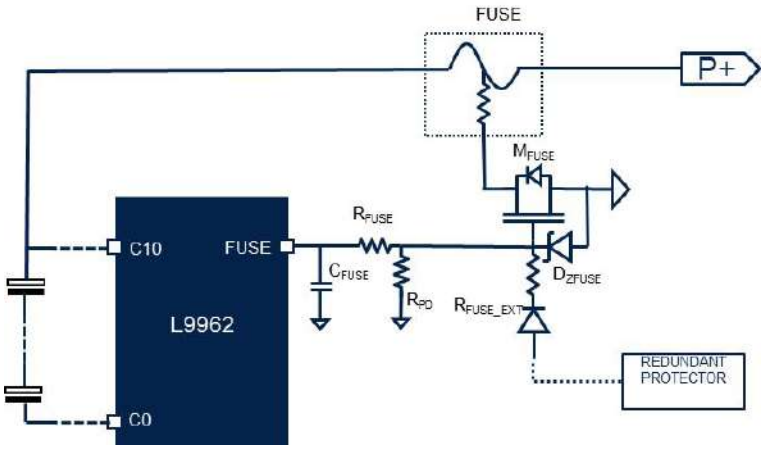


Table 38. **Typical BOM of the fuse circuit**

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{FUSE}	15	kΩ	10%	1/4W	Filters the signal coming from redundant protector: cut-off frequency is $f_C = \frac{1}{(2\pi R_{FUSE} C_{FUSE})}$
C_{FUSE}	2.2	nF	10%	60V	Filters the signal coming from redundant protector: cut-off frequency is $f_C = \frac{1}{(2\pi R_{FUSE} C_{FUSE})}$
R_{FUSE_EXT}	15	kΩ	10%	1/4W	Decoupling resistor for wired-OR connection with a secondary protector
M_{FUSE}				100V	The STD47N10F7AG is recommended
D_{ZFUSE}	14	V			
FUSE				62V	The ITV5432L4030WR is recommended for applications up to 30A
R_{PD_FUSE}	1	MΩ	10%	1/8W	Pull-down resistor. It is intended to keep the voltage low in STANDBY state.
D_{FUSE_EXT}					Diode reverse voltage has to be chosen according to VFUSE_EXT. Example: if VFUSE= 3.3 V, the diode reverse voltage can be 20 V; if VFUSE= 60 V, the diode reverse voltage has to be at least 60 V.

5.7 Digital I/Os

Figure 21. **Typical digital I/Os circuit**

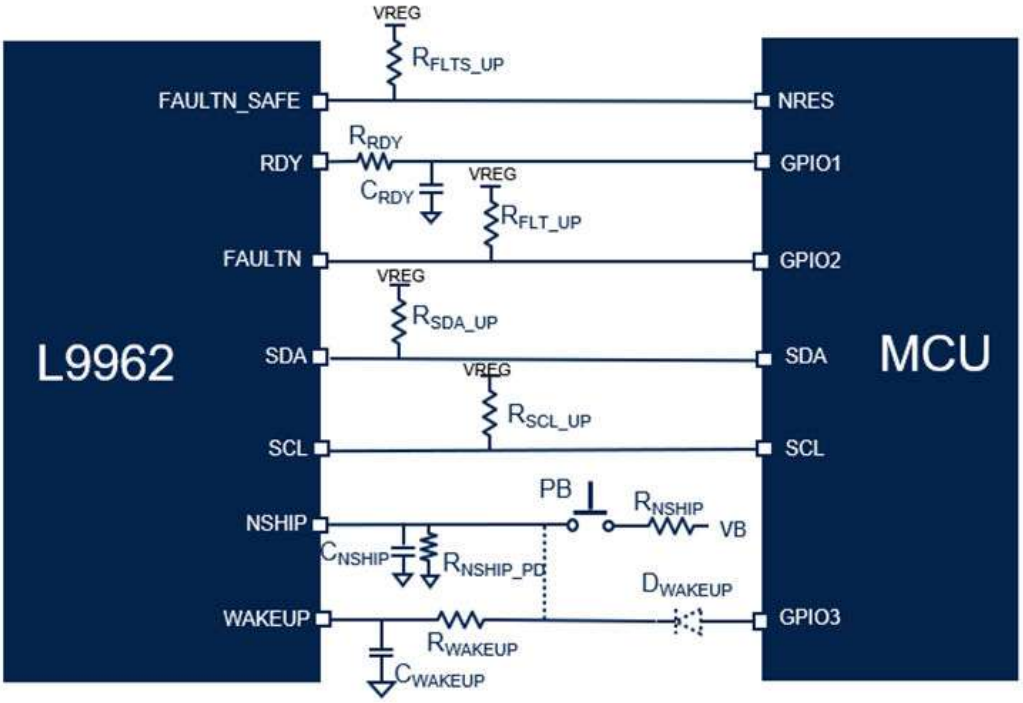


Table 39. **Typical BOM for a digital I/Os circuit**

Components	Value	Unit	Max. tolerance	Rating	Comments
R_{FLTS_UP}	4.7	kΩ	10%	1/10W	Pull-up resistor
R_{FLT_UP}	4.7	kΩ	10%	1/10W	Pull-up resistor
R_{SCL_UP}	4.7	kΩ	10%	1/10W	Pull-up resistor
R_{SDA_UP}	4.7	kΩ	10%	1/10W	Pull-up resistor
R_{RDY}	100	Ω	10%	1/8W	LPF resistor for RDY signal. The differential filter cut-off frequency is $f_C = \frac{1}{(4\pi R_{RDY} C_{RDY})}$
R_{NSHIP}	10	kΩ	10%	1/10W	Debouncing filter resistor for push button
R_{NSHIP_PD}	100	kΩ	10%	1/10W	Pull-down resistor
R_{WAKEUP}	1	kΩ	10%	1/10W	Debouncing filter resistor for push button
C_{NSHIP}	100	nF	10%	100V	Debouncing filter capacitor for push button
C_{WAKEUP}	100	nF	10%	100V	Debouncing filter capacitor for push button
C_{RDY}	100	pF	10%	16V	LPF capacitor for RDY signal. The filter cut-off frequency is $f_C = \frac{1}{(4\pi R_{RDY} C_{RDY})}$

Components	Value	Unit	Max. tolerance	Rating	Comments
PB					Push button to wake up L9962 from SHIPMENT - DEEP SLEEP state
D_{WAKEUP}	100	V			Blocking diode

5.8 Charger connection

In case of LS configuration, if the charger is hot-plugged (that is, with its two terminals not in High-Z condition), the VSC pin needs to be protected against AMR violation. ST recommends the application circuit in Figure 22.

On the contrary, the HS configuration does not require any additional components, but requires the FET's common drain to be connected to VB in order to feed the CP with the higher voltage between the battery stack and battery charger, thus ensuring the right overdrive to switch on the discharge MOSFET.

Figure 22. Application circuit in LS/HS configuration

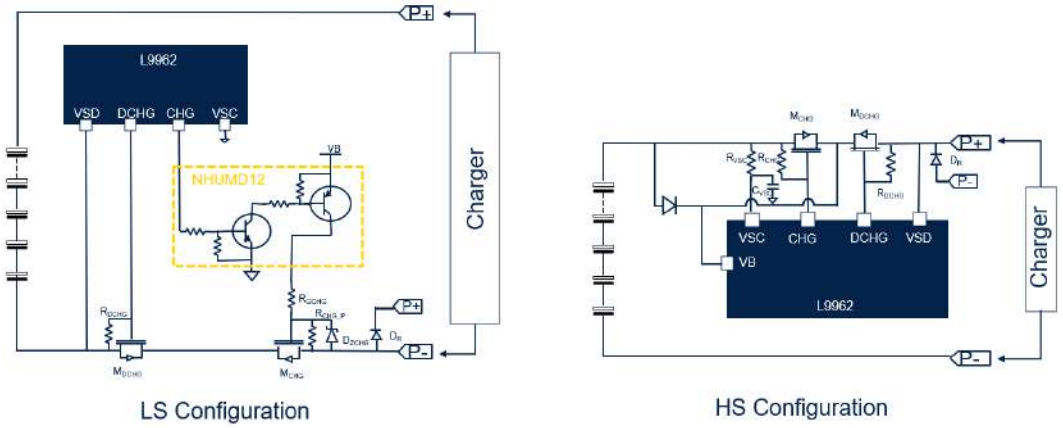


Table 40. BOM in LS configuration when charger is hot-plugged

Components	Value	Unit	Max. tolerance	Rating	Comments
RCHG_P	220	kΩ	5%	1/10W	Pull-down resistor
RGCHG	22	kΩ	5%	1/4W	Limits Zener current
DZCHG	14	V			Clamps the VGS of the CHG MOSFET
NHUMD12					Level shifter used to drive the CHG MOSFET. NHUMD12 NPN-PNP transistor switch pair is recommended.

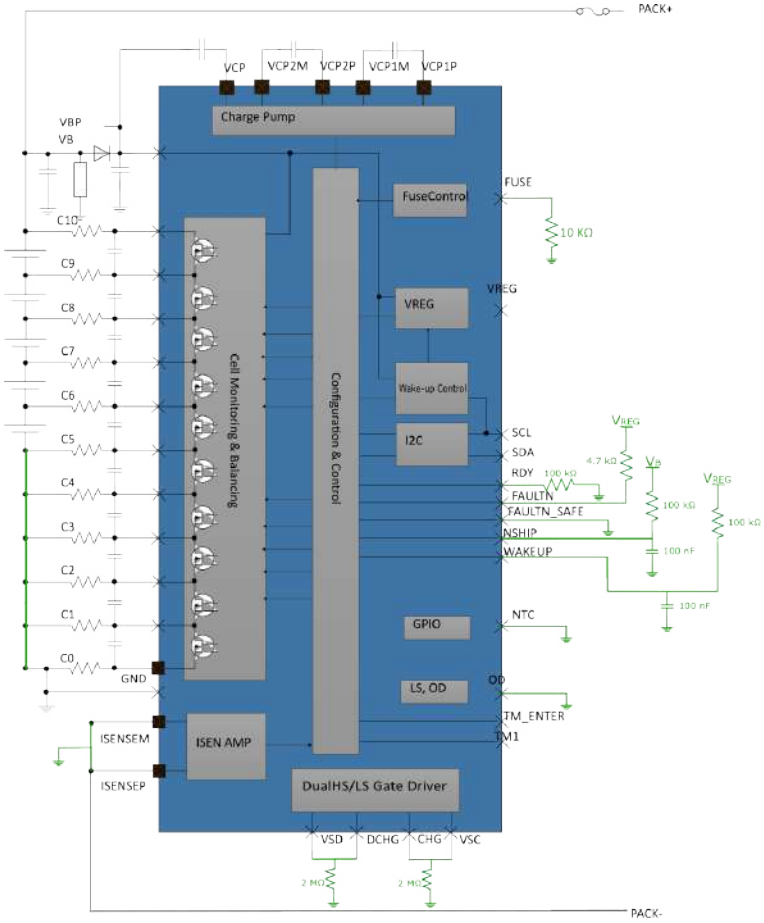
5.9 Unused pins connections

Cells shall be mounted starting from the top pair (C10-C9) and moving downwards. C pairs (CX – CX-1) which are completely unused shall be short-circuited and connected to the negative terminal of the first mounted cell upwards.

If less than 5 cell channels are used:

- Mount the cells starting from the top-most (C10-C5).
- A minimum of 5 cells must be connected to the L9962 and the top-most cell of the stack must be connected to the C5 pin.

Figure 23. Unused pins connections



Besides, for other functions, when not used, the recommended pin configuration is according to the following table:

Table 41. Typical unused pins connection

Unused pin #	Symbol	Pin functions	Pin type	Connection
8	ISENSEP	Current sense ADC positive input terminal	Analog in	Short to ISENSEM and connect to GND
9	ISENSEM	Current sense ADC negative input terminal	Analog in	short to ISENSEP and connect to GND
18	RDY	Ready interrupt output	Push/pull	Pull-down to GND by 100 kΩ
13	NTC	NTC sensing input	Analog in	Short to GND

Unused pin #	Symbol	Pin functions	Pin type	Connection
14	OD	Open-drain switch for NTC connection to GND	Open-drain	Short to GND
15	FAULTN_SAFE	Critical fault output	Open-drain	Short to GND
16	FAULTN	Fault output / external CHG DCHG shutdown trigger	Digital input / open-drain	Pull-up 4.7 kΩ to V_{REG}
22	WAKEUP	Wakeup from STANDBY input	Digital I/O	Short to GND through C=100nF and pull-up to VB through R=100 kΩ
23	NSHIP	Wakeup from SHIPMENT - DEEP SLEEP input	Analog input	Short to GND through C=100nF and pull-up to Vreg through R=100kΩ
24	FUSE	Fuse pre-driver output / external fuse activation trigger	Analog out/digital in	Pull-down to GND by 10 kΩ
26/27	DCHG-VSD	Discharge switch gate	Analog out	Short VSD to DCHG and pull-down to GND through R=2MΩ
28/29	VSC-CHG	Charge switch source and gate	Analog out	Short VSC to CHG and pull-down to GND through R=2 MΩ
47-43	C1, C2, C3, C4, C5	Cell sensing/balancing terminal	Analog in	Shorted to GND
48	C0	Cell sensing/balancing negative terminal	Analog in	Short to C1 and short to GND

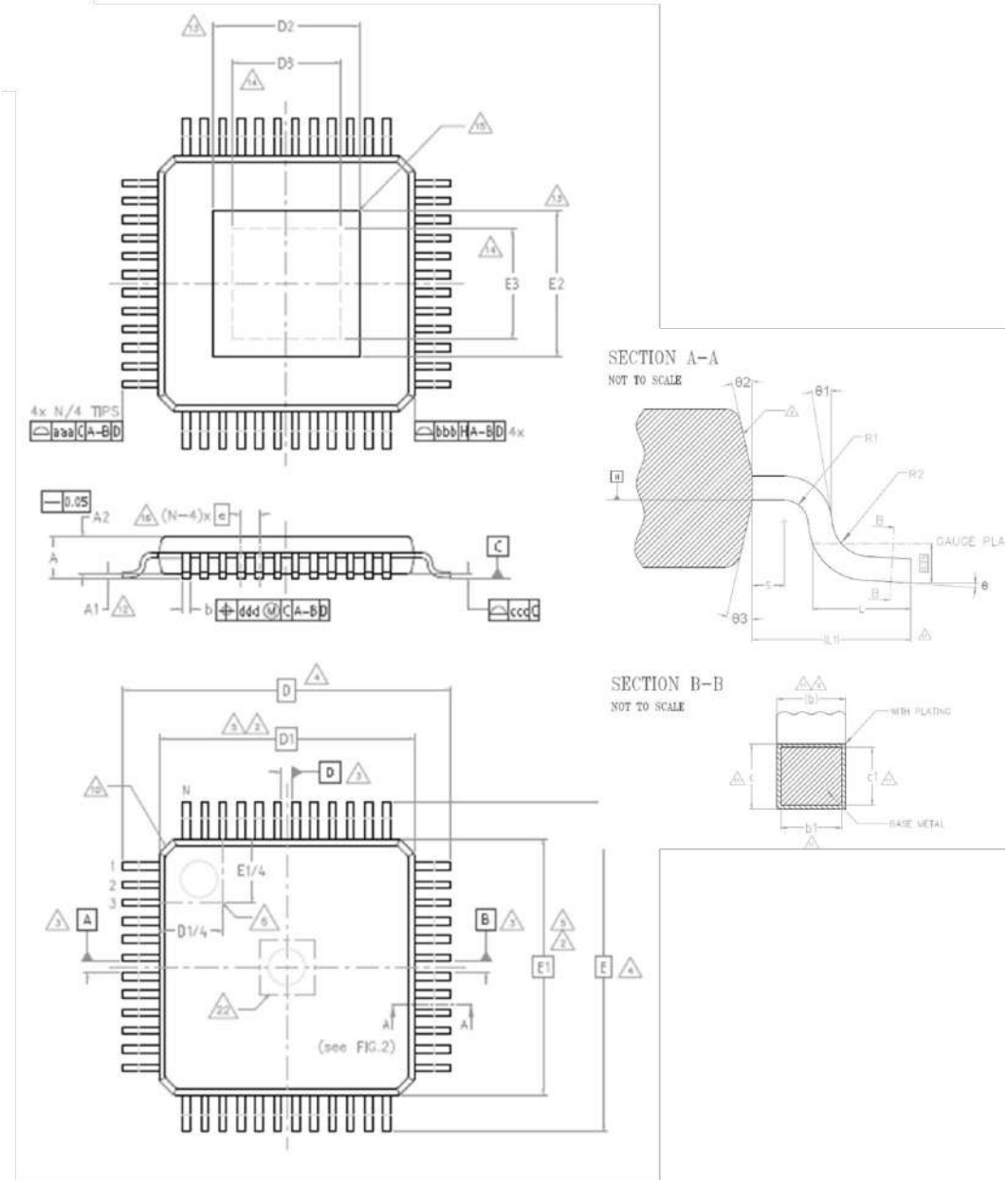
6 Package Information

In order to meet environmental requirements, ST offers these devices in different grades of *ECOPACK* packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

6.1 TQFP 7x7 48L EXPOSED PAD DOWN package information

Figure 24. TQFP 7x7 48L EXPOSED PAD DOWN

BOTTOM VIEW



TOP VIEW

Figure 25. **Proposed PCB landpattern**

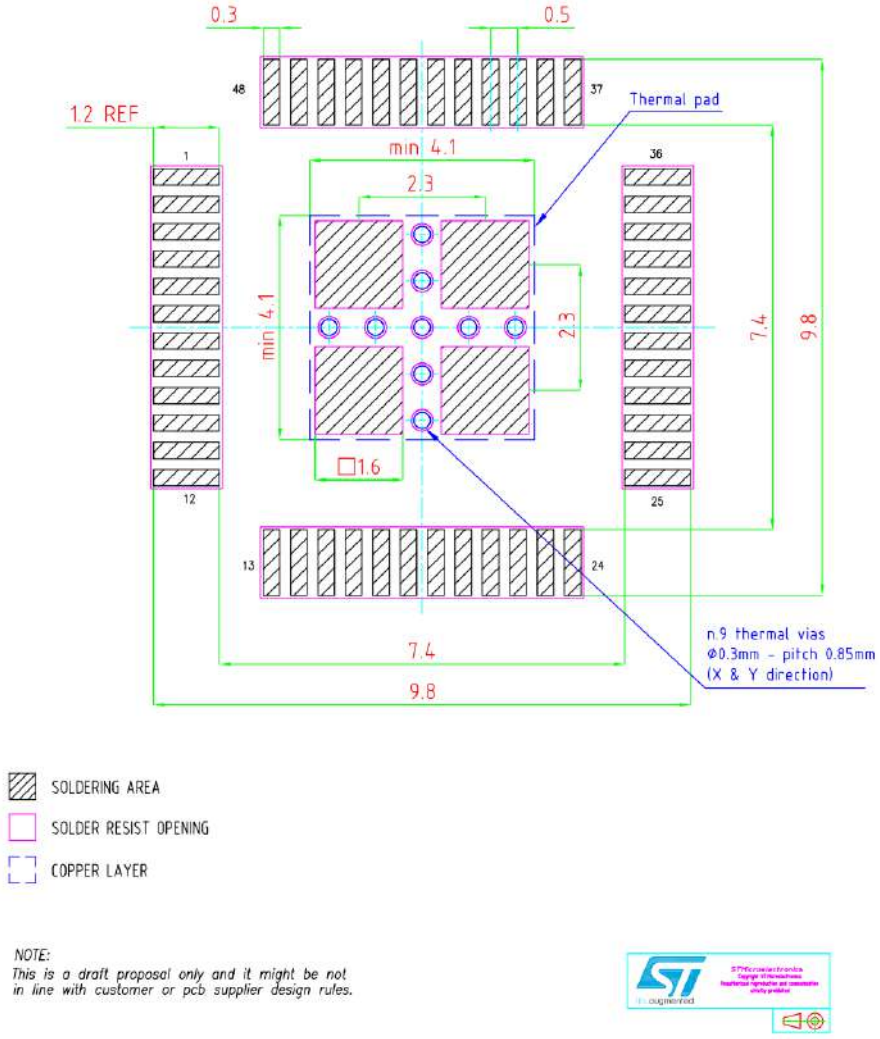


Table 42. **TQFP 7x7 48L EXPOSED PAD DOWN package mechanical data**

ST Databook				
Symbol	**Min.**	**Nom.**	**Max.**	**Note**
Θ	0°	3.5°	7°	
Θ1	0°	-	-	
Θ2	10°	12°	14°	
Θ3	10°	12°	14°	
A	-	-	1.20	15
A1	0.05	-	0.15	12
A2	0.95	1.00	1.05	15
b	0.17	0.22	0.27	9,11
b1	0.17	0.20	0.23	11
c	0.09	-	0.20	11
c1	0.09	-	0.16	11
D	9.00 BSC			4
D1	7.00 BSC			2,5
D2	-	-	4.47	13
D3	2.50	-	-	14
e	0.50 BSC			
E	9.00 BSC			4
E1	7.00 BSC			2,5
E2	-	-	4.47	13
E3	2.50	-	-	14
L	0.45	0.60	0.75	
L1	1.00 REF			
N	48			16
R1	0.08	-	-	
R2	0.08	-	0.20	
S	0.20	-	-	

Table 43. **Tolerance of form and position**

Tolerance of form and position		
Symbol	**ST databook**	**Note**
aaa	0.20	1,7,20
bbb	0.20	
ccc	0.08	
ddd	0.08	

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.

5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "*0.25 mm*" per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.

6. Details of pin 1 identifier are optional but must be located within the zone indicated.

7. All Dimensions are in millimeters.

8. No intrusion allowed inwards the leads.

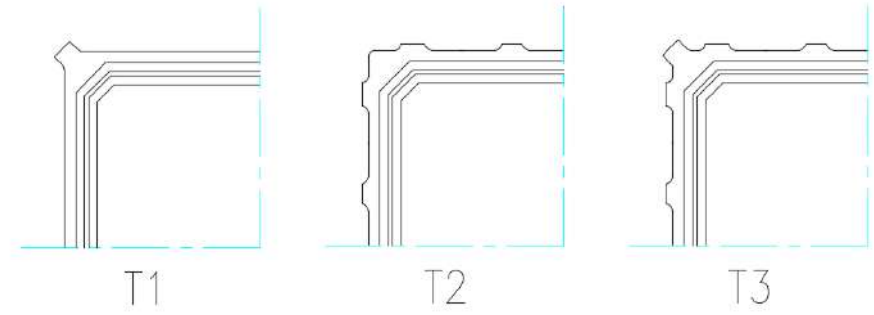
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.

10. Exact shape of each corner is optional.

11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.

12. A1 is defined as the distance from the seating plane to the lowest point on the package body.

13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad is variable depending on leadframe pad design (T1, T2, T3), as shown in the figure below. End user should verify D2 and E2 dimensions according to specific device application.



14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.

15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.

16. "N" is the number of terminal positions for the specified body size.

17. For Tolerance of Form and Position see Table.

18. Critical dimensions:
    - 18.1 Stand-Off
    - 18.2 Overall Width
    - 18.3 Lead Coplanarity

19. Component cross reference: DM00516738.

20. For Symbols, Recommended Values and Tolerances see Table below:

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the "coplanarity" of the package terminals.

Symbol	Definition	Notes
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

21. POA FORMAT & CONTENT spec. reference number is CD10033601.

22. Notch may be present in this area (MAX 1.5mm square) if center top gate molding technology is applied. Resin gate residual not protruding out of package top surface.

Parts marked as ES are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7 Ordering information

Table 44. **Ordering information**

Order code	Package	Packing
L9962	TQFP48	Tray
L9962-TR		Tape&Reel

Revision history

Table 45. **Document revision history**

Date	Version	Changes
15-Jan-2026	1	Initial release.
04-Feb-2026	2	Minor changes, typos correction in the document and updated images Section 5.5, Figure 20 and Figure 23
06-Mar-2026	3	Minor changes to Section 3.7.1 Battery pack charge/discharge relays (CHG/DCHG) and Section 5.5 HS/LS pre-drivers circuit
16-Jun-2026	4	Updated Table 23, modified Section 4: Device register map and Figures in Table 36.

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