Arm® Cortex®-M33 32-bit MCU , 180 MHz, 512 KB Flash, 128 KB SRAM, with Programmable Power Control Accelerator (Dual Cortex®-M33, 200 MHz, 112 KB SRAM)

Features




- High-performance, low-power 32-bit single-core Arm® Cortex®-M33-based microcontroller featuring a DSP, FPU, MPU, TrustZone (TZ) extension, state-of-the-art security features, 512 KB Read-While-Write (RWW) Flash with ECC support, and 128 KB SRAM
- **Programmable power control accelerator (PPCA)**:
  - Two independent Arm® Cortex®-M33 microcontroller cores with DSP, FPU and 112 KB SRAM
  - Four 12-bit, 25 Msps SAR ADC modules with parallel sampling of up to 24 channels, with up to 6 channels supporting 64x oversampling for 15-bit effective resolution
  - Nine differential comparator slope generators with <10 ns latency
  - Built-in 12-bit DAC and two Coordinate Rotation Digital Computer (CORDIC) blocks
  - 14x 16-bit and 12x 32-bit timer/counter pulse-width modulators (TCPWM) supporting <100 ps high-resolution pulse-width modulator (HRPWM)
  - Configurable and programmable Events Processing Unit (EPU) block
  - Two independent 3P3Z hardware filter blocks with six channels and a Custom Logic Block (CLB) featuring a digital current observer and matrix converter
- Additional, 2x 16-bit, and 2x 32-bit TCPWM
- **Communication interfaces**: Up to seven serial communication blocks (SCBs), including two with PMBus support. It also provides two CAN FD interfaces, with one supporting speeds up to 8 Mbps
- **Low-power operation**: Supports Sleep and Deep Sleep modes with three configurable options
- **Input/Output**: Offers up to 60 GPIOs (14 analog capable), and up to 26 dedicated analog inputs
- **Security**: PSA L2 certified. Some devices are PSA L3 certified
- **Safety**: Class B and SIL 2 compliant safety test libraries are available
- **Packages**: VQFN-48, VQFN-64, E-LQFP-64, E-LQFP-80, E-LQFP-100, with an operating temperature range of T_A = - 40°C to 115°C

Green

Halogen-free

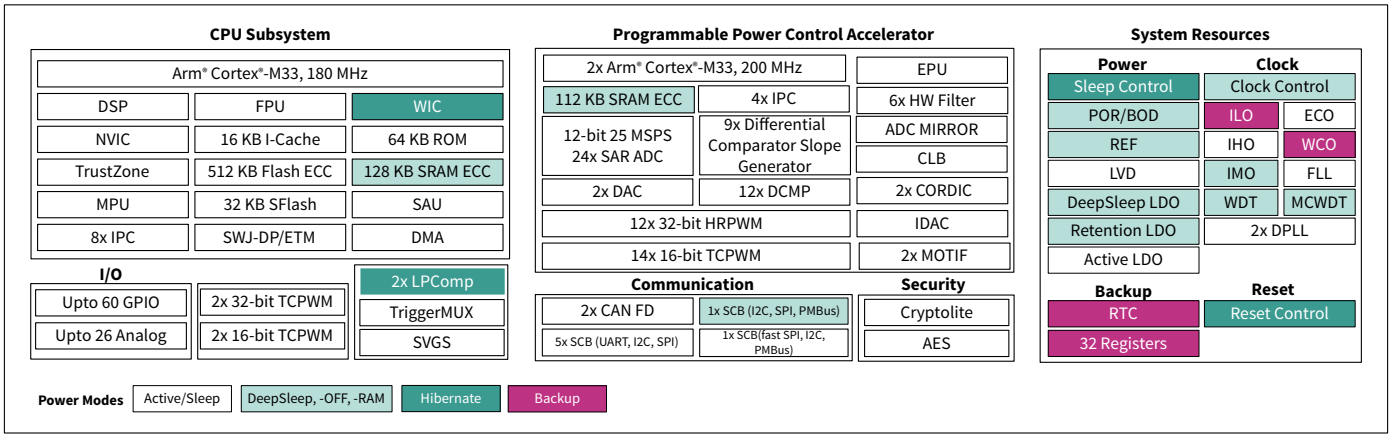
Lead-free

Target applications

- Digital power applications with switching frequencies up to 2 MHz, used in power supplies for AI servers, telecom, EV chargers, and solar systems
- High-switching-frequency wide-bandgap technologies such as silicon carbide (SiC) and gallium nitride (GaN), enabling power conversion and motor control applications
- Motor control application devices for appliances, light electric vehicles, robots, and drones

Description

The PSOC™ Control C3(P/M)(8/7)x devices use an Arm® Cortex®-M33 running up to 180 MHz with DSP/FPU, and PPCA block with two Cortex®-M33 cores running up to 200 MHz. Features include 12-bit 25 Msps ADCs, comparators with differential-slope generators, hardware filters, a custom logic block, DACs, and advanced high-resolution timers.



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1 Introduction

The PSC3P8xx, PSC3M8xx, PSC3P7xx, and PSC3M7xx devices are part of the PSOC™ Control C3 MCU family, designed for real-time control, enhanced sensing, secure operation, and low-power applications.

Target applications include:

- Telecom and AI server high-power conversion systems
- Power-stage converters
- EV chargers
- Automation devices
- Home appliances
- Industrial motor controllers

A detailed block diagram of the MCU is shown in Figure 1.

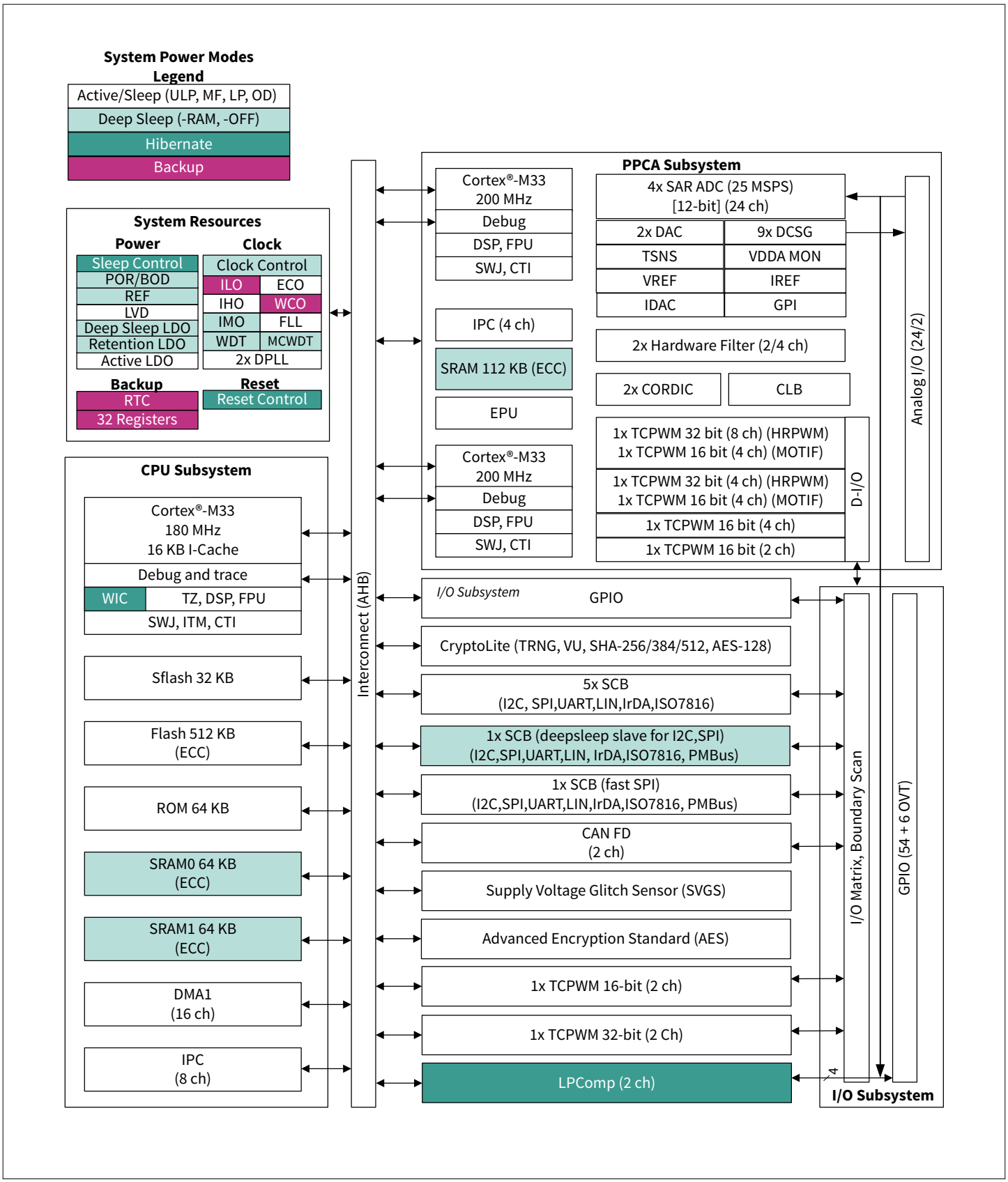


Figure 1 Functional block diagram

Device identification and revisions

Family ID = 0x119 (12-bit); Si ID range = EE80 - EE96; Major-minor rev ID = 0x1, 0x1

2 Detailed features

This device supports the following features:

- **CPU subsystem**:
  - Arm® Cortex®-M33 processor running at up to 180 MHz
  - Digital signal processor (DSP), floating-point unit (FPU), memory protection unit (MPU), and 16 KB instruction cache (I-cache)
  - One direct memory access (DMA) controller with 16 channels
- **Security**:
  - Some devices are Platform Security Architecture Level 2 (PSA L2) certified, and some are PSA L3 certified
  - Features secured boot, secured firmware update, secured debug, and secured RMA mode for field failure analysis
  - Infineon proprietary protection units for memory and peripherals
  - Stepwise authentication of execution images until control is handed over to usercode
  - Secure execution of code in execute-only mode for protected routines
  - Image authentication and integrity check
  - TrustZone framework that establishes an isolated device root of trust (RoT) for trust attestation and software management
- **Memory**:
  - On-chip flash memory:
    - Up to 512 KB Flash with error correction code (ECC) support, RWW capability, 64 KB ROM for boot code, and bootloader functions, 32 KB reserved for the supervisory region
    - Built-in device firmware upgrade (DFU) support in the boot ROM via a serial interface (UART)
  - Static random access memory (SRAM):
    - 128 KB SRAM with ECC support
    - Organized as two independent 64 KB blocks (SRAM0 and SRAM1)
    - Full 64 KB + 64 KB SRAM is available in Deep Sleep mode
    - Protected SRAM data path using hardware ECC for soft error detection and correction
- **Clocking subsystem**:
  - 8 MHz IMO with Deep Sleep operation, offering ±2% accuracy
  - 48 MHz internal high-frequency oscillator (IHO) with ±1% accuracy
  - 4 to 35 MHz external crystal oscillator (ECO) with a phase-locked loop (PLL) for CPU and subsystem clocking
  - 32 kHz external watch crystal oscillator (WCO), usable for real-time clock (RTC) applications
  - 32 kHz internal low-frequency oscillator (ILO) with ±10% accuracy
  - External clock (EXTCLK): Maximum frequency 100 MHz
  - One frequency lock loop (FLL) with 25-100 MHz output range
  - Two digital phase-locked loops, DPLL#0 and DPLL#1, with 50-200 MHz output range
- **Low-power operation**:
  - Operates at low power with a voltage range of 1.71 V to 3.63 V
  - Supports six power modes for fine-grained power management:
    - Active
    - Sleep
    - Deep Sleep
    - Deep Sleep-RAM

  - Deep Sleep-OFF
  - Hibernate
- **Deep Sleep mode**:
  - Current draw of 16 µA at a 3.3 V external supply using an internal voltage regulator
- **Hibernate mode**: Current draw of up to 1 µA with RTC and LPComp enabled

- **Communication peripherals**:
  - **Serial communication blocks (SCBs)**:
    - Up to five independent run-time-reconfigurable SCBs:
      - Each SCB is software-configurable as I^2C, SPI, or UART in master or slave mode
    - Two additional run-time-reconfigurable SCBs with PMBus protocol support:
      - Software-configurable as master or slave for I^2C, SPI, or UART protocols
      - PMBus protocol features:
        - Baud rates of up to 1 Mbps
        - Timeout event generation (TGS) for wrong or stuck commands
        - Hardware address screening with support for a minimum of five slave address masks (MSAs) to reject or NACK incoming address commands
        - Compliance with PMBus (v1.4) and SMBus (v3.2) specifications
      - One SCB instance supports wakeup from Deep Sleep mode with PMBus extensions
    - **Additional features**:
      - One SCB supports operation in Deep Sleep mode and wakeup from Deep Sleep in I^2C slave and SPI slave modes
      - One SCB supports fast SPI operation with speeds of up to 50 MHz
      - SCBs support single-wire, half-duplex mode for UART communication
  - **CAN FD**:
    - Supports up to two CAN FD channels
    - Each channel operates at speeds of up to 8 Mbps
- **I/O subsystem**:
  - **Programmable GPIO pins**:
    - Supports up to 86 functional pins, including 60 digital GPIOs, 24 dedicated analog-only inputs (14 of the 60 GPIOs are analog inputs capable), and two dedicated analog pins configurable as inputs or outputs only
    - Provides programmable drive modes, strengths, and slew rates
    - Six of the 60 GPIOs as *GPIO_OVT* to support PMBus/SMBUS compliance with input leakage specifications
    - Up to four *GPIO_OVT* pins can be routed to analog inputs of ATOP and used by the ADC or comparator
- **Cryptography**:
  - **Cryptography accelerator**:
    - Supports hardware acceleration for symmetric cryptographic algorithms (AES-128) and asymmetric cryptographic algorithms (RSA and elliptic curve cryptography (ECC)) through the vector unit (VU)
    - Support for hash functions such as SHA-256, SHA-384, and SHA-512
    - Provides a true random number generator (TRNG) function for enhanced security
  - **Advanced Encryption Standard (AES-256)**:
    - Provides high-performance AES-256 encryption with protection against unauthorized access
    - Supports key lengths of 128 bits and 256 bits for enhanced flexibility and security

- **Low-power comparator (LPComp)**:
  - Supports a pair of low-power comparators
  - Provides comparator thresholds for comparison, which can be sourced either from an external pin or an internal fixed reference of approximately 0.6 V ± 0.2 V
- **Timer/counter pulse-width modulator (TCPWM)**:
  - One group provides two 32-bit TCPWM channels
  - Another group provides two 16-bit TCPWM channels
  - Both TCPWM outputs and inputs are exclusively connected to the event processing unit (EPU) and trigger mux
  - One instance is clocked using a stable clock source and can be used for monitoring the main CPU
  - The second instance is clocked using a robust clock source to ensure reliable heart-beat monitoring of the PPCA and can be used for monitoring the PPCA CPUs
- **Supply voltage glitch sensor (SVGS)**:
  - A voltage-glitch sensor designed to detect supply-voltage manipulations by attackers attempting to disrupt device operation
- **Programmable power control accelerator subsystem (PPCA)**:
  - PPCA CPU subsystem:
    - **CPUs**:
      - Two Arm® Cortex®-M33 processors (CPU0 and CPU1), each operating at up to 200 MHz
      - Digital signal processor (DSP), floating-point unit (FPU)
    - **CPUs memories**:
      - Five instances of SRAM memory modules are available
      - SRAM supports ECC, allowing them to detect two errors and correct one error
      - Four local memory blocks with the following sizes: 32 KB, 16 KB, 32 KB, and 16 KB. The first two blocks are assigned to the first PPCA CPU (CPU0) for code and data. The other two blocks are allocated to the second PPCA CPU (CPU1) for code and data. If CPU1 is not used, these blocks serve as code extension and data extension for CPU
      - A 16 KB shared memory block is accessible by both PPCA CPU0 and PPCA CPU1. This memory can also be used as a data extension for either CPU0 or CPU1
    - **IPC block**:
      - An IPC block facilitates communication between PPCA CPU0 and PPCA CPU1. This block operates through the shared 16 KB SRAM
      - The IPC block supports one group, four channels, and four interrupts
    - **AMBA Bus infrastructure**:
      - Includes a bus matrix, five AHB slave inputs, and 12 AHB master outputs
  - **Analog TOP subsystem (ATOP SS)**:
    - **Analog-to-digital converter (ADC)**:
      - Four 12-bit (greater than 10-bit ENOB) SAR ADCs (ADC0 - ADC3) with a conversion rate of up to 25 Msps
      - Supports up to 12 dedicated differential analog input channels or up to 24 dedicated single-ended input channels
      - An option to connect 16 multiplexed additional analog inputs to two analog input channels
      - Input voltage range: -0.4 V to 3.3 V
      - Enables simultaneous sampling, arbitrary sampling, or continuous programmable sampling sequences

  - A selectable internal or external 1.2 V ADC voltage reference
  - An analog front end (AFE) with selectable input gain values of ×8.25, ×16.5, ×33, and ×66
  - Initiates the start of conversion (SOC) via a dedicated hardware signal per channel, per group of channels, or by writing into the ADC trigger register
  - Aligns the end of sampling (EOS) with the provided SOC or by using the control ADC conversion FSM
  - Provides a configurable ADC trigger source from the event processing unit (EPU)
- **Digital comparators (DCMP)**:
  - Features digital comparator outputs directed to the EPU
  - Up to 12 digital comparators with configurable digital thresholds
  - Generates an event when the input signal crosses the programmed threshold
  - Supports configurable comparison methods including immediate comparison, integration of immediate comparison, accumulation of immediate comparisons, and averaged comparisons
- **ADC filters (ADC FILTs)**:
  - The ADC embeds a configurable set of digital filters, including a median filter, linear interpolation/ extrapolation filter, low-pass filter, cascaded integrator third-order comb filter, configurable average filter, detection of minimum values in the input data stream, and detection of maximum values in the input data stream
  - Supports up to 64× oversampling, providing 15-bit effective resolution on up to six ADC channels
  - Filters can be chained together and optionally sourced from the output of another ADC core
  - The MIN/MAX module can be sourced either by the input or the output of the median filter
- **Differential analog comparator with slope generator (DCSG)**:
  - Features 9 active, configurable differential or single-ended comparators with a worst-case comparator delay of 5 ns
  - A differential analog comparator with an embedded DAC for programmable thresholds or references
  - Employs a dynamic latch comparator architecture, supporting a maximum clock frequency of 200 MHz
  - Three comparators with selectable digital slope generator
  - Supports a selectable input voltage range of 0 V to 3.3 V or ±200 mV
  - Ensures a maximum jitter of one clock cycle and a propagation delay of less than two clock cycles
  - Offset matches DAC resolution, providing ±0.7 mV for a 3.3 V rail-to-rail range and a 12-bit DAC
  - Supports 12-bit DAC threshold settings with differential non-linearity (DNL) less than four LSB
  - Ensures 10-bit monotonicity and a maximum DAC refresh rate of 50 Msps (minimum 20 Msps)
  - Guarantees less than 10 clock cycles settling time for 400 code jumps with an accuracy of ±8 LSB
  - Integrates a DAC refresh trigger function with a blanking time of less than 12 clock cycles
  - Supports A versus B comparisons
  - Provides comparator trigger inputs and outputs connected to the event processing unit (EPU) module
- **Digital-to-analog converter (DAC) R2R**:
  - Two 12-bit single-ended DACs with a refresh rate of 2 MHz
  - Ensures 10-bit monotonicity
  - Selectable DAC output ranges, including 0 V to VREF (1.2 V), 0 V to VDDA/2, ±0.2 V, or ±VDDA

  - Provides a selectable buffered DAC output full-scale range of 0.1 V to VDDA/2 or 0.1 V to VREF
  - Features a 50 pF load driver
- **Additional features**:
  - Temperature sensor (TSNS) with an accuracy of ±5°C
  - Provides a current reference (AREF) for ATOP subsystem resources
  - Voltage reference (VREF) for ATOP SS resources
  - Features a current digital-to-analog converter (IDAC) module to generate a selectable, known current for sensing external resistance
  - General-Purpose Input (GPI) module to convert an analog input into a digital output by using fixed analog thresholds
- **Event Processing Unit (EPU)**:
  - Facilitates flexible management of events generated by peripherals to create triggers
  - Supports trigger generation through a linear combination of processed input events and allows routing of input triggers as interrupts to the PPCA CPUs
  - Configurable and programmable event processing system, comprising 32 Type-1 processing units and 16 Type-2 processing units
  - Processes selected inputs connected to events generated by CPUs and peripheral resources, with outputs connected to triggers of CPUs and peripheral resources
  - Supports various functionalities, including asynchronous operation, synchronous bypass, input polarity inversion, and rising-edge extraction
  - Integrates filtering capabilities such as masking filters, blanking filters, de-bouncing filters (through integration), and pulse delays of up to 128 clock cycles
- **Hardware filter (HWFILT3P3Z)**:
  - Supports two instances of the hardware filter (HWFILT3P3Z), each of which can be allocated to one of the PPCA CPUs
  - The first instance supports four 3Poles3Zeros (3P3Z) hardware filters
  - The second instance supports two 3Poles3Zeros (3P3Z) hardware filters
  - Features a 16-bit input and a 24-bit output
  - A 40-bit multiplier and a 44-bit internal accumulator
  - Ensures execution latency of up to eight CPU clock cycles
  - Provides support for arithmetic 2's complement and saturation operators
  - Programmable dedicated data path for enhanced performance
- **Custom logic block (CLB)**:
  - The CLB module provides dedicated hardware support for specific functions or control algorithms that require high computational resources
  - Examples of supported functions include digital observers used in Totem Pole PFC controllers and matrix converter commutation
  - Additionally, the CLB module supports trajectory control and spread-pulse start-up functionalities
- **Coordinate Rotation Digital Computer (CORDIC)**:
  - Supports all CORDIC operating modes for solving circular (trigonometric) and hyperbolic functions
  - Integrates independent lookup tables to accelerate calculations for enhanced performance
- **Timer/Counter pulse-width modulation (TCPWM)**:
  - Four instances of TCPWM (TCPWM0 - TCPWM3) are available within the PPCA
  - All counters (PERIOD, DUTY, CC0, CC1, DT) support greater than or equal to (≥) match as well as equal to (=) match conditions

- Center-aligned, edge modes
- Shadow update of duty, period, dead-time, output signal polarity
- Comparator-based triggering of kill signals
- Trigger inputs for all instances are connected to the event processing unit (EPU) outputs, while trigger outputs for all instances are connected to the EPU inputs
- All four instances operate synchronously with the PPCA CPUs and run on the PPCA clock, with a maximum frequency of 200 MHz
- HRPWM feature for period, duty, and dead-time insertion with a typical resolution of less than 100 ps
- **First TCPWM instance (TCPWM0)**:
  - Eight 32-bit counters with high-resolution PWM (HRPWM) functionality
  - Parallel input data path for CC0 and CC1 registers enabled for four 32-bit counters
  - Four 16-bit counters, with the 16-bit counter group supporting MOTIF
  - PWM outputs for all 16-bit and 32-bit counters are connected to HSIOM
- **Second TCPWM instance (TCPWM1)**:
  - Four 32-bit counters with HRPWM functionality
  - Parallel data path for CC0 and CC1 enabled for two 32-bit counters
  - Four 16-bit counters, with the 16-bit counter group supporting MOTIF
- **Third TCPWM instance (TCPWM2)**:
  - Four 16-bit counters
  - Trigger inputs and outputs are connected to the EPU
  - Trigger outputs for PWM outputs are also connected to the trigger Mux
- **Fourth TCPWM instance (TCPWM3)**:
  - Two 16-bit counters
  - Trigger inputs and outputs are connected to the EPU
  - Trigger outputs for PWM outputs are also connected to the trigger Mux

3 Chip-level functional description

3.1 Power

The device provides advanced features for managing and reducing power consumption. It supports multiple power modes, including Active, Sleep, Deep Sleep, and Hibernate. Deep Sleep mode offers three variations based on the retention of SRAM.

The power control block ensures that voltage levels meet the requirements for each power mode. Its key functions include:

- Delay mode entry (for example, at power-on reset (POR)) until the voltage levels are suitable for proper operation
- Detects operation below safe power supply levels:
  - Generates interrupts for low-voltage detection (LVD)
  - Generates resets for brownout detection (BOD)

The device operates using a single, regulated VDDD and VDDIO supply within a range of 1.71 V to 3.63 V. The analog supply, VDDA, must be within a range of 2.6 V to 3.63 V. The external analog reference supply, VAREF_EXT, provides a fixed reference voltage of 1.2 V for the ADC and DCSG.

In addition, an optional VBACKUP supply is available, with a range of 1.71 V to 3.63 V. A linear regulator powers the core logic at four voltage levels: 0.9 V, 1.0 V, 1.1 V, and 1.2 V. Voltage-level switching is implemented by writing to the power control registers. The core logic voltage can be set based on the application's performance and power requirements. Clock gating at peripheral and bus levels allows fine-grained energy optimization.

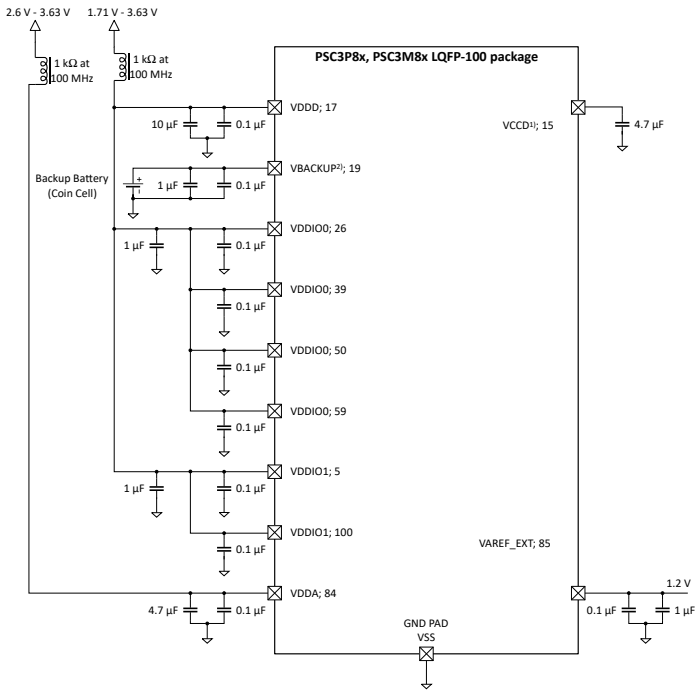
The backup domain typically requires an input voltage of 1.71 V to 3.63 V, which can be provided by connecting a backup battery or supercapacitor to the VBACKUP pin. The internal backup switch automatically selects between VDDD and VBACKUP when VDDD is no longer available. This ensures that the backup domain peripherals, such as RTC, WCO, ILO, and backup registers, remain powered. Some I/O cells are powered by the VBACKUP supply before the internal backup switch. If a dedicated backup source is not required, VBACKUP can be connected externally to VDDD to ensure that I/O cells powered by VBACKUP remain functional.

The device includes multiple VDDIO pins to power I/O cells, except those in the backup domain. VDDIO can either share the same supply as VDDD or use an independent supply voltage within the valid operating range. This flexibility allows different logic levels for port pins powered by separate VDDIO supplies. The VDDIO supply can be switched off if the port I/Os are not in use. However, switching off the VDDIO supply is permitted only in Active or Deep Sleep modes. It must not be switched off when the device is in Hibernate mode. For details about the VBACKUP or VDDIO supply used to power port I/O cells, see Pins.

3.1.1 Power connections

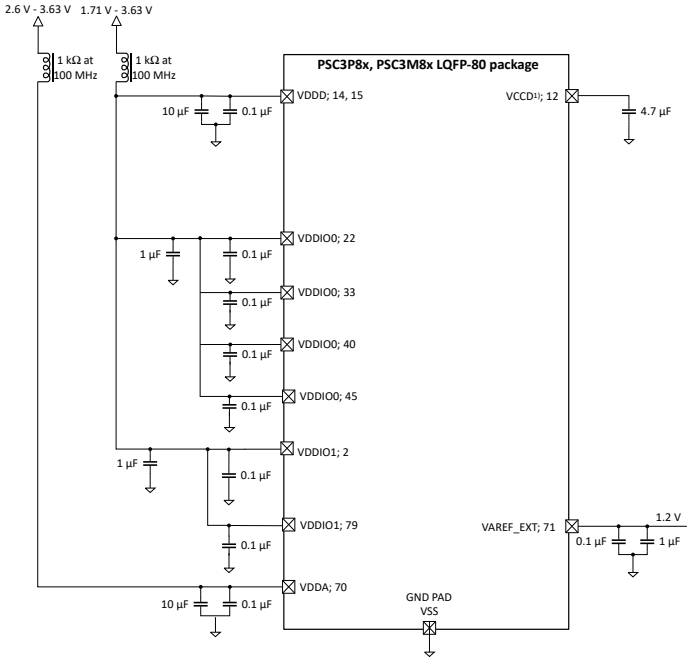
Figure 2 to Figure 5 illustrate typical connections for the power pins across all supported packages. In these diagrams, each package pin is labeled with its name and pin number, for example, “VDDD; 17”.

There is no dependency on power-supply sequencing.



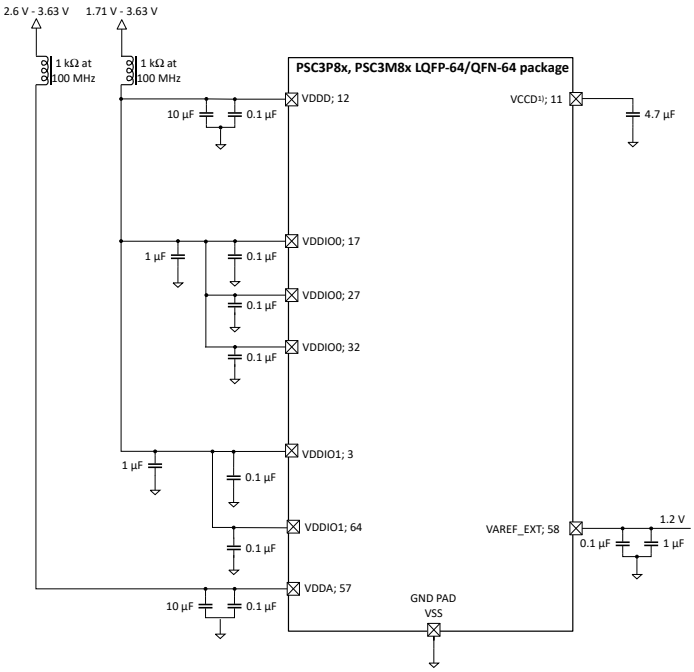
1) VCCD pin is only used to connect an external bypass capacitor for the integrated core logic supply LDO. Do not use to power external circuits.
2) VBACKUP can be connected to a coin cell (1.4 V to 3.63 V) or a supercapacitor depending on the application. If not used, it is connected to VDDD.

Figure 2 LQFP-100 package power connections



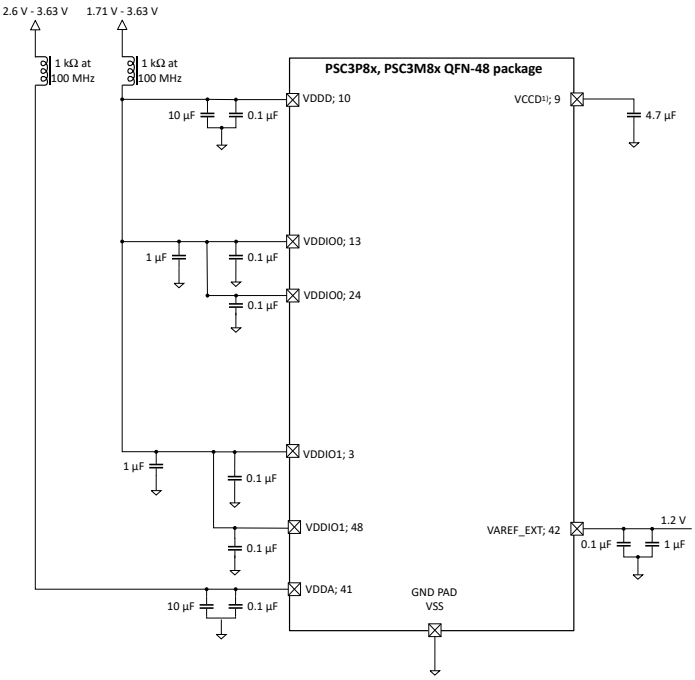
1) VCCD pin is only used to connect an external bypass capacitor for the integrated core logic supply LDO. Do not use to power external circuits.

Figure 3 LQFP-80 package power connections



1) VCCD pin is only used to connect an external bypass capacitor for the integrated core logic supply LDO. Do not use to power external circuits.

Figure 4 LQFP-64/QFN-64 package power connection



1) VCCD pin is only used to connect an external bypass capacitor for the integrated core logic supply LDO. Do not use to power external circuits.

Figure 5 QFN-48 package power connections

3.1.2 Power domains

The device features independent power domains, enabling power to be selectively turned on or off depending on the power mode.

A diagram of the power connections and routing is shown in Figure 6.

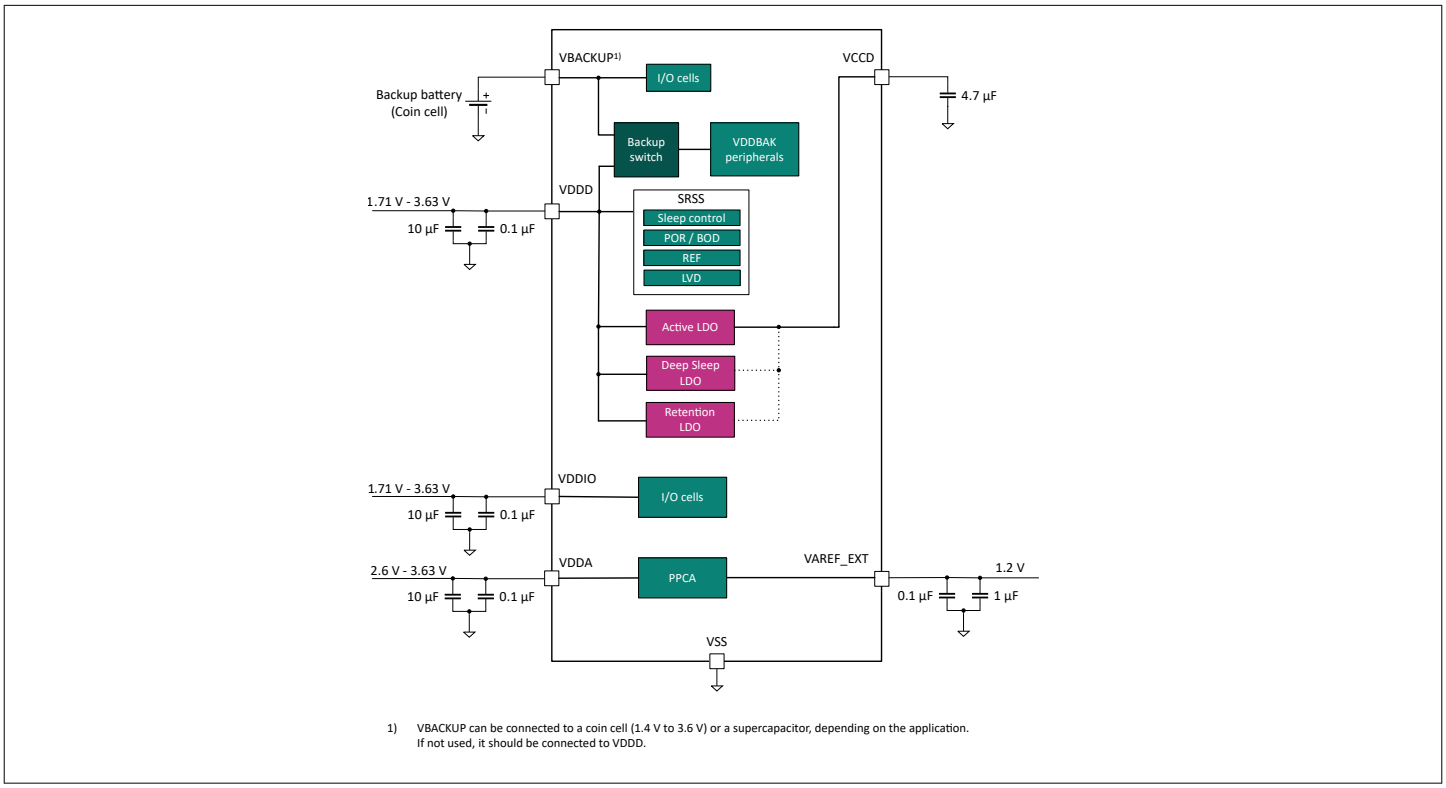


Figure 6 Power distribution and domains

3.1.3 Power modes

This product operates in five power modes designed to minimize average power consumption in applications. The supported power modes are as follows:

- **Active/Sleep**:
  - All peripherals are powered
  - The CPU is either active and executing code or in sleep mode (clock-gated)
  - Any interrupt can wake up the CPU within one CPU clock cycle to resume operation
  - In Active mode, the core voltage can be set to one of four values, which affects both power consumption and the maximum clock frequency for the CPU and peripherals

  The following Active modes are supported:

  - **Ultra-Low Power (ULP)**: 0.9 V core voltage with 50 MHz CPU, PPCA clock, and 25 MHz clock frequencies
  - **Medium Frequency (MF)**: 1.0 V core voltage with 70 MHz CPU, PPCA clock, and 35 MHz ATOP clock frequencies
  - **Low Power (LP)**: 1.1 V core voltage with 150 MHz CPU, PPCA clock, and 100 MHz ATOP clock frequencies
  - **Overdrive (OD)**: 1.2 V core voltage with 180 MHz CPU, 200 MHz PPCA clock, and 100 MHz ATOP clock frequencies
- **Deep Sleep**: The CPU remains in retention mode. System RAM and PPCA SRAM content are retained. Only Deep Sleep-capable peripherals can wake up the system. Once awake, the system resumes operation seamlessly

- **Deep Sleep-RAM**: The CPU is turned off, while System SRAM and PPCA SRAM are retained to enable a warm boot upon wakeup. Only Deep Sleep-capable peripherals, if enabled, remain operational and can wake up the system
- **Deep Sleep-OFF**: This mode is similar to Deep Sleep-RAM, except the RAM is also turned off. The wakeup action triggers a reset or a cold boot
- **Hibernate**: All peripherals, except LPComp and backup-domain peripherals, such as RTC and HIB, are turned off. All clocks, except the backup-domain clock, and all internal regulators are turned off, resulting in asynchronous operation of the LPComp. The system undergoes a reset upon exiting Hibernate mode

3.1.4 Power mode transitions

The device supports Arm®-standard power modes. See the Power modes section for detailed information. Table 1 lists the parameters for the supported power modes.

Table 1 Power mode support

	Active/Sleep	Deep Sleep	Deep Sleep-RAM	Deep Sleep-OFF	Hibernate	Off
Parameters						
Wake source[1)]	Any interrupt	DS peripherals	DS peripherals	DS peripherals	RTC/HIB peripherals	Power on
Wake action	Resume	Resume	Warm boot	Reset/cold boot	Reset	Reset
Wake time	One CPU cycle	<20 µs	Deep Sleep + warm boot	Deep Sleep + cold boot	POR + cold boot <= 4 ms	
Resources						
ECO	On/Off	On/Off	On/Off	On/Off	Off	Off
IHO	On	Off	Off	Off	Off	Off
IMO	On	On/Off	Off	Off	Off	Off
ILO	On/Off	On/Off	On/Off	On/Off	Off	Off
WCO	On/Off	On/Off	On/Off	On/Off	On/Off	Off
CPU	On/Sleep	Retention	Off	Off	Off	Off
PPCA (except SRAM)	On	Off	Off	Off	Off	Off
System SRAM	On	On/Off	On/Off	Off	Off	Off
PPCA SRAM	On	On	On	Off	Off	Off

1) For the list of peripherals available in Deep Sleep (DS) and Hibernate (HIB) power modes, see Power block support.

3.1.5 Power block support

Table 2 shows the available operational states for the major blocks in this device. Note that operational states in low-power modes are generally limited in functionality and parametric performance compared to their capabilities in Active power mode. Additionally, blocks that do not support low-power modes, such as Deep Sleep and Hibernate, cannot wake up the CPU from these power modes. See Power modes for more details.

Table 2 Block power modes

Block	Power mode				
	Active	**Sleep**	**Deep Sleep**	**Hibernate**	**Backup**
CPUSS					
CPU	Y	N	N	N	N
NVIC	Y	Y	N	N	N
WIC	Y	Y	Y	N	N
FLASH	Y	Y	N	N	N
SRAM	Y	Y	Y	N	N
DMA	Y	Y	N	N	N
Peripherals					
TCPWM (also in PPCA)	Y	Y	N	N	N
SCB	Y	Y	Y[1)]	N	N
CAN FD	Y	Y	N	N	N
LPComp	Y	Y	Y[2)]	Y	N
PPCA					
CPUs	Y	Y	N	N	N
SRAM	Y	Y	Y	N	N
CORDIC	Y	Y	N	N	N
ADC	Y	Y	N	N	N
DCSG	Y	Y	N	N	N
Custom logic block	Y	Y	N	N	N
Hardware filters	Y	Y	N	N	N
I/O					
GPIO	Y	Y	Y	Y[3)]	N
Backup					
RTC	Y	Y	Y	Y	Y
Registers	Y	Y	Y	Y	Y

1) Only SCB 0 (I^2C, SPI)
2) Only in Deep Sleep mode. Not available in Deep Sleep-RAM and Deep Sleep-OFF modes.
3) Only the hibernate_wakeup pins (P2.1 and P7.0) are operational and capable of waking the device from Hibernate mode. For more information, see Pins.

3.2 Security

This product line features an Arm® TrustZone-enabled Cortex®-M33 CPU as the main core and two Cortex®-M33 CPUs as a subsystem. It offers an isolated, fully secured, hardware-based Root of Trust (RoT) that supports secure boot, provisioning, and secure debugging.

Both secure and nonsecure debug accesses are supported. In nonsecure access, the debugger cannot access areas marked as “secure”. For secure access, the device can be “locked”, preventing it from being acquired for testing or debugging. A debug token ensures appropriate access for secure debugging and RMA transitions.

This device is fully compliant with Arm® TrustZone at both hardware and software levels. An additional layer of security is implemented using Infineon-proprietary protection units.

PSA L3-certified components support PSA-compliant cryptographic services, key management, and secure storage services.

3.2.1 Security features

- **Arm® platform security architecture**: Compliant with PSA Level 3 pre-certification
- **Secure boot and debug**: Support for secure boot, secure firmware updates, secure debug, and secure RMA mode for field failure analysis
- **Protected firmware features**: Firmware protection based on the part number
- **Hardware crypto accelerator**: Comprehensive support for cryptographic algorithms
- **Secure processing isolation**: Secure isolation of processing environments achieved via Arm® TrustZone
- Infineon-proprietary MPU, MPC, and PPCs for memory and peripheral access control
- **Trusted Firmware-M (TF-M)**: Off-the-shelf secure isolation using Trusted Firmware-M (TF-M) and mbedTLS cryptographic acceleration package

3.2.2 Security architecture overview

This product line features an Arm® TrustZone-enabled Cortex®-M33 CPU as the main core and two Cortex®-M33 CPUs as a subsystem as shown in Figure 7.

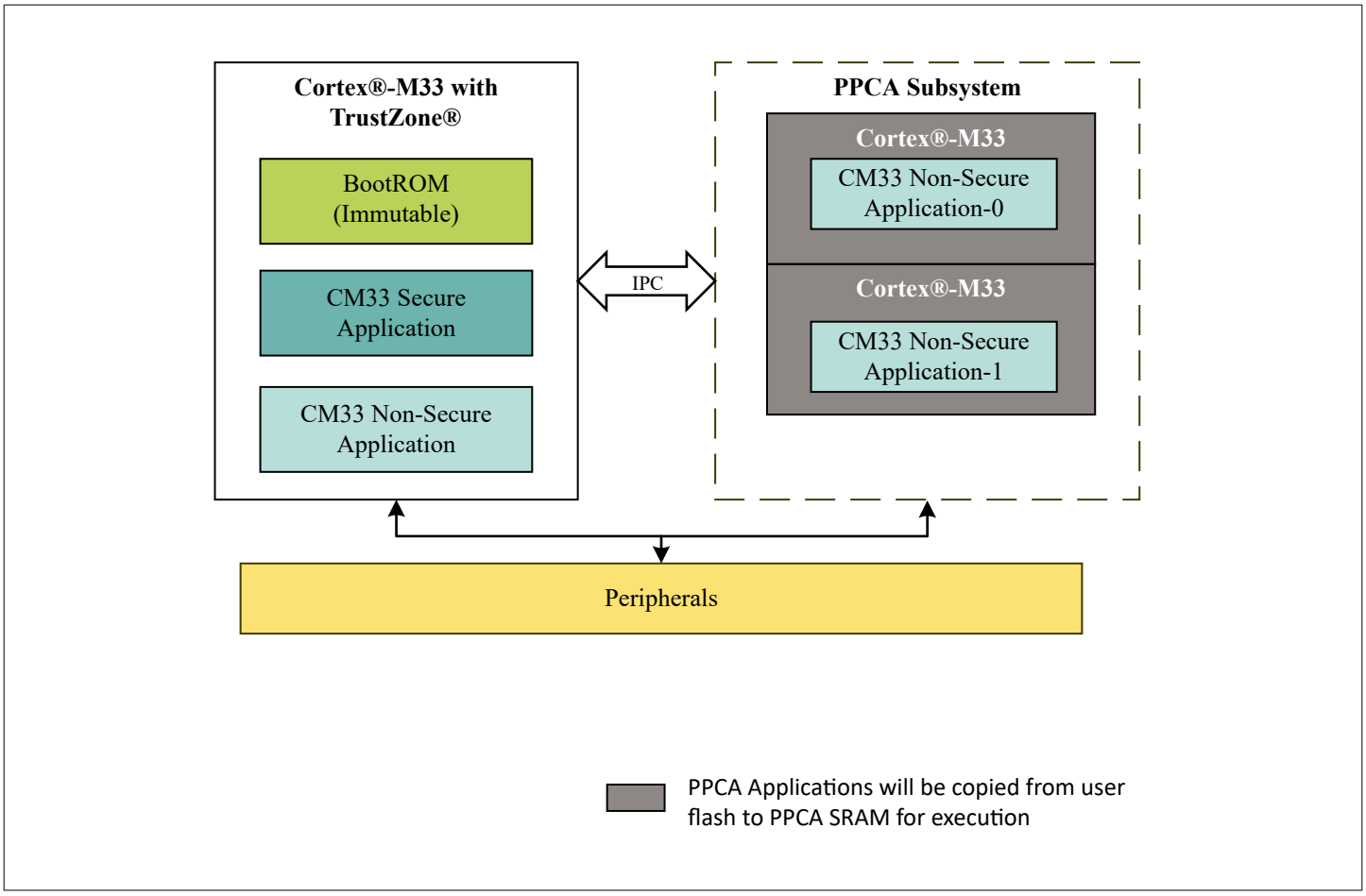


Figure 7 Security architecture

3.2.2.1 Cortex®-M33 with TrustZone

- **Arm® TrustZone-enabled core**: Supports two processing environments - secure (SPE) and nonsecure (NSPE)
- **Infineon-proprietary protection units**: Provides memory and peripheral protection
- **Integrated mbedTLS crypto acceleration package**: Supports both software and hardware cryptography services
- **Trusted Firmware-M (TF-M)**: Provided by Infineon and implemented in SPE. Its services are utilized by the Cortex®-M33 in both NSPE and SPE

4 Block functional description

4.1 CPU

- **Arm® Cortex®-M33**: Includes a digital signal processor (DSP) and floating-point unit (FPU)
- **TrustZone framework**: Establishes an isolated device Root of Trust for trusted attestation and software management
- **Memory protection unit (MPU)**: Supports eight regions each for secure and non-secure MPUs
- **Secure attribution unit (SAU)**: Defines the security status of up to eight memory regions
- **Debug facilities**: Includes trace capabilities with an embedded trace macrocell (ETM) but does not include an embedded trace buffer (ETB)
- **Instruction cache (I-cache)**: Features a 16 KB I-cache for flash and ROM access

A separate 8-channel interprocessor communication (IPC) module with two IRQs provides seamless support for semaphores and mailbox structures within secure and non-secure execution.

The subsystems include an interrupt controller, such as a nested vectored interrupt controller (NVIC). The chip also includes a wake-up interrupt controller (WIC), which wakes the processor from system Deep Sleep mode. This feature allows the main processor's power and clocks to remain turned off when the chip is in Deep Sleep mode, conserving energy.

The CPU subsystem incorporates debug interfaces and supports both SWD and JTAG. Additionally, the chip supports boundary scan, essential for testing on a PCB. A separate test access port (TAP) controller is provided to manage boundary scan functions.

4.2 DMA

The Cortex®-M33 CPU includes a DMA controller that facilitates data transfers between memory and peripheral registers. These controllers enable autonomous data transfers from peripherals, such as an ADC, to memory. They also provide deterministic control of peripherals, such as PWM.

The DMA controllers act as bus masters within their respective domains. It includes 16 channels and operates with a single transfer engine that arbitrates bus master access for all channels. The DMA controllers utilize the 32-bit AHB bus, which shares the same clock as the CPU.

4.3 Cryptography support (CryptoLite)

One instance of the cryptographic acceleration block that implements hardware support for true random number generator (TRNG), SHA-256/384/512, AES-128, and vector unit (VU), is provided.

4.4 Advanced Encryption Standard (AES-256)

The device supports hardware acceleration for the Advanced Encryption Standard (AES-256). The hardware is programmable to perform AES encryption or decryption with key lengths of 128/256 bits. It includes built-in security features, such as masking and redundancy mechanisms, to protect the key, input data, and output data from power analysis, fault, and probing attacks.

4.5 Memory

The device includes multiple types of non-volatile and volatile memory. Both the CPU and other bus masters have access to all memory blocks. The number of wait states varies depending on the access path.

4.5.1 Flash

The device offers up to 512 KB of user-programmable flash memory. The flash supports both single and dual-bank modes. Dual-bank mode enables the Read-While-Write (RWW) feature, allowing one sector to be read while another sector is being programmed. Additionally, the flash module includes ECC support.

4.5.2 SFlash

All devices include 32 KB of supervisory flash (SFlash) memory. SFlash is used to store device trim settings, secure key hashes, and FLASH_BOOT firmware. The device trim settings initialize hardware resources to ensure proper operation. Secure key hashes authenticate Infineon and OEM assets and images. SFlash is not available for storing user data.

4.5.3 ROM

All devices provide 64 KB of ROM, which stores boot and configuration routines as well as authentication checks. Following a reset event, the boot code in the supervisory ROM (SROM) evaluates the Reset Cause register to determine if the reset was triggered by a Hibernate event. If so, it ensures the fastest possible transition to executing user code, minimizing wake-up time from Hibernate mode. This process is quicker compared to a power-on reset (POR) or an external reset (XRES) event.

4.5.4 RAM

The device includes a total of 128 KB of SRAM, which is divided into two separate and independent SRAM blocks, each with a capacity of 64 KB, with support for memory retention during Deep Sleep power mode. The SRAM features ECC support for detecting and correcting soft errors.

4.6 eFuse

The device includes 1,024 one-time programmable (OTP) eFuse bits, reserved for system functions, such as device life-cycle management, trim settings, and hash values. These eFuse bits cannot be directly programmed by the user.

Each eFuse is individually programmed, and once programmed (or “blown”), its state becomes permanent and cannot be changed. Blowing a fuse changes its state from the default value of ‘0’ to ‘1’. To program an eFuse, the VDDIO0 voltage must be set to 2.5 V ±10%.

Since blowing an eFuse is an irreversible process, it is recommended that eFuse programming be performed only during mass production under controlled factory conditions using Infineon-provided provisioning tools.

4.7 Clock system

The device clock system provides clocks to all subsystems that require them and seamlessly switches between different clock sources without glitches. It also ensures that no metastable conditions occur during operation.

A clock supervision (CSV) circuit is implemented for each `clk_hf` domain. The CSV circuit monitors the clock and detects either a stopped clock or an abnormal frequency. It uses clock counters for both the monitored clock and the reference clock. Parameters for each counter define the reference clock's frequency and the upper and lower limits for the monitored clock's frequency.

If the dedicated frequency range comparator detects either a stopped clock or a clock outside the specified frequency range, it signals an abnormal state. Based on the register settings and the usage of the monitored clock on the device, the system responds by generating either a reset or an interrupt.

The device provides the following clock sources:

- **Internal oscillators**:
  - **Internal main oscillator (IMO)**: 8 MHz ±2%, fast wake-up, low jitter
  - **Internal high-speed oscillator (IHO)**: 48 MHz ±1%
  - **Internal low-speed oscillator (ILO)**: 32 kHz ±10%, also used as a wake-up source for the RTC
- **External crystal oscillators (ECO and WCO):**
  - **External crystal oscillator (ECO)**: 4 MHz to 35 MHz
  - **External watch crystal oscillator (WCO)**: 32.768 kHz
  - **External clock (EXTCLK)**: Maximum frequency 100 MHz
- **Frequency locked loop (FLL)**: Output range of 25 MHz to 100 MHz with ±1% accuracy
- **Two digital phase-locked loops (DPLL#0 and DPLL#1)**: Output range of 50 MHz to 200 MHz, used for the main CPU, PPCA, SCB, and TCPWM (outside the PPCA)

4.7.1 Internal main oscillator (IMO)

The internal main oscillator (IMO) operates at a fixed frequency of 8 MHz with a tolerance of ±2%. A high-speed clock can be generated by combining the IMO with a digital phase-locked loop (DPLL). The IMO features fast wake-up and low jitter, making it suitable for applications requiring quick response and precise timing.

4.7.2 Internal high-frequency oscillator (IHO)

The internal high-frequency oscillator (IHO) operates at a fixed frequency of 48 MHz with a tolerance of ±1%. A high-speed clock can be generated by combining the IHO with a DPLL.

4.7.3 Internal low-frequency oscillator (ILO)

The internal low-speed oscillator (ILO) is a low-power oscillator with a typical current consumption of 0.3 µA and a frequency of 32 kHz with ±10% accuracy. It can be used as a wake-up source for the real-time clock (RTC).

4.7.4 External crystal oscillator (ECO)

The external crystal oscillator (ECO) supports crystals with frequencies ranging from 4 MHz to 35 MHz for generating a high-precision clock. This option is suitable when the precision provided by internal oscillators is insufficient.

4.7.5 Watch crystal oscillator (WCO)

The watch crystal oscillator (WCO) uses an external 32.768 kHz crystal for applications requiring higher-precision real-time clock (RTC) functionality. The WCO clock can be routed directly to the RTC to achieve higher precision and avoid glitches caused by internal clock source switching.

4.7.6 Watchdog timer (WDT)

One watchdog timer (WDT) and one multi-counter watchdog timer (MCWDT) are provided. The WDT is implemented in the clock block and operates using either the ILO or the WCO. This enables watchdog functionality during Deep Sleep and can trigger a watchdog reset if it is not serviced before the timeout. The watchdog reset is logged in the Reset Cause register.

4.7.7 Real-time clock (RTC)

The device includes a real-time clock (RTC) with the following features:

- Operates in both 12-hour format with an AM/PM flag and 24-hour format
- Provides automatic leap year correction
- Includes an alarm feature that generates an interrupt, which can wake up the system from Sleep, Deep Sleep, and Hibernate power modes

4.8 Reset

The device can be reset from multiple sources, including a software reset. Reset events are asynchronous and ensure that the system reverts to a known state. The reset cause (WDT, MCWDT, faults, debug, software, and clock supervision) is recorded in a sticky register that retains its value through a reset, allowing the software to identify the cause of the reset. An XRES pin is also available for external reset.

4.9 Supply Voltage Glitch Sensor (SVGS)

The device includes a voltage glitch sensor designed to detect manipulations of the input voltage by an attacker attempting to disrupt the operation of the device.

The SVGS module provides the following functionality:

- VCCD overshoot monitor with a configurable threshold
- VCCD undershoot monitor with a configurable threshold, using a filtered VCCD signal
- VCCD noise monitor with a configurable threshold
- VDDQ undershoot monitor, detecting voltage levels below the brownout threshold

4.10 Low-power comparator (LPComp)

The device includes two low-power comparators capable of operating in all power modes. These comparators enable the monitoring of external voltage levels even in Deep Sleep and Hibernate modes, allowing other analog system resources to be disabled to conserve power.

The comparator outputs are typically synchronized to prevent metastability. However, in asynchronous power modes, such as Hibernate, the wakeup circuit is activated by a comparator-switch event.

4.11 Fixed function digital

4.11.1 Timer/counter pulse-width modulator (TCPWM)

The device includes a single TCPWM instance, located outside the PPCA, which is divided into two groups. The TCPWM inputs and outputs are exclusively connected to the EPU and TriggerMux.

- The first group is configured as a system timer for the main CPU. It features a 32-bit timer with two counters, clocked by a stable clock source. This setup provides a reliable and accurate timing signal for the main CPU and is used for system-level monitoring of the main CPU
- The second group is designed for PPCA CPU monitoring. It features a 16-bit timer with two counters, clocked by a robust clock source. This configuration enables reliable heartbeat monitoring of the PPCA CPUs

4.11.2 Serial communication block (SCB)

The device includes up to seven SCB modules that can be software-configured to operate as I^2C, UART, or SPI interfaces in either master or slave mode during Active mode. One SCB module can function in Deep Sleep mode using an external clock, limited to I^2C slave or SPI slave operation. Each SCB module features a 256-byte-deep FIFO for efficient data handling and supports DMA transfers. Additionally, one SCB instance with PMBus extensions enables wakeup from Deep Sleep, while another supports fast SPI communication with data rates up to 50 MHz. The fast SPI instance does not support Deep Sleep wakeup.

4.11.2.1 Inter-integrated circuit (I^2C)

The hardware I^2C block implements a full multi-master and multi-slave interface, with support for multi-master arbitration. It operates at speeds of up to 1 Mbps (Fast Mode Plus) and provides flexible buffering options, reducing interrupt overhead and CPU latency.

This block also supports EZI2C functionality, which allows the creation of a mailbox address range in the device memory. This feature reduces I^2C communication overheads when reading from or writing to an array in memory. Additionally, the integrated FIFO minimizes the need for clock stretching, ensuring efficient operation by preventing delays caused by the CPU not reading data on time.

Furthermore, the I^2C instances in this device also support the PMBus protocol with the following features:

- Communication at baud rates up to 1 Mbps
- Timeout event generation
- A minimum of five slave address masks for hardware address screening
- De-glitching of SMBCLK and SMBDAT signals to ensure noise-immune communication

4.11.2.2 Universal Asynchronous Transmitter Receiver (UART)

The full-feature UART operates at speeds of up to 8 Mbps and supports multiple communication protocols, including LIN (automotive single-wire interface), IrDA (infrared interface), and SmartCard (ISO7816). It also supports a 9-bit multiprocessor mode, enabling the addressing of peripherals connected over shared RX and TX lines.

Key UART features include:

- Hardware flow control
- Parity
- Break detection
- Frame error detection

Additionally, the SCB can be configured in half-duplex UART mode, enabling single-wire communication.

4.11.2.3 Serial peripheral interface (SPI)

The SPI mode supports multiple protocols, including:

- **Motorola SPI**: Standard full-duplex communication
- **Texas Instruments Synchronous Serial Port (SSP)**: Adds a start pulse for synchronizing SPI codecs
- **National Semiconductor Microwire**: A half-duplex variant of SPI

The SPI block also includes an EZ-SPI mode, which simplifies data interchange by mapping it to reading from and writing to an array in memory. Additionally, the fast SPI mode supports both master and slave functionalities at speeds of up to 50 MHz.

4.11.3 Controller Area Network Flexible Data-Rate (CAN FD)

The CAN FD module features two channels, each with timestamp support and a 4-KB message RAM. It supports data transmission rates of up to 8 Mbps, enabling high-speed communication.

4.12 Trigger multiplexer (TriggerMux)

The Trigger MUX, located outside of the PPCA, facilitates the connection of trigger and input/output signals between various peripherals. It enables communication and signal routing among components such as DMA (for example, SCB to DMA or PPCA to DMA), TCPWM, PPCA, CPUSS, and GPIO pins.

4.13 Coordinate Rotation Digital Computer (CORDIC)

The CORDIC module is designed for precise computations of transforms required in motor speed and position estimation, as well as reference plane transforms commonly used in field-oriented control (FOC). By calculating trigonometric functions directly in hardware, it offloads computational tasks from the main CPU, improving system efficiency.

Supported algorithms include:

- Sine and cosine
- Arctangent (arctan)
- Hyperbolic sine (sinh) and hyperbolic cosine (cosh)
- Hyperbolic arctangent (arctanh)
- Phase computation
- Square root (sqrt)
- Park transform

4.14 General-purpose input/output (GPIO) ports

PSOC™ Control C3 (P/M) (7/8) provides up to 10 logical GPIO ports (60 GPIO pads) with two pad-power-supply domains. Two of the GPIOs are multiplexed with analog inputs, allowing for a maximum of 26 dedicated analog input connections. Additionally, 14 auxiliary analog inputs GPIOs can be connected to one of the ADC channels through multiplexers. The GPIO block includes the following features:

- Eight drive modes, including:
  - Strong push-pull
  - Resistive pull-up and pull-down
  - Open-drain and open-source
  - Input-only
  - Disabled
- Input threshold selection (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching the previous state, which retains the I/O state during Deep Sleep and Hibernate modes
- Selectable slew rates for dV/dt-related noise control
- Supports two PMBus signal outputs on overvoltage tolerant (OVT) GPIOs

The GPIO pins are organized into logical entities called "ports." During power-on and reset, all GPIO blocks are forced into a disabled state to prevent crowbarring inputs or causing excess turn-on current. A multiplexing network, known as the "high-speed I/O matrix" (HSIOM), is used to connect various signals to each I/O pin.

The data output and pin state registers store values to be driven on the pins and monitor the state of the pins. Each I/O pin can generate interrupts when enabled, with each I/O port having an associated interrupt request (IRQ) and interrupt service routine (ISR) vector.

The I/O ports retain their state during Hibernate mode.

- If restored using a reset, the pins will transition to the High-Z state
- If restored using the wakeup pin, the pin drivers will retain their previously frozen state until the firmware modifies them

For simultaneous output switching in high-current mode, proper line termination and appropriate decoupling capacitor sizing are required to control switching transient voltages.

Overvoltage-tolerant (OVT) pins use an alternate design without clamping diodes connected to supply lines, which limit leakage current when the corresponding VDDIO voltage is lower than the external voltage applied to the pin, such as when the device is powered down (VDDIO = 0 V) while connected to an active bus. These pins are recommended for PMBus or SMBus interfaces. They do not support operation with external logic voltages that exceed the pin input/output voltage range specifications.

4.15 Device Firmware Update (DFU)

The immutable BootROM includes a built-in DFU protocol that enables secure and reliable firmware upgrades through a serial interface. By default, DFU functionality is disabled and must be explicitly enabled in the OEM policy. The device must also be provisioned before DFU can be used. For more details, contact Infineon Support.

DFU mode is selected during device boot-up based on the state of the *P8.2* pins, as described in Table 3. When the device enters DFU mode, pins *P8.1* and *P8.2* function as the serial communication interface. Use pull-up or pull-down resistors of 1 kΩ or less connected to VDDIO_1 or VSS to set the DFU select pin (*P8.2*) to logic high or low. For a High-Z state, the DFU select pin (*P8.2*) can be left floating.

Table 3 DFU mode and serial communication pins

Pin	UART
P8.0	UART - Rx
P8.1	UART - Tx
P8.2	DFU enable (VSS)/DFU disable (VDDIO_1/High-Z)

The following parameters are used for DFU-UART communication:

UART configuration:

1. **Baud rate**: 115200
2. **Data bits**: 8
3. **Stop bits**: 1
4. **RTS/CTS**: No
5. **Parity**: None

4.16 Serial Wire JTAG Debug Port (SWJ-DP)

The PSOC™ Control C3 (P/M) (7/8) MCU incorporates the Arm® Serial Wire JTAG Debug Port (SWJ-DP), which supports both the 2-wire SWD interface and the 4-wire or 5-wire Joint Test Action Group (JTAG) interface.

By default, the SWD interface is enabled after power-on, while the JTAG interface remains disabled. The JTAG interface can be activated in either 4-wire or 5-wire mode by modifying the OEM policy. For further information on enabling JTAG, contact Infineon Support.

4.17 Embedded Trace Macrocell (ETM)

The Arm® Embedded Trace Macrocell (ETM) is supported by the PSOC™ Control C3 (P/M) (8/7) MCU. It enables the reconstruction of program execution by transmitting high-speed compressed data through the ETM pins.

The ETM interface includes:

- One clock pin (trace.clock)
- Up to four data pins (trace.data0 to trace.data3)

4.18 Programmable power control accelerator (PPCA)

The device features a programmable power subsystem that facilitates the implementation of high-performance switched-mode power supply control algorithms. It supports the implementation of at least two independent control loops, with the capability to share information and data between the loops, enabling support for different power topologies.

The programmable power control accelerator (PPCA) block provides the necessary computational capability and includes a range of peripherals, such as:

- High-resolution timer/counter PWM
- 3-pole/3-zero hardware filters
- Event processing unit modules
- CORDIC accelerator
- ADCs including ADC filters, and analog front end (AFE)
- Comparators
- Differential comparator and slope generator
- Voltage and current references
- Custom logic block

PPCA peripherals are not available in Deep Sleep or Hibernate modes. In Deep Sleep (-RAM, -OFF) mode, only SRAMs remain accessible.

4.18.1 PPCA CPU subsystem

The PPCA CPU subsystem hosts two Cortex®-M33 CPUs (CPU0 and CPU1). Each CPU includes an interrupt controller and supports DSP and FPU extensions. Each processor also features an AHB slave access port, which is used for debug and trace operations.

The CPUs can operate at a maximum frequency of 200 MHz in Overdrive (OD) mode.

The bus matrix provides the following AHB interfaces:

- **AHB slave interfaces:**
  - CPU0, CPU1, and external AHB master (main subsystem)
- **AHB master interfaces:**
  - Local, shared memories, IPC, PPCA CPUs, SRAMs, and CPUSS configuration

4.18.2 PPCA RAM

The PPCA subsystem includes a total of 112 KB of SRAM, with support for memory retention during Deep Sleep power mode. The SRAM features ECC support for detecting and correcting soft errors.

- 32 KB of SRAM for program memory for each CPU
- 16 KB of SRAM for data memory for each CPU
- 16 KB of shared SRAM, configurable as a data memory extension for either CPU during runtime

4.18.3 PPCA ATOP subsystem

4.18.3.1 12-bit 25 Msps SAR ADC converter

The device features four blocks of 12-bit SAR ADCs, capable of synchronized sampling across multiple Sample-and-Hold (S/H) circuits. The ADC subsystem offers the following features:

Two ADCs (ADC0 and ADC3) support up to eight differential or 16 single-ended input channels, feature an analog front end with configurable gain. The available gain options are 8.25, 16.5, 33, and 66. Each of these ADCs can be connected with up to eight additional analog inputs to one of the channels through the analog multiplexers.

The other two ADCs (ADC1 and ADC2) support up to four differential or eight single-ended input channels each. Both include an analog front end with programmable gain on at least one differential channel, offering the same gain options: 8.25, 16.5, 33, and 66.

The analog inputs can be configured as either differential or single-ended, with a combined total of up to 40 analog inputs across all ADCs. It features manual, auto, and arbitrary triggering modes for a single channel and a programmable group of channels conversion. This flexibility allows a wide range of input configurations, enabling versatile system design.

The module also incorporates ADC filters (ADC FILTs) comprising a median filter, a linear interpolation and extrapolation filter, a low pass filter, a cascade integrator third order comb filter, and a programmable average filter with the capability of detecting the minimum and maximum values of the input data stream. These filters can be cascaded in a user-defined sequence, allowing for flexible signal processing. The filter chain can be optionally sourced by the output of another ADC core, enabling further customization.

Performance features:

- **Sampling rate**: The ADCs provide an effective sampling rate ranging from 250 ksps to 25,000 ksps, with a maximum conversion rate of 25 Msps during synchronous sampling
- **Oversampling**: The ADCs support up to 64x oversampling with hardware averaging, improving resolution up to 3-bits. This ensures higher accuracy and resolution for specific applications

Reference and power supply options:

- The ADCs can operate using either an internal 1.2 V reference or an external 1.2 V reference, providing flexibility in system design and configuration
- The ADCs operate within an analog supply range defined by VDDA, accommodating a wide range of power supply options

4.18.3.2 Differential comparator and slope generator (DCSG)

The device incorporates nine DCSG blocks, each equipped with a user-configurable 12-bit DAC. The comparator outputs are fast-synchronized to avoid metastability, ensuring reliable and accurate comparisons.

The DCSG supports a wide range of input voltages, including ±200 mV for current monitoring and 0 to 3.3 V for voltage monitoring. The inputs are shared with ADC inputs, enabling simultaneous measurement of the same voltage or current by both the ADC and comparator. This feature leverages the faster response time of the comparator for tasks such as overvoltage and overcurrent protection or current mode control.

The in-built DAC operates on an internal or external 1.2 V reference and supports the specified voltage range. It has a refresh time of at least 50 µs, ensuring the programmed threshold remains constant without degradation of parameters. The DAC can be refreshed at a deterministic point in time, and an auto-refresh mechanism ensures reliable operation.

During DAC refreshing, the DCSG output is blanked for a maximum duration of 50 ns. A defined output state can be selected for the DAC during blanking. Additionally, the device enables seamless monitoring of analog inputs by other DCSGs while one DCSG is blanking, ensuring uninterrupted application performance.

The device supports multiple DCSG configurations, including monitoring analog inputs measured by the ADC with up to three different DCSGs. At least three slope generator functionalities are available on three separate DCSGs. The DCSG outputs are routed to the EPU, which distributes them to embedded peripherals. This allows the DCSG outputs to be used as inputs for controlling various functions, such as disabling the PWM signal in case of overvoltage or overcurrent detection, or serving as ADC trigger inputs.

4.18.3.3 12-bit R2R DAC and buffer

The device features two 12-bit resolution DACs with output buffers. These DACs support a maximum update rate of 2 Msps and have a settling time of 500 ns.

The output buffer at the DAC supports an input and output voltage range of 0.1 V to 1.2 V when operating with a 1.2 V reference. When a VDDA/2 reference is used, the voltage range extends from 0.1 V to VDDA/2.

Additionally, the device includes a provision to route the R2R DAC outputs to the DCSG inputs, enabling seamless integration between the DAC and DCSG functionality.

4.18.3.4 Current DAC (IDAC)

The device includes a single instance of a programmable current source, referred to as the Current DAC (IDAC), which generates a current output.

The IDAC enables measurement of externally connected resistances by passing a fixed current through the resistor. This is accomplished by sourcing a known current through the external resistor and measuring the resulting voltage drop using the on-chip ADC.

In addition, the IDAC facilitates the measurement of the pull-down-to-ground resistor in the PMBUS for SMBUS addressing. This is performed by passing a fixed current through the resistor and measuring the corresponding voltage drop using the on-chip ADC.

The IDAC also offers functionality to detect floating conditions on all analog-only input pins. This is achieved by sourcing a small current through each input pin and measuring the resulting voltage drop with the on-chip ADC.

4.18.3.5 General-purpose input (GPI)

The GPI module is a digital comparator that converts an analog input into a digital output by comparing the input against two fixed thresholds: 0.3 VDDA and 0.7 VDDA. Analog inputs from AIN0 and AIN1 are compared to these thresholds, and the resulting comparison generates a corresponding digital output.

4.18.3.6 Temperature sensor (TSNS)

The device integrates a temperature sensor capable of measuring temperature with an output precision of ±5°C. The output of the sensor is accessed through the ADC via the AMUX. Calibration and trimming are performed once, ensuring accurate temperature measurements. This process does not interfere with ADC operation during runtime.

4.18.4 PPCA - Event Processing Unit (EPU)

The device includes an Event Processing Unit (EPU), which provides a flexible event management system capable of generating triggers based on a linear combination of processed input events. The EPU receives input events from peripherals within the PPCA and the TriggerMux outside the PPCA and generates output triggers that are routed to peripherals inside the PPCA and the TriggerMux.

The EPU enables routing input triggers as interrupts to the PPCA CPUs and processing and routing input triggers as interrupts to the main CPU. Additionally, it can process and route input triggers as triggers to peripherals outside the PPCA, such as the DW and SCB. This functionality ensures efficient and effective event processing across the entire system.

The primary purpose of the EPU is to create a hardware sequence of processed, timed triggers that enable the operation of PPCA subsystem modules. This offloads the instantiated processors and accelerates system operations. The EPU also sends interrupts to PPCA CPU0 and CPU1, as well as to the boundary of the PPCA, allowing triggers to be shared within and outside the PPCA.

The EPU supports 32 Processing Unit Type_1 (PU_T1) modules and 16 Processing Unit Type_2 (PU_T2) modules. These modules connect selected inputs, generated by PPCA resources (CPUs and peripherals), to outputs connected to triggers of PPCA resources (CPUs and peripherals).

The features of the EPU-PU_T1 modules include:

- Asynchronous and synchronous bypass
- Masking filter (up to 128 clock cycles)
- Blanking filter (up to 128 clock cycles)
- Debouncing filter through integration (up to 128 clock cycles)
- Pulse delay (up to 128 clock cycles)
- Input polarity inversion
- Rising-edge extraction

The features of the EPU-PU_T2 modules include:

- Asynchronous and synchronous bypass
- Input polarity inversion
- Rising-edge extraction

The EPU supports a total of 256 event input signals from peripherals and 123 event trigger output signals to peripherals. The EPU interrupt generator module (EPU_IRQ) includes a group of multiplexers that select up to eight COMBO output signals (EVOUT).

4.18.5 PPCA - Custom Logic Block (CLB)

The Custom Logic Block (CLB) module provides dedicated hardware support for specific functions or control algorithms that require very high computational resources. Examples include the digital observer used in the Totem-Pole PFC controller or the matrix converter commutation. A typical application of the CLB is the implementation of a Totem-Pole PFC controller based on a digital current observer, which enables operation at higher switching frequencies.

The CLB supports the following functions:

- Digital current observer
- Matrix converter commutation logic
- Trajectory control and spread-pulse startup

The CLB also manages kill events, mask events, and debug state scenarios. It processes data from ADCs and generates output signals shared with PWMs. This allows the CLB to process ADC data and produce PWM outputs based on the results.

For example, the digital current observer function estimates and observes three-phase currents in Totem-Pole PFC topologies. It receives current measurements filtered by on-chip ADCs and post-processing filters and generates PWM outputs in hysteretic control mode based on the results from the observer.

The matrix commutation logic function includes the following features:

- Support for three-phase converters with six bidirectional switches
- Commutation of a maximum of 20 different states with programmable hold-time
- Redundant storage to enable shadow updates while commutation is in progress

4.18.6 PPCA - Hardware filter (HW filter 3P3Z)

The PPCA provides two independent instances of a configurable hardware filter (HW Filter 3P3Z). Each instance can be allocated to the PPCA CPUs.

- The first instance integrates one hardware filter 3P3Z, configured to support four 3Poles-3Zeroes hardware filters
- The second instance integrates one hardware filter 3P3Z, configured to support two 3Poles-3Zeroes hardware filters

The hardware 3P3Z module features:

- 16-bit input format (q0.15)
- 24-bit output format (q0.23)
- 24-bit coefficients format (q0.23)
- 48-bit multiplier
- 58-bit internal accumulator
- 2-bit gain input
- 3-bit attenuator output

Additional features include support for saturation and rounding operators, arithmetic two's complement processing, and a maximum execution latency of eight CPU clock cycles.

4.18.7 PPCA - Timer/counter pulse-width modulator (TCPWM)

The PPCA-TCPWM module includes four independent TCPWM instances, each equipped with its own AHB slave interface, enabling flexible allocation to either PPCA CPU.

- The first TCPWM instance consists of three groups:
  - One group with four high-resolution 32-bit TCPWMs with data-path inputs
  - One group with four high-resolution 32-bit TCPWMs
  - One group with four CPU clock-resolution 16-bit TCPWMs and a MOTIF interface
- The second TCPWM instance also consists of three groups:
  - One group with two high-resolution 32-bit TCPWMs with data-path inputs
  - One group with two high-resolution 32-bit TCPWMs
  - One group with four CPU clock-resolution 16-bit TCPWMs and a MOTIF interface
- The third TCPWM instance contains a single group with four CPU clock-resolution 16-bit TCPWMs
- The fourth TCPWM instance contains a single group with two CPU clock-resolution 16-bit TCPWM

The High-Resolution PWM (HRPWM) module, integrated with the TCPWM and an analog interpolator, provides advanced functionality, including:

- Configurable 32-bit counters with <100 ps resolution for duty cycle, dead time, and period
- Complementary output with programmable dead time, independent outputs, and push-pull outputs
- Support for single-slope, increment-and-decrement, and dual-slope configurations
- Synchronization input signal for synchronizing all PWM modules
- Kill function and optional hardware duty generation linked to the PWM counter slope
- Masking line output based on the received mask input signal
- Shadow and non-shadow update registers, capture compare feature, and AHB slave interface
- Register slave interface connected to the hardware filter (HW 3P3Z) output

4.18.8 PPCA - Coordinate Rotation Digital Computer (CORDIC)

The PPCA includes two CORDIC modules, which are used for precise computations required in motor speed and position estimation, as well as reference plane transforms commonly employed in field-oriented control (FOC). These modules calculate trigonometric functions directly in hardware, thereby offloading processing tasks from the main CPU.

The CORDIC modules support the following algorithms:

- Sine and cosine
- Arctangent (arctan)
- Hyperbolic sine (sinh) and hyperbolic cosine (cosh)
- Hyperbolic arctangent (arctanh)
- Phase computation
- Square root (sqrt)
- Park transform

5 Pins

GPIO ports and analog inputs are powered by the following VDDx pins:

- **P0**: VBACKUP
- **P1, P2, P3, P4, P5, P6**: VDDIO_0
- **P7, P8, P9**: VDDIO_1
- **AIN_N, AIN_P**: AVDD

The number of available GPIOs is limited in some packages. For detailed information on supported packages, see Package information.

Table 4 Packages and pin information

Pin	Capability	Packages			
		E-LQFP-100	E-LQFP-80	E-LQFP-64/ VQFN-64	VQFN-48
VDDD	-	17	14	12	10
VDDD	-	18	15	-	-
VDDA	-	84	70	57	41
VDDIO_0_0	-	26	22	17	13
VDDIO_0_1	-	39	33	27	-
VDDIO_0_2	-	50	40	32	24
VDDIO_0_3	-	59	45	-	-
VDDIO_1_0	-	5	2	3	3
VDDIO_1_1	-	100	79	64	48
VCCD	-	15	12	11	9
VCCD	-	16	13	-	-
VSSD	-	GND PAD	GND PAD	GND PAD	GND PAD
VAREF_EXT	-	85	71	58	42
VBACKUP	-	19	-	-	-
AIN0	AM	72	58	45	35
AIN0N	AD, DCSG	67	53	40	30
AIN0P	AD, DCSG	66	52	39	29
AIN1	AM	73	59	46	36
AIN10N	AD, DCSG	91	-	-	-
AIN10P	AD, DCSG	90	-	-	-
AIN11N	AD, DCSG	93	-	-	-
AIN11P	AD, DCSG	92	-	-	-
AIN1N	AD, DCSG	69	55	42	32
AIN1P	AD, DCSG	68	54	41	31
AIN2N	AD, DCSG	71	57	44	34
AIN2P	AD, DCSG	70	56	43	33
AIN3N	AD, DCSG	75	61	48	-

(table continues...)

Table 4 (continued) Packages and pin information

Pin	Capability	Packages			
		E-LQFP-100	E-LQFP-80	E-LQFP-64/ VQFN-64	VQFN-48
AIN3P	AD, DCSG	74	60	47	-
AIN4N	AD, DCSG	77	63	50	38
AIN4P	AD, DCSG	76	62	49	37
AIN5N	AD, DCSG	79	65	52	-
AIN5P	AD, DCSG	78	64	51	-
AIN6N	AD, DCSG	81	67	54	40
AIN6P	AD, DCSG	80	66	53	39
AIN7N	AD, DCSG	83	69	56	-
AIN7P	AD, DCSG	82	68	55	-
AIN8N	AD, DCSG	87	73	60	44
AIN8P	AD, DCSG	86	72	59	43
AIN9N	AD, DCSG	89	75	-	-
AIN9P	AD, DCSG	88	74	-	-
XRES	-	14	11	10	8
P0.0	-	20	16	-	-
P0.1	-	21	17	-	-
P1.0	-	22	18	13[1)]	-
P1.1	-	23	19	14	-
P1.2	-	24	20	15	11
P1.3	-	25	21	16	12
P1.4	-	27	23	-	-
P1.5	-	28	24	18	-
P1.6	-	29	25	19	-
P1.7	-	30	26	20	-
P2.0	OVT	31	27	21	14
P2.1	OVT, HIB	32	28	22	15
P2.2	OVT	33	29	23	16
P2.3	OVT	34	30	24	17
P2.4	OVT	35	31	25	18
P2.5	OVT	36	32	26	19
P3.0	-	37	-	-	-
P3.1	-	38	-	-	-
P3.2	-	40	-	-	-
P3.3	-	41	-	-	-

(table continues...)

Table 4 (continued) Packages and pin information

Pin	Capability	Packages			
		E-LQFP-100	E-LQFP-80	E-LQFP-64/ VQFN-64	VQFN-48
P3.4	-	42	-	-	-
P3.5	-	43	34	-	-
P3.6	-	44	35	-	-
P3.7	-	45	-	-	-
P4.0	-	46	36	28	20
P4.1	-	47	37	29	21
P4.2	-	48	38	30	22
P4.3	-	49	39	31	23
P4.4	-	51	-	-	-
P4.5	-	52	-	-	-
P4.6	-	53	-	-	-
P4.7	-	54	-	-	-
P5.0	-	55	41	-	-
P5.1	-	56	42	-	-
P5.2	-	57	43	-	-
P5.3	AM	58	44	-	-
P6.0	AM	60	46	33	-
P6.1	AM	61	47	34	-
P6.2	AC, AM	62	48	35	25
P6.3	AC, AM	63	49	36	26
P6.4	AC, AM	64	50	37	27
P6.5	AC, AM	65	51	38	28
P7.0	HIB, AM	94	76	61	45
P7.1	AM	95	77	62	46
P7.2	AM	96	78	63	47
P7.3	AM	97	-	-	-
P7.4	AM	98	-	-	-
P7.5	AM	99	-	-	-
P7.6	AM	1	-	-	-
P7.7	-	2	-	-	-
P8.0	-	3	80	1	1
P8.1	-	4	1	2	2
P8.2	-	6	3	4	4
P8.3	-	7	4	5	5

(table continues...)

Table 4 (continued) Packages and pin information

Pin	Capability	Packages			
		E-LQFP-100	E-LQFP-80	E-LQFP-64/ VQFN-64	VQFN-48
P8.4	-	8	5	6	6
P8.5	-	9	6	7	7
P9.0	-	10	7	8	-
P9.1	-	11	8	9	-
P9.2	-	12	9	-	-
P9.3	-	13	10	-	-

1) This pin is designated as VDDD for the E-LQFP-64 package.

Table 5 Pin capability abbreviations

Abbreviation	Capability
AD	Dedicated analog pin directly connected to the sampler
AM	Dedicated analog pin/analog capable GPIO pin connected to the sampler through MUX
DCSG	Dedicated analog pin that can be connected to the comparator slope generator input
AC	Analog capable GPIO pin (LPComp input)
OVT	Overvoltage tolerant GPIO
HIB	Hibernate wake-up capable pin

***Note**: All GPIO pins are PWM capable. Any TCPWM channel line or line_compl output can be routed to any GPIO pin.*

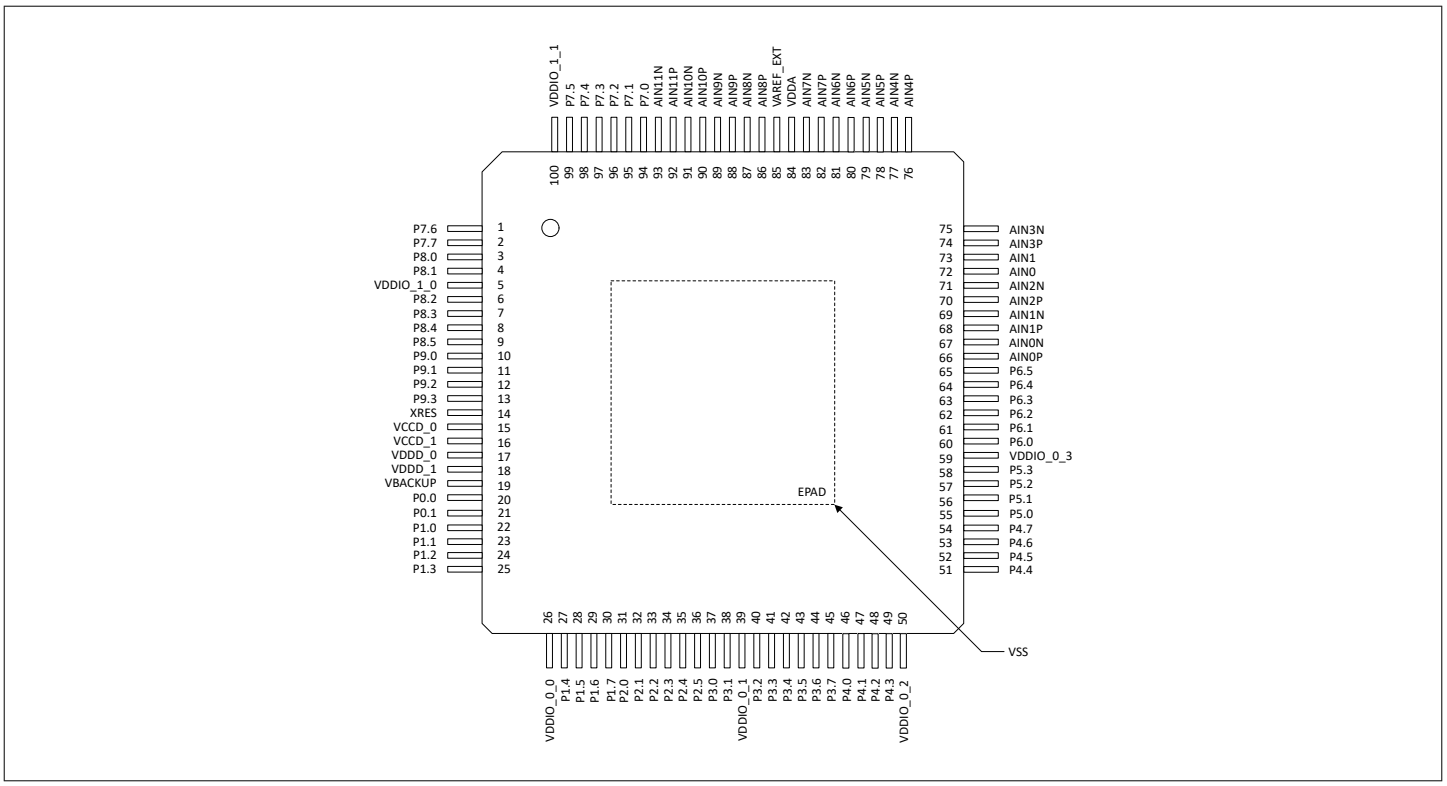


Figure 8 Device pinout for E-LQFP-100 package (top view)

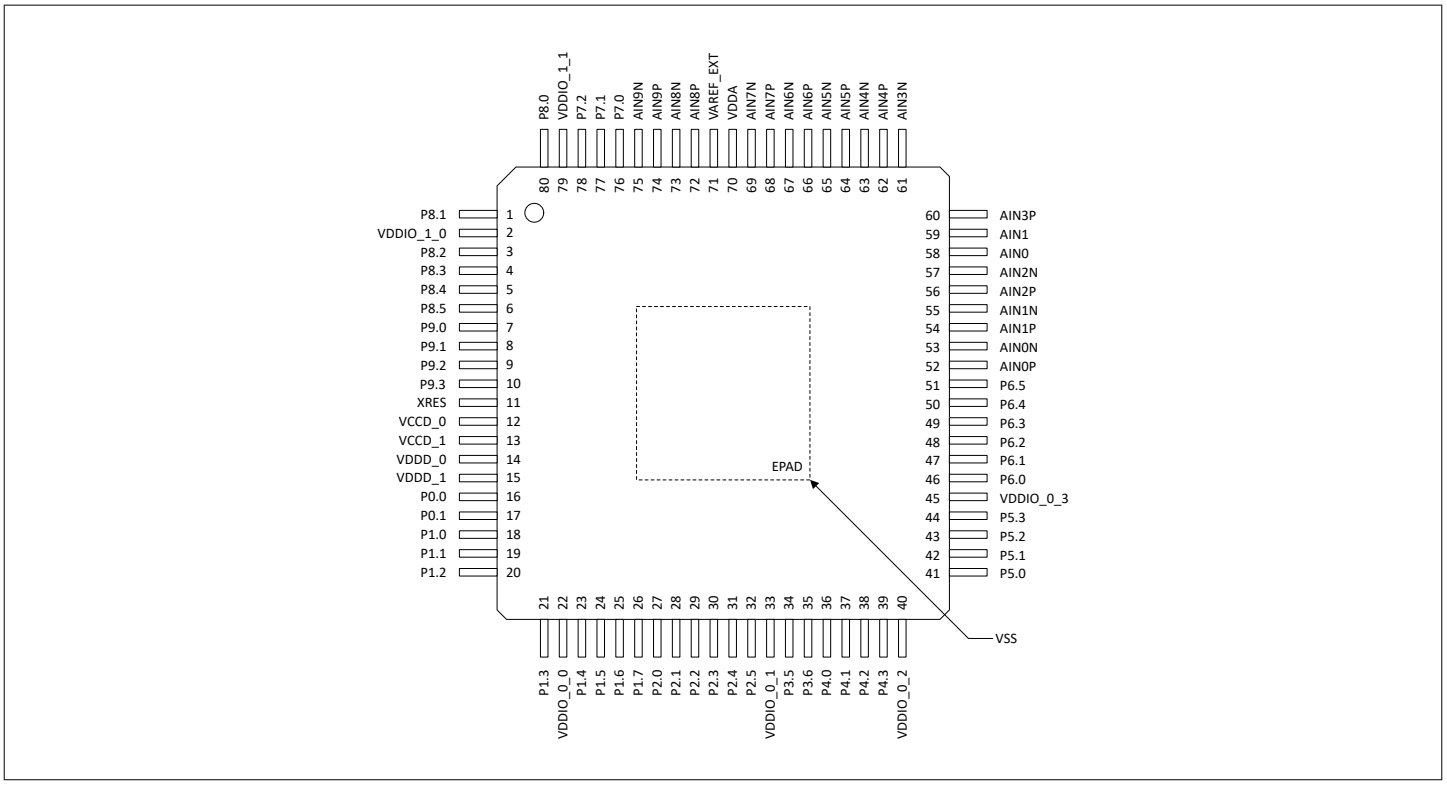


Figure 9 Device pinout for E-LQFP-80 package (top view)

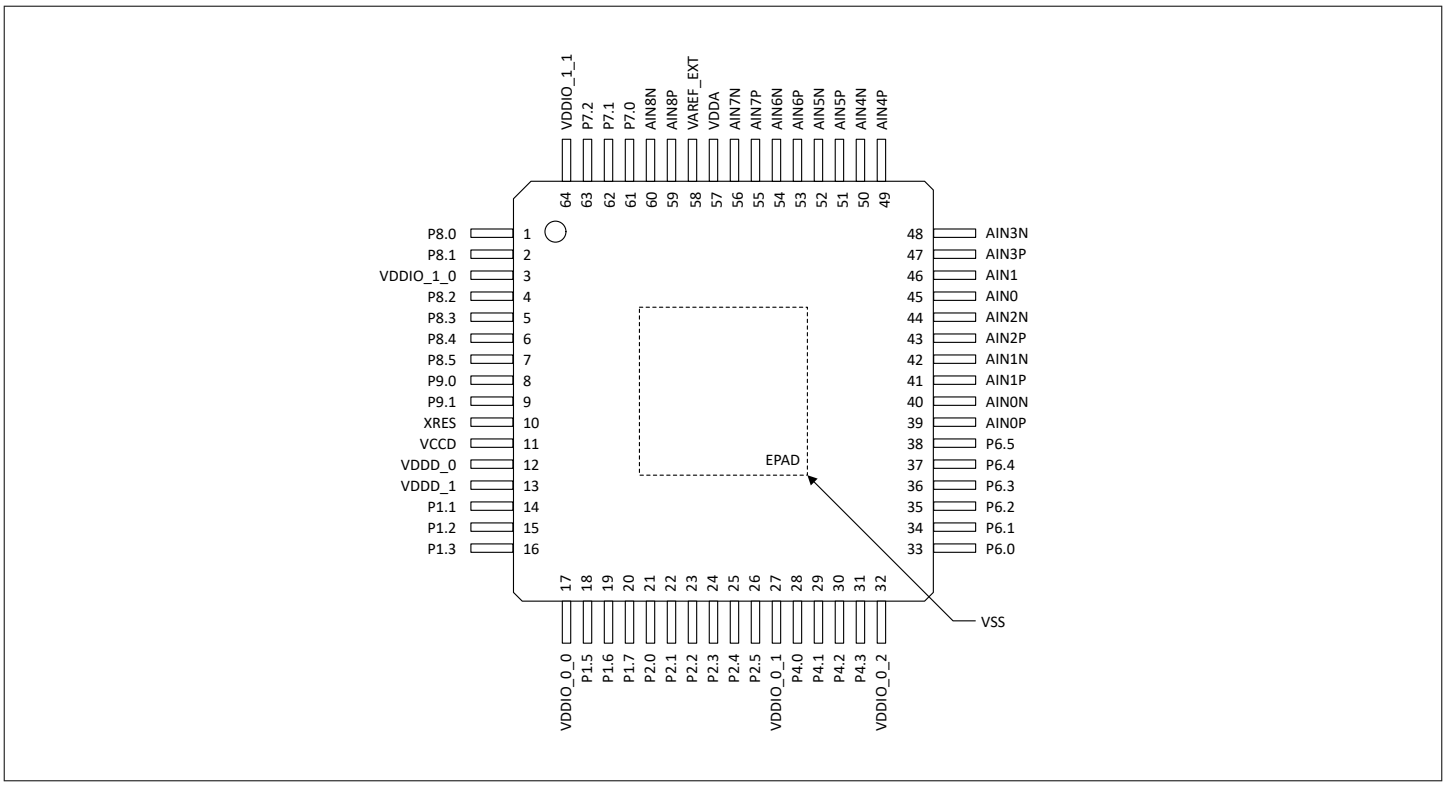


Figure 10 Device pinout for E-LQFP-64 package (top view)

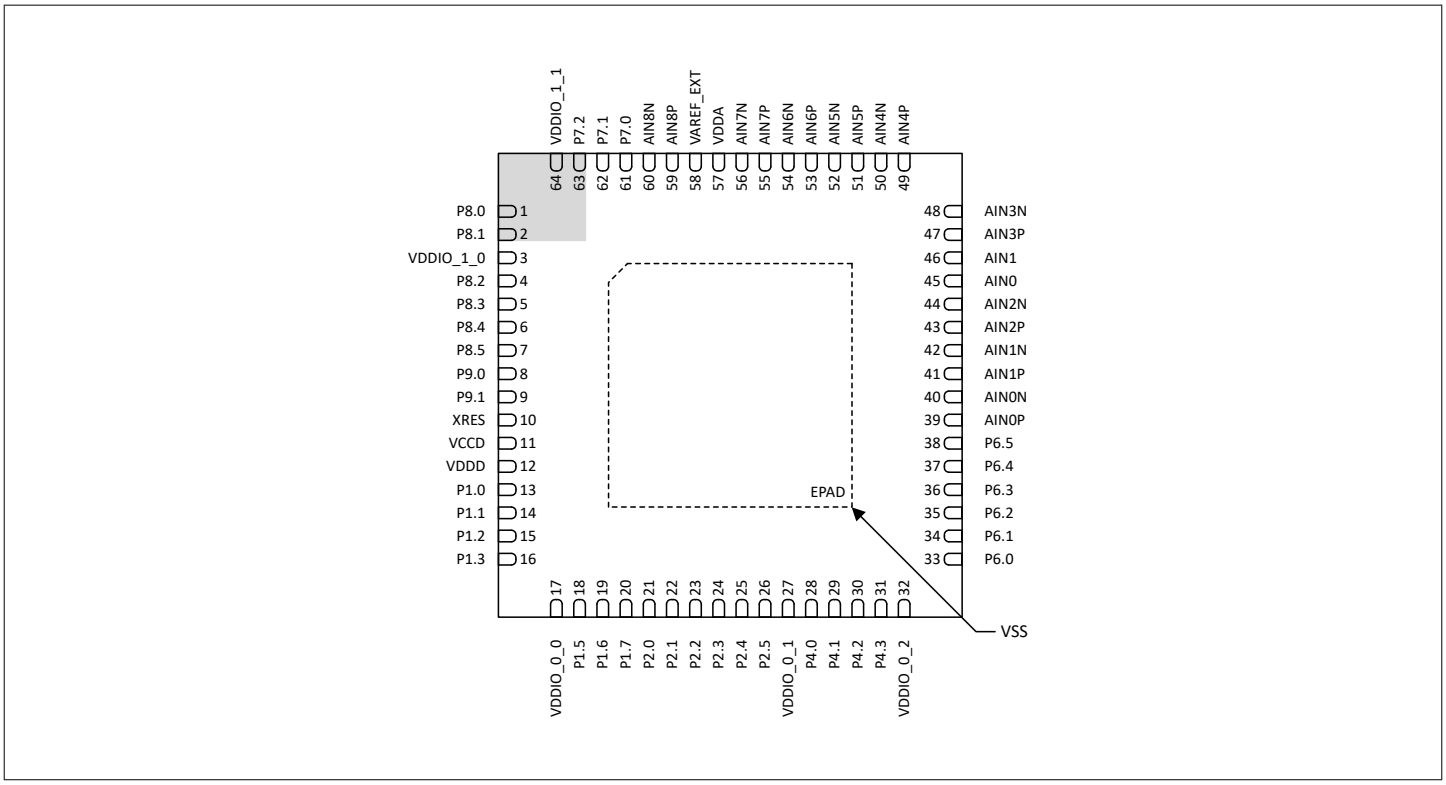


Figure 11 Device pinout for VQFN-64 package (top view)

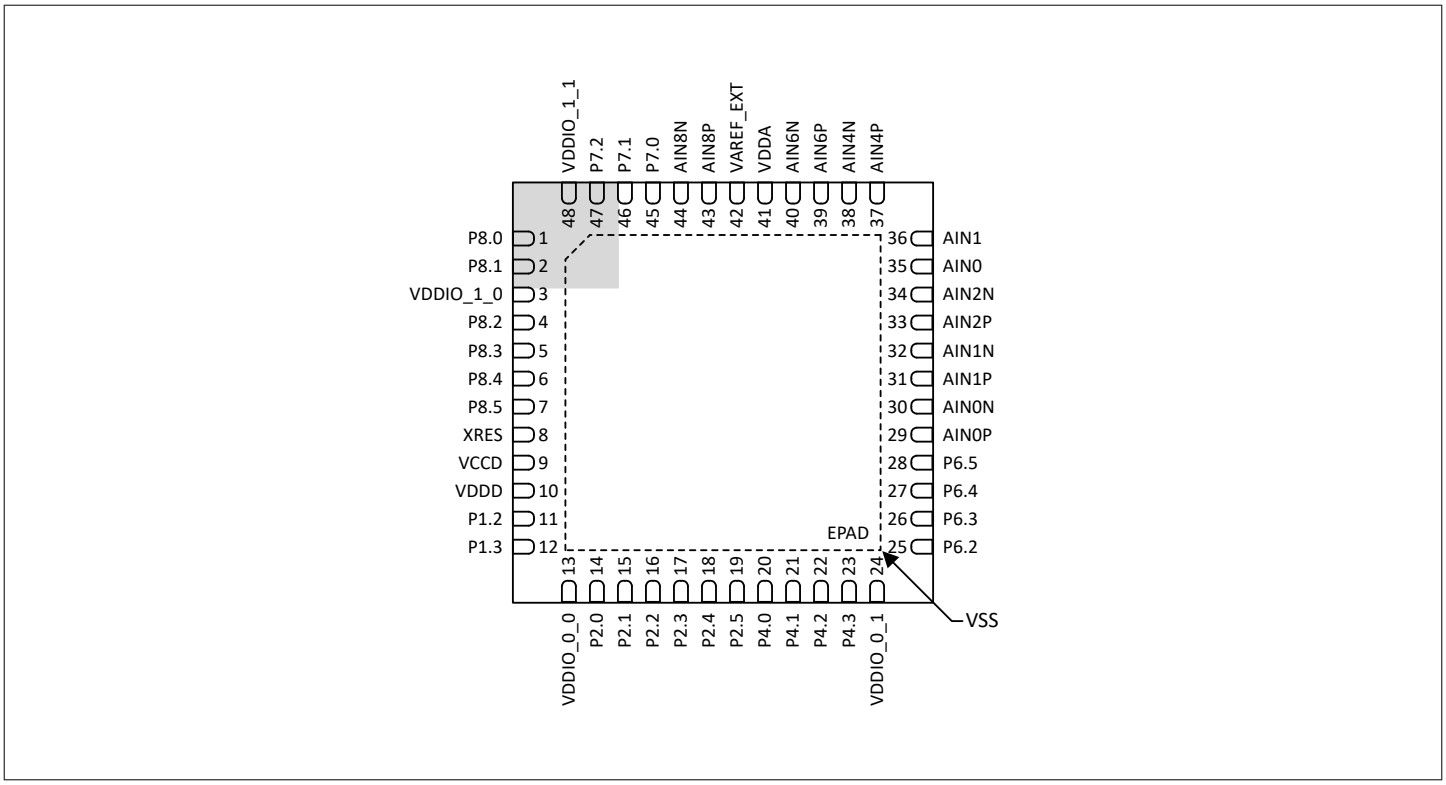


Figure 12 Device pinout for VQFN-48 package (top view)

6 GPIO alternate functions

Table 6 GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
P0.0	wco_out	fixed	ppca.ppcaio[54]:0	ACT #0
	peri.tr_io_input[0]:0	ACT #13	peri.tr_io_output[0]:0	ACT #14
	peri.tr_io_output[60]:0	ACT #15		
P0.1	wco_in	fixed	ppca.ppcaio[55]:0	ACT #0
	peri.tr_io_input[1]:0	ACT #13	peri.tr_io_output[1]:0	ACT #14
	peri.tr_io_output[61]:0	ACT #15		
P1.0	eco_in	fixed	ppca.ppcaio[56]:0	ACT #0
	peri.tr_io_input[2]:0	ACT #13	peri.tr_io_output[2]:0	ACT #14
	peri.tr_io_output[62]:0	ACT #15		
P1.1	eco_out	fixed	ppca.ppcaio[57]:0	ACT #0
	peri.tr_io_input[3]:0	ACT #13	peri.tr_io_output[3]:0	ACT #14
	peri.tr_io_output[63]:0	ACT #15		
P1.2	ppca.ppcaio[58]:0	ACT #0	tcpwm0.g0.cnt0+	ACT #10
	peri.tr_io_input[4]:0	ACT #13	peri.tr_io_output[4]:0	ACT #14
	peri.tr_io_output[64]:0	ACT #15	swj.swclk/tclk	DS #5
P1.3	ppca.ppcaio[59]:0	ACT #0	tcpwm0.g0.cnt0-	ACT #10
	peri.tr_io_input[5]:0	ACT #13	peri.tr_io_output[5]:0	ACT #14
	peri.tr_io_output[65]:0	ACT #15	swj.swdio/tms	DS #5
P1.4	ppca.ppcaio[10]:0	ACT #0	peri.tr_io_input[6]:0	ACT #13
	peri.tr_io_output[6]:0	ACT #14	peri.tr_io_output[66]:0	ACT #15
P1.5	ppca.ppcaio[11]:0	ACT #0	peri.tr_io_input[7]:0	ACT #13
	peri.tr_io_output[7]:0	ACT #14	peri.tr_io_output[67]:0	ACT #15
P1.6	ppca.ppcaio[12]:0	ACT #0	peri.tr_io_input[8]:0	ACT #13
	peri.tr_io_output[8]:0	ACT #14	peri.tr_io_output[68]:0	ACT #15
P1.7	ppca.ppcaio[13]:0	ACT #0	peri.tr_io_input[9]:0	ACT #13
	peri.tr_io_output[9]:0	ACT #14	peri.tr_io_output[69]:0	ACT #15
P2.0	vext_ref_reg	fixed	ppca.ppcaio[48]:0	ACT #0
	scb6.spi.mosi	ACT #6	scb6.uart.tx	ACT #7
	scb6.i2c.sda	ACT #9	peri.tr_io_input[10]:0	ACT #13
	peri.tr_io_output[10]:0	ACT #14	peri.tr_io_output[70]:0	ACT #15
P2.1	hibernate_wakeup	fixed	ppca.ppcaio[49]:0	ACT #0
	scb6.spi.clk	ACT #6	scb6.uart.rx	ACT #7

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
	scb6.i2c.scl	ACT #9	peri.tr_io_input[11]:0	ACT #13
	peri.tr_io_output[11]:0	ACT #14	peri.tr_io_output[71]:0	ACT #15
	swj.swdoe/tdi	DS #5		
P2.2	ppca.ppcaio[50]:0	ACT #0	cal_wave	DS #0
	scb6.spi.miso	ACT #6	scb6.uart.rts	ACT #7
	scb6.i2c.scl_do	ACT #9	peri.tr_io_input[12]:0	ACT #13
	peri.tr_io_output[12]:0	ACT #14	peri.tr_io_output[72]:0	ACT #15
	swj.trstn	DS #5		
P2.3	ppca.ppcaio[51]:0	ACT #0	can0.rx	ACT #3
	scb0.spi.clk	DS #1	scb0.uart.rx	DS #2
	scb0.i2c.scl	DS #3	peri.tr_io_input[13]:0	ACT #13
	peri.tr_io_output[13]:0	ACT #14	peri.tr_io_output[73]:0	ACT #15
	swj.swo/tdo	DS #5		
P2.4	ppca.ppcaio[52]:0	ACT #0	can0.tx	ACT #3
	scb0.spi.mosi	DS #1	scb0.uart.tx	DS #2
	scb0.i2c.sda	DS #3	tcpwm0.g0.cnt1+	ACT #10
	peri.tr_io_input[14]:0	ACT #13	peri.tr_io_output[14]:0	ACT #14
	peri.tr_io_output[74]:0	ACT #15		
P2.5	ppca.ppcaio[53]:0	ACT #0	scb0.spi.miso	DS #1
	scb0.uart.rts	DS #2	scb0.i2c.scl_do	DS #3
	tcpwm0.g0.cnt1-	ACT #10	peri.tr_io_input[15]:0	ACT #13
	peri.tr_io_output[15]:0	ACT #14	peri.tr_io_output[75]:0	ACT #15
P3.0	ppca.ppcaio[31]:0	ACT #0	can0.tx	ACT #3
	scb2.spi.select1[1)]	ACT #4	scb6.spi.select0	ACT #6
	scb6.uart.cts	ACT #7	scb6.i2c.sda_do	ACT #9
	peri.tr_io_input[16]:0	ACT #13	peri.tr_io_output[16]:0	ACT #14
	peri.tr_io_output[76]:0	ACT #15		
P3.1	ppca.ppcaio[30]:0	ACT #0	can0.rx	ACT #3
	scb2.spi.select0[1)]	ACT #4	scb6.spi.select1	ACT #6
	scb2.uart.cts[1)]	ACT #7	scb2.i2c.sda_do[1)]	ACT #9
	peri.tr_io_input[17]:0	ACT #13	peri.tr_io_output[17]:0	ACT #14
	peri.tr_io_output[77]:0	ACT #15		
P3.2	ppca.ppcaio[40]:0	ACT #0	scb2.spi.miso[1)]	ACT #4

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
	scb6.spi.select2	ACT #6	scb2.uart.rts[1)]	ACT #7
	scb2.i2c.scl_do[1)]	ACT #9	peri.tr_io_input[18]:0	ACT #13
	peri.tr_io_output[18]:0	ACT #14	peri.tr_io_output[78]:0	ACT #15
P3.3	ppca.ppcaio[41]:0	ACT #0	scb2.spi.mosi[1)]	ACT #4
	scb2.uart.tx[1)]	ACT #7	scb2.i2c.sda[1)]	ACT #9
	tcpwm0.g1.cnt0+	ACT #10	peri.tr_io_input[19]:0	ACT #13
	peri.tr_io_output[19]:0	ACT #14	peri.tr_io_output[79]:0	ACT #15
P3.4	ppca.ppcaio[42]:0	ACT #0	scb2.spi.clk[1)]	ACT #4
	scb2.uart.rx[1)]	ACT #7	scb2.i2c.scl[1)]	ACT #9
	tcpwm0.g1.cnt0-	ACT #10	peri.tr_io_input[20]:0	ACT #13
	peri.tr_io_output[20]:0	ACT #14	peri.tr_io_output[80]:0	ACT #15
P3.5	ppca.ppcaio[43]:0	ACT #0	scb4.spi.clk[1)]	ACT #5
	scb4.uart.rx[1)]	ACT #8	scb4.i2c.scl[1)]	ACT #9
	tcpwm0.g1.cnt1+	ACT #10	peri.tr_io_input[21]:0	ACT #13
	peri.tr_io_output[21]:0	ACT #14	peri.tr_io_output[81]:0	ACT #15
P3.6	ppca.ppcaio[44]:0	ACT #0	scb4.spi.mosi[1)]	ACT #5
	scb4.uart.tx[1)]	ACT #8	scb4.i2c.sda[1)]	ACT #9
	tcpwm0.g1.cnt1-	ACT #10	peri.tr_io_input[22]:0	ACT #13
	peri.tr_io_output[22]:0	ACT #14	peri.tr_io_output[82]:0	ACT #15
P3.7	ppca.ppcaio[45]:0	ACT #0	scb2.spi.select2[1)]	ACT #4
	scb4.spi.select2[1)]	ACT #5	peri.tr_io_input[23]:0	ACT #13
	peri.tr_io_output[23]:0	ACT #14	peri.tr_io_output[83]:0	ACT #15
P4.0	ppca.ppcaio[23]:0	ACT #0	scb0.spi.select2	DS #1
	scb4.spi.miso[1)]	ACT #5	scb6.spi.select0	ACT #6
	scb6.uart.cts	ACT #7	scb4.uart.rts[1)]	ACT #8
	scb6.i2c.sda_do	ACT #9	scb4.i2c.scl_do[1)]	ACT #10
	peri.tr_io_input[24]:0	ACT #13	peri.tr_io_output[24]:0	ACT #14
	peri.tr_io_output[84]:0	ACT #15		
P4.1	ppca.ppcaio[22]:0	ACT #0	scb0.spi.select1	DS #1
	scb6.spi.select1	ACT #6	peri.tr_io_input[25]:0	ACT #13
	peri.tr_io_output[25]:0	ACT #14	peri.tr_io_output[85]:0	ACT #15
P4.2	ppca.ppcaio[21]:0	ACT #0	scb0.spi.select0	DS #1
	scb0.uart.cts	DS #2	scb0.i2c.sda_do	DS #3

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
	scb6.spi.select2	ACT #6	peri.tr_io_input[26]:0	ACT #13
	peri.tr_io_output[26]:0	ACT #14	peri.tr_io_output[86]:0	ACT #15
P4.3	ppca.ppcaio[20]:0	ACT #0	scb1.spi.miso[1)]	ACT #4
	scb4.spi.select0[1)]	ACT #5	scb1.uart.rts[1)]	ACT #7
	scb4.uart.cts[1)]	ACT #8	scb1.i2c.scl_do[1)]	ACT #9
	scb4.i2c.sda_do[1)]	ACT #10	peri.tr_io_input[27]:0	ACT #13
	peri.tr_io_output[27]:0	ACT #14	peri.tr_io_output[87]:0	ACT #15
P4.4	ppca.ppcaio[24]:0	ACT #0	peri.tr_io_input[28]:0	ACT #13
	peri.tr_io_output[28]:0	ACT #14	peri.tr_io_output[88]:0	ACT #15
P4.5	ppca.ppcaio[25]:0	ACT #0	scb1.spi.select2[1)]	ACT #4
	peri.tr_io_input[29]:0	ACT #13	peri.tr_io_output[29]:0	ACT #14
	peri.tr_io_output[89]:0	ACT #15		
P4.6	ppca.ppcaio[26]:0	ACT #0	scb1.spi.select1[1)]	ACT #4
	peri.tr_io_input[30]:0	ACT #13	peri.tr_io_output[30]:0	ACT #14
	peri.tr_io_output[90]:0	ACT #15		
P4.7	ppca.ppcaio[27]:0	ACT #0	scb1.spi.select0[1)]	ACT #4
	scb1.uart.cts[1)]	ACT #7	scb1.i2c.sda_do[1)]	ACT #9
	peri.tr_io_input[31]:0	ACT #13	peri.tr_io_output[31]:0	ACT #14
	peri.tr_io_output[91]:0	ACT #15		
P5.0	ppca.ppcaio[28]:0	ACT #0	scb1.spi.mosi[1)]	ACT #4
	scb4.spi.select1[1)]	ACT #5	scb1.uart.tx[1)]	ACT #7
	scb1.i2c.sda[1)]	ACT #9	peri.tr_io_input[32]:0	ACT #13
	peri.tr_io_output[32]:0	ACT #14	peri.tr_io_output[92]:0	ACT #15
P5.1	ppca.ppcaio[29]:0	ACT #0	scb1.spi.clk[1)]	ACT #4
	scb1.uart.rx[1)]	ACT #7	scb1.i2c.scl[1)]	ACT #9
	peri.tr_io_input[33]:0	ACT #13	peri.tr_io_output[33]:0	ACT #14
	peri.tr_io_output[93]:0	ACT #15		
P5.2	ppca.ppcaio[14]:0	ACT #0	peri.tr_io_input[34]:0	ACT #13
	peri.tr_io_output[34]:0	ACT #14	peri.tr_io_output[94]:0	ACT #15
P5.3	ppca.ai8_ai	fixed	ppca.ppcaio[15]:0	ACT #0
	peri.tr_io_input[35]:0	ACT #13	peri.tr_io_output[35]:0	ACT #14
	peri.tr_io_output[95]:0	ACT #15		
P6.0	ppca.ai7_ai	fixed	ppca.ppcaio[16]:0	ACT #0

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
	peri.tr_io_input[36]:0	ACT #13	peri.tr_io_output[36]:0	ACT #14
	peri.tr_io_output[96]:0	ACT #15		
P6.1	ppca.ai6_ai	fixed	ppca.ppcaio[17]:0	ACT #0
	peri.tr_io_input[37]:0	ACT #13	peri.tr_io_output[37]:0	ACT #14
	peri.tr_io_output[97]:0	ACT #15		
P6.2	lpcomp1.in-	fixed	ppca.ai5_ai	fixed
	ppca.ppcaio[18]:0	ACT #0	scb4.spi.select0[1)]	ACT #5
	scb4.uart.cts[1)]	ACT #8	scb4.i2c.sda_do[1)]	ACT #10
	peri.tr_io_input[38]:0	ACT #13	peri.tr_io_output[38]:0	ACT #14
	peri.tr_io_output[98]:0	ACT #15		
P6.3	lpcomp1.in+	fixed	ppca.ai4_ai	fixed
	ppca.ppcaio[19]:0	ACT #0	scb4.spi.miso[1)]	ACT #5
	scb4.uart.rts[1)]	ACT #8	scb4.i2c.scl_do[1)]	ACT #10
	peri.tr_io_input[39]:0	ACT #13	peri.tr_io_output[39]:0	ACT #14
	peri.tr_io_output[99]:0	ACT #15		
P6.4	lpcomp0.in-	fixed	ppca.ai3_ai	fixed
	ppca.ppcaio[46]:0	ACT #0	scb4.spi.mosi[1)]	ACT #5
	scb4.uart.tx[1)]	ACT #8	scb4.i2c.sda[1)]	ACT #9
	peri.tr_io_input[40]:0	ACT #13	peri.tr_io_output[40]:0	ACT #14
	peri.tr_io_output[100]:0	ACT #15		
P6.5	lpcomp0.in+	fixed	ppca.ai2_ai	fixed
	ppca.ppcaio[47]:0	ACT #0	scb4.spi.clk[1)]	ACT #5
	scb4.uart.rx[1)]	ACT #8	scb4.i2c.scl[1)]	ACT #9
	cpuss.fault[0]:1	ACT #10	peri.tr_io_input[41]:0	ACT #13
	peri.tr_io_output[41]:0	ACT #14	peri.tr_io_output[101]:0	ACT #15
P7.0	ppca.ai9_ai	fixed	hibernate_wakeup	fixed
	ppca.ppcaio[32]:0	ACT #0	can1.rx	ACT #3
	scb5.spi.clk[1)]	ACT #6	scb5.uart.rx[1)]	ACT #8
	scb5.i2c.scl[1)]	ACT #9	trace.clock	ACT #10
	peri.tr_io_input[42]:0	ACT #13	peri.tr_io_output[42]:0	ACT #14
	peri.tr_io_output[102]:0	ACT #15		
P7.1	ppca.ai10_ai	fixed	ppca.ppcaio[33]:0	ACT #0
	can1.tx	ACT #3	scb5.spi.mosi[1)]	ACT #6

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
	scb5.uart.tx[1)]	ACT #8	scb5.i2c.sda[1)]	ACT #9
	trace.data0	ACT #10	peri.tr_io_input[43]:0	ACT #13
	peri.tr_io_output[43]:0	ACT #14	peri.tr_io_output[103]:0	ACT #15
P7.2	ppca.ai11_ai	fixed	ppca.ppcaio[34]:0	ACT #0
	scb5.spi.miso[1)]	ACT #6	scb5.uart.rts[1)]	ACT #8
	scb5.i2c.scl_do[1)]	ACT #9	trace.data1	ACT #10
	ext_clk	ACT #11	peri.tr_io_input[44]:0	ACT #13
	peri.tr_io_output[44]:0	ACT #14	peri.tr_io_output[104]:0	ACT #15
P7.3	ppca.ai12_ai	fixed	ppca.ppcaio[35]:0	ACT #0
	scb5.spi.select0[1)]	ACT #6	scb5.uart.cts[1)]	ACT #8
	scb5.i2c.sda_do[1)]	ACT #9	trace.data2	ACT #10
	peri.tr_io_input[45]:0	ACT #13	peri.tr_io_output[45]:0	ACT #14
	peri.tr_io_output[105]:0	ACT #15		
P7.4	ppca.ai13_ai	fixed	ppca.ppcaio[36]:0	ACT #0
	can1.tx	ACT #3	scb5.spi.select1[1)]	ACT #6
	trace.data3	ACT #10	peri.tr_io_input[46]:0	ACT #13
	peri.tr_io_output[46]:0	ACT #14	peri.tr_io_output[106]:0	ACT #15
P7.5	ppca.ai14_ai	fixed	ppca.ppcaio[37]:0	ACT #0
	can1.rx	ACT #3	scb5.spi.select2[1)]	ACT #6
	peri.tr_io_input[47]:0	ACT #13	peri.tr_io_output[47]:0	ACT #14
	peri.tr_io_output[107]:0	ACT #15		
P7.6	ppca.ai15_ai	fixed	ppca.ppcaio[38]:0	ACT #0
	peri.tr_io_input[48]:0	ACT #13	peri.tr_io_output[48]:0	ACT #14
	peri.tr_io_output[108]:0	ACT #15		
P7.7	ppca.ppcaio[39]:0	ACT #0	peri.tr_io_input[49]:0	ACT #13
	peri.tr_io_output[49]:0	ACT #14	peri.tr_io_output[109]:0	ACT #15
P8.0	ppca.ppcaio[0]:0	ACT #0	scb3.spi.clk	ACT #4
	scb5.spi.select0[1)]	ACT #6	scb3.uart.rx	ACT #7
	scb3.i2c.scl	ACT #9	trace.data3	ACT #10
	cpuss.clk_fm_pump	ACT #11	peri.tr_io_input[50]:0	ACT #13
	peri.tr_io_output[50]:0	ACT #14	peri.tr_io_output[110]:0	ACT #15
P8.1	ppca.ppcaio[1]:0	ACT #0	scb3.spi.mosi	ACT #4
	scb5.spi.select1[1)]	ACT #6	scb3.uart.tx	ACT #7

(table continues...)

Table 6 (continued) GPIO alternate functions and HSIOM routes

GPIO	Alternate functions and HSIOM routes			
	scb3.i2c.sda	ACT #9	trace.data2	ACT #10
	peri.tr_io_input[51]:0	ACT #13	peri.tr_io_output[51]:0	ACT #14
	peri.tr_io_output[111]:0	ACT #15		
P8.2	ppca.ppcaio[2]:0	ACT #0	scb3.spi.miso	ACT #4
	scb5.spi.select2[1)]	ACT #6	scb3.uart.rts	ACT #7
	scb3.i2c.scl_do	ACT #9	trace.data1	ACT #10
	peri.tr_io_input[52]:0	ACT #13	peri.tr_io_output[52]:0	ACT #14
	peri.tr_io_output[112]:0	ACT #15		
P8.3	svgs.svgs_test_vccd_feed	fixed	ppca.ppcaio[3]:0	ACT #0
	scb3.spi.select0	ACT #4	scb3.uart.cts	ACT #7
	scb3.i2c.sda_do	ACT #9	trace.data0	ACT #10
	ext_clk	ACT #11	peri.tr_io_input[53]:0	ACT #13
	peri.tr_io_output[53]:0	ACT #14	peri.tr_io_output[113]:0	ACT #15
P8.4	ppca.ppcaio[4]:0	ACT #0	scb3.spi.select1	ACT #4
	trace.clock	ACT #10	peri.tr_io_input[54]:0	ACT #13
	peri.tr_io_output[54]:0	ACT #14	peri.tr_io_output[114]:0	ACT #15
P8.5	ppca.ppcaio[5]:0	ACT #0	scb3.spi.select2	ACT #4
	cpuss.fault[0]:0	ACT #10	peri.tr_io_input[55]:0	ACT #13
	peri.tr_io_output[55]:0	ACT #14	peri.tr_io_output[115]:0	ACT #15
P9.0	ppca.ppcaio[6]:0	ACT #0	peri.tr_io_input[56]:0	ACT #13
	peri.tr_io_output[56]:0	ACT #14	peri.tr_io_output[116]:0	ACT #15
P9.1	ppca.ppcaio[7]:0	ACT #0	peri.tr_io_input[57]:0	ACT #13
	peri.tr_io_output[57]:0	ACT #14	peri.tr_io_output[117]:0	ACT #15
P9.2	ppca.ppcaio[8]:0	ACT #0	peri.tr_io_input[58]:0	ACT #13
	peri.tr_io_output[58]:0	ACT #14	peri.tr_io_output[118]:0	ACT #15
P9.3	ppca.ppcaio[9]:0	ACT #0	peri.tr_io_input[59]:0	ACT #13
	peri.tr_io_output[59]:0	ACT #14	peri.tr_io_output[119]:0	ACT #15

1) SCB1, SCB2, and SCB4 are not available on 64-pin devices. Additionally, SCB5 is not available on 48-pin devices.

Table 7 GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
cal_wave	P2.2	can0.rx	P2.3, P3.1	can0.tx	P2.4, P3.0
can1.rx	P7.0, P7.5	can1.tx	P7.1, P7.4	cpuss.clk_fm_pump	P8.0

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
cpuss.fault[0]:0	P8.5	cpuss.fault[0]:1	P6.5	eco_in	P1.0
eco_out	P1.1	ext_clk	P7.2, P8.3	hibernate_wakeup	P2.1, P7.0
lpcomp0.in+	P6.5	lpcomp0.in-	P6.4	lpcomp1.in+	P6.3
lpcomp1.in-	P6.2	peri.tr_io_input[0]:0	P0.0	peri.tr_io_input[10]:0	P2.0
peri.tr_io_input[11]:0	P2.1	peri.tr_io_input[12]:0	P2.2	peri.tr_io_input[13]:0	P2.3
peri.tr_io_input[14]:0	P2.4	peri.tr_io_input[15]:0	P2.5	peri.tr_io_input[16]:0	P3.0
peri.tr_io_input[17]:0	P3.1	peri.tr_io_input[18]:0	P3.2	peri.tr_io_input[19]:0	P3.3
peri.tr_io_input[1]:0	P0.1	peri.tr_io_input[20]:0	P3.4	peri.tr_io_input[21]:0	P3.5
peri.tr_io_input[22]:0	P3.6	peri.tr_io_input[23]:0	P3.7	peri.tr_io_input[24]:0	P4.0
peri.tr_io_input[25]:0	P4.1	peri.tr_io_input[26]:0	P4.2	peri.tr_io_input[27]:0	P4.3
peri.tr_io_input[28]:0	P4.4	peri.tr_io_input[29]:0	P4.5	peri.tr_io_input[2]:0	P1.0
peri.tr_io_input[30]:0	P4.6	peri.tr_io_input[31]:0	P4.7	peri.tr_io_input[32]:0	P5.0
peri.tr_io_input[33]:0	P5.1	peri.tr_io_input[34]:0	P5.2	peri.tr_io_input[35]:0	P5.3
peri.tr_io_input[36]:0	P6.0	peri.tr_io_input[37]:0	P6.1	peri.tr_io_input[38]:0	P6.2
peri.tr_io_input[39]:0	P6.3	peri.tr_io_input[3]:0	P1.1	peri.tr_io_input[40]:0	P6.4
peri.tr_io_input[41]:0	P6.5	peri.tr_io_input[42]:0	P7.0	peri.tr_io_input[43]:0	P7.1
peri.tr_io_input[44]:0	P7.2	peri.tr_io_input[45]:0	P7.3	peri.tr_io_input[46]:0	P7.4
peri.tr_io_input[47]:0	P7.5	peri.tr_io_input[48]:0	P7.6	peri.tr_io_input[49]:0	P7.7
peri.tr_io_input[4]:0	P1.2	peri.tr_io_input[50]:0	P8.0	peri.tr_io_input[51]:0	P8.1
peri.tr_io_input[52]:0	P8.2	peri.tr_io_input[53]:0	P8.3	peri.tr_io_input[54]:0	P8.4

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
peri.tr_io_input[55]:0	P8.5	peri.tr_io_input[56]:0	P9.0	peri.tr_io_input[57]:0	P9.1
peri.tr_io_input[58]:0	P9.2	peri.tr_io_input[59]:0	P9.3	peri.tr_io_input[5]:0	P1.3
peri.tr_io_input[6]:0	P1.4	peri.tr_io_input[7]:0	P1.5	peri.tr_io_input[8]:0	P1.6
peri.tr_io_input[9]:0	P1.7	peri.tr_io_output[0]:0	P0.0	peri.tr_io_output[100]:0	P6.4
peri.tr_io_output[101]:0	P6.5	peri.tr_io_output[102]:0	P7.0	peri.tr_io_output[103]:0	P7.1
peri.tr_io_output[104]:0	P7.2	peri.tr_io_output[105]:0	P7.3	peri.tr_io_output[106]:0	P7.4
peri.tr_io_output[107]:0	P7.5	peri.tr_io_output[108]:0	P7.6	peri.tr_io_output[109]:0	P7.7
peri.tr_io_output[10]:0	P2.0	peri.tr_io_output[110]:0	P8.0	peri.tr_io_output[111]:0	P8.1
peri.tr_io_output[112]:0	P8.2	peri.tr_io_output[113]:0	P8.3	peri.tr_io_output[114]:0	P8.4
peri.tr_io_output[115]:0	P8.5	peri.tr_io_output[116]:0	P9.0	peri.tr_io_output[117]:0	P9.1
peri.tr_io_output[118]:0	P9.2	peri.tr_io_output[119]:0	P9.3	peri.tr_io_output[11]:0	P2.1
peri.tr_io_output[12]:0	P2.2	peri.tr_io_output[13]:0	P2.3	peri.tr_io_output[14]:0	P2.4
peri.tr_io_output[15]:0	P2.5	peri.tr_io_output[16]:0	P3.0	peri.tr_io_output[17]:0	P3.1
peri.tr_io_output[18]:0	P3.2	peri.tr_io_output[19]:0	P3.3	peri.tr_io_output[1]:0	P0.1
peri.tr_io_output[20]:0	P3.4	peri.tr_io_output[21]:0	P3.5	peri.tr_io_output[22]:0	P3.6
peri.tr_io_output[23]:0	P3.7	peri.tr_io_output[24]:0	P4.0	peri.tr_io_output[25]:0	P4.1
peri.tr_io_output[26]:0	P4.2	peri.tr_io_output[27]:0	P4.3	peri.tr_io_output[28]:0	P4.4
peri.tr_io_output[29]:0	P4.5	peri.tr_io_output[2]:0	P1.0	peri.tr_io_output[30]:0	P4.6
peri.tr_io_output[31]:0	P4.7	peri.tr_io_output[32]:0	P5.0	peri.tr_io_output[33]:0	P5.1

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
peri.tr_io_output[34]:0	P5.2	peri.tr_io_output[35]:0	P5.3	peri.tr_io_output[36]:0	P6.0
peri.tr_io_output[37]:0	P6.1	peri.tr_io_output[38]:0	P6.2	peri.tr_io_output[39]:0	P6.3
peri.tr_io_output[3]:0	P1.1	peri.tr_io_output[40]:0	P6.4	peri.tr_io_output[41]:0	P6.5
peri.tr_io_output[42]:0	P7.0	peri.tr_io_output[43]:0	P7.1	peri.tr_io_output[44]:0	P7.2
peri.tr_io_output[45]:0	P7.3	peri.tr_io_output[46]:0	P7.4	peri.tr_io_output[47]:0	P7.5
peri.tr_io_output[48]:0	P7.6	peri.tr_io_output[49]:0	P7.7	peri.tr_io_output[4]:0	P1.2
peri.tr_io_output[50]:0	P8.0	peri.tr_io_output[51]:0	P8.1	peri.tr_io_output[52]:0	P8.2
peri.tr_io_output[53]:0	P8.3	peri.tr_io_output[54]:0	P8.4	peri.tr_io_output[55]:0	P8.5
peri.tr_io_output[56]:0	P9.0	peri.tr_io_output[57]:0	P9.1	peri.tr_io_output[58]:0	P9.2
peri.tr_io_output[59]:0	P9.3	peri.tr_io_output[5]:0	P1.3	peri.tr_io_output[60]:0	P0.0
peri.tr_io_output[61]:0	P0.1	peri.tr_io_output[62]:0	P1.0	peri.tr_io_output[63]:0	P1.1
peri.tr_io_output[64]:0	P1.2	peri.tr_io_output[65]:0	P1.3	peri.tr_io_output[66]:0	P1.4
peri.tr_io_output[67]:0	P1.5	peri.tr_io_output[68]:0	P1.6	peri.tr_io_output[69]:0	P1.7
peri.tr_io_output[6]:0	P1.4	peri.tr_io_output[70]:0	P2.0	peri.tr_io_output[71]:0	P2.1
peri.tr_io_output[72]:0	P2.2	peri.tr_io_output[73]:0	P2.3	peri.tr_io_output[74]:0	P2.4
peri.tr_io_output[75]:0	P2.5	peri.tr_io_output[76]:0	P3.0	peri.tr_io_output[77]:0	P3.1
peri.tr_io_output[78]:0	P3.2	peri.tr_io_output[79]:0	P3.3	peri.tr_io_output[7]:0	P1.5
peri.tr_io_output[80]:0	P3.4	peri.tr_io_output[81]:0	P3.5	peri.tr_io_output[82]:0	P3.6
peri.tr_io_output[83]:0	P3.7	peri.tr_io_output[84]:0	P4.0	peri.tr_io_output[85]:0	P4.1

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
peri.tr_io_output[86]:0	P4.2	peri.tr_io_output[87]:0	P4.3	peri.tr_io_output[88]:0	P4.4
peri.tr_io_output[89]:0	P4.5	peri.tr_io_output[8]:0	P1.6	peri.tr_io_output[90]:0	P4.6
peri.tr_io_output[91]:0	P4.7	peri.tr_io_output[92]:0	P5.0	peri.tr_io_output[93]:0	P5.1
peri.tr_io_output[94]:0	P5.2	peri.tr_io_output[95]:0	P5.3	peri.tr_io_output[96]:0	P6.0
peri.tr_io_output[97]:0	P6.1	peri.tr_io_output[98]:0	P6.2	peri.tr_io_output[99]:0	P6.3
peri.tr_io_output[9]:0	P1.7	ppca.ai10_ai	P7.1	ppca.ai11_ai	P7.2
ppca.ai12_ai	P7.3	ppca.ai13_ai	P7.4	ppca.ai14_ai	P7.5
ppca.ai15_ai	P7.6	ppca.ai2_ai	P6.5	ppca.ai3_ai	P6.4
ppca.ai4_ai	P6.3	ppca.ai5_ai	P6.2	ppca.ai6_ai	P6.1
ppca.ai7_ai	P6.0	ppca.ai8_ai	P5.3	ppca.ai9_ai	P7.0
ppca.ppcaio[0]:0	P8.0	ppca.ppcaio[10]:0	P1.4	ppca.ppcaio[11]:0	P1.5
ppca.ppcaio[12]:0	P1.6	ppca.ppcaio[13]:0	P1.7	ppca.ppcaio[14]:0	P5.2
ppca.ppcaio[15]:0	P5.3	ppca.ppcaio[16]:0	P6.0	ppca.ppcaio[17]:0	P6.1
ppca.ppcaio[18]:0	P6.2	ppca.ppcaio[19]:0	P6.3	ppca.ppcaio[1]:0	P8.1
ppca.ppcaio[20]:0	P4.3	ppca.ppcaio[21]:0	P4.2	ppca.ppcaio[22]:0	P4.1
ppca.ppcaio[23]:0	P4.0	ppca.ppcaio[24]:0	P4.4	ppca.ppcaio[25]:0	P4.5
ppca.ppcaio[26]:0	P4.6	ppca.ppcaio[27]:0	P4.7	ppca.ppcaio[28]:0	P5.0
ppca.ppcaio[29]:0	P5.1	ppca.ppcaio[2]:0	P8.2	ppca.ppcaio[30]:0	P3.1
ppca.ppcaio[31]:0	P3.0	ppca.ppcaio[32]:0	P7.0	ppca.ppcaio[33]:0	P7.1
ppca.ppcaio[34]:0	P7.2	ppca.ppcaio[35]:0	P7.3	ppca.ppcaio[36]:0	P7.4
ppca.ppcaio[37]:0	P7.5	ppca.ppcaio[38]:0	P7.6	ppca.ppcaio[39]:0	P7.7
ppca.ppcaio[3]:0	P8.3	ppca.ppcaio[40]:0	P3.2	ppca.ppcaio[41]:0	P3.3
ppca.ppcaio[42]:0	P3.4	ppca.ppcaio[43]:0	P3.5	ppca.ppcaio[44]:0	P3.6
ppca.ppcaio[45]:0	P3.7	ppca.ppcaio[46]:0	P6.4	ppca.ppcaio[47]:0	P6.5
ppca.ppcaio[48]:0	P2.0	ppca.ppcaio[49]:0	P2.1	ppca.ppcaio[4]:0	P8.4
ppca.ppcaio[50]:0	P2.2	ppca.ppcaio[51]:0	P2.3	ppca.ppcaio[52]:0	P2.4
ppca.ppcaio[53]:0	P2.5	ppca.ppcaio[54]:0	P0.0	ppca.ppcaio[55]:0	P0.1
ppca.ppcaio[56]:0	P1.0	ppca.ppcaio[57]:0	P1.1	ppca.ppcaio[58]:0	P1.2
ppca.ppcaio[59]:0	P1.3	ppca.ppcaio[5]:0	P8.5	ppca.ppcaio[6]:0	P9.0

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
ppca.ppcaio[7]:0	P9.1	ppca.ppcaio[8]:0	P9.2	ppca.ppcaio[9]:0	P9.3
scb0.i2c.scl	P2.3	scb0.i2c.scl_do	P2.5	scb0.i2c.sda	P2.4
scb0.i2c.sda_do	P4.2	scb0.spi.clk	P2.3	scb0.spi.miso	P2.5
scb0.spi.mosi	P2.4	scb0.spi.select0	P4.2	scb0.spi.select1	P4.1
scb0.spi.select2	P4.0	scb0.uart.cts	P4.2	scb0.uart.rts	P2.5
scb0.uart.rx	P2.3	scb0.uart.tx	P2.4	scb1.i2c.scl[1)]	P5.1
scb1.i2c.scl_do[1)]	P4.3	scb1.i2c.sda[1)]	P5.0	scb1.i2c.sda_do[1)]	P4.7
scb1.spi.clk[1)]	P5.1	scb1.spi.miso[1)]	P4.3	scb1.spi.mosi[1)]	P5.0
scb1.spi.select0[1)]	P4.7	scb1.spi.select1[1)]	P4.6	scb1.spi.select2[1)]	P4.5
scb1.uart.cts[1)]	P4.7	scb1.uart.rts[1)]	P4.3	scb1.uart.rx[1)]	P5.1
scb1.uart.tx[1)]	P5.0	scb2.i2c.scl[1)]	P3.4	scb2.i2c.scl_do[1)]	P3.2
scb2.i2c.sda[1)]	P3.3	scb2.i2c.sda_do[1)]	P3.1	scb2.spi.clk[1)]	P3.4
scb2.spi.miso[1)]	P3.2	scb2.spi.mosi[1)]	P3.3	scb2.spi.select0[1)]	P3.1
scb2.spi.select1[1)]	P3.0	scb2.spi.select2[1)]	P3.7	scb2.uart.cts[1)]	P3.1
scb2.uart.rts[1)]	P3.2	scb2.uart.rx[1)]	P3.4	scb2.uart.tx[1)]	P3.3
scb3.i2c.scl	P8.0	scb3.i2c.scl_do	P8.2	scb3.i2c.sda	P8.1
scb3.i2c.sda_do	P8.3	scb3.spi.clk	P8.0	scb3.spi.miso	P8.2
scb3.spi.mosi	P8.1	scb3.spi.select0	P8.3	scb3.spi.select1	P8.4
scb3.spi.select2	P8.5	scb3.uart.cts	P8.3	scb3.uart.rts	P8.2
scb3.uart.rx	P8.0	scb3.uart.tx	P8.1	scb4.i2c.scl[1)]	P3.5, P6.5
scb4.i2c.scl_do[1)]	P4.0, P6.3	scb4.i2c.sda[1)]	P3.6, P6.4	scb4.i2c.sda_do[1)]	P4.3, P6.2
scb4.spi.clk[1)]	P3.5, P6.5	scb4.spi.miso[1)]	P4.0, P6.3	scb4.spi.mosi[1)]	P3.6, P6.4
scb4.spi.select0[1)]	P4.3, P6.2	scb4.spi.select1[1)]	P5.0	scb4.spi.select2[1)]	P3.7
scb4.uart.cts[1)]	P4.3, P6.2	scb4.uart.rts[1)]	P4.0, P6.3	scb4.uart.rx[1)]	P3.5, P6.5
scb4.uart.tx[1)]	P3.6, P6.4	scb5.i2c.scl[1)]	P7.0	scb5.i2c.scl_do[1)]	P7.2
scb5.i2c.sda[1)]	P7.1	scb5.i2c.sda_do[1)]	P7.3	scb5.spi.clk[1)]	P7.0
scb5.spi.miso[1)]	P7.2	scb5.spi.mosi[1)]	P7.1	scb5.spi.select0[1)]	P7.3, P8.0
scb5.spi.select1[1)]	P7.4, P8.1	scb5.spi.select2[1)]	P7.5, P8.2	scb5.uart.cts[1)]	P7.3
scb5.uart.rts[1)]	P7.2	scb5.uart.rx[1)]	P7.0	scb5.uart.tx[1)]	P7.1
scb6.i2c.scl	P2.1	scb6.i2c.scl_do	P2.2	scb6.i2c.sda	P2.0
scb6.i2c.sda_do	P3.0, P4.0	scb6.spi.clk	P2.1	scb6.spi.miso	P2.2
scb6.spi.mosi	P2.0	scb6.spi.select0	P3.0, P4.0	scb6.spi.select1	P3.1, P4.1
scb6.spi.select2	P3.2, P4.2	scb6.uart.cts	P3.0, P4.0	scb6.uart.rts	P2.2

(table continues...)

Table 7 (continued) GPIO alternate functions

Function	GPIOs	Function	GPIOs	Function	GPIOs
scb6.uart.rx	P2.1	scb6.uart.tx	P2.0	svgs.svgs_test_vccd_feed	P8.3
swj.swclk/tclk	P1.2	swj.swdio/tms	P1.3	swj.swdoe/tdi	P2.1
swj.swo/tdo	P2.3	swj.trstn	P2.2	tcpwm0.g0.cnt0+	P1.2
tcpwm0.g0.cnt0-	P1.3	tcpwm0.g0.cnt1+	P2.4	tcpwm0.g0.cnt1-	P2.5
tcpwm0.g1.cnt0+	P3.3	tcpwm0.g1.cnt0-	P3.4	tcpwm0.g1.cnt1+	P3.5
tcpwm0.g1.cnt1-	P3.6	trace.clock	P7.0, P8.4	trace.data0	P7.1, P8.3
trace.data1	P7.2, P8.2	trace.data2	P7.3, P8.1	trace.data3	P7.4, P8.0
vext_ref_reg	P2.0	wco_in	P0.1	wco_out	P0.0

7 Electrical specifications

7.1 Absolute maximum ratings

Table 8 Absolute maximum ratings

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID1	Analog or Digital supply relative to Vss (Vssd=Vssa)	VDD_ABS	–0.5	-	4	V	Absolute maximum
SID2	Direct digital core voltage input relative to Vssd	VCCD_ABS	–0.5	-	1.2	V	Absolute maximum
SID3	GPIO voltage ; VDDD or VDDA	VGPIO_ABS	–0.5	-	VDD+0.5	V	Absolute maximum
SID4	Current per GPIO	IGPIO_ABS	–25	-	25	mA	Absolute maximum
SID5	GPIO injection current per pin	IGPIO_injection	–0.5	-	0.5	mA	Absolute maximum
SID3A	Electrostatic discharge human body model	ESD_HBM	2000	-	-	V	Absolute maximum
SID4A	Electrostatic discharge charged device model	ESD_CDM	500	-	-	V	Absolute maximum
SID5A	Pin current for latchup free operation	LU	–100	-	100	mA	Absolute maximum
SIDWA8	Maximum undershoot voltage for I/O	Vundershoot	-	-	–0.5	V	Duration not to exceed 25% of the duty cycle
SIDWA9	Maximum overshoot voltage for I/O	Vovershoot	-	-	VDDIO + 0.5	V	Duration not to exceed 25% of the duty cycle
SIDWA10	Maximum junction temperature	Tj	-	-	125	°C	

7.2 Power supplies

Table 9 Power supplies

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
DC specifications							
SID6	Internal regulator	VDDD	1.71	-	3.63	V	The user must ensure that VDDA is powered up before or same time as VDDD to avoid any cross current flowing from VDDD. If VDDA is not powered up while VDDD is available, VDDA shall be grounded.
SID7B	GPIO supply for Ports 1, 2, 3, 4, 5, 6, 7	VDDIO_0	1.71	-	3.63	V	
SID7C	GPIO supply for Ports 8 and 9	VDDIO_1	1.71	-	3.63	V	
SID7A	Analog power supply for ADC and comparator	VDDA	2.97	-	3.63	V	The user must ensure that VDDA is powered up before or same time as VDDD to avoid any cross current flowing from VDDD. If VDDA is not powered up while VDDD is available, VDDA shall be grounded. Analog subsystem(ATOP SS) is designed to handle supply transients upto 2.6 V.
SID6B	Backup power; normally shorted to VDDD (supply PORT 0)	VBACKUP	1.71	-	3.63	V	Min. is 1.4 V in Backup mode.
SID7D	Chip supply ground	VSSS	-	0	-	V	
SID7F	Analog ground supply	VSSA	-	0	-	V	
SID8	Output voltage (for core logic bypass)	VCCD (OD)	-	1.2	-	V	Overdrive mode. Valid for –40 to 125°C.

(table continues...)

Table 9 (continued) Power supplies

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID8A	Output voltage (for core logic bypass)	VCCD (LP)	-	1.1	-	V	High-speed mode. Valid for –40 to 125°C.
SID8B	Output voltage (for core logic bypass)	VCCD (MF)	-	1	-	V	MF mode. Valid for –40 to 125°C.
SID8C	Output voltage (for core logic bypass)	VCCD (ULP)	-	0.9	-	V	ULP mode. Valid for –40 to 125°C.
SID10	External regulator voltage (VCCD) bypass	CEFC	3.8	4.7	5.6	µF	X5R ceramic or better. Value for 0.8 10 1.2 V.
SID11	Power supply decoupling capacitor	CEXC	-	10	-	µF	X5R ceramic or better
Deep Sleep mode							
SIDDS1	With internal LDO enabled and no SRAM retention	IDD33	-	16	-	µA	Not including analog leakage on VDDA and VAREF_EXT
SIDDS1_A	With internal LDO enabled and 64K SRAM retention	IDD33A	-	17	-	µA	Not including analog leakage on VDDA and VAREF_EXT
SIDDS1_B	With internal LDO enabled and 128K SRAM retention	IDD33A_B	-	18.5	-	µA	Not including analog leakage on VDDA and VAREF_EXT
SIDDS2	Leakage on analog supply and analog reference in deep sleep mode	IDDA	-	0.1	3	µA	Max value is at 85°C
Hibernate mode							
SIDHIB1	Leakage current at VDDD = 1.8 V	IDD34	-	300	-	nA	No clocks running (not including analog leakage on VDDA and VAREF_EXT)
SIDHIB2	Leakage current at VDDD = 3.3 V	IDD34A	-	2400	-	nA	No clocks running (not including analog leakage on VDDA and VAREF_EXT)
SIDHIB3	Leakage current at VDDD = 1.8 V with WCO running	IDD35	-	800	-	nA	WCO is running, lpcomp active (not including analog leakage on VDDA and VAREF_EXT)

(table continues...)

Table 9 (continued) Power supplies

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SIDHIB4	Leakage current at VDDD = 3.3 V with WCO running	IDD35A	-	3000	-	nA	WCO is running, lpcomp active (not including analog leakage on VDDA and VAREF_EXT)
SIDHIB5	Leakage on analog supply and analog reference in Hibernate mode.	IDDA	-	0.1	3	µA	Max value is at 85°C and VDDD=3.3 V

7.3 CPU current and transition times

Table 10 CPU current and transition times

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
Cortex®-M33. Active mode							
SIDC2	Execute from Cache; CM33 Active 180 MHz. PLL. Dhrystone. OD mode	IDD4	-	21	43	mA	VDDD=3.3 V, Max at 125°C and PPCA not included
SIDC2A	Execute from Cache; CM33 Active 180 MHz. PLL. Dhrystone. OD mode	IDD4A	-	21	43	mA	VDDD=1.8 V, Max at 125°C and PPCA not included
SIDC3	Execute from Cache; CM33 Active 150 MHz. PLL. Dhrystone. LP mode	IDD5	-	16	35	mA	VDDD=3.3 V, Max at 125°C and PPCA not included
SIDC3A	Execute from Cache; CM33 Active 150 MHz. PLL. Dhrystone. LP mode	IDD5A	-	16	35	mA	VDDD=1.8 V, Max at 125°C and PPCA not included
SIDC4	Execute from Cache; CM33 Active 70 MHz. PLL. Dhrystone. MF mode	IDD6	-	8	23	mA	VDDD=3.3 V, Max at 125°C and PPCA not included
SIDC4A	Execute from Cache; CM33 Active 70 MHz. PLL. Dhrystone. MF mode	IDD6A	-	8	23	mA	VDDD=1.8 V, Max at 125°C and PPCA not included
SIDC5	Execute from Cache; CM33 Active 50 MHz. PLL. Dhrystone. ULP mode	IDD7	-	6	19	mA	VDDD=3.3 V, Max at 125°C and PPCA not included

(table continues...)

Table 10 (continued) CPU current and transition times

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SIDC5A	Execute from Cache; CM33 Active 50 MHz. PLL. Dhrystone. ULP mode	IDD7A	-	6	19	mA	VDDD=1.8 V, Max at 125°C and PPCA not included
Cortex®-M33 Sleep mode							
SIDS1	CM33 Sleep 180 MHz. PLL., OD mode	IDD11	-	8	20	mA	VDDD=3.3 V, Max at 105°C
SIDS1A	CM33 Sleep 180 MHz. PLL., OD mode	IDD11A	-	8	20	mA	VDDD=1.8 V, Max at 105°C
SIDS2	CM33 Sleep 150 MHz. PLL., LP mode	IDD12	-	7	17	mA	VDDD=3.3 V, Max at 105°C
SIDS2A	CM33 Sleep 150 MHz. PLL., LP mode	IDD12A	-	7	16	mA	VDDD=1.8 V, Max at 105°C
SIDS3	CM33 Sleep 70 MHz. PLL., MF mode	IDD13	-	4	12	mA	VDDD=3.3 V, Max at 105°C
SIDS3A	CM33 Sleep 70 MHz. PLL., MF mode	IDD13A	-	4	12	mA	VDDD=1.8 V, Max at 105°C
SIDS4	CM33 Sleep 50 MHz. PLL., ULP mode	IDD14	-	3	9.5	mA	VDDD=3.3 V, Max at 105°C
SIDS4A	CM33 Sleep 50 MHz. PLL., ULP mode	IDD14A	-	3	9.5	mA	VDDD=1.8 V, Max at 105°C
Boot time							
SIDBT0	Boot time after reset (without secure Boot)	BTIME_NO_SEC	-	-	1.2	ms	
SIDBT1	Boot time after reset (including HASH verification)	BTIME	-	-	18.5	ms	HASH of OEM image size of 256 Kb
SIDBT1_A	Boot time after reset (including HASH verification)	BTIME_512	-	-	30.5	ms	HASH of OEM image size of 512 Kb
SIDBT2	Boot time after reset (including HASH verification and signature validation)	BTIME_VER_256	-	-	93	ms	HASH and ECDSA P-256 Signature validation of OEM image size of 16 Kb
SIDBT2_A	Boot time after reset (including HASH verification & signature validation)	BTIME_VER_521	-	-	336	ms	HASH and ECDSA P-521 Signature validation of OEM image size of 16 Kb

(table continues...)

Table 10 (continued) CPU current and transition times

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
Power mode transition times							
SID13A	Deep Sleep to Active OD transition time	TDS_ACT	-	-	45	µs	Deep Sleep to Active OD for VDDD > 2.25 V
SID13A1	Deep Sleep to Active OD transition time	TDS_ACT1	-	-	45	µs	Deep Sleep to Active OD for VDDD < 2.25 V
SID13B	Deep Sleep to Active LP transition time	TDS_ACTLP	-	-	26	µs	Deep Sleep to Active LP for VDDD > 2.25 V
SID13B1	Deep Sleep to Active LP transition time	TDS_ACTLP1	-	-	26	µs	Deep Sleep to Active LP for VDDD < 2.25 V
SID13C	Deep Sleep-RAM to Active transition time	TDSR_ACT	-	-	750	µs	Deep Sleep-RAM to Active OD
SID13D	Deep Sleep-RAM to Active LP transition time	TDSR_ACTLP	-	-	750	µs	Deep Sleep-RAM to Active LP
SID14	Hibernate to Active transition time	THIB_ACT	-	1330	1800	µs	Including PLL lock time
SID14A	Active OD to Deep Sleep transition	TACT_DS	-	-	35	µs	For VDDD < 2.25 V
SID14B	Active OD to Deep Sleep transition	TACT_DS1	-	-	35	µs	For VDDD > 2.25 V

7.4 XRES

Table 11 XRES

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
XRES AC specifications							
SID15	POR or XRES release to Active transition time	TXRES_ACT	-	1.5	2.7	ms	Listening window = 0 ms
SID16	XRES Pulse width	TXRES_PW	5	-	-	µs	-
XRES DC specifications							
SID17	IDD when XRES asserted	TXRES_IDD	-	180	-	µA	VDDD = 1.8 V
SID17A	IDD when XRES asserted	TXRES_IDD_1	-	330	-	µA	VDDD = 3.3 V
SID77	Input voltage high threshold	VIH	0.7*VDDD	-	-	V	CMOS Input
SID78	Input voltage low threshold	VIL	-	-	0.3*VDDD	V	CMOS Input

(table continues...)

Table 11 (continued) XRES

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID80	Input capacitance	CIN	-	3	-	pF	XRES resistor removed
SID81	Input voltage hysteresis	VHYSXRES	-	100	-	mV	-
SID82	Current through protection diode to VDDD/VSSS	IDIODE	-	-	100	µA	-

7.5 GPIO

Table 12 GPIO

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
GPIO DC specifications							
SID57	Input voltage high threshold	VIH	0.7*VDDD	-	-	V	CMOS Input
SID57A	Input current when Pad > VDDIO for OVT inputs	Iihs	-	-	10	µA	Per I^2C Spec
SID58	Input voltage low threshold	VIL	-	-	0.3*VDDD	V	CMOS Input
SID243	LVTTL input, VDDD >= 2.7 V	VIH	2.0	-	-	V	-
SID244	LVTTL input, VDDD >= 2.7 V	VIL	-	-	0.8	V	-
SID59	Output voltage high level	VOH	VDDD-0.5	-	-	V	Ioh = 6 mA
SID62A	Output voltage low level	VOL	-	-	0.4	V	Iol = 6 mA
SID63	Pull-up resistor	RPULLUP	3.5	5.6	8.5	kΩ	-
SID64	Pull-down resistor	RPULLDOWN	3.5	5.6	8.5	kΩ	-
SID65	Input leakage current(absolute value)	IIL	-	-	2	nA	25° C, VDDD = 3.0 V
SID66	Input capacitance	CIN	-	-	5	pF	-
SID67	Input hysteresis LVTTL VDDD > 2.7V	VHYSTTL	100	-	-	mV	-
SID68	Input hysteresis CMOS	VHYSCMOS	0.05*VDDD	-	-	mV	-
SID69	Current through protection diode to VDDD/VSSS	IDIODE	-	-	100	µA	-
SID69A	Maximum total source or Sink chip current	ITOT_GPIO	-	-	200	mA	-

(table continues...)

Table 12 (continued) GPIO

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
GPIO AC specifications							
SID70	Rise time in Fast Strong mode. 10% to 90% of VDDD	TRISEF	-	-	5.5	ns	Cload = 15 pF, 8 mA drive strength, VDDIO <= 2.7 V
SID70A	Rise time in Fast Strong mode. 10% to 90% of VDDD	TRISEF_1	-	-	3.5	ns	Cload = 15 pF, 8 mA drive strength 2.7 V < VDDIO <= 3.6 V
SID71	Fall time in Fast Strong mode. 10% to 90% of VDDD	TFALLF	-	-	5.5	ns	Cload = 15 pF, 8 mA drive strength, VDDIO <= 2.7 V
SID71A	Fall time in Fast Strong mode. 10% to 90% of VDDD	TFALLF_1	-	-	3.5	ns	Cload = 15 pF, 8 mA drive strength 2.7 V < VDDIO <= 3.6 V
SID72	Rise time in Slow Strong mode. 10% to 90% of VDDD	TRISES_1	-	-	14.4	ns	Cload = 15 pF, 8 mA drive strength, VDDIO <= 2.7 V
SID72A	Rise time in Slow Strong mode. 10% to 90% of VDDD	TRISES_2	-	-	7.2	ns	Cload = 15 pF, 8 mA drive strength, 2.7V < VDDIO <= 3.6
SID73	Fall time in Slow Strong mode. 10% to 90% of VDDD	TFALLS_1	-	-	14.4	ns	Cload = 15 pF, 8 mA drive strength, VDDIO <= 2.7 V
SID73A	Fall time in Slow Strong mode. 10% to 90% of VDDD	TFALLS_2	-	-	7.2	ns	Cload = 15 pF, 8 mA drive strength, 2.7 V < VDDIO <= 3.6 V
SID73G	Fall time (30% to 70% of VDDD) in Slow Strong mode	TFALL_I2C	20*VDDIO/5.5	-	250	ns	Cload = 10 pF to 400 pF, 8 mA drive strength
SID74	GPIO Fout. Fast Strong mode.	FGPIOUT1	-	-	80	MHz	90/10%, 15 pF load, 60/40 duty cycle
SID75	GPIO Fout; Slow Strong mode.	FGPIOUT2	-	-	16.7	MHz	90/10%, 15 pF load, 60/40 duty cycle
SID76	GPIO Fout; Fast Strong mode.	FGPIOUT3	-	-	7	MHz	90/10%, 25 pF load, 60/40 duty cycle

(table continues...)

Table 12 (continued) GPIO

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID245	GPIO Fout,Slow Strong mode.	FGPIOUT4	-	-	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	GPIO input operating frequency	FGPIOIN	-	-	100	MHz	90/10% Vio
PPCA							
SIDPPCA1	Execute both CM33 Active 200 MHz Dhrystone, PPCA active. OD mode	IDD8	-	25	-	mA	VCCD=1.2 V and VDDD=3.3 V
SIDPPCA2	All analog macro active inside PPCA	IDD8A	-	35	-	mA	VDDA=3.3 V

7.6 Analog subsystem

Table 13 Analog subsystem

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
Analog peripherals							
SIDAS	Leakage on AI0 and AI1 Pad	AIN_LEAK1	-	0.2	1	µA	Maximum leakage at 125°C. Guaranteed by design.
SIDAS2B	Leakage on AINxN and AINxP Pad (x =0-11)	AIN_LEAK2	-	0.2	1	µA	Maximum leakage at 125°C. Guaranteed by design.
SIDAS2	Input capacitance of DCSG	AIN_CAP_CSG	-	-	2.5	pF	Guaranteed by design.
SIDAS2A	Input capacitance of ADC	AIN_CAP_ADC	-	-	1.5	pF	Guaranteed by design.
SIDAS3	Total resistance on channel reaching DCSG	AIN_RES_CSGS	-	-	1800	Ω	Guaranteed by design.
SIDAS4	Total resistance of directly connected analog channel AI0/ AI1	AIN_RES_ADC1	-	-	3000	Ω	Guaranteed by design.
SIDAS4A	Total resistance of directly connected analog channel AI2-AI15	AIN_RES_ADC2	-	-	6000	Ω	Guaranteed by design.
SIDAS4B	Total resistance of directly connected analog channel AINxPIN	AIN_RES_ADC3	-	-	3000	Ω	Guaranteed by design.
SIDADC	External reference	VAREF_EXT	-	1.2	-	V	Precision of +/-1%

(table continues...)

Table 13 (continued) Analog subsystem

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SIDAS4C	Total resistance of analog channel AIN3PIN and AIN11PIN through AMUX	AIN_RES_ADC4	-	-	3000	Ω	Guaranteed by design.
SIDAS9	Input voltage range at the pin	A_VINS	–0.25	-	VDDA+0.25	V	Max input allowed on the pin dependent on VDDA.

7.7 LPComp

Table 14 LPComp

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
LPComparator DC specifications							
SID84	Input offset voltage for COMP1. Normal power mode.	VOFFSET1	–10	-	10	mV	-
SID85A	Input offset voltage. Low-power mode.	VOFFSET2	–25	+/-12	25	mV	-
SID85B	Input offset voltage. Ultra low-power mode.	VOFFSET3	–25	+/-12	25	mV	-
SID86	Hysteresis when enabled in Normal mode	VHYST1	-	-	60	mV	-
SID86A	Hysteresis when enabled in Low-power mode	VHYST2	-	-	80	mV	-
SID87	Input common mode voltage in Normal mode	VICM1	0.1	-	VDDIO1-0.1	V	-
SID247	Input common mode voltage in Low power mode	VICM2	0.1	-	VDDIO1-0.1	V	-
SID247A	Input common mode voltage in Ultra low power mode	VICM3	0.1	-	VDDIO1-0.1	V	-
SID88	Common mode rejection ratio in Normal power mode	CMRR	42	-	-	dB	-
SID89	Block Current, Normal mode	ICMP1	-	-	150	µA	-
SID248	Block Current, Low power mode	ICMP2	-	-	10	µA	-
SID249	Block Current in Ultra low-power mode	ICMP3	-	0.3	0.85	µA	-
SID90	DC Input impedance of comparator	ZCMP	35	-	-	MΩ	-
LPComparator AC specifications							
SID91	Response time, Normal mode, 100 mV overdrive	TRESP1	-	-	100	ns	-

(table continues...)

Table 14 (continued) LPComp

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID258	Response time, Low power mode, 100 mV overdrive	TRESP2	-	-	1000	ns	-
SID92	Response time, Ultra-low power mode, 100 mV overdrive	TRESP3	-	-	20	µs	-
SID92E	Time from Enabling to operation	T_CMP_EN1	-	-	10	µs	Normal and Low-power modes. Guaranteed by design.
SID92F	Time from Enabling to operation	T_CMP_EN2	-	-	50	µs	Ultra low-power mode. Guaranteed by design.

7.8 ATOP subsystem

Table 15 ATOP subsystem

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
DCSG DC specifications							
SIDDCSG	Reference voltage for DAC	DAC_REF	-	1.2	-	V	Internal 1.2 V reference or VAREF_EXT
SIDDCSG.0	Input referred residual offset for A vs B mode	VOFFSET	–6	-	6	mV	Hysteresis of +/-16 LSB and denounce of 3 clocks cycles.
SIDDCSG.1	Input common mode voltage for differential input	VCMR	–0.2	-	0.2	V	-
SIDDCSG.1A	Input common mode voltage for single ended input	VCMRA	0	-	3.3	V	-
SIDDCSG.2	Operating current on VDDA at 200 MHz	IVDDA	-	-	600	µA	Includes comparator, DAC on VDDA and all internal blocks. Only one instance of DCSG.
SIDDCSG.2A	Operating current on VCCD at 200 MHz	IVCCD	-	-	100	µA	Only for one instance of DCSG, Guaranteed by design.

(table continues...)

Table 15 (continued) ATOP subsystem

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SIDDCSG.3	DCSG response time	TRES	-	-	2	Clock Cycle	No update on DAC threshold setting. Result is out within clock cycle. Guaranteed by design.
SIDDCSG.4	Integral non-linearity	INL	–2	-	2	LSB	LSB referred to 12-bit with full scale LSB at 1.2 V.
SIDDCSG.5	Differential non -linearity	DNL	–1	-	1	LSB	LSB referred to 12-bit with full scale LSB at 1.2 V.
SIDDCSG.6	Start Up time after stable supply	STARTTIME	-	-	50	µs	-
SIDDCSG.7	DAC resolution	resolution	-	12	-	bits	-
SIDDCSG.8	DAC monotonicity	MONOTONIC	-	10	-	bits	-
SIDDCSG.9	Residual gain after calibration	GAINERRDCSG	–1	-	1	%	Reference supply with precision of +/-0.5%
SIDDCSG.11	Input voltage range for differential input	DCSG_VINS_DIF	–0.2	-	0.2	V	For VDDA≥ 3.3 V output saturates at input = 3.3 V and for VDDA <3.3 V, output does not reach full code range up to 4096.
DCSG AC specifications							
SIDCSG.10	DAC settling accuracy for 511 LSB change	DACSET	–8	-	8	LSB	Referred to 12-bit with settling time of 20 ns. Guaranteed by design.
SIDCSG.10A	DAC settling accuracy for 4095 LSB change	DACSETA	–8	-	8	LSB	Referred to 12-bit with settling time of 20 ns. Guaranteed by design.
SIDCSG.10B	DAC settling accuracy for 4095 LSB change	DACSETB	–4	-	4	LSB	Referred to 12-bit with settling time of 50 ns. Guaranteed by design.

(table continues...)

Table 15 (continued) ATOP subsystem

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SIDCSG.12	DAC blanking time if the DAC word is not changed for 50 µs	DAC_BLANKING	-	-	50	ns	DAC refresh to the programmed word is needed if DCSG DAC word does not change in 50 µs. Guaranteed by design.
12-bit ADC DC specifications							
SIDADC.0	ADC resolution	RES	-	-	12	bits	-
SIDADC.3	Gain error at gain =1 after calibration using internal reference	GAINERR1	–1	-	1	%	-
SIDADC.4A	Offset error after calibration	OFFSETERR	–4	-	4	LSB	Input referred offset referred to full scale LSB at 3.3 V.
SIDADC.6	Integral non-linearity	A_INL	–3	-	3	LSB	Using VAREF
SIDADC.7	Differential non-linearity	A_DNL	-1	-	2	LSB	Using VAREF on non-trimmed parts
SIDADC.8	Current consumption	A_ISAR_1	-	-	10	mA	Max current consumption for ADC with AFE in max BW mode.
SIDADC.9A	Input voltage range for differential input	A_VINS_DIF	–3.3	-	3.3	V	For VDDA≥ 3.3 V output saturates at input = 3.3 Vt.
SIDADC.9B	Input voltage range for single ended input	A_VINS_SE	0	-	3.3	V	For VDDA≥ 3.3 V output saturates at input = 3.3 V.
12-bit ADC AC specifications							
SIDADC.13	Inter-channel crosstalk for ADC (differential ended)	CROSSTALK_1	–2	-	2	LSB	LSB referred to full-scale input at 3.3 V for fADC = 100 MHz for differential ended
SIDADC.13A	Inter-channel crosstalk for ADC (single ended)	CROSSTALK_2	–4	-	4	LSB	LSB referred to full-scale input at 3.3V for fADC = 100 MHz for single ended

(table continues...)

Table 15 (continued) ATOP subsystem

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SIDADC.14	Sample rate	A_SAMP_1	-	-	25	Msps	Includes min 1 clock cycle sampling + 3 cycle conversion at 100 MHz
SIDADC.16	Effective number of bits	A_ENOB	10	-	-	bit	Calculated out of SNR.
SIDADC.17	Start up time after stable supply	T_STARTUP	-	-	100	us	at ADC clock = 100 MHz
SIDADC.19	Minimum sampling time for analog input through analog pad direct connection to S/H	T_SAMPLE	1	-	-	cycles	Referred to fADC, max fADC = 100 MHz
SIDADC.19B	Minimum sampling time for analog input through analog pad connected to S/H via AROUTE (AMUX)	T_SAMPLE_AROUTE	4	-	-	cycles	Referred to fADC, max fADC = 100 MHz
SIDADC.19C	Minimum sampling time for analog input through GPIO or ADFT connected to S/H via AROUTE (AMUX)	T_SAMPLE_GPIO	10	-	-	cycles	Referred to fADC, max fADC = 100 MHz
AFE specification							
SIDAFE.1	Input Signal frequency for Gain = 33 and 66 setting	AIN_FREQ_LBW	-	-	100	kHz	Current consumption of AFE = 1 mA
SIDAFE.1A	Input Signal frequency for Gain = 8.25 and 16.5 setting, high power	AIN_FREQ_HBWA	-	-	10000	kHz	Current consumption of AFE = 9 mA
SIDAFE.1B	Input Signal frequency for Gain = 8.25 and 16.5 setting, medium power	AIN_FREQ_HBWB	-	-	5000	kHz	Current consumption of AFE = 3 mA
SIDAFE.1C	Input Signal frequency for Gain = 8.25 and 16.5 setting, low power	AIN_FREQ_HBWC	-	-	2500	kHz	Current consumption of AFE = 1.5 mA
SIDAFE.2	Sample rate for low bandwidth for gain =33 and 66	AFE_SAMP_LBW	-	-	3.125	MSPS	Current consumption of AFE = 1 mA
SIDAFE.2A	Sample rate for high bandwidth (10 MHz) for gain =8.25 and 16.5	AFE_SAMP_HBWA	-	-	25	MSPS	Current consumption of AFE = 9 mA
SIDAFE.2B	Sample rate for high bandwidth (5 MHz) for gain =8.25 and 16.5	AFE_SAMP_HBWB	-	-	12.5	MSPS	Current consumption of AFE = 3 mA
SIDAFE.2C	Sample rate for high bandwidth (2.5 MHz) for gain = 8.25 and 16.5	AFE_SAMP_HBWC	-	-	6.25	MSPS	Current consumption of AFE = 1.5 mA

(table continues...)

Table 15 (continued) ATOP subsystem

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SIDAFE.3	Differential input voltage for Gain = 66	AFE_VINS_DIF64	–50	-	50	mV	-
SIDAFE.4	Differential input voltage for Gain = 33	AFE_VINS_DIF32	–100	-	100	mV	-
SIDAFE.5	Gain error	AFE_GAINERR	-	-	6	%	Untrimmed for AIN_FREQ<= Max Frequency and full scale output voltage
SIDAFE.6	Gain error for DC input	AFE_GAINERR_DC	-	-	2	%	For DC input
SIDAFE.7	Spurious Free Dynamic Range (all gain settings), only AFE	AFE_SFDR	-	-	–40	dB	-
R2R DAC specification							
SIDR2R.1	DAC resolution	Resolution	-	12	-	bits	Resolution
SIDR2R.2	Gain error	GAINERR	–1	-	1	%	Post Calibration
SIDR2R.3	DNL of R2R DAC	R_DNL	–1	-	1	LSB	LSB referred to 10-bit
SIDR2R.4	INL of R2R DAC	R_INL	–2	-	2	LSB	LSB referred to 10-bit
SIDR2R.5	Full scale range of R2R DAC in Config 2	R_FULLSCALE	VSSA	-	VDDA	V	Can not be used with the Buffer and only on AI0
SIDR2R.5A	Full scale range of R2R DAC in Config 3	R_FULLSCALEA	VSSA	-	1.2	V	Can not be used with the Buffer and only on AI0
SIDR2R.5B	Full scale range of R2R DAC	R_FULLSCALEB	-VDDA	-	VDDA	V	Can not be used with the Buffer and only on AI0/AI1
SIDR2R.5D	Full scale range of R2R DAC in Config 1	R_FULLSCALED	VSSA	-	0.5*VDDA	V	Can not be used with the Buffer and only on AI0/AI1
SIDR2R.6	DAC settling time for transition between minimum code to maximum or vice-versa via the output buffer	RDAC_SET	-	-	500	ns	Guaranteed by design.

(table continues...)

Table 15 (continued) ATOP subsystem

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SIDR2R.6A	DAC settling time for transition between minimum code to maximum or vice-versa via AI0 and AI1	RDAC_SETA	-	-	15	µs	With bench capacitance loading of less than 30 pF. Internal capacitance loading of 10 pF.
SIDR2R.6B	DAC settling time for transition between minimum code to maximum or vice-versa via AI0 and AI1	RDAC_SETB	-	-	13	µs	With bench capacitance loading of less than 15 pF. Internal capacitance loading of 10 pF.
SIDR2R.6C	DAC settling time for transition between minimum code to maximum or vice-versa via AI0 and AI1	RDAC_SETC	-	-	10	µs	With bench capacitance loading of less than 5 pF. Internal capacitance loading of 10 pF.
SIDR2R.7	Current consumption	R_IDAC	-	-	300	µA	Maximum current at 125℃ temperature.
R2R DAC buffer specification							
SIDR2RB.1	Input range supported by Buffer	INPUT_RANGE	0.1	-	1.2	V	Input range is a function of selection on R2R DAC
SIDR2RB.2	Output range supported by Buffer	OUTPUT_RANGE	0.1	-	0.5*VDDA	V	-
SIDR2RB.3	Buffer settling from 0.1 V to VDDA/2	BUF_SET	-	-	500	ns	-
SIDR2RB.4	Offset error without calibration	OFFSET_NOCAL	–10	-	10	mV	-
SIDR2RB.5	Offset error after calibration	OFFSET	–4	-	4	mV	-
SIDR2RB.6	Current consumption	IBUF	-	-	500	µA	-
IDAC specification							
SIDAC.1	IDAC output current	IIDAC	9	10	11	µA	Guaranteed by design.
Temperature sensor specifications							
SID93	Temperature sensor accuracy	TSENSACC	–5	-	5	°C	–40 to +125 C
Internal reference specifications							
SID93R	Internal bandgap reference	VREFBG	1.194	1.2	1.206	V	Accuracy of +/-0.5%

7.9 HRPWM specifications

Table 16 HRPWM specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
HRPWM specifications							
SIDHRPWM.1	HRPWM resolution	HR_RES	-	(1)/ (Fc*64)	-	ps	Max Fc = 200 MHz, resulting in typical resolution = 78.1 ps. When HRPWM feature is enabled, prescalar is not allowed to be used in PERI as well as in TCPWM Counter
SIDHRPWM.2	HRPWM is monotonic	MONOTONIC	-	Yes	-	-	HRPWM Monotonicity is guaranteed by BIST/Built-in self Test)

7.10 TCPWM specifications

Table 17 TCPWM specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
TCPWM specifications							
SID.TCPWM.2B	Block current consumption at 100 MHz	ITCPWM4	-	-	6100	µA	All modes (Timer/ Counter/PWM)
SID.TCPWM.2C	Block current consumption at 200 MHz	ITCPWM4	-	-	7000	µA	All modes (Timer/ Counter/PWM)
SID.TCPWM.3	Operating frequency (Fc)	TCPWMFREQ	-	-	200	MHz	Fc max = 200 MHz
SID.TCPWM.4	Input trigger pulse width for all trigger events	TPWMENEXT	2/Fc	-	-	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

(table continues...)

Table 17 (continued) TCPWM specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID.TCPWM.5	Output trigger pulse widths	TPWMEXT	1.5/Fc	-	-	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	Resolution of Counter	TCRES	1/Fc	-	-	ns	Minimum time between successive counts at VDDD=3.3 V
SID.TCPWM.5B	PWM resolution	PWMRES	1/Fc	-	-	ns	Minimum pulse width of PWM Output at VDDD=3.3 V

7.11 SCB

Table 18 SCB

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
Fixed I^2C DC specifications							
SID149	Block current consumption at 100 kHz	II2C1	-	-	30	µA	Guaranteed by design.
SID150	Block current consumption at 400 kHz	II2C2	-	-	80	µA	Guaranteed by design.
SID151	Block current consumption at 1 Mbps	II2C3	-	-	180	µA	Guaranteed by design.
SID152	I^2C enabled in Deep Sleep mode	II2C4	-	-	1,7	µA	At 60 C. Guaranteed by design.
SMBUS specifications							
SID.SMBUS1	Detect low clock timeout	T_TIMEOUT1	25	-	35	ms	At 100 kHz
SID.SMBUS2	Detect low clock timeout	T_TIMEOUT2	25	-	35	ms	1
SID.SMBUS3	Detect low clock timeout	T_TIMEOUT3	25	-	35	ms	At 1 MHz
Fixed I^2C AC specifications							
SID153	Bit rate	FI2C1	-	-	1	Mbps	-

(table continues...)

Table 18 (continued) SCB

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
Fixed UART DC Specifications							
SID160	Block current consumption at 100 Kbps	IUART1	-	-	30	µA	Guaranteed by design.
SID161	Block current consumption at 1000 Kbps	IUART2	-	-	180	µA	Guaranteed by design.
Fixed UART AC specifications							
SID162A	Bit rate	FUART1	-	-	3	Mbps	ULP mode
SID162B	Bit rate	FUART2	-	-	8	Mbps	LP mode
Fixed SPI DC specifications							
SID163	Block current consumption at 1 Mbps	ISPI1	-	-	220	µA	Guaranteed by design.
SID164	Block current consumption at 4 Mbps	ISPI2	-	-	340	µA	Guaranteed by design.
SID165	Block current consumption at 8 Mbps	ISPI3	-	-	360	µA	Guaranteed by design.
SID165A	Block current consumption at 25 Mbps	ISPI4	-	-	800	µA	Guaranteed by design.
Fixed SPI AC specifications for LP mode (1.1 V), OD, MF and ULP modes unless noted otherwise							
SID166	SPI operating frequency master and externally clocked slave in LP and OD mode	FSPI_EXT	-	-	25	MHz	For LP, OD mode
SID166U	SPI operating frequency master and externally clocked slave in ULP mode	FSPI_EXT_UL	-	-	6,25	MHz	For ULP mode
SID166A	SPI operating frequency master and externally clocked slave in high speed mode in LP and OD mode	FSPI_EXT_HS	37,5	-	50	MHz	Min. Is for LP mode, Max. Is for OD mode.
SID166AU	SPI operating frequency master and externally clocked slave in high speed mode in ULP mode	FSPI_EXT_HS_UL	12,5	-	17,5	MHz	Min. Is for ULP mode , Max. Is for MF mode
SID166B	SPI operating frequency master in LP and OD mode	FSPI	-	-	FSCB/4	MHz	LP,and OD mode, FSCB = 100 MHz
SID166BU	SPI operating frequency master in MF and ULP mode	FSPI_UL	-	-	FSCB/4	MHz	MF and ULP mode, FSCB = 25 MHz
SID166BHS	SPI operating frequency master in high speed mode in LP and OD	FSPI_HS	-	-	FSCB/4	MHz	LP/OD mode, FSCB = 150/200 MHz

(table continues...)

Table 18 (continued) SCB

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID166BHS_UL	SPI operating frequency master in high speed mode in MF and ULP	FSPI_HS_UL	-	-	FSCB/4	MHz	ULP mode, FSCB = 50 MHz, MF mode FSCB=70 MHz
SID166C	SPI slave internally clocked in MF and ULP	FSPI_IC	-	-	4	MHz	ULP/MF modes with FSCB = 25 MHz
SID166C_OD	SPI slave internally clocked in LP and OD	FSPI_IC_OD	-	-	12,5	MHz	LP/OD modes with FSCB = 100 MHz
SID166C_HS	SPI slave internally clocked in in High-Speed mode in MF and ULP	FSPI_IC_HS	7	-	9	MHz	Min at ULP mode FSCB = 50 MHz and Max. at MF mode FSCB=70 MHz
SID166C_HS_OD	SPI slave internally clocked in in High-Speed mode in LP and OD	FSPI_IC_HS_OD	17	-	25	MHz	Min. at LP mode, FSCB = 150 MHz and Max. at OD mode, FSCB = 200 MHz
Fixed SPI master mode AC specifications for LP (1.1 V), OD, MF and ULP modes unless noted otherwise							
SID167_A	SCB clock period	TSCB	-	-	1/FSCB	ns	FSCB depends on choice of standard or HS mode as well different power modes
SID167_B	SPI clock period	TSPI	-	-	1/FSPI	ns	FSPI depends on choice of standard or HS SPI mode as well different power modes
SID167	MOSI valid after Sclock driving edge	TDMO	-	-	10	ns	LP, OD mode
SID167UL	MOSI valid after Sclock driving edge	TDMO_UL	-	-	40	ns	ULP and MF mode
SID167HS	MOSI valid after Sclock driving edge	TDMO_HS	5	-	7	ns	Max. Is OD mode and Min. is LP mode
SID167HS_UL	MOSI valid after Sclock driving edge	TDMO_HS_UL	14	-	20	ns	Max. Is ULP mode and Min. is MF mode
SID168	MISO valid before Sclock capturing edge	TDSI	20	-	-	ns	LP, OD Full clock, late MISO sampling

(table continues...)

Table 18 (continued) SCB

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID168_ULP	MISO valid before Sclock capturing edge	TDSI_ULP	105	-	-	ns	ULP and MF mode, Full clock, late MISO sampling
SID168HS	MISO valid before Sclock capturing edge for LP mode	TDSI_HS	15	-	-	ns	-
SID168HS_OD	MISO valid before Sclock capturing edge for OD mode	TDSI_HS_OD	10	-	-	ns	OD mode, for 50 MHz operation at VDDIO(max)
SID168HS_ULP	MISO valid before Sclock capturing edge	TDSI_HS_UL	22	-	-	ns	ULP mode, for 50 MHz operation
SID169	MOSI data hold time	THMO	0	-	-	ns	Referred to Slave capturing edge in LP and OD mode
SID169_UL	MOSI data hold time	THMO_UL	0	-	-	ns	Referred to Slave capturing edge in ULP and MF mode
SID169HS	MOSI data hold time in HS mode	THMO_HS	0	-	-	ns	Referred to Slave capturing edge for HS SPI in LP and OD mode
SID169HS_UL	MOSI data hold time	THMO_HS_UL	0	-	-	ns	Referred to Slave capturing edge for HS SPI in ULP and MF mode
SID169A	SSEL Valid to first SCK Valid edge	TSSELMSCK1	1/4*TSCB	-	-	ns	Referred to Master clock edge for all modes and SPI and HS SPI
SID169B	SSEL Hold after last SCK Valid edge	TSSELMCK2	1/4*TSPI	-	-	ns	Referred to Master clock edge for all modes and SPI and HS SPI
Fixed SPI slave mode AC specifications for LP mode (1.1 V), OD, MF and ULP modes unless noted otherwise							
SID170	MOSI valid before Sclock capturing edge	TDMI	5	-	-	ns	LP, OD mode
SID170_UL	MOSI valid before Sclock capturing edge	TDMI_UL	24	-	-	ns	MF and ULP mode
SID170_HS	MOSI valid before Sclock capturing edge	TDMI_HS	2,5	-	-	ns	LP, OD mode, for 50 MHz operation
SID170_HS_UL	MOSI valid before Sclock capturing edge	TDMI_HS_UL	5	-	-	ns	ULP, MF mode, for 50 MHz operation

(table continues...)

Table 18 (continued) SCB

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID171A	MISO valid after Sclock driving edge in Ext. Clk. mode	TDSO_EXT	-	-	20	ns	LP, OD mode
SID171A_UL	MISO valid after Sclock driving edge in Ext. Clk. mode	TDSO_EXT_UL	-	-	35	ns	MF and ULP mode
SID171A_HS	MISO valid after Sclock driving edge in Ext. Clk. mode	TDSO_EXT_HS	-	-	16	ns	LP for 50 MHz operation
SID171A_HS_OD	MISO valid after Sclock driving edge in Ext. Clk. mode	TDSO_EXT_HS_OD	-	-	10	ns	OD mode, for 50 MHz operation with 10 pf load at VDDIO(max)
SID171A_HS_UL	MISO valid after Sclock driving edge in Ext. Clk. mode	TDSO_EXT_HS_UL	-	-	25	ns	ULP , MF mode, for 50 MHz operation
SID171	MISO valid after Sclock driving edge in Internally Clk. mode	TDSO	-	-	TDSO_EXT + 2*Tscb	ns	Tscb is serial communication block clock period.
SID171B	MISO valid after Sclock driving edge in Internally Clk. mode with Median filter enabled.	TDSO_M	-	-	TDSO_EXT + 3*Tscb	ns	Tscb is serial communication block clock period.
SID172	MOSI and MISO data hold time	THSO	5	-	-	ns	ULP, MF, LP and OD mode. Both for standard and HS SPI
SID172A	SSEL valid to first SCK Valid edge	TSSELSCK1	4*Tscb	-	-	ns	SPI Slave internally clocked mode
SID172B	SSEL hold after Last SCK Valid edge	TSSELSCK2	4*Tscb	-	-	ns	SPI Slave internally clocked mode
SID172C	MISO valid after SSEL falling edge	TVSS_EXT	-	-	20	ns	For LP and OD mode
SID172C_ULP	MISO valid after SSEL falling edge	TVSS_EXT_ULP	-	-	35	ns	For ULP and MF mode
SID172C_HS	MISO valid after SSEL falling edge	TVSS_EXT_HS	-	-	18	ns	High-Speed SPI, LP mode
SID172C_HS_OD	MISO valid after SSEL falling edge	TVSS_EXT_HS_OD	-	-	12	ns	High-Speed SPI, OD mode
SID172C_HS_UL	MISO valid after SSEL falling edge	TVSS_EXT_HS_UL	-	25	27	ns	High-Speed SPI, typical value for MF mode and max value at ULP mode.

7.12 Memory

Table 19 Memory

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
Flash DC specifications							
SID173	Erase and program voltage	VPE	1.71	-	3.63	V	Erase and program not supported at ULP levels (0.9 V)
SID173A	Erase and program current	IPE	-	-	6	mA	-
Flash AC specifications							
SID174	Row (Block) write time (Erase and program)	TROWWRITE	-	-	16	ms	Row (Block) = 512 bytes
SID175	Row erase time	TROWERASE	-	-	11	ms	-
SID176	Row program time after erase	TROWPROGRAM	-	-	5	ms	-
SID180	Total device program time	TDEVPROG	-	-	5.2	seconds	-
SID181	Flash endurance	FEND	100K	-	-	cycles	-
SID182	Flash retention. Ta<= 25 C, 100K P/E cycles	FRET1	10	-	-	years	-
SID182A	Flash retention. Ta<= 85 C, 10K P/E cycles	FRET2	10	-	-	years	-
SID182B	Flash retention. Ta<= 55 C, 20K P/E cycles	FRET3	20	-	-	years	-
SID256	Number of wait states at 180 MHz	TWS180	-	-	9	-	OD mode (1.2 V)
SID256A	Number of wait states at 150 MHz	TWS150	-	-	8	-	LP mode (1.1 V)
SID256B	Number of wait states at 70 MHz	TWS70	-	-	5	-	MF mode (1.0 V)
SID256C	Number of wait states at 50 MHz	TWS50	-	-	4	-	ULP mode (0.9 V)

7.13 POR

Table 20 POR

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
System resources							
Power-on-reset with brownout DC specifications							
SID190	BOD trip voltage in Active and Sleep modes. VDDD.	VFALLPPOR	1.54	-	-	V	BOD reset guaranteed for levels below 1.54V

(table continues...)

Table 20 (continued) POR

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID192	BOD trip voltage in Deep Sleep. VDDD	VFALLDPSLP	1.54	-	-	V	-
SID192A	Maximum power supply ramp rate (any supply)	VDDRAMP	-	-	100	mV/µs	Active mode
POR with brownout AC specification							
SID194A	Maximum power supply ramp rate (any supply) in Deep Sleep	VDDRAMP_DS	-	-	10	mV/µs	BOD operation guaranteed

7.14 Voltage monitors

Table 21 Voltage monitors

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
Voltage monitors DC specifications							
SID196	BOD voltage threshold	VHVDI2	1.57	1.63	1.75	V	-
SID197	BOD voltage threshold	VHVDI3	1.76	1.83	1.89	V	-
SID198	BOD voltage threshold	VHVDI4	1.95	2.03	2.10	V	-
SID199	BOD voltage threshold	VHVDI5	2.05	2.13	2.20	V	-
SID200	BOD voltage threshold	VHVDI6	2.15	2.23	2.30	V	-
SID201	BOD voltage threshold	VHVDI7	2.24	2.33	2.41	V	-
SID202	BOD voltage threshold	VHVDI8	2.34	2.43	2.51	V	-
SID203	BOD voltage threshold	VHVDI9	2.44	2.53	2.61	V	-
SID204	BOD voltage threshold	VHVDI10	2.53	2.63	2.72	V	-
SID205	BOD voltage threshold	VHVDI11	2.63	2.73	2.82	V	-
SID206	BOD voltage threshold	VHVDI12	2.73	2.83	2.92	V	-
SID207	BOD voltage threshold	VHVDI13	2.82	2.93	3.03	V	-
SID208	BOD voltage threshold	VHVDI14	2.92	3.03	3.13	V	-
SID209	BOD voltage threshold	VHVDI15	3.02	3.13	3.23	V	-
SID211	Block current	LVI_IDD	-	5	15	µA	-

7.15 SWD and trace interface

Table 22 SWD and trace interface

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID214	Single wire debug clock in OD mode	F_SWDCLK2	-	-	25	MHz	OD mode; VCCD = 1.2 V and 1.71 V <= VDDD <= 3.6 V

(table continues...)

Table 22 (continued) SWD and trace interface

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID214LP	Single wire debug clock in LP mode	F_SWDCLK2A	-	-	20	MHz	LP mode; VCCD = 1.1 V and 1.71 V <= VDDD <= 3.6 V
SID214L	Single wire debug clock in MF/ULP mode	F_SWDCLK2L	-	-	12	MHz	ULP and MF mode. VCCD = 0.9/1.0 V and 1.71 V <= VDDD <= 3.6 V
SID215	Single wire debug input setup time	T_SWDI_SETUP	0.25*T	-	-	ns	T = 1/f SWDCLK
SID216	Single wire debug input hold time	T_SWDI_HOLD	0.25*T	-	-	ns	T = 1/f SWDCLK
SID217	Single wire debug output valid time	T_SWDO_VALID	-	-	0.5*T	ns	T = 1/f SWDCLK
SID217A	Single wire debug output hold time	T_SWDO_HOLD	1	-	-	ns	T = 1/f SWDCLK
SID214T	With trace data setup/hold times of 2/1 ns respectively	F_TRCLK_LP1	-	-	90	MHz	OD mode. VCCD = 1.2 V with load capacitance =15 pF
SID215T	With trace data setup/hold times of 2/1 ns respectively	F_TRCLK_LP2	-	-	75	MHz	LP mode. VCCD = 1.1 V with load capacitance =15 pF
SID216T	With trace data setup/hold times of 3/2 ns respectively	F_TRCLK_LP2	-	-	50	MHz	MF mode. VCCD = 1.0 V with load capacitance =15 pF
SID217T	With trace data setup/hold times of 3/2 ns respectively	F_TRCLK_ULP	-	-	25	MHz	ULP mode. VCCD = 0.9 V with load capacitance =15 pF

7.16 Internal oscillator, crystal oscillator, and external clock specifications

Table 23 Internal oscillator, crystal oscillator, and external clock specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
IMO DC specification							
SID218	IMO operating current at 8 MHz	IIMO1	-	9	15	µA	Guaranteed by design.

(table continues...)

Table 23 (continued) Internal oscillator, crystal oscillator, and external clock specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
IMO AC specifications							
SID223	Frequency variation centered on 8 MHz	FIMOTOL1	-	-	±2	%	-
SID227	Cycle-to-cycle and Period jitter	TJITR	-	250	-	ps	-
IHO DC specifications							
SID218A	IHO Operating current at 48 MHz	IIHO1	-	80	100	µA	Guaranteed by design.
IHO AC specifications							
SID223A	Frequency variation centered on 48 MHz	FIHOTOL1	-	-	±1	%	-
SID227A	Cycle-to-cycle and Period jitter	TJITR	-	60	-	ps	-
ILO DC specifications							
SID231	ILO Operating current at 32 kHz	IILO2	-	0.3	0.7	µA	Guaranteed by design.
ILO AC specifications							
SID234	ILO Start-up time	TSTARTILO1	-	-	7	uS	Startup time to 95% of final frequency
SID236	ILO Duty cycle	TILODUTY	45	50	55	%	-
SID237	32 kHz trimmed frequency	FILOTRIM1	28.8	32	35.2	kHz	+/-10% variation
Frequency-locked loop (FLL) specifications							
SID450	Input frequency range.	FLL_RANGE	0.008	-	100	MHz	-
SID451	Output frequency range. VCCD = 1.1V	FLL_OUT_DIV2	24.00	-	100.00	MHz	Output range of FLL divided-by-2 output
SID451A	Output frequency range. VCCD = 0.9V	FLL_OUT_DIV2	24.00	-	50.00	MHz	Output range of FLL divided-by-2 output
SID452	Divided-by-2 output; High or Low	FLL_DUTY_DIV2	47.00	-	53.00	%	Guaranteed by design.
SID454	Time from stable input clock to 1% of final value on deep sleep wakeup	FLL_WAKEUP	-	-	7.50	uS	With IMO input, for < 10 C change in temperature while in Deep Sleep and Fout ≥ 50 MHz
SID455	Period jitter (1 sigma) at 100 MHz	FLL_JITTER	-	-	35	pS	50 ps at 48 MHz, 35 pS at 100 MHz. Guaranteed by design

(table continues...)

Table 23 (continued) Internal oscillator, crystal oscillator, and external clock specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID456	Overall current	FLL_CURRENT	-	-	3,6	uA/MHz	FLL_Out=100 MHz with VCCD=1.1
MHz ECO DC specifications							
SID316	Block operating current with Cload up to 18 pF.	Idd_MHz	-	800	1600	µA	Max at 33 MHz. Typ at 16 MHz.
MHz ECO AC specifications							
SID317	Crystal frequency range	F_MHz	4	-	36	MHz	-
External clock specifications							
SID_EXT	External clock max input frequency	FEXT	-	-	80	MHz	In OD and LP mode, duty cycle between 45% and 55% and max rise/fall time of 20% period
SID_EXT1	External clock max input frequency in MF mode	FEXT_MF	-	-	50	MHz	In MF mode, duty cycle between 45% and 55% and max rise/fall time of 20% period
SID_EXT2	External clock max input frequency in ULP mode	FEXT_ULP	-	-	40	MHz	In ULP mode, duty cycle between 45% and 55% and max rise/fall time of 20% period
kHz WCO DC specifications							
SID318	Block operating current with 32 kHz crystal	Idd_kHz	-	0.38	1	µA	-
SID321E	Equivalent Series Resistance	ESR32K	-	80	-	kΩ	-
SID322E	Drive Level	PD32K	-	-	1	µW	-
kHz WCO AC specifications							
SID319	32 kHz trimmed frequency	F_kHz	-	32.768	-	kHz	-
SID320K	Startup time	Ton_kHz	-	-	1000	ms	-
SID320E	Frequency tolerance	FTOL32K	-	50	250	ppm	May be calibrated to sub-10 ppm levels
DPLL specifications							
SIDPLL.0	Time to achieve PLL Lock at 4 MHz reference	PLL_LOCK_4M	-	-	20	µS	
SIDPLL.1	Time to achieve PLL Lock at 8 MHz reference	PLL_LOCK_8M	-	-	20	µS	

(table continues...)

Table 23 (continued) Internal oscillator, crystal oscillator, and external clock specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SIDPLL.2	Output frequency from PLL Block	PLL_OUT	-	160	240	MHz	
SIDPLL.3	PLL current	PLL_IDD	-	700	1000	uA	For PLL_OUT = 200 MHz. Guaranteed by design.
SIDPLL.4	Period jitter	PLL_PJTR_100	-200	-	200	pS	for PLL_OUT = 100 MHz. Guaranteed by design.
SIDPLL.4A	Period jitter	PLL_PJTR_200	-100	-	100	pS	for PLL_OUT = 200 MHz. Guaranteed by design.
SIDPLL.7	Duty cycle	PLL_DC	45	-	55	%	for PLL_OUT = Fdco/N , N >1 and integer

7.17 JTAG boundary scan specifications

Table 24 JTAG boundary scan specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
JTAG: Parameters for 1.1 V (LP) and 1.2 V (OD) mode operations							
SID460	TCK low minimum	TCKLOW	33	-	-	ns	-
SID461	TCK high	TCKHIGH	11	-	-	ns	-
SID461A	Clock period , 30 pF Load	TCK_PERIOD	-	44	-	ns	-
SID462	TDO clock-to-out (max) from falling TCK	TCK_TDO	-	-	22	ns	-
SID463	TDI, TMS setup time before rising TCK.	TSU_TCK	12	-	-	ns	-
SID464	TDI, TMS hold time after rising TCK.	TCK_TDO	10	-	-	ns	-
SID465	TCK to TDO data valid (High-Z to Active).	TCK_TDOV	22	-	-	ns	-
SID466	TCK to TDO data valid (Active to High-Z).	TCK_TDOZ	22	-	-	ns	-
SID467	JTAG TDO hold Time	JTAG_TDO_HOLD	-	-	5	ns	-
SID467A	JTAG Input Transition Time	JTAG_INPUT_TRANSITION_TIME	-	-	5	ns	-

(table continues...)

Table 24 (continued) JTAG boundary scan specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
JTAG: Parameters for 0.9 V (ULP) mode operations and 1.0 V (MF) mode operations							
SID483	TCK low Minimum	TCKLOW	60	-	-	ns	-
SID484	TCK high	TCKHIGH	20	-	-	ns	-
SID485	Clock Period , 30 pF Load	TCK_PERIOD	-	80	-	ns	-
SID486	TDO clock-to-out (max) from falling TCK	TCK_TDO	40	-	50	ns	Max is in ULP mode and Min is in MF mode
SID487	TDI, TMS setup time before rising TCK.	TSU_TCK	20	-	-	ns	-
SID488	TDI, TMS hold time after rising TCK.	TCK_THD	20	-	-	ns	-
SID489	TCK to TDO data valid (High-Z to Active).	TCK_TDOV	40	-	50	ns	Max is in ULP mode and Min is in MF mode
SID490	TCK to TDO data valid (Active to High-Z).	TCK_TDOZ	40	-	50	ns	Max is in ULP mode and Min is in MF mode
SID491	JTAG TDO hold Time	JTAG_TDO_HOLD	-	-	5	ns	-
SID492	JTAG Input Transition Time	JTAG_INPUT_TRANSITION_TIME	-	-	5	ns	-
JTAG Boundary Scan Parameters for 1.1 V (LP) and 1.2 V (OD) mode operation:							
SID468	TCK low	TCKLOW	51	-	-	ns	-
SID469	TCK high	TCKHIGH	11	-	-	ns	-
SID469A	CLK_JTAG_PERIOD, 30 pF Load	TCKPERIOD	-	62	-	ns	-
SID470	TCK falling edge to output valid	TCK_TDO	-	-	40	ns	-
SID471	Input valid to TCK rising edge	TSU_TCK	12	-	-	ns	-
SID472	Input hold time to TCK rising edge	TCK_TDO	10	-	-	ns	-
SID473	TCK falling edge to output valid (High-Z to Active).	TCK_TDOV	40	-	-	ns	-
SID474	TCK falling edge to output valid (Active to High-Z).	TCK_TDOZ	40	-	-	ns	-
SID474A	JTAG_BSCAN_TDO_HOLD	TCK_TDOH	-	-	5	ns	-
JTAG boundary scan parameters for 0.9 V (ULP) and 1.0 V (MF) mode operation:							
SID475	TCK low	TCKLOW	102	-	-	ns	-
SID476	TCK high	TCKHIGH	20	-	-	ns	-
SID476A	CLK_JTAG_PERIOD, 30 pF Load	TCKPERIOD	-	122	-	ns	-

(table continues...)

Table 24 (continued) JTAG boundary scan specifications

Spec ID	Parameter	Symbol	Values			Unit	Note or test condition
			Min.	Typ.	Max.		
SID478	TCK falling edge to output valid	TCK_TDO	-	-	80	ns	-
SID479	Input valid to TCK rising edge	TSU_TCK	20	-	-	ns	-
SID480	Input hold time to TCK rising edge	TCK_TDO	20	-	-	ns	-
SID481	TCK falling edge to output valid (High-Z to Active).	TCK_TDOV	80	-	-	ns	-
SID482	TCK falling edge to output valid (Active to High-Z).	TCK_TDOZ	80	-	-	ns	-

8 Ordering information

Table 25 lists the PSC3P8x device part numbers and features. All devices include an Arm® Cortex®-M33 with a 180 MHz CPU speed, a PPCA with two Arm® Cortex®-M33 processors running at 200 MHz, four 12-bit, 25 Msps SAR ADC modules with four AFE, 2-channel 16-bit TCPWM, 2-channel 32-bit TCPWM, 2-channel CAN FD, and CryptoLite functionality.

Table 25 Ordering information PSC3P8x

Product	Flash	SRAM	GPIO/Analog Inputs	PPCA TCPWM (includes 12 Ch HRPWM)	PPCA SRAM	DCSG Channels	Security (PSA Level)	SCB (UART, SPI, I²C)	Silicon ID	Pin
PSC3P8GFS3PAHQ1	512 KB	128 KB	60/40	26 Ch	112 KB	9	L3	7	0xEE86	E-LQFP-100
PSC3P8GFS3PAFQ1	512 KB	128 KB	45/33	26 Ch	112 KB	9	L3	7	0xEE87	E-LQFP-80
PSC3P8GFS3PACQ1	512 KB	128 KB	33/29	26 Ch	112 KB	6[1)]	L3	4[2)]	0xEE8A	E-LQFP-64
PSC3P8GFS3PLHQ1	512 KB	128 KB	34/29	26 Ch	112 KB	6 [1)]	L3	4 [2)]	0xEE8B	VQFN-64
PSC3P8FES2PLHQ1	256 KB	64 KB	34/29	26 Ch	96 KB[3)]	6 [1)]	L2	4 [2)]	0xEE8C	VQFN-64
PSC3P8GFS3PLGQ1	512 KB	128 KB	25/19	26 Ch	112 KB	6 [1)]	L3	3 [4)]	0xEE92	VQFN-48
PSC3P8FES2PLGQ1	256 KB	64 KB	25/19	26 Ch	96 KB [3)]	6 [1)]	L2	3 [4)]	0xEE93	VQFN-48

1) DCSG Ch6, 7, and 8 are not available in these devices.
2) SCB1, SCB2, and SCB4 are not available in 64-pin devices.
3) PPCA CPU0 and CPU1 data SRAM are 8 KB in these devices.
4) SCB1, SCB2, SCB4, and SCB5 are not available in 48-pin devices.

Table 26 lists the PSC3M8x device part numbers and features. All devices include an Arm® Cortex®-M33 with a 180 MHz CPU speed, a PPCA with two Arm® Cortex®-M33 processors running at 200 MHz, CORDIC, MOTIF, four 12-bit, 25 Msps SAR ADC modules with four AFE, 2-channel 16-bit TCPWM, 2-channel 32-bit TCPWM, 2-channel CAN FD, and CryptoLite functionality.

Table 26 Ordering information PSC3M8x

Product	Flash	SRAM	GPIO/Analog Inputs	PPCA TCPWM (includes 12 Ch HRPWM)	PPCA SRAM	DCSG Channels	Security (PSA Level)	SCB (UART, SPI, I²C)	Silicon ID	Pin
PSC3M8GFS3PAHQ1	512 KB	128 KB	60/40	26 Ch	112 KB	9	L3	7	0xEE80	E-LQFP-100
PSC3M8GFS3PAFQ1	512 KB	128 KB	45/33	26 Ch	112 KB	9	L3	7	0xEE81	E-LQFP-80
PSC3M8GFS3PACQ1	512 KB	128 KB	33/29	26 Ch	112 KB	6[1)]	L3	4[2)]	0xEE83	E-LQFP-64
PSC3M8GFS3PLHQ1	512 KB	128 KB	34/29	26 Ch	112 KB	6 [1)]	L3	4 [2)]	0xEE85	VQFN-64
PSC3M8FES2PLHQ1	256 KB	64 KB	34/29	26 Ch	96 KB[3)]	6 [1)]	L2	4 [2)]	0xEE8D	VQFN-64
PSC3M8GFS3PLGQ1	512 KB	128 KB	25/19	26 Ch	112 KB	6 [1)]	L3	3 [4)]	0xEE84	VQFN-48
PSC3M8FES2PLGQ1	256 KB	64 KB	25/19	26 Ch	96 KB [3)]	6 [1)]	L2	3 [4)]	0xEE94	VQFN-48

1) DCSG Ch6, 7, and 8 are not available in these devices.
2) SCB1, SCB2, and SCB4 are not available in 64-pin devices.
3) PPCA CPU0 and CPU1 data SRAM are 8 KB in these devices.
4) SCB1, SCB2, SCB4, and SCB5 are not available in 48-pin devices.

Table 27 lists the PSC3P7x device part numbers and features. All devices include an Arm® Cortex®-M33 with a 180 MHz CPU speed, a PPCA with one Arm® Cortex®-M33 processor running at 200 MHz, four 12-bit, 25 Msps SAR ADC modules with four AFE, 2-channel 16-bit TCPWM, 2-channel 32-bit TCPWM, 2-channel CAN FD, and CryptoLite functionality.

Table 27 Ordering information PSC3P7x

Product	Flash	SRAM	GPIO/Analog Inputs	PPCA TCPWM	PPCA SRAM	DCSG Channels	Security (PSA Level)	SCB (UART, SPI, I²C)	Silicon ID	Pin
PSC3P7GES3PAFQ1	512 KB	128 KB	45/33	26 Ch [1)]	96 KB [2)]	9	L3	7	0xEE88	E-LQFP-80
PSC3P7FES2PLHQ1	256 KB	64 KB	34/29	16 Ch [3)]	48 KB [4)]	6 [5)]	L2	4 [6)]	0xEE8E	VQFN-64
PSC3P7FES2PLGQ1	256 KB	64 KB	25/19	16 Ch [3)]	48 KB [4)]	3 [7)]	L2	3 [8)]	0xEE95	VQFN-48

1) Includes 12 HRPWM channels in this device.
2) PPCA CPU0 and CPU1 data SRAM are 8 KB in these devices.
3) TCPWM Channels 12, 13, 14, 15, 16, 17, 18, 19, 24 and 25 are not available. Includes eight HRPWM.
4) PPCA CPU0 code 32 KB and data SRAM 16 KB are available in these devices.

5) DCSG Ch6, 7, and 8 are not available in these devices.
6) SCB1, SCB2, and SCB4 are not available in 64-pin devices.
7) DCSG Ch0, 1, 2, 3, 4, 5 and 6 are not available in these devices.
8) SCB1, SCB2, SCB4, and SCB5 are not available in 48-pin devices.

Table 28 lists the PSC3M7x device part numbers and features. All devices include an Arm® Cortex®-M33 with a 180 MHz CPU speed, a PPCA with one Arm® Cortex®-M33 processor running at 200 MHz, CORDIC, MOTIF, four 12-bit, 25 Msps SAR ADC modules with four AFE, 2-channel 16-bit TCPWM, 2-channel 32-bit TCPWM, 2-channel CAN FD, and CryptoLite functionality.

Table 28 Ordering information PSC3M7x

Product	Flash	SRAM	GPIO/Analog Inputs	PPCA TCPWM	PPCA SRAM	DCSG Channels	Security (PSA Level)	SCB (UART, SPI, I²C)	Silicon ID	Pin
PSC3M7GES3PAFQ1	512 KB	128 KB	45/33	26 Ch[1)]	96 KB[2)]	9	L3	7	0xEE89	E-LQFP-80
PSC3M7FES2PLHQ1	256 KB	64 KB	34/29	16 Ch[3)]	48 KB[4)]	6[5)]	L2	4[6)]	0xEE8F	VQFN-64
PSC3M7FES2PLGQ1	256 KB	64 KB	25/19	16 Ch[3)]	48 KB [4)]	3[7)]	L2	3[8)]	0xEE96	VQFN-48

1) Includes 12 HRPWM channels in this device.
2) PPCA CPU0 and CPU1 data SRAM are 8 KB in these devices.
3) TCPWM Channels 12, 13, 14, 15, 16, 17, 18, 19, 24 and 25 are not available. Includes eight HRPWM.
4) PPCA CPU0 code 32 KB and data SRAM 16 KB are available in these devices.
5) DCSG Ch6, 7, and 8 are not available in these devices.
6) SCB1, SCB2, and SCB4 are not available in 64-pin devices.
7) DCSG Ch0, 1, 2, 3, 4, 5 and 6 are not available in these devices.
8) SCB1, SCB2, SCB4, and SCB5 are not available in 48-pin devices.

***Note**: Product names are derived from memory sizes rounded to the nearest standard size, as specified in the part nomenclature table.*

8.1 Part number nomenclature

MPN decoder:

PS C3 A B CC DD E FF G H II J K

Field	Description	Values	Meaning
PS	Brand	PS	Brand
C3	Family	C3	Family
A	Series	P	Power control
		M	Motor control
B	Sub-series	Entry Line	1-3
		Main Line	4-6
		Performance Line	7-9
CC	Memory (Flash/SRAM)	A	8 KB

Field	Description	Values	Meaning
		B	16 KB
		C	32 KB
		D	64 KB
		E	128 KB
		F	256 KB
		G	512 KB
		H	768 KB
		J	1 MB
		K	2 MB
		L	3 MB
		M	4 MB
		N	6 MB
		O	7 MB
		P	8 MB
DD	Security	S2	PSA L2 (PSA certification Level 2)
		S3	PSA L3 (PSA certification Level 3)
E	Special attributes	D	Dual Core
		P	Programmable Power Control Subsystem
FF	Package	AB	EQFP-48 (0.5 mm)
		AC	EQFP-64 (0.5 mm)
		AF	EQFP-80 (0.5 mm)
		AH	QFP-100 (0.5 mm)
		AI	QFP-128 (0.5 mm)
		AE	QFP-144 (0.5 mm)
		LB	VQFN-24 (0.5 mm)
		LC	VQFN-32 (0.5 mm)
		LE	VQFN-40 (0.4 mm)
		LF	VQFN-48 (0.35 mm)
		LG	VQFN-48 (0.4 mm)
		LH	VQFN-64 (0.4 mm)
G	Temperature	C	Consumer (0°C to +70°C)
		I	Industrial (-40°C to +85°C)
		Q	Extended range (-40°C to +105°C)

Field	Description	Values	Meaning
H	Maximum Core Frequency	1	100-199 MHz
		2	200-299 MHz
II	Sample (Optional)	ES	Engineering sample
J	Revision	-	Base
		A	Die revision
K	Packing (Optional)	T	Tape and Reel
		-	Tray

9 Package information

The PSC3P8xx and PSC3M8xx devices are available in VQFN-48, VQFN-64, E-LQFP-64, E-LQFP-80, and E-LQFP-100 packages. For pinout details, see Pins.

Table 29 Package dimensions

Spec ID#	Package	Description	Package drawing number
PKG_1	E-LQFP-100	E-LQFP-100 14.0 mm x 14.0 mm x 1.6 mm height with 0.5 mm pitch, 6.5 x 6.5 mm EPAD	002-40570 Rev. *B
PKG_2	E-LQFP-80	E-LQFP-80, 12.0 mm x 12.0 mm x 1.6 mm height with 0.5 mm pitch, 4.6 x 4.6 mm EPAD	002-38596 Rev. *B
PKG_3	E-LQFP-64	E-LQFP-64, 10.0 mm x 10.0 mm x 1.6 mm height with 0.5 mm pitch, 4.0 x 4.0 mm EPAD	002-42581 Rev. **
PKG_4	VQFN-64	VQFN-64, 8.0 mm x 8.0 mm x 0.9 mm height with 0.4 mm pitch, 4.2 x 4.2 mm EPAD (SAWN type)	002-40328 Rev. *A
PKG_5	VQFN-48	VQFN-48, 6.0 mm x 6.0 mm x 0.9 mm height with 0.4 mm pitch, 4.5 x 4.5 mm EPAD (SAWN type)	002-42583 Rev. **

Table 30 Package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	-	-40	25	115[1)]	°C
T_J	Operating junction temperature, all packages	-	-40	-	125	°C
T_{JA}	Package θ_{JA} (E-LQFP-100)	-	-	17.7	-	°C/watt
T_{JB}	Package θ_{JB} (E-LQFP-100)	-	-	9.9	-	°C/watt
T_{JC}	Package θ_{JC} (E-LQFP-100)	-	-	5.6	-	°C/watt
T_{JA}	Package θ_{JA} (E-LQFP-80)	-	-	18.8	-	°C/watt
T_{JB}	Package θ_{JB} (E-LQFP-80)	-	-	7.0	-	°C/watt

(table continues...)

Table 30 (continued) Package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{JC}	Package θ_{JC} (E-LQFP-80)	-	-	5.6	-	°C/watt
T_{JA}	Package θ_{JA} (E-LQFP-64)	-	-	19.4	-	°C/watt
T_{JB}	Package θ_{JB} (E-LQFP-64)	-	-	5.9	-	°C/watt
T_{JC}	Package θ_{JC} (E-LQFP-64)	-	-	5.7	-	°C/watt
T_{JA}	Package θ_{JA} (VQFN-64)	-	-	19.4	-	°C/watt
T_{JB}	Package θ_{JB} (VQFN-64)	-	-	4.7	-	°C/watt
T_{JC}	Package θ_{JC} (VQFN-64)	-	-	1.5	-	°C/watt
T_{JA}	Package θ_{JA} (VQFN-48)	-	-	20.1	-	°C/watt
T_{JB}	Package θ_{JB} (VQFN-48)	-	-	3.5	-	°C/watt
T_{JC}	Package θ_{JC} (VQFN-48)	-	-	1.4	-	°C/watt

1) T_A can be extended to this range as long as T_J does not exceed the device T_{Jmax}.

***Notes**:*

1. *Thermal resistance between the chip and ambient (θ_{JA}) as per JESD51-2A & JESD51-7*
2. *Thermal resistance between the chip and the printed circuit board (θ_{JB}) as per JESD51-8 & JESD51-7*
3. *Thermal resistance between the chip and the package bottom surface by isothermal heat extraction method (θ_{JC})*
4. *The end-application PCB design and operational profile may differ from the conditions described above. The user shall estimate the maximum power without exceeding the maximum junction temperature (T_J) of 125°C, based on the end-application PCB design and operational profile*

Thermal calculations

The maximum junction temperature of the chip can be calculated using the following equation:

T_J max = T_A max + (P_D max × T_{JA})

Where:

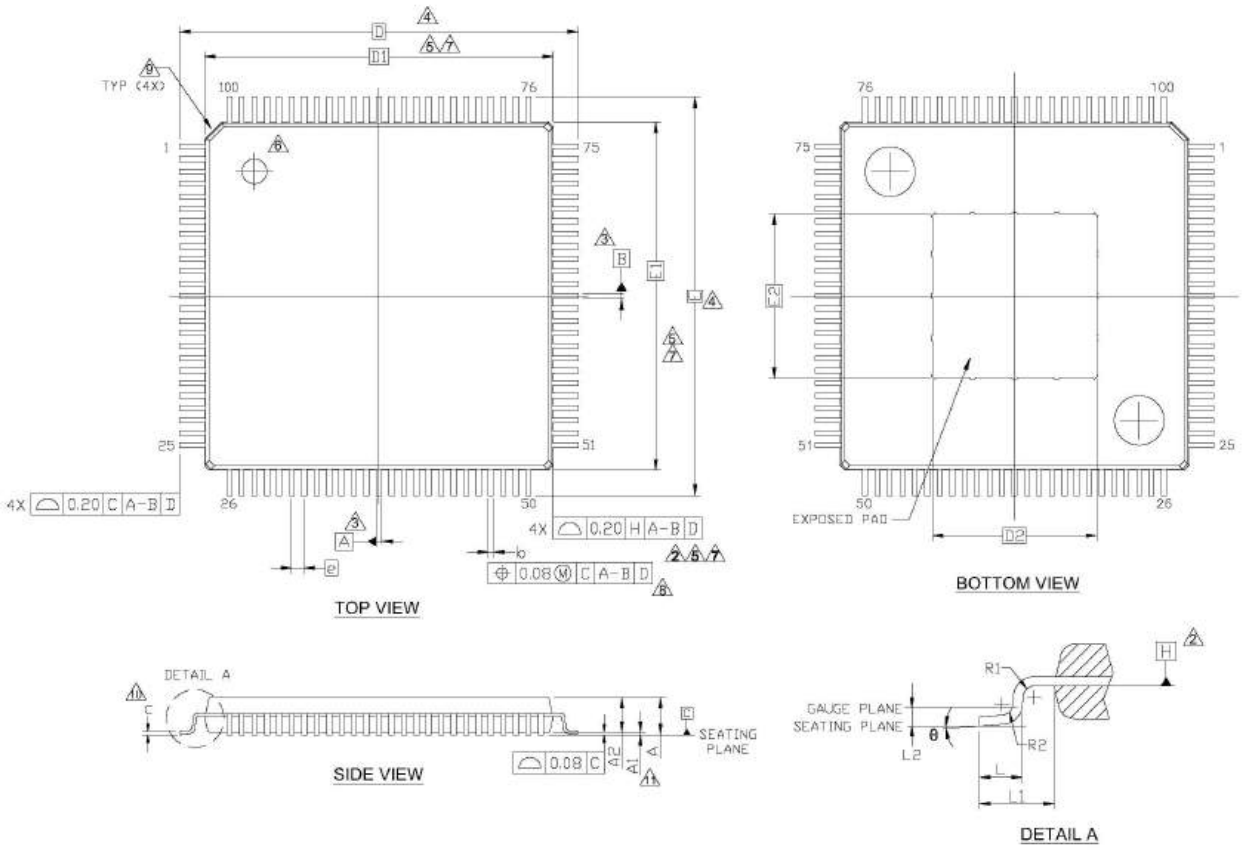
- T_J max is the maximum junction temperature in °C
- T_A max is the maximum ambient temperature in °C
- P_D max is the maximum power dissipation in the chip in watts
- T_{JA} is the package junction to ambient thermal resistance

Table 31 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time at peak temperature
All packages	260°C	30 seconds

Table 32 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
All packages	MSL3

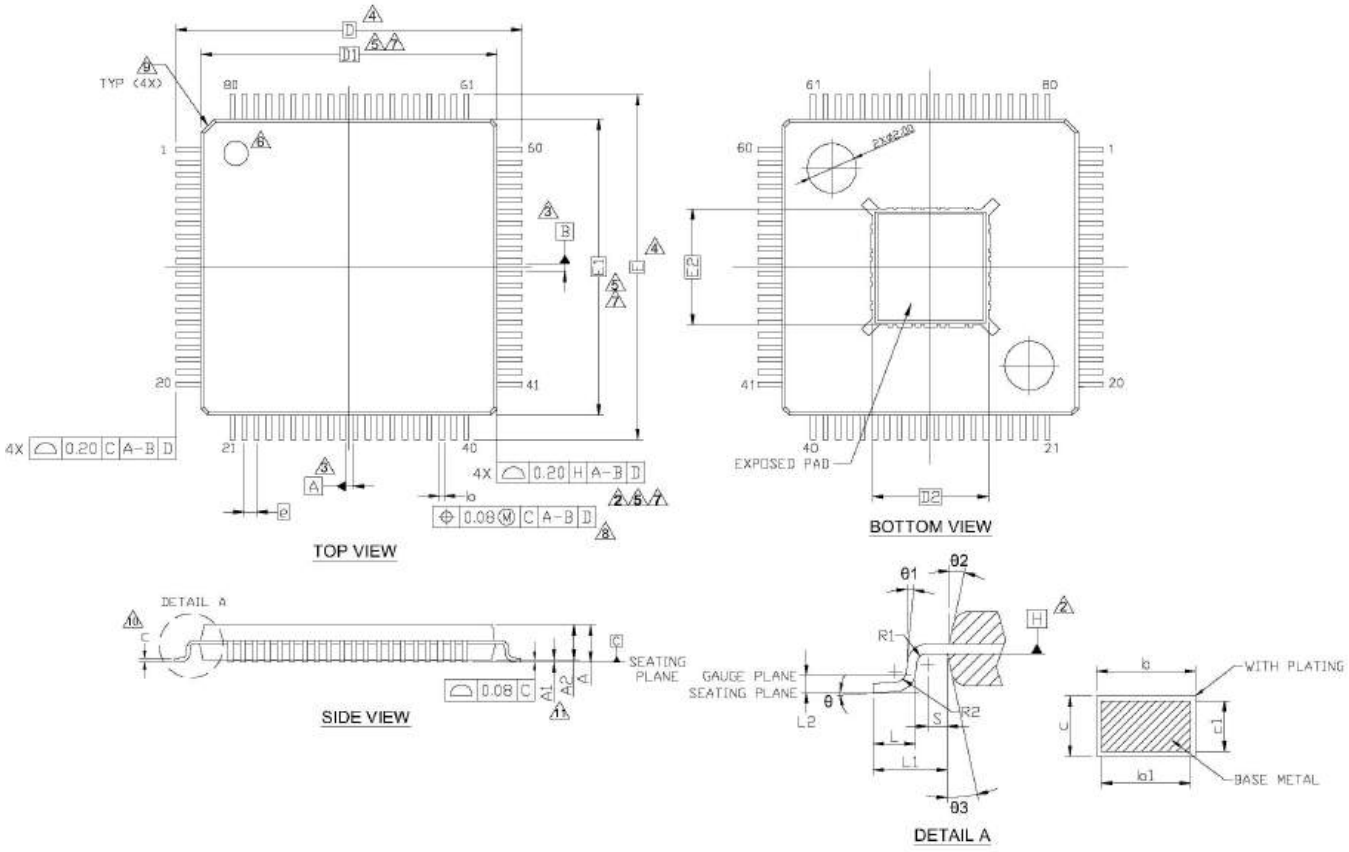


SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D		16.00 BSC	
D1		14.00 BSC	
D2	6.35	—	6.65
E		16.00 BSC	
E1		14.00 BSC	
E2	6.35	—	6.65
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	—	8°
c	0.10	0.127	0.20
b	0.17	0.20	0.26
L	0.45	0.60	0.75
L1		1.00 REF	
L2		0.25 REF	
e		0.50 BSC	

NOTES
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-40570 Rev. *B

Figure 13 100-lead E-LQFP (14.0×14.0×1.6 mm) AE100A (6.5×6.5 mm) EPAD, package outline



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	14.00 BSC		
D1	12.00 BSC		
D2	4.30	—	4.85
E	14.00 BSC		
E1	12.00 BSC		
E2	4.30	—	4.85
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	11°	12°	13°
θ3	11°	12°	13°
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16

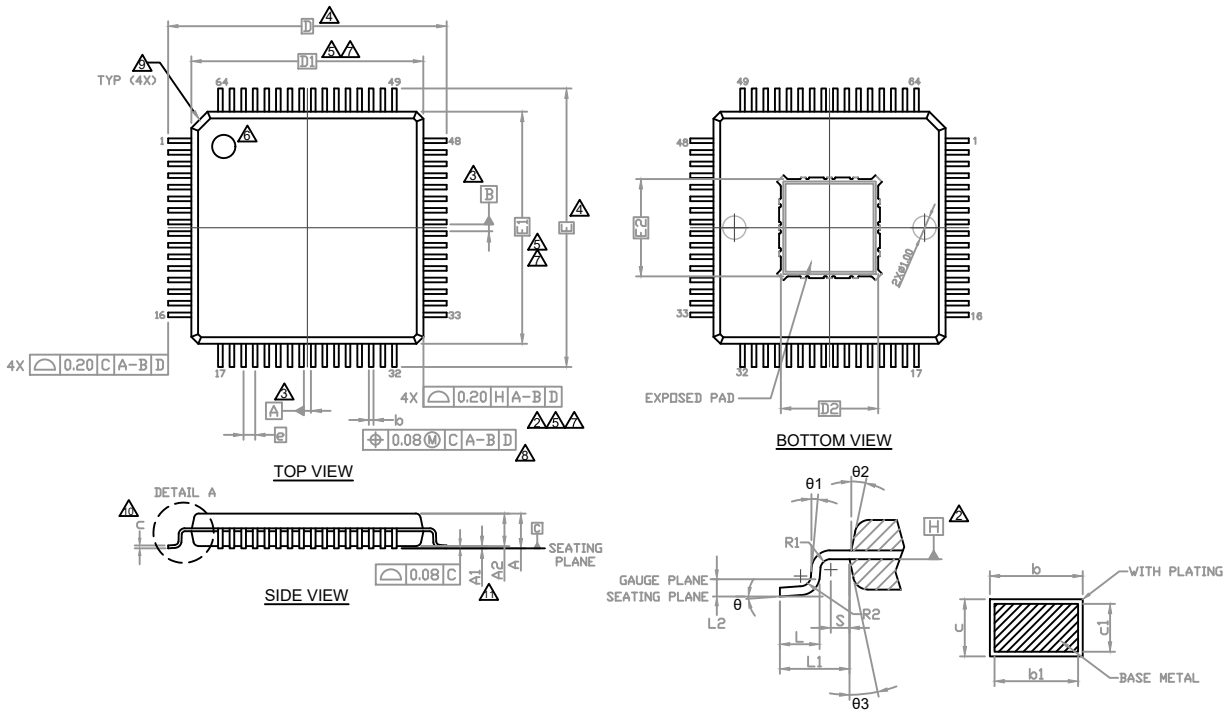
SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 REF		
e	0.50 BSC		
S	0.20	—	—

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-38596 Rev. *B

Figure 14 80-lead E-TQFP (12.0×12.0×1.6 mm) AE80A (4.6×4.6 mm) EPAD, package outline



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D		12.00 BSC	
D1		10.00 BSC	
D2	3.79	—	4.34
E		12.00 BSC	
E1		10.00 BSC	
E2	3.79	—	4.34
R1	0.08	—	—
R2	0.08	—	0.20
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	11°	12°	13°
θ3	11°	12°	13°
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16

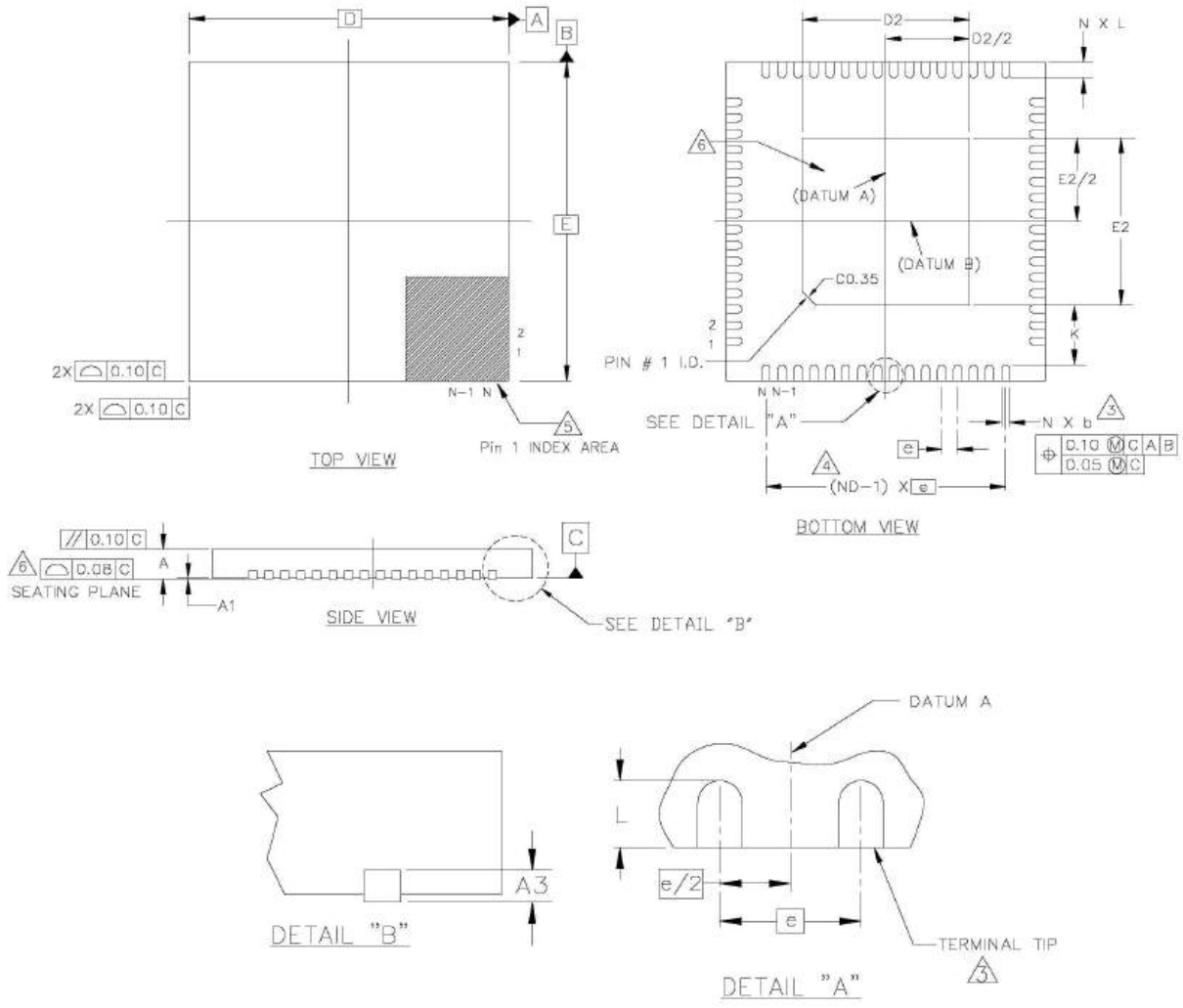
SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
L	0.45	0.60	0.75
L1		1.00 REF	
L2		0.25 REF	
e		0.50 BSC	
S	0.20	—	—

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-42581 Rev. **

Figure 15 64-lead E-LQFP (10.0×10.0×1.6 mm) AE64C (4.0×4.0 mm) EPAD, package outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.40 BSC	
N		64	
ND		16	
L	0.35	0.40	0.45
b	0.15	0.20	0.25
D2	4.15	4.20	4.25
E2	4.15	4.20	4.25
D		8.00 BSC	
E		8.00 BSC	
A	-	-	0.90
A1	0.00	-	0.05
A3		0.203 REF	
K		0.20 MIN	

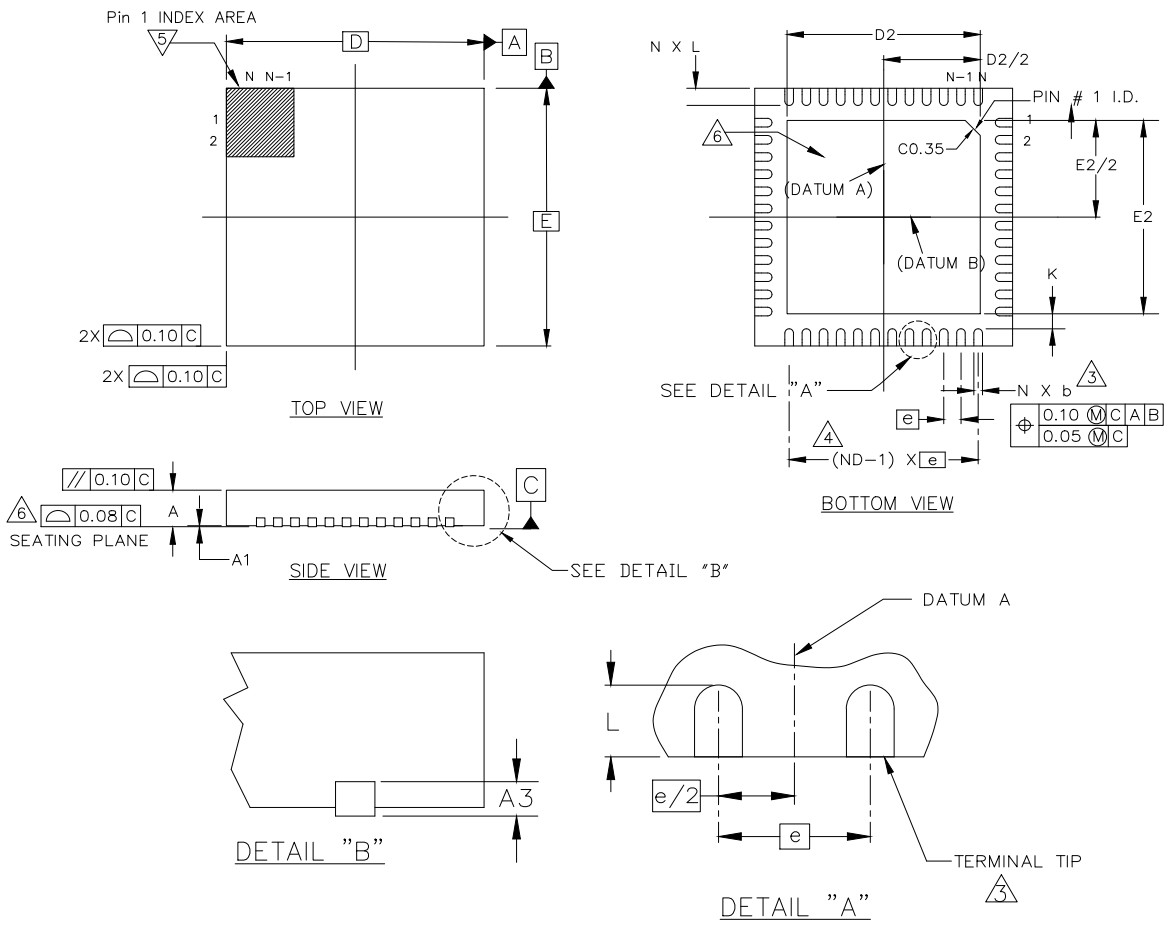
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-40328 Rev. *A

Figure 16 64-lead QFN (8.0×8.0×0.9 mm) LT64B (4.2×4.2 mm) EPAD (SAWN), package outline

9 Package information



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.40 BSC	
N		48	
ND		12	
L	0.30	0.40	0.50
b	0.15	0.20	0.25
D2	4.65	4.70	4.75
E2	4.65	4.70	4.75
D	5.90	6.00	6.10
E	5.90	6.00	6.10
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF	
K	0.20	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-42583 Rev. **

Figure 17 48-lead QFN (6.0×6.0×0.9 mm) LT48G (4.7×4.7 mm) EPAD (SAWN), package outline

10 Errata

This section outlines the errata for the PSOC™ Control C3 (P/M) (8/7) MCU product line. It includes details on errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. For more details, contact Infineon Support.

10.1 Part numbers affected

Table 33 Part numbers affected

Part number	Device characteristics
All	PSOC™ Control C3(P/M)(8/7) MCU product line

10.2 PSOC™ Control C3(P/M)(8/7) qualification status

Production silicon

10.3 PSOC™ Control C3(P/M)(8/7) errata summary

Table 34 defines the errata applicability for available product-line devices.

***Note**: Click on any item entry to view its description.*

Table 34 Errata applicability across product-line devices

Items		Silicon revision	Fix status
No alarm is triggered in AES when the status-ready signal is faulty	All	1	Fix not planned
R2R DAC linearity measurement does not meet the datasheet specification	All	1	Fix not planned
R2R DAC gain performance not meeting specification	All	1	Fix not planned
PSA Level 3 (PSA L3) certification requirement not met	All	1	Fix planned
Intermittent faults during AES operations using the AES-256 hardware accelerator	All	1	Fix planned

No alarm is triggered in AES when the status-ready signal is faulty	
Problem definition	In a specific window after the start of the calculation, fault injection is not detected, and no alarm is triggered. Once the calculation is completed, the wrong result is delivered due to the fault.
Parameters affected	AES alarm
Trigger condition	Fault injection causes incorrect behavior
Scope of impact	In a specific window after the start of the calculation, fault injection is not detected, and no alarm is triggered.

No alarm is triggered in AES when the status-ready signal is faulty	
Workaround	After each AES encryption/decryption, the software must follow these steps: **1. Compare input and output data**: • If the input is different from the output: Accept the result, process is complete • If the input is equal to the output: There is a potential attack. Proceed to Step 2 **2. Repeat the encryption/decryption** **3. Compare input and output data again**: • If the input is different from the output: An attack occurred during the first operation, but the correct result is now obtained • If the input is equal to the output: Accept the result, process is complete
Fix status	Fix not planned

R2R DAC linearity measurement does not meet the datasheet specification	
Problem definition	R2R DAC exhibits a discontinuity at the mid-code boundary when operated over the full 12-bit code range. While the DAC meets all documented specifications when limited to half-scale operation, using the full-scale code range introduces a mid-code jump that degrades linearity performance. The DAC does not meet the specified INL and DNL performance over the full 0–4095 code range.
Parameters affected	• Differential Non-Linearity (DNL) (SIDR2R.3) - R2R DAC DNL over code range 0–4095: ±4 LSB • Integral Non-Linearity (INL) (SIDR2R.4) - R2R DAC INL over code range 0–4095: ±8 LSB • When the DAC is limited to half-code range (0 - 2047) operation, all documented specifications are met. - Effective output voltage range (with or without output buffer) is limited to half of the range specified in: - SIDR2R.5 - SIDR2R.5A - SIDR2R.5B - SIDR2R.5D - SIDR2RB.2
Trigger condition	The DAC output code transitions across the mid-code boundary (approximately code 2047 to 2048), where a mid-code jump occurs

R2R DAC linearity measurement does not meet the datasheet specification	
Scope of impact	This issue affects R2R DAC GRP0 and GRP1 when used with or without the output buffer enabled. Applications that use the full DAC code range may experience INL and DNL specification violations, while operation limited to codes 0–2047 is not impacted and meets all specifications.
Workaround	None
Fix status	Fix not planned

R2R DAC gain performance not meeting specification	
Problem definition	The R2R DAC exhibits gain error after calibration that does not meet the specified limits defined for parameters, particularly in the extended-range ±VDDA configuration
Parameters affected	SIDR2R.2 – R2R DAC Gain Error After Calibration
Trigger condition	The deviation occurs when the R2R DAC is operated in the Extended Range (±VDDA) configuration
Scope of impact	In Extended Range ±VDDA mode: • Gain error may exceed the ±1% specification, with worst-case deviations up to +1.0% to -5.0%
Workaround	None
Fix status	Fix not planned

PSA Level 3 (PSA L3) certification requirement not met	
Problem definition	The device does not fulfill the full PSA L3 certification requirements
Parameters affected	This deviation affects the security feature set and certification status of the device
Trigger condition	The deviation is present whenever PSA L3 compliance or certification is assumed
Scope of impact	Solutions designed under the assumption of PSA L3 certification may not meet certification
Workaround	None
Fix status	Fix planned

Intermittent faults during AES operations using the AES-256 hardware accelerator	
Problem definition	The AES-256 hardware accelerator may intermittently enter a locked alarm state, causing subsequent accesses to fault and disrupting cryptographic services that rely on the hardware AES block.
Parameters affected	AES operations, including all data transfers to and from the AES hardware IP
Trigger condition	• AES encryption or decryption processing • Data transfers between the CPU and the AES module

Intermittent faults during AES operations using the AES-256 hardware accelerator	
Scope of impact	At runtime, the AES hardware accelerator may sporadically enter an alarm (locked) state. Once in this state, all subsequent accesses to the AES module may result in faults. Any PSA Crypto API function that relies on the hardware AES accelerator may be impacted. For example, the TF-M Protected Storage service, which uses AES-CCM with 128-bit or 256-bit keys.
Workaround	• If an unexpected alarm occurs, reset the AES-256 module from the application software and re-execute the most recent cryptographic operation. The software must track the last successfully completed operation to allow safe recovery • Use Mbed TLS with Cryptolite acceleration as the cryptographic backend instead of the hardware AES block
Fix status	Fix planned

11 Document conventions

11.1 Units of measure

Table 35 Units of measure

Symbol	Unit of measure
°C	Degree Celsius
KB	1024 bytes
kHz	Kilohertz
Mbps	Megabits per second
Msps	Million samples per second
MHz	Megahertz
ns	Nanosecond
%	Percent
V	Volt

Glossary

ADC
Analog-to-digital converter

AES
Advanced encryption standard

AFE
Analog front end

AMUX
Analog multiplexer

ATOP
Analog top

BLDC
Brushless direct current

BOD
Brownout detect

CAN
Controller area network

CLB
Custom logic block

CORDIC
Coordinate Rotation Digital Computer

CSV
Clock supervision

CTI
Cross trigger interface

DAC
Digital-to-analog converter

DCMP
Digital comparator

DCSG
Differential analog comparator with slope generator

DFU
Device firmware upgrade

DMA
Direct memory access

DSI
Digital signal interconnect

DSP
Digital signal processor

ECC
Error correcting code

ECO
External crystal oscillator

ENOB
Effective number of bits

EOS
End of sampling

EPU
Event processing unit

ETB
Embedded Trace Buffer

ETM
Embedded Trace Macrocell

FET
Field effect transistor

FIFO
First in, First out

FOC
Field-oriented control

FPU
Floating point unit

GPI
General purpose input

GPIO
General-purpose input/output

HPPASS
High-performance programmable analog subsystem

HRPWM
High-resolution pulse-width modulator

HSIOM
High-speed I/O matrix

HWFILT3P3Z
Hardware filter - 3 poles 3 zeros

I-cache
Instruction-cache

I2C
Inter-integrated circuit

IHO
Internal high-speed oscillator

ILO
Internal low-speed oscillator

IMO
Internal main oscillator

IPC
Inter-processor communication

IRQ
Interrupt request

ISR
Interrupt service routine

ITM
Instrumentation Trace Macrocell

LPComp
Low-power comparator

LUT
Lookup table

LVD
Low-voltage detection

LVTTL
Low-voltage transistor-transistor logic

MCU
Microcontroller

MCWDT
Multi-counter watchdog timer

MOTIF
Motion interface

MPU
Memory protection unit

NVIC
Nested Vectored Interrupt Controller

PAL
Programmable array logic

PLD
Programmable logic device

PLL
Phase-locked loops

PMBus
Power management bus

POR
Power-on reset

PPCA
Programmable Power Control Accelerator

ROM
Read-only memory

RSA
Rivest-Shamir-Adleman, a public-key cryptography algorithm

RTC
Real-time clock

RWW
Read-While-Write

S/H
Sample/Hold

SAR
Successive Approximation Register

SAU
Secure Attribution Unit

SCB
Serial communication blocks

SHA
Secure Hash Algorithm

SIL
Safety integrity levels

SMBus
System management bus

SOC
Start of conversion

SPI
Serial Peripheral Interface

SRAM
Static random access memory

SRSS
System resources subsystem

SVGS
Supply voltage glitch sensor

TCPWM
Timer/counter pulse-width modulator

TRNG
True Random Number Generator

TZ
TrustZone

UART
Universal Asynchronous Transmitter Receiver

WCO
Watch crystal oscillator

WIC
Wakeup Interrupt Controller

XRES
External reset input pin

Revision history

Document revision	Date	Description of changes
*D	2026-06-25	Public release.

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