SY75707

Ultra-Low Additive Jitter Differential Input to Two 1.2V to 1.8V Output LVCMOS Buffers

Features

- A Differential Input to Two LVCMOS Outputs
- LVCMOS Outputs Support 1.2V to 1.8V
- Ultra-Low Additive Jitter 32 fs (typical) in 12 kHz to 20 MHz Band at 156.25 MHz
- Supports Frequencies from 0 Hz up to 250 MHz
- Output-to-Output Skew Less Than 50 ps (maximum)
- Transparent for Spread Spectrum
- Extended Temperature Range: –40°C to +105°C
- 1.4 mm x 1.6 mm VDFN Package

Applications

- Clock Distribution
- Green Servers
- Battery-Powered Applications

General Description

The SY75707 is a low-power LVCMOS clock buffer and voltage level translator featuring ultra-low additive jitter and an extended operating temperature range.

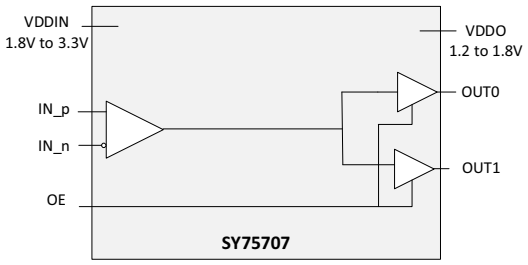
The device has an extended temperature range of –40°C to +105°C, allowing it to be used in harsh environments.

Package Type

SY75707
8-Lead VDFN
(Top View)

Functional Block Diagram

Simplified SY75707 Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DDIN}) ..... –0.5V to +4.0V
Supply Voltage (V_{DDO}) ..... –0.5V to +2.3V
Input Voltage (V_{IN}) ..... –0.5V to V_{DDIN} + 0.5V
Input ESD Protection (HBM) ..... 2 kV
Input ESD Protection (CDM) ..... 1 kV

Operating Ratings ‡

1.2V Operating Voltage (V_{DDO}) ..... +1.08V to +1.32V
1.5V Operating Voltage (V_{DDO}) ..... +1.35V to +1.65V
1.8V Operating Voltage (V_{DDIN}/V_{DDO}) ..... +1.62V to +1.98V
2.5V Operating Voltage (V_{DDIN}) ..... +2.25V to +2.75V
3.3V Operating Voltage (V_{DDIN}) ..... +2.97V to +3.63V

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions may affect device reliability.

‡ Notice: The data sheet limits are not guaranteed if the device is operated beyond the recommended operating conditions.

CURRENT CONSUMPTION

Electrical Characteristics: V_{DDIN} = 3.3V ±10%, V_{DDIN} = 2.5V ±10%, V_{DDIN}/V_{DDO} = 1.8V ±10%, V_{DDO} = 1.5V ±10%, V_{DDO} = 1.2V ±10%, T_A = –40°C to +105°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
V_{DDIN} Current	$I_{DD\_INPUT\_1.8V}$	—	4.7	—	mA	Outputs disabled, input clock 25 MHz
	$I_{DD\_INPUT\_2.5V}$	—	4.7	—	mA	
	$I_{DD\_INPUT\_3.3V}$	—	4.8	—	mA	
V_{DDO} Current	$I_{OUT\_1.8V}$	—	8.5	—	mA	Note 1
	$I_{OUT\_1.5V}$	—	5.8	—	mA	
	$I_{OUT\_1.2V}$	—	3.9	—	mA	

Note 1: Tested with 25 MHz clock with outputs driving 4” long trace with 50Ω characteristic impedance, terminated with 2 pF capacitors to ground (2 pF is for validation test).

INPUT ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDIN} = 3.3V ±10%, V_{DDIN} = 2.5V ±10%, V_{DDIN}/V_{DDO} = 1.8V ±10%, V_{DDO} = 1.5V ±10%, V_{DDO} = 1.2V ±10%, T_A = –40°C to +105°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
LVCMOS Input (OE)						
Input High Voltage	V_{IH}	0.7*V_{DDIN}	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.3*V_{DDIN}	V	—
Input Capacitance	C_{IN}	—	—	5	pF	—
Input Leakage Current for OE Input (includes current due to pull down resistors)	I_{IL_OE}	–5	—	50	µA	—
Maximum Input Voltage	$V_{IN(MAX)}$	—	—	V_{DDIN} + 0.4	V	—
Minimum Input Voltage	$V_{IN(MIN)}$	–0.3	—	—	V	—

INPUT ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{DDIN} = 3.3V ±10%, V_{DDIN} = 2.5V ±10%, V_{DDIN}/V_{DDO} = 1.8V ±10%, V_{DDO} = 1.5V ±10%, V_{DDO} = 1.2V ±10%, T_A = –40°C to +105°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Differential Input DC-Coupled						
Differential Input Slew Rate	DSR_{IN}	0.6	—	—	V/ns	—
Differential Input Voltage	V_{ID}	0.2	—	—	V	—
Input Leakage Current	I_{IL_IN}	–5	—	50	µA	—
Absolute Crossing Point Voltage	V_{CROSS}	0.25	—	0.55	V	—
Maximum Input Voltage	$V_{IN(MAX)}$	—	—	1.15	V	—
Minimum Input Voltage	$V_{IN(MIN)}$	–0.3	—	—	V	—
Differential Input Duty Cycle	D_{DUTY_CYCLE}	45	50	55	%	—
Input Frequency	f_{IN_D}	0	—	250	MHz	—

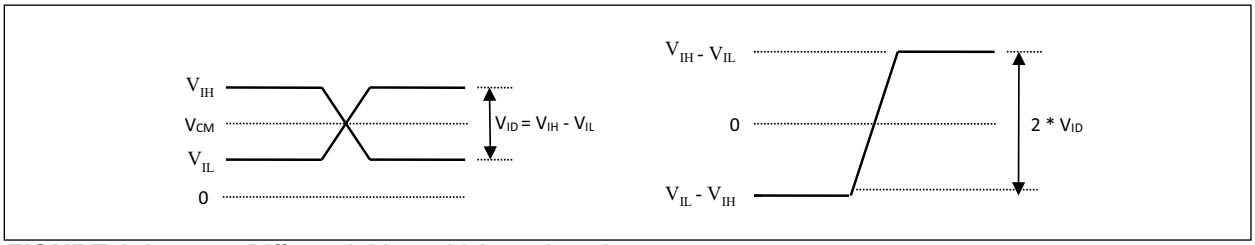


FIGURE 1-1: *Differential Input Voltage Levels.*

OUTPUT ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDIN} = 3.3V ±10%, V_{DDIN} = 2.5V ±10%, V_{DDIN}/V_{DDO} = 1.8V ±10%, V_{DDO} = 1.5V ±10%, V_{DDO} = 1.2V ±10%, T_A = –40°C to +105°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Rise Time (20% to 80%)	t_R	320	400	540	ps	Note 1
Output Fall Time (80% to 20%)	t_F	300	370	500	ps	Note 1
Output High Voltage	V_{OH}	0.8*V_{DDO}	—	—	V	I_{OUT} = 3 mA
Output Low Voltage	V_{OL}	—	—	0.2*V_{DDO}	V	I_{OUT} = –3 mA
Output Duty Cycle (when input has 50% duty cycle)	DC	45	50	55	%	f_{OUT} = 156.25 MHz
Output Frequency	f_{OUT}	0	—	250	MHz	—
Device-to-Device Skew	t_{DDSK}	—	—	340	ps	—
Input-to-Output Delay	$t_{IOD\_DIFF\_IN}$	0.9	1.2	2.3	ns	—
Output-to-Output Skew	t_{OOSK}	—	—	20	ps	—
Output Enable Time	t_{EN}	3	—	5	cycles	—
Output Disable Time	t_{DIS}	2	—	4	cycles	—
Output Impedance	O_{IMP}	40	50	60	Ω	Note 2

Note 1: Bench tested with 100 MHz clock with outputs driving 4” long trace with 50Ω characteristic impedance, terminated with 2 pF capacitors to ground.

2: 50Ω output impedance is with 1.2V V_{DDO}. When output is powered with 1.8V V_{DDO}, the output impedance will be slightly lower (approximately 40Ω).

JITTER AND PHASE NOISE

Electrical Characteristics: V_{DDIN} = 3.3V ±10%, V_{DDO} = 1.8V ±10%, T_A = –40°C to +105°C.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Additive RMS jitter in 1 MHz to 5 MHz band	$t_{j\_1M\_5M}$	—	27	40.6	fs_{RMS}	Note 1, 25 MHz clock
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	38	43.1	fs_{RMS}	Note 1, 100 MHz clock
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	32.7	35.7	fs_{RMS}	Note 1, 156.25 MHz clock
Additive RMS jitter in 12 kHz to 5 MHz band	$t_{j\_12k\_5M}$	—	38.9	46.1	fs_{RMS}	Note 1, 25 MHz clock
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	39.7	44.8	fs_{RMS}	Note 1, 100 MHz clock
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	34.2	37.3	fs_{RMS}	Note 1, 156.25 MHz clock
Noise Floor	N_F	—	–166.4	–153.4	dBc/Hz	Note 1, 25 MHz clock
		—	–167.5	–163.8	dBc/Hz	Note 1, 100 MHz clock
		—	–165.3	–162.9	dBc/Hz	Note 1, 156.25 MHz clock

Note 1: Tested with input fed with low jitter input source (R&S SMA100B function generator) and with outputs driving R&S FSWP8 Phase Noise Analyzer via SMA cable.

JITTER AND PHASE NOISE

Electrical Characteristics: V_{DDIN} = 1.8V ±10%, V_{DDO} = 1.8V ±10%, T_A = –40°C to +105°C.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Additive RMS jitter in 1 MHz to 5 MHz band	$t_{j\_1M\_5M}$	—	27.6	38.6	fs_{RMS}	Note 1, 25 MHz clock
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	35.7	40.9	fs_{RMS}	Note 1, 100 MHz clock
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	30.6	33.9	fs_{RMS}	Note 1, 156.25 MHz clock
Additive RMS jitter in 12 kHz to 5 MHz band	$t_{j\_12k\_5M}$	—	31.6	43.8	fs_{RMS}	Note 1, 25 MHz clock
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	37.3	42.7	fs_{RMS}	Note 1, 100 MHz clock
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	32.1	35.5	fs_{RMS}	Note 1, 156.25 MHz clock
Noise Floor	N_F	—	–165.4	–160	dBc/Hz	Note 1, 25 MHz clock
		—	–167.8	–164.2	dBc/Hz	Note 1, 100 MHz clock
		—	–165.9	–162.7	dBc/Hz	Note 1, 156.25 MHz clock

Note 1: Tested with input fed with low jitter input source (R&S SMA100B function generator) and with outputs driving R&S FSWP8 Phase Noise Analyzer via SMA cable.

JITTER AND PHASE NOISE

Electrical Characteristics: V_{DDIN} = 3.3V ±10%, V_{DDO} = 1.2V ±10%, T_A = –40°C to +105°C.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Additive RMS jitter in 1 MHz to 5 MHz band	$t_{j\_1M\_5M}$	—	38.1	62.8	fs_{RMS}	Note 1, 25 MHz clock
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	40.7	68.5	fs_{RMS}	Note 1, 100 MHz clock
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	34	48.2	fs_{RMS}	Note 1, 156.25 MHz clock
Additive RMS jitter in 12 kHz to 5 MHz band	$t_{j\_12k\_5M}$	—	52.9	74.4	fs_{RMS}	Note 1, 25 MHz clock
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	44.4	74.3	fs_{RMS}	Note 1, 100 MHz clock
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	38	53.1	fs_{RMS}	Note 1, 156.25 MHz clock
Noise Floor	N_F	—	–163.8	–156.7	dBc/Hz	Note 1, 25 MHz clock
		—	–166.8	–160	dBc/Hz	Note 1, 100 MHz clock
		—	–165.5	–159	dBc/Hz	Note 1, 156.25 MHz clock

Note 1: Tested with input fed with low jitter input source (R&S SMA100B function generator) and with outputs driving R&S FSWP8 Phase Noise Analyzer via SMA cable.

JITTER AND PHASE NOISE

Electrical Characteristics: V_{DDIN} = 1.8V ±10%, V_{DDO} = 1.2V ±10%, T_A = –40°C to +105°C.						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Additive RMS jitter in 1 MHz to 5 MHz band	$t_{j\_1M\_5M}$	—	37.5	62	fs_{RMS}	Note 1, 25 MHz clock
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	39.4	67.2	fs_{RMS}	Note 1, 100 MHz clock
Additive RMS jitter in 1 MHz to 20 MHz band	$t_{j\_1M\_20M}$	—	33.2	47.3	fs_{RMS}	Note 1, 156.25 MHz clock
Additive RMS jitter in 12 kHz to 5 MHz band	$t_{j\_12k\_5M}$	—	51.2	73.3	fs_{RMS}	Note 1, 25 MHz clock
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	43.1	73	fs_{RMS}	Note 1, 100 MHz clock
Additive RMS jitter in 12 kHz to 20 MHz band	$t_{j\_12k\_20M}$	—	37.2	52.2	fs_{RMS}	Note 1, 156.25 MHz clock
Noise Floor	N_F	—	–165.7	–158.5	dBc/Hz	Note 1, 25 MHz clock
		—	–167.7	–160	dBc/Hz	Note 1, 100 MHz clock
		—	–166.6	–159.3	dBc/Hz	Note 1, 156.25 MHz clock

Note 1: Tested with input fed with low jitter input source (R&S SMA100B function generator) and with outputs driving R&S FSWP8 Phase Noise Analyzer via SMA cable.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Operating Temperature Range	T_A	–40	—	+105	°C	—
Package Thermal Resistances						
Junction-to-Ambient Thermal Resistance, VDFN-8Ld	Θ_{JA}	—	138	—	°C/W	Still-Air
		—	132	—	°C/W	1 m/s airflow
		—	127	—	°C/W	2.5 m/s airflow
Junction-to-Board Thermal Resistance, VDFN-8Ld	Θ_{JB}	—	104	—	°C/W	—
Junction-to-Case Thermal Resistance, VDFN-8Ld	Θ_{JC}	—	105	—	°C/W	—
Thermal Characterization, Junction-to-Top of Package	Ψ_{JT}	—	11.5	—	°C/W	Still-Air

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Description
1	IN_p	I	**Differential Input Reference** Input frequency range >0 Hz to 250 MHz Input has fail-safe circuit to prevent oscillation if the input is not driven. >0 Hz because OE is synchronous and requires three to five clock cycles to enable/disable the output. Once outputs are enabled, the device can transfer a DC level. These pins are pulled low with a 100 kΩ to 300 kΩ resistor.
2	IN_n		
7	OUT0	O	**Ultra-Low Additive Jitter LVCMOS Outputs** Output frequency range >0 Hz to 250 MHz These outputs have embedded series resistance of 50Ω (at 1.2V V_{DDO}).
6	OUT1		
4	OE	I	**Output Enable (Synchronous)** When low, the output is low. When high, the output is enabled. Three to five clock cycles are required for the outputs to become enabled or disabled. This pin is pulled down internally with 100 kΩ to 300 kΩ resistor.
3	VDDIN	P	**Positive Input Supply Voltage.** Connect to between 1.8V and 3.3V supply.
8	VDDO	P	**Positive Output Supply Voltage.** Connect to between 1.2V and 1.8V supply.
5	GND	P	**Ground.** Connect to ground.

3.0 FUNCTIONAL DESCRIPTION

SY75707 is a differential to LVCMOS, ultra-low additive jitter buffer with synchronous Output Enable (OE) control signal. The device can operate at extended temperatures of –40°C to +105°C.

The LVCMOS outputs have built-in 50Ω series resistance, which makes them suitable for driving standard transmission lines (50Ω characteristic impedance) without any external components.

The following phase noise plots captured with R&S FSWP8 Phase Noise Analyzer show typical phase noise performance. Figure 3-1 shows the phase noise of input clock generated with R&S SMA100B signal generator and Figure 3-2 shows the output phase noise.

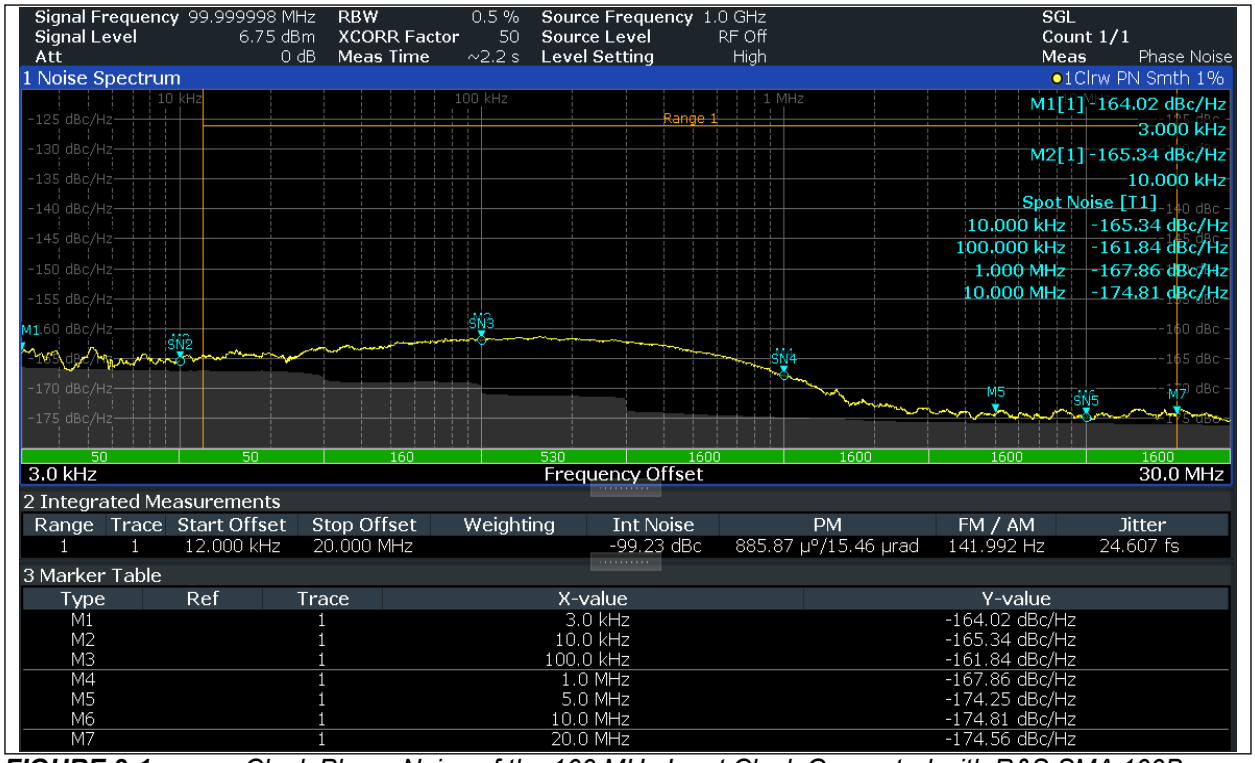


FIGURE 3-1: *Clock Phase Noise of the 100 MHz Input Clock Generated with R&S SMA 100B.*

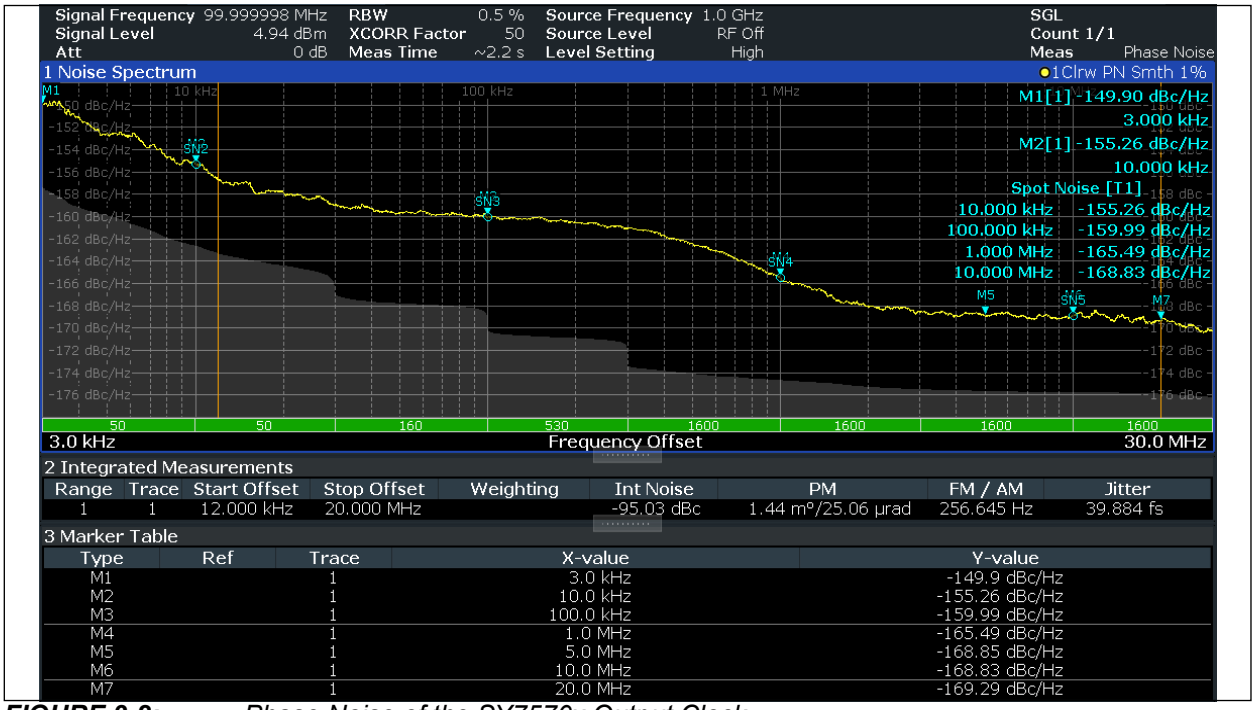


FIGURE 3-2: *Phase Noise of the SY7570x Output Clock.*

The plot above shows that the device has a very low noise floor of –168.8 dBc/Hz, resulting in ultra-low additive jitter in the 12 kHz to 20 MHz band of only 31.2 fs.

3.1 Clock Input

The differential clock input natively supports (no external component) HCSL differential signaling as shown in the following figure.

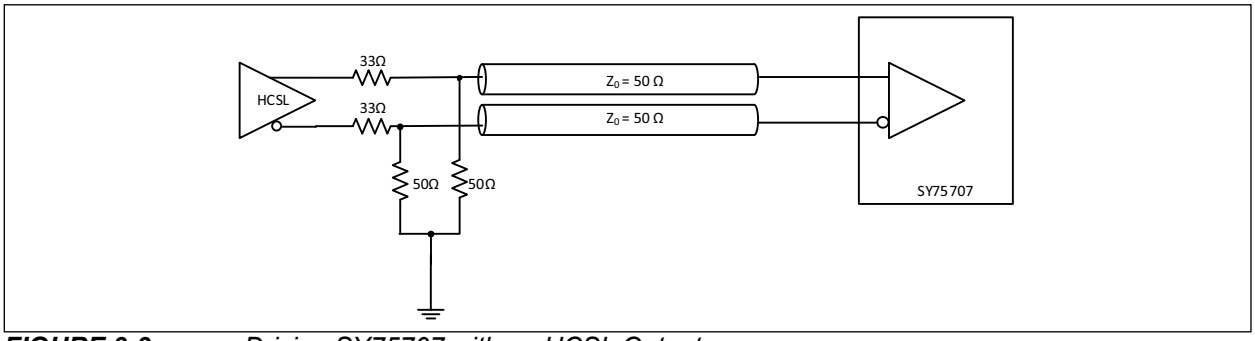
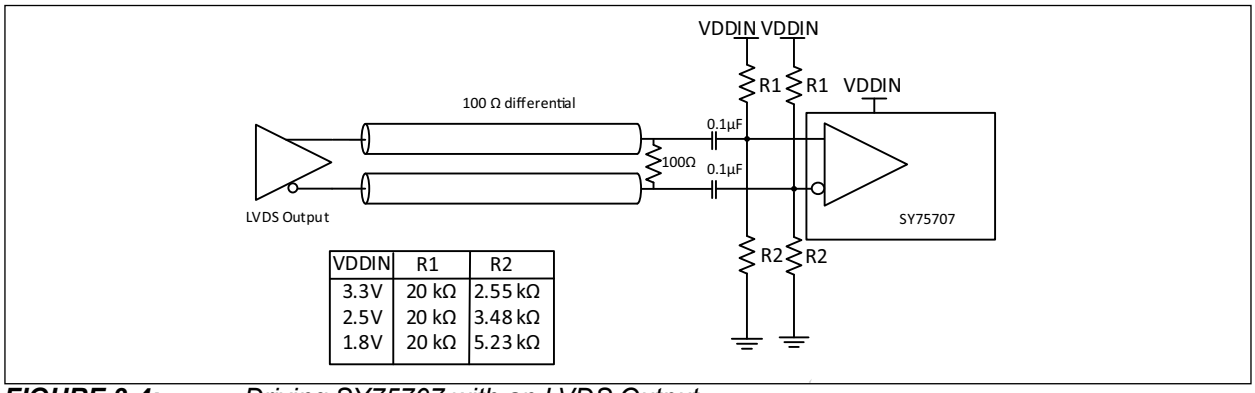


FIGURE 3-3: *Driving SY75707 with an HCSL Output.*

The following figure shows how to interface an LVDS driver to the SY75707 input. The 100Ω termination resistor is placed before AC-coupling capacitors because most LVDS drivers need a DC path between p and n outputs.

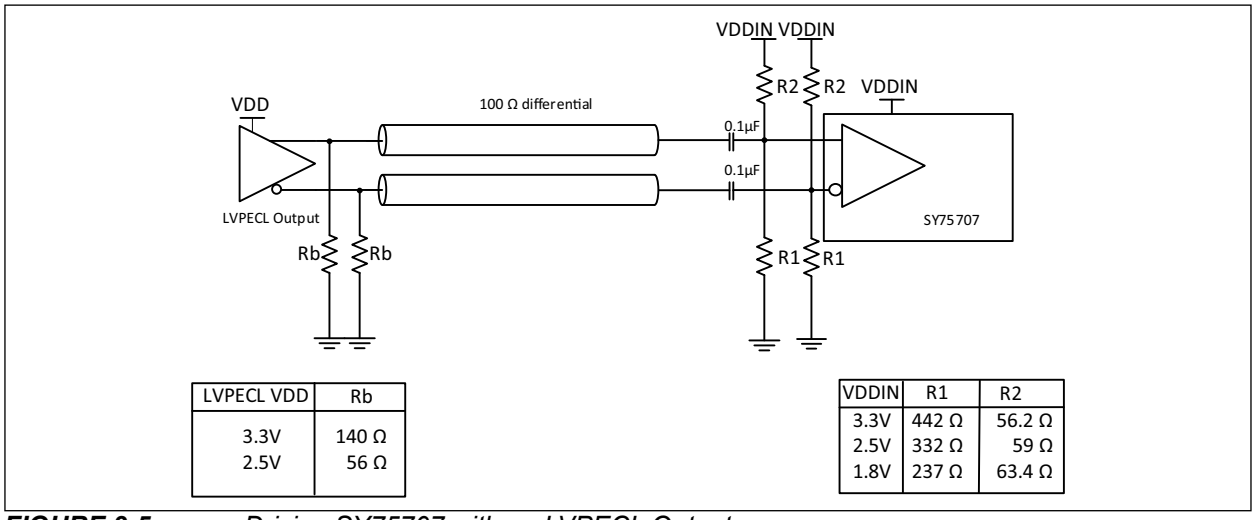
If the LVDS driver does not need the DC path between p and n, the 100Ω resistor can be placed after the AC-coupling capacitors. Alternatively, R1 and R2 can be selected to act as biasing and termination resistors. In that case, 100Ω can be removed.



VDDIN	R1	R2
3.3V	20 kΩ	2.55 kΩ
2.5V	20 kΩ	3.48 kΩ
1.8V	20 kΩ	5.23 kΩ

FIGURE 3-4: *Driving SY75707 with an LVDS Output.*

Figure 3-5 shows driving SY75707 differential input with an LVPECL driver.



LVPECL VDD	Rb
3.3V	140 Ω
2.5V	56 Ω

VDDIN	R1	R2
3.3V	442 Ω	56.2 Ω
2.5V	332 Ω	59 Ω
1.8V	237 Ω	63.4 Ω

FIGURE 3-5: *Driving SY75707 with an LVPECL Output.*

3.2 Clock Output

The LVCMOS output has built-in 50Ω series termination which reduces BOM cost and area on the PCB. The following figure shows how to terminate the LVCMOS output.

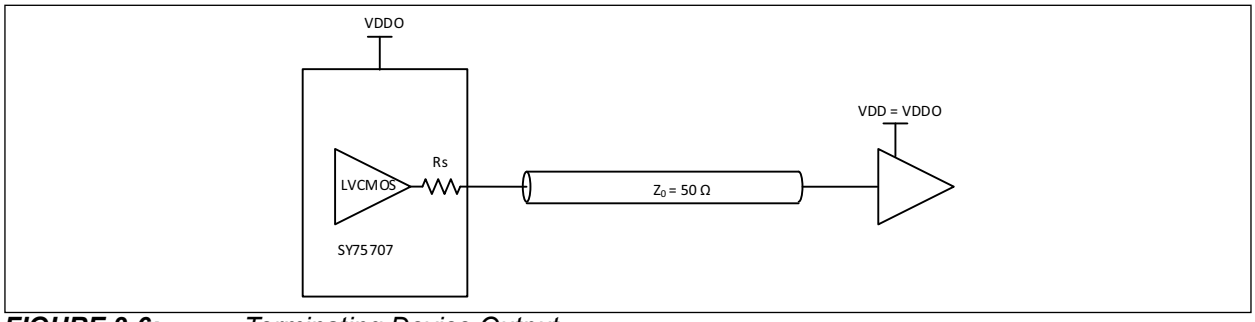


FIGURE 3-6: *Terminating Device Output.*

3.3 Power Supply Filtering

The power pins (VDDIN/VDDO) should be decoupled with a 0.1 µF capacitor with a minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R ceramic capacitors with a 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pin. To reduce the power noise from adjacent digital components on board, the power supply pin could be further insulated with a low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. The following figure shows recommended decoupling for each power pin.

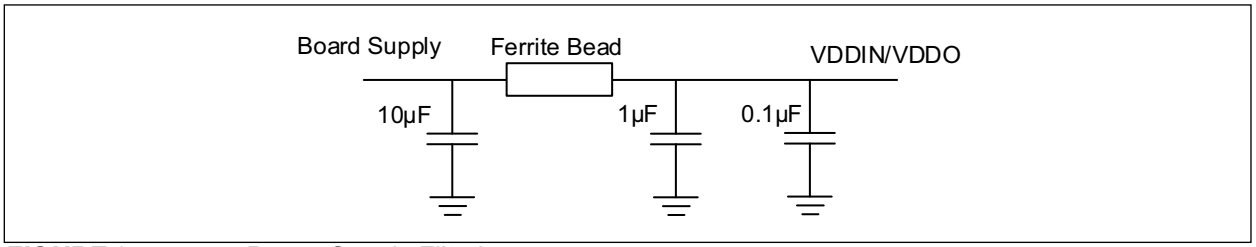
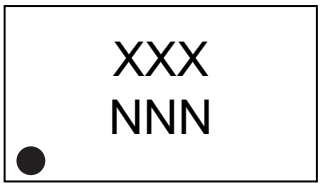


FIGURE 3-7: *Power Supply Filtering.*

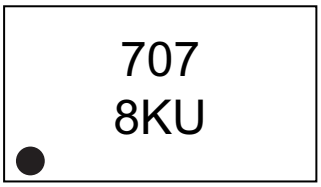
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Lead VDFN*



Example



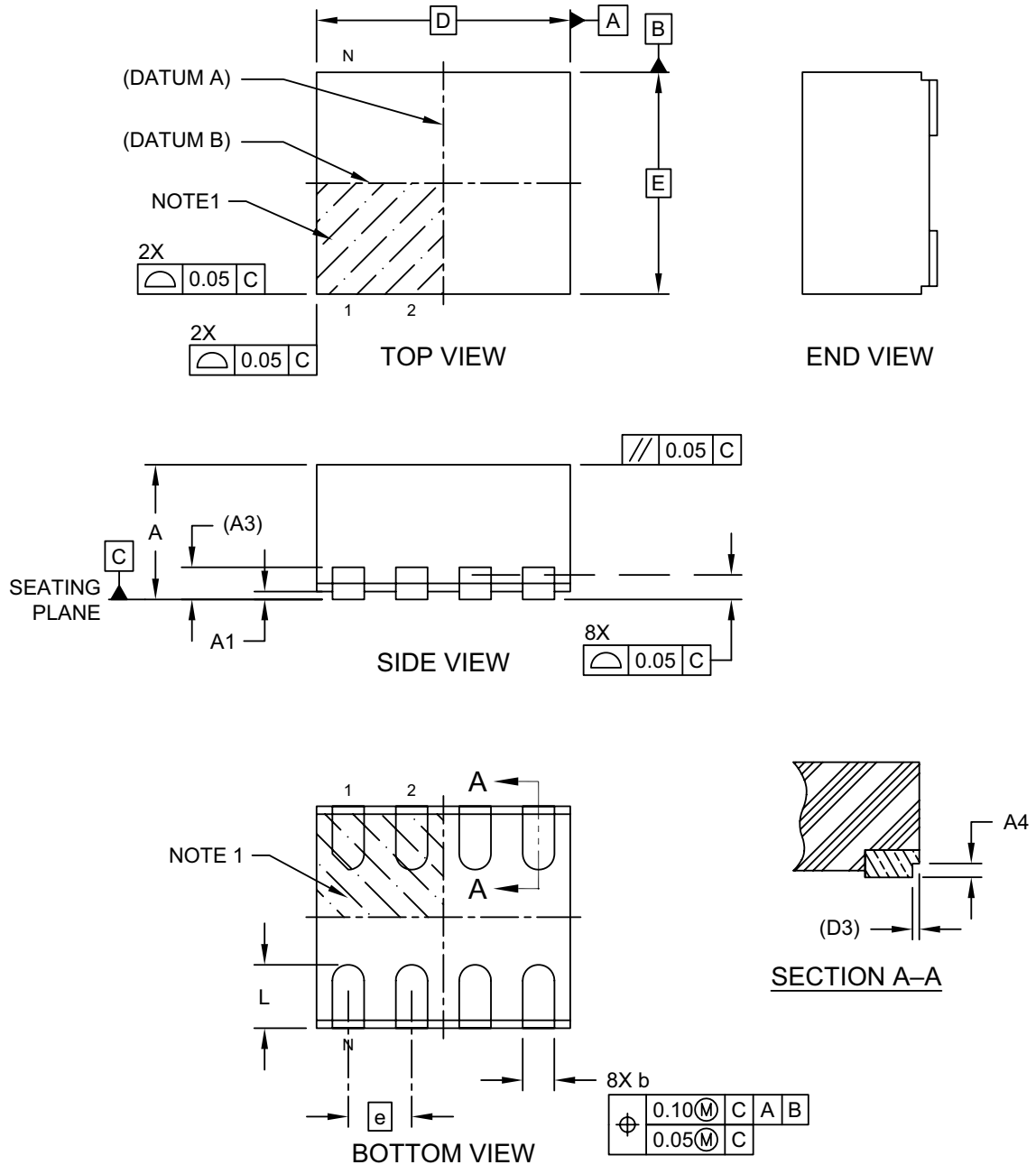
Legend:	XX...X	Product code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

8-Lead Very Thin Dual Flat, No Lead Package (NNC) - 1.6x1.4x0.9 mm Body [VDFN]
With Stepped Wettable Flanks

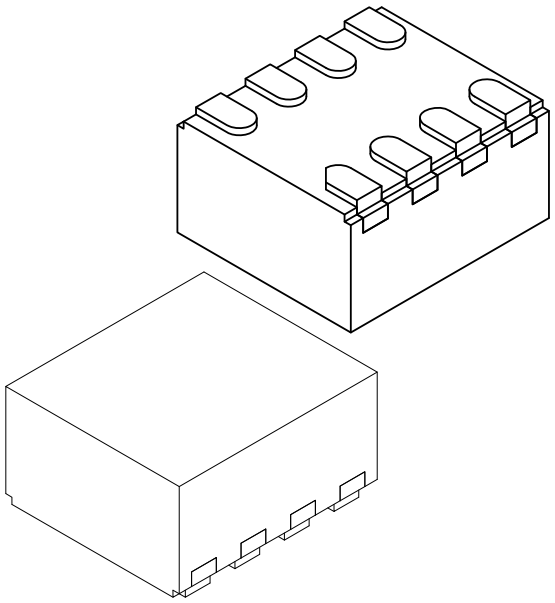
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25509 Rev A Sheet 1 of 2

8-Lead Very Thin Dual Flat, No Lead Package (NNC) - 1.6x1.4x0.9 mm Body [VDFN] With Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		1.60 BSC	
Overall Width	E		1.40 BSC	
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Wettable Flank Step Length	D3		0.05 REF	
Wettable Flank Step Height	A4	0.10	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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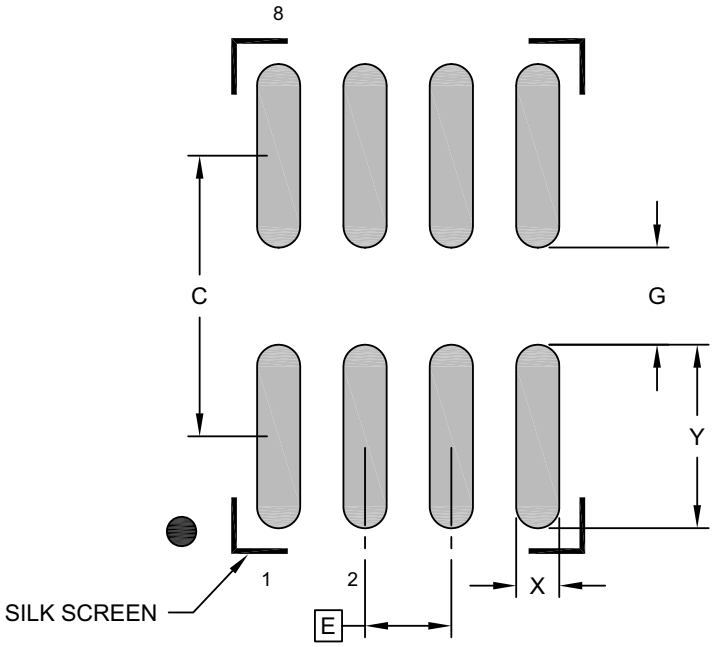
8-Lead Very Thin Dual Flat, No Lead Package (NNC) - 1.6x1.4x0.9 mm Body [VDFN]
With Stepped Wettable Flanks

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Contact Pad Spacing	C		1.30	
Contact Pad Width (Xnn)	X			0.20
Contact Pad Length (Xnn)	Y			0.85
Contact Pad to Contact Pad (Xnn)	G	0.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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APPENDIX A: REVISION HISTORY

Revision A (March 2026)

- Initial release of SY75707 as Microchip data sheet DS20007132A.

Revision B (May 2026)

- Updated the descriptions in Table 2-1.
- Updated the General Description.
- Updated in the Input Electrical Characteristics table.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	XXX	[-XX]
Device	Package	Media Type

Device:	SY75707:		2 Output Ultra-Low Additive Jitter Differential to 1.2V to 1.8V LVCMOS Buffer
Package:	TWL	=	8-Lead 1.4 mm x 1.6 mm VDFN (wettable flank)
Media Type:	TR	=	Tape and Reel (2,000/Reel)

Examples:

a) SY75707TWL-TR: 2 Output Ultra-Low Additive Jitter Differential to 1.2V to 1.8V LVCMOS Buffer, 8-Lead VDFN, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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