Datasheet

BL54LM20 Series

Version 0.3

Revision History

Version	Date	Notes	Contributor(s)	Approver
0.1	13 July 2026	Initial PRELIMINARY release.	Louis Chang	Jonathan Kaye
0.2	21 July 2026	1. Update module footprint in 8.2 2. Update Antenna performance measurement setup in 9.2	Louis Chang	Jonathan Kaye
0.3	28 Aug 2026	Updated datasheet for BL54LM20 Series, including BL54LM20B variant support and product information updates.	Louis Chang	Jonathan Kaye

Contents

1 Overview

Experience a new pinnacle of performance, efficiency, and security with our new BL54LM20 Series, built on Nordic Semiconductor's powerful **nRF54LM20** family. Elevating what you know and love from the nRF52 series, this next generation redefines Bluetooth LE and 802.15.4 solutions. Unleashing enhanced processing power, expanded memory, and innovative peripherals, the BL54LM20 Series is the ultimate choice for low power connectivity.

Powered by **Nordic's nRF54LM20A and nRF54LM20B** SoCs, our compact BL54LM20 Series modules deliver secure and robust Bluetooth LE and 802.15.4 with flexible programming via Nordic's nRF Connect SDK or Ezurio Canvas Software Suite.

Featuring a **128MHz ARM Cortex M33** and **128MHz RISC-V coprocessor**, supported by 2 MB non-volatile memory and 512 KB RAM. An extended peripheral set, including high-speed USB, brings out the full capabilities of the BL54LM20 Series, including up to **+8** dBm transmit power, **1.7V – 3.6V** supply considerations, and **NFC A-Tag** implementation.

The BL54LM20B further extends the platform with an integrated Axon Neural Processing Unit (NPU), enabling real-time on-device Edge AI applications with significantly improved inferencing performance and power efficiency. The integrated Edge AI accelerator provides up to 15× faster AI inferencing compared to CPU-only implementations.

It's further enhanced with state-of-the-art security and is designed for PSA Certified level 3 and supports services such as Secure Boot, Secure Firmware Update, Secure Storage plus protection from physical attacks.

Note: BL54LM20 Series hardware provides all functionality of the corresponding nRF54LM20A or nRF54LM20B chipset used in the module design. This is a hardware datasheet only – it does not cover the software aspects of the BL54LM20 Series. Information presented in this datasheet is derived from and references the Nordic nRF54LM20A and nRF54LM20B product documentation.

1.1 Features and Benefits

- **Nordic nRF54LM20 Series SoC**– 3.02 x 2.43 mm CAAA61 package with 40 GPIOs utilized.
- **Multi-protocol support:** Bluetooth LE, 802.15.4 (Thread & Matter)
- **Cortex M33** processor core: 128 MHz ARM Cortex M33
- **RISC-V** co-processor core: 128 MHz VPR
- **BL54LM20B only**:
  - Integrated Axon Neural Processing Unit (NPU)
  - Built-in Edge AI Accelerator
  - Up to 15× faster AI inferencing compared with CPU-only execution
- **Memory:** 2 MB non-volatile memory, 512 KB RAM
- **High Speed Peripherals**: - HS-SPI/UART, software defined peripherals on 128 MHz VPR, GPIO - 1x 64 MHz Port, 1.7 – 3.6V, 6 GPIOs
- **Low Leakage Peripherals:** 2x QDEC, 7x Timer, Global RTC, 2x WDT, NFC A-Tag, TEMP, I2S, COMP, 3x PWM, LPCOMP, 14-bit 8CH ADC, 7x TWI/SPI/UART, GPIO (3 x 8 MHz Port (P0, P1, P3), 34 GPIO's, 1.7-3.6V)
- **Antenna choice** – integrated pre-certified **On-Board Chip antenna** or external antenna support via **MHF4 connector**
- **Ultra-small footprint** (11 mm x 8 mm x 0.6 mm)
- **Extended** Industrial **Temperature Rating** (-40° to +85 °C)
- **Bluetooth LE**: Channel Sounding, LE 2M, LE Coded, LE Secure Connections & more
- **Qualified against Bluetooth Core 6.0**
- Firmware Over the Air **(FOTA)** via MCUboot and nRF Connect SDK
- **Hostless operation** – Multi Core MCU reduces BOM
- **Fully featured development kits** to jump-start Bluetooth LE development

1.2 Application Areas

- Building Automation
- Security
- Medical Peripherals
- Industrial Sensors

2 Specification

2.1 Specification Summary

Categories/Feature	Implementation
Specification	
Bluetooth®	Bluetooth Core 6.0 • Channel Sounding • GATT client & GATT server – Any adopted/custom services • Central/Peripheral roles • Mesh networking • LE CODED • LE 2M • LE Secure Connections • Extended Advertising • LE Power Control • DTM Firmware (Test Modes)
IEEE 802.15.4-2020 PHY	2405–2480 MHz IEEE 802.15.4-2020 compliant • 250kbps, 2450MHz, O-QPSK PHY • Channels 11-26. Channel 11 2405MHz and CH26 2480MHz. • Clear channel assessment (CCA) • Energy detection (ED) scan • CRC generation
Nordic proprietary 1Mbps, 2Mbps, 4Mbps modes radio	2402–2480 MHz Nordic proprietary 1Mbps and 2Mbps modes radio transceiver • 1Mbps nRF proprietary mode (ideal transmitter) • 2Mbps nRF proprietary mode (ideal transmitter) • 4Mbps nRF proprietary mode (ideal transmitter)
Frequency	2.402 - 2.480 GHz for BLE (CH0 to CH39) 2.405 - 2.480 GHz for IEEE 802.15.4-2020 PHY (CH11 to CH26)
Raw Data Rates	1 Mbps BLE (over-the-air) 2 Mbps BLE (over-the-air) 125 kbps BLE (over-the-air) 500 kbps BLE (over-the-air) 250 kbps IEEE 802.15.4-2020 (over-the-air) Nordic proprietary 1Mbps, 2Mbps and 4Mbps modes (over-the-air)
Maximum Transmit Power Setting	8 dBm — Chip antenna (453-00586 for BL54LM20A, 453-00672 for BL54LM20B) (Exclude antenna gain) 8 dBm — External antenna connection via on-module IPEX MHF4 (453-00585 for BL54LM20A, 453-00671 for BL54LM20B) (Test at MHF4 connector)
Minimum Transmit Power Setting	TBD dBm
Receive Sensitivity (≤37byte packet for BLE)	BLE 1 Mbps (BER=1E-3) — -94.5 dBm typical BLE 2 Mbps — -92 dBm typical BLE 125 kbps — -102.5 dBm typical BLE 500 kbps — -98 dBm typical IEEE 802.15.4-2020 250kbps — TBD dBm typical
Link Budget (conducted)	101.5 dB @ BLE 1 Mbps (using +7 dBm TX power) 109.5 dB @ BLE 125 kbps (using +7 dBm TX power)
NFC	
NFC-Type A Listen mode compliant	**Based on NFC forum specification:** 13.56 MHz, Date rate 106 kbps, NFC Type2 and Type 4 emulation **Modes of Operation:** Disable, Sense, Activated **Use Cases:** Touch-to-Pair with NFC, NFC enabled Out-of-Band Pairing

Security	Designed for PSA Certified Level 3 with Secure Boot, Secure Firmware Update, and Secure Storage. Integrated tamper sensors detect attacks and take action, and cryptographic accelerators are hardened against side-channel attacks.

Host Interfaces and Peripherals	Application Core (High Performance)	Software defined peripheral Core (ultra-low power)
Total	40 x multifunction I/O lines	
Processing Cores	Arm Cortex-M33 with DSP, FPU, TrustZone support. 2 MB non-volatile RRAM 512 KB RAM L1 cache 128MHz clock Uses voltage and clock frequency scaling	RISC-V CPU (VPR) fast lightweight peripheral processor (FLPR) dedicated for software defined peripherals 16MHz clock
GPIO	Up to 40 multifunction GPIO's	
	64MHz 1.7-3.6V GPIO port P2.00-P2.05	8MHz 1.7-3.6V GPIO port P0.03, P0.04, P0.06, P0.07, P0.08 P1.00, P1.01, P1.02, P1.03, P1.04, P1.05, P1.06, P1.07, P1.11, P1.13, P1.14, P1.15, P1.16, P1.19, P1.20, P1.21, P1.22, P1.24, P1.25, P1.26, P1.27, P1.28, P1.29, P1.30, P1.31 P3.01, P3.03, P3.04, P3.05
ADC (14-bit)	14-bit 62.5KS/s with oversampling 12-bit 125KS/s with oversampling 10-bit 2MS/s AIN0-AIN7 pins up to 8 programmable gain channels	
Global RTC (GRTC)		Implements full real time clock and calendar as shared system time. Can run in System OFF mode. Ultra-low power, 1us resolution, 52bits wide, uses 16MHz clock, 32.768kHz when other power modes.
USB	The USBHS (USB high speed) peripheral is a USB 2.0 device that supports USB 2.0 and is backward compatible with the USB 1.1 Specification.	
High Speed SPI/UART	1 x	
SPI/UART/TWI		7x
PWM		3x 4 channels PWM
I2S		1x I2S (Inter-IC sound interface)
PDM		1x PDM (Pulse code modulation interface) for digital microphones
NPU (BL54LM20B only)	Integrated Axon Neural Processing Unit (Axon NPU) Built-in Edge AI Accelerator Supports up to 15× faster AI inferencing compared with CPU-only execution	N/A
TIMER		7x Timer (32bit)
QDEC		2x QDEC (Quadrature decoder)
COMP		1x COMP (comparator)
LPCOMP		1x LPCOMP (low power comparator)

Host Interfaces and Peripherals	Application Core (High Performance)	Software defined peripheral Core (ultra-low power)
TEMP		1x Temperature sensor Temperature range equal to operating temperature range
WDT		2x WDT (Watchdog timer)
NFC A-Tag		1x
Wakeup pins		34x
External optional 32.768 kHz crystal		Not needed for normal radio operation. Optionally, connect +/-20ppm accuracy crystal for more accurate protocol timing. Fit associated load capacitor for crystal or use nRF54LM20 internal load capacitor, which is configurable as 3 pF to 18 pF in 0.65 pF steps on pins XL1, XL2.
Security	Designed for PSA Certified Level 3 with Secure Boot, Secure Firmware Update, and Secure Storage. Integrated tamper sensors detect attacks and take action, and cryptographic accelerators are hardened against side-channel attacks.	

Programmability	**Via SWD (JTAG) 2 wire interface**	
Options	**Nordic nRF Connect SDK:** Software/Support available from Nordic directly https://devzone.nordicsemi.com/ **Canvas SW Suite**: Software/ Support available from https://www.ezurio.com/canvas/software-suite	
FW upgrade	Via SWD (JTAG) 2 wire interface or UART	
Supply Voltage	Normal Voltage Mode (VDD_nRF): 1.7V-3.6V	
Power Consumption		
Active Modes Peak Current (for max Tx power +7dBm) – Radio only	mA peak Tx, 15mA avg TX@ 1.8V, LE1M mA peak Tx, 23mA avg TX@ 1.8V, CW mA peak Tx, 8.3mA avg TX@ 3.3V, LE1M mA peak Tx, 12.6mA avg TX@ 3.3V, CW	
Active Modes Peak Current (for Tx power -40dBm) – Radio only	mA peak Tx, 2.5mA avg TX @ 1.8V, LE1M mA peak Tx, 3.1mA avg TX@ 1.8V, CW mA peak Tx, 2.1mA avg TX @ 3.3V, LE1M mA peak Tx, 2.6mA avg TX @ 3.3V, CW	TBD
Active Modes Average Current	Depends on many factors.	
Ultra-low Power Modes	System ON Idle	uA (System ON IDLE with GRTC (XOSC) and 512KB RAM)
	System OFF	uA
Antenna Options		
Internal	Chip antenna – on-board (453-00586 for BL54LM20A, 453-00672 for BL54LM20B)	
External	Connection via *on-module* IPEX MHF4 (453-00585 for BL54LM20A, 453-00671 for BL54LM20B)	
Physical		
Dimensions	11mm x 8mm x 0.6mm Pad Pitch – 0.65 mm Pad Type – LGA - Land Grid Array	
Weight	<1 gram	
Environmental		
Operating	-40 °C to +85 °C	
Storage	-40 °C to +85 °C	
Miscellaneous		
Lead Free	Lead-free and RoHS compliant	
Warranty	One-Year Warranty	

Development Tools	
Development Kit	For development with either the BL54LM20A or BL54LM20B, Ezurio recommends the BL54LM20B development kits: 453-00672-K1 and 453-00671-K1.
Development Tools	Nordic nRFConnect - Android and iOS applications UART firmware upgrade Xbit Tools and utilities
Bluetooth®	Full Bluetooth SIG Declaration ID
FCC/ISED/CE/MIC/RCM/UKCA/KC	All BL54LM20 Series

3 Hardware Specifications

3.1 Block Diagram and Pin-out

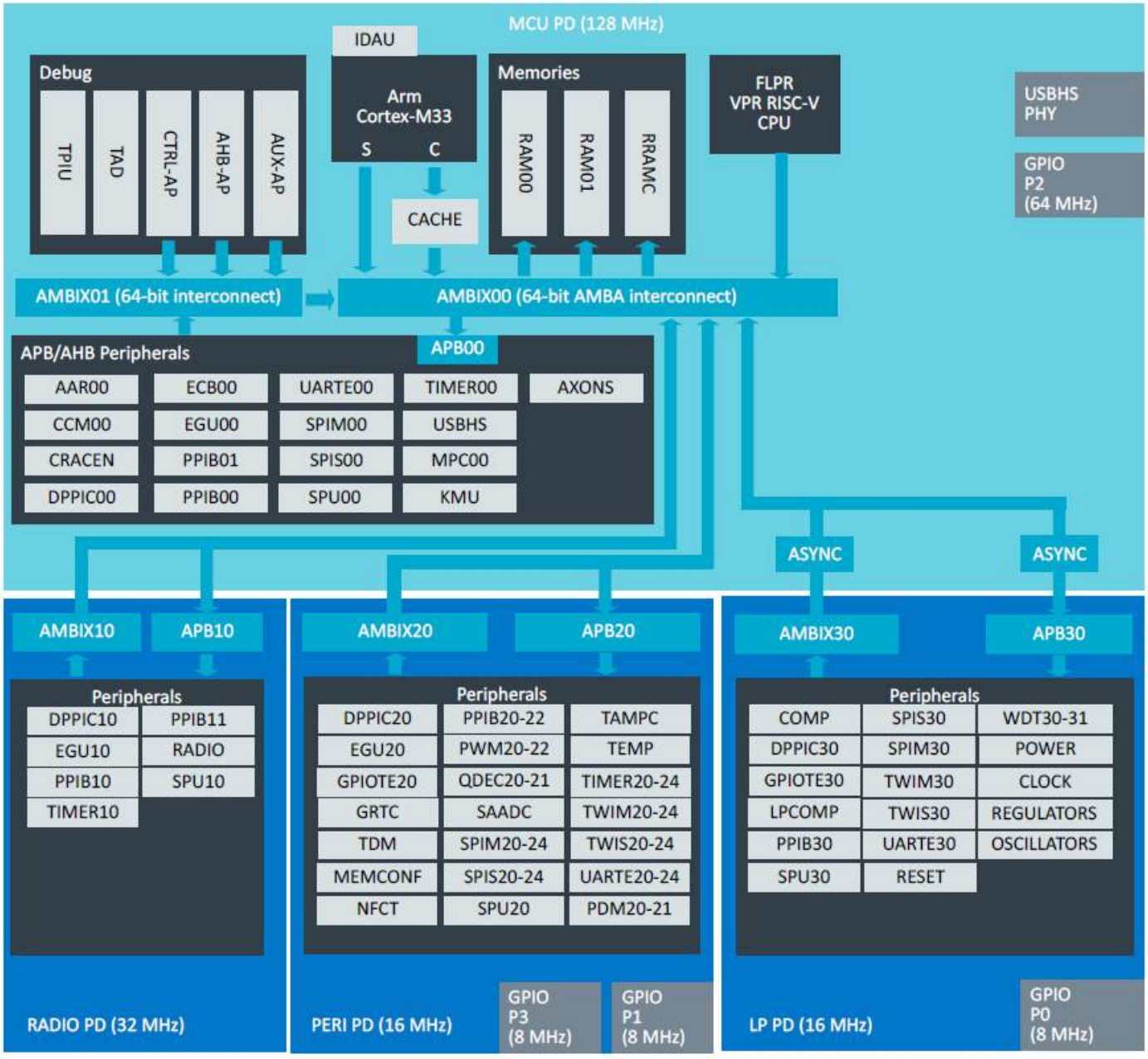


Figure 1: BL54LM20 Series HW block diagram

Note : The AXONS neural processing unit (NPU) shown in the block diagram is available on BL54LM20B variants only.

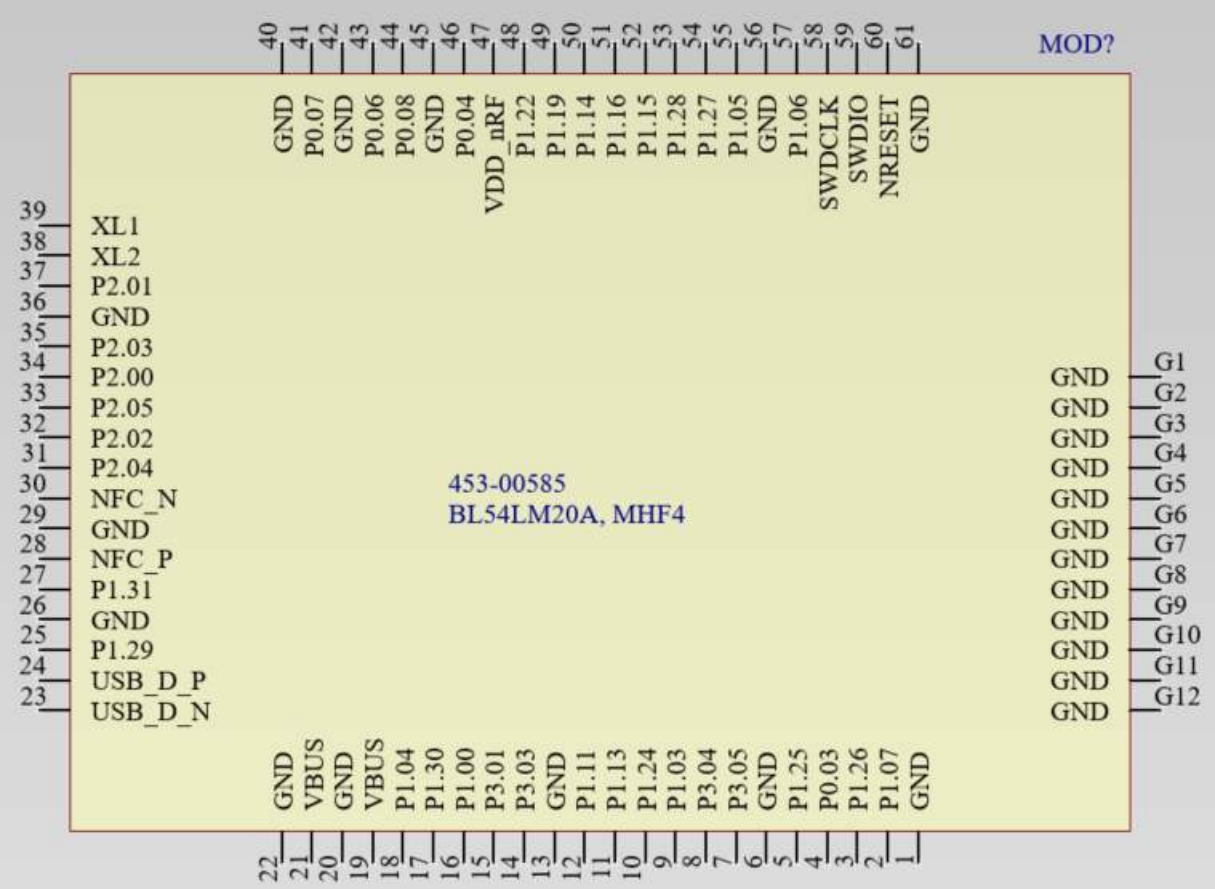


Figure 2: Top view - Schematic symbol for BL54LM20 Series Module (Nordic nRF54LM20A / B)

3.2 Pin Definitions

Table 1: Pin definitions

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54LM20 Series CSP61 Pin	nRF54LM20 Series CSP61 Name	Description	Dedicated function	Default function designed on DVK
1	GND	-	VSS			
2	P1.07	H5	P1.07 EXTREF	General Purpose I/O GRTC CLKOUTFAST ADC external reference	GRTC	Spare
3	P1.26	B8	P1.26 ASI [3]	General Purpose I/O TAMPC active shield 3 input		Button0 control
4	P0.03	H4	P0.03	General Purpose I/O GRTC PWM	GRTC	Button3 control
5	P1.25	D7	P1.25 ASO [3]	General Purpose I/O TAMPC active shield 3 output	TAMPC	LED1 control
6	GND		VSS			
7	P3.05	G4	P3.05	General Purpose I/O		Spare
8	P3.04	G5	P3.04	General Purpose I/O		MIKROE RESET

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54LM20 Series CSP61 Pin	nRF54LM20 Series CSP61 Name	Description	Dedicated function	Default function designed on DVK
9	P1.03	G9	P1.03 AIN7	General Purpose I/O Analog input		MIKROE SPI CS
10	P1.24	E6	P1.24	General Purpose I/O		MIKROE SPI SCK
11	P1.13	F1	P1.13	General Purpose I/O		MIKROE SPI MISO
12	P1.11	F2	P1.11	General Purpose I/O		MIKROE SPI MOSI
13	GND		VSS			
14	P3.03	F5	P3.03	General Purpose I/O		MIKROE/QWIIC/PMIC SCL
15	P3.01	F6	P3.01	General purpose I/O		MIKROE/QWIIC/PMIC SDA
16	P1.00	H10	P1.00 AIN0	General Purpose I/O Analog input		MIKROE INT
17	P1.30	F9	P1.30 AIN2	General Purpose I/O Analog input		MIKROE AN
18	P1.04	G8	P1.04 AIN6	General Purpose I/O Analog input		MIKROE INT
19	VBUS	H9	VBUS	USB 5V supply	USB	
20	GND		VSS			
21	VBUS	H9	VBUS	USB 5V supply	USB	
22	GND		VSS			
23	USB_D_N	H6	D-	USB D- line	USB	
24	USB_D_P	H7	D+	USB D+ line	USB	
25	P1.29	E9	P1.29 AIN3	General Purpose I/O Analog input		MIKROE UART TX
26	GND		VSS			
27	P1.31	G10	P1.31 AIN1	General Purpose I/O Analog input		MIKROE PWM
28	NFC_P	F8	P1.02 NFC2	General Purpose I/O NFC antenna pin 2	NFC	NFC
29	GND		VSS			
30	NFC_N	E8	P1.01 NFC1	General Purpose I/O NFC antenna pin 1	NFC	NFC
31	P2.04	D10	P2.04 FLPR.2 QSPI.D1 SPIM00.SDI SPIS00.SDI UARTE00.CTS	General Purpose I/O General Purpose I/O QSPI D1 SPIM00 SDI SPIS00 SDI UARTE00 CTS	 FLPR FLPR(QSPI) SPIM00 SPIS00 UARTE00	QSPI_IO1
32	P2.02	B10	P2.02 FLPR.1 QSPI.D0 SPIM00.SDO SPIS00.SDO UARTE00.TXD	General Purpose I/O General Purpose I/O QSPI D0 SPIM00 SDO SPIS00 SDO UARTE00 TXD	 FLPR FLPR(QSPI) SPIM00 SPIS00 UARTE00	QSPI_IO0

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54LM20 Series CSP61 Pin	nRF54LM20 Series CSP61 Name	Description	Dedicated function	Default function designed on DVK
33	P2.05	D9	P2.05 FLPR.5 QSPI.CSN SPIM00.CSN SPIS00.CSN UARTE00.RTS	General Purpose I/O General Purpose I/O QSPI CSN SPIM00 CSN SPIS00 CSN UARTE00 RTS	 FLPR FLPR(QSPI) SPIM00 SPIS00 UARTE00	QSPI_CS
34	P2.00	A10	P2.00 FLPR.4 QSPI.D3 SPIM00.DCX UARTE00.RXD	General Purpose I/O General Purpose I/O QSPI D3 SPIM00 DCX UARTE00 RXD	 FLPR FLPR(QSPI) SPIM00 UARTE00	QSPI_IO3
35	P2.03	B9	P2.03 FLPR.3 QSPI.D2	General Purpose I/O QSPI D2	 FLPR FLPR (QSPI)	QSPI_IO2
36	GND		VSS			
37	P2.01	A9	P2.01 FLPR.0 QSPI.SCK SPIM00.SCK SPIS00.SCK	General Purpose I/O General Purpose I/O QSPI SCK SPIM00 SCK SPIS00 SCK	 FLPR FLPR (QSPI) SPIM00 SPIS00	QSPI_SCK
38	XL2	B7	P1.21 RADIO [6] XL2	General Purpose I/O Radio DFE GPIO Connection for 32.768 kHz crystal	 Radio	32.768K crystal
39	XL1	B6	P1.20 RADIO [5] XL1	General Purpose I/O Radio DFE GPIO	 Radio	32.768K crystal
40	GND					
41	P0.07	G2	P0.07	General Purpose I/O		UART0 RXD
42	GND					
43	P0.06	H1	P0.06	General Purpose I/O		UART0 TXD
44	P0.08	G1	P0.08	General Purpose I/O		UART0 RTS
45	GND					
46	P0.04	H2	P0.04	General Purpose I/O GRTC CLKOUT32K	 GRTC	UART0 CTS
47	VDD_nRF	A4, E10	VDD	VDD for DCDC		
48	P1.22	D6	P1.22	General Purpose I/O		LED0 control
49	P1.19	E5	P1.19 RADIO [4]	General Purpose I/O Radio DFE GPIO	 Radio	UART1 CTS
50	P1.14	F4	P1.14	General Purpose I/O		UART1 RTS
51	P1.16	B5	P1.16 ASI [2] RADIO [1]	General Purpose I/O TAMPC active shield 2 input Radio DFE GPIO	 TAMPC Radio	UART1 TXD

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54LM20 Series CSP61 Pin	nRF54LM20 Series CSP61 Name	Description	Dedicated function	Default function designed on DVK
52	P1.15	B4	P1.15 ASO [2] RADIO [0]	General Purpose I/O TAMPC active shield 2 output Radio DFE GPIO	TAMPC Radio	UART1 RXD
53	P1.28	D8	P1.28	General Purpose I/O		LED3 control
54	P1.27	E7	P1.27	General Purpose I/O		LED2 control
55	P1.05	F7	P1.05 AIN5 ASO [0]	General Purpose I/O Analog input TAMPC active shield 0 output		Button1 control
56	GND		VSS			
57	P1.06	G7	P1.06 AIN4 ASI [0]	General Purpose I/O Analog input TAMPC active shield 0 input	TAMPC	Button2 control
58	SWDCLK	D5	SWDCLK	Serial wire clock. Input with pulldown.		SWD
59	SWDIO	E4	SWDIO	Serial wire data. Bidirectional with high-drive and pull-up.		SWD
60	NRESET	E2	nRESET	Chip nReset input with pull-up		SWD
61	GND		VSS			
G1~G12	GND		VSS			

Pin Definition Notes:

Note 1 GPIO	GPIO = General Input or Output (GPIO level voltage tracks VDD pin). AIN =Analog input. If GPIO is selected as an input, ensure the input is not floating (which can cause current consumption to drive with time in low power modes (such as System ON Idle), by selecting the internal pull up or pull down. Must connect all GND pads to host board PCB GND plane.
Note2 Clock for serial interfaces or trace	Some peripherals (SPI, TWI, PDM, I2S, GRTC) have clock signals. Dedicated clock pins have been optimized to ensure correct timing relationship between clock and data signal for these peripherals. Pins that can be used as clock signals are shown with pin name in red colour. The peripheral data signal must be configured to use pins close to the clock pin. This ensures that the internal paths from the peripheral to the pin have the same delay, so that the data and clock signals reach the pins at the same time. For high-speed signals, the printed circuit board (PCB) layout must use short PCB traces of identical length. This makes sure any delays are kept to a minimum and it assures close to identical delay and clock path.

Pin #	Pin Name (red coloured pins for clock for interfaces, trace)	nRF54LM20 Series CSP61 Pin	nRF54LM20 Series CSP61 Name	Description	Dedicated function	Default function designed on DVK
Note 3 Dedicated pins		**GRTC:** Has dedicated pins for clock and PWM output. **TAMPC:** Has dedicated pins for active shield inputs and outputs. **FLPR:** Uses dedicated pins on GPIO port P2 for emulated peripherals such as QSPI. **RADIO:** Uses dedicated pins on GPIO port P1 for antenna switch control (DFEGPIO for direction finding). **NFC:** Uses dedicated pins as listed in the pin assignments table for the selected device. These pins are configured as NFC antenna pins from reset. To use the pins for Digital I/O, NFC function must be disabled.				
Note 4 SWDIO /SWCLK / nRESET / VDD / GND		Customer MUST bring out SWDIO, SWCLK, nRESET, VDD, GND for programming purposes.				
Note 5		The BL54LM20A and BL54LM20B modules share an identical pinout and footprint. Pin assignments shown in this section apply to both module variants.				

3.3 Electrical Specifications

3.3.1 Absolute Maximum Ratings

Absolute maximum ratings are the extreme limits for supply voltage and voltages on digital and analogue pins of the module are listed below; exceeding these values causes permanent damage.

Table 2: Absolute maximum ratings

Parameter	Min	Max	Unit
Supply Voltages			
VDD_nRF	-0.3	3.9	V
VBUS	-0.3	6	V
I/O pin voltage			
Voltage at GPIO pin (at VDD_nRF ≤3.6V)	-0.3	VDD_nRF + 0.3	V
Voltage at GPIO pin (at VDD_nRF >3.6V)	-0.3	3.9	V
NFC antenna pin current (NFC1/2)	-	130	mA
Environmental			
Storage temperature	-40	+125	°C
MSL (Moisture Sensitivity Level)	-	4	-
ESD (as per EN301-489)			
Conductive		4	kV
Air Coupling		8	kV
RRAM Endurance (Note 1)	10,000		Write/rewrite cycles
RRAM Retention	10 years at 85°C		years

Absolute maximum Ratings Notes:	
Note 1	Applications with frequent non-volatile memory updates should implement appropriate memory management techniques to maximize RRAM endurance.

3.3.2 Recommended Operating Parameters

Table 3: Power supply operating parameters

Parameter	Min	Typ	Max	Unit
VDD_nRF supply range (Note)	1.7		3.6	V
VDD_POR during power-on reset	1.75			V
VBUS	3.67	5	5.5	V
Operating Temperature Range	-40	+25	+85	°C
Recommended storage temperature		40		°C

Recommended Operating Parameters Notes:

Note 2 VDD_nRF supply is required for device operation. VBUS is optional and is only used to supply the USB physical interface when the USB interface is in use. VBUS cannot be used to power the device.

3.4 Clocks

3.4.1 HFXO - 32MHz crystal oscillator and nRF54LM20 internal load capacitor mandatory setting

The BL54LM20 Series module contains a 32 MHz crystal. The load capacitors used for the 32 MHz crystal oscillator are integrated inside the nRF54LM20 device. The internal load capacitance can be configured from 4 pF to 17 pF in 0.25 pF steps if needed.

The 32 MHz crystal inside the BL54LM20 module is a high accuracy crystal (±15 ppm at room temperature) that helps with radio operation and reduce power consumption in the active modes.

3.4.2 LFCLK – Low Frequency clock source

There are four possibilities (see Figure 3) for the low frequency clock (LFCLK) and options are:

LFRC (32.768kHz RC oscillator): The Internal 32.768 kHz RC oscillator (LFRC) is fully embedded in the nRF54LM20 device (and does not require additional external components) with an accuracy ±250 ppm (after calibration of LFRC at least every eight seconds using the HFCLK as a reference oscillator).

LFXO (32.768kHz crystal oscillator): For higher LFCLK accuracy (greater than ±250ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used. To use LFXO, a 32.768kHz crystal must be connected between the XL1 and XL2 pins and the load capacitance between each crystal terminal and ground. Optionally internal capacitors of maximum 18 pF in 0.65 pF steps are provided on pins XL1 and XL2.

Low frequency (32.768 kHz) external source: The 32.768 kHz oscillator (LFXO) is designed to work with external sources

LFSYNT (32.768kHz Synthesized clock) from HFCLK (LFSYNT): The LFCLK can be synthesized from the HFCLK source. LFSYNT depends on the HFCLK to run. The accuracy of the LFCLK clock with LFSYNT as a source assumes the accuracy of the HFCLK. If high accuracy is required, the HFCLK must be generated from the HFXO. Using the LFSYNT clock removes the requirement for an external 32.768kHz crystal but increases the average power consumption as the HFCLK will be turned on in the system.

3.4.3 Other Internal Clocks

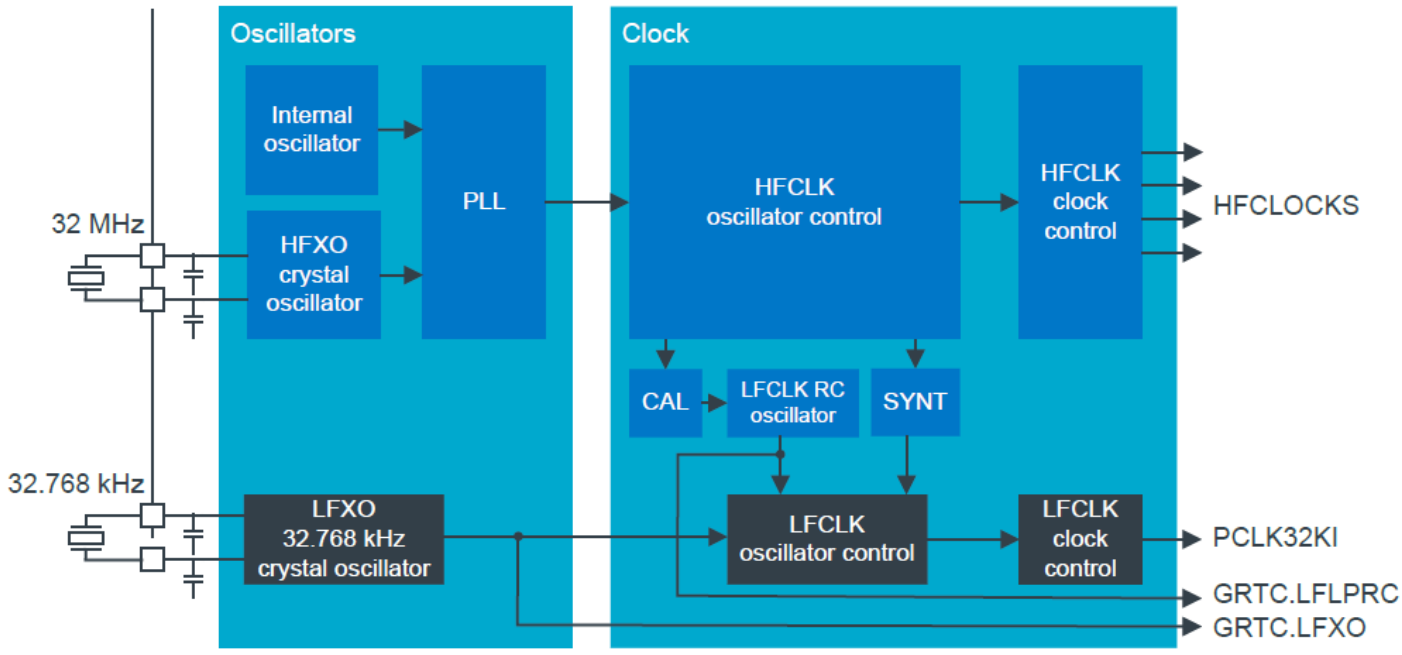


Figure 3: nRF54LM20 Clock System Overview (adapted from Nordic)

3.5 BL54LM20 Series Power Supply

The main supply voltage (1.7V-3.6V) is connected to VDD_nRF pin (pin47). See Figure 4.

The device also has an USB regulator, which is provided by VBUS and only powers the USB physical interface. It will not power the device.

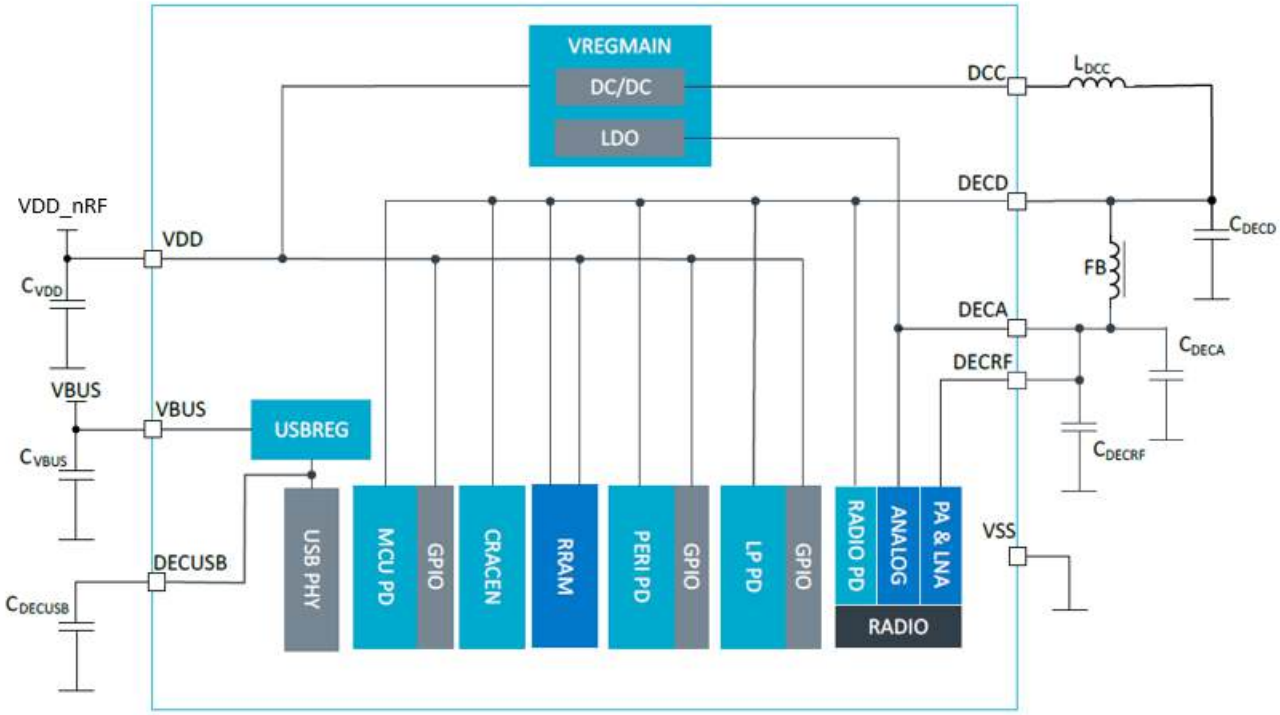


Figure 4: Regulator configuration

4 Programmability

4.1 BL54LM20 Series Default Firmware

The BL54LM20 Series modules are shipped from Ezurio manufacturing facilities with no firmware programmed.

4.2 BL54LM20 Series Firmware Options

Firmware for use with the BL54LM20 Series can be divided into the following types.

- **Bootloader –** This software resides on the Arm Cortex-M33 Application Core and is responsible for boot management and firmware updates of the Application and FLPR images.
- MCUboot or Trusted Firmware-M (TF-M) bootloaders are recommended as the basis for implementing bootloader functionality on the BL54LM20 Series.
- **Application** – This is the main application running on the Arm Cortex-M33 Application Core. It interfaces with the integrated radio stack(s) and provides supplementary functionality in addition to the time-critical activities performed for radio operation.
- **Software Defined Peripheral** – Software running on the dedicated RISC-V FLPR (Fast Lightweight Peripheral Processor) core used for software-defined peripheral implementations and offloaded processing tasks.

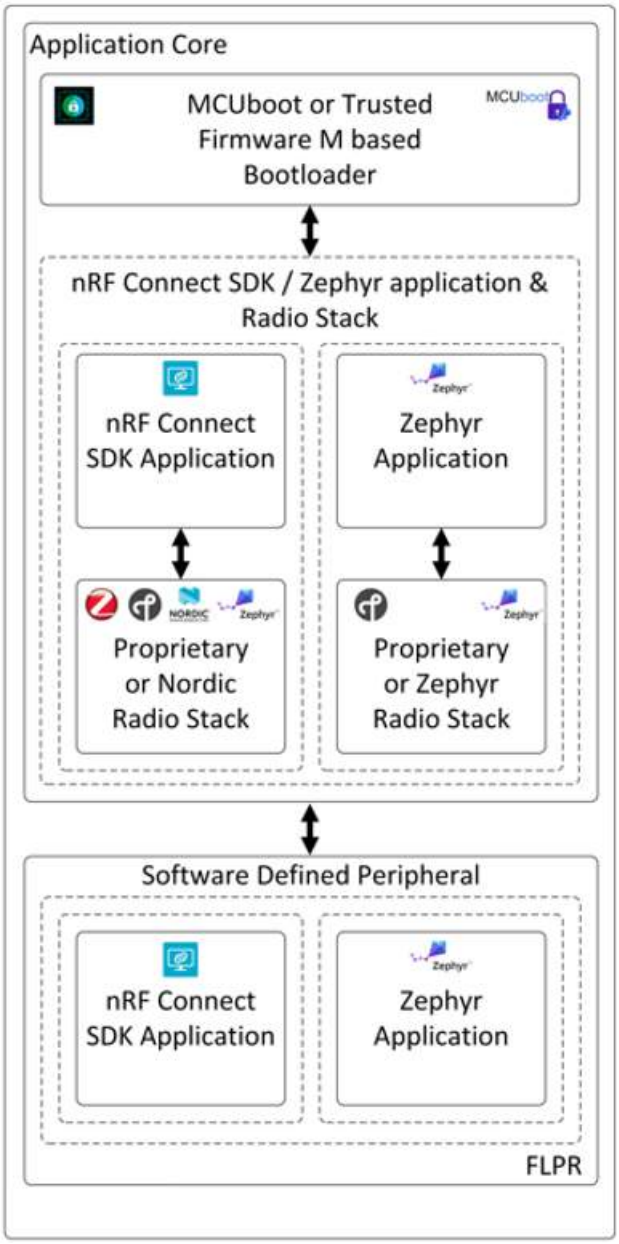


Figure 5 : Functional software architecture of the BL54LM20 Series.

5 Peripherals

Feature		
Memory	Non-volatile memory (RRAM)	2036 KB
	Random access memory (RAM)	512 KB
AI Processing	Axon Neural Processing Unit (NPU)	BL54LM20B only
Radio	Bluetooth Low Energy	Yes
	Bluetooth Low Energy Coded PHY (Long range)	Yes
	Bluetooth Constant Tone Extension (Direction-finding)	Yes
	IEEE 802.15.4	Yes
GPIO pins	GPIO pins	40
	Wakeup-pins	34
	Analog input pins	8
	GPIO voltage	VDD_nRF (1.7V-3.6V)
Peripherals	Timers (TIMER)	7
	Real-time counter (RTC)	-
	Global real-time counter (GRTC)	1
	Serial interfaces (UART, SPI, TWI)	7
	Temperature sensor	Yes
	Comparator (COMP)	Yes
	Successive Approximation ADC (SAADC)	Yes
	Quadrature decoder (QDEC)	2
	Inter-IC sound interface (I2S)	1
	Near-field communication (NFC)	Yes
	Pulse density modulation interface (PDM)	2
	Pulse-width modulator (PWM)	3
	Watchdog timer (WDT)	2
Security	Active tamper shield pin pairs (in/out)	4
	Glitch detectors	Yes
	Key management unit	Yes
	Cryptographic accelerator (CRACEN)	Yes
Debug	ITM parallel trace	Yes

6 SW requirements related to hardware

6.1 32MHz crystal internal load capacitor setting

The BL54LM20 Series module includes a 32 MHz crystal. The load capacitors required for the crystal oscillator are integrated within the nRF54LM20 device. The internal load capacitance can be configured from 4 pF to 17 pF in 0.25 pF steps, or the default setting may be used.

6.2 32.768KHz Low frequency clock load capacitor setting

The BL54LM20 Series supports multiple low frequency clock (LFCLK) sources for low power operation and timekeeping functions.

The available LFCLK sources are:

- LFRC – Internal 32.768 kHz RC oscillator
- LFXO – External 32.768 kHz crystal oscillator connected to XL1 and XL2
- External 32.768 kHz clock source
- LFSYNT – Synthesized 32.768 kHz clock derived from the HFCLK

The LFCLK source is configured in software.

For applications requiring the highest timing accuracy and lowest long-term frequency drift, the LFXO source is recommended. The optional 32.768 kHz crystal oscillator uses internal load capacitors integrated within the nRF54LM20 device. The internal load capacitance can be configured from 3 pF to 18 pF in 0.65 pF steps to match the crystal load capacitance requirements.

When lower BOM cost is preferred and frequency accuracy is less critical, the internal LFRC may be used without any external components.

Using LFSYNT removes the requirement for an external 32.768 kHz crystal but increases overall power consumption because the high-frequency clock must remain active to generate the LFCLK.

7 Hardware Integration Suggestions

7.1 Circuit

The following are suggestions for your design for the best performance and functionality.

Checklist (for Schematic):

- **BL54LM20 Series power supply:**

  External supply voltage (1.7V-3.6V) is connected to both VDD_nRF pin (pin47).

  5V is used to provide to VBUS (input of USB regulator), which only powers the USB physical interface. It will not power the device.

  External power source should be within the operating range, rise time and noise/ripple specification of the BL54LM20 Series. Add decoupling capacitors for filtering the external source. Power-on reset circuitry within BL54LM20 Series module incorporates a brown-out detector, thus simplifying your power supply design. Upon application of power, the internal power-on reset ensures that the module starts correctly.

- **AIN (ADC) and GPIO pin IO voltage levels**
  BL54LM20 Series GPIO voltage levels are at VDD_nRF. Ensure input voltage levels into GPIO pins are at VDD_nRF also. Ensure ADC pin maximum input voltage for damage is not violated.

- **AIN (ADC) impedance and external voltage divider setup**
  If you need to measure with ADC a voltage higher than 3.6V, you can connect a high impedance voltage divider to lower the voltage to the ADC input pin.

- **SWD**
  This is REQUIRED for loading firmware. MUST wire out the SWD two wire interface on host design. Five lines should be wired out, namely SWDIO, SWDCLK, nRESET, GND and VDD.

- **UART and flow control (CTS, RTS)**
  Required if customer requires UART.

- **TWI (I2C)**
  It is essential to remember that pull-up resistors on both SCL and SDA lines are required, the value as per I2C standard. The nRF54LM20 device provides internal pull-up resistors (typically 14 kΩ). For other values, fit external pull-up resistor on both SCL and SDA as per I2C specification to set speed. The I2C specification allows a line capacitance of 400pF.

- **QSPI, High Speed SPI, High speed TWI (I2C, 1Mbps)**
  High-Speed SPI, TWI come on dedicated GPIO pins only. Other lower speed SPI and TWI can come out on any GPIO pins.
  For all high-speed signals, the printed circuit board (PCB) layout must ensure that connections are made using short PCB traces.

- **GPIO pins**
  If GPIO is selected as an input, ensure the input is not floating, which may increase current consumption in low power modes such as System ON Idle, by selecting the internal pull up or pull down.

- **NFC antenna connector**
- To make use of the Ezurio flexi-PCB NFC antenna (part # 0600-00061), fit connector:
  - Description – FFC/FPC Connector, Right Angle, SMD/90d, Dual Contact,1.2 mm Mated Height
  - Manufacturer – Molex
  - Manufacturers Part number – 512810598

  Add tuning capacitors of 300 pF on NFC1 pin to GND and 300 pF on NFC2 pins to GND if the PCB track length is similar as development board.

- **nRESET pin (active low)**
  Hardware reset. Wire out to push button or drive by host.
  By default module is out of reset when power applied to VDD_nRF pins (14K pull-ups inside nRF54LM20 device).

- **Optional External 32.768kHz crystal**

  If the optional external 32.768kHz crystal is needed, then use a crystal that meets specifications and add load capacitors (either using the internal load capacitors integrated within the nRF54LM20 device or discrete capacitors outside BL54LM20 Series module), whose values should be tuned to meet all specification for frequency and oscillation margin.

7.2 PCB Layout on Host PCB - General

Checklist (for PCB):

- MUST locate BL54LM20 Series module close to the edge of PCB (mandatory for the 453-00586 for on-board chip antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- All module GND pins MUST be connected to host PCB GND.
- Place GND vias close to module GND pads as possible.
- Unused PCB area on surface layer can flooded with copper but place GND vias regularly to connect the copper flood to the inner GND plane. If GND flood copper is on the bottom of the module, then connect it with GND vias to the inner GND plane.
- Route traces to avoid noise being picked up on VDD_nRF supply and AIN (analogue), GPIO (digital) traces and high-speed traces.
- Ensure no exposed copper is on the underside of the module (refer to land pattern of BL54LM20B development board).

7.3 PCB Layout on Host PCB for 453-00586 or 453-00672

7.3.1 Antenna Keep-out on Host PCB

The 453-00586 or 453-00672 has an integrated chip antenna and its performance is sensitive to host PCB. It is critical to locate 453-00586 or 453-00672 on the edge of the host PCB (or corner) to allow the antenna to radiate properly. Refer to guidelines in section Host PCB Land Pattern and Antenna Keep-out for the 453-00586 and 453-00672 or 453-00672. Some of those guidelines are repeated below.

- Ensure there is no copper in the antenna keep-out area on any layers of the host PCB. Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
- For best antenna performance, place the 453-00586 or 453-00672 module on the edge of the host PCB, preferably in the edge center.
- The BL54LM20B development board (453-00672-K1) has the 453-00672 module on the edge of the board (not in the corner). The antenna keep-out area is defined by the BL54LM20B development board shown in Figure 6 which was used for module development and antenna performance evaluation, where the antenna keep-out area is ~2.943mm wide, ~5.875mm long; with HOST PCB dielectric (no copper) height ~1.6 mm sitting under the 453-00672 integrated chip antenna module.
- The integrated chip antenna used on the 453-00586 and 453-00672 modules is tuned when the module is mounted on the development board (host PCB) with dimensions of 116 mm × 68.5 mm × 1.57 mm.
- A different host PCB thickness dielectric will have small effect on antenna.
- The antenna-keep-out is defined in the **Error! Reference source not found.** section.

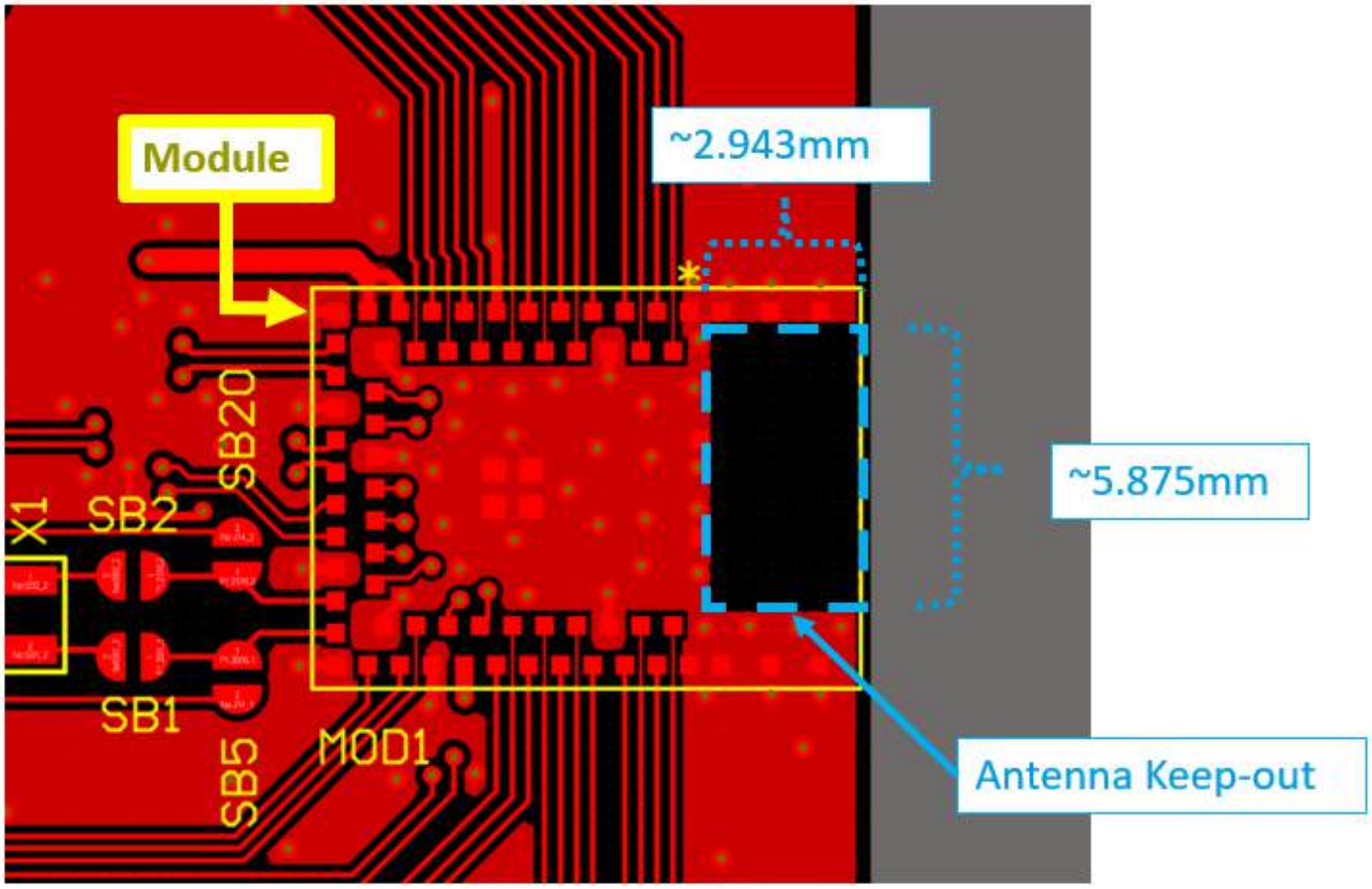


Figure 6 : Chip Antenna keep-out area (shown in blue) from the BL54LM20B development board for the 453-00672 module.

Antenna Keep-out Notes:	
Note 1	The BL54LM20 Series module is placed on the edge, preferably edge centre of the host PCB.
Note 2	Copper cut-away on all layers in the *Antenna Keep-out* area under the 453-00586 or 453-00672 on host PCB.

7.3.2 Antenna Keep-out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40 mm top/bottom and 30 mm left or right.
- Metal close to the 453-00586 or 453-00672 chip antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. The amount of that degradation is entirely system dependent, meaning you will need to perform some testing with your host application.
- Any metal closer than 20 mm will begin to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that you test the range with a mock-up (or actual prototype) of the product to assess effects of enclosure height (and materials, whether metal or plastic) and host PCB ground (GND plane size).

7.4 External Antenna Integration with BL54LM20 Series MHF4 variant (453-00585 or 453-00671)

Please refer to the regulatory sections for FCC, ISED, CE, MIC, UKCA and RCM requirements when using BL54LM20 Series modules with external antennas in each regulatory region.

The BL54LM20 Series has been designed to operate with the below external antennas (with a maximum gain of 2.32 dBi). The required antenna impedance is 50 ohms. See Table 4. External antennas improve radiation efficiency.

Table 4: External antennas for the BL54LM20 Series MHF4 variant modules (453-00585 and 453-00671)

Manufacturer	Model	Ezurio Part Number	Type	Connector	Peak Gain	
					2400-2500 MHz	2400-2480 MHz
Ezurio (Laird Connectivity)	NanoBlue	EBL2400A1-10MH4L	PCB Dipole	IPEX MHF4	2 dBi	-
Ezurio (Laird Connectivity)	FlexPIFA	001-0022	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	mFlexPIFA	EFA2400A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	iFlexPIFA Mini	EFG2401A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	Ezurio NFC	0600-00061	NFC	N/A	-	-
TE Connectivity	ANT-2.4-CW-RAH	-	Dipole	RP-SMA	1.6dBi	

8 Mechanical Details

8.1 BL54LM20 Series Mechanical Details

Mechanical dimensions, PCB footprints, land patterns, and antenna keep-out requirements are identical between the BL54LM20A and BL54LM20B module families. Unless otherwise noted, the information in this section applies to both module variants.

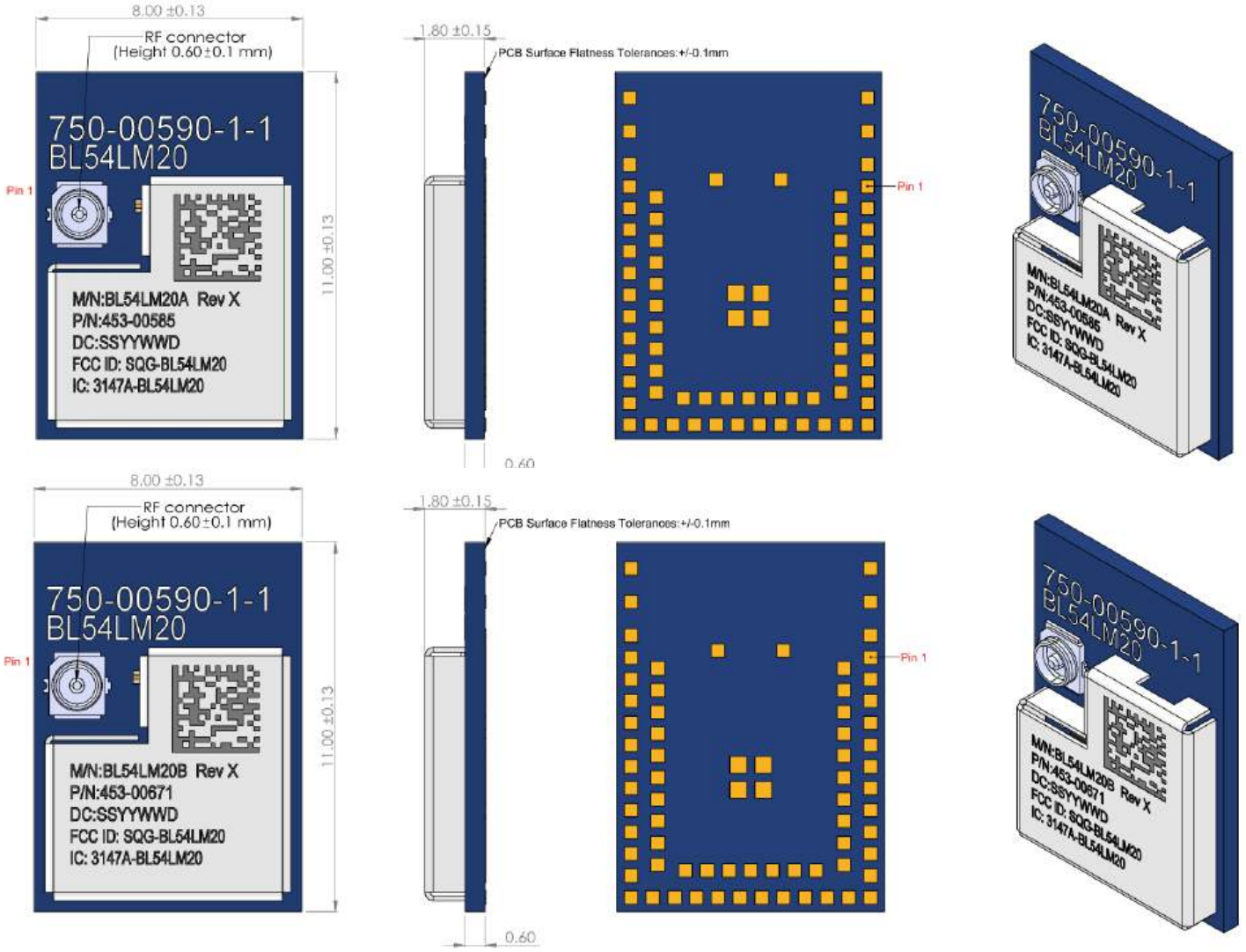


Figure 7 : Mechanical Details – MHF4 Antenna Variant Modules (453-00585 and 453-00671)

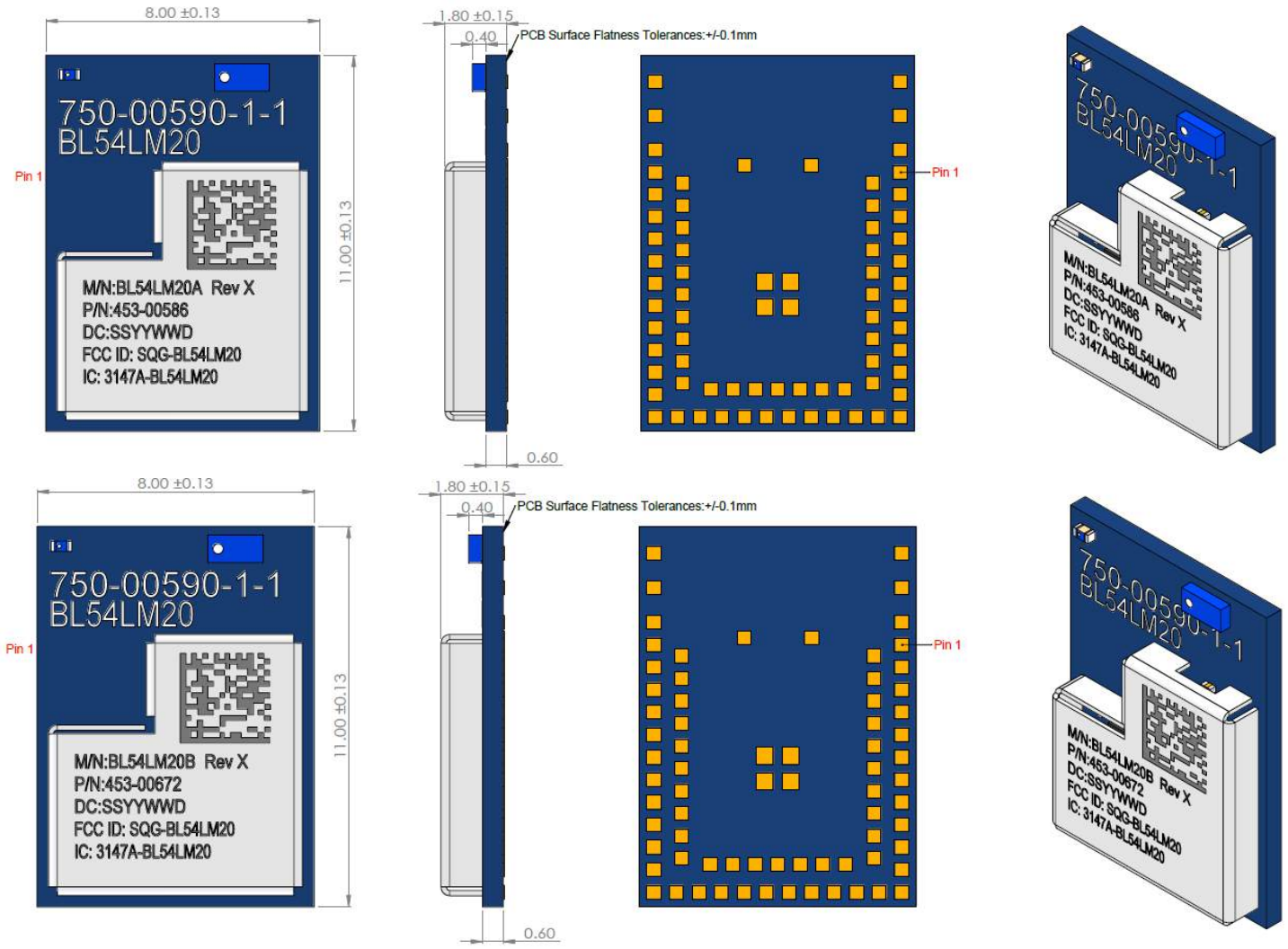


Figure 8 : Mechanical Details – Chip Antenna Variant Modules (453-00586 and 453-00672)

3D models of the BL54LM20 Series MHF4 Antenna Variant and chip antenna variant will be made available at:

BL54LM20A Series Support Page

BL54LM20B Series Support Page

8.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00586 and 453-00672

BL54LM20 Series PCB Footprint and BL54LM20 Series Schematic Symbol can be found on the BL54LM20 Series product pages –

BL54LM20A Series Support Page

BL54LM20B Series Support Page

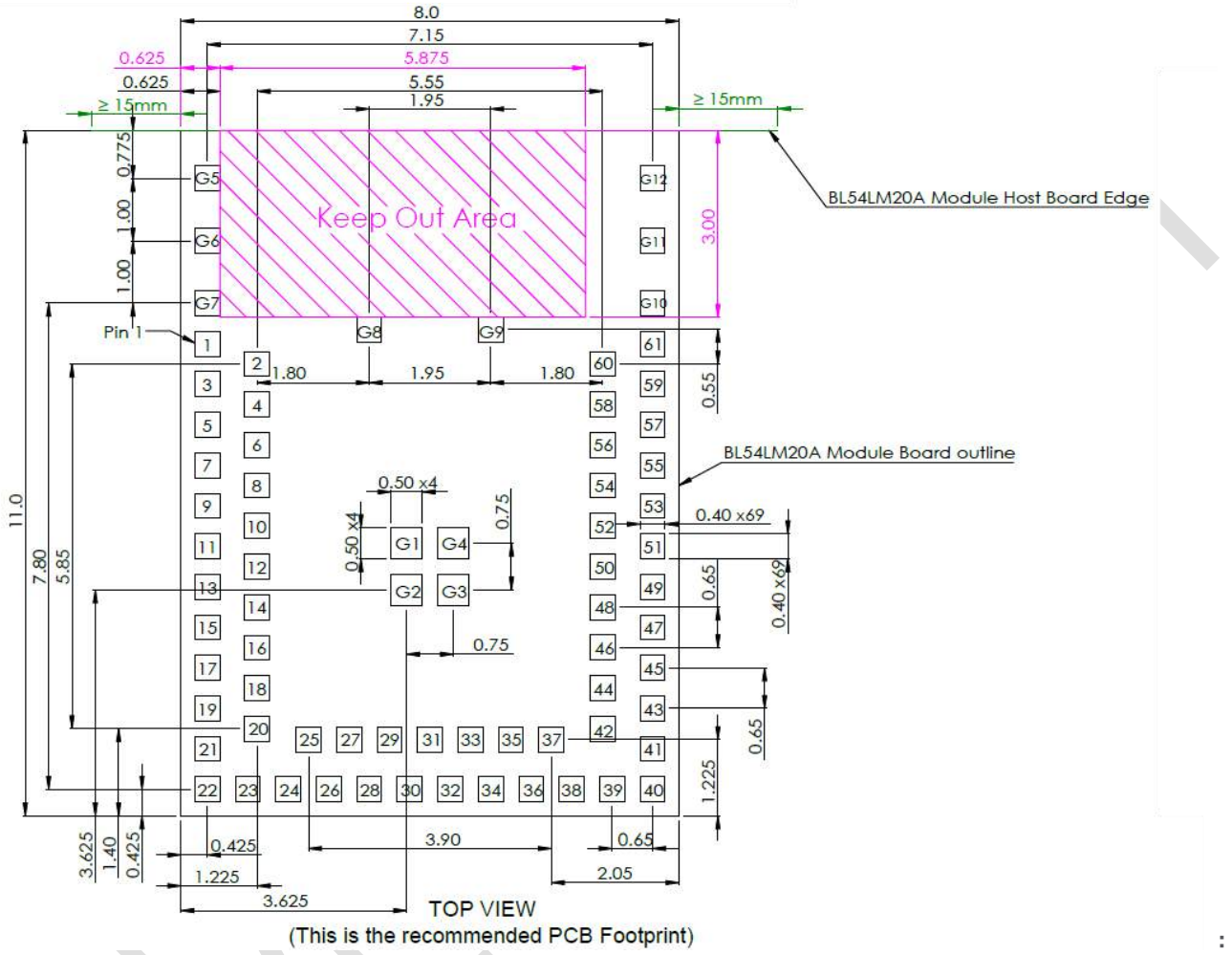


Figure 9 : Land Pattern and Antenna Keep-out for the 453-00586 and 453-00672

All dimensions are in mm.

Host PCB Land Pattern and Antenna Keep-out for the 453-00586 Notes:	
Note 1	Ensure there is no copper in the antenna 'keep out area' on any layers of the host PCB. Also keep all mounting hardware or any metal clear of the area (Refer to 7.3.2) to reduce effects of proximity detuning the antenna and to help antenna radiate properly.
Note 2	For the best on-board antenna performance, the module 453-00586 and 453-00672 MUST be placed on the edge of the host PCB, preferably near the edge centre and host PCB, the antenna "Keep Out Area" is extended (see Note 4).
Note 3	The BL54LM20B development board (453-00672-K1) places the 453-00672 module on the edge of the PCB (not in a corner) to provide the intended antenna keep-out environment.
Note 4	Ensure that the antenna keep-out area, including the area beneath the antenna section of the module, is completely free of copper, traces, planes, and vias on all layers of the host PCB.
Note 5	You may modify the PCB land pattern dimensions based on their experience and/or process capability.

9 On -Board PCB Chip Antenna Characteristics

9.1 Summary of Antenna Performance

Model	BL54LM20 Series-PCB_3D_Gain_FS_2402-2480MHz		
Test / Position	Gain /Free Space		
Frequency	**2402**	**2440**	**2480**
Ant. Port Input Pwr. (dB)	0	0	0
Tot. Rad. Pwr. (dB)	-5.23	-4.16	-4.69
Peak EIRP (dB)	**-2.43**	**-1.25**	**-2.00**
Directivity (dBi)	2.80	2.91	2.69
Efficiency (dB)	-5.23	-4.16	-4.69
Efficiency (%)	29.96	38.37	33.93
Gain (dBi)	-2.43	-1.25	-2.00
NHPRP ±Pi/4 (dB)	-6.58	-5.43	-5.95
NHPRP ±Pi/6 (dB)	-8.17	-6.95	-7.50

9.2 Antenna performance measurement setup

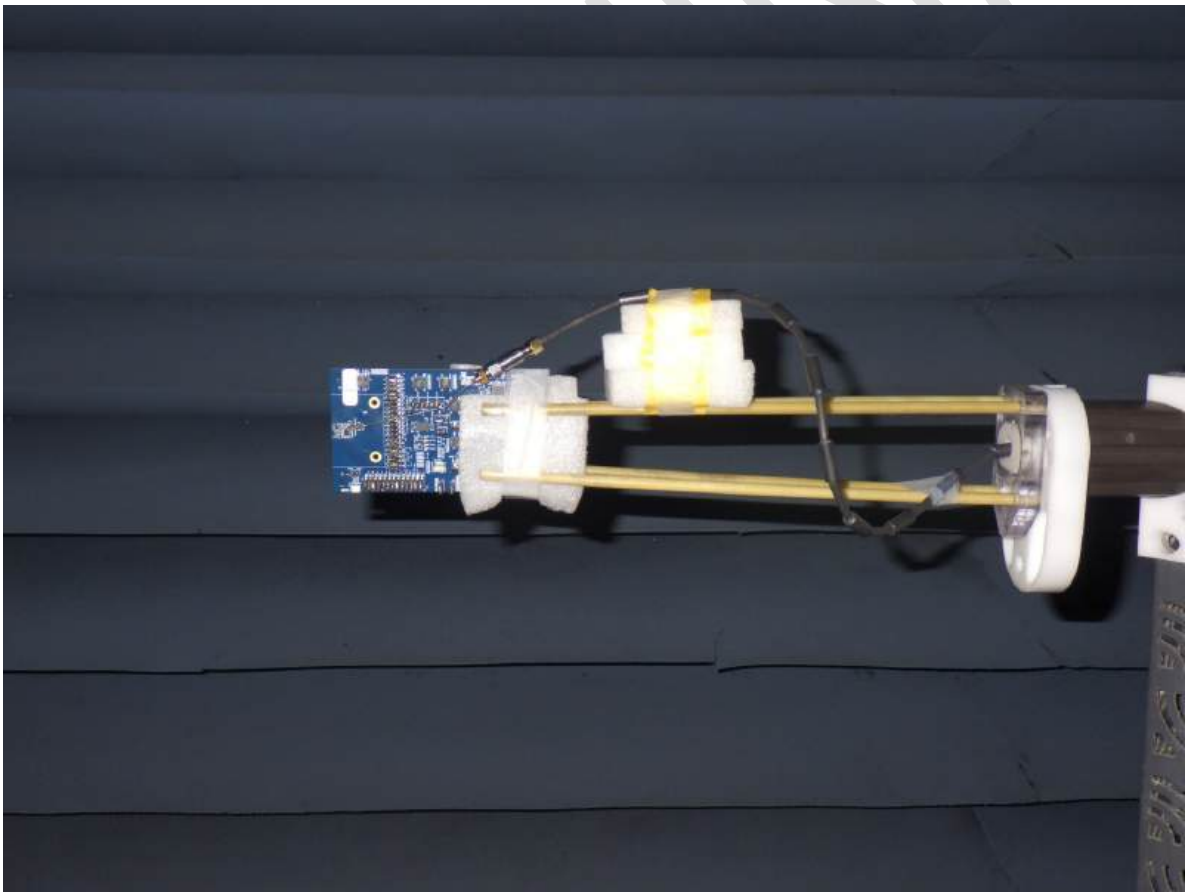
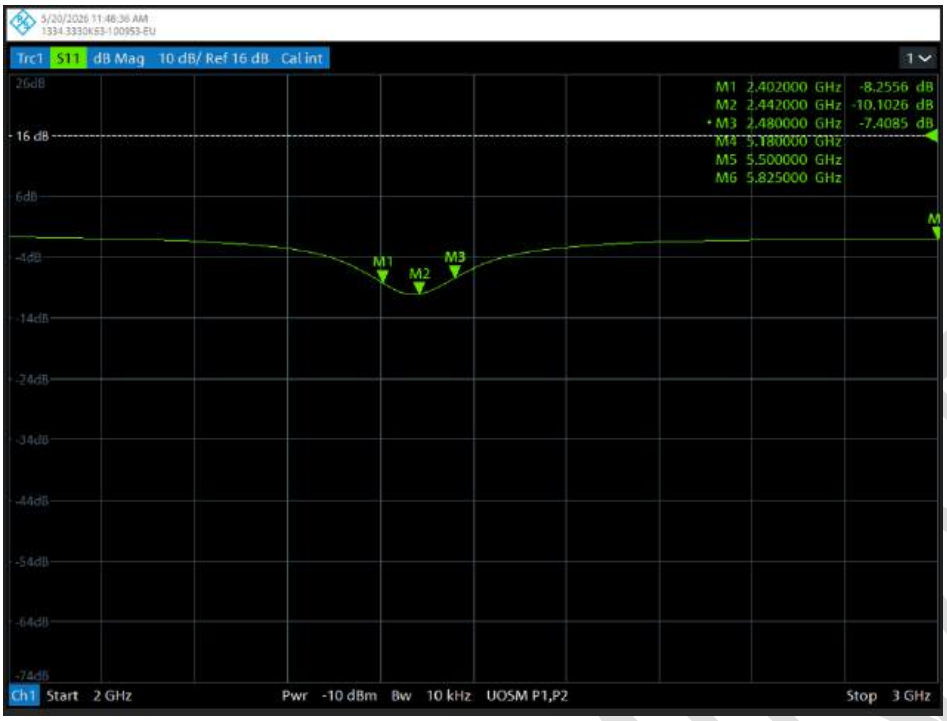


Figure 10: Antenna performance measurement setup

9.3 Antenna S11 measuring data



10 Application Note for Surface Mount Modules

10.1 Introduction

Ezurio's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of several commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

Part numbers – **453-00585R and 453-00586R** and **453-00671R and 453-00672R** are shipped as Tape / Reel, with a reel containing 2,500 pcs.

10.2 Module Packaging Configuration

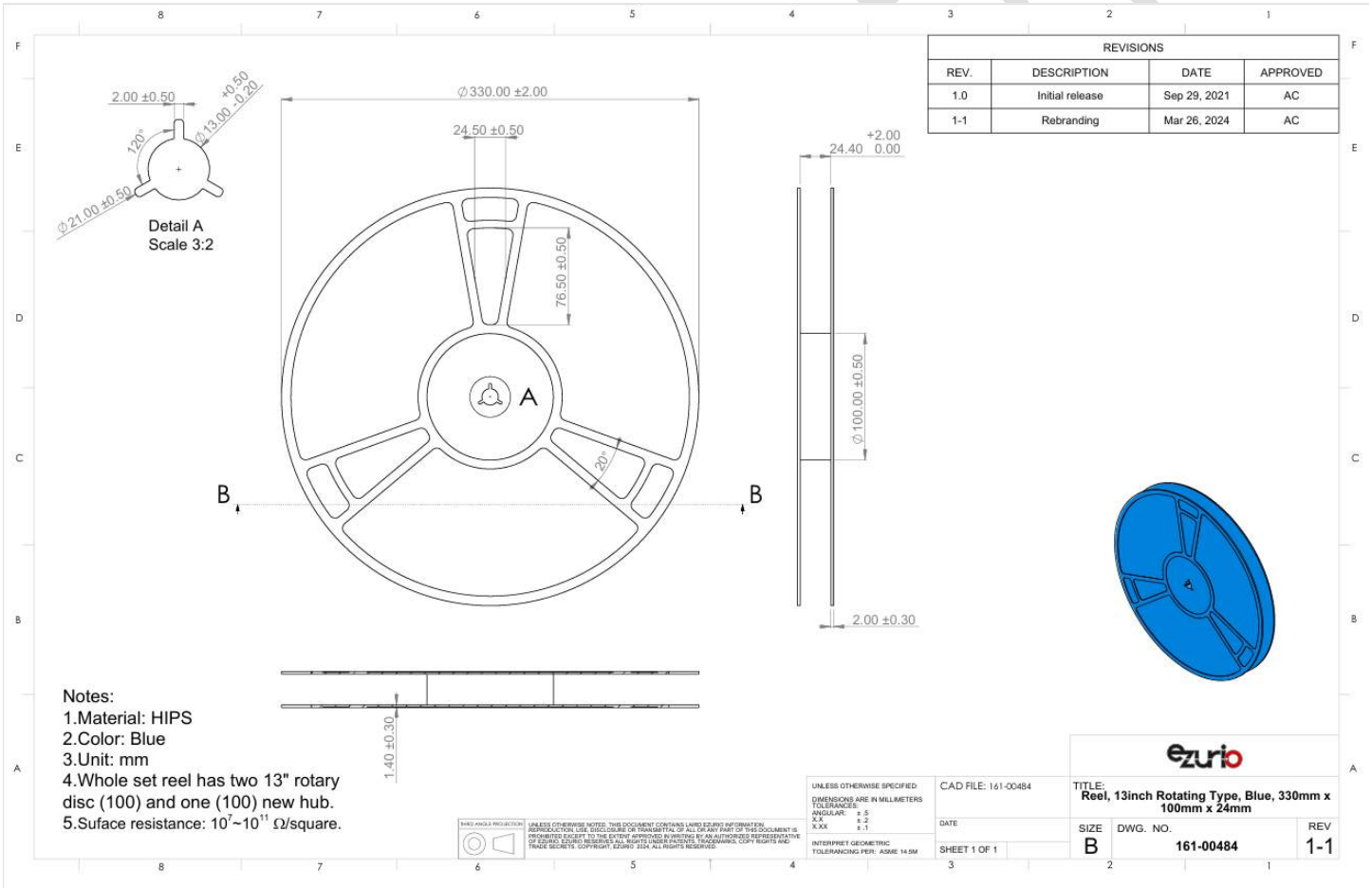


Figure 11: Reel specifications – 2,500 pieces per reel

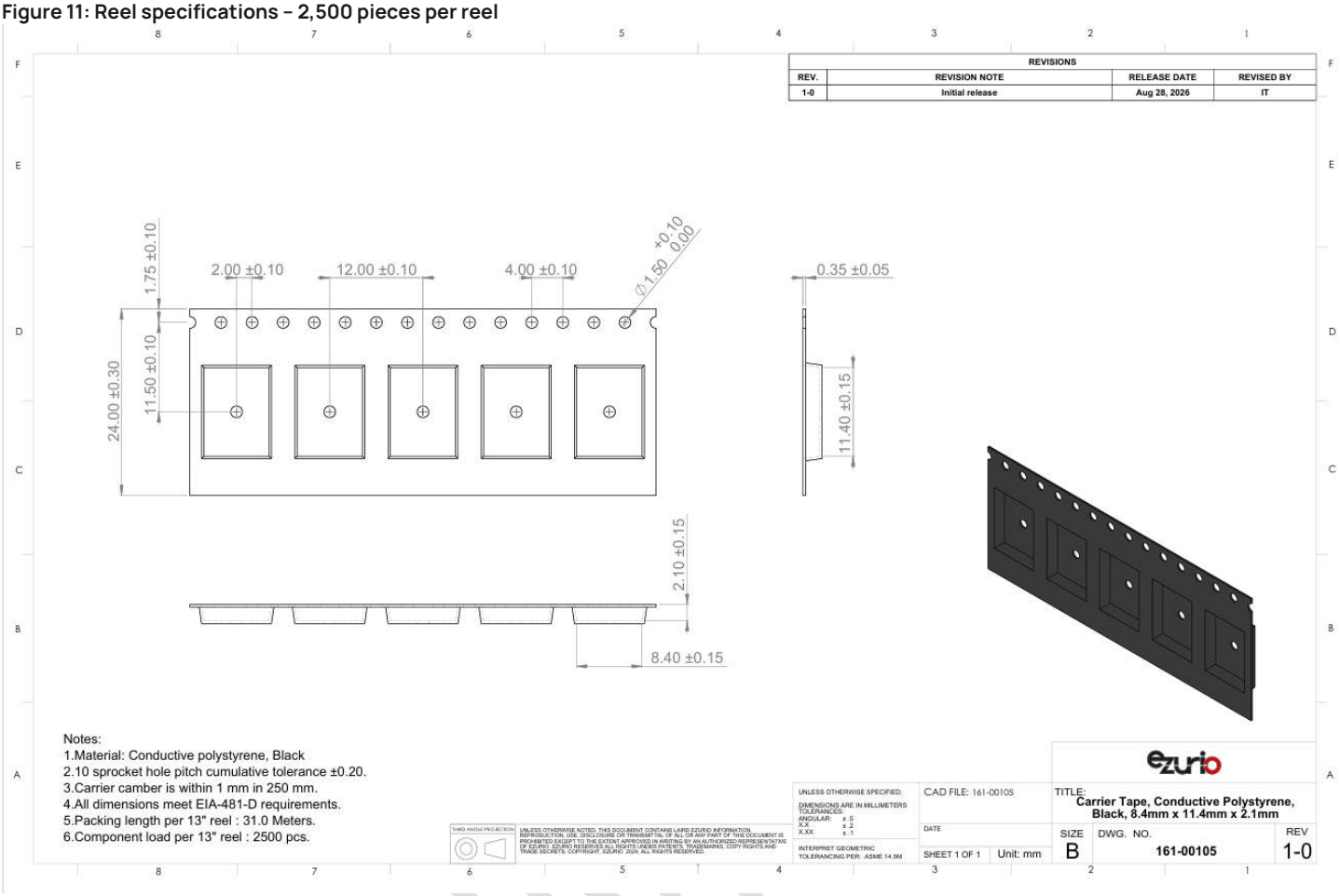


Figure 12: Carrier Tape specifications

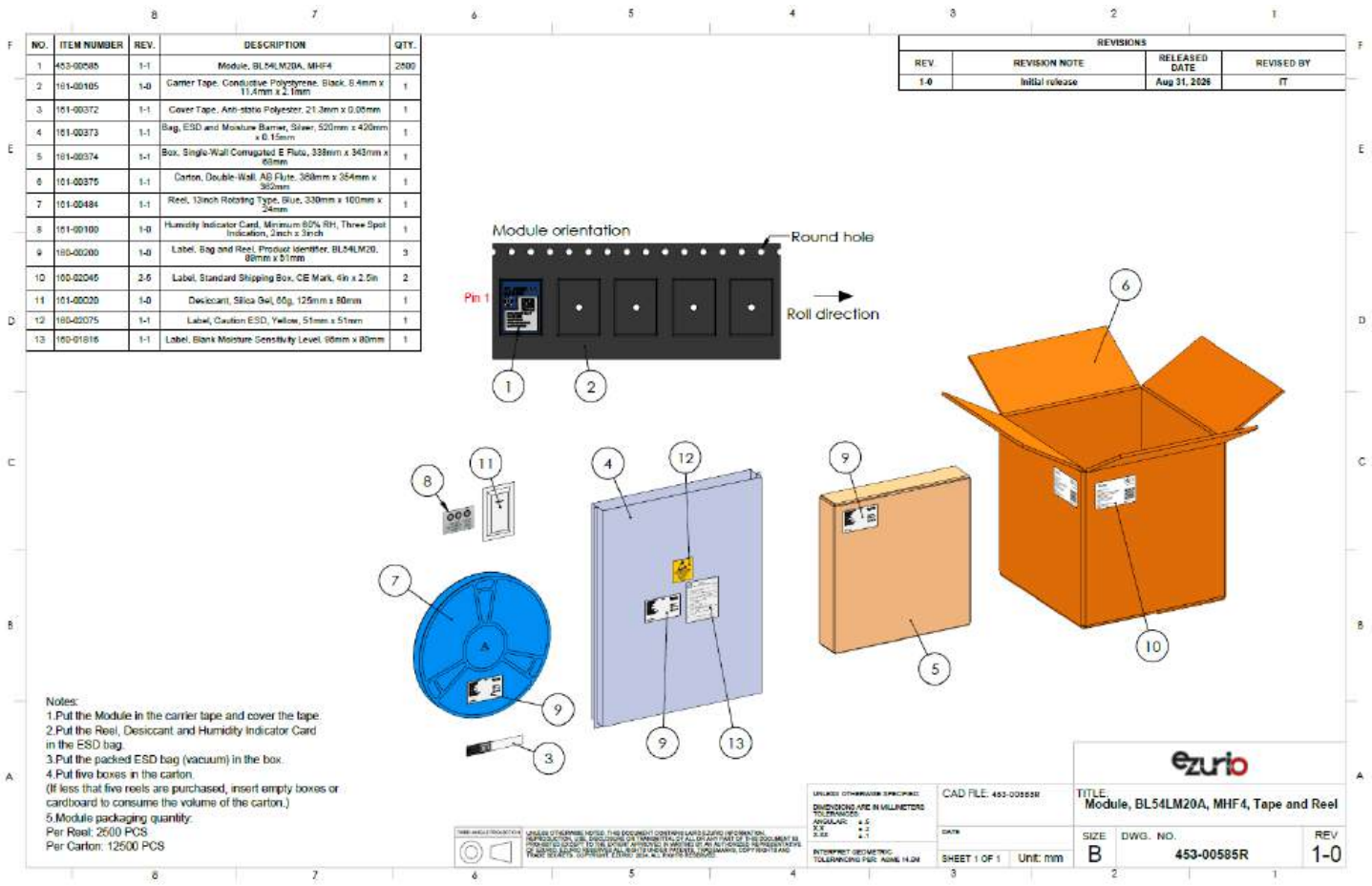
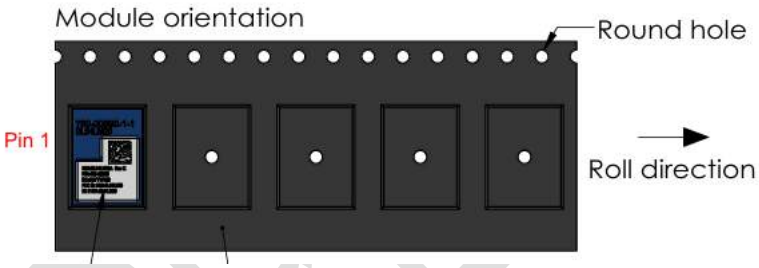


Figure 13: BL54LM20 Series Packaging Process



10.3 Module Shipping

All modules are shipped in tape and reel package and sealed in ESD Bags.

10.4 Labeling

The following labels are placed on the anti-static bag. The BL54LM20 modules are classified as MSL4 devices.

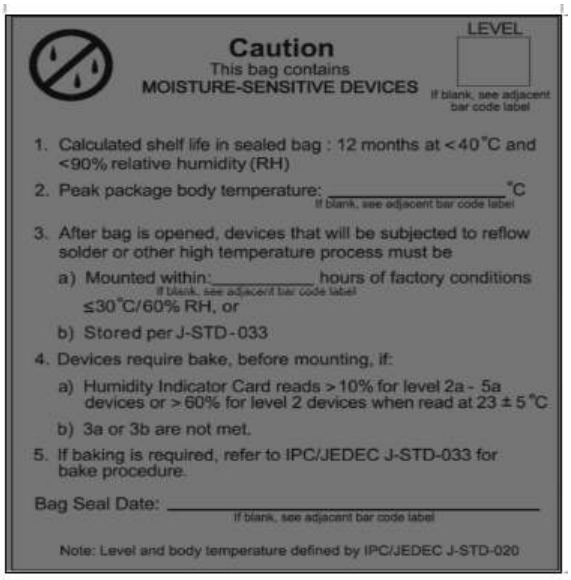


Figure 14: Moisture Sensitivity Level Label

Figure 15: Product Identifier Label

The following labels are placed on the pizza box.

Figure 16: Product Identifier Label

The following labels are placed on the master shipping carton.

Figure 17: Standard Shipping Carton Label

10.5 Required Storage Conditions

10.5.1 Prior to Opening the Dry Packing

The following are required storage conditions ***prior* to opening the dry packing**:

- Normal temperature: 5~40˚C
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

Note: Humidity means relative humidity.

10.5.2 After Opening the Dry Packing

The following are required storage conditions ***after* opening the dry packing** (to prevent moisture absorption):

- Storage conditions for one-time soldering:
  - Temperature: 5-25°C
  - Humidity: 60% or less
  - Period: 72 hours or less after opening
- Storage conditions for two-time soldering
  - Storage conditions following opening and prior to performing the 1st reflow:
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: A hours or less after opening
  - Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: B hours or less after completion of the 1st reflow

---

Note: Should keep A+B within 72 hours.

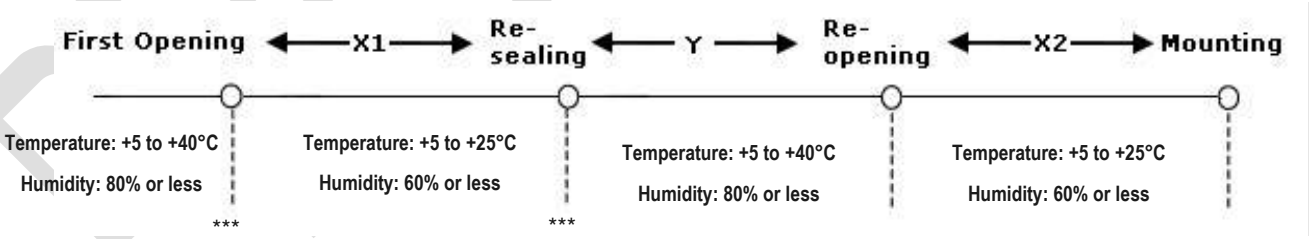
10.5.3 Temporary Storage Requirements after Opening

The following are temporary storage requirements after opening:

- Only re-store the devices *once* prior to soldering.
- Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using vacuumed heat-sealing.

The following indicate the required storage period, temperature, and humidity for this temporary storage:

- Storage temperature and humidity:



*** - External atmosphere temperature and humidity of the dry packing

- Storage period:
  - X1+X2 – Refer to After Opening the Dry Packing storage requirements. Keep is X1+X2 within 72 hours.
  - Y – Keep within two weeks or less.

10.6 Baking Conditions

Baking conditions and processes for the module follow the J-STD-033 standard which includes the following:

- The calculated shelf life in a sealed bag is 12 months at <40℃ and <80% relative humidity.
- Once the packaging is opened, the module must be mounted (per MSL4/Moisture Sensitivity Level 4) within 72 hours at <30 ˚C and <60% relative humidity.
- If the module is not mounted within 72 hours or if, when the dry pack is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125 ˚C (±5 ˚C).

10.7 Surface Mount Conditions

The following soldering conditions are recommended to ensure device quality.

10.7.1 Soldering

Note: When soldering, the stencil thickness should be ≥ 0.1 mm.

Convection reflow or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)

- Measuring point – IC package surface
- Temperature profile:

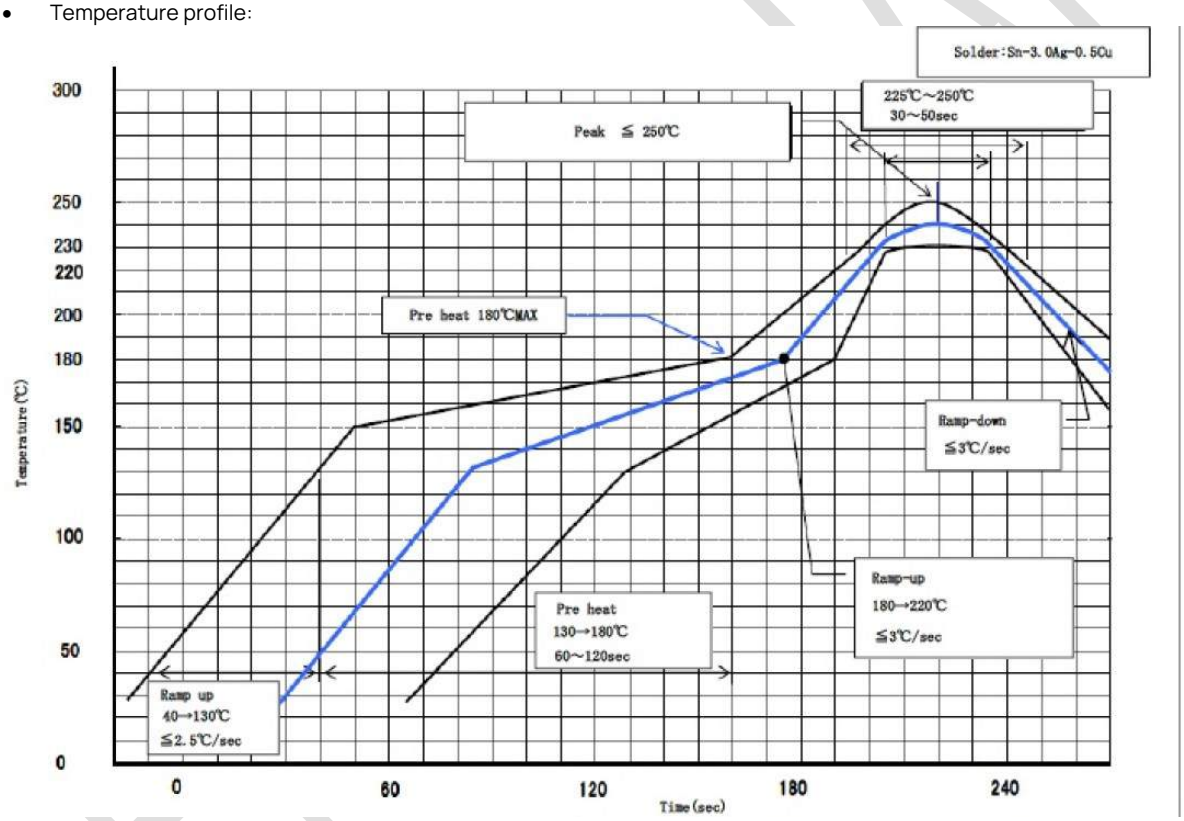


Figure 18: Temperature profile

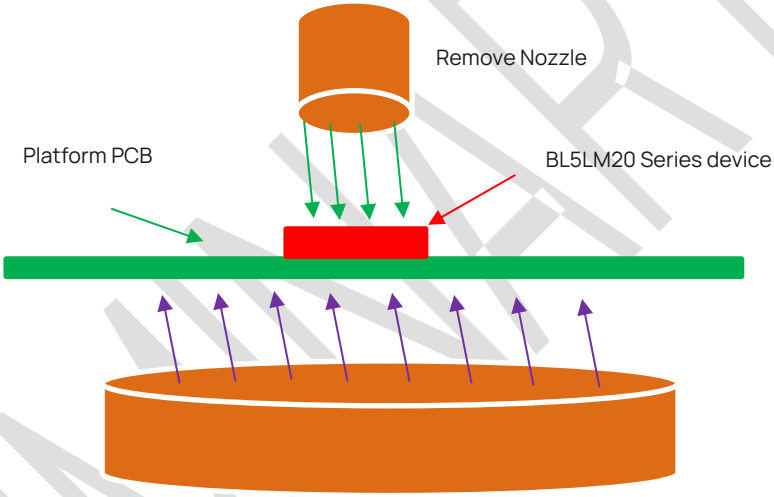
- Ramp-up: 40-130 ˚C. Less than 2.5 ˚C/sec
- Pre heat: 130-180 ˚C 60-120 sec, 180 ˚C MAX
- Ramp-up: 180-220 ˚C. Less than 3 ˚C/sec
- Peak Temperature: MAX 250 ˚C
  - 225 ˚C ~ 250 ˚C, 30 ~ 50 sec
- Ramp-down: Less than 3 ˚C/sec

10.7.2 Cautions When removing the BL54LM20 Series from the Platform for RMA

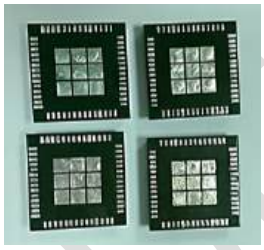
- Bake the platform before removing the BL54LM20 Series device from the platform. Reference baking conditions.
- Remove the BL54LM20Series device by using a hot air gun. This process should be carried out by a skilled technician.

Suggestion conditions:

- One-side component platform:
  - Set the hot plate at 280 °C.
  - Put the platform on the hot plate for 8~10 seconds.
  - Remove the SIP from platform.
- Two-side components platform:
  - Use two hot air guns
  - On the bottom side, use a pre-heated nozzle (temperature setting of 200~250 °C) at a suitable distance from the platform PCB.
  - On the top side, apply a remove nozzle (temperature setting of 330 °C). Heat the SIP until it can be removed from platform PCB.



- Remove the residue solder under the bottom side of module. (Note: Alternate module pictured as an example)



(Not accepted for RMA)

(Accepted for RMA analysis)

Example module with residue solder on the bottom ***Example Module, no residue solder***

- Remove and clean the residue flux as needed.

10.7.3 Precautions for Use

- Opening/handing/removing must be done on an anti-ESD treated workbench. All workers must also have undergone anti-ESD treatment.
- The devices should be mounted within one year of the date of delivery.
- The BL54LM20 Series modules are MSL 4 rated.

11 Reliability Test

11.1 Climatic And Dynamic Reliability Test

Table 5: Climatic and Dynamic Reliability Test Results for BL54LM20B Modules

Test Item	Specification	Standard	Test Result
Thermal Shock	Temperature: -40 ~ 85℃ Ramp time: Less than 10 seconds. Dwell Time: 10 minutes Number of Cycles: 350 times	*JESD22-A106 *IEC 60068-2-14 for dwell time and number of cycles	TBD
Vibration Non-Operating Unpackaged device	Vibration Wave Form: Sine Waveform Vibration frequency / Displacement: 20-80 Hz/1.5mm Vibration frequency / Acceleration: 80-2000 Hz/20g Cycle Time: 4 min/cycle Number of Cycles: 4 cycle/axis Vibration Axes: X, Y and Z (Rotate each axis on vertical vibration table)	JEDEC 22-B103B (2016)	TBD
Mechanical Shock Non-Operating Unpackaged device	Pulse shape: Half-sine waveform Impact acceleration: 1500 g Pulse duration: 0.5 ms Number of shocks: 30 shocks (5 shocks for each face) Orientation: Bottom, top, left, right, front, and rear faces	JEDEC 22-B110B.01 (2019)	TBD

11.2 Reliability MTBF Prediction

Table 6: MTBF Predictions for BL54LM20B Modules

Ezurio Part Number	Environment	Standard	Test Result 45 ℃ (Hours)
453-00585R 453-00585C 453-00671R 453-00671C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	TBD
453-00586R 453-00586C 453-00672R 453-00672C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	TBD
453-00585R 453-00585C 453-00671R 453-00671C	Mobile, Fixed, Uncontrolled	Telcordia Issue 4	TBD
453-00586R 453-00586C 453-00672R 453-00672C	Mobile, Fixed, Uncontrolled	Telcordia Issue 4	TBD
Ezurio Part Number	**Environment**	**Standard**	**Test Result 105 ℃ (Hours)**
453-00585R 453-00585C 453-00671R 453-00671C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	TBD
453-00586R 453-00586C 453-00672R 453-00672C	Ground, Fixed, Uncontrolled	Telcordia Issue 4	TBD
453-00585R 453-00585C 453-00671R 453-00671C	Mobile, Fixed, Uncontrolled	Telcordia Issue 4	TBD
453-00586R 453-00586C 453-00672R 453-00672C	Mobile, Fixed, Uncontrolled	Telcordia Issue 4	TBD

12 Regulatory

Full regulatory information on the BL54LM20 Series, including the Regulatory Information Guide, grants, and test reports are available on the product support pages:

BL54LM20A Series Support Page

BL54LM20B Series Support Page

The BL54LM20 Series holds current certifications in the following countries:

Table 7: BL54LM20 Series Certifications

Country/Region	Regulatory ID
USA (FCC)	TBD
EU (ETSI)	N/A (No ID Number Required)
UKCA	N/A (No ID Number Required)
Canada (ISED)	TBD
Japan (MIC)	TBD
Australia (RCM)	N/A
New Zealand (RCM)	N/A
Korea	TBD

12.1 Certified Antennas for the BL54LM20 Series

Table 8: Certified Antennas for BL54LM20 Series Modules

Model	MPN	Manufacturer	Type	Connector	Peak Gain (2400 – 2500 MHz)
NanoBlue	EBL2400A1-10MH4L	Ezurio	PCB Dipole	IPEX MHF4	2 dBi
FlexPIFA	001-0022	Ezurio	FlexPIFA	IPEX MHF4L	2 dBi
mFlexPIFA	EFA2400A3S-10MH4L	Ezurio	PIFA	IPEX MHF4L	2 dBi
I-FlexPIFATM Mini Series	EFG2401A3S-10MHF4L	Ezurio	I-FlexPIFA	IPEX MHF4L	2 dBi
Ezurio NFC	0600-00061	Ezurio	Coiled Inductor	FFC/FPC Connector	-
TE Connectivity	ANT-2.4-CW-RAH	-	Dipole	RP-SMA	1.6dBi

13 Bluetooth Qualification Process

13.1 Overview

The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:

To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

13.2 Scope

TBD

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference a single existing design, that has not been modified, (refer to Section 3.2.1 of the Qualification Program Reference Document v3).

This option applies to a Member qualifying a Product that includes an existing Design that has a DN, QDID, or DID and that Design has not been modified (e.g., rebranding a Qualified Product from another Member). The Design identified by the DN, QDID, or DID may only implement Bluetooth Specifications that are active or deprecated at the time of Submission. No modifications may be made to the Design, including changes to the ICS Form.

Changes to the Product outside the Design are allowed, including:

- Enabling technologies
- Changes to the industrial design
- Changes to the communication technology other than Bluetooth
- Changes to the features that are unrelated to Bluetooth, branding, packaging, colour, shape, Product name, or Model number

Members are responsible for assessing that modifications to the Product outside of the Design do not affect compliance with Bluetooth Specifications or result in a change to the ICS Form.

For the purposes of this document, it is assumed that the member is combining a single unmodified Core-Complete Configuration.

13.3 Qualification Steps When Referencing a single existing design, (unmodified) – Option 1 in the QPRDv3

For this qualification, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process**.
3. Product Details to be entered:
    - Project Name (this can be the product name or the Bluetooth Design name).
    - Product Description
    - Model Number
    - Product Publication Date (the product publication date may not be later than 90 days after submission)

- Product Website (optional)
- Internal Visibility (this will define if the product will be visible to other users prior to publication)
- If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.

4. Specify the Design:
   - Do you include any existing Design(s) in your Product? Answer Yes, I do.
   - Enter the single DN or QDID used in your, (for Option 1 only one DN or QDID can be referenced)
   - Once the DN or QDID is selected it will appear on the left-hand side, indicating the layers covered by the design.
   - Select 'I'm finished entering DN's
   - What do you want to do next? Answer, 'Use this Design without Modification'
   - Save and go to Product Qualification Fee
5. Product Qualification Fee:
   - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
   - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
   - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
   - Once you have selected the Prepaid Qualifi[illegible] 'Sav[illegible] to Submission'
6. Submission:
   - Some automatic checks occur to ensure all su[illegible]missio[illegible] requ[illegible]em[illegible]nts ar[illegible]complete.
   - To complete the listing any errors must be co[illegible]rected
   - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
   - Now select 'Complete the Submission'.
   - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
   - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
7. Download Product and Design Details:
   a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

13.4 Example Designs for reference

The following gives an example of a design possible under option 1:

Ezurio End Product design using Nordic Component based design

Design Name	Owner	Design ID	Link to listing on the SIG website
BL54LM20A	Ezurio	TBD	https://qualification.bluetooth.com/ListingDetails/274104

13.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select 'Manage Submitted Products' in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

14 Ordering Information

Part Number	Product Description
453-00586R	Module, BL54LM20A, (Nordic nRF54LM20A), Chip Antenna, Tape/Reel
453-00585R	Module, BL54LM20A, (Nordic nRF54LM20A), MHF4 Connector, Tape/Reel
453-00672R	Module, BL54LM20B, (Nordic nRF54LM20B), Chip Antenna, Tape/Reel
453-00671R	Module, BL54LM20B, (Nordic nRF54LM20B), MHF4 Connector, Tape/Reel
453-00586C	Module, BL54LM20A, (Nordic nRF54LM20A), Chip Antenna, Cut Tape
453-00585C	Module, BL54LM20A, (Nordic nRF54LM20A), MHF4 Connector, Cut Tape
453-00672C	Module, BL54LM20B, (Nordic nRF54LM20B), Chip Antenna, Cut Tape
453-00671C	Module, BL54LM20B, (Nordic nRF54LM20B), MHF4 Connector, Cut Tape
453-00672-K1	Development kit, Module, BL54LM20B, (Nordic nRF54LM20B), Chip Antenna
453-00671-K1	Development kit, Module, BL54LM20B, (Nordic nRF54LM20B), MHF4 Connector

15 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 388 S. Main St. Suite 330 Akron, OH 44311 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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