XD9704/XD9705 Series

ETR05099-001a

Qualified for automotive 36V & 600mA Synchronous Step-Down DC/DC Converters

☆AEC-Q100 Grade1

■GENERAL DESCRIPTION

The XD9704/XD9705 series are 36V operation synchronous step-down DC/DC converter ICs with a built-in High side driver FET and Low side driver FET. The XD9704/XD9705 series has an operating voltage range of 3.0V to 36.0V, a switching frequency of 2.2MHz, and by utilizing synchronous rectification, delivers stable voltage with high efficiency.

The output voltage can be changed from 2.8V to 20.0V(XD9704), 2.8V to 15.0V(XD9705) using an external resistor, so the same part number can be used for multiple power lines.

By connecting a resistor and capacitor to the EN/SS pin, the soft-start time can be externally adjusted to be longer than the internal soft-start. The power good function also monitors the state of the output voltage. This soft-start external adjustment and power good functions make it easy to configure the power supply sequence.

Over-current protection and thermal shutdown are built in as protection function, and it can be used safely.

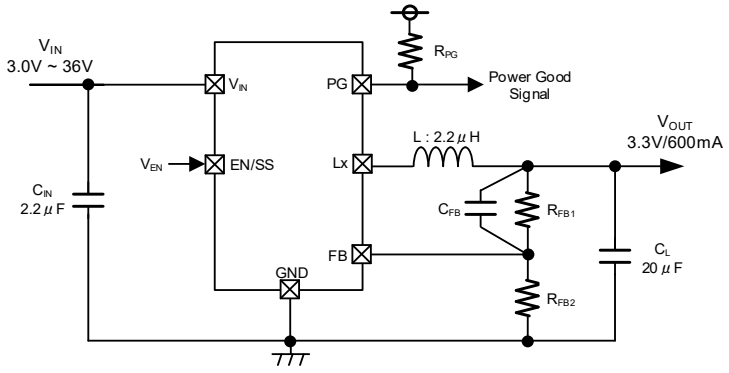
■APPLICATIONS

- ●Automotive Body Control
- ●Automotive Infotainment
- ●Automotive accessories
  - ・Drive recorder
  - ・Car-mounted camera
  - ・ETC
- ●Industrial Equipment

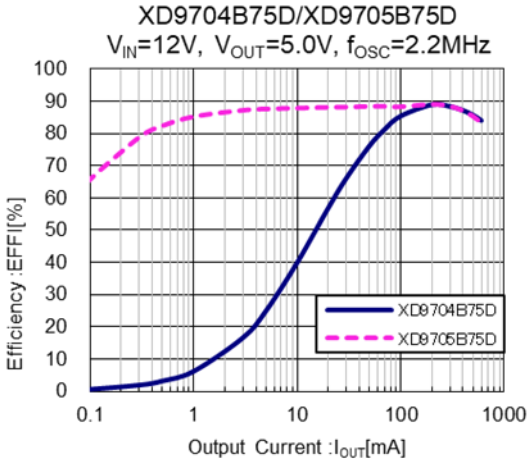
■FEATURES

Input Voltage Range	:	3.0V ~ 36.0V (Absolute Max 40.0V)
Surge Voltage	:	46.0V (Applied Time≦400ms)
Output Voltage Range	:	2.8V ~ 20.0V (XD9704) 2.8V ~ 15.0V (XD9705)
FB Voltage	:	0.75V±1.5%
Maximum Output Current	:	600mA
Oscillation Frequency	:	2.2MHz
Quiescent Current	:	11μA (XD9705)
Control Methods	:	F-PWM Control (XD9704) PWM/PFM Control (XD9705)
Efficiency	:	88%@12V→5V, 300mA
Protection functions	:	Current Limit (Automatic Recovery) Thermal Shutdown
Functions	:	Soft-Start (external adjustment) Power Good (DFN1820-6J only), UVLO
Output Capacitor	:	Ceramic Capacitor
Operating Junction Temperature	:	-40℃ ~ 150℃
Packages	:	SOT-89-5 (4.5 x 4.6 x 1.6mm) (Without Power Good) DFN1820-6J (1.8 x 2.0 x 0.6mm) (With Power Good)
Environmentally Friendly		EU RoHS Compliant, Pb Free

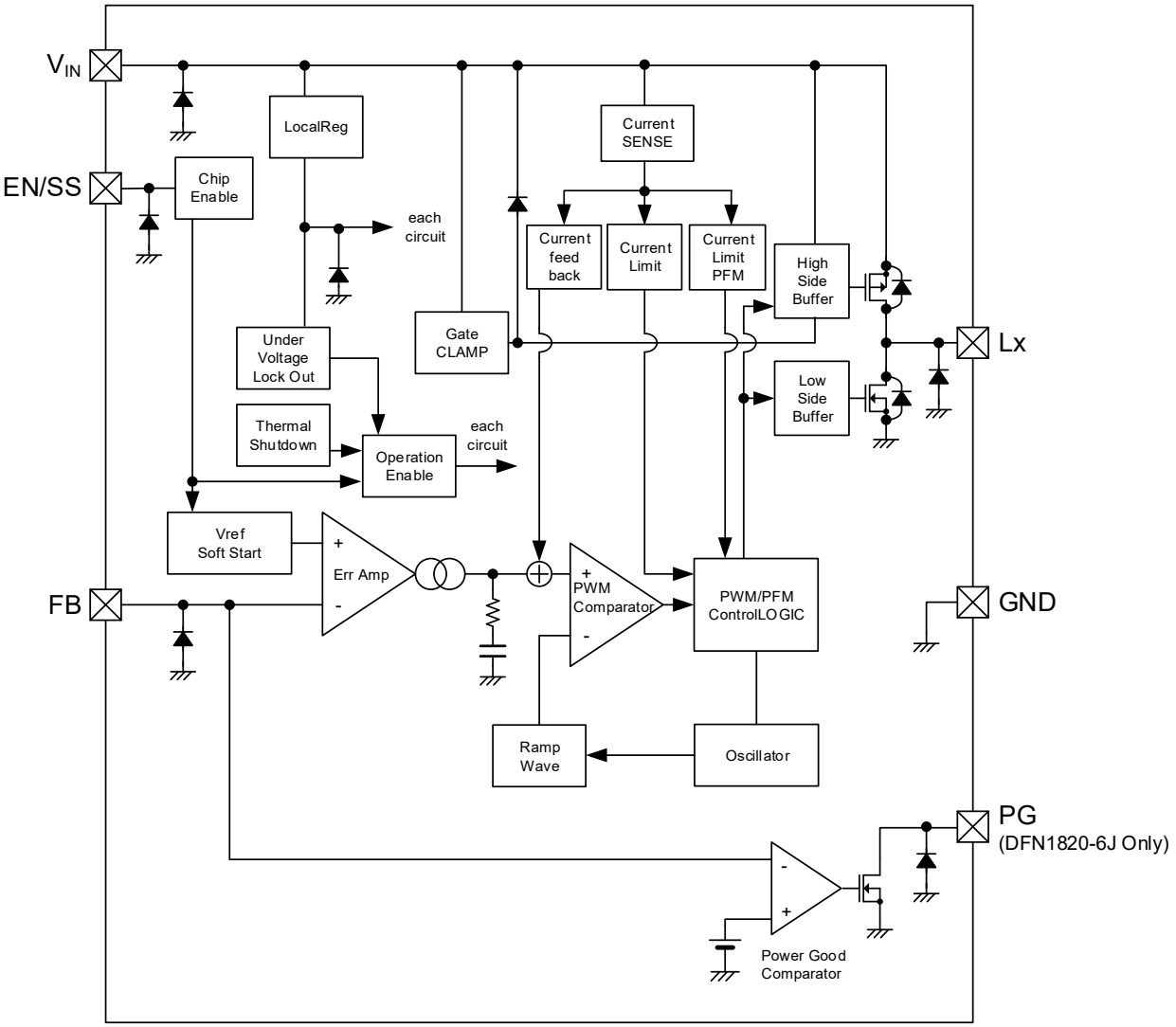
■TYPICAL APPLICATION CIRCUIT



■TYPICAL PERFORMANCE CHARACTERISTICS



■BLOCK DIAGRAM



* Diodes inside the circuit are ESD protection diodes and parasitic diodes.

■PRODUCT CLASSIFICATION

●Ordering Information

XD9704①②③④⑤⑥-⑦(*1) : F-PWM Control

XD9705①②③④⑤⑥-⑦(*1) : PWM/PFM Control

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	B	-
②③	FB Voltage	75	0.75V
④	Oscillation Frequency	D	2.2MHz
⑤⑥-⑦	Packages	PR-Q(*1)	SOT-89-5 (1,000pcs/Reel) (*2)
		8R-Q(*1)	DFN1820-6J (3,000pcs/Reel) (*2) * Under development

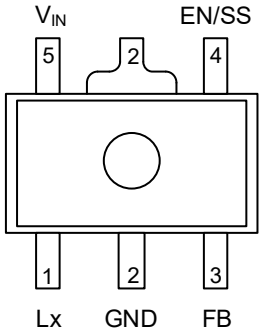
(*1) The “-Q” suffix denotes “AEC-Q100” compliant.

(*2) “Halogen and Antimony free” as well as being fully EU RoHS compliant.

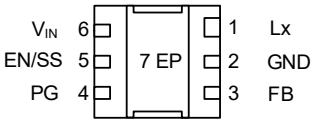
●Selection Guide

FUNCTION	SOT-89-5	DFN1820-6J
Enable	Yes	Yes
UVLO	Yes	Yes
Thermal Shutdown	Yes	Yes
Soft Start	Yes	Yes
Power-Good	-	Yes
Current Limiter (Automatic Recovery)	Yes	Yes

■PIN CONFIGURATION



SOT-89-5
(TOP VIEW)



DFN1820-6J
(BOTTOM VIEW)

* Under development

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-89-5	DFN1820-6J		
1	1	Lx	Switching Output
2	2	GND	Ground
3	3	FB	Output Voltage Sense
-	4	PG	Power-good Output
4	5	EN/SS	Enable, Soft-start
5	6	V_{IN}	Power Input
-	7	EP	Exposed thermal pad. The Exposed pad is recommended to be connected to GND (Pin2)

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN/SS	H	Active
	L	Stand-by
	OPEN	Stand-by

PIN NAME	CONDITION		SIGNAL
PG	EN/SS = H	$V_{FB} > V_{PGDET}$	H (High impedance)
		$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
		Thermal Shutdown	L (Low impedance)
		UVLO ($V_{IN} < V_{UVLOD}$)	Undefined State
	EN/SS = L	Stand-by	L (Low impedance)

■ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
V_{IN} Pin Voltage		V_{IN}	-0.3 ~ 40.0	V
EN/SS Pin Voltage		$V_{EN/SS}$	-0.3 ~ 40.0	V
FB Pin Voltage		V_{FB}	-0.3 ~ 6.2	V
Lx Pin Voltage		V_{Lx}	-0.3 ~ V_{IN} + 0.3 or 40.0 (*1)	V
PG Pin Voltage (*4)		V_{PG}	-0.3 ~ 6.2	V
PG Pin Current (*4)		I_{PG}	8	mA
Power Dissipation (Ta=25℃)	SOT-89-5	Pd	2150 (JESD51-7 Board) (*2)	mW
	DFN1820-6J		2160 (JESD51-7 Board) (*2)	mW
V_{IN} Pin Surge Voltage		V_{IN_SURGE}	46.0 (*3)	V
EN/SS Pin Surge Voltage		V_{EN/SS_SURGE}	46.0 (*3)	V
Junction Temperature		Tj	-40 ~ 150	℃
Storage Temperature		Tstg	-55 ~ 150	℃

All voltages are described based on the GND pin.

(*1) The maximum value should be either V_{IN}+0.3V or 40.0V, whichever is lower

(*2) The power dissipation figure shown is PCB mounted and is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

(*3) Applied Time≦400ms

(*4) For the DFN1820-6J only.

■RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Setting Output Voltage Range	XD9704	V_{OUTSET}	2.8	-	20.0	V
	XD9705				15.0	
Input Voltage		V_{IN}	3.0	-	36.0	V
Output Current		I_{OUT}	0.0	-	600	mA
EN/SS Pin Voltage		$V_{EN/SS}$	0.0	-	36.0	V
PG Pull-up Voltage		V_{PG}	0.0	-	5.5	V
PG Pull-up Resistor		R_{PG}	5	100	-	kΩ
Operating Ambient Temperature		Topr	-40	-	125	℃
Input Capacitor (Effective Value) (*1)		C_{IN}	0.5	-	1000 (*2)	μF
Output Capacitor (Effective Value) (*1)	$V_{OUTSET} \leqq 3.3V$	C_L	13.2	-	1000 (*3)	μF
	$3.3V < V_{OUTSET} \leqq 6V$		10.4			
	$6V < V_{OUTSET}$		12.0			
Inductor	$V_{OUTSET} \leqq 3.3V$	L	2.2 x 0.7	2.2	2.2 x 1.3	μH
	$3.3V < V_{OUTSET} \leqq 6V$		3.3 x 0.7	3.3	3.3 x 1.3	
	$6V < V_{OUTSET}$		4.7 x 0.7	4.7	4.7 x 1.3	

All voltages are described based on the GND pin.

(*1) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(*2) If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance(C_{IN}), place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase and the IC may malfunction.

(*3) If a large-capacity capacitor is used as output capacitor(C_L), the output stability may be reduced, and the ripple voltage may increase. Even if a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor is used as output capacitor(C_L), place a low-ESR ceramic capacitor in parallel. Even if the capacitance is within the recommended range, the output stability may be reduced depending on the type and ESR etc. of the capacitor used, so please thoroughly test it on the actual equipment before use.

■ELECTRICAL CHARACTERISTICS

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
Operating Input Voltage Range	V_{IN}	-		3.0	-	36.0	V	-
Setting Output Voltage Range	V_{OUTSET}	-	XD9704	2.8	-	20.0	V	-
			XD9705	2.8	-	15.0		
FB Voltage	V_{FB}	V_{FB}=0.739V→0.761V, V_{FB} Voltage when Lx pin voltage changes from "H" to "L"		0.739	0.750	0.761	V	②
			-40≦Ta≦125℃	0.728	-	0.773		
Over Voltage Protection	V_{OVP}	-		-	0.81	-	V	-
UVLO Detect Voltage	V_{UVLOD}	$V_{EN/SS}$=12V, V_{IN}:2.80V→2.60V, V_{FB}=0V V_{IN} Voltage when Lx pin changes from “H” to "L"		2.60	2.70	2.80	V	②
			-40≦Ta≦125℃	2.50	-	2.87		
UVLO Release Voltage	V_{UVLOR}	$V_{EN/SS}$=12V, V_{IN}:2.70V→2.90V, V_{FB}=0V V_{IN} Voltage when Lx pin changes from “L” to "H"		2.70	2.80	2.90	V	②
			-40≦Ta≦125℃	2.60	-	2.97		
Quiescent Current	I_q	V_{FB}=0.765V	XD9704	-	320	640	μA	④
			-40≦Ta≦125℃	-	-	700		
			XD9705	-	11	19		
			-40≦Ta≦125℃	-	-	28		
Stand-by Current	I_{STB}	V_{IN}=12V, $V_{EN/SS}$=0V		-	0.6	1.2	μA	④
			-40≦Ta≦125℃	-	-	1.5		
Oscillation Frequency	f_{OSC}	Connected to external components		2.013	2.200	2.387	MHz	①
			-40≦Ta≦125℃	1.900	-	2.650		
Minimum Duty Cycle	D_{MIN}	V_{FB}=0.825V	-40≦Ta≦125℃	-	-	0	%	②
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.675V	-40≦Ta≦125℃	100	-	-	%	②
Lx SW "H" On Resistance	R_{LxH}	V_{FB}=0.6V, I_{Lx}=200mA		-	1.20	1.38	Ω	⑤
Lx SW "L" On Resistance	R_{LxL}	I_{Lx}=200mA		-	0.60	0.70	Ω	−
High side Current Limit	I_{LIMH}	V_{OUT}=V_{OUTSET}×0.98		1.1	1.4	-	A	−
Internal Soft-Start Time	t_{SS1}	V_{FB}=0.71V		1.0	2.2	4.5	ms	②
External Soft-Start Time	t_{SS2}	V_{FB}=0.71V, R_{SS}=430kΩ, C_{SS}=0.47μF		14	21	32	ms	③

Test Condition : Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V

■ELECTRICAL CHARACTERISTICS

Ta=25℃

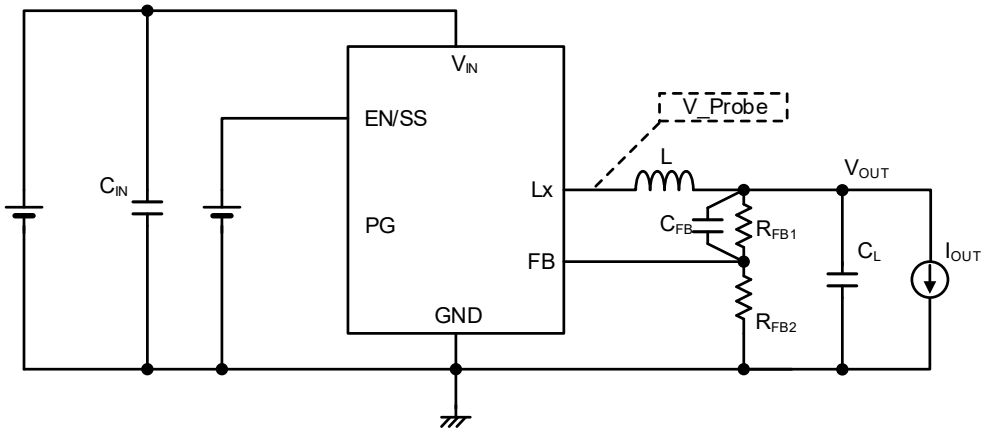
PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
PG Detect Voltage (*1)	V_{PGDET}	V_{FB}=0.72V→0.63V, R_{PG}:100kΩ pull-up to 5V V_{FB} Voltage when PG pin voltage changes from "H" to "L"		0.638	0.675	0.712	V	⑤
			-40≦Ta≦125℃	0.63	-	0.72		
PG Output Voltage (*1)	V_{PG}	V_{FB}=0.6V, I_{PG}=1mA	-40≦Ta≦125℃	-	-	0.3	V	②
PFM Switch Current (XD9705)	I_{PFM}	Connected to external components, I_{OUT}=0mA		-	450	-	mA	①
FB Voltage Temperature Characteristics	$\Delta V_{FB}/(\Delta T_{opr} \cdot V_{FBE})$	-40℃≦T_{opr}≦125℃		-	±100	-	ppm/℃	②
FB "H" Current	I_{FBH}	V_{IN}=$V_{EN/SS}$=36V, V_{FB}=3.0V	-40≦Ta≦125℃	-	0.0	0.1	μA	④
FB "L" Current	I_{FBL}	V_{IN}=$V_{EN/SS}$=36V, V_{FB}=0V	-40≦Ta≦125℃	-	0.0	0.1	μA	④
EN/SS "H" Voltage	V_{ENSSH}	$V_{EN/SS}$=0.3V→2.5V, V_{FB}=0.71V $V_{EN/SS}$ Voltage when Lx pin voltage changes from "L" to "H"		2.5	-	36.0	V	④
			-40≦Ta≦125℃					
EN/SS "L" Voltage	V_{ENSSL}	$V_{EN/SS}$=2.5V→0.3V, V_{FB}=0.71V $V_{EN/SS}$ Voltage when Lx pin voltage changes from "H" to "L"		GND	-	0.3	V	④
			-40≦Ta≦125℃					
EN/SS "H" Current	I_{ENSSH}	V_{IN}=$V_{EN/SS}$=36V, V_{FB}=0.825V	-40≦Ta≦125℃	-	0.1	0.3	μA	④
EN/SS "L" Current	I_{ENSSL}	V_{IN}=36V, $V_{EN/SS}$=0V, V_{FB}=0.825V	-40≦Ta≦125℃	-	0.0	0.1	μA	④
Thermal Shutdown Temperature	T_{TSD}	Junction Temperature		-	160	-	℃	-
Hysteresis Width	T_{HYS}	Junction Temperature		-	25	-	℃	-

Test Condition : Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V

(*1) For the DFN1820-6J only.

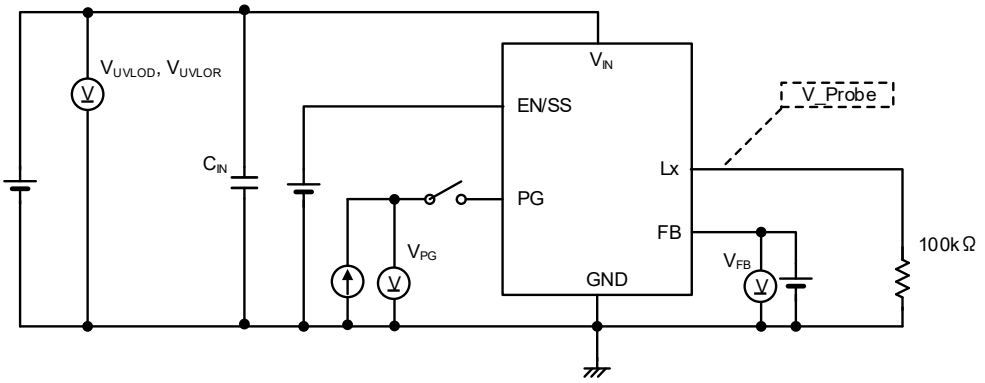
■TEST CIRCUITS

CIRCUIT①

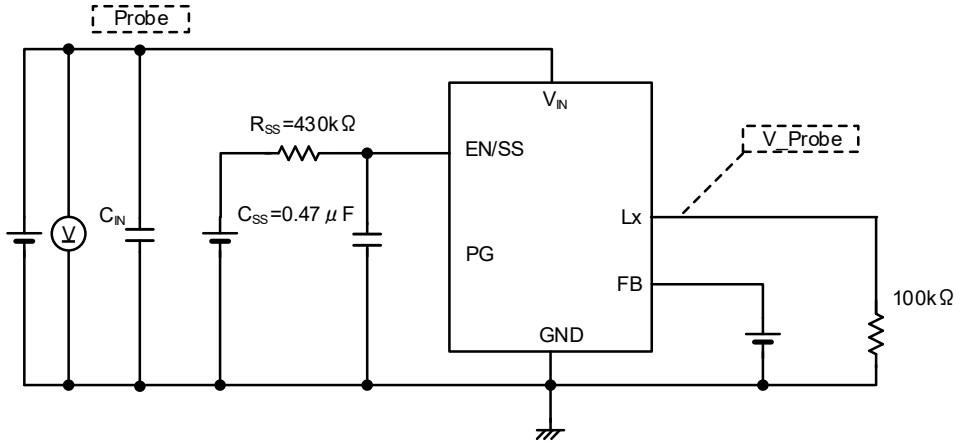


f_{osc}=2.2MHz: L=3.3μH, R_{FB1}=680kΩ, R_{FB2}=120kΩ, C_{FB}=12pF, C_L=10μF×2parallel, C_{IN}=2.2μF

CIRCUIT②

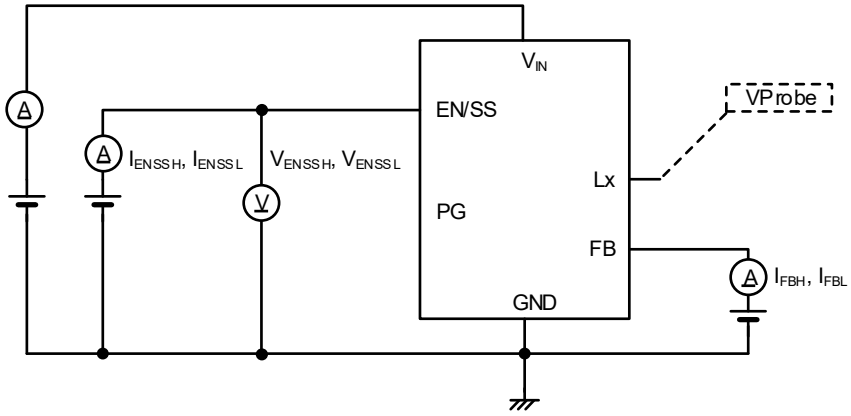


CIRCUIT③

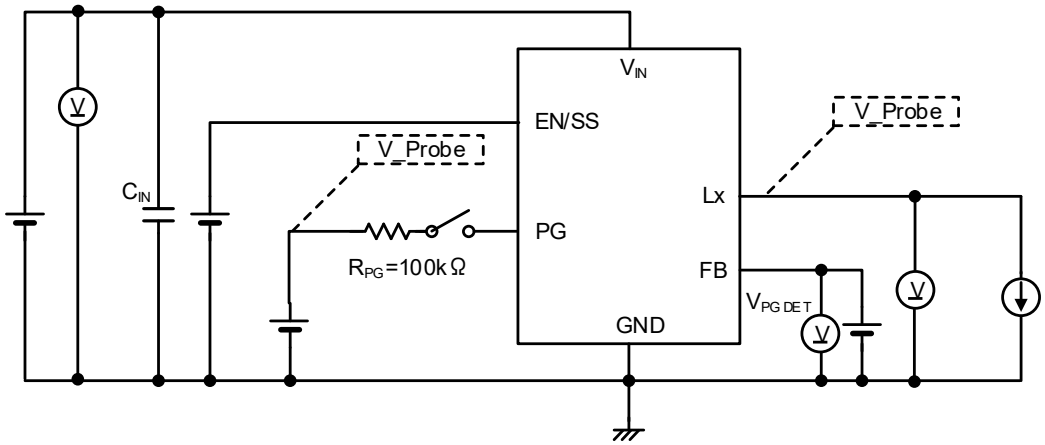


■TEST CIRCUITS

CIRCUIT④

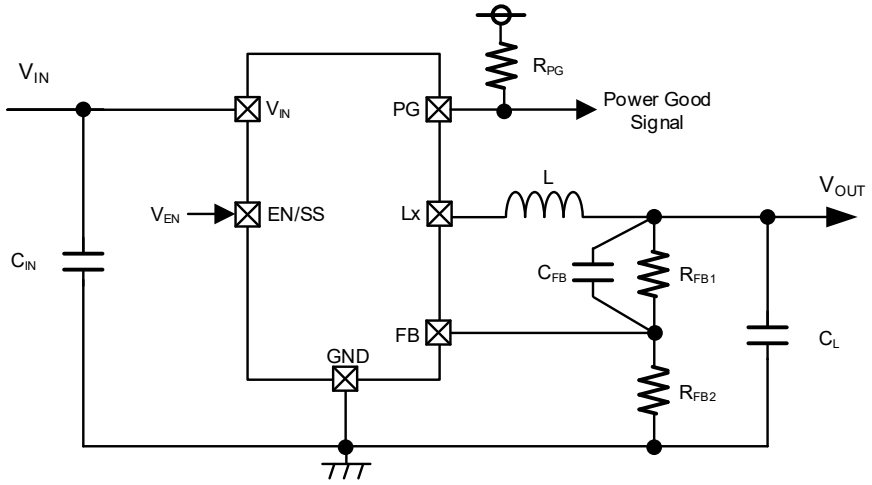


CIRCUIT⑤



.

■TYPICAL APPLICATION CIRCUIT / Parts Selection Method



	VOUTSET	MANUFACTURER	PRODUCT NUMBER	VALUE
L	VOUTSET≦3.3V	TDK	CLF5030NIT-2R2N-D	2.2μH
		Coilcraft	XGL3530-222ME	
			XGL4030-222ME	
		Taiyo Yuden	LCXND4040TKL2R2MDG	
		Tokyo Coil	SHP0420P-F2R2NAP	
	3.3V＜VOUTSET≦6V	TDK	CLF5030NIT-3R3N-D	3.3μH
		Coilcraft	XGL3530-332ME	
			XGL4030-332ME	
		Taiyo Yuden	LCXND4040TKL3R3MDG	
		Tokyo Coil	SHP0420P-F3R3NAP	
	6V＜VOUTSET	TDK	CLF5030NIT-4R7N	4.7μH
		Coilcraft	XGL3530-472ME	
			XGL4030-472ME	
		Taiyo Yuden	LCXND5050WDL4R7MMG	
		Tokyo Coil	SHP0530P-F4R7AP	

■TYPICAL APPLICATION CIRCUIT / Parts Selection Method

	V_{OUTSET}	MANUFACTURER	PRODUCT NUMBER	VALUE
C_{IN}	-	TDK	CGA4J3X7R1H225K125AB	2.2μF/50V
C_L	$V_{OUTSET} \leqq 6V$	TDK	CGA4J3X7S1A106K125AB	10μF/10V 2parallel
	$6V < V_{OUTSET} \leqq 12V$	TDK	CGA4J1X7S1E106K125AC	10μF/25V 2parallel
	$12V < V_{OUTSET}$	TDK	CGA5L1X7R1V106K160AC	10μF/35V 2parallel
		TDK	CGA5L1X7R1H106K160AC	10μF/50V 2parallel

(*1) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(*2) If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance(C_{IN}), place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase and the IC may malfunction.

(*3) If a large-capacity capacitor is used as output capacitor(C_L), the output stability may be reduced, and the ripple voltage may increase. Even if a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor is used as output capacitor(C_L), place a low-ESR ceramic capacitor in parallel. Even if the capacitance is within the recommended range, the output stability may be reduced depending on the type and ESR etc. of the capacitor used, so please thoroughly test it on the actual equipment before use.

■TYPICAL APPLICATION CIRCUIT / Parts Selection Method (Continued)

＜Output voltage setting＞

The output voltage can be set by adding an external dividing resistor.

The output voltage setting is determined by the equation below based on the values of R_{FB1} and R_{FB2}.

$$V_{OUTSET} = V_{FBE} \times (R_{FB1}+R_{FB2}) / R_{FB2}$$
$$R_{FB2} \leqq 200k\Omega \text{ and } R_{FB1}+R_{FB2} \leqq 1M\Omega$$

If the IC does not operate properly due to external noise, noise resistance performance can be improved by using a combination of R_{FB1} and R_{FB2} that is smaller than the above conditional expression.

＜C_{FB} setting＞

Adjust the value of the phase compensation speed-up capacitor C_{FB} within ±20% using the equation below.

$$C_{FB} = \frac{1}{2\pi \times fzfb \times R_{FB1}}$$

$$fzfb = \frac{1}{2\pi\sqrt{C_L \times L}}$$

【Calculation Example】

To set output voltage to 5.0V, (f_{osc}=2.2MHz, C_L=10μF×2, L=3.3μH)

V_{OUTSET} = 0.75V×(680kΩ+120kΩ)/120kΩ = 5.0V, and fzfb is set to a target of 19.6kHz using the above equation,

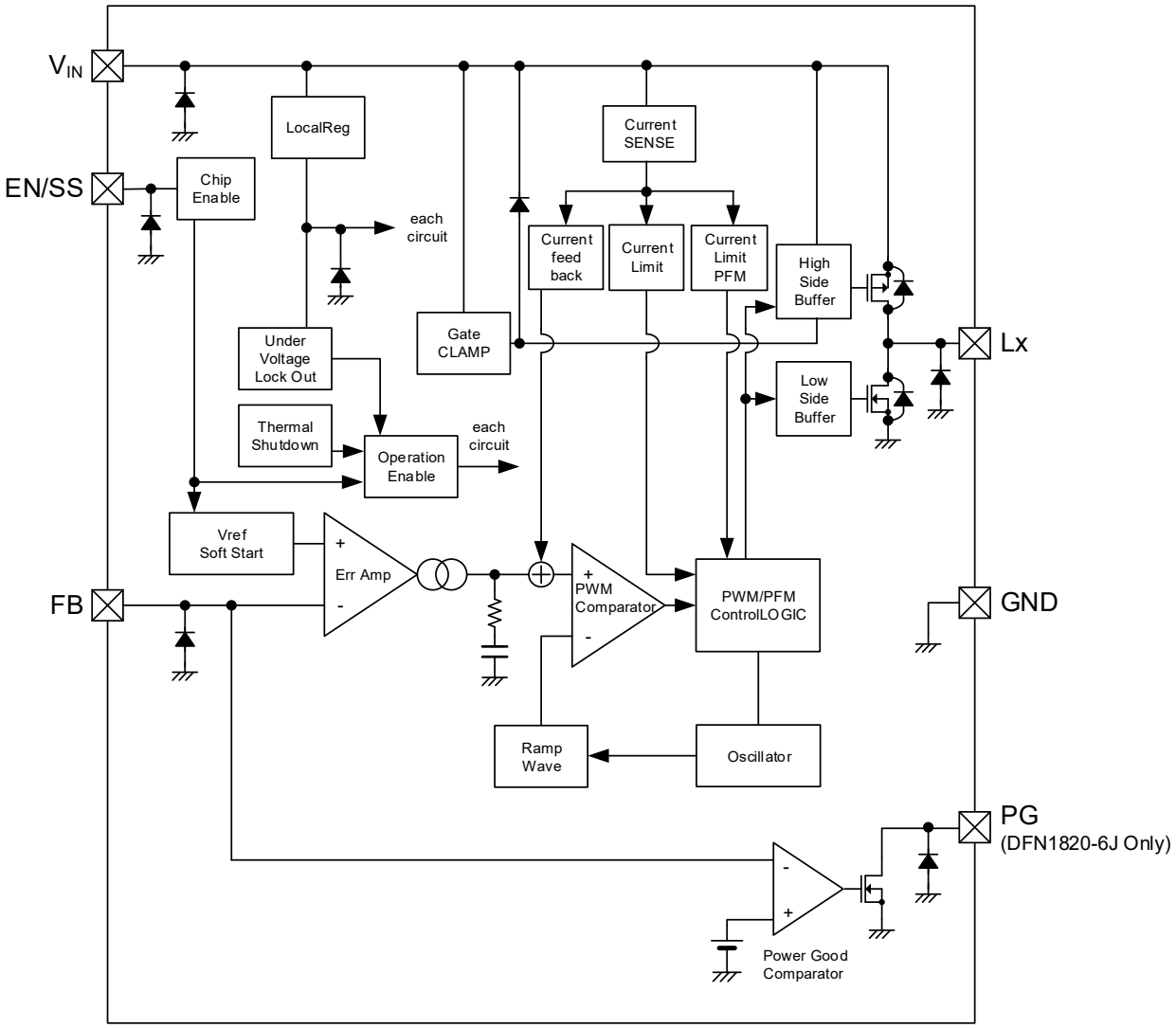
C_{FB} = 1/(2×π×19.6kHz×680kΩ) = 11.95pF, which is 12pF for the E24 series.

【Typical example】

V_{OUTSET}	R_{FB1}	R_{FB2}	L	C_L	C_{FB}	fzfb
3.3V	510kΩ	150kΩ	2.2μH	10μF×2	13pF	24.0kHz
5.0V	680kΩ	120kΩ	3.3μH	10μF×2	12pF	19.6kHz
12.0V	360kΩ	24kΩ	4.7μH	10μF×2	27pF	16.4kHz

■OPERATIONAL EXPLANATION

The XD9704/XD9705 series consists internally of a reference voltage supply with soft-start function, error amplifier, PWM comparator, ramp circuit, oscillator circuit, phase compensation (current feedback) circuit, current limit circuit, current limiting-PFM circuit, High-side driver FET, Low-side driver FET, buffer drive circuit, internal power supply (Local Reg) circuit, under voltage lockout (UVLO) circuit, gate clamp circuit, thermal shutdown circuit etc.



■OPERATIONAL EXPLANATION

＜Normal operation＞

The reference voltage Vref and FB pin voltage are compared using an error amplifier, the output from the error amplifier is phase compensated, and the signal is input to the PWM comparator to determine the ON time of switching during PWM operation.

The output signal from the error amplifier is compared to the ramp wave by the PWM comparator, and the output is sent to the buffer drive circuit and output from the Lx pin as the duty width of switching. This operation is performed continuously to stabilize the output voltage.

The current sense circuit monitors the driver FET current at each switching, and the output signal from the error amplifier is modulated as a multi-feedback signal (current feedback circuit). This allows a stable feedback control to be achieved even when even when a low ESR capacitor such as a ceramic capacitor is used, and this stabilizes the output voltage.

XD9704 Series : F-PWM control

XD9704 series operates in forced PWM mode.

XD9704 series operates at a constant frequency f_{OSC} regardless of the output current, making it easy to filter switching noise.

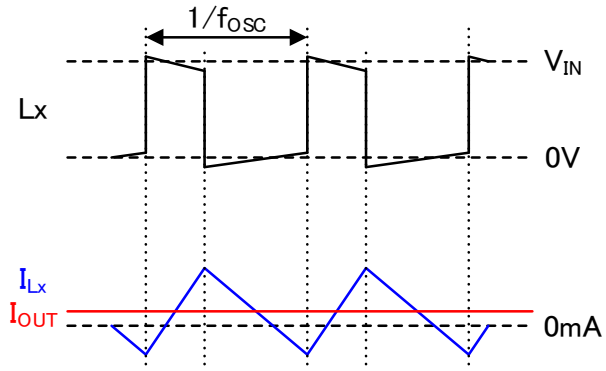
Also, if the FB pin voltage remains higher than V_{FB}, the switching operation will be stopped (High side driver FET turned off, Low side driver FET turned on) until the FB pin voltage drops.

XD9705 Series : PWM/PFM Auto switching control

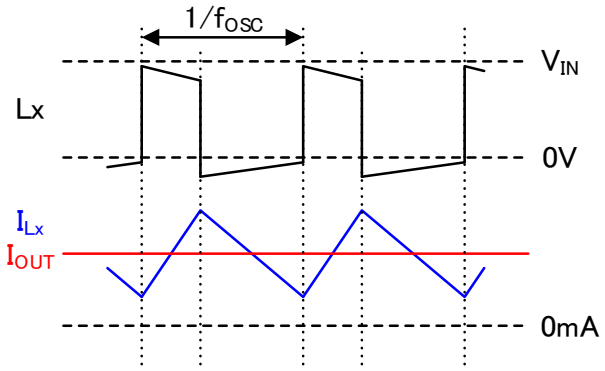
XD9705 series operates in PWM/PFM automatic switching mode.

PWM/PFM automatic switching control drops the switching frequency during light loads by turning on the High side driver FET until the coil current reaches the I_{PFM} (TYP. 450mA).

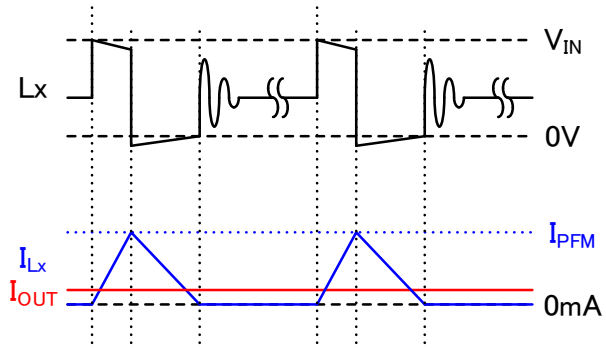
This operation reduces the loss during light loads and achieves high efficiency from light to heavy loads. As the output current increases, the switching frequency increases proportional to the output current, and when the switching frequency increases f_{OSC}, the circuit switches from PFM control to PWM control and the switching frequency becomes fixed.



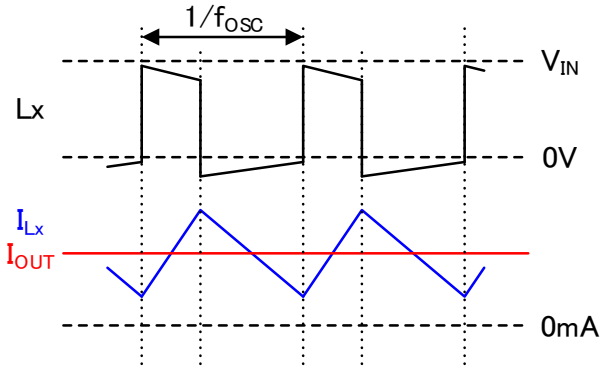
XD9704 Series(F-PWM Control)：Example of light load operation



XD9704 Series (F-PWM Control)：Example of heavy load operation



XD9705 Series(PWM/PFM Control)：Example of light load operation



XD9705 Series(PWM/PFM Control)：Example of heavy load operation

■OPERATIONAL EXPLANATION

＜EN Function / Start Mode・Soft-start Function＞

The state of the IC can be switched by applying voltage to the EN/SS pin.

SIGNAL	STATUS
H	Active
L	Stand-by
OPEN	Stand-by

EN/SS="L" : Stand-by mode

When the "L" voltage is input to the EN/SS pin, the IC enters the stand-by mode, and the current consumption is reduced to the stand-by current I_{STB} (TYP. 0.6μA). In the stand-by mode, no signal is output to the Lx pin and the output voltage does not rise.

In addition, various protection functions stop operating.

EN/SS="H" : Active mode

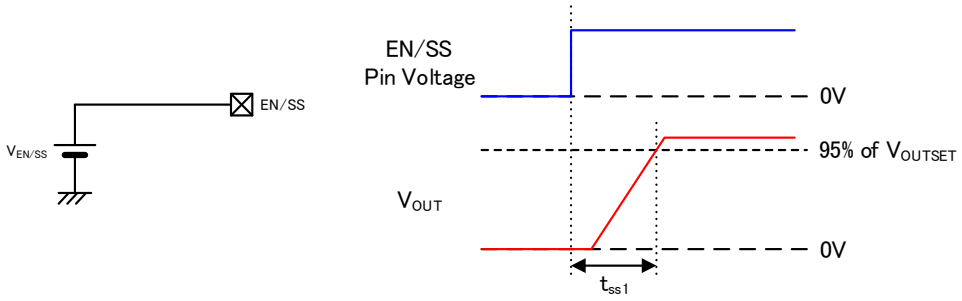
When the EN/SS pin voltage is "H", the IC becomes active. When the IC becomes active, it enters start-up mode and increases the output voltage to the set output voltage.

In start-up mode, a soft-start function is provided to gently raise the output voltage to suppress inrush current at start-up.
The soft-start time can be adjusted by externally mounting a capacitor and resistor on the EN/SS pin.

During the start-up mode, the device operates in the same way as in normal operation, except that the reference voltage increases linearly.

(a) Internal soft-start time (without external RC)

When the EN/SS pin voltage rises steeply, the output voltage rises with an internally set soft-start time of t_{ss1} (TYP. 2.2ms) and shifts to normal mode.



(b) Soft-start time external adjustment (with external RC)

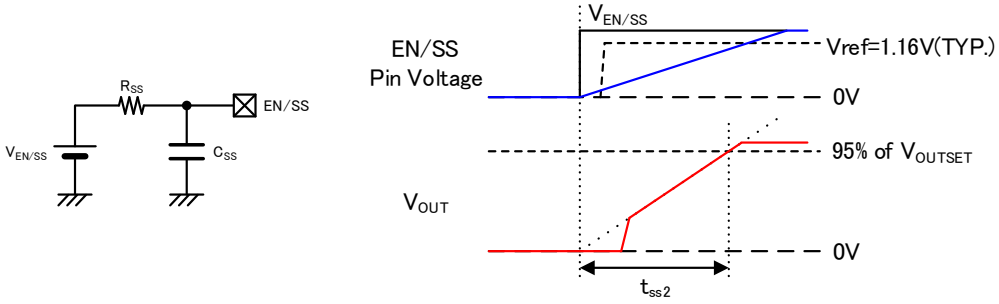
The soft-start time can be adjusted by externally mounting a capacitor and resistor on the EN/SS pin.
The externally set soft-start time (t_{SS2}) is determined by the following formula, depending on the EN/SS pin voltage ($V_{EN/SS}$), R_{SS}, and C_{SS} values.

$$t_{ss2} = C_{ss} \times R_{ss} \times \ln \frac{V_{EN/SS}}{V_{EN/SS} - 1.16V}$$

For example, When the soft-start time at C_{SS} = 0.47μF, R_{SS} = 430kΩ, $V_{EN/SS}$ = 12V

$$t_{ss2} = 0.47 \times 10^{-6} \times 430 \times 10^{3} \times \ln \frac{12}{12 - 1.16} = 21\text{ms}$$

However, it cannot start faster than the internally setting soft-start time t_{ss1}.



* Definition of soft-start time : Time from $V_{EN/SS}$ start-up until output voltage reaches 95% of set output voltage.

■OPERATIONAL EXPLANATION

＜Current Limit＞

The current limit circuit of this IC detects the current flowing through the driver FET connected to Lx pin and equivalently monitors the coil current. The current limit function operates when over current is detected. When the current limit function operates, the High side current limit function and Low side current limit function operate.

The current limit state continues until the overcurrent state is released, and the output voltage automatically recovers when the overcurrent state is released.

A current fold-back circuit is used for the current limit function.

The current foldback circuit reduces the current limit when the output voltage drops. This operation reduces the output current when the output voltage drops.

High side Current Limit

The High side current limit function detects when the coil current exceeds the High side current limit value I_{LIMH} (TYP. 1.4A) and turns off the High side driver FET. In other words, it controls the coil current so that it does not exceed a certain peak value. However, if the input voltage is high, the coil current peak value may exceed I_{LIMH} due to the operation delay of the internal circuit.

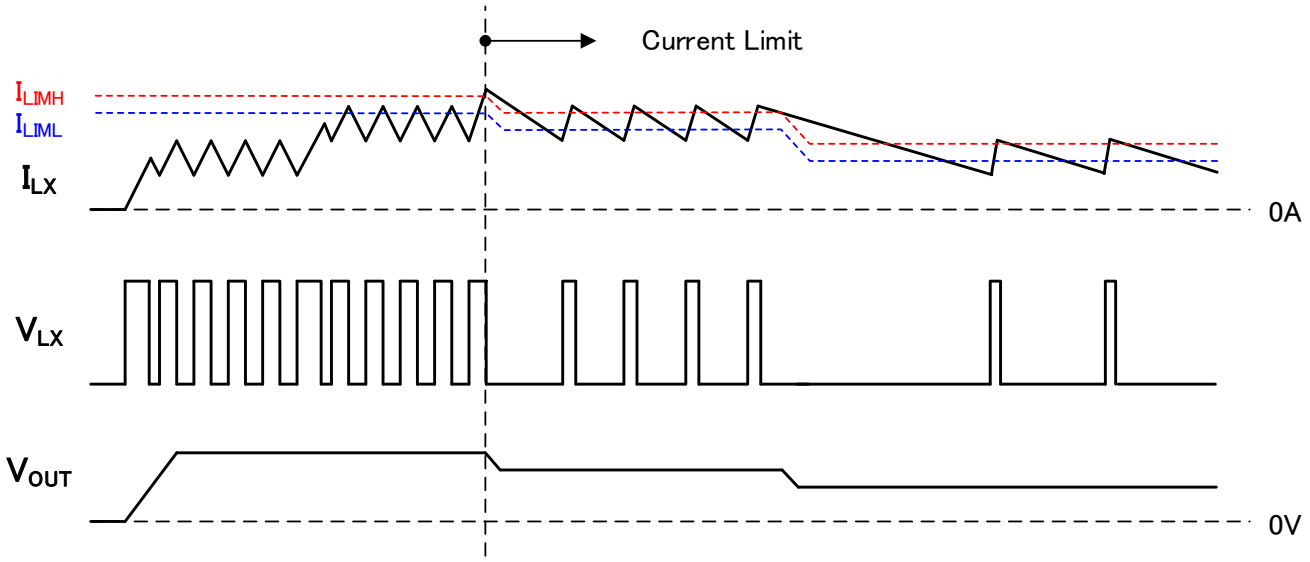
Low side Current Limit

The Low side current limit function turns on the Low side driver FET until the coil current becomes less than the Low side current limit value I_{LIML} (TYP. 1.0A). In other words, it controls the coil current to stay below a certain coil current bottom value.

The current limit function also operates during start-up mode.

During start-up mode, the output voltage is lower than the set output voltage, the current limit value is reduced, which speeds up overcurrent detection.

If an output capacitance with a higher effective capacitance value than the recommended component is used, the start-up will take place while the current limit function is operating, and the start-up time may be much longer than the soft-start time.



■OPERATIONAL EXPLANATION

＜Thermal Shutdown＞

The junction temperature is monitored to protect the IC from thermal destruction.

When the junction temperature reaches the thermal shutdown detection temperature T_{TSD} (TYP. 160°C), the thermal shutdown is activated, the High side driver FET and Low side driver FET are turned off. When the junction temperature drops to the thermal shutdown release temperature T_{TSD}-T_{HYS} (TYP. 135℃) by stopping the current supply, the output voltage is turned on by the start-up mode, and then normal operation starts.

In the XD9705 series, the thermal shutdown function is disabled during PFM control to reduce current consumption under light load conditions. The thermal shutdown function becomes active when the output current increases and the operation transitions to PWM control.

＜UVLO＞

This function monitors the internal power supply of the IC and prevents false pulse output from the Lx pin due to unstable operation when the internal power supply is low. As the IC's internal power supply drops as the V_{IN} pin voltage drops, the UVLO function operates.

When the V_{IN} pin voltage falls below V_{UVLOD}(TYP. 2.7V), the UVLO function operates, and forcibly turns off the driver FETs.

When the V_{IN} pin voltage rises above V_{UVLOR}(TYP. 2.8V), the UVLO function is released, and the output voltage rises according to the start-up mode.

Moreover, during the UVLO operation, the internal circuit is operating because stopping by UVLO is not same as a stand-by mode and just switching operation is stopped.

＜Negative Current Limit＞

When the output voltage becomes higher than the set voltage, the Low side driver FET turns on to reduce the output voltage. If the Low side driver FET continues to be turned on, the coil current reverses and a negative current continues to flow.
This reverse current is limited to -900mA (TYP.) by the negative current limit function.

When the negative current limit function operates, the Low side driver FET turns off and remains until the next cycle. During this period, the reverse current flows through the parasitic diode of the High side driver FET into the power supply connected to the V_{IN} pin.

If the negative current limit function operates during start-up mode, the switching operation stops until the reference voltage becomes higher than the FB voltage.

＜Over Voltage Protection＞

An output overvoltage protection function is built in to suppress output voltage overshoots after completion of start-up or transient response. When the FB pin voltage rises above V_{OVP} (TYP. 0.81V), the output overvoltage protection function operates and forcibly turns off the High side driver FET.

In forced PWM control (XD9704), the Low side driver FET is turned on immediately after the output overvoltage protection function operates and remains this state until the next cycle.

In PWM/PFM automatic switching control (XD9705), the driver FET is turned off by the output overvoltage protection function. When the output voltage drops to the set value due to the output current, switching operation resumes.

■OPERATIONAL EXPLANATION

＜Power Good＞

On DFN1820-6J Package, the output state of IC can be monitored using the power good function.

CONDITIONS		SIGNAL
EN/SS = H	$V_{FB} > V_{PGDET}$	H (High impedance)
	$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
	Thermal Shutdown	L (Low impedance)
	UVLO ($V_{IN} < V_{UVLOD}$)	Undefined State
EN/SS = L	Stand-by	L (Low impedance)

The PG pin is an Nch open drain output, therefore a pull-up resistance (approx. 100kΩ) must be connected to the PG pin. When the power good function is not used, connect the PG pin to GND or leave it open.

A delay time of 400μs(TYP.) is provided from the moment, the FB pin voltage drops below V_{PGDET} to PG="L".
If the FB pin voltage returns to a voltage higher than V_{PGDET} during the delay time, PG remains “H”.
This prevents PG="L" due to output undershoot during transient response.
In addition, there is no intentional delay for PG="L" due to the operation of the protection function or transition to the stand-by state.

■NOTES ON USE

1) For the phenomenon of temporary and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications. Also, if used under out of the recommended operating range, the IC may not operate normally or may cause deterioration.

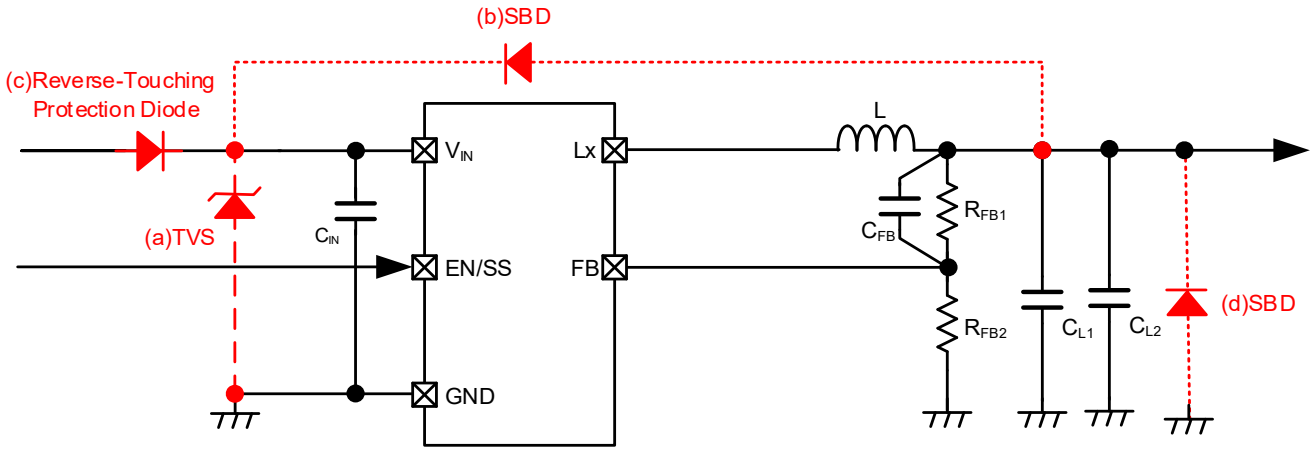
If a voltage exceeding the absolute maximum voltage is applied to the IC due to chattering caused by a mechanical switch or an external surge voltage, please use a protection circuit as a countermeasure.
Please see the countermeasures from (a) to (d) shown below.

(a) When voltage exceeding the absolute maximum ratings comes into the V_{IN} pin due to the transient change on the power line, there is a possibility that the IC breaks down in the end. To prevent such a failure, please add a TVS between V_{IN} and GND as a countermeasure.

(b) When the input voltage decreases below the output voltage, there is a possibility that an overcurrent will flow in the IC's internal parasitic diode and exceed the absolute maximum rating of the Lx pin.
If the current is pulled into the input side by the low impedance between Vin and GND, then please add an SBD between V_{OUT} and V_{IN} as a countermeasure.

(c) When a negative voltage is applied to the input voltage by a reverse connection or chattering, an overcurrent could flow in the IC's parasitic diode and damage the IC. Please add a reverse touching protection diode as a countermeasure.

(d) When a sudden surge of electrical current travels along the V_{OUT} pin and GND due to a short-circuit, electrical resonance of circuit involving parasitic inductor of cable related to short circuit. An output capacitor (C_L) and impedance such as V_{OUT} line generates a negative voltage exceeding the breakdown voltage and may damage the device. Please take measures such as adding an SBD between V_{OUT} and GND.



2) Switching regulators such as DC/DC converters generate spike noise and ripple voltage. The DC/DC converter characteristics depend greatly on the externally connected components such as coil inductance value, capacitor, board layout of peripheral components. Please refer to the specifications and standard circuit examples of each component when carefully considering which components to select.

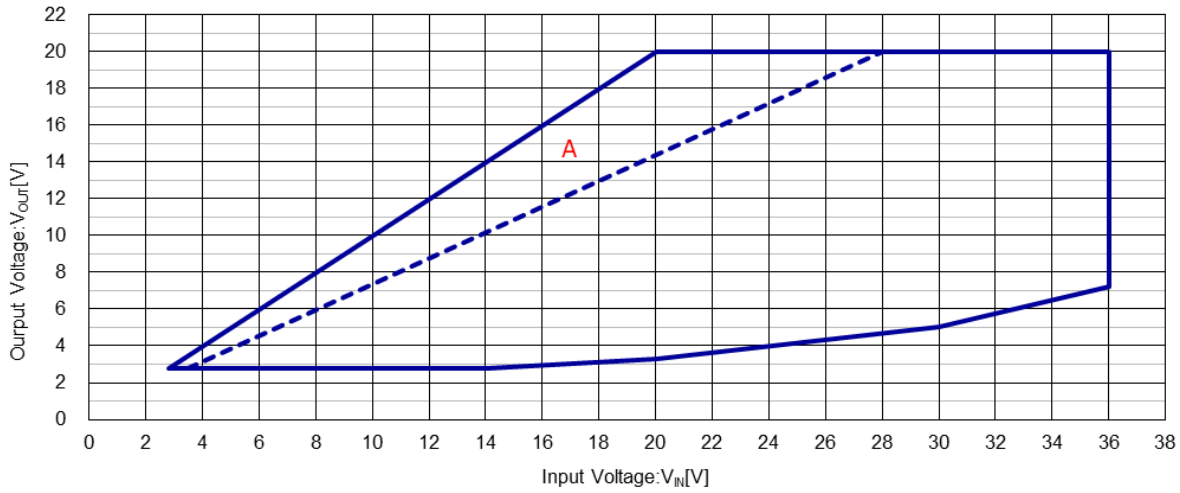
■NOTES ON USE

3) Stable operating range

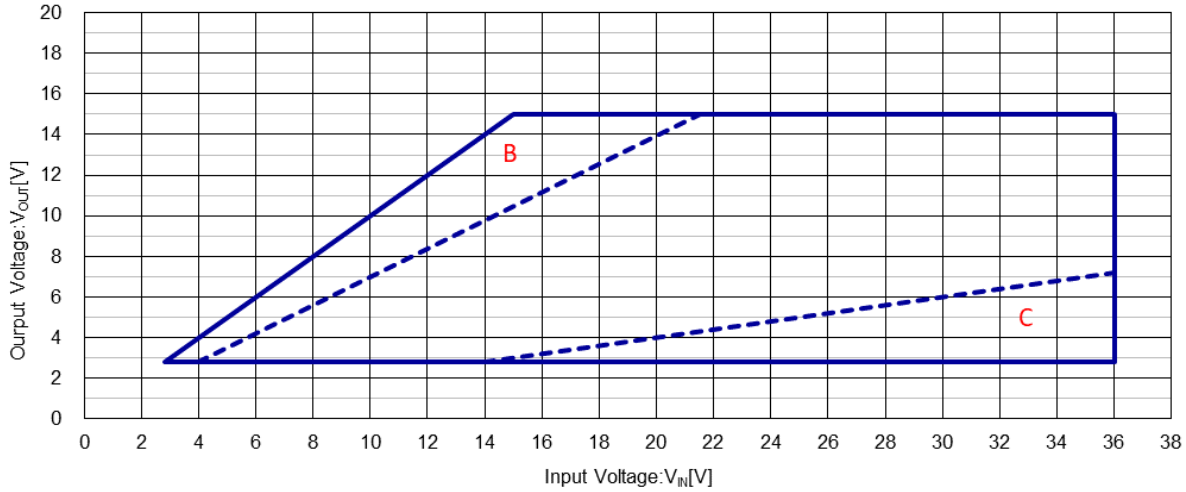
The recommended operating range of this IC can operate normally varies depending on the product number.
Please confirm that the power supply specifications you are using are within the recommended operating range before use.

V_{OUTSET}-V_{IN} Stable operating range

XD9704B75D (F-PWM control, f_{OSC}:2.2MHz)



XD9705B75D (PWM/PFM Auto switching control, f_{OSC}:2.2MHz)



【Operation within the stable operating range】

Please note the following points when using in areas A to C within the stable operating range.

(A) The switching frequency may drop or the V_{OUT} ripple voltage may increase near the switch to 100% Duty cycle.

(B) The coil current may reverse, and the efficiency may drop significantly due to F-PWM operation instead of PFM operation at light loads. In addition, the switching frequency may drop and the V_{OUT} ripple voltage may increase near the switch to 100% Duty cycle.

(C) Due to the Minimum On-time, the Lx oscillation may become unstable and the V_{OUT} ripple voltage may increase, or the IC may not switch to PWM operation up to the maximum output current.

【Operation over the stable operating range】

If the IC is used over the stable operating range, the following operations may occur, and the IC may not operate normally.

(a) Under conditions where the step-down ratio is high, Lx oscillation may not be stable or pulse skipping may occur and the ripple voltage may increase, due to Minimum On-time.

(b) Under conditions where the step-down ratio is low, the unit may operate at Maximum Duty Cycle and the output voltage may drop below the set output voltage.

■NOTES ON USE

4) The ripple voltage could be increased when switching from discontinuous conduction mode to continuous conduction mode and when switching to 100% Duty cycle.

5) When using an external soft-start using the EN/SS pin, if the EN/SS pin is at an intermediate voltage when the power is turned on, the external soft-start will not work, and the inrush current will increase. etc.

6) The output overvoltage protection function suppresses output voltage overshoot, but on the other hand, it operates to suppress the operation of the error amplifier.
Therefore, the output overvoltage protection function and the error amplifier may operate mutually, causing the output voltage to become unstable voltage. If the output overvoltage protection function operates and the output voltage is unstable due to sudden load fluctuations, etc., take measures such as increasing the output capacity.

7) In the XD9705 series, the thermal shutdown function is disabled during PFM control to reduce current consumption under light load conditions. The thermal shutdown function becomes active when the output current increases and the operation transitions to PWM control. However, under high input voltage conditions, the transition current from PFM to PWM control increases; therefore, the thermal shutdown function may only become effective near the maximum output current.

8) Torex places an importance on improving our products and their reliability. We request that users incorporate fail safe designs and post aging protection treatment when using Torex products in their systems.

9) Instructions of pattern layouts
Especially noted in the pattern layout are as follows.
Please refer to the reference pattern layout on the next page.

(a) Wire the large current line using thick, short connecting traces.
This makes it possible to reduce the wire impedance, which is expected to reduce noise and improve heat dissipation.
If the wire impedance of the large current line is large, it may cause noise, or the IC cannot operate normally.

(b) Place the input capacitance C_{IN}, output capacitance C_L, inductor L and IC which the large current flows on the same surface.
If they are placed on both sides, a large current will flow through Via which has high impedance, it may cause noise and the IC may not operate normally.

(c) Please mount each external component as close to the IC as possible.
Especially place the input capacitance C_{IN} near the IC and connect it with as low impedance as possible.
If the input capacity C_{IN} and IC are too far apart, it may cause noise, or the IC may not operate normally.

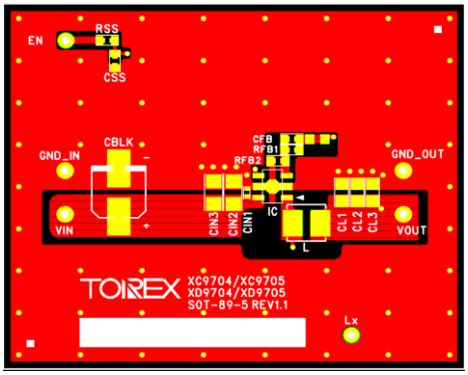
(d) The FB line connected to the FB pin is extremely sensitive to noise, so connect it with the shortest possible wire. If the FB line is long, the IC may not operate normally due to switching noise and external noise.
If the IC does not operate normally due to external noise, etc., please review the board layout or reduce the FB resistance value.
If the FB resistance value is lowered, the efficiency during PFM operation may decrease. Please use it after confirming it with the actual machine.

■NOTES ON USE

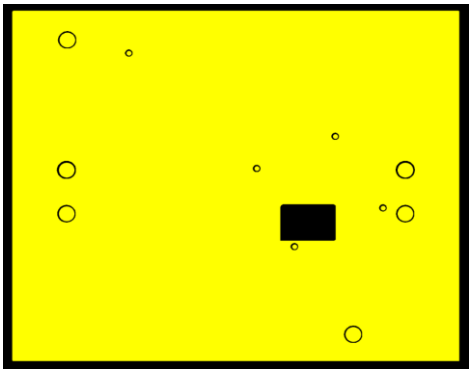
＜Pattern layout＞

SOT-89-5

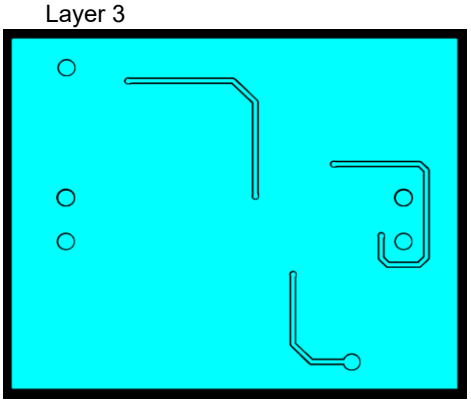
Layer 1



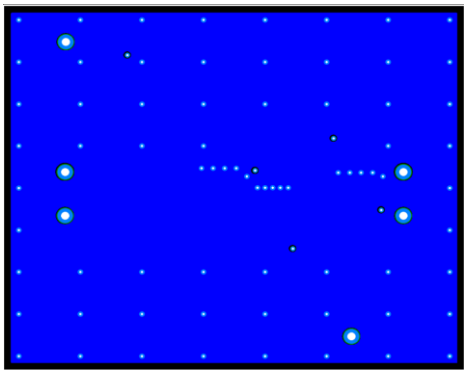
Layer 2



Layer 3

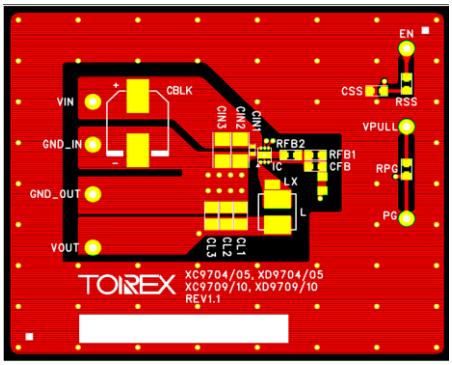


Layer 4

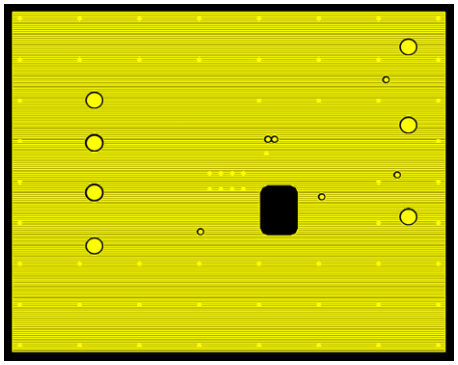


DFN1820-6J

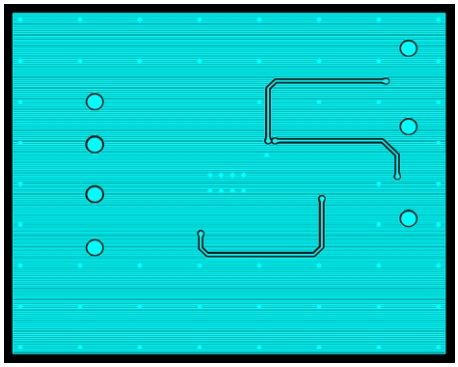
Layer 1



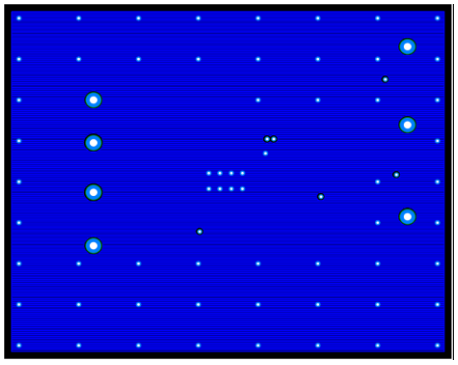
Layer 2



Layer 3



Layer 4

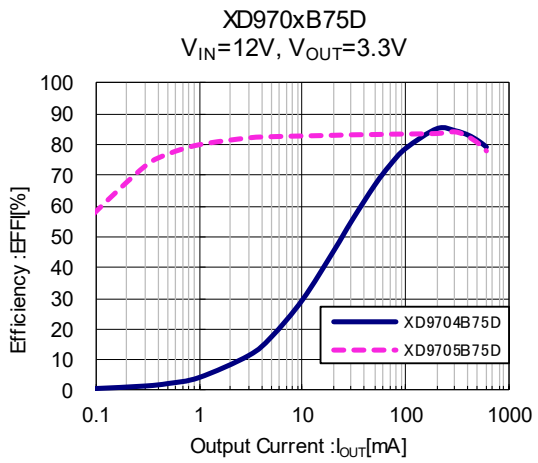


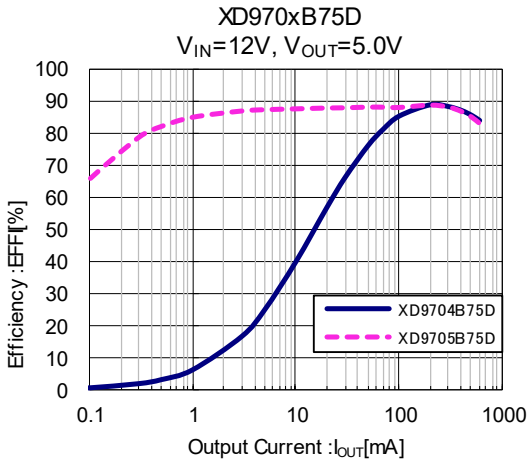
■TYPICAL PERFORMANCE CHARACTERISTICS

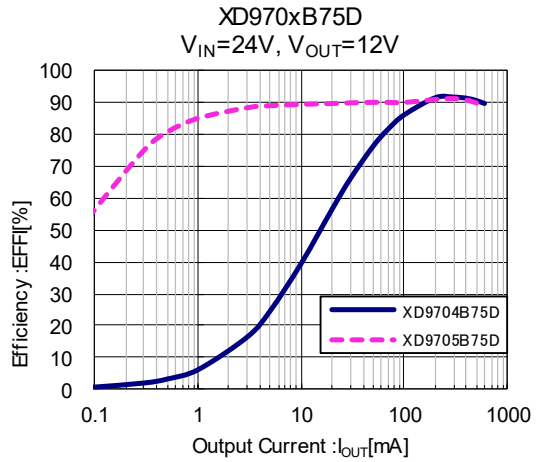
PRODUCTS	CONDITIONS	L	C_{IN}	C_L
XD9704B75D XD9705B75D	V_{IN}=12V, V_{OUT}=3.3V	2.2μH (CLF5030NIT-2R2N)	2.2μF (CGA4J3X7R1H225K125AB)	10μF×2 (CGA4J3X7S1A106K125AB)
	V_{IN}=12V, V_{OUT}=5.0V	3.3μH (CLF5030NIT-3R3N)	2.2μF (CGA4J3X7R1H225K125AB)	10μF×2 (CGA4J3X7S1A106K125AB)
	V_{IN}=24V, V_{OUT}=5.0V	3.3μH (CLF5030NIT-3R3N)	2.2μF (CGA4J3X7R1H225K125AB)	10μF×2 (CGA4J3X7S1A106K125AB)
	V_{IN}=24V, V_{OUT}=12V	4.7μH (CLF5030NIT-4R7N)	2.2μF (CGA4J3X7R1H225K125AB)	10μF×2 (CGA4J1X7S1E106K125AC)

■TYPICAL PERFORMANCE CHARACTERISTICS

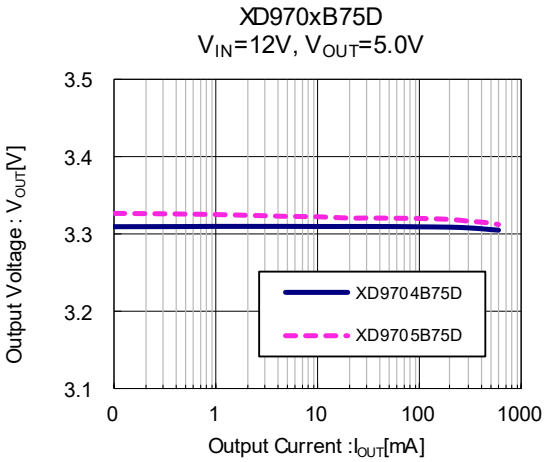
(1) Efficiency vs. Output current

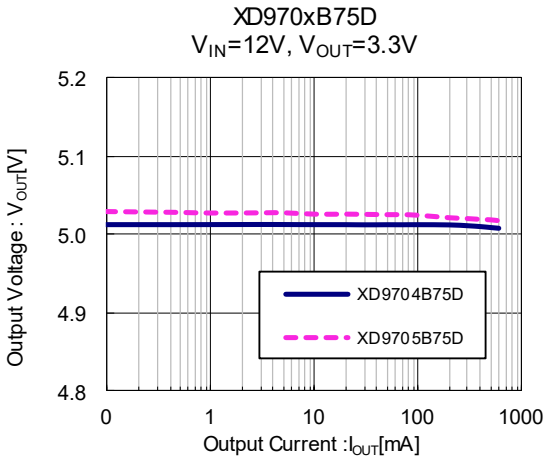






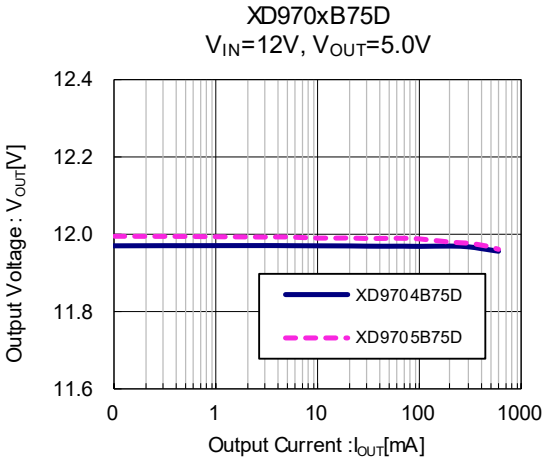
(2) Output Voltage vs. Output Current



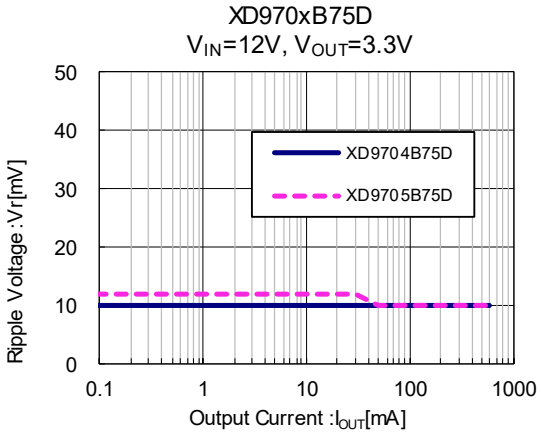


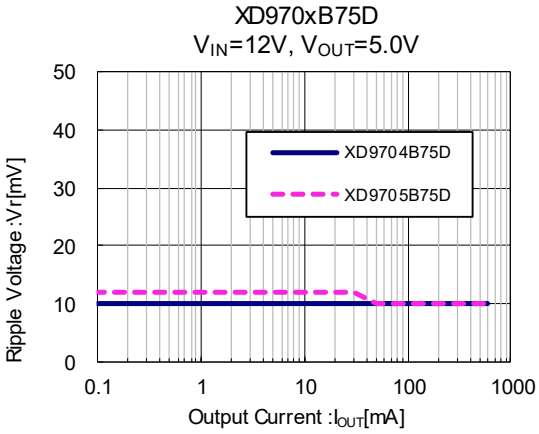
■TYPICAL PERFORMANCE CHARACTERISTICS

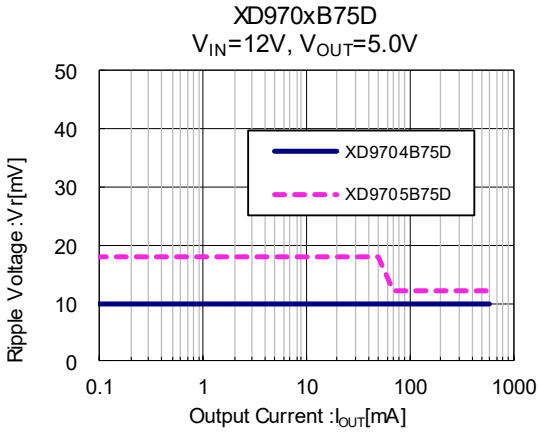
(2) Output Voltage vs. Output Current



(3) Ripple Voltage vs. Output Current

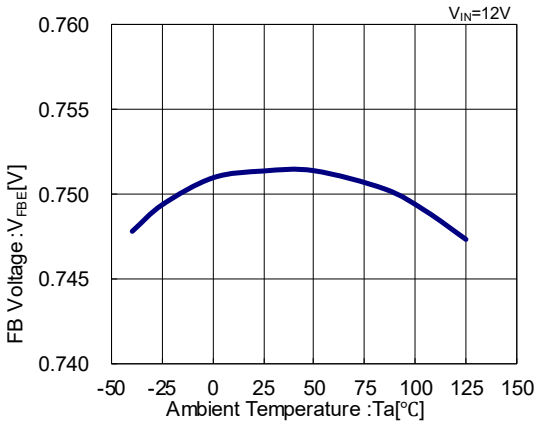




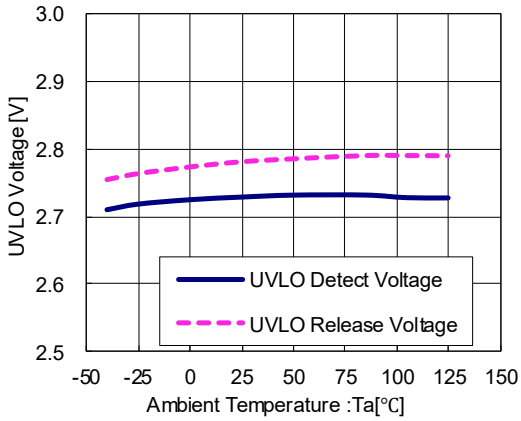


■TYPICAL PERFORMANCE CHARACTERISTICS

(4) FB Voltage vs. Ambient Temperature

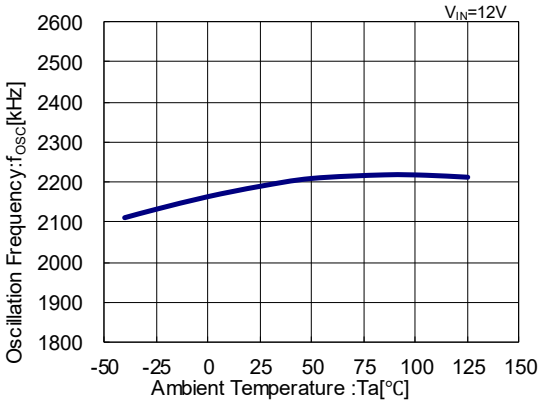


(5) UVLO Voltage vs. Ambient Temperature

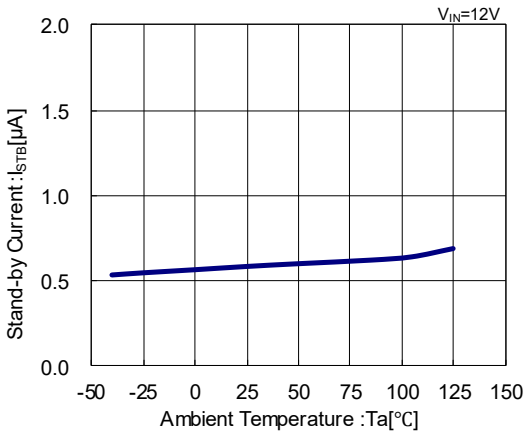


(6) Oscillation Frequency vs. Ambient Temperature

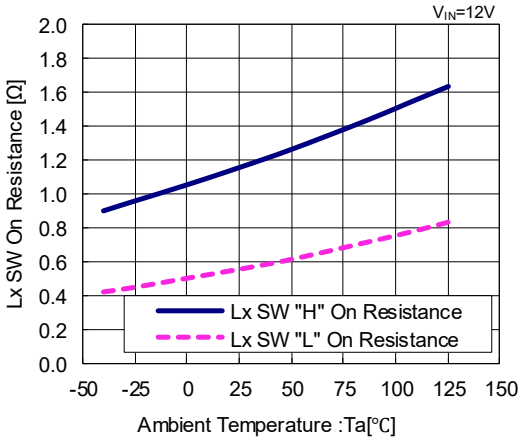
XD970xB75D



(7) Stand-by Current vs. Ambient Temperature



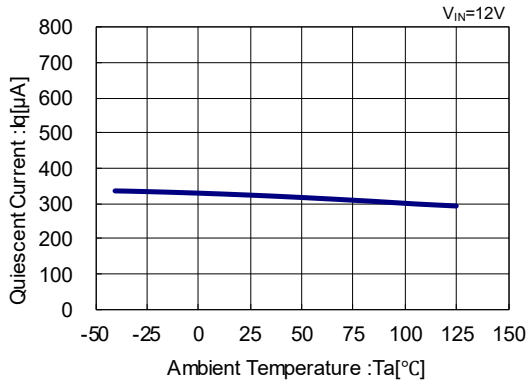
(8) Lx SW On Resistance vs. Ambient Temperature



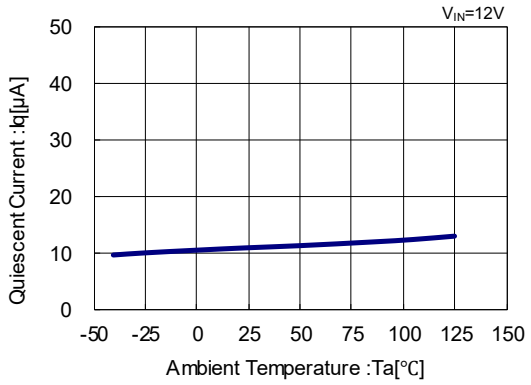
■TYPICAL PERFORMANCE CHARACTERISTICS

(9) Quiescent Current vs. Ambient Temperature

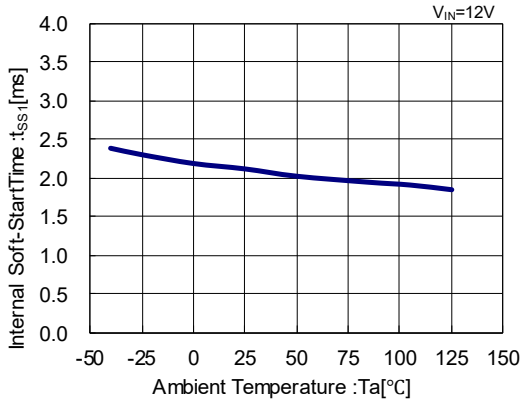
XD9704B75D



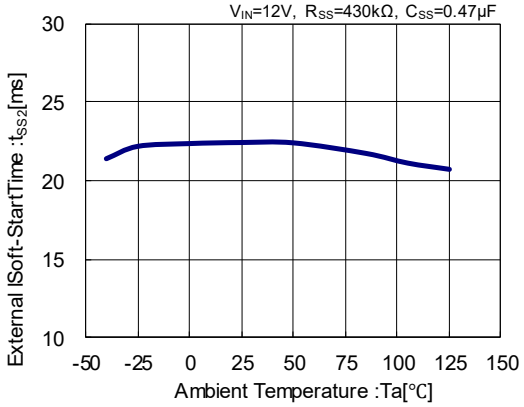
XD9705B75D



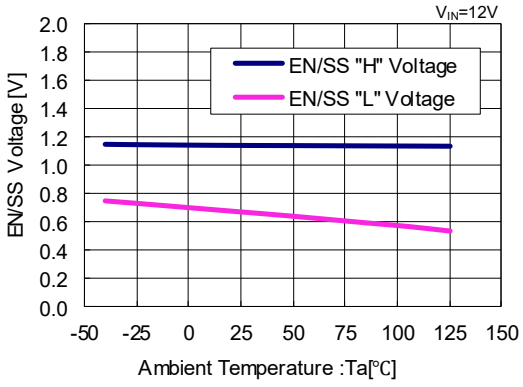
(10) Internal Soft-Start Time vs. Ambient Temperature



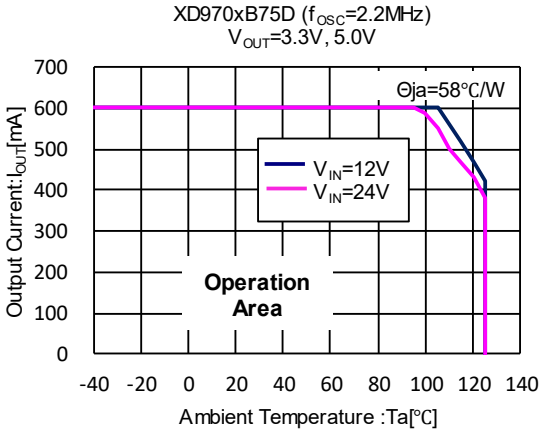
(11) External Soft-Start Time vs. Ambient Temperature



(12) EN/SS Voltage vs. Ambient Temperature



(13) Output Current Operation Area

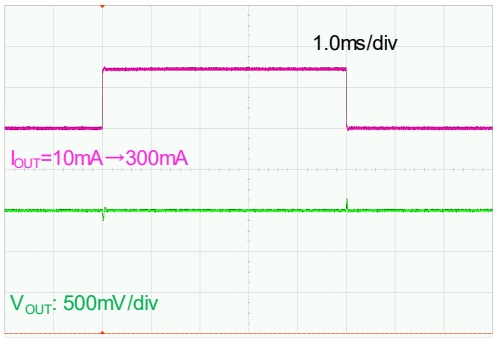


■TYPICAL PERFORMANCE CHARACTERISTICS

(14) Load Transient Response

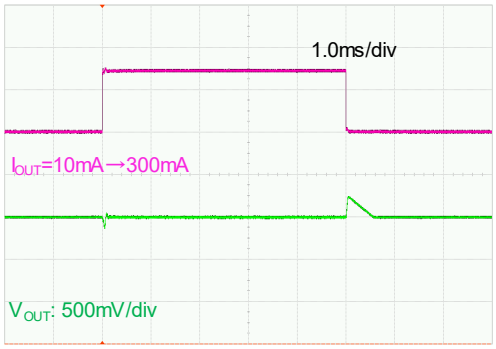
XD9704B75D

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=10mA→300mA, tr=tf=5μs



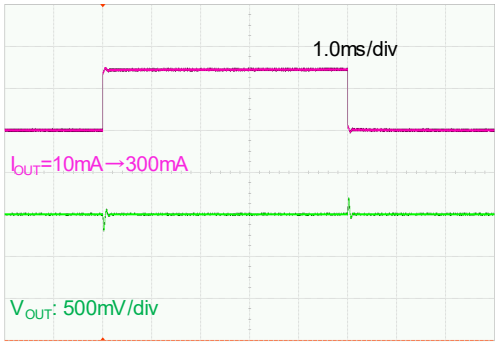
XD9705B75D

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=10mA→300mA, tr=tf=5μs



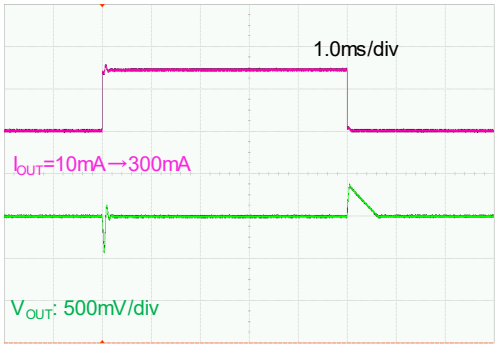
XD9704B75D

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA, tr=tf=5μs



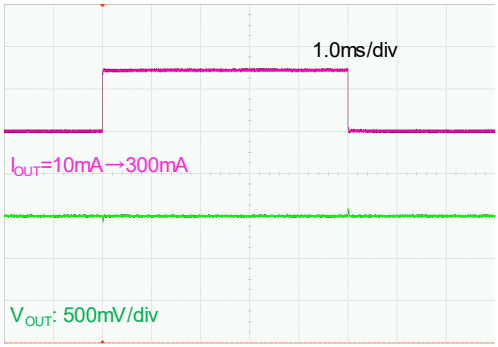
XD9705B75D

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA, tr=tf=5μs



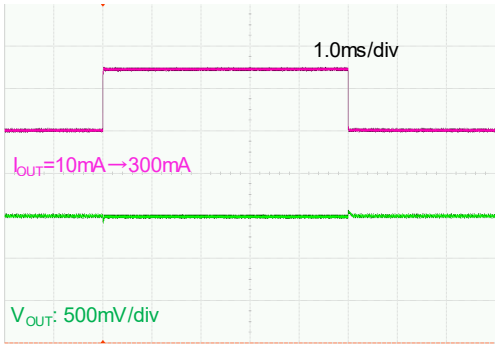
XD9704B75D

V_{IN}=24V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA, tr=tf=5μs



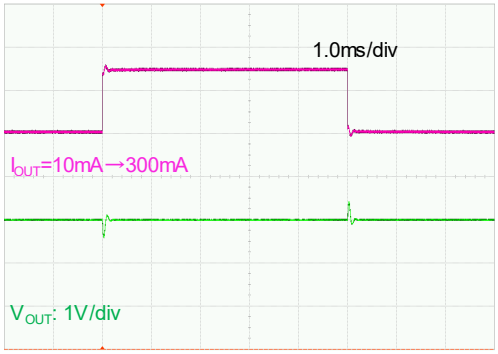
XD9705B75D

V_{IN}=24V, V_{OUT}=5.0V, I_{OUT}=10mA→300mA, tr=tf=5μs



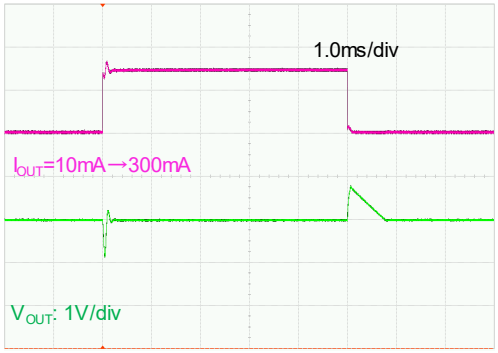
XD9704B75D

V_{IN}=24V, V_{OUT}=12V, I_{OUT}=10mA→300mA, tr=tf=5μs



XD9705B75D

V_{IN}=24V, V_{OUT}=12V, I_{OUT}=10mA→300mA, tr=tf=5μs

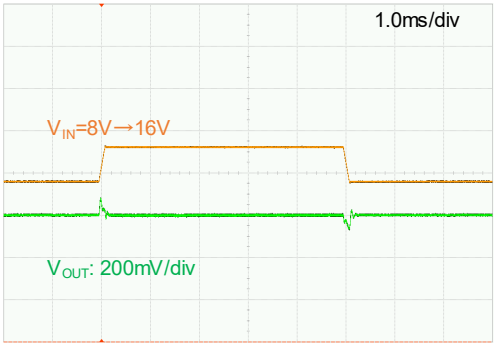


■TYPICAL PERFORMANCE CHARACTERISTICS

(15) Input Transient Response

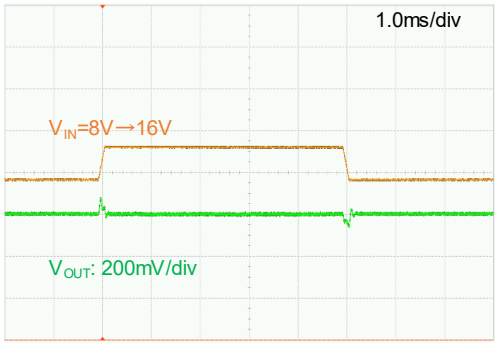
XD9704B75D

V_{IN}=8V→16V, tr=tf=100μs, V_{OUT}=3.3V, I_{OUT}=300mA



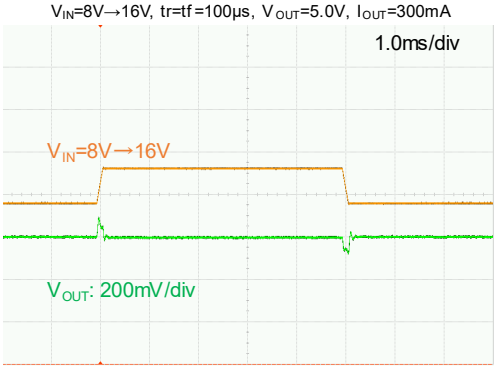
XD9705B75D

V_{IN}=8V→16V, tr=tf=100μs, V_{OUT}=3.3V, I_{OUT}=300mA



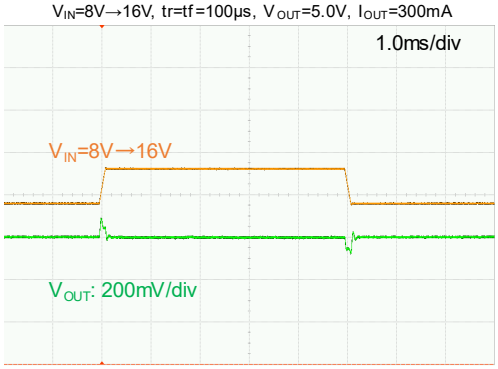
XD9704B75D

V_{IN}=8V→16V, tr=tf=100μs, V_{OUT}=5.0V, I_{OUT}=300mA



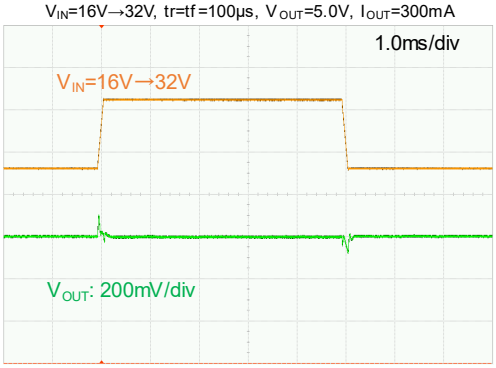
XD9705B75D

V_{IN}=8V→16V, tr=tf=100μs, V_{OUT}=5.0V, I_{OUT}=300mA



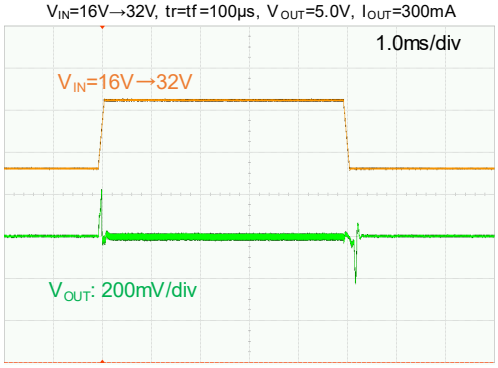
XD9704B75D

V_{IN}=16V→32V, tr=tf=100μs, V_{OUT}=5.0V, I_{OUT}=300mA



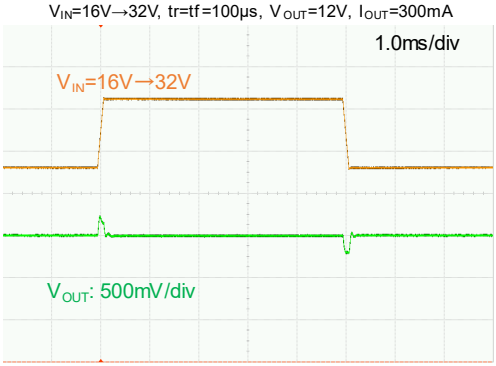
XD9705B75D

V_{IN}=16V→32V, tr=tf=100μs, V_{OUT}=5.0V, I_{OUT}=300mA



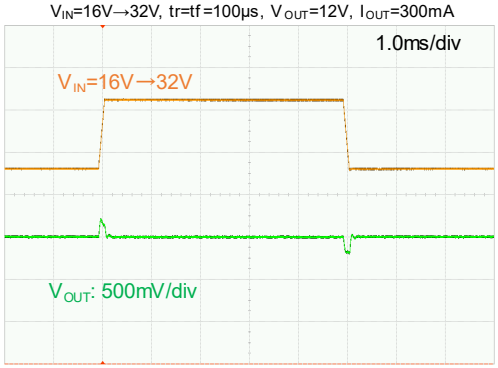
XD9704B75D

V_{IN}=16V→32V, tr=tf=100μs, V_{OUT}=12V, I_{OUT}=300mA



XD9705B75D

V_{IN}=16V→32V, tr=tf=100μs, V_{OUT}=12V, I_{OUT}=300mA

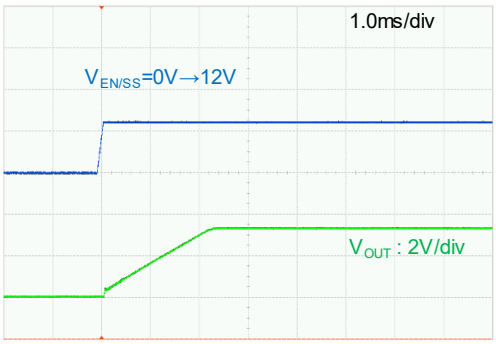


■TYPICAL PERFORMANCE CHARACTERISTICS

(16) Start-up Waveform (EN/SS Rising)

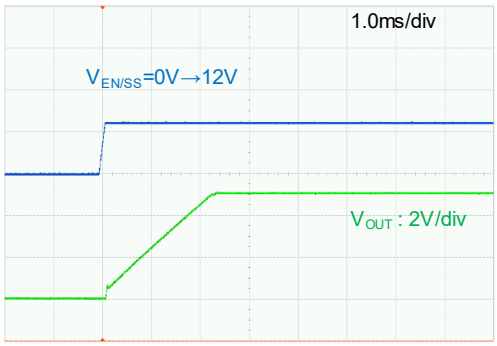
XD9704B75D/XD9705B75D

V_{IN}=12V, V_{ENSS}=0→12V, V_{OUT}=3.3V, R_L=11Ω



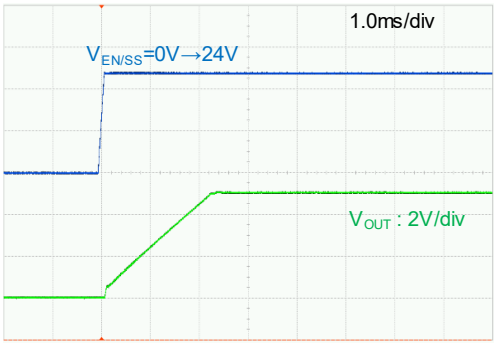
XD9704B75D/XD9705B75D

V_{IN}=12V, V_{ENSS}=0→12V, V_{OUT}=5.0V, R_L=16Ω



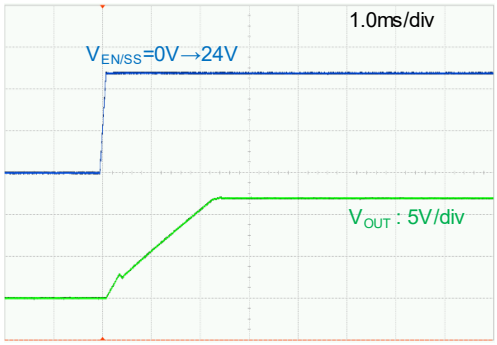
XD9704B75D/XD9705B75D

V_{IN}=24V, V_{ENSS}=0→24V, V_{OUT}=5.0V, R_L=16Ω



XD9704B75D/XD9705B75D

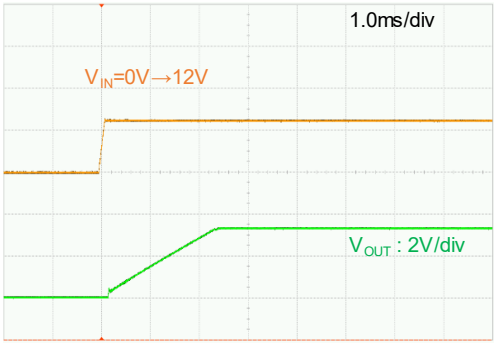
V_{IN}=24V, V_{ENSS}=0→24V, V_{OUT}=12V, R_L=40Ω



(17) Start-up Waveform (V_{IN} Rising)

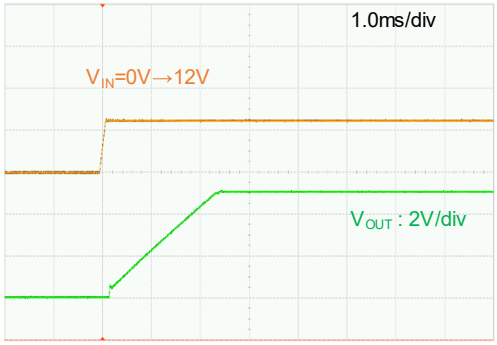
XD9704B75D/XD9705B75D

V_{IN}=V_{ENSS}=0→12V, V_{OUT}=3.3V, R_L=11Ω



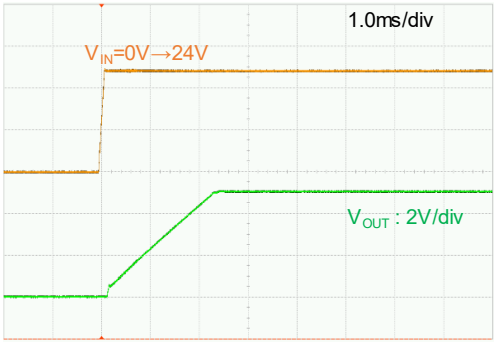
XD9704B75D/XD9705B75D

V_{IN}=V_{ENSS}=0→12V, V_{OUT}=5.0V, R_L=16Ω



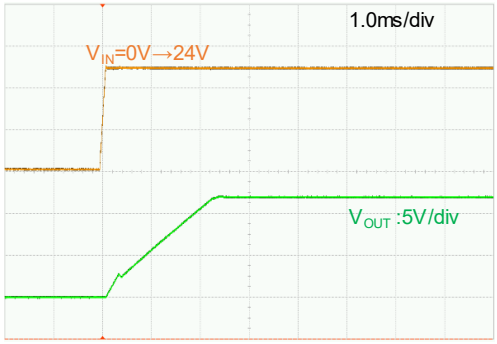
XD9704B75D/XD9705B75D

V_{IN}=V_{ENSS}=0→24V, V_{OUT}=5.0V, R_L=16Ω



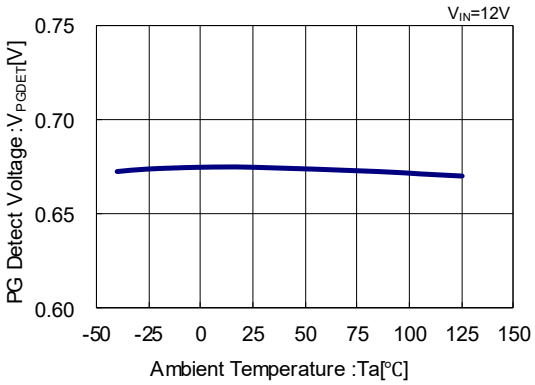
XD9704B75D/XD9705B75D

V_{IN}=V_{ENSS}=0→24V, V_{OUT}=12V, R_L=40Ω

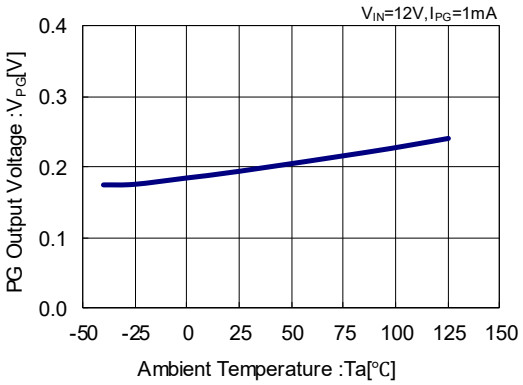


■TYPICAL PERFORMANCE CHARACTERISTICS

(12) PG Detect Voltage vs. Ambient Temperature



(13) PG Output Voltage vs. Ambient Temperature



■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
SOT-89-5	SOT-89-5 PKG	SOT-89-5 Power Dissipation
DFN1820-6J	TBD	TBD

■MARKING RULE

①,② represents products series

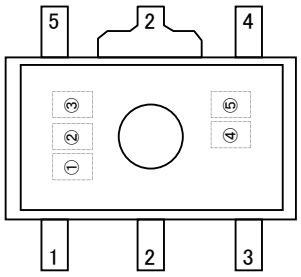
MARK		PRODUCT SERIES
①	②	
1	N	XD9704B75***-Q
	P	XD9705B75***-Q

③ represents type, Oscillation Frequency,

MARK	Oscillation Frequency	PRODUCT SERIES
A	2.2MHz	XD970*B75D**-Q

④ ⑤ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order. (G, I, J, O, Q, W excluded)
* No character inversion used.

SOT-89-5



1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions, excluding when specified for in-vehicle use or other uses.
   Do not use the product for in-vehicle use or other uses unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9.

TOREX SEMICONDUCTOR LTD.