LOW-NOISE, 20V, 200mA ULDO REGULATOR

Description

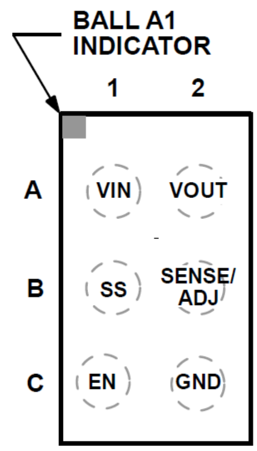
The AP7372 is a low-dropout linear regulator that operates from 2.7V to 20V and delivers 200mA output current. The wide input voltage LDO is suitable for the regulation of high-performance analog and mixed-signal circuits operating from 19.5V to 1.2V rails.

The AP7372 features high power supply rejection, low noise, and achieves excellent line and load transient response with a small 2.2µF ceramic output capacitor. The output noise is 8µVrms, independent of the output voltage for the fixed options of 5V or less.

The AP7372 has 1.8V, 2.5V, 3.3V and 5.0V fixed output voltage. Each fixed output voltage can be adjusted above the initial set point with an external feedback divider. This allows the AP7372 to provide an output voltage from 1.2V to VIIN – VDO with high PSRR and low noise.

A programmable soft-start with an external capacitor is available in the AP7372. The AP7372 is available in U-WLB1012-6 (Type A1) package.

Pin Assignments



U-WLB1012-6 (Type A1)

Features

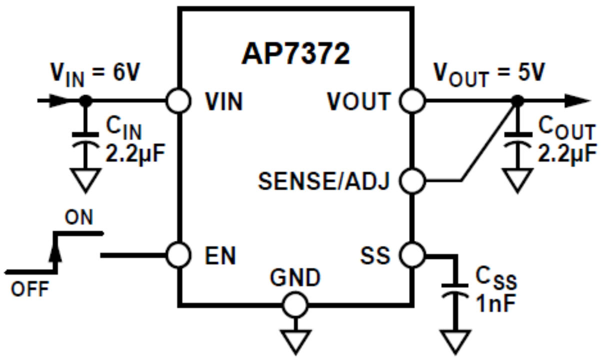
- Low Noise: 8µVrms Independent of Fixed Output Voltage
- High PSRR: 90dB @10kHz, 70dB @100kHz, 52dB @1MHz
- Input Voltage Range: 2.7V to 20V
- Maximum Output Current: 200mA
- High Output Voltage Accuracy: ±0.8%
- Accuracy over Line, Load, and Temperature ±1.8%, T_J = -40°C to +125°C
- Low Dropout Voltage: 120mV @I_{OUT} = 200mA (typ)
- User-Programmable Soft-Start
- Low Quiescent Current, I_{GND}: 66µA (typ)
- Low Shutdown Current:
  - 3.1µA @V_{IN} = 5V
  - 3.3µA @V_{IN} = 20V
- Stable with a 2.2µF Ceramic Output Capacitor
- Adjustable Output from 1.2V to VIN – VDO, output can be adjusted above initial set point
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.** **https://www.diodes.com/quality/product-definitions/**

Applications

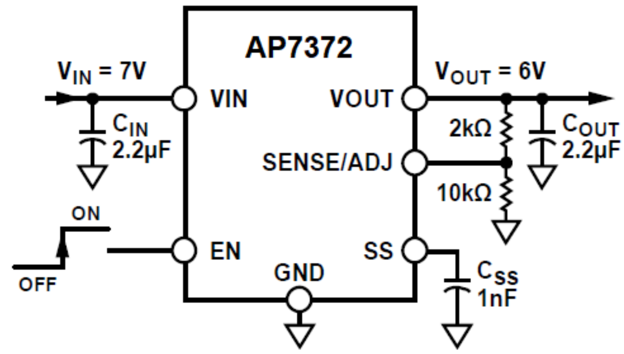
- Regulation to noise sensitive applications
  - ADC and DAC circuits, precision amplifiers, power for VCO V_{TUNE} controls
- Communications and infrastructures
- Medical and healthcares
- Industrials and instrumentation

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit



AP7372 with Fixed Output Voltage, 5V

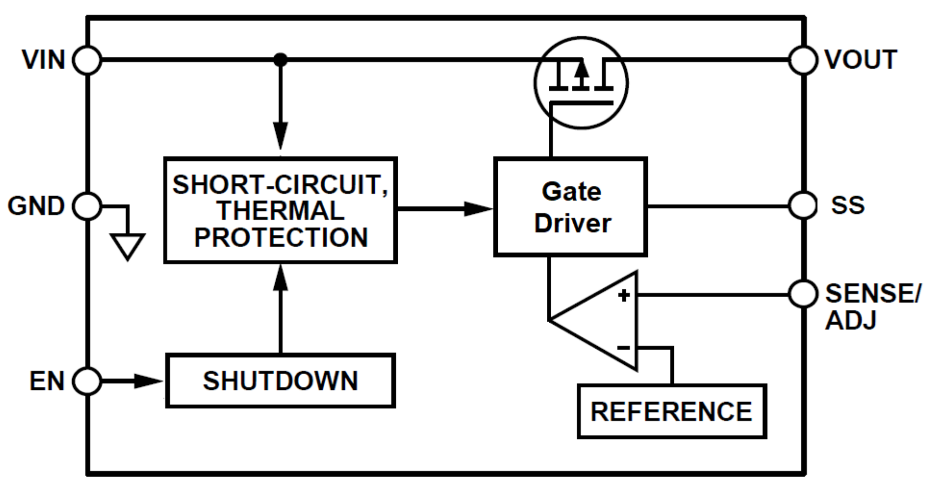


AP7372 with 5V Output Adjusted to 6V

Pin Descriptions

Pin Number	Pin Name	Function
A1	VIN	Input Voltage
B1	SS	Soft-Start. An external capacitor connected to this pin determines the soft-start time. Leave this pin open for a typical 340µs startup time. Do not ground this pin.
C1	EN	The enable pin controls the operation of the LDO. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
A2	VOUT	Regulated Output Voltage
B2	SENSE/ADJ	Sense Input (SENSE). Connect to load. Adjustable model (ADJ). The adjustable model has a fixed output set to 1.2V. The output can be set to a voltage higher than 1.2V by connecting an external resistor divider to the ADJ pin.
C2	GND	Ground

Functional Block Diagram



Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Input Voltage	-0.3 to 24	V
V_{OUT}	Regulated Output Voltage	-0.3 to V_{IN}	V
V_{EN}	Enable Pin Voltage	-0.3 to 26	V
$V_{SENSE/ADJ}$	Sense and Adjustable Voltage	-0.3 to 6	V
V_{SS}	Soft-Start Voltage	-0.3V to VIN or +6V (whichever is less)	V
I_{OUT}	Output Current	Internally limited	mA
T_{LEAD}	Lead Temperature (Soldering, 10sec)	+260	°C
T_J	Operating Junction Temperature	+150	°C
T_A	Operating Ambient Temperature	-40 to +85	°C
T_{STG}	Storage Temperature Range	-40 to +150	°C
HBM	ESD (Human Body Model)	2000	V
CDM	ESD (Change Device Model)	1000	V

Note: 4. a). Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
b). Ratings apply to ambient temperature at +25°C. The JEDEC STD.51 High-K board design used to derive this data was a 3inch x 3inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Input Voltage	2.7	20	V
V_{EN}	Enable Pin Voltage	0	20	V
V_{OUT}	Supply Output Voltage	1.2	V_{IN} - V_{DO}	V
I_{OUT}	Output Current	0	200	mA
T_J	Operating Junction Temperature	-40	+125	°C
C_{MIN} (Note 5)	Input and Output Minimum Capacitance	1.5	—	µF
$C_{OUT(MAX)}$	Output Maximum Capacitance	—	22	µF
R_{ESR}	Capacitor Effective Series Resistance (ESR)	0.001	0.3	Ω

Note: 5. The minimum input and output capacitance must be greater than 1.5µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, whereas Y5V and Z5U capacitors are not recommended for use with any LDO.

Package Thermal Information

Thermal Metric (Note 6)		U-WLB1012-6 (Type A1)	Unit
$R_{θJA}$	Junction-to-Ambient Thermal Resistance	163.76	°C/W
$R_{θJC(top)}$	Junction-to-Case (Top) Thermal Resistance	46.8	°C/W
$R_{θJB}$	Junction-to-Board Thermal Resistance	28.29	°C/W
$ψ_{JT}$	Junction-to-Top Characterization Parameter	2.84	°C/W
$ψ_{JB}$	Junction-to-Board Characterization Parameter	28.29	°C/W
$R_{θJC(bot)}$	Junction-to-Case (Bottom) Thermal Resistance	32.8	°C/W

Note: 6. Ratings apply to ambient temperature at +25°C. The JEDEC STD.51 High-K board design used to derive this data was a 3inch × 3inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.

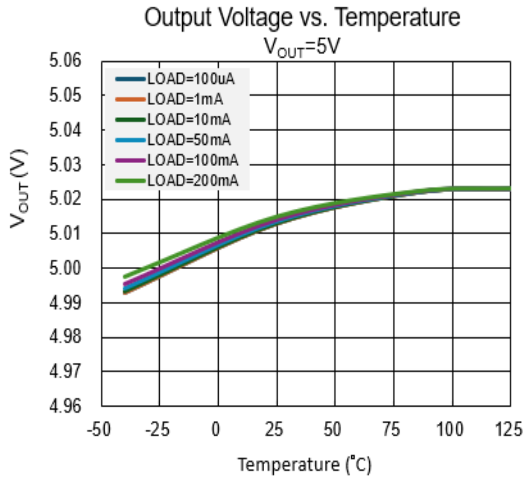
Electrical Characteristics

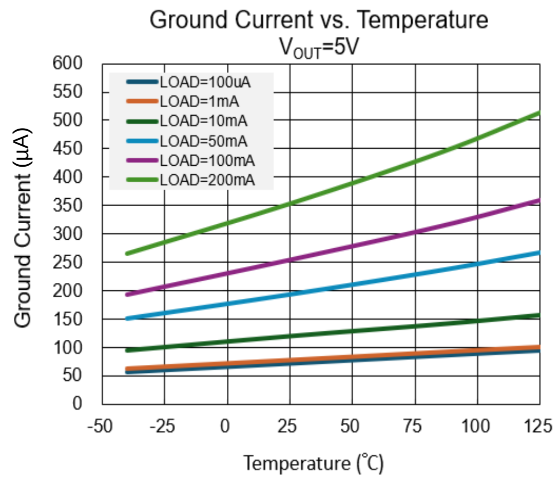
V_{IN} = V_{OUT} + 1V or 2.7V, whichever is greater, V_{OUT} = 5V, EN = V_{IN}, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 2.2µF, C_{SS} = 0pF, T_A = +25°C for typical specifications, T_J = -40°C to +125°C for minimum/maximum specifications, unless otherwise noted.

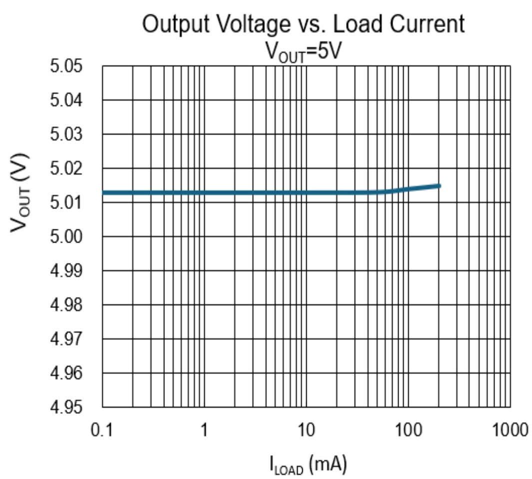
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	—	2.7	—	20	V
I_{LOAD_MAX}	Maximum Output Current	—	—	200	—	mA
I_{GND}	Ground Current	I_{OUT} = 0µA	—	66	110	µA
		I_{OUT} = 10mA	—	110	185	µA
		I_{OUT} = 200mA	—	280	500	µA
I_{SHDN}	Shutdown Current	EN = GND	—	3.1	—	µA
		EN = GND, V_{IN} = 20V	—	3.5	11	µA
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 10mA, T_J = +25°C	-0.8	—	0.8	%
		100µA < I_{OUT} < 200mA, V_{IN} = (V_{OUT} + 1V) to 20V	-1.8	—	1.8	%
$\triangle V_{OUT}/\triangle V_{IN}$	Line Regulation	V_{IN} = (V_{OUT} + 1V) to 20V	-0.01	—	0.01	%/V
$\triangle V_{OUT}/\triangle I_{OUT}$	Load Regulation	I_{OUT} = 100µA to 200mA	—	0.001	0.003	%/mA
$SENSE_{I\text{-}BIAS}$	Sense Input Bias Current	100µA < I_{OUT} < 200mA, V_{IN} = (V_{OUT} + 1V) to 20V	—	10	1000	nA
V_{DO}	Dropout Voltage	I_{OUT} = 10mA	—	60	100	mV
		I_{OUT} = 200mA	—	120	280	mV
$t_{STARTUP}$	Startup Time	V_{OUT} = 5V	—	340	—	µs
$SS_{I\text{-}SOURCE}$	Soft-Start Source Current	SS = GND	—	1	—	µA
I_{CL}	Output Current Limit	—	245	360	500	mA
T_{SSD}	Thermal Shutdown Threshold	T_J rising	—	+155	—	°C
$T_{SSD\text{-}HYS}$	Thermal Shutdown Hysteresis		—	+20	—	°C
V_{UVLO}	UVLO Threshold	V_{IN} rising	—	—	2.65	V
		V_{IN} falling	2.1	—	—	
		Hysteresis	—	0.24	—	
EN INPUT STANDBY						
$EN_{STBY\text{-}HIGH}$	EN Input Logic High	2.7V ≤ V_{IN} ≤ 20V	1.0	—	—	V
$EN_{STBY\text{-}LOW}$	EN Input Logic Low		—	—	0.4	V
$EN_{STBY\text{-}HYS}$	EN Input Logic Hysteresis		—	0.11	—	V
EN INPUT PRECISION						
EN_{HIGH}	EN Input Logic High	2.7V ≤ V_{IN} ≤ 20V	1.0	1.24	1.45	V
EN_{LOW}	EN Input Logic Low		0.9	1.13	1.3	V
EN_{HYS}	EN Input Logic Hysteresis		—	110	—	mV
$I_{EN\text{-}LKG}$	EN Input Leakage Current	EN = V_{IN} or GND	—	0.01	0.1	µA
$t_{EN\text{-}DLY}$	EN Input Delay Time	From EN rising from 0V to V_{IN} to 0.1 × V_{OUT}	—	140	—	µs
V_n	Output Noise Voltage	BW = 10Hz to 100kHz, all output voltage options	—	8	—	µVrms
PSRR	Power-Supply Rejection Ratio	f = 1MHz, V_{IN} = 7V, V_{OUT} = 5V	—	52	—	dB
		f = 100kHz, V_{IN} = 7V, V_{OUT} = 5V	—	70	—	dB
		f = 10kHz, V_{IN} = 7V, V_{OUT} = 5V	—	90	—	dB

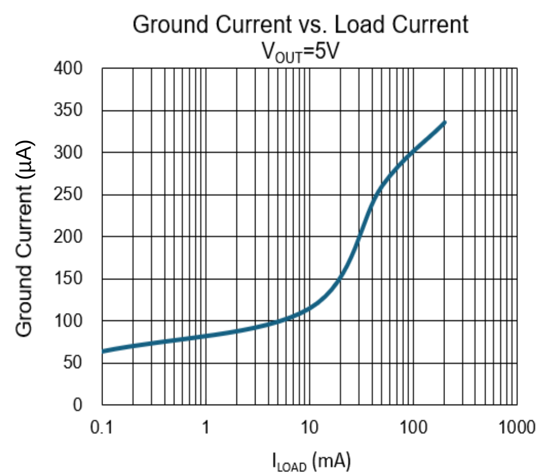
Performance Characteristics

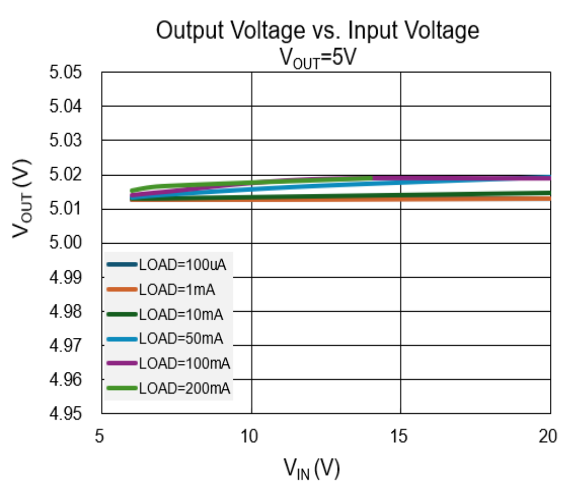
$V_{IN} = V_{OUT} + 1V$ or 2.7V, whichever is greater, $V_{OUT} = 5V$, $I_{LOAD} = 10mA$, $C_{IN} = C_{OUT} = 2.2\mu F$, $T_A = +25°C$, unless otherwise noted.

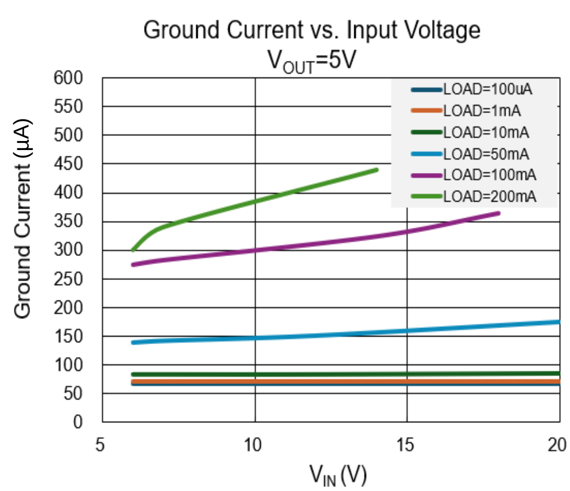












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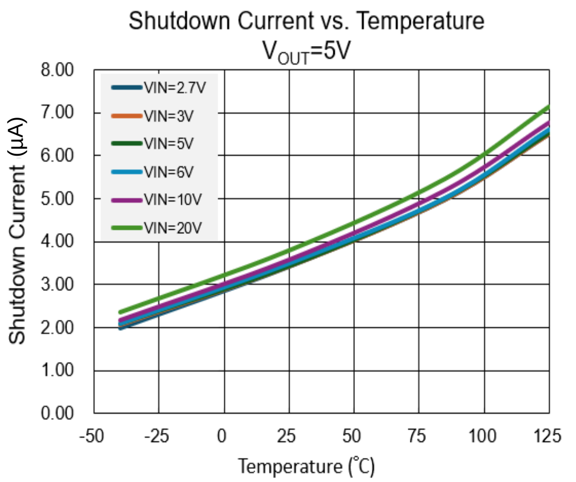

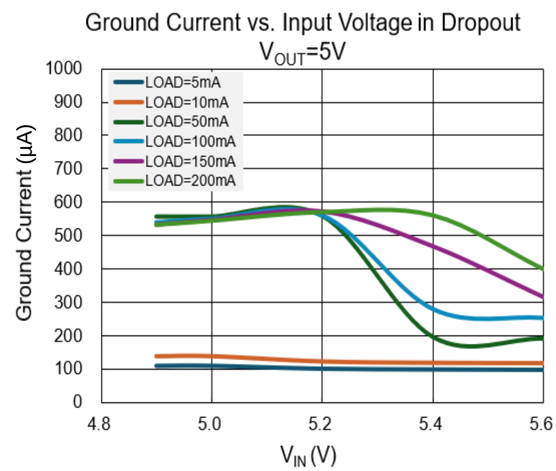

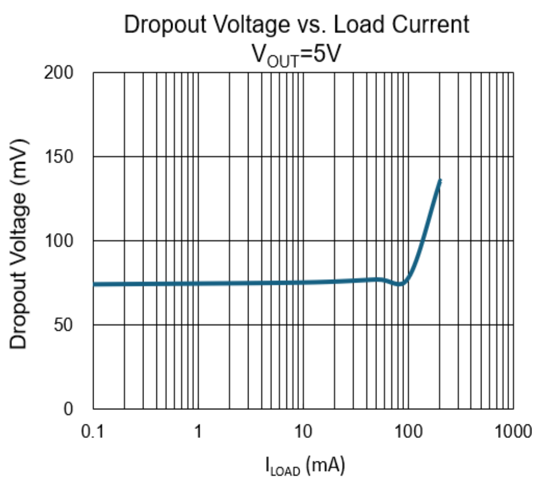

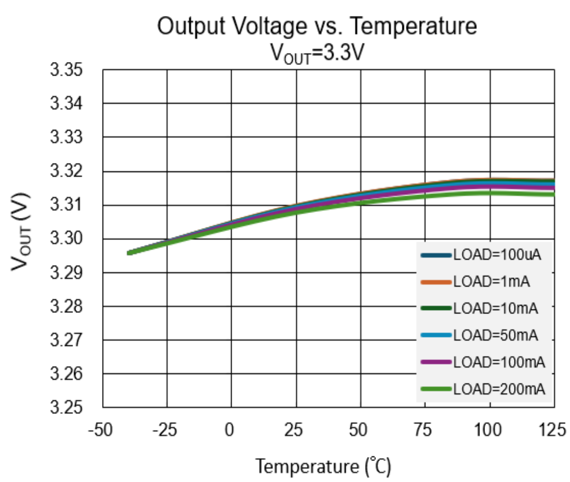

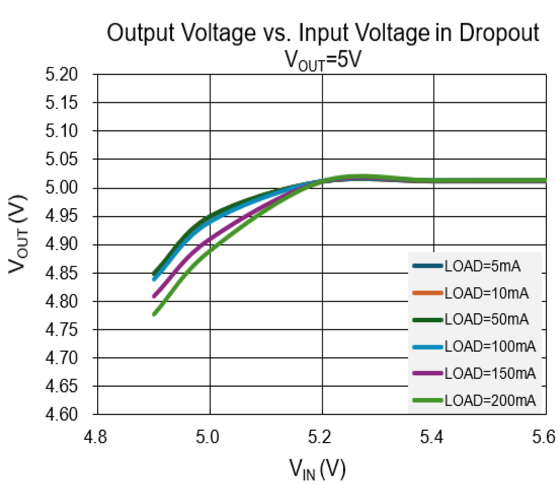

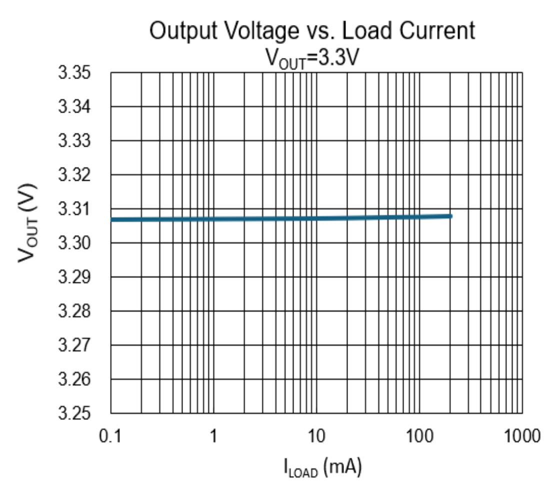

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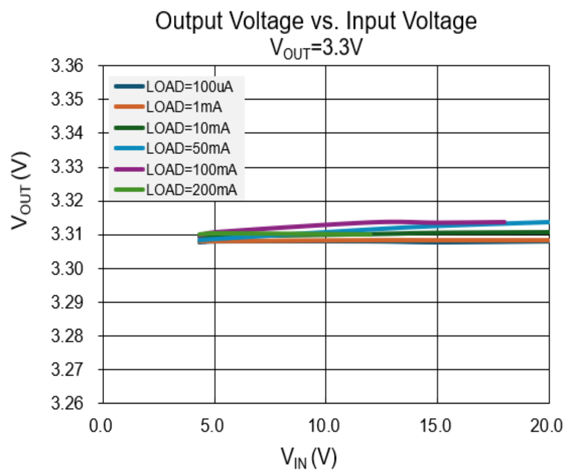

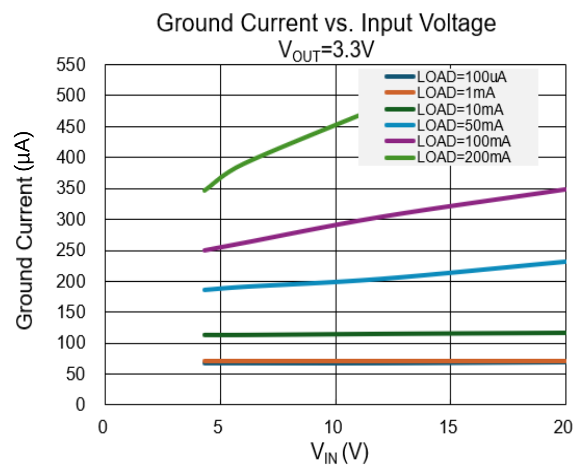

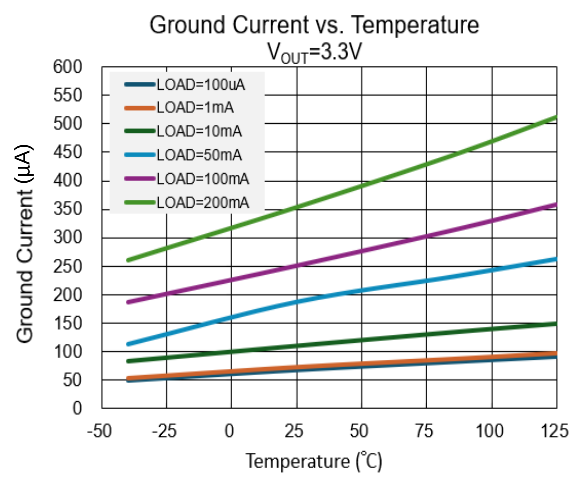

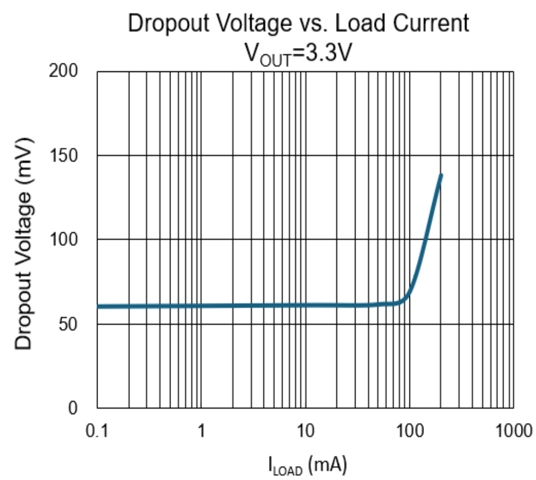

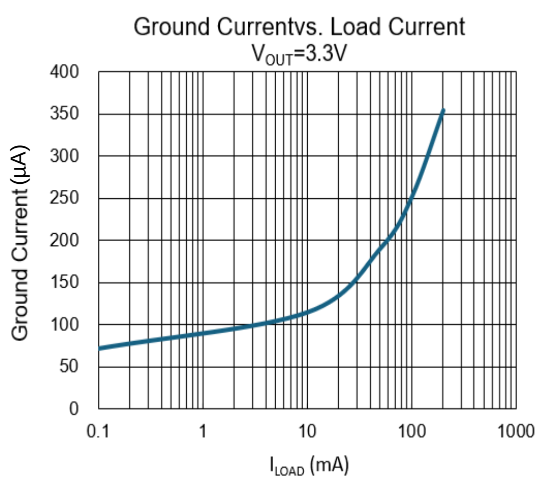

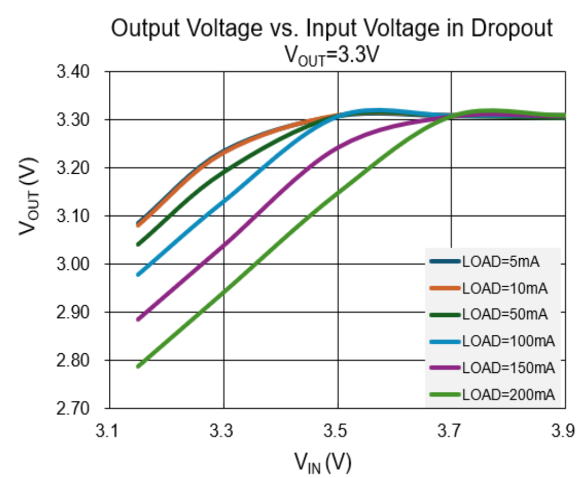

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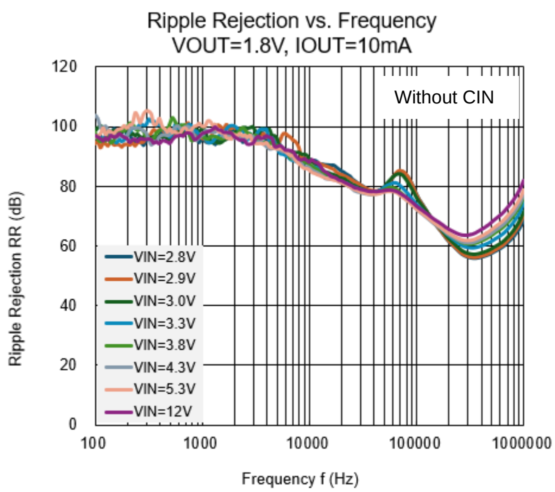
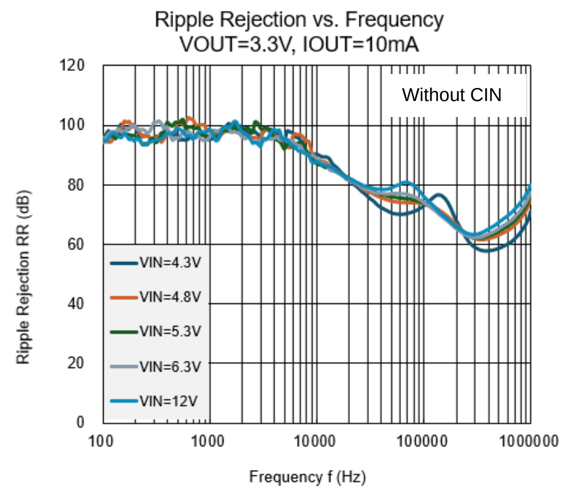
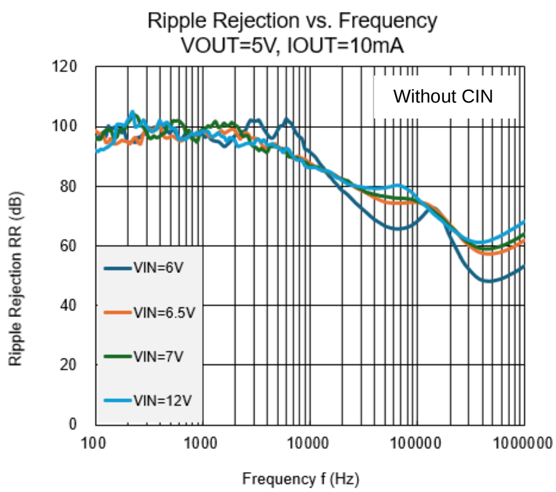
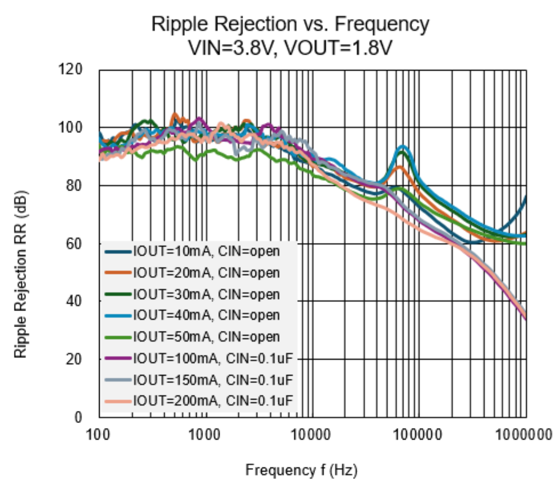
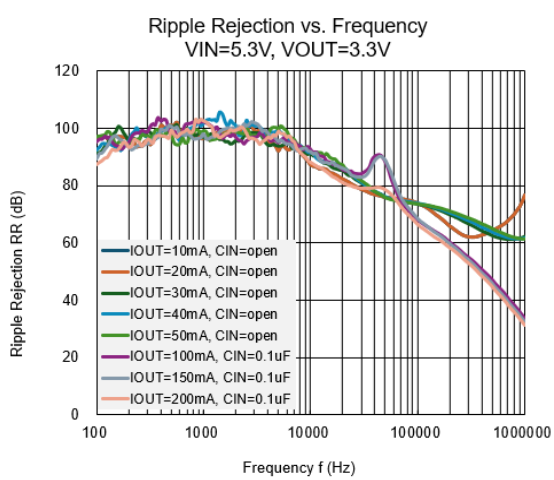
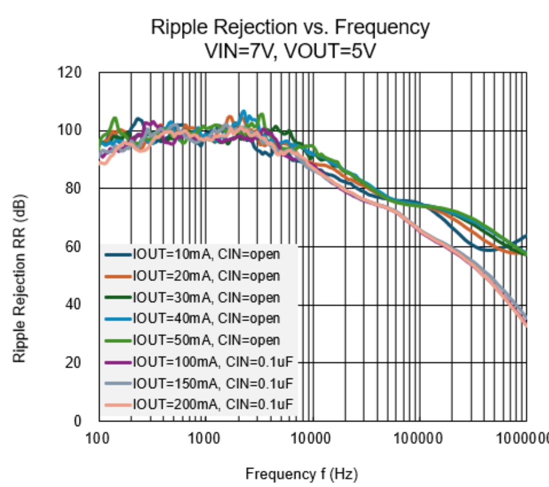






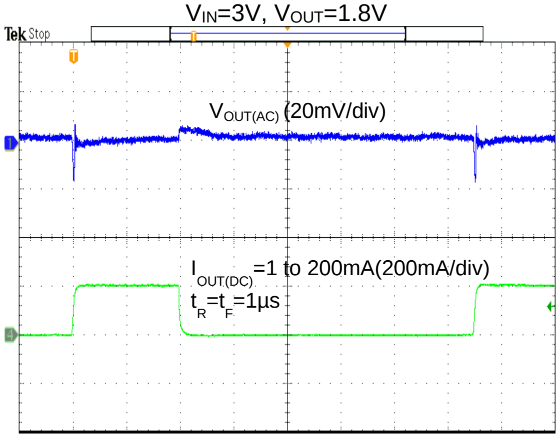




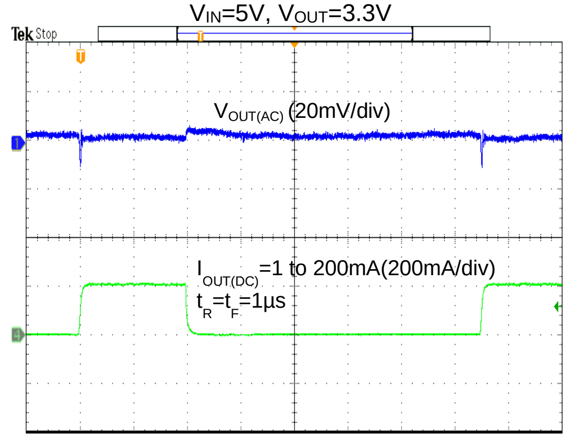


Performance Characteristics (continued)

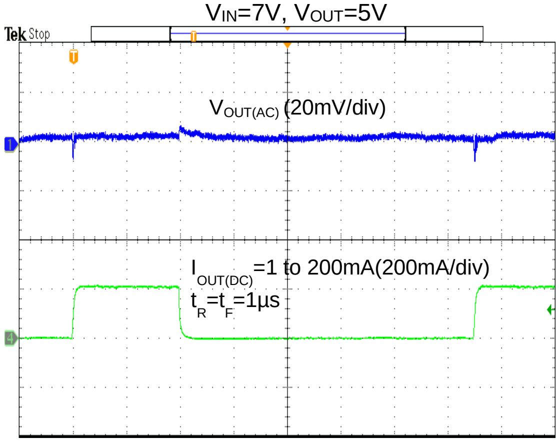
Load Transient Response
V_{IN}=3V, V_{OUT}=1.8V



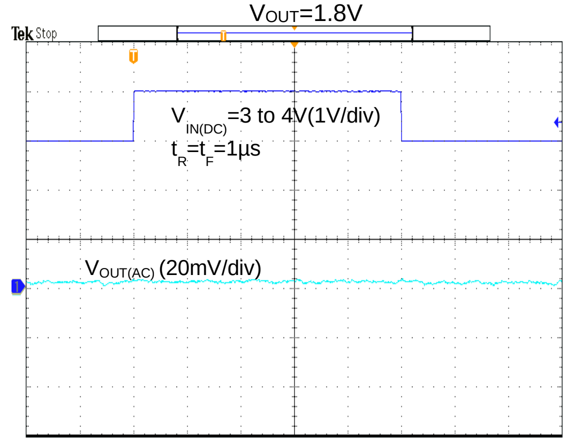
Load Transient Response
V_{IN}=5V, V_{OUT}=3.3V



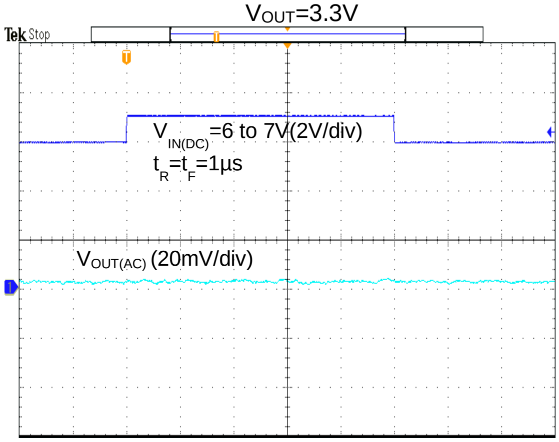
Load Transient Response
V_{IN}=7V, V_{OUT}=5V



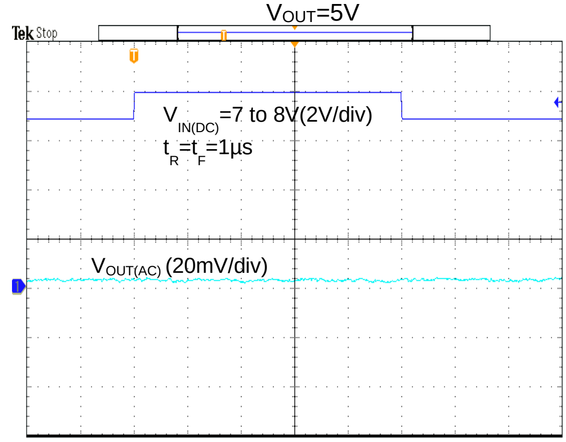
Line Transient Response
V_{OUT}=1.8V



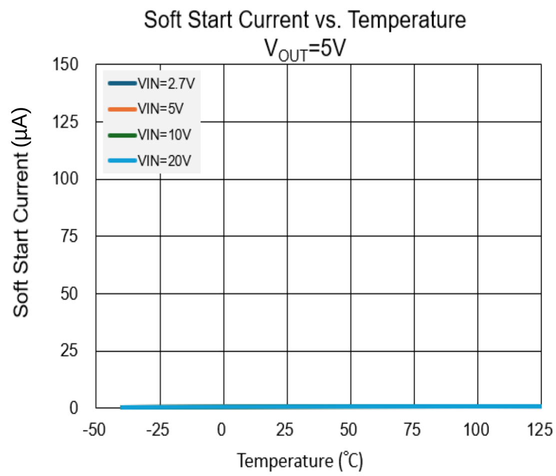
Line Transient Response
V_{OUT}=3.3V

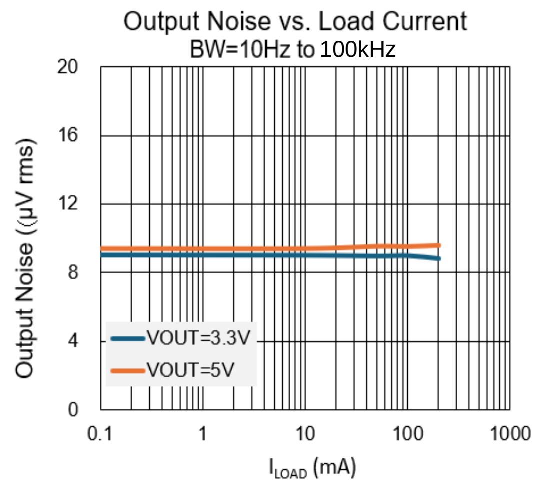


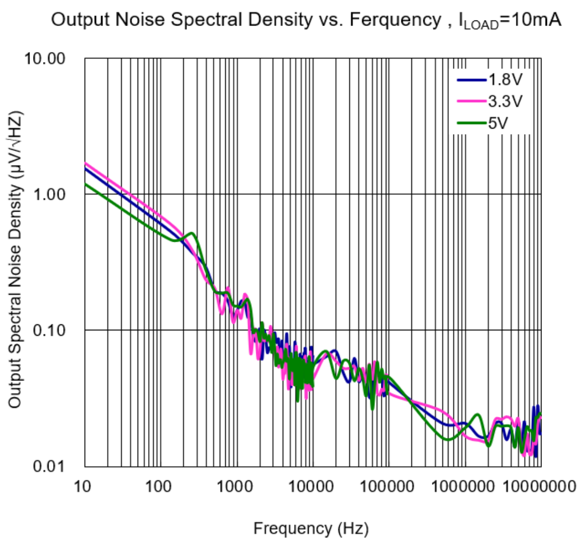
Line Transient Response
V_{OUT}=5V

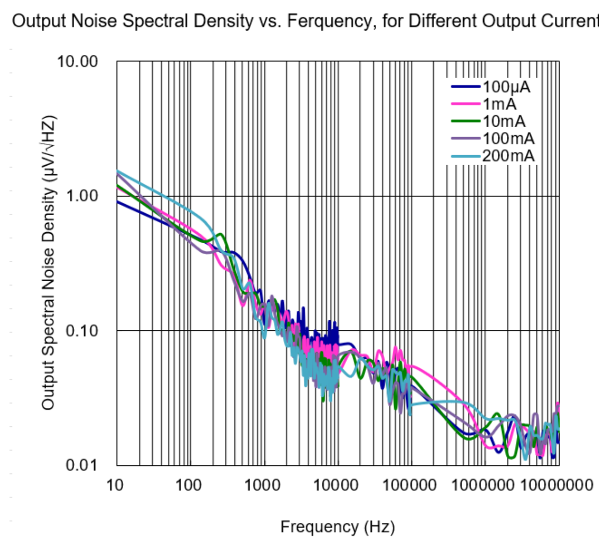


Performance Characteristics (continued)









Application Information

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is 2.2μF. A ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place the output capacitor as close as possible to VOUT and GND pins.

Input Capacitor

A 2.2μF ceramic capacitor is recommended to connect VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to ensure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Current-Limit and Short-Circuit Protection

When output current at VOUT pin is higher than the current-limit threshold or the VOUT pin directly shorts to GND, current-limit protection will be triggered and clamp the output current at a pre-designed level to prevent overcurrent and thermal damage.

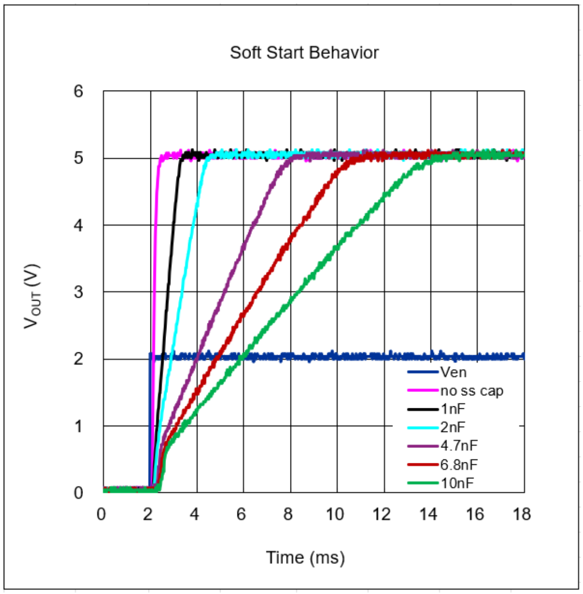
Soft-Start

The AP7372 uses an internal soft-start (SS pin open) to limit the inrush current when the output is enabled. The startup time for the 5V option is approximately 340µs from the time the EN active threshold is crossed to when the output reaches 90% of the final value.

An external capacitor connected to the SS pin determines the soft-start time. This SS pin can be left open for a typical 340µs startup time. Do not ground this pin. When an external soft-start capacitor (CSS) is used, the soft-start time is determined by the following equation:

$$SS_{TIME}\,(\text{sec}) = t_{START\text{-}UP\ at\ 0\ pF} + (0.8 \times C_{SS})/I_{ss}$$

Where: $t_{START\text{-}UP}$ *at 0pF* is the startup time at C_{SS} = 0pF (typically 340µs).
C_{SS} is the soft-start capacitor (F).
I_{SS} is the soft start current (typically 1µA).



Application Information (continued)

Thermal Protection

The AP7372 has internal thermal sense and protection circuits. When excessive power dissipation happens on the device, such as short circuit at the output pin or very heavy load current with a large voltage drop across the device, the internal thermal protection circuit will be triggered, shutting down the power MOSFET to prevent the LDO from damage. As soon as the excessive thermal condition is removed and the temperature of the device drops down, the thermal protection circuit will release the control of the power MOSFET, and the LDO device returns to normal operation.

Layout Considerations

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from V_{IN} to V_{OUT}, and load circuit.

Adjustable Output Voltage

The AP7372 is available in 4 fixed output voltage options, ranging from 1.8V to 5.0V. The AP7372 architecture allows any fixed output voltage to be set to a higher voltage with an external voltage divider. For example, a fixed 5V output can be set to a 6V output according to the following equation: VOUT = 5V(1 + R1/R2) where R1 and R2 are the resistors in the output voltage divider shown in Figure 1.

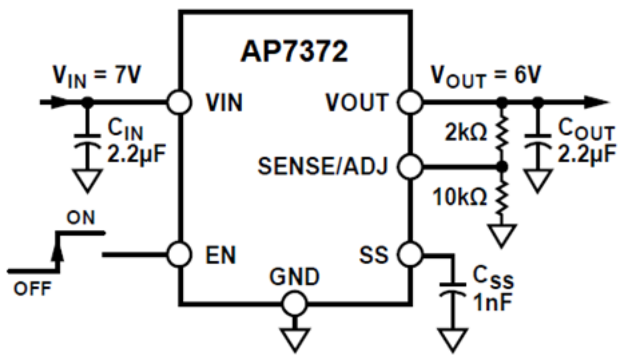


Figure 1. Typical Adjustable Output Voltage Application Schematic

Ordering Information (Note 7)

AP7372 - XX XXXX - X

Output Voltage	Package	Packing
12 : 1.2V(ADJ) 18 : 1.8V 25 : 2.5V 33 : 3.3V 50 : 5.0V	CBA6 : U-WLB1012-6 (Type A1)	7: Tape & Reel

Orderable Part Number	Package Code	Package	Packing	
			Qty.	Carrier
AP7372-XXCBA6-X	CBA6	U-WLB1012-6 (Type A1)	3,000	7” Tape and Reel

Note: 7. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

U-WLB1012-6 (Type A1)

(Top View)

XX
Y W

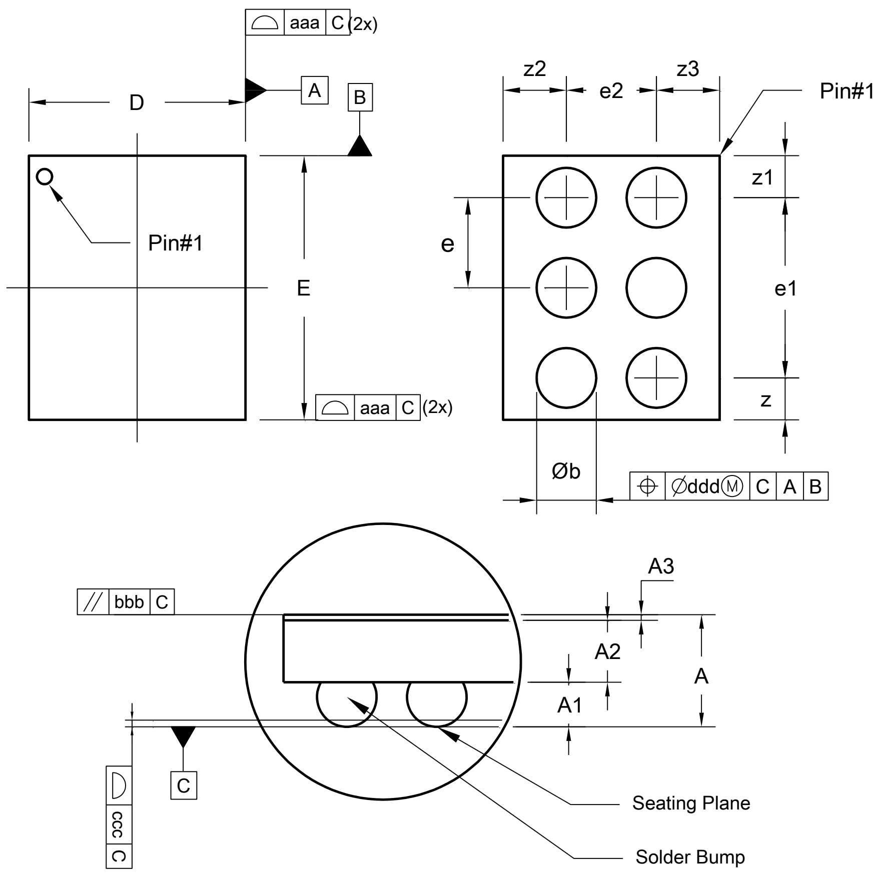
XX : Identification Code
Y : Year : 0 to 9 (ex: 5 = 2025)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents
week 52 and 53

Orderable Part Number	Package	Identification Code
AP7372-12CBA6-7	U-WLB1012-6 (Type A1)	C2
AP7372-18CBA6-7	U-WLB1012-6 (Type A1)	C3
AP7372-25CBA6-7	U-WLB1012-6 (Type A1)	C4
AP7372-33CBA6-7	U-WLB1012-6 (Type A1)	C5
AP7372-50CBA6-7	U-WLB1012-6 (Type A1)	C6

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1012-6 (Type A1)

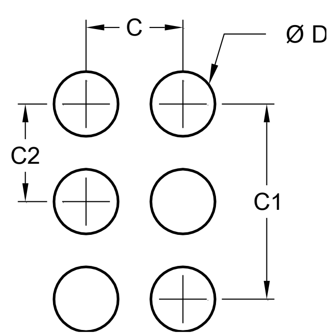


U-WLB1012-6 (Type A1)			
Dim	**Min**	**Max**	**Typ**
A	0.4502	0.5458	0.4980
A1	0.1782	0.2178	0.1980
A2	0.2500	0.3000	0.2750
A3	0.0220	0.0280	0.0250
b	0.2253	0.3048	0.2650
D	0.9350	0.9900	0.9625
E	1.1450	1.200	1.1725
e	--	--	0.4000
e1	--	--	0.8000
e2	--	--	0.4000
z	--	--	0.1863
z1	--	--	0.1863
z2	--	--	0.2813
z3	--	--	0.2813
aaa	--	--	0.0275
bbb	--	--	0.0600
ccc	--	--	0.0300
ddd	--	--	0.1500
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-WLB1012-6 (Type A1)



Dimensions	Value (in mm)
C	0.400
C1	0.800
C2	0.400
D	0.316

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - SnAgCu. Solderable per MIL-STD-202 Method 208 (e1)
- Weight: 0.0012 grams (Approximate)

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