# LOW IQ REVERSE BATTERY POLARITY AND OVERVOLTAGE PROTECTION CONTROLLER

## Description

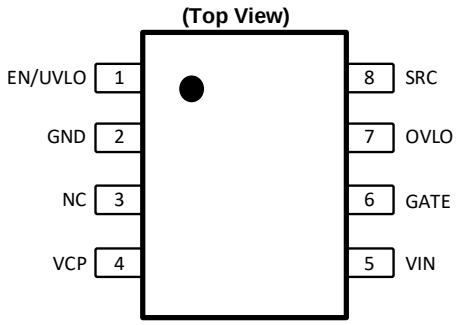
The AP74502Q, AP74502HQ is an automotive AEC-Q100 qualified reverse battery polarity and overvoltage protection controller, which operates with 2 of external N-channel MOSFETs.

The AP74502Q, AP74502HQ is for input protection of 12V/24V/48V automotive systems. The input voltage support as low as 3.2V is particularly for severe cold crank requirements in automotive systems and up to 75V.

The AP74502Q, AP74502HQ controller provides a charge pump gate drive for an external Back to Back N-channel MOSFETs with the enable pin low, the controller is off and draws approximately 1μA of current.

The AP74502Q, AP74502HQ is available in SOT28 package.

## Pin Assignments




**SOT28**

## Applications

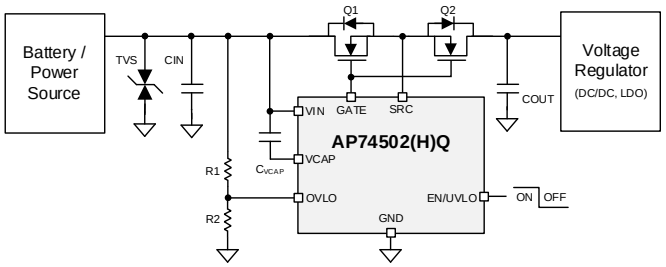
- Automotive body control units
- Automotive infotainment systems – head units, telematics control units
- Automotive ADAS systems – cameras
- Power of industrial automation such as PLC
- Enterprise power supplies

## Features

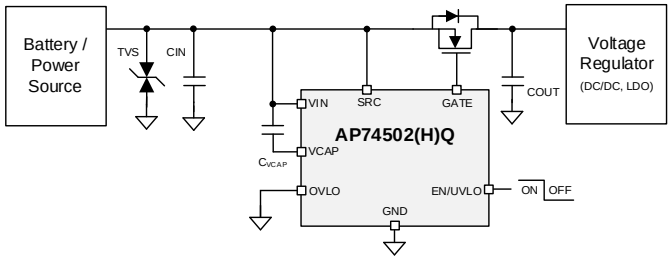
- Input Voltage Ranges from 3.2V to 80V (3.9V Start-Up)
- -80V Reverse Battery Voltage
- Charge Pump for External N-ch Power MOSFETs
- Drives External Back to Back N-ch MOSFETs
- Gate Driver Strength Option
- AP74502Q: 60μA Peak Gate Source
- AP74502HQ: 11mA Peak Gate Source
- Low Shutdown Current of 0.9μA When Disabled
- Low Quiescent Current of 62μA When Enabled
- 2.3A Peak Gate Turn-Off Current
- ESD Protection: 2kV of HBM and 750V of CDM
- AEC-Q100 Qualification Compliance with Device Temperature Grade 1 (-40°C to +125°C Ambient Operating Temperature Range)
- 8-Pin SOT28 Package
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP74502Q, AP74502HQ are suitable for automotive applications requiring specific change control; these parts are AEC-Q100 qualified, PPAP capable, and manufactured in IATF16949 certified facilities.**
  **https://www.diodes.com/quality/product-definitions/**

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

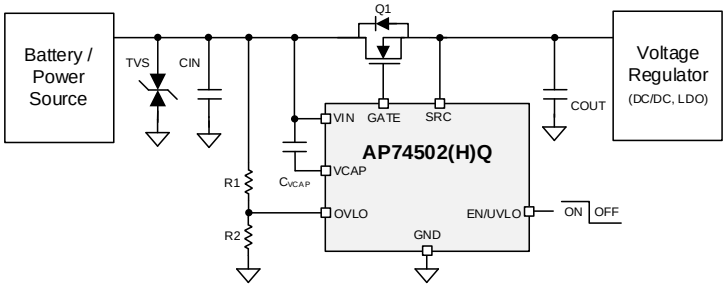
## Typical Applications Circuit




**Reverse Polarity/Overvoltage Protection with Load Disconnect (Dual FETs)**




**Reverse Polarity Protection (Single FET)**

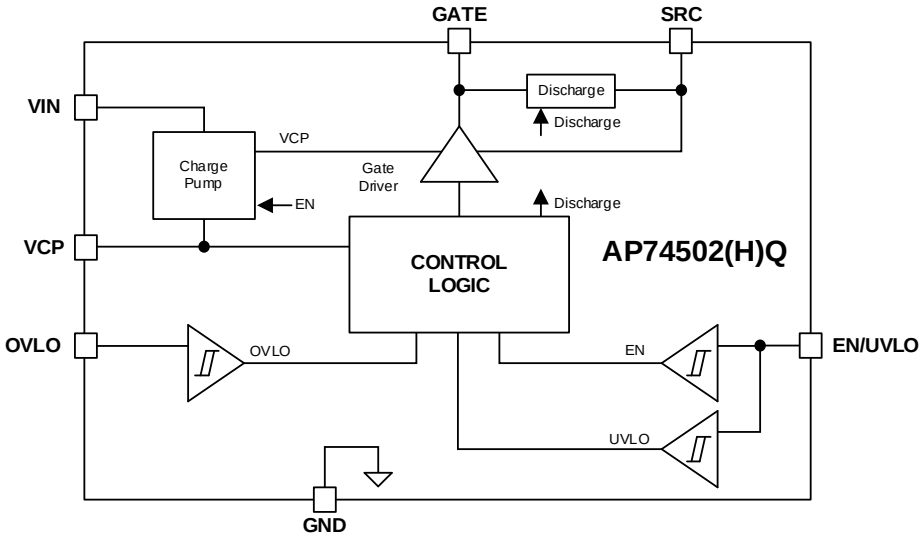



**Load Switch Controller with Overvotlage Protection (Single FET)**

## Pin Descriptions

| Pin Name | Pin Number | Function |
|---|---|---|
| EN/UVLO | 1 | EN/ UVLO Control pin. Enable/ Shutdown can be controlled IO control from processor. This pin also support UVLO feature with external resistor divider. |
| GND | 2 | Ground Pin |
| NC | 3 | No Connection |
| VCAP | 4 | Charge pump output pin. Connect external Capacitor (minimum 0.1μF) between VIN and VCAP. |
| VIN | 5 | Input power supply to the device. Connect CIN (> 0.1μF) between VIN and GND. |
| GATE | 6 | GATE driver output. Connect to the gate of external NMOS FET. |
| OVLO | 7 | OVLO input pin. Connect external resistor divider to adjust OVLO threshold. Connect to GND if OVLO feature is not used. |
| SRC | 8 | Power input for gate driver. Connect to the source of external NMOS FET. |

## Functional Block Diagram



## Absolute Maximum Ratings (@$T_A$ = +25°C, unless otherwise specified.) (Note 4)

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| ESD HBM | Human Body ESD Protection | ±2 | kV |
| ESD CDM | Charged Device Model ESD Protection | ±750 | V |
| VIN to GND | Input Voltage at VIN | -80 to +80 | V |
| EN/UVLO, OVLO to GND | $V_{VIN}$ > 0V | -0.3 to +80 | V |
| | $V_{VIN}$ ≤ 0V | $V_{VIN}$ to ($V_{VIN}$ +80) | V |
| SRC to GND | $V_{VIN}$ > 0V | -(80-$V_{VIN}$) to $V_{VIN}$ | V |
| | $V_{VIN}$ ≤ 0V | $V_{VIN}$ +0.3 | V |
| GATE to SRC | — | 0 to 15 | V |
| VCAP to VIN | — | -0.3 to 15 | V |
| $T_{J(MAX)}$ | Maximum Operating Junction Temperature | -40 to +150 | °C |
| $T_{STG}$ | Storage Temperature | -40 to +150 | °C |

Note: 4. Stresses greater than the *'Absolute Maximum Ratings'* specified above can cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability can be affected by exposure to absolute maximum rating conditions for extended periods of time.

## Package Thermal Information (Notes 5 & 6)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-Ambient Thermal Resistance | 176.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-Case (Top) Thermal Resistance | 122.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-Board Thermal Resistance | 46.0 | °C/W |
| $\psi_{JT}$ | Junction-to-Top Characterization Parameter | 10.1 | °C/W |
| $\psi_{JB}$ | Junction-to-Board Characterization Parameter | 44.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-Case (Bottom) Thermal Resistance | 50.0 | °C/W |

Notes: 5. $R_{\theta JA}$ and $R_{\theta JC}$ are measured at $T_A$ = +25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.
6. Device mounted on the JEDEC High-K 2S2P board.

## Recommended Operating Conditions (@$T_A$ = +25°C, unless otherwise specified.)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| VIN, EN/UVLO, OVLO, SRC to GND | Input Voltage at VIN, EN/UVLO, OVLO, SRC | -75 | +75 | V |
| VIN Capacitance | Input Capacitor at VIN (Note 7) | 0.1 | — | µF |
| VIN to VCAP Capacitance | Charge Pump Capacitor (Note 7) | 0.1 | — | µF |
| External MOSFET VGS Max | Gate to SRC (Note 7) | 15 | — | V |
| $T_J$ | Operating Junction Temperature Range | -40 | +150 | °C |

Note: 7. Refer to the typical application circuit.

## Electrical Characteristics

($T_J$ = -40°C to +125°C, $V_{IN}$ = 12V, $C_{VCAP}$ = 0.1µF, $V_{EN}$ = 3.3V, typical values are at $T_J$ = +25°C, unless otherwise specified.)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **VIN Supply** | | | | | | | |
| $V_{VIN}$ | Operating Input Voltage | — | | 4 | — | 75 | V |
| $V_{VIN\_POR\_RISING}$ | VIN UVLO Rising Threshold | — | | — | — | 3.9 | V |
| $V_{VIN\_POR\_FALLING}$ | VIN UVLO Falling Threshold | — | | 2.2 | 2.8 | 3.1 | V |
| $V_{VIN\_POR\_HYS}$ | VIN UVLO Hysteresis | — | | 0.44 | — | 0.67 | V |
| $I_{SHDN}$ | Shutdown Supply Current | $V_{EN\_UVLO}$ = 0V | | — | 0.9 | 1.5 | µA |
| $I_Q$ | Operating Quiescent Current | $V_{EN\_UVLO}$ = High | | — | 62 | 84 | µA |
| $I_{REV}$ | Leakage Current During Reverse Polarity Condition | 0V < $V_{VIN}$ ≤ -65V | | — | 140 | 200 | µA |
| **EN/UVLO Input** | | | | | | | |
| $V_{EN\_UVLO\_RISING}$ | EN/UVLO Rising Threshold | — | | 1.16 | 1.24 | 1.32 | V |
| $V_{EN\_UVLO\_FALLING}$ | EN/UVLO Falling Threshold | — | | 1.027 | 1.14 | 1.235 | V |
| $V_{EN\_UVLO\_HYS}$ | EN/UVLO Hysteresis | — | | 38 | 90 | 132 | mV |
| $V_{ENF}$ | EN Threshold Voltage for $I_{SHDN}$ | — | | 0.32 | 0.64 | 0.94 | V |
| $I_{EN}$ | EN/UVLO Sink Current | — | | — | 3 | 5 | µA |
| **GATE Drive** | | | | | | | |
| $I_{GATE\_SOURCE}$ | Peak Source Current | $V_{GATE}$ – $V_{SRC}$ = 5.0V | AP74502Q | 40 | 60 | 77 | µA |
| | | | AP74502HQ | 3 | 11 | — | mA |
| $I_{GATE\_SINK}$ | Peak Sink Current | EN/UVLO = High to Low, $V_{GATE}$ – $V_{SRC}$ = 5.0V | | — | 2370 | — | mA |
| $R_{DS\_ON}$ | GATE Discharge Switch $R_{DS\_ON}$ | EN/UVLO = High to Low $V_{GATE}$ – $V_{SRC}$ = 100mV | | 0.4 | — | 2 | Ω |
| **Charge Pump** | | | | | | | |
| $V_{VCAP}$ – $V_{SRC}$ | Charge Pump Voltage at $V_{SRC}$ = 3.2V | $I_{VCAP}$ ≤ 30µA | | 8 | — | — | V |
| | Charge Pump Turn-On Voltage | — | | 10.3 | 11.6 | 13 | V |
| | Charge Pump Turn-Off Voltage | — | | 11 | 12.4 | 13.9 | V |
| | Charge Pump Turn-On/Off Hysteresis | — | | 0.45 | 0.8 | 1.6 | V |
| $I_{VCAP\_SOURCE}$ | Charge Pump Source Current | $V_{VCAP}$ – $V_{SRC}$ = 7V | | 162 | 250 | 600 | µA |
| $I_{VCAP\_SINK}$ | Charge Pump Sink Current | $V_{VCAP}$ – $V_{SRC}$ = 14V | | — | 5 | 10 | µA |
| $V_{VCAP\_UVLO\_RISING}$ | $V_{VCAP}$ – $V_{SRC}$ UVLO Rising Threshold | — | | 5.7 | 6.5 | 7.5 | V |
| $V_{VCAP\_UVLO\_FALLING}$ | $V_{VCAP}$ – $V_{SRC}$ UVLO Falling Threshold | — | | 5.05 | 5.4 | 6.5 | V |
| **OVERVOLTAGE PROTECTION** | | | | | | | |
| $V_{OV\_RISING}$ | Overvoltage Input Rising Threshold | — | | 1.165 | 1.25 | 1.333 | V |
| $V_{OV\_FALLING}$ | Overvoltage Input Falling Threshold | — | | 1.063 | 1.143 | 1.222 | V |
| $V_{OV\_HYS}$ | Overvoltage Hysteresis | — | | — | 100 | — | mV |
| $I_{OV}$ | Overvoltage Input Leakage Current | — | | 12 | 50 | 110 | nA |

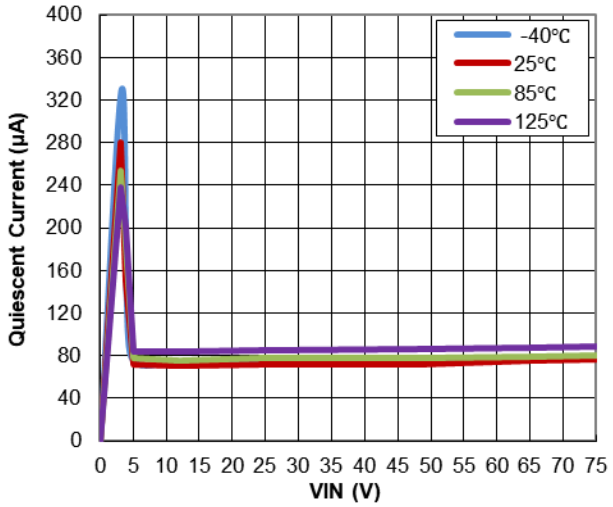
## Switching Characteristics ($T_J$ = -40°C to +125°C, $V_{IN}$ = 12V, $C_{VCAP}$ = 0.1µF, $V_{EN}$ = 3.3V, typical values are at $T_J$ = +25°C, unless otherwise specified.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Switching Characteristics** | | | | | | |
| $t_{EN\_DELAY}$ | Delay from Enable Switching High to Gate Turn On | $V_{VCP}$ > $V_{VCP\_UVLO}$, $V_{EN/UVLO}$ Step from 0V to > $V_{EN\_UVLORISING}$, $V_{GATE-SRC}$ > 5V, $C_{GATE-SRC}$ = 4.7nF | — | 75 | 110 | µs |
| $t_{UVLO\_OFF\_GATE}$ | Gate Turn-Off Delay by EN/UVLO | $V_{EN/UVLO}$ falling to $V_{GATE\_SRC}$ < 1V, $C_{GATE-SRC}$ = 4.7nF | — | 2 | — | µs |
| $t_{OVP\_OFF\_GATE}$ | Gate Turn-Off Delay by $V_{OV}$ Rising > $V_{OV\_RISING}$ (Note 8) | $V_{OV}$ Rising > $V_{OV\_RISINNG}$ to $V_{GATE-SRC}$ < 1V, $C_{GATE-SRC}$ = 4.7nF | — | 0.6 | 1 | µs |
| $t_{OVP\_ON\_GATE}$ | Gate Turn-On Delay by $V_{OV}$ Falling < $V_{OV\_FALLING}$ (Note 8) | $V_{OV}$ Falling < $V_{OV\_FALLING}$ to $V_{GATE-SRC}$ > 5V, $C_{GATE-SRC}$ = 4.7nF | — | 7 | 10 | µs |

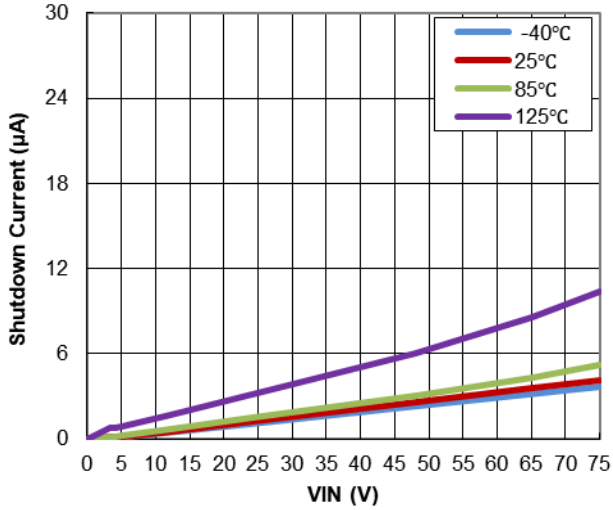
Note: 8. Parameter guaranteed by Bench characterization.

## Typical Performance Characteristics ($V_{IN}$ = 12V, $V_{EN}$ = 3.3V, $C_{VCAP}$ = 0.1µF, $T_J$ = +25°C, unless otherwise specified.)

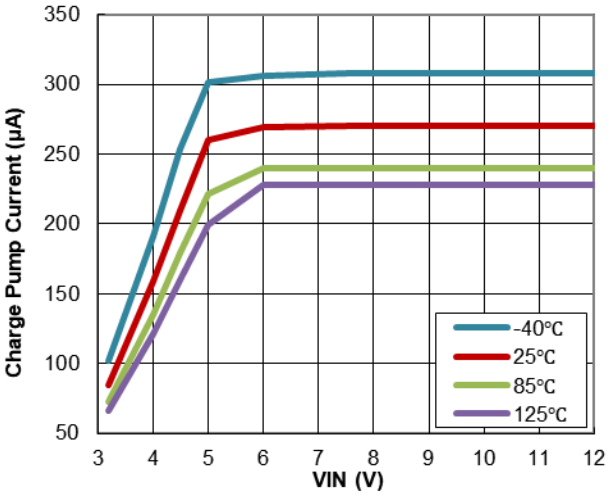
**Shutdown Supply Current vs Supply Voltage**



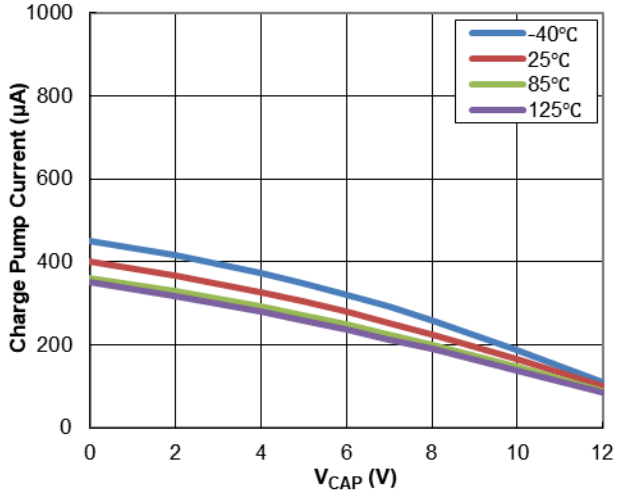

**Operating Quiescent Current vs Supply Voltage**



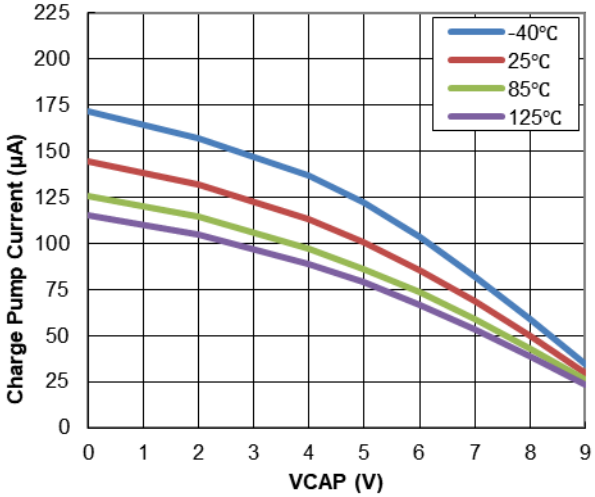

**Charge Pump Current vs Supply Voltage at VCAP = 6V**



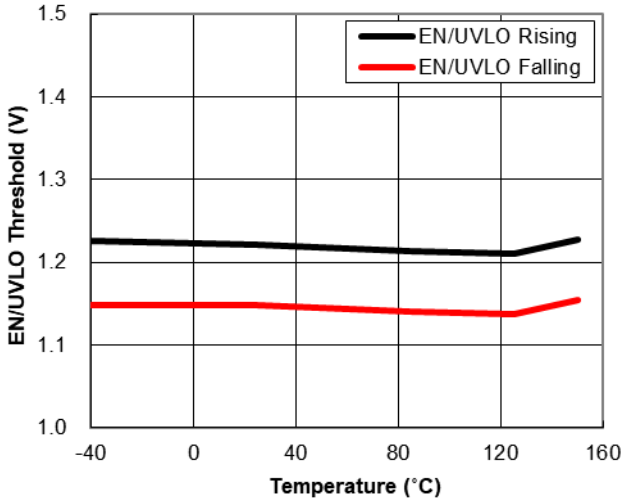

**Charge Pump V-I Characteristics at VIN > = 12V**




**Charge Pump V-I Characteristics at VIN = 3.2V**

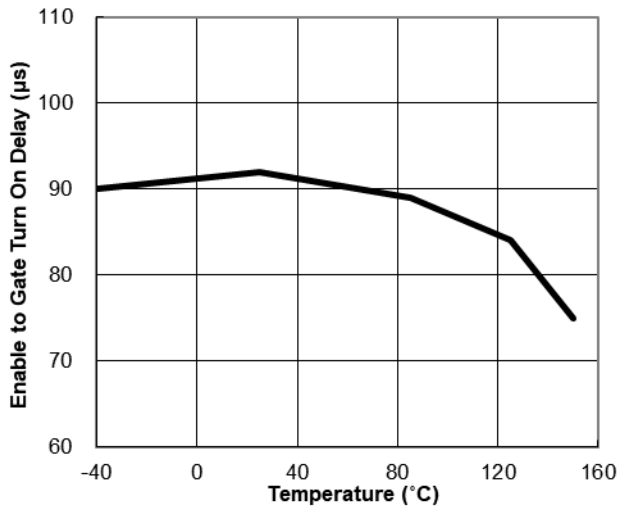



**EN/UVLO Rising and Falling threshold vs Temperature**

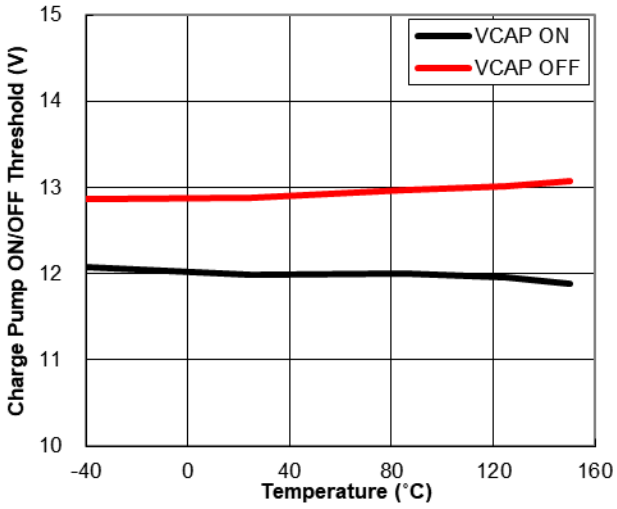


## Typical Performance Characteristics ($V_{IN}$ = 12V, $V_{EN}$ = 3.3V, $C_{VCAP}$ = 0.1µF, $T_J$ = +25°C, unless otherwise specified.)
(continued)

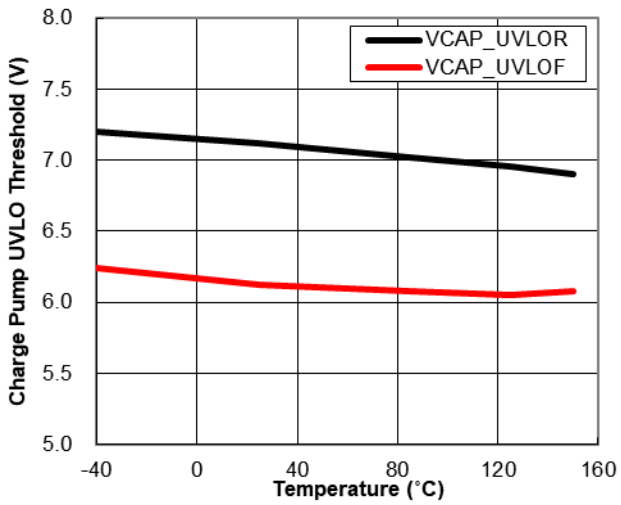
**Enable to Gate Delay vs Temperature (AP74502HQ)**



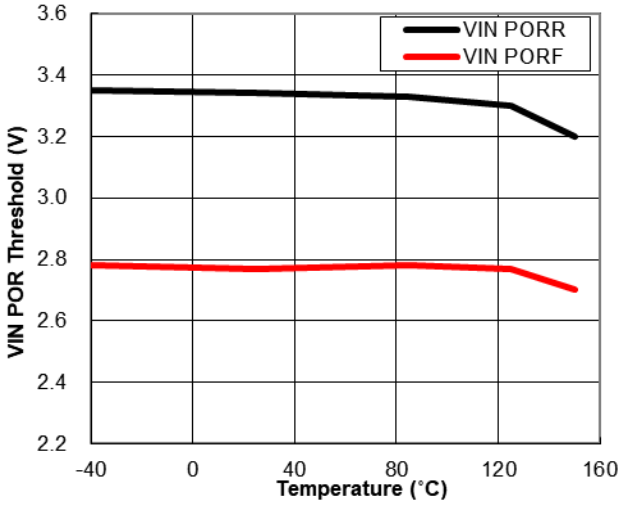

**Charge Pump ON and OFF Threshold vs Temperature**



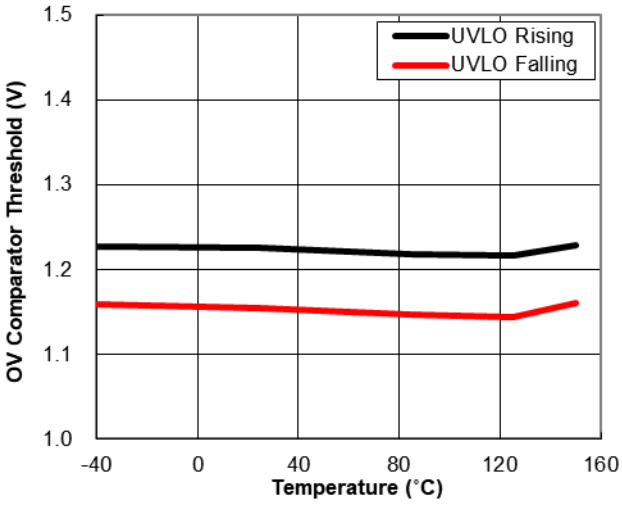

**Charge Pump UVLO Threshold vs Temperature**



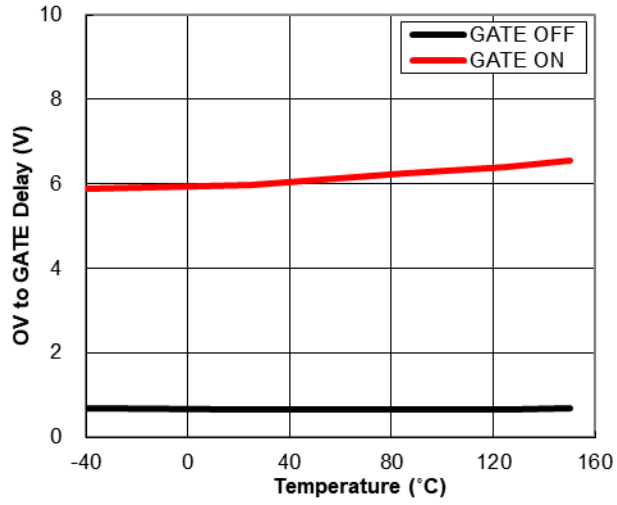

**VIN POR Threshold vs Temperature**



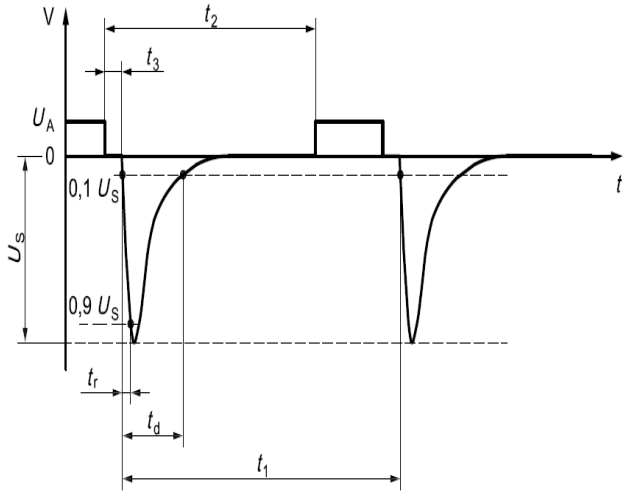

**OVLO Comparator Threshold vs Temperature**



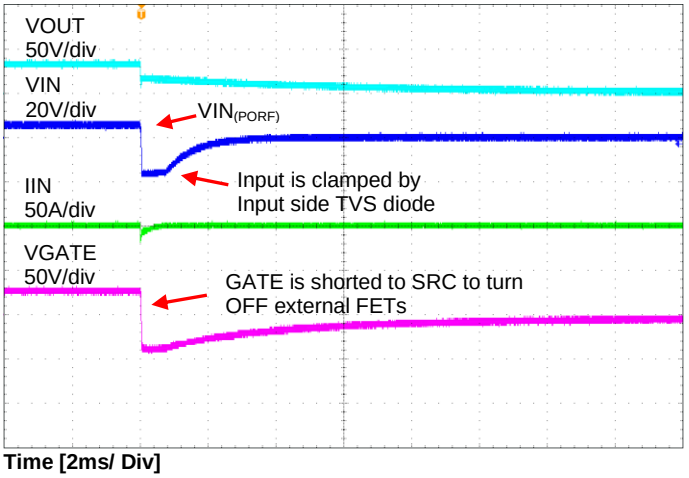

**OVLO to GATE Delay vs Temperature (AP74502HQ)**



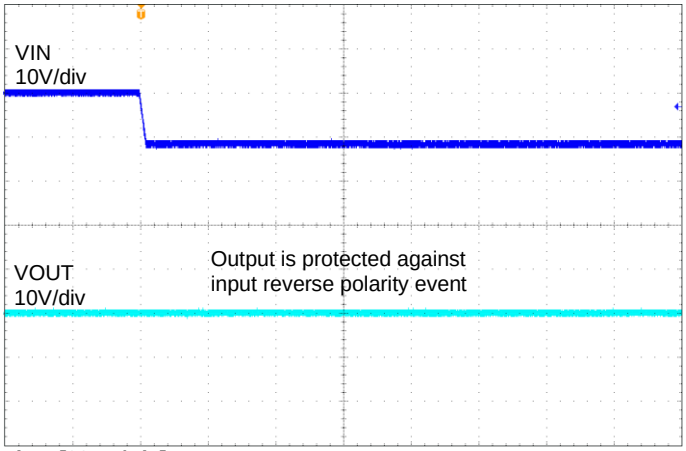
## Application Curves



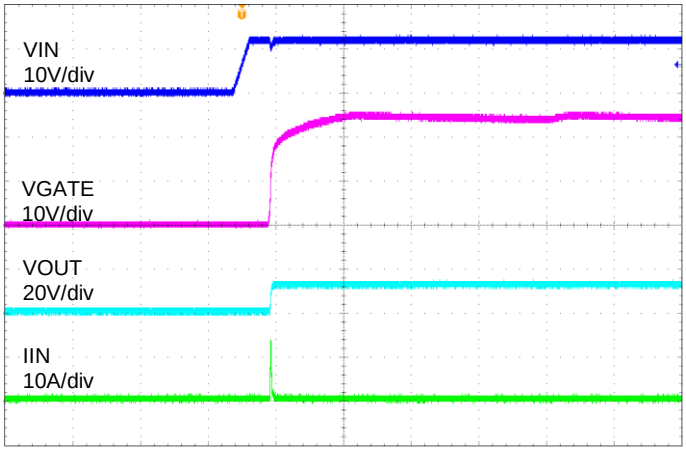

**ISO 7637-2 Pulse 1**



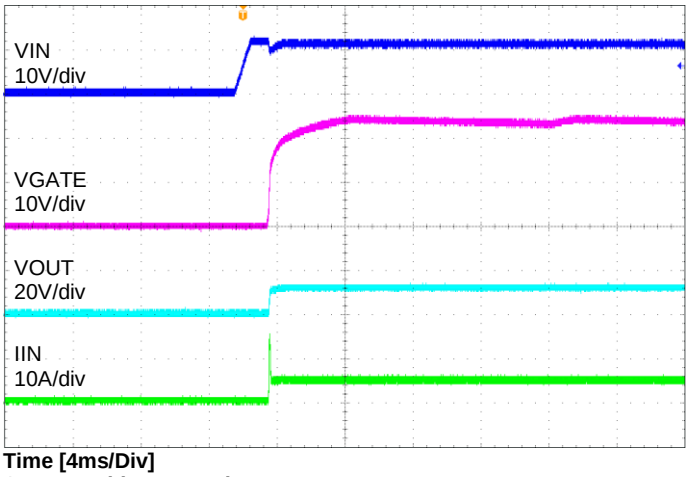

**Time [2ms/ Div]**
**Response to ISO 7637-2 Pulse 1(–150V)**



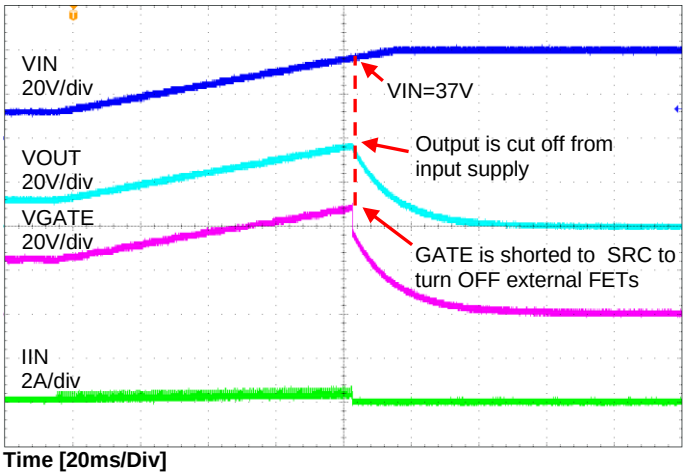

**Time [20ms/Div]**
**Start-up with Input Reverse Voltage(–12 V)**




**Time [4ms/Div]**
**Start-up with No Load**

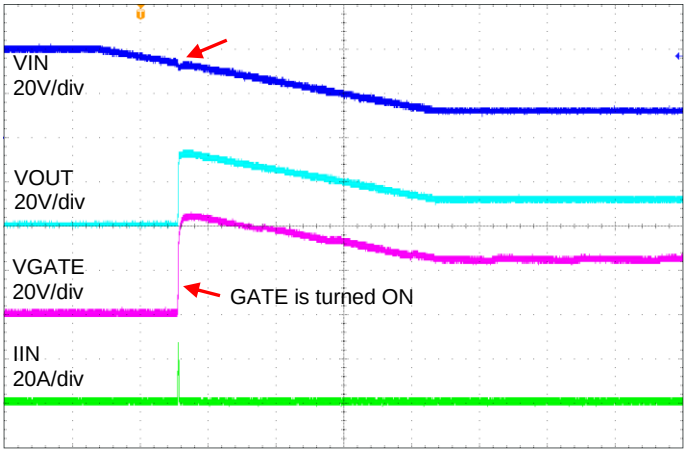



**Time [4ms/Div]**
**Start-up with 5-A Load**

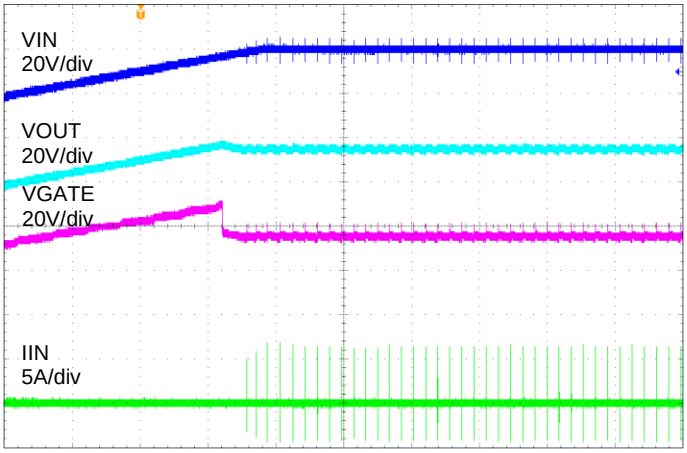



**Time [20ms/Div]**
**Overvoltage Cutoff Response (37V)**

## Application Curves (continued)




**Time [10ms/Div]**
**Overvoltage Recovery**




**Time [20ms/Div]**
**Overvoltage Clamp Response**

## Switching Waveforms

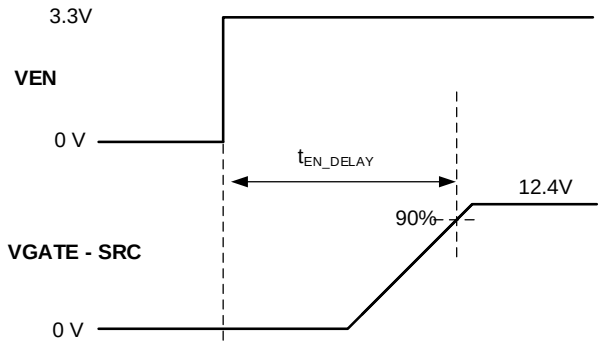



**Figure 1 Timing Diagram tEN_Delay**

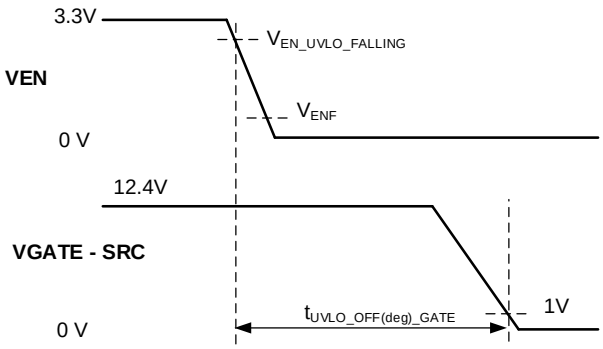



**Figure 2 Timing Diagram tUVLO_OFF_GATE**

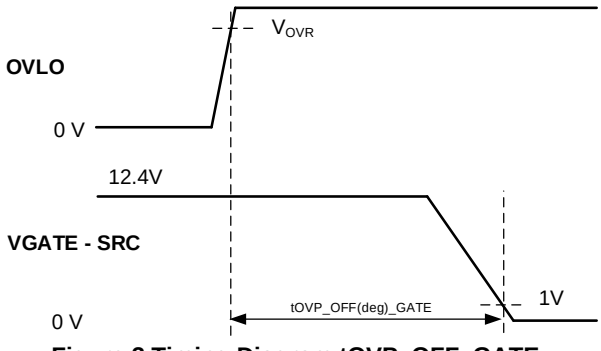



**Figure 3 Timing Diagram tOVP_OFF_GATE**

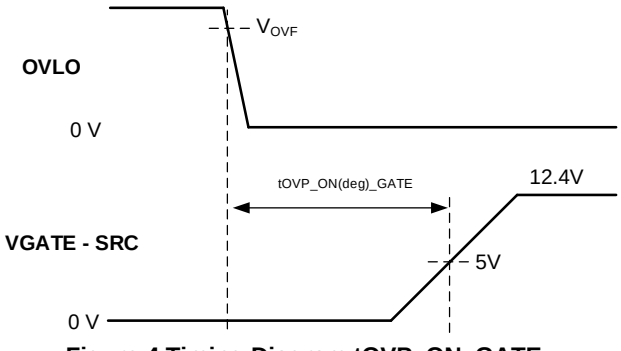



**Figure 4 Timing Diagram tOVP_ON_GATE**

## Detailed Description

### Overview

The AP74502Q, AP74502HQ controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit with load disconnect function. This easy-to-use reverse polarity protection controller is paired with an external back-to-back connected N-channel MOSFETs to replace other reverse polarity schemes such as a P-channel MOSFETs. The wide input supply of 4V to 80V allows protection and control of 12V, 24V and 48V automotive battery powered ECUs. The device can withstand and protect the loads from negative supply voltages down to -65V. An integrated charge pump drives external back-to-back connected N-channel MOSFETs with gate drive voltage of approximately 12.4V to realize reverse polarity protection and load disconnect function in case of overvoltage and under voltage event. The AP74502Q with its typical gate drive strength of 60µA provides smooth start-up with inherent inrush current control due to its lower gate drive strength. The AP74502HQ with its 11mA typical peak gate drive strength is suitable for applications which need faster turn on such as load switch applications. The AP74502Q, AP74502HQ features an adjustable overvoltage cutoff protection feature using a programming resistor divider to OVLO terminal. The AP74502Q, AP74502HQ features enable control. With the enable pin low during the standby mode, both the external MOSFETs and controller is off and draws a very low 0.9µA of current.

### Input Voltage

The VIN pin is used to power the AP74502Q, AP74502HQ internal circuitry, typically drawing 62µA when enabled and 0.9µA when disabled. If the VIN pin voltage is greater than the POR Rising threshold, then the AP74502Q, AP74502HQ operates in either shutdown mode or conduction mode in accordance with the EN/UVLO pin voltage. The voltage from VIN to GND is designed to vary from 80V to -80V, allowing the AP74502Q, AP74502HQ to withstand negative voltage transients.

### Built-in Charge Pump with External Capacitor

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and VIN pin to provide power to turn on the external MOSFET. For the charge pump to supply current to the external capacitor the EN/UVLO pin, voltage must be > $V_{ENF}$. When EN/UVLO > $V_{ENF}$ the charge pump sources a charging current of 300µA typically. If EN/UVLO < $V_{ENF}$ then the charge pump remains disabled. To ensure that the external N-channel MOSFET can be driven above its specified $V_{TH}$, the VCAP to VIN voltage must be above the undervoltage lockout threshold, typically 6.5V, before the internal gate driver is enabled. Use below equation to calculate the initial gate driver enable delay.

$$T_{DRV\_EN} = 75\mu s + C_{VCAP} \times \frac{V_{VCAP\_UVLO\_RISING}}{300\mu A}$$

Where,

$C_{VCAP}$ is the charge pump capacitance connected across ANODE and VCP pins

$V_{VCAP\_UVLO\_RISING}$ = 6.5V (typical)

Typical 1V hysteresis of VCP UVLO threshold enhances linearity of gate driver. The charge pump remains enabled until the VCP to ANODE voltage reaches 12.4V, typically, at which point the charge pump is disabled, decreasing the current draw on the ANODE pin. The charge pump remains disabled until the VCP to ANODE voltage is below 11.6V typically, at which point the charge pump is enabled. The voltage between VCP and ANODE continues to charge and discharge between 11.6V and 12.4V. By enabling and disabling the charge pump, the operating quiescent current of the AP74502Q is reduced. When the charge pump is disabled, it sinks 5µA typical.

#### Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the appropriate GATE to SRC voltage. Before the gate driver is enabled following three conditions must be achieved:

- The EN/UVLO pin voltage must be greater than the specified input high voltage.
- The VCAP to VIN voltage must be greater than the undervoltage lockout voltage.
- The VIN voltage must be greater than VIN POR Rising threshold.

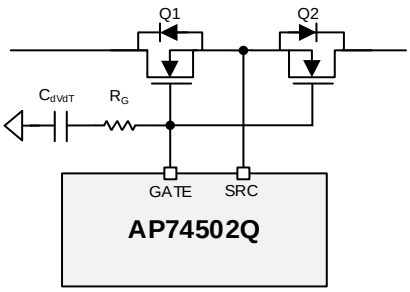
If any of above is not met, the GATE pin is internally connected to the SRC pin, external MOSFET is disabled. After these conditions are met the gate driver operates for enhancing the external MOSFET. The controller offers two gate drive variants. The AP74502Q with typical peak gate drive strength of 60µA is suitable to achieve smooth start-up with inherent inrush current control due to its lower gate drive strength. The AP74502HQ with its 11mA typical peak gate drive strength is suitable for applications, which need faster turn-on such as load switch applications.

The AP74502Q, AP74502HQ SRC pin is capable of handling negative voltage which also makes it suitable for load disconnect switch applications with loads which are inductive in nature.

## Detailed Description (continued)

**Inrush Current Control**

An external circuit can be added on the GATE pin of the AP74502Q to have additional inrush current control for the applications, which have large capacitive loads.




**Inrush Current Limiting with External Components (AP74502Q Only)**

The $C_{dVdT}$ capacitor can control GATE voltage ramping up rate upon external NMOS FET turn on. Use below equation 2 to calculate $C_{dVdT}$ capacitance value.

$$C_{dVdT} = \frac{I_{GATE_{Source}} \times C_{OUT}}{I_{INRUSH}}$$

Whereas $I_{GATE\_SOURCE}$ is 60μA for the AP74502Q, $I_{INRUSH}$ is proportional to ratio of $C_{OUT}$ over $C_{dVdT}$. The series resistor of $R_G$ increases isolation between GATE driver to CdVdT which helps to decrease turn off time. This inrush control circuit with external components is only applicable to the AP74502Q and AP74502HQ is designed to have a strong GATE driver for quickly turn on for loadswitch applications.

**Enable and Undervoltage Lockout (EN/UVLO)**

The AP74502Q, AP74502HQ has an enable pin, EN/UVLO. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN/UVLO pin voltage is greater than the rising threshold, the gate driver and charge pump operate as described in Gate Driver and Charge Pump sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the AP74502Q, AP74502HQ in shutdown mode. The EN/UVLO pin can withstand a voltage as large as 80V and as low as -80V. This feature allows for the EN/UVLO pin to be connected directly to the VS pin if enable functionality is not needed. In conditions where EN/UVLO is left floating, the internal sink current of 3μA pulls EN/UVLO pin low and disables the device. An external resistor divider connected from input to EN/UVLO to ground can be used to implement the input Undervoltage Lockout (UVLO) functionality. When EN/UVLO pin voltage is lower than UVLO comparator rising threshold ($V_{EN\_UVLO\_RISING}$) but higher than enable falling threshold (VENF), the device disables gate drive voltage, however, charge pump is kept on. This action ensures quick recovery of gate drive when UVLO condition is removed. If UVLO functionality is not required, connect EN/UVLO pin to VS.

**Overvoltage Protection (OVLO)**

The AP74502Q, AP74502HQ provides programmable overvoltage protection feature with OVLO pin. A resistor divider can be connected from input source to OVLO pin to ground to set overvoltage threshold. An internal comparator compares the input voltage against fixed reference (1.25V) and disables the gate drive as soon as OVLO pin voltage goes above the OVLO comparator reference. When the resistor divider is referred from input supply side, the device is configured for overvoltage cutoff functionality. When the resistor divider is referred from output side (VOUT), the device is configured for overvoltage clamp functionality. When OVLO pin voltage goes above OVLO comparator $V_{OV\_RISING}$ threshold (1.24V typical), the device disables gate drive, however, charge pump remains active. When OVLO pin voltage falls below $V_{OV\_FALLING}$ threshold (1.14V typical), the gate is quickly turned on as charge pump is kept on and the device does not go through the device start-up process. When OV pin is not used, it can be connected to ground.

## Detailed Description (continued)

**Device Operation Mode**

| VIN | EN/UVLO | OVLO | Gate Driver (GATE) | Charge Pump (VCP) | Device Operation Mode |
|---|---|---|---|---|---|
| < $V_{VIN\_POR}$ | Don't Care | Don't Care | N/A | N/A | Power Off (No Power) |
| > $V_{VIN\_POR}$ | < $V_{ENF}$ | Don't Care | Connect to SRC | Disabled | Shutdown Mode |
| | > $V_{ENF}$, < $V_{EN\_UVLO}$ | < $V_{OV}$ | Connect to SRC | Enabled | UVLO Mode |
| | > $V_{EN\_UVLO}$ | < $V_{OV}$ | Enabled | Enabled | Conduction Mode |
| | | > $V_{OV}$ | Connect to SRC | Enabled | OVP Mode |

**Shutdown Mode**

The AP74502Q, AP74502HQ enters shutdown mode when the EN/UVLO pin voltage is below $V_{EN\_UVLO}$. In this mode, both the gate driver and the charge pump are disabled in shutdown mode and the AP74502Q consume minimum power by $I_{SHDN}$ (typ 0.9μA) at VIN pin.

**Conduction Mode**

The AP74502Q, AP74502HQ enters conduction mode driving external NMOSFET to be in enhancement mode only if all of below conditions are met.

- VIN > $V_{VIN\_POR}$
- EN/UVLO > $V_{EN\_UVLO}$
- OVLO < $V_{OV}$

In this mode, Gate pin will drive external NMOSFET to be in conduction state. The AP74502Q and AP74502HQ drive Gate pin in 2 different methods.

- The AP74502Q drives Gate pin through 60μA current source for slow turning on external NMOSFET.
- The AP74502HQ connects Gate to VCP for fast turning external NMOSFET.

**UVLO Mode and OVP Mode**

To protect downstream application circuit, In UVLO mode or OVP mode, the AP74502Q, AP74502HQ turn off external NMOS FET by routing Gate pin to SRC and keeps enabled Charge pump for being ready to go back to conduction mode whenever UVLO or OVLO condition is removed.

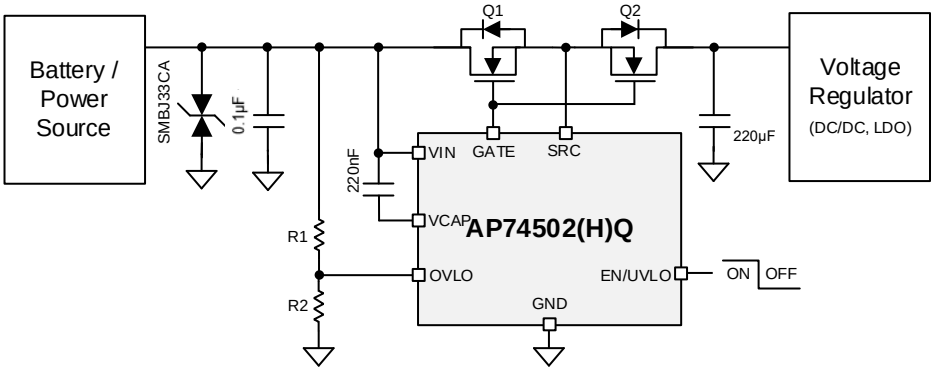
The AP74502Q, AP74502HQ enter UVLO or OVP mode.

- If EN/UVLO < $V_{EN\_UVLO}$ or OVLO > $V_{OV}$

## Application Information

The AP74502Q, AP74502HQ is used with N-Channel MOSFET controller in a typical reverse polarity protection application. The schematic for the 12V battery protection application is shown below where the AP74502Q, AP74502HQ is used to drive back-to-back connected MOSFETs Q1 and Q2 in series with a battery for reverse polarity protection and load disconnection. The TVS is required for protection for the AP74502Q, AP74502HQ and its downstream application against positive and negative voltage surges and ESD event. Output Capacitor is recommended for filtering out supply upon dynamic load condition.

**Typical Application**




**Design Example**

| Design Parameter | Example Value |
|---|---|
| VIN Range | 12V Vehicle Battery, 12V nominal with 3.2V cold crank and 35V load dump condition |
| VOUT | 3.2V during cold crank to 35V load dump |
| IOUT | 3A nominal and 5A maximum |
| COUT | 220µF typical hold up Capacitor |
| Overvotlage Protection | Typical 37V for 12V battery system |
| Automotive EMC Compliance | ISO 7637-2 and ISO 16750-2 |

**MOSFET Selection**

The important MOSFET electrical parameters are the maximum continuous drain current, $I_D$, the maximum drain-to-source voltage, $V_{DS(MAX)}$, the maximum source current through body diode, and the drain-to-source on resistance, $R_{DS(ON)}$.

The maximum continuous drain current, $I_D$, rating must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. It is recommended to use MOSFETs with voltage rating up to 75V maximum with the AP74502Q, AP74502HQ. The maximum $V_{GS}$ the AP74502Q, AP74502HQ can drive is 13.9V, so a MOSFET with 15V minimum $V_{GS}$ rating must be selected. If a MOSFET with $V_{GS}$ rating < 15V is selected, a Zener diode can be used to clamp $V_{GS}$ to safe level within Max $V_{GS}$ of the MOSFET.

To reduce the MOSFET conduction losses, lowest possible $R_{DS(ON)}$ is preferred. Selecting a MOSFET with $R_{DS(ON)}$ that gives $V_{DS}$ drop 20mV to 50 mV at full load provides good trade off in terms of power dissipation and cost. Thermal resistance of the MOSFET must be considered against the expected maximum power dissipation in the MOSFET to ensure that the junction temperature ($T_J$) is well controlled.

## Application Information (continued)

**Overvoltage Protection Threshold**

Resistors R1 and R2 voltage divider can be used to adjust the overvoltage threshold. Connecting R1 to VIN provides overvoltage cutoff and switching the connection to VOUT provides overvoltage clamp response. The resistor values required for setting the overvoltage threshold $V_{OV}$ to 37V are calculated by below equation.

$$V_{OVProtection\_threshold} = V_{OVR} \cdot \left(1 + \frac{R_1}{R_2}\right) = 1.25V \times \left(1 + \frac{R_1}{R_2}\right)[V] \; whereas \; V_{OVR} \; is \; 1.25V.$$

For minimizing the input current drawn from the supply through resistors R1 and R2, we recommend to use higher value of resistance. Using high value resistors adds error in the calculations because the current through the resistors at higher value becomes comparable to the leakage current into the OVLO pin. Select (R1 + R2) such that current through resistors is around 100 times higher than $I_{OV}$, which is the leakage into OVLO pin (Max 110nA). R1 = 100kΩ and R2 = 3.5kΩ as a standard resistor value to set overvoltage cutoff of 37V. Based on application use case, overvoltage threshold can be set at the lower voltage as it enables lower rated downstream components, thus providing solution size and lower cost benefit.

**Charge Pump VCAP, Input and Output Capacitance**

Minimum required capacitance for charge pump(C_VCAP), Input capacitance (CIN) and output capacitance are:

- C_VCAP: Minimum recommended value of C_VCAP [μF] ⩾ 10 × $C_{ISS(MOSFET\_effective)}$ [μF], C_VCAP of 0.22 [μF] is selected
- CIN: Typical input capacitor of 0.1 [μF]
- COUT: Typical output capacitor 220 [μF]

**Appropriate TVS Diodes for 12V Battery Applications**

TVS diodes are used in automotive systems for protection against transients. In the 12V battery protection application circuit shown below, a bi-directional TVS diode is used to protect from positive and negative transient voltages that occur during normal operation of the car and these transient voltage levels and pulses are specified in ISO 7637-2 and ISO 16750-2 standards.

There are two important specifications, breakdown voltage and clamping voltage of the TVS. Breakdown voltage is the voltage at which the TVS diode goes into avalanche similar to a Zener diode and is specified at a low current value typical 1mA, and the breakdown voltage should be higher than worst case steady state voltages seen in the system. The breakdown voltage of the TVS+ should be higher than 24V jump start voltage and 35V suppressed load dump voltage and less than the maximum ratings of the AP74502Q(80V). The breakdown voltage of TVS- should be beyond maximum reverse battery voltage -16V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

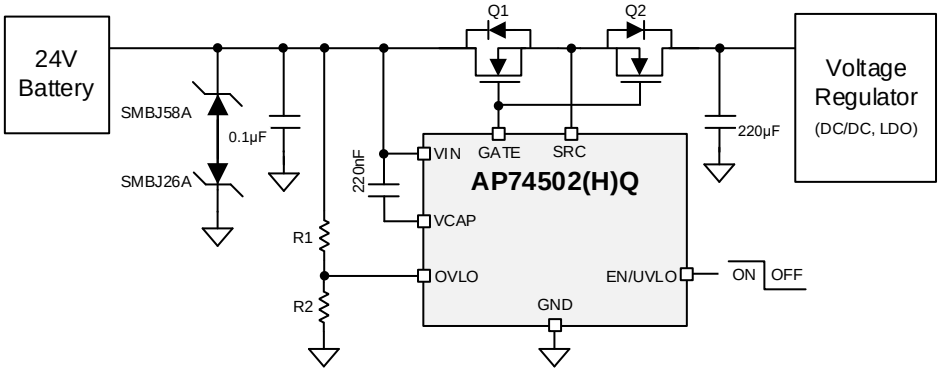
Clamping voltage is the voltage the TVS diode clamps in high current pulse situations and this voltage is much higher than the breakdown voltage. TVS diodes are meant to clamp transient pulses and should not interfere with steady state operation. In the case of ISO 7637-2 Pulse 1, the input voltage goes up to -150V with a generator impedance of 10Ω. This translates to 15A flowing through the TVS- and the voltage across the TVS would be close to its clamping voltage.

The next criterion is that the absolute minimum rating of VIN voltage of the AP74502Q (-80V) and the maximum VDS rating MOSFET are not exceeded. In the design example, 60V rated MOSFET is selected. SMBJ series of TVS are rated up to 600W peak pulse power levels. This rating is sufficient for ISO 7637-2 pulses and suppressed load dump (ISO-16750-2 pulse B).

## Application Information (continued)

**Appropriate TVS Diodes and MOSFET for 24V Battery Applications**

Typical 24V battery protection application circuit shown in below diagram that uses two uni-directional TVS diodes to protect from positive and negative transient voltages.



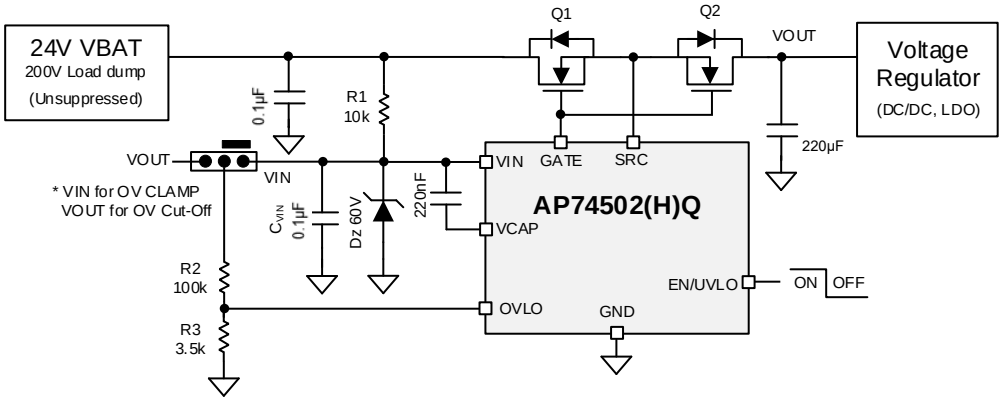

The breakdown voltage of the TVS+ must be higher than 48V jump start voltage, less than the absolute maximum ratings of source and enable pin of the AP74502Q, AP74502HQ (80V) and must withstand 65V suppressed load dump. The breakdown voltage of TVS- must be lower than maximum reverse battery voltage -32V, so that the TVS- is not damaged due to long time exposure to reverse connected battery.

During ISO 7637-2 pulse 1, the input voltage goes up to -600V with a generator impedance of 50Ω. Single bi-directional TVS cannot be used for 24V battery protection because breakdown voltage for TVS+ ≥ 48V, maximum negative clamping voltage is ⩽ 65V. Two uni-directional TVS connected back-to-back must be used at the input. For positive side TVS+, We recommend SMBJ58A with the breakdown voltage of 64.4V (minimum), 67.8 (typical). For the negative side TVS-, We recommend SMBJ26A with breakdown voltage close to 32V (to withstand maximum reverse battery voltage -32 V) and maximum clamping voltage of 42V.

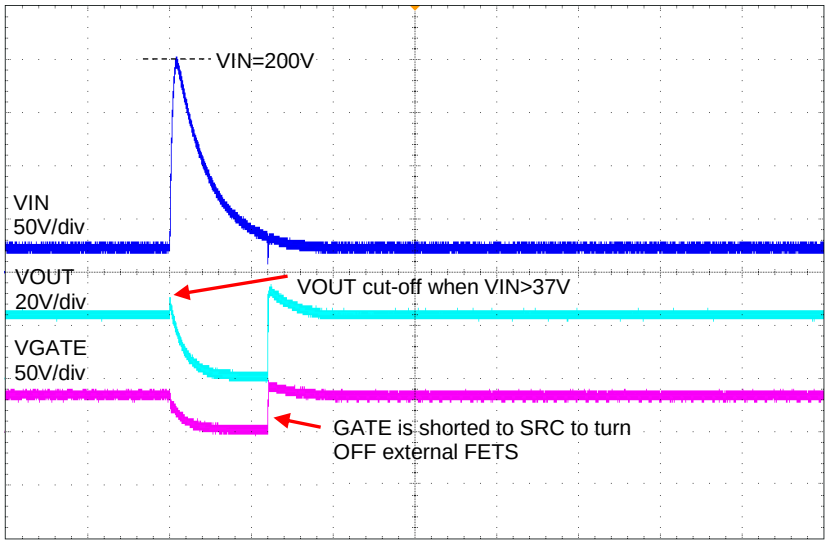
For 24V battery protection, we recommend a 75V rated MOSFET to be used along with SMBJ26A and SMBJ58A connected back-to-back at the input.

**Surge Stopper Using the AP74502Q, AP74502HQ**

Many automotive applications are designed to comply with unsuppressed load dump transients specified by ISO16750-2 Pulse 5A. The AP74502Q, AP74502HQ can be configured as input surge stopper to provide overvoltage along with input reverse supply protection and protect the downstream loads in case of unsuppressed load dump event.



## Application Information (continued)




**Time [100ms/Div]**
**200V Surge Stopper with Overvoltage Cutoff Using AP74502Q**

**VIN Capacitance ($C_{VIN}$), Resistor R1 and Zener Clamp (Dz)**

A minimum of 1µF $C_{VIN}$ capacitance is required. During input overvoltage transient, resistor R1 and Zener diode $D_Z$, are used to protect VIN pin from exceeding the maximum ratings by clamping VIN to 60V. Choosing R1 = 10kΩ, the peak power dissipated in Zener diode $D_Z$ can be calculated using below equation:

$$P_{DZ} = V_{DZ} \times \frac{(V_{IN_{MAX}} - V_{DZ})}{R_1}$$

Where $V_{DZ}$ is the breakdown voltage of Zener diode. Select the Zener diode that can handle peak power requirement.
Peak power dissipated in resistor R1 can be calculated using below equation:

$$P_{R1} = \frac{(V_{IN_{MAX}} - V_{DZ})^2}{R_1}$$

Select a resistor package which can handle peak power and maximum DC voltage.

**Overvoltage Protection**

For the overvoltage setting, refer to the resistor selection procedure described in Overvoltage Protection. Select $R_2$ = 100kΩ and $R_3$ = 3.5kΩ as a standard resistor value to set overvoltage cutoff of 37V.

**MOSFET Selection**

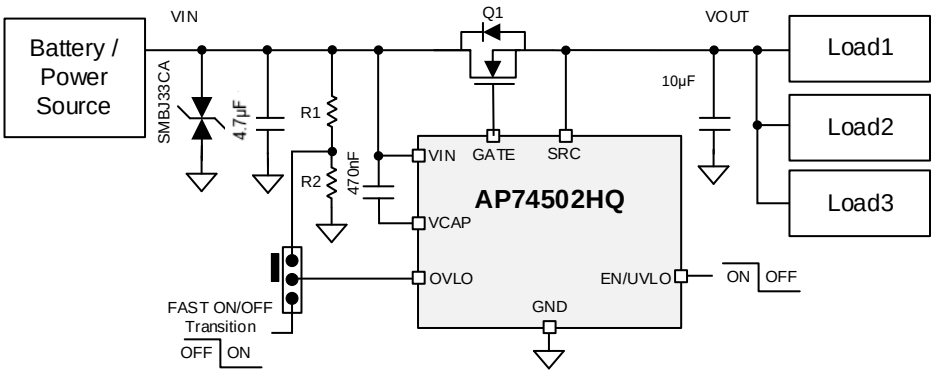
The VDS rating of the MOSFET Q1 must be minimum VIN(max) for designs with output overvoltage cutoff where output can reach 0V with higher loads. For designs with output overvoltage clamp, MOSFET VDS rating must be (VIN(max) – VOUT_CLAMP). The VGS rating is based on GATE-SRC maximum voltage of 15V. We recommend a 20V VGS rated MOSFET. Power dissipation on MOSFET Q1 on a design where output is clamped is critical and SOA characteristics of the MOSFET must be considered with sufficient design margin for reliable operation. An additional Zener diode from GATE to SRC can be needed to protect the external FET in case output is expected to drop to the level where it can exceed external FET VGS(max) rating.

## Application Information (continued)

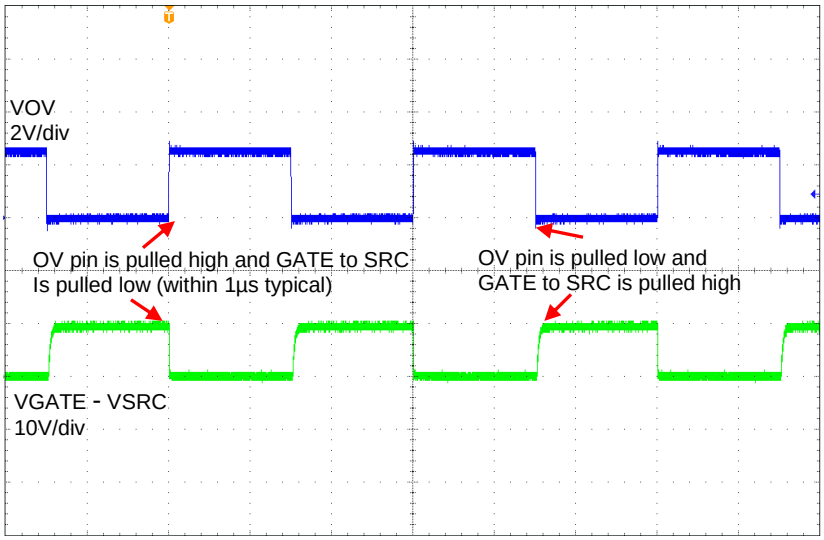
**Fast Turn-On and Turn-Off High Side Switch Driver Using the AP74502HQ**

In automotive load driving applications N-Channel MOSFET based high side switch is very commonly used to disconnect the loads from supply line in case of faults such as overvoltage event. The AP74502Q, AP74502HQ can be used to drive external MOSFET to perform simple high side switch with overvoltage protection. Below diagram shows a typical application circuit where the AP74502HQ is used to drive external MOSFET Q1 as a switch for main power path control. A resistor divider from input to OVLO pin to ground can be used to set the overvoltage threshold.

If VOUT node (SRC pin) of the device is expected to drop in case of events such as overcurrent or short-circuit on load side, then additional Zener diode is required across gate and source pin of external MOSFET to protect it from exceeding its maximum $V_{GS}$ rating.




Many safety applications require fast switching off of the MOSFET in case of fault events such as overvoltage or overcurrent fault. Some of the load driving path applications also require PWM operation of high side switch. The AP74502HQ OVLO pin can be used as control input to perform fast turn-on and turn-off mode transition. With OVLO pin pulled above $V_{OVR}$ threshold of (1.25V typical), the AP74502HQ turns off the external MOSFET (with $C_{ISS}$ = 4.7nF) within 1µs typically. When OVLO pin is pulled low, the AP74502HQ with its peak gate drive strength of 11mA turns on external MOSFET with turn-on speed of 7µs typical.




**Time [200µs/Div]**
**Fast Turn-On and Turn-Off High Side Switch Driver Using AP74502HQ**

**Power Supply Recommendations**

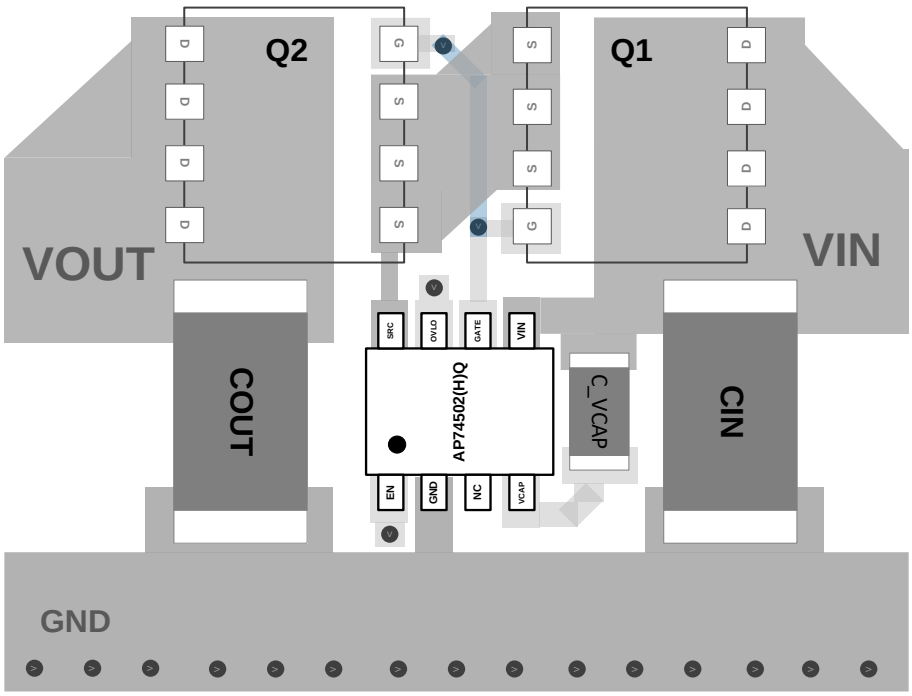
The AP74502Q, AP74502HQ reverse polarity protection controller is designed for the supply voltage range of 3.2V ≤ VS ≤ 80V. If the input supply is located more than a few inches from the device, we recommend an input ceramic bypass capacitor higher than 0.1µF. Based on system requirements, a higher input bypass capacitor can be needed with the AP74502HQ to avoid supply glitch in case of high inrush current start-up event. To prevent the AP74502Q, AP74502HQ and surrounding components from damage under the conditions of a direct output short circuit, use a power supply having overload and short-circuit protection.

## Application Information (continued)

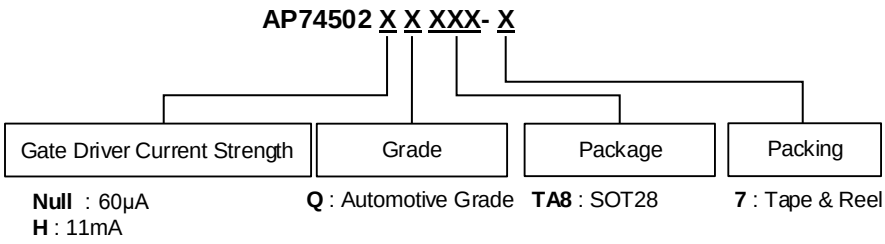
**Layout Guidelines**

- Connect GATE and SRC pin of the AP74502Q, AP74502HQ close to the MOSFET's gate and source pin.
- Use thick traces or filled plane for source and drain of the MOSFET to minimize resistive losses because the high current path of for this solution is through the MOSFET.
- Keep the charge pump capacitor across VCAP and VIN pin away from the MOSFET to lower the thermal effects on the capacitance value.
- Connect the GATE pin of the AP74502Q, AP74502HQ to the MOSFET gate with short trace. Avoid excessively thin and long running trace to the Gate Drive.

**Layout Example**



## Ordering Information

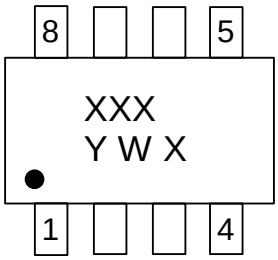



| Orderable Part Number | Gate Driver Strength | Enable Active | Package Code | Package | Packing | |
|---|---|---|---|---|---|---|
| | | | | | Qty. | Carrier |
| AP74502QTA8-7 | 60µA | HIGH | TA8 | SOT28 | 3000 | 7" Tape and Reel |
| AP74502HQTA8-7 | 11mA | HIGH | TA8 | SOT28 | 3000 | 7" Tape and Reel |

## Marking Information

**SOT28**

**(Top View)**



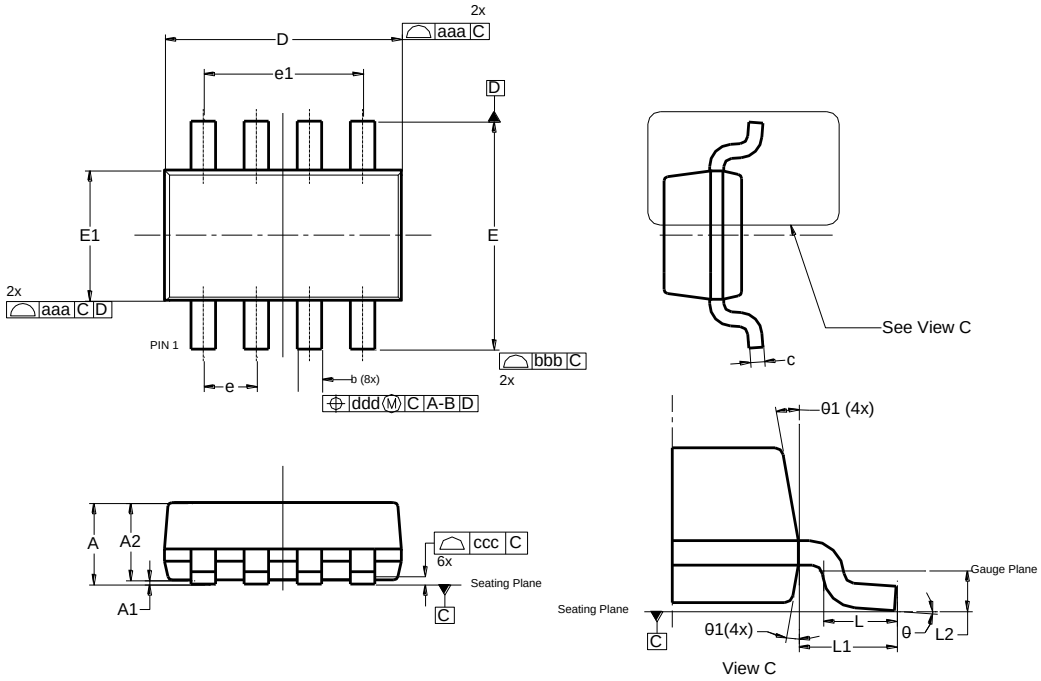

XXX : Identification Code
Y : Year 0 to 9
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents 52 and 53 week
X : Internal Code

| Orderable Part Number | Package | Identification Code |
|---|---|---|
| AP74502QTA8-7 | SOT28 | T2Q |
| AP74502HQTA8-7 | SOT28 | T3Q |

## Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

**SOT28**

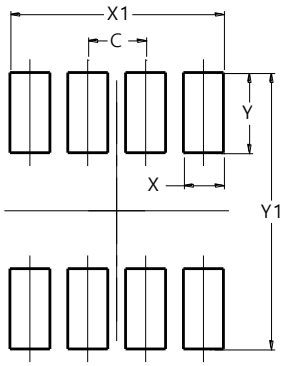



| SOT28 | | | |
|---|---|---|---|
| **Dim** | **Min** | **Max** | **Typ** |
| **A** | 0.90 | 1.10 | 1.00 |
| **A1** | 0.00 | 0.10 | -- |
| **A2** | -- | -- | 0.95 |
| **b** | 0.20 | 0.40 | 0.30 |
| **c** | 0.08 | 0.20 | -- |
| **D** | 2.85 | 2.95 | 2.90 |
| **E** | 2.65 | 2.95 | 2.80 |
| **E1** | 1.55 | 1.65 | 1.60 |
| **e** | 0.65 BSC | | |
| **e1** | 1.95 BSC | | |
| **L** | 0.30 | 0.60 | 0.45 |
| **L1** | 0.60 REF | | |
| **L2** | 0.25 BSC | | |
| **θ** | 0° | 8° | -- |
| **θ1** | 9° | 11° | 10° |
| **aaa** | 0.15 | | |
| **bbb** | 0.25 | | |
| **ccc** | 0.10 | | |
| **ddd** | 0.20 | | |
| **All Dimensions in mm** | | | |

## Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

**SOT28**



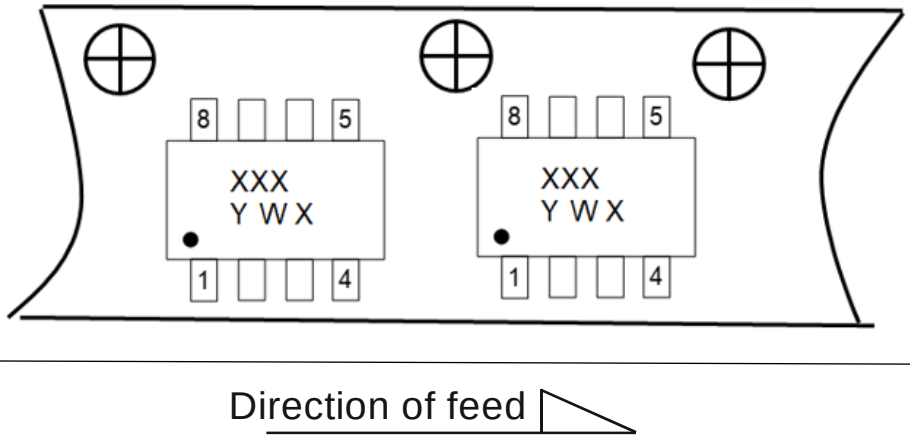

| Dimensions | Value (in mm) |
|---|---|
| **C** | 0.950 |
| **G** | 1.600 |
| **X** | 0.700 |
| **Y** | 0.900 |
| **Y1** | 3.400 |

**Note:** The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application. These dimensions may be modified based on user equipment capability or fabrication criteria. A more robust pattern may be desired for wave soldering and is calculated by adding 0.2 mm to the 'Z' dimension. For further information, please reference document IPC-7351A, Naming Convention for Standard SMT Land Patterns, and for international grid details, please see document IEC, Publication 97.

**Note:** For high-voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

## Device Taping Orientation

**Package Type: SOT28**

| Tape Width | Part Number Suffix | Tape Orientation |
|---|---|---|
| 8mm | -7 |  |

**Note**: For part marking, refer to product datasheet.
**Note:** Tape and package drawings are not to scale and are shown for device tape orientation only.
**Note:** The taping orientation of the other package type can be found on our website at https://www.diodes.com/assets/Packaging-Support-Docs/AP02007.pdf.

## Mechanical Data

- Surface-Mount Package
- Moisture Sensitivity: Level 1 per J-STD-020
- Package Material: Molded Plastic, UL Flammability Classification Rating 94V-0
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.016 grams (Approximate)
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020

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