AVR32SD20/28/32 Preliminary Data Sheet

AVR32SD20/28/32

www.microchip.com Product Pages: AVR32SD20, AVR32SD28, AVR32SD32

Introduction

The AVR® SD Family microcontrollers, designed in compliance with the ISO 26262 functional safety standard, incorporate the AVR® CPU with a hardware multiplier running at clock speeds up to 20 MHz. They offer 32/64 KB of Flash, 4/8 KB of SRAM, and 256 bytes of EEPROM. The microcontrollers are available in 20-, 28-, 32- and 48-pin packages. The family uses our latest technologies, with a flexible and low-power architecture, including an Event System, accurate analog features, and advanced digital peripherals. The AVR® SD provides a dual-core lockstep CPU, Single-Error Correcting and Double-Error Detecting (SECDED) ECC on Flash, EEPROM and SRAM, Error Controller for functional safety, and Program and Debug Interface Disable (PDID) for security.

Features

- AVR CPU in Dual-Core Lockstep (DCLS) Configuration
  - Running at up to 20 MHz
  - Single-cycle I/O access
  - Two-level interrupt controller
  - Two-cycle hardware multiplier
  - Supply voltage range: 2.7-5.5V
- Memories
  - 32 KB in-system-programmable Flash memory with ECC
  - 4 KB SRAM with ECC
  - 256B EEPROM with ECC
  - 512B of user row in Non-Volatile Memory (NVM) that can keep data during chip-erase and be programmed while the device is locked
  - 256B of Boot Row for cryptographic keys, only readable from the Boot Section
- System
  - Power-on Reset (POR)
  - Brown-out Detector (BOD) with programmable levels
  - Voltage Regulator Monitor (VMON)
  - Clock options
    - High-precision internal oscillator with selectable frequency up to 20 MHz
    - PLL up to 48 MHz for high-frequency operation of the TCD
    - Internal 32.768 kHz oscillator
    - External 32.768 kHz crystal oscillator
    - External clock input
    - High-frequency external crystal oscillator

  - Clock Failure Detection (CFD)
  - Clock Frequency Measurement (CFM)
  - Single-pin Unified Program and Debug Interface (UPDI)
  - Three sleep modes
    - Idle with all peripherals running for immediate wake-up
    - Standby with a configurable operation of selected peripherals
    - Power-Down with full data retention
  - Automated Cyclic Redundancy Check (CRCSCAN) program memory scan
    - Verification of the Boot Flash section
    - CRC-16-CCITT or CRC-32 (IEEE 802.3)
  - External interrupt on all general-purpose pins
- Peripherals
  - 6-channel Event System for predictable and CPU-independent inter-peripheral signaling
  - One 16-bit Timer/Counter type A (TCA) with three compare channels for PWM and waveform generation
  - Up to four 16-bit Timer/Counter type B (TCB) with input capture for capture and signal measurements
  - One 12-bit Timer/Counter type D (TCD) optimized for power control
  - One 16-bit Real-Time Counter (RTC) that can run from an external crystal or internal oscillator
  - Up to three USARTs
    - Operation modes: RS-485, LIN client, host SPI, and IrDA
    - Fractional baud rate generator, auto-baud, and start-of-frame detection
  - Two SPI with host/client operation modes
  - Two I^2C with simultaneous host/client operation (dual mode) and dual address match
  - One Configurable Custom Logic (CCL) with up to six programmable Lookup Tables (LUTs)
  - Two 10-bit, 170 ksps, Analog-to-Digital Converters (ADC) with independent voltage reference sources
  - One 10-bit Digital-to-Analog Converter (DAC)
  - Three Analog Comparators (AC)
  - Up to two Zero Cross Detectors (ZCD)
  - Internal 1.024V, 2.048V, 4.096V and 2.500V voltage references, and external reference option
- System Integrity Functions
  - Error Controller (ERRCTRL)
    - Central interface for fault detection
    - Fault handling in hardware according to programmable severity
    - Optional Heartbeat output
    - Optional tri-stating of all I/O pins in case of fault
  - Parity on data buses
  - Dual Watchdogs
    - Synchronous Watchdog Timer (SWDT)
    - Watchdog Timer (WDT) with window mode and separate on-chip oscillator with clock failure detection
  - Voltage Level Monitor (VLM) with interrupt
  - Program and Debug Interface Disable (PDID)
- I/O and Packages

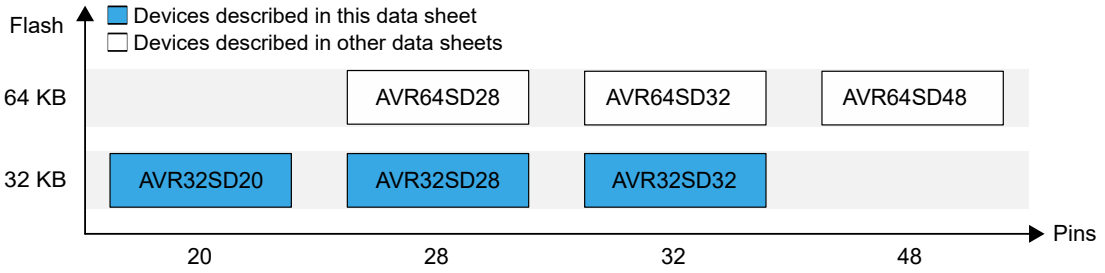
  - Up to 25 programmable I/O pins
  - Multi-voltage I/O with built-in voltage level converters
  - 20-pin SSOP
  - 28-pin VQFN, SSOP, and SPDIP
  - 32-pin VQFN and TQFP
- Temperature Ranges
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

AVR® SD Family Overview

The figure below shows the AVR SD devices, laying out pin count variants and memory sizes:

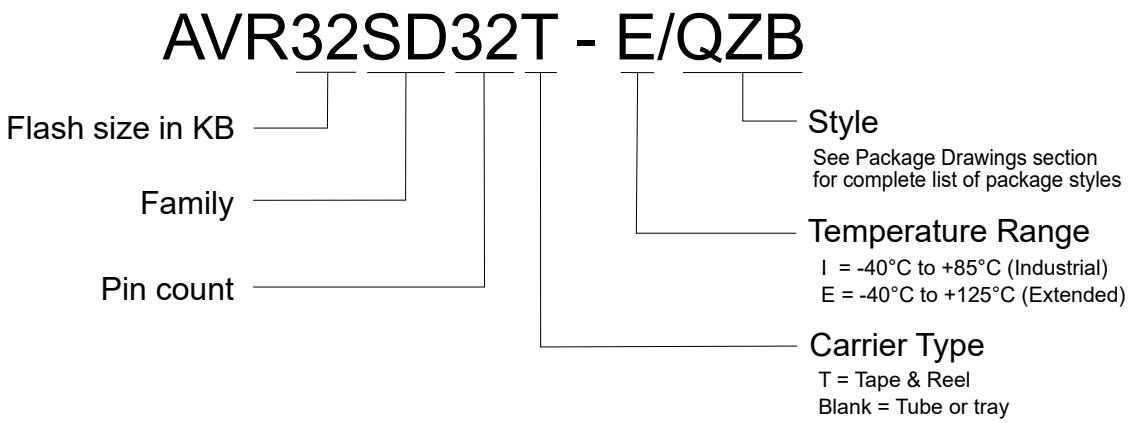
- Vertical migration is possible without code modification, as these devices are fully pin- and feature-compatible
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1. AVR SD Family Overview



A device name in the AVR SD Family is decoded as follows:

Figure 2. AVR® SD Device Designations



Memory Overview

The following table shows the memory overview of the entire AVR SD family.

Table 1. Memory Overview

Devices	AVR32SD20 AVR32SD28 AVR32SD32	AVR64SD28 AVR64SD32 AVR64SD48
Flash memory with ECC	32 KB	64 KB
SRAM with ECC	4 KB	8 KB
EEPROM	256B	256B
User row	512B	512B
Boot row/cryptographic key storage	256B	256B

Peripheral Overview

The following table shows the peripheral overview of the entire AVR SD family.

Table 2. Peripheral Overview

Feature	AVR32SD20	AVR32SD28 AVR64SD28	AVR32SD32 AVR64SD32	AVR64SD48
Pins	20	28	32	48
Max. frequency (MHz)	20	20	20	20
Clock Controller (CLKCTRL) with Clock Failure Detection (CFD) and Clock Frequency Measurement (CFM)	1	1	1	1
Clock Failure Detection (CFD)	2	2	2	2
Clock Frequency Measurement (CFM)	2	2	2	2
16-bit Timer/Counter type A (TCA)	1	1	1	1
16-bit Timer/Counter type B (TCB)	4	4	4	4
12-bit Timer/Counter type D (TCD)	1	1	1	1
Real-Time Counter (RTC)	1	1	1	1
USART	2	3	3	3
SPI	2	2	2	2
TWI/I^2C[1]	1[1]	1[1]	2[1]	2[1]
10-bit ADC (channels)	2 (13)	2 (19)	2 (23)	2 (28)
Analog Comparator (AC)	3	3	3	3
Digital-to-Analog Converter (DAC)	1	1	1	1
Zero Cross Detector (ZCD)	1	2	2	2
Peripheral Touch Controller (PTC)	-	-	-	-
Operational amplifier (OP)	-	-	-	-
Configurable Custom Logic Look-up Table (CCL LUT)	6	6	6	6
Error Controller (ERRCTRL)	1	1	1	1
Synchronous Watchdog Timer (SWDT)	1	1	1	1
Watchdog Timer (WDT)	1	1	1	1
Event System (EVSYS) channels	6	6	6	6
General Purpose I/O	15	21	25	40
PORT	PA[7:0], PC[3:1], PD[7:4]	PA[7:0], PC[3:0], PD[7:1], PF[1,0]	PA[7:0], PC[3:0], PD[7:1], PF[5:0]	PA[7:0], PB[5:0], PC[7:0], PD[7:0], PE[3:0], PF[5:0]
PORT pins with MVIO capability	PC[3:1]	PC[3:0]	PC[3:0]	PC[7:0]
External interrupts	15	21	25	40
CRCSCAN	1	1	1	1
Unified Program and Debug Interface (UPDI)	1	1	1	1

Note:

1. The TWI/I^2C can operate simultaneously as host and client on different pins.