LN-CSAC Low-Noise Chip-Scale Atomic Clock

The Low-Noise Chip-Scale Atomic Clock (LN-CSAC)

The Low-Noise Chip-Scale Atomic Clock (LN-CSAC) model SA65-LN combines the spectral purity of a crystal with the accuracy and stability of an atomic clock into a single device, saving board space, power and design time.

Microchip, the developer of CSAC, has integrated its 3rd generation low power evacuated miniature crystal oscillator (EMXO) into the design, enabling a lower profile height of ½ inch (12.7 mm) that it is well suited for narrow VPX-style chassis. Its impressive power consumption (<295 mW) and wide temperature range enables battery-powered operation in diverse environmental conditions.

Rapid Calibration

The LN-CSAC accepts a 1 PPS input to automatically calibrate the phase and frequency to an external reference clock to within 1 ns and 1×10^{-12} , respectively. The loop settings can be easily adjusted by the user, saving board space and software development time.

Field Deployable

The low power consumption and wide temperature range (option -002) make the LN-CSAC ideal for battery powered and temperature-exposed applications. The temperature stability of the EMXO is improved by the CSAC, maintaining a maximum frequency tolerance of $\pm 3 \times 10^{-10}$ regardless of external temperature changes. This is especially important when the LN-CSAC is in free-running "holdover" mode and cannot be calibrated to a primary reference clock.

Features

- CSAC accuracy and temperature stability
- Sine wave output
 - ADEV @ 1s < 3 × 10⁻¹¹
 - Phase Noise @ 10 Hz < -120 dBc /Hz
- Wide temperature (option -002) –40°C to +80°C

Surger SAC

- Height < ½ inch (12.7 mm)
- Power < 295 mW

Applications

- Low SWaP VPX designs
- Mobile radar
- Dismounted radios
- Dismounted IED jamming systems
- Autonomous sensor networks
- Unmanned vehicles



This product is compatible with Microchip's Clockstudio[™] software tool for control and analysis of atomic clocks: microchip.com/clockstudio







Specifications¹

Electrical

RF Output (Pin 3)			
Frequency	10 MHz		
Format	Sine Wave		
Amplitude	6–9 dBm		
Load Impedance	50Ω		
Quantity	1		
1PPS (Output (Pin 10)		
Rise/fall Time	<10 ns		
Pulse Width	20 µs		
(programmable)	(10 μS - 500 mS, 10 μS step)		
Level	0V to 3V		
Logic High (V ^{OH}) Min	2.80V		
Logic Low (V ^{OL}) Max	0.30V		
Load Impedance	1 MΩ		
Quantity	1		
1PPS Input (Pin 9)			
Format	Rising edge		
Low Level	<0.5V		
High Level	2.5V to 3.3V		
Load Impedance	1 MΩ		
Quantity	1		
Serial Comm	nunications (Pins 7, 8)		
Protocol	RS-232		
Format	CMOS 0V to 3V		
Tx/Rx Impedance	1 MΩ		
Baud Rate	57600		
Built-In Test Equipment (BITE) Output (Pin 6)			
Format	CMOS 0V to 3V		
Load Impedance	1 ΜΩ		
Logic	0= Normal operation 1= Alarm		
Power Input (Pin 5)			
Operating	≤295 mW		
Warmup	<850 mW		
Input Voltage (Vcc)	3.3 ±0.1 VDc		
	t input voltage Vcc = 3.3 Vbc and ambient temperature		

¹At input voltage Vcc = 3.3 Vbc and ambient temperature = 25 °C, unless otherwise specified.

Performance Parameters

Specification	Details
Time to Lock	<180s
Digital Tuning	Range: $\pm 1 \times 10^{-6}$ Resolution: 1 × 10 ⁻¹²
Maximum Offset at Shipment	±5 × 10 ⁻¹¹
Maximum Retrace (48 hrs Off)	$\pm 5 \times 10^{-10}$

Stability

Observation Time	ADEV
τ = 1 s	<3 × 10 ⁻¹¹
τ = 10 s	<5 × 10 ⁻¹¹
τ = 100 s	<3 × 10 ⁻¹¹

Frequency Drift ²		
Monthly Rate	<9 × 10 ⁻¹⁰	
Yearly Rate	<1 × 10 ⁻⁸	

²Typical after 30 days of continuous operation.

Offset	Phase Noise (SSB)
f = 1 Hz	<-85 dBc/Hz
f = 10 Hz	<-120 dBc/Hz
f = 100 Hz	<-140 dBc/Hz
f = 1 kHz	<-145 dBc/Hz
f = 10 kHz	<-150 dBc/Hz
f = 100 kHz	<-155 dBc/Hz



Environmental

Operating Temperature ⁴	-40°C to +80°C
TempCo ^{3,4} -	
Total Sensitivity of Frequency to Temperature over specified range	$\pm 3 \times 10^{-10}$
Total Sensitivity of Frequency to Voltage over specified range	$\pm 4 \times 10^{-10}$
Magnetic sensitivity (≤2.0 Gauss)	±9 × 10 ⁻¹¹ /Gauss
Radiated Emissions	Compliant to FCC part 15, Class B
Vibration	Maintains lock under MIL- STD-810G, Operational, 7.7 grms per Figure 514.7E-1. Category 24
Humidity	0%–95% RH per MIL-STD-810, Method 507.5
Non-Operating (Stor	age and Transport)
Temperature	–55°C to +105°C
Vibration	MIL-STD-810, Method 514.6, Figure 514.6E-1, 7.7 grms (General Minimum Integrity Exposure)
Shock	MIL-STD-202, 30g, half sine, 11 ms

Physical

Specification	Details
Weight	<85 g
Size	2.0" × 2.0" × 0.5"
	(51 × 51 × 12.7 mm)
MTBF	>100,000 hours

³ Maximum Rate of Change 0.5°C per Minute

⁴ Option -002

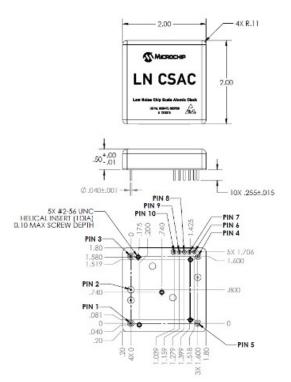
Ordering Information

Part Number	Description	ТетрСо	Temp Range
090-04018-001	LN-CSAC - (SA65-LN, base)	$\pm 5 \times 10^{-10}$	-10°C to +65°C
090-04018-002	LN-CSAC - (SA65-LN, wide temp. option)	$\pm 3 \times 10^{-10}$	-40°C to +80°C

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Pinout Definition

Pin Number	Function
1	N/C
2	GND
3	10 MHz SINE OUT
4	GND
5	Input Supply
6	BITE
7	TXD
8	RXD
9	1 PPS IN
10	1 PPS OUT