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VD55G0

Datasheet

Advanced 644 x 604 pixel, backside illuminated global shutter, ultra compact sensor, with high QE, high MTF, excellent PLS, and full-features

Order code	Description
VD55G0CCA1/RW	Bare die

Application
Engineered for high-performance computer vision applications, including AR/VR, personal and industrial robotics, drones, barcodes, biometrics and gestures, embedded vision or scene recognition. Typical use cases where high-performance near IR sensing is key. Demanding computer vision on scene with movement requiring no shutter artifacts.

Features

- Global shutter technology, STMicroelectronics proprietary single layer
- 3D stacked sensor 40 nm/65 nm
- 2.61 µm x 2.61 µm BSI pixel with full CDTI (capacitive deep trench)
- High performance with excellent
  - QE (quantum efficiency)
  - MTF (modulation transfer function) up to near IR
  - Perfect PLS (shutter efficiency)
- Smallest sensor on market with:
  - Compact die size: 2.6 mm x 2.5 mm
  - 640 pixel x 600 pixel resolution
  - Very small pixel array, 1.67 mm x 1.57 mm
  - Optical format between 1/9 inch
- Operating junction temperature: -30°C to 85°C
- Single lane transmitter MIPI CSI-2 (copyright© 2005-2010 MIPI Alliance, Inc. Standard for camera serial interface 2 (CSI-2) version 1.0) version 1.3, 1.2 Gbps per lane
- Fast mode+ I²C control interface
- Integrated temperature sensor
- Up to 210 fps (frames per second) at full resolution and 260 fps with VGA resolution
- Programmable sequences of 4-frame contexts, including frame parameters
- Automatic dark calibration
- Dynamic defective correction
- Embedded auto-exposure
- 4 multiple function IO, dynamically programmable with frame contexts (GPIO, strobe pulse, pulse-width modulation, V sync)
- Up to 4 illumination control outputs, synchronized with sensor integration periods and leader or follower external frame start
- Mirror/flip readout
- Fully sequenceable with frame contexts
- Crop
- Binning (x2 and x4)
- Analog binning: 320x240 @ 500 fps, 320x252 @ 480 fps, 320x300 @ 414 fps
- Subsampling (x2 and x4)

Description

The VD55G0 is a global shutter image sensor with high BSI performance which captures up to 210 frames per second in a 644 x 604 resolution format. The pixel construction of this device minimizes crosstalk while enabling a high quantum efficiency (QE) in the near infrared spectrum.

1 Acronyms and abbreviations

Table 1. Acronyms and abbreviations

Acronym/abbreviation	Definition
BSI	backside illumination
CCI	camera control interface
CP	charge pump
CPU	central processing unit
CRA	chief ray angle
CSI	camera serial interface
DTI	deep trend isolation
EMI	electromagnetic interference
EMC	electromagnetic compatibility
EXTCLK	external clock
FoV	field of view
FPN	fixed pattern noise
fps	frames per second
GPIO	general-purpose input/output
I²C	inter-integrated circuit (bus)
IP	intellectual property
ISL	intelligent status line
ISP	image signal processor
LDO	low dropout regulator
LP	low power
MIPI	mobile industry processor interface
OIF	output interface
OTP	one-time programmable
QE	quantum efficiency
PHY	physical layer
PLS	photo light sensitivity
PWM	pulse-width modulation
STBY	standby
SW	software

2 Overview

Table 2. Technical specifications

Feature		Detail
Pixel resolution		644 x 604 (including four borders)
Sensor technology		3D stacked
Pixel size		2.61 µm x 2.61 µm
Analog gain		x1–x8
Power consumption	60 fps	55 mW
	30 fps	35 mW
	10 fps	14 mW
Junction temperature range (Tj)		-30°C to 85°C functional
Shutter		Global
Package option		Bare die
Frame rate at full resolution		185 fps
CSI-2 serial interface data rate		Up to 1.2 Gbps
Pixel output format		RAW10 and RAW8
Supply voltages		2.8 V analog supply 1.8 V digital – IO supply 1.15 V digital – core supply
Temperature sensor accuracy		±3°C in range -30°C to 85°C
External clock frequency range		6 MHz – 27 MHz
Frame synchronization		Internal, external I²C, external hardware

3 Functional description

3.1 Interfaces

3.1.1 Inter-integrated circuit (I²C)

The VD55G0 is configured and controlled via an I²C interface. It operates in either Fast mode (up to 400 kHz) or Fast+ mode (up to 1 MHz) at 1.8 V. After the CPU boot sequence, the default I²C configuration is fast mode plus with a sink capability set to 20 mA. Drive capability can be decreased to 4 mA (fast mode) by writing a dedicated register once the system has booted.

Device addressing uses a CCI protocol with 2-byte subaddresses.

The default sensor address, 0x20 (including R/W bit), can be overridden:

- Permanently if a non-null value is stored in the OTP dedicated register
- Dynamically with a CPU command when the CPU state is SW STBY

3.1.2 Camera serial interface (CSI)

The sensor is ready to connect via a single lane mobile industry processor interface (MIPI) CSI-2 serial interface. The single lane MIPI CSI-2 serial interface supports up to 1.2 Gbps. Resolution is scalable between RAW8 and RAW10.

3.2 Power supplies

The power supplies required by the sensor are:

- 2.8 V for the analog blocks
- 1.8 V for the digital I/Os
- 1.15 V for the core digital logic and MIPI CSI-2 output drivers

The pixel array requires different positive and negative voltages, all internally generated by charge pumps and regulators. Two voltage references, internally generated, need external decoupling capacitors.

The internal CPU handles the entire power management of the sensor to guarantee the lowest power consumption at any given time.

3.3 Clock

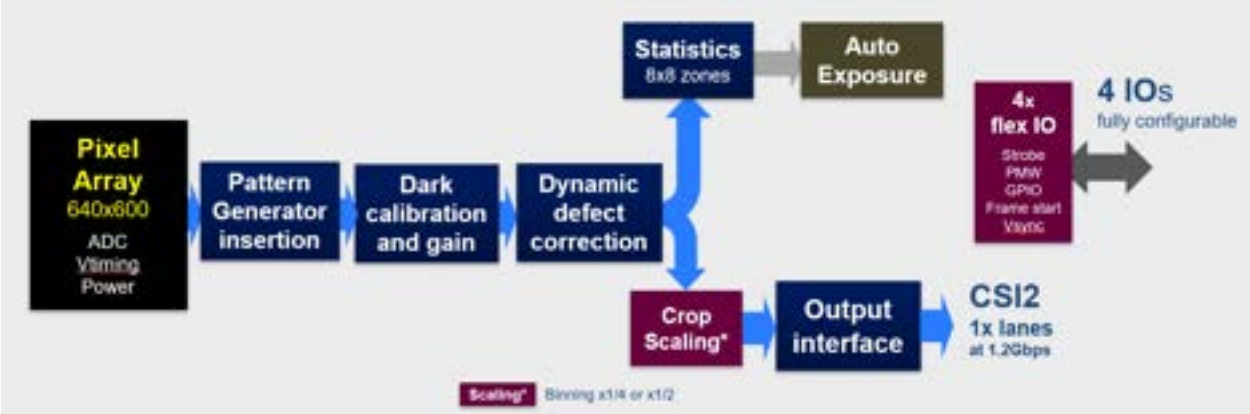
An input clock is required from an external digital clock source in the range of 6 MHz to 27 MHz.

3.4 Video pipe

The video pipe performs a number of functions designed to ensure an image of high quality. These functions include:

- Analog subsampling
- Pattern generation
- Defective pixel correction
- Dark calibration
- Auto exposure
- Digital binning
- Embedded status lines
- Output interface
- Context
- Crop

Figure 1. Video pipe



3.4.1 Pattern generation

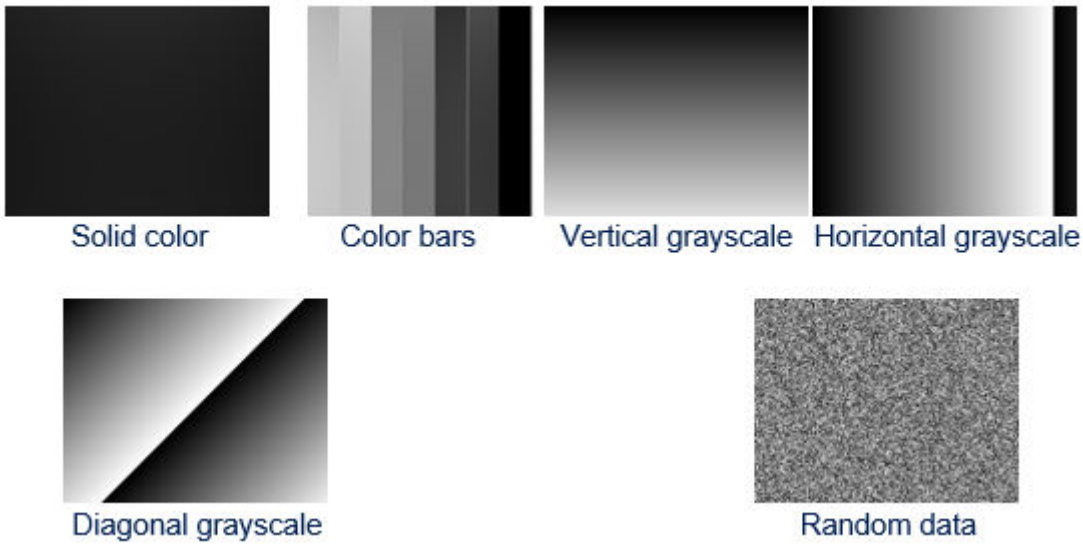
The pattern generation allows the insertion of digital patterns in the frame. Two modes are available:

- Whole or part of the active data is replaced with a pattern
- Dark lines are kept untouched

The available patterns are:

- Solid color
- Color bars
- Vertical grayscale
- Horizontal grayscale
- Diagonal grayscale
- Random data

Figure 2. Available patterns



3.4.2 Defective pixel correction

Active pixels are automatically corrected by a dynamic algorithm embedded in the sensor ISP. This mechanism can be deactivated for specific use cases such as structured light.

3.4.3 Dark calibration

A dark calibration is performed to extract the dark rows from the stream. Then, the dark noise level computed by this block is averaged and removed from the pixels in the active image.

A temporal smoothing and a sub bit dithering is applied to avoid a sudden one-code step.

Dark calibration implements a digital gain feature with a granularity of 1/256.

3.4.4 Auto exposure

The sensor integrates an auto exposure module to compute statistics on a given part of the active image. This module allows the exposure parameter to be changed accordingly.

3.4.5 Digital binning

The digital binning process reduces the image resolution by a factor of 2 or 4 in each direction. Digital binning is weighted to avoid special phase shift, an artifact which may occur on the output image.

3.4.6 Embedded status lines

The output interface (OIF) embeds the intelligent status line generator (ISLGEN) IP. This allows the metadata to be sent through the MIPI image data interface. Optionally, these data lines can be deactivated.

3.4.7 Output interface (OIF)

The OIF embeds a single data lane MIPI D-PHY interface. It supports up to 1.2 Gb/s of data. RAW10 and RAW8 data formats are supported over the CSI2-OIF.

The OIF can output a combination of the following:

- Intelligent status lines
- Frame data

3.4.8 Context

The sensor allows the configuration of up to four different rolling contexts. Contexts can be chained one to another in an ending or non-ending sequence.

3.4.9 Subsampling

The device supports x2 and x4 subsampling, which reduces overall image size and keeps the same field of view (FoV). Subsampling is applied vertically and horizontally during the ADC readout, where every two or every four pixels are read. When subsampling is used, the frame rate can be increased by decreasing the frame length.

Digital binning and subsampling are mutually exclusive.

3.4.10 Crop

The host can accurately choose which area of the whole pixel array it receives. This reduces traffic on the CSI interface and saves processing time.

3.5 Synchronization modes

The sensor has multiple synchronization modes:

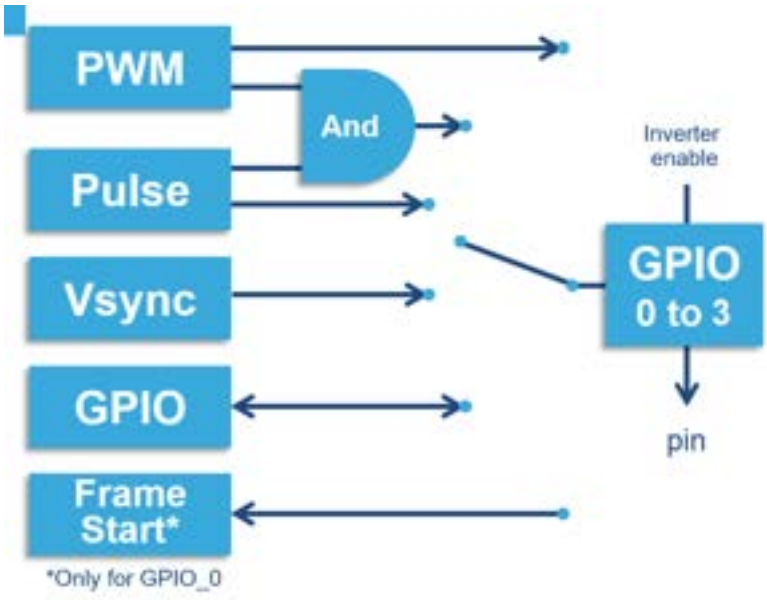
1. Leader mode
2. Follower mode:
   a. Using GPIO pulses
   b. Using I²C triggering commands

3.6 General purpose input/outputs (GPIOs)

The sensor provides four GPIOs:

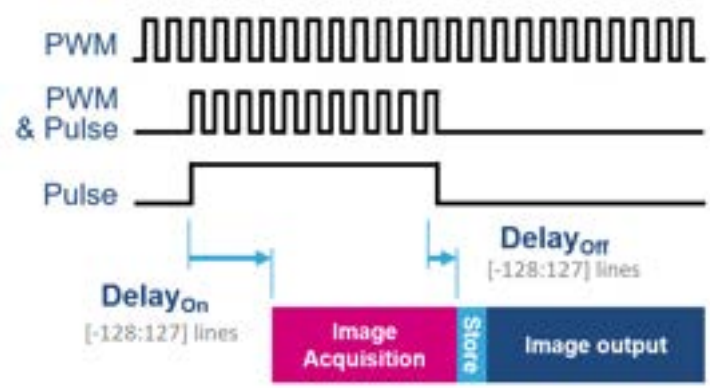
- GPIO0 is used as a frame start synchronization signal or as a generic GPIO if not used for this function
- GPIO[1-3] are used as strobe output, PWM output, VSYNC or as a generic GPIO as per the configuration

Figure 3. GPIO modes



All GPIO settings are fully configurable for the four context setups. Each output signal can be mapped to one or several of the GPIOs. All GPIOs have configurable polarity.

Figure 4. PWM and pulse overview



3.7 Use cases

Table 3. Functional use cases

Resolution	ADC resolution	
	9 bit	10 bit
644 x 604	210 fps	185 fps
640 x 560	225 fps	205 fps
VGA 640 x 480	260 fps	225 fps
QVGA 320 x 240	430 fps	390 fps
QQVGA 160 x 120	760 fps	600 fps
128 x 128	640 fps	580 fps

This global shutter pixel has full deep trend isolation (DTI) for ultra-low crosstalk, and high sensitivity.

VD55G0 product is designed to work in combination with a module/package with near infrared bandpass filter. For a use in monochromatic mode (no IR filter, visible domain), electrical performances are tested. For image quality performance, it is recommended the end users validate their own module and package performance (lens, FoV…).

4 Pin description and assignment

Table 4. Pin description table

Ball name	Type	Description	Reset state	Reference supply
Power supply				
VCORE	PWR	1.15 power supply for the digital core		1.15 V
VDDIO		1.8 V power supply for the digital core		1.8 V
VANA		2.8 V power supply for the digital core		2.8 V
DGND		Digital ground		VDDIO
AGND		Analog ground		VANA
Reference				
RCALIB	REF	Not connected		VCORE
VCPNEG_IN		Must be connected to VCPNEG_OUT		VANA
VCPNEG_OUT		Must be connected to VCPNEG_IN		
VCPPOS_IN		Must be connected to VCPPOS_OUT		
VCCPOS_OUT		Must be connected to VCPPOS_IN		
CSI-2 interface				
DATA1P, DATA1N	MIPI DPHY	CSI-2 data lane 1, positive and negative	Low	VCORE
CLKP, CLKN		CSI-2 clock, positive and negative		
Host interface				
XSHUTDOWN	I	Reset active low		VDDIO
SDA	IO	I²C data		
SCL	I	I²C clock		
GPIO0	IO	General purpose I/O and strobe light control	Low	
GPIO1				
GPIO2				
GPIO3				
CLKIN	I	Input clock		
Other pins				
PORTEST	I	Must be connected to digital ground		VDDIO
NC		Not connected		

Table 5. Pin coordinates

The pin coordinates (0, 0) are the die center

Pin number	Bonding point X coordinate	Bonding point Y coordinate	Net name
1	-1087.46	1144.4	DGND
2	-928.04	1144.4	VANA
3	-824.49	1144.4	AGND
4	-720.94	1144.4	VCORE
5	-617.39	1144.4	VCORE
6	-513.84	1144.4	DGND
7	-410.29	1144.4	VANA
8	-306.74	1144.4	AGND
9	-203.19	1144.4	VANA
10	-99.64	1144.4	AGND
11	3.91	1144.4	VANA
12	107.46	1144.4	AGND
13	211.01	1144.4	DGND
14	314.56	1144.4	DGND
15	418.11	1144.4	VCORE
16	595.08	1144.4	NC
17	698.63	1144.4	VDDIO
18	802.18	1144.4	PORTST
19	905.73	1144.4	NC
20	1076.96	1144.4	VCORE
21	1184.9	1045.38	SCL
22	1184.9	895.32	SDA
23	1184.9	772.31	DGND
24	1184.9	668.74	XSHUTDOWN
25	1184.9	565.16	VANA
26	1184.9	461.6	GPIO3
27	1184.9	358.03	DGND
28	1184.9	254.45	GPIO2
29	1184.9	150.88	GPIO1
30	1184.9	47.31	VCORE
31	1184.9	-56.25	VDDIO
32	1184.9	-159.83	DGND
33	1184.9	-263.39	VCORE
34	1184.9	-366.97	GPIO0
35	1184.9	-470.54	DGND
36	1184.9	-574.11	VCORE
37	1184.9	-677.68	CLKIN
38	1184.9	-781.25	DGND
39	1184.9	-884.82	DGND
40	1184.9	-1034.88	AGND

Pin number	Bonding point X coordinate	Bonding point Y coordinate	Net name
41	1087.46	-1144.4	VANA
42	937.38	-1144.4	VDDIO
43	833.82	-1144.4	VCORE
44	730.25	-1144.4	CLKN
45	626.68	-1144.4	CLKP
46	523.11	-1144.4	DGND
47	419.54	-1144.4	DATA1N
48	315.97	-1144.4	DATA1P
49	144.73	-1144.4	DGND
50	41.16	-1144.4	RCALIB
51	-62.41	-1144.4	AGND
52	-165.98	-1144.4	AGND
53	-269.55	-1144.4	VANA
54	-398.07	-1144.4	VANA
55	-501.64	-1144.4	NC
56	-605.22	-1144.4	VCORE
57	-708.78	-1144.4	NC
58	-812.36	-1144.4	NC
59	-915.93	-1144.4	NC
60	-1076.96	-1144.4	AGND
61	-1184.9	-1045.38	AGND
62	-1184.9	-152.41	VCPNEGIN
63	-1184.9	-48.84	VCPNEGOUT
64	-1184.9	54.73	DGND
65	-1184.9	158.3	AGND
66	-1184.9	261.87	VANA
67	-1184.9	365.44	VCORE
68	-1184.9	469	VCPPOSIN
69	-1184.9	572.58	VCPPOSOUT

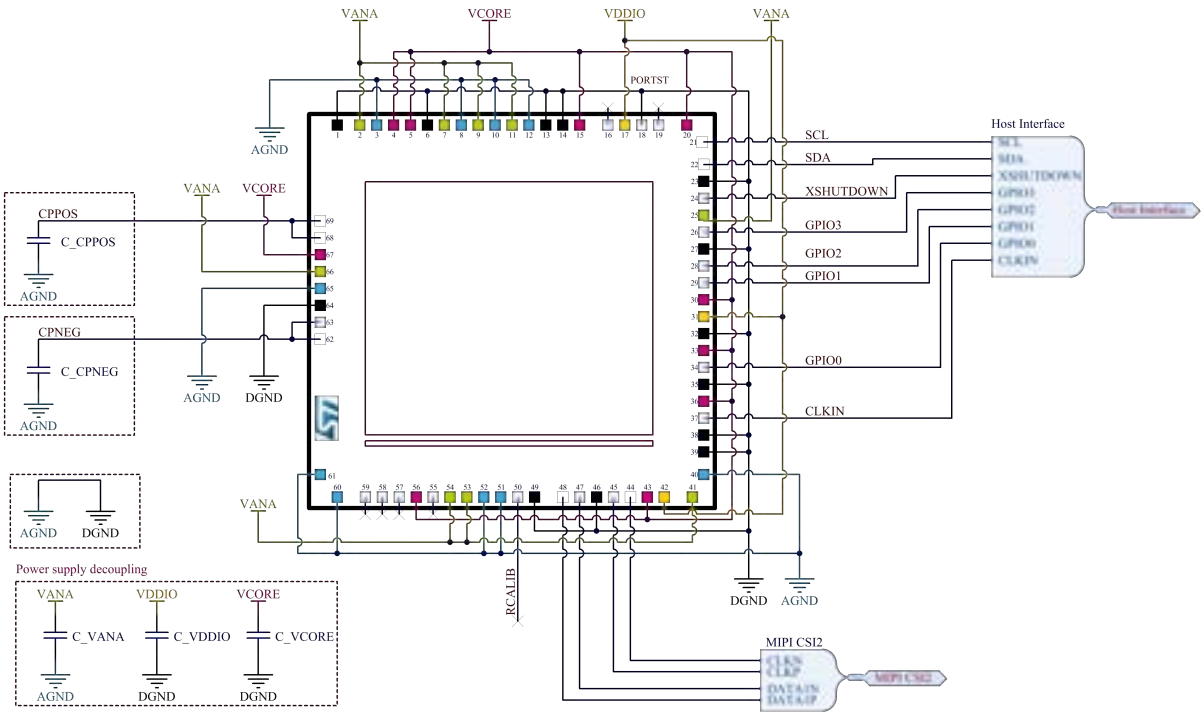
5 Application schematic

Capacitor values should be based on capacitor positions (embedded in the camera module or external to the camera module).

Table 6. Capacitor needs

Capacitor name	Associated pin name	Capacitor position	Typical voltage	Minimum capacitor	Typical capacitor	Maximum capacitor	Operating frequencies	Capacitor GND	Purpose
C_CPPOS	CPPOS_IN, CPPOS_OUT	Embedded	3.55 V	330 nF	470 nF	550 nF	160 MHz	AGND	CP tank capacitor
C_CPNEG	CPNEG_IN, CPNEG_OUT	Embedded	-2.0 V	1 µF	1.25 µF	1.5 µF	160 MHz	AGND	CP tank capacitor
C_VDDIO	VDDIO	Embedded	1.8 V				1 MHZ	DGND	Supply decoupling
		External			1 µF				
C_VCORE	VCORE	Embedded	1.15 V		470 nF		800 MHz 1 GHz - 1.2 GHz 160 MHz - 200 MHz	DGND	Supply decoupling
		External			1 µF				
C_VANA	VANA	Embedded	2.8 V		100 nF		160 MHz	AGND	Supply decoupling
		External			1 µF				

Figure 5. Typical electric schematic



6 Die specification

In the table below, the die dimensions are after sawing. The optical center is with the die center as reference.

Table 7. Die size after sawing

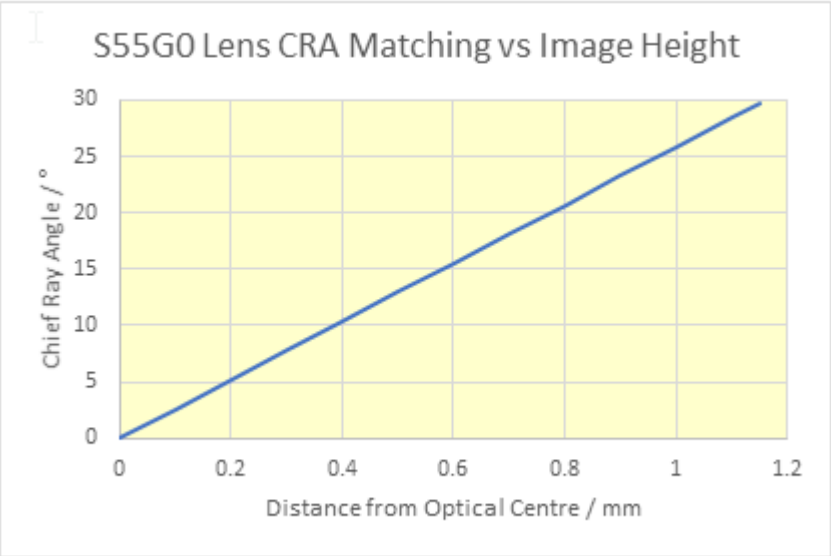
Description	Min.	Typical	Max.	Unit
X die (after sawing)	2574	2584	2594	µm
Y die (after sawing)	2493	2503	2513	µm
Die thickness	143	150	157	µm

Table 8. Optical center

Description	X	Y
Optical center	0.0	0.0

7 Chief ray angle (CRA)

Figure 6. **Chief ray angle**



8 Electrical characteristics

The electrical characteristics have been measured under the following conditions:

- Full resolution (644 x 604 pixels)
- Nominal power supply levels
- External clock at 12 MHz
- 185 fps
- 10 bits/pixel
- 1200 Mbits/s on MIPI interface
- 60°C

8.1 Operating conditions

Table 9. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDIO	Digital IO power supply	1.7	1.8	1.9	V
VANA	Analog power supply	2.7	2.8	2.9	V
VCORE	Digital core power supply	1.1	1.15	1.26	V
VIO	IO referenced to VDDIO	-0.3	VDDIO	VDDIO + 0.5	V
Temperature					
T JF	Junction temperature (functional operation)	-30		85	°C

8.2 Power consumption

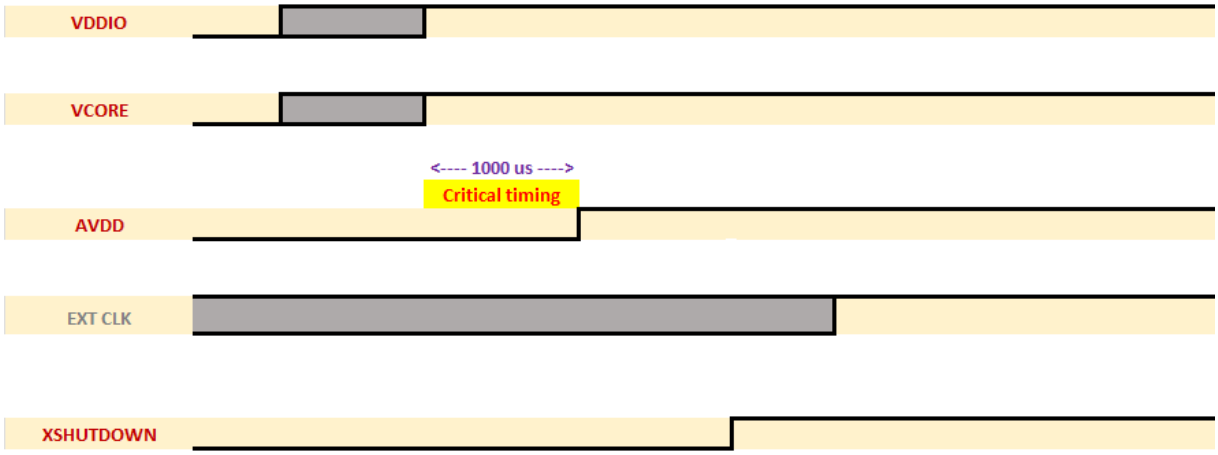
Table 10. Power consumption

State	VDDIO		VCORE		VANA		Unit
	Typ.	Max.	Typ.	Max.	Typ.	Max.	
Streaming	0.25	0.5	46	61	17.3	21	mA
SW_STANDBY	0.0062	0.04	1.75	8	0.092	0.3	
HW_STANDBY	0.00135	0.04	0.5	7	0.28	0.5	

8.3 Powerup sequence

- VDDIO and DVDD can be raised in any order but this must be done before AVDD
- Wait at least 1000 µs after VDDIO and VCORE are established before raising the AVDD
- EXT CLOCK can be supplied at any moment
- XSHUTDOWN must be released after AVDD
- Power supplies are considered established when they are above the minimum value required by the datasheet
- AVDD is considered down when it is below 20% of the minimum value targeted by the datasheet

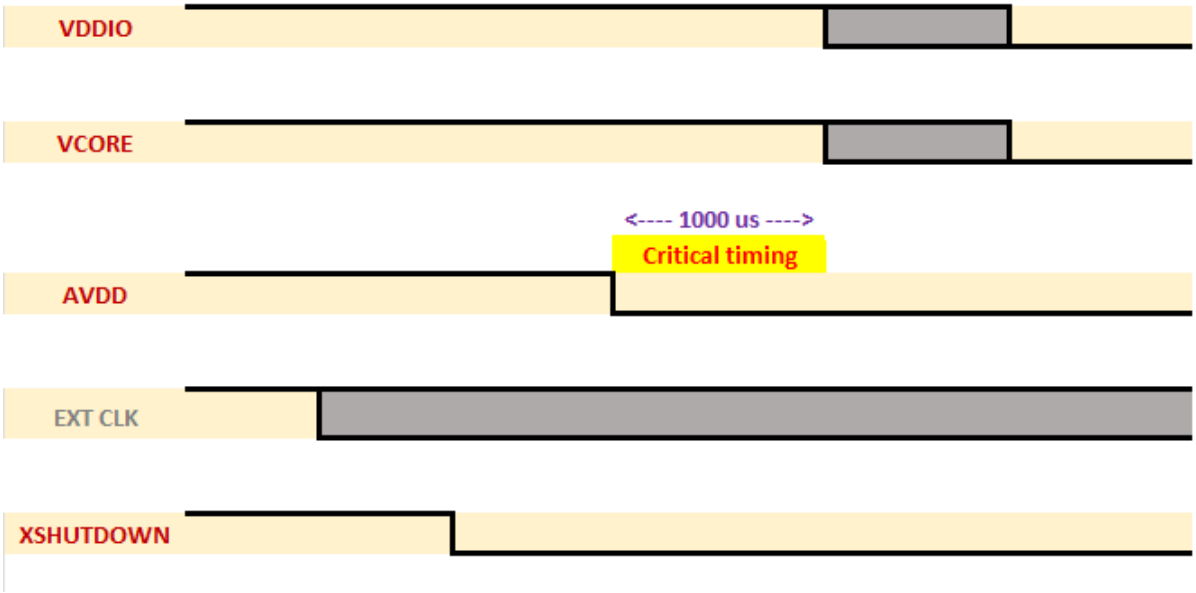
Figure 7. Powerup sequence



8.4 Powerdown sequence

- VDDIO and DVDD can be shut down in any order after AVDD
- AVDD must be shut down at least 1000 µs before VDDIO and DVDD are shut down
- EXT CLOCK can be shut down at any moment
- XSHUTDOWN must be stopped before AVDD
- Power supplies are considered established when they are above the minimum value required by the datasheet
- AVDD is considered down when it is below 20% of the minimum value targeted by the datasheet

Figure 8. Powerdown sequence



8.5 Inrush current

The transient characterization is done at Vnom/Tnom.

Figure 9. Release of the shutdown

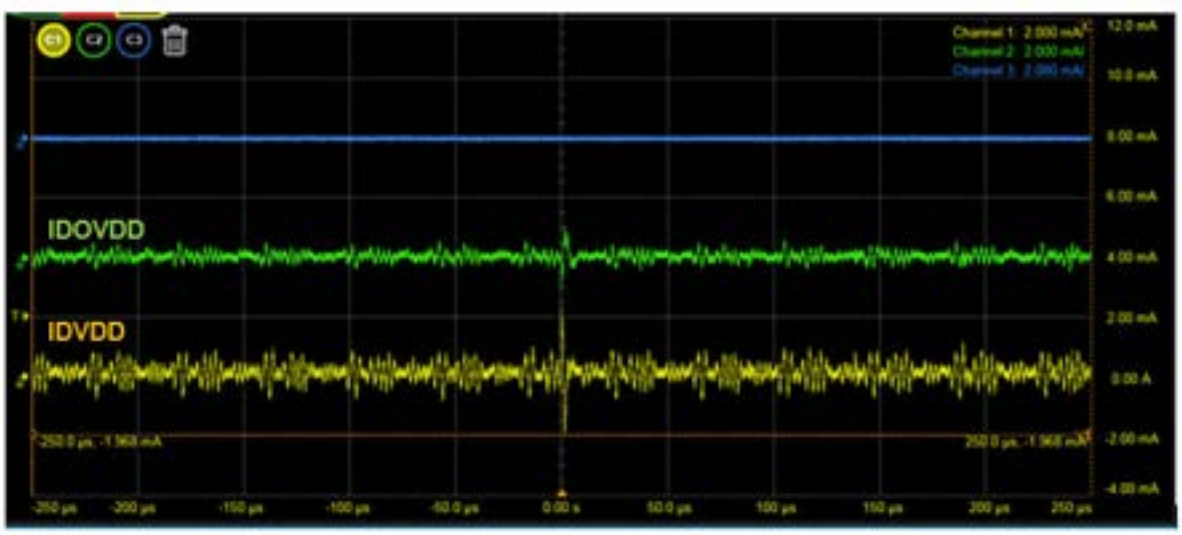


Table 11. Overshoot/Undershoot of the DVDD at the release of shutdown

Supply	Overshoot/Undershoot
DVDD	2.29 mA/-1.96 mA

Figure 10. Start streaming

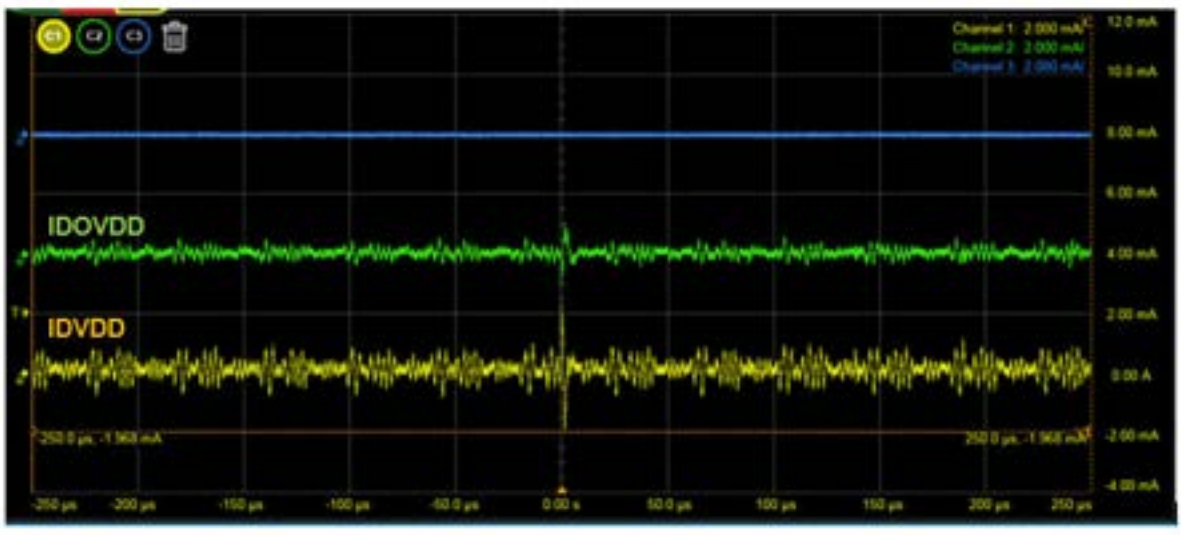


Table 12. Overshoot of the VDDIO and DVDD at the start of the stream

Supply	Overshoot
VDDIO	6.53 mA
DVDD	38 mA

8.6 AC ripples

Table 13. AC ripples

Supply	AC ripple (mV)	Frequency range
AVDD	10	Up to 10 MHz
DVDD	20	
VDDIO	10	

8.7 EXTCLK input

Table 14. EXTCLK input

Symbol	Parameter	Min.	Max.	Unit
$V_{EXTCLKL}$	DC-coupled square wave low-level input	-0.3	0.35 x VDDIO	V
$V_{EXTCLKH}$	DC-coupled square wave high-level input	0.65 x VDDIO	VDDIO + 0.3	
f_{EXTCLK}	Clock input frequency	6	27	MHz
C to Cjitter	Clock maximum cycle to cycle jitter	—	200	ps
Duty cycle	Clock duty cycle	45	55	%
I_{EXTCLK}	Input leakage current	—	10	µA
twl	Low level width	16.67	91.67	ns
twh	High level width	16.67	91.67	ns

8.8 Digital inputs and outputs

Table 15. Digital inputs

Symbol	Parameter	Min.	Max.	Unit
V_{IL}	Low-level input voltage	-0.5	0.3 x VDDIO	V
V_{IH}	High-level input voltage	0.7 x VDDIO	VDDIO + 0.5	
I_{Leak}	Input leakage current (1)	—	10	µA

1. *For 0 ≤ VI ≤ VDDIO*

Table 16. Digital outputs

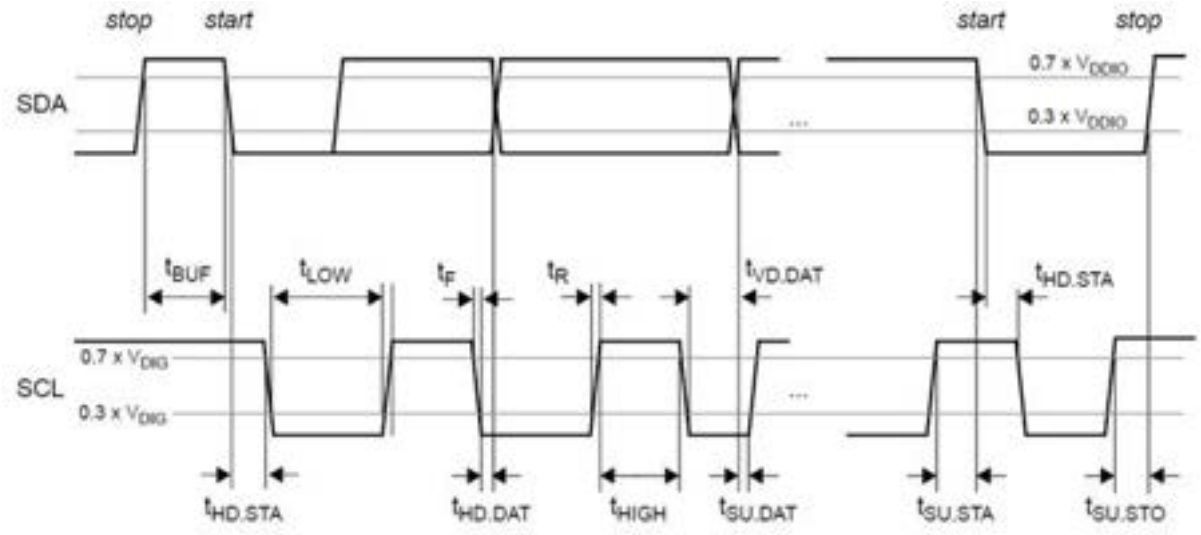
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Low-level output voltage	IOL = -4 mA		0.15	V
V_{OH}	High-level output voltage	IOH = 4 mA	VDDIO - 0.4	—	
I_{max}	Maximum current	—	—	4	mA

8.9 I²C interface - SDA, SCL

Table 17. I²C interface - SDA, SCL

Parameter	Symbol	Fast mode		Fast mode plus		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	t_{SCL}	0	400	0	1000	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD.STA}$	0.6	—	0.26	—	µs
LOW period of the SCL clock	t_{LOW}	1.3	—	0.5	—	
HIGH period of the SCL clock	t_{HIGH}	0.6	—	0.26	—	
Setup time for a repeated START condition	$t_{SU.STA}$	0.6	—	0.26	—	
Data hold time	$t_{HD.DAT}$	0	—	0	—	
Data setup time	$t_{SU.DAT}$	100	—	50	—	ns
Rise time of both SDA and SCL	t_R	20	300	—	120	
Fall time of both SDA and SCL	t_F	20 x (VDD/5.5 V)	300	15 x (VDD/5.5 V)	120	
Setup time for STOP condition	$t_{SU.STO}$	0.6	—	0.26	—	µs
Bus free time between a STOP and START condition	t_{BUF}	1.3	—	0.5	—	
Capacity load for each bus line	C_O	—	400	—	550	pF
Data valid time	$t_{VD.DAT}$	—	0.9	—	0.45	µs
Data valid acknowledge time	$t_{VD.ACK}$	—	0.9	—	0.45	
Noise margin at LOW level for each connected device (including hysteresis)	V_{nL}	0.054 x VDD	—	0.054 x VDD	—	V
Noise margin at HIGH level for each connected device (including hysteresis)	V_{nH}	0.054 x VDD	—	0.054 x VDD	—	

Figure 11. I²C interface timing



8.10 CSI-2 interface

8.10.1 DC specifications

The DC specifications are characterized, not tested.

Table 18. CSI-2 interface, High-speed mode, DC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CMTX}	HS transmits static common-mode voltage	150	200	250	mV
V_{OD}	HS transmits differential voltage (1)	140	200	270	
V_{OHHS}	HS outputs high voltage (1)	—	—	360	
Z_{OS}	Single-ended output impedance	40	50	62.5	Ω

1. *Value when driving into load impedance anywhere in the ZID range (80-125 Ω)*

Table 19. CSI-2 interface, Low-power mode, DC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OH}	Output high-level	1.1	1.2	1.3	V
V_{OL}	Output low-level	-50	—	50	mV
Z_{OLP}	Output impedance of LP transmitter	110	—	—	Ω

8.10.2 AC specifications

Table 20. CSI-2 interface, High-speed mode, AC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
—	Data rate	—	804	—	Mbit/s
t_{clkp}	Average data period	—	1.25	—	ns
t_r and t_f	t_f 20% - 80% rise time and fall time	100	—	0.3UI	ps
t_{skew}	Data-to-clock skew	-0.15UI	—	0.15UI	—

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 Sawn die information

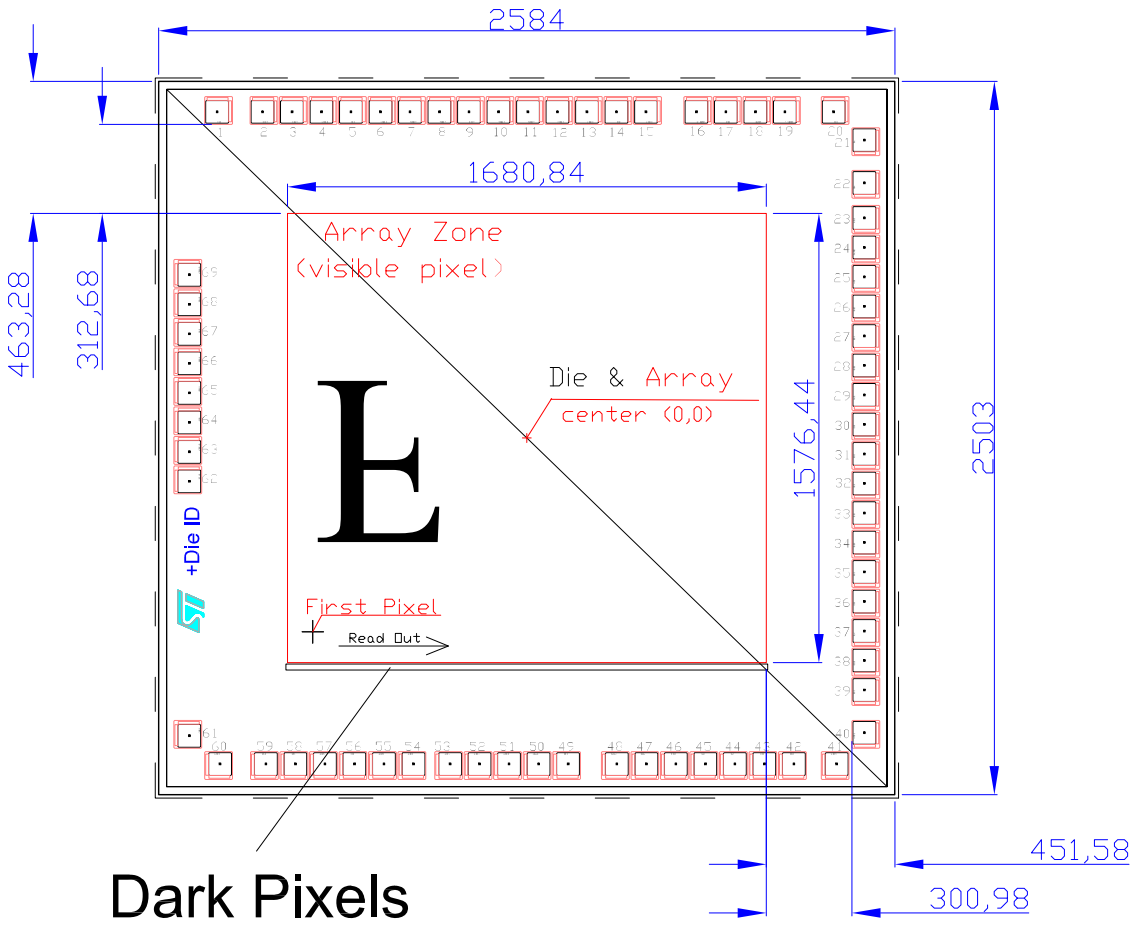
The tested die is delivered as a sawn die reconstructed into a 100% yield wafer format on blue or UV-tape, and delivered on a metallic ring.

The frames are packed in plastic containers, each including a maximum of 13 double-spaced reconstructed wafer rings.

ST uses various package labels with its reconstructed wafer shipments:

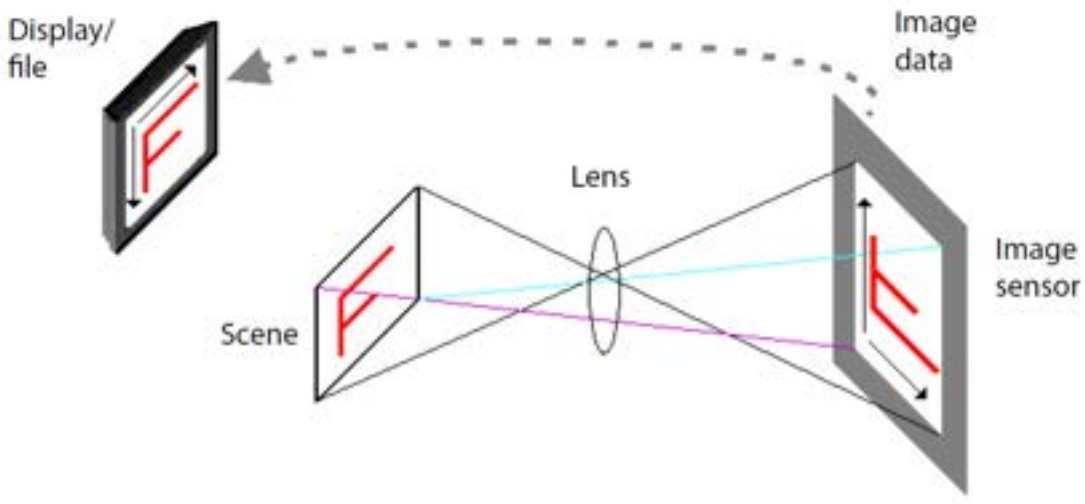
- Labels on RW frames
- Labels on carrier boxes

Figure 12. Sawn die information



Note: Sawn die size = -10 µm

Figure 13. **Image orientation**



This document is related to the die so the image orientation (depicted in this document with an “F” symbol) shows the image as it is captured by the sensor.

The pixel readout is fully programmable (x and y flip) but the default read fashion is from right to left and top to bottom as shown in Figure 13. Image orientation. This is illustrated by the “F” symbol orientation.

10 PNPID

STMicroelectronics is registered as SMO in the PNPID registry since 14th June 2007. The PNPID for the VD55G0 sensor is SMO55F0.

11 Ordering information

Table 21. **Order codes**

Order code	Description
VD55G0CCA1/RW	Bare die

Revision history

Table 22. **Document revision history**

Date	Version	Changes
16-Apr-2024	10	First public release.

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