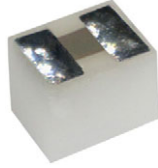


AEC-Q200 Qualified High Frequency 70 GHz Thin Film Chip Resistor



FEATURES

- Operating frequency 70 GHz
- AEC-Q200 qualified
- Thin film microwave resistors
- Ohmic range: 10 Ω to 500 Ω
- Design kits available
- Modelithics® library available
- Small internal reactance (LC down to 1×10^{-24})
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
GREEN
(5-2008)

LINKS TO ADDITIONAL RESOURCES



3D Models



S-Parameters



Simulation Tools



Application Notes



Capabilities and Custom Options



Did You Know?



Infographics



Why It Matters

Those miniaturized components are designed in such a way that their internal reactance is very small. When correctly mounted and utilized, they function as almost pure resistors on a very large range of frequency, up to 70 GHz from 10 Ω to 500 Ω.

STANDARD ELECTRICAL SPECIFICATIONS

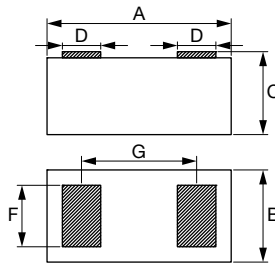
MODEL	SIZE	RESISTANCE RANGE Ω	RATED POWER Pn ⁽¹⁾ W	LIMITING ELEMENT VOLTAGE V	TOLERANCE ± %	TEMPERATURE COEFFICIENT ± ppm/°C
CHA02016	02016	10 to < 50	0.030	30	5	100 (50 upon request)
CHA02016	02016	50 to ≤ 500	0.030	30	2, 5	100 (50 upon request)
CHA02016	02016	50 and 100	0.030	30	1, 2, 5	100 (50 upon request)

Note

⁽¹⁾ PCB mounting with +70 °C ambient temperature

DIMENSIONS in millimeters (inches)

CHA02016 F



CASE SIZE MODEL / TERMINATION	DIMENSIONS						
	± 0.10 (± 0.004)	± 0.10 (± 0.004)	± 0.127 (± 0.005)	D		± 0.050 (± 0.002)	± 0.050 (± 0.002)
				E when applicable MIN.	MAX.		
CHA02016	0.480 (0.020)	0.390 (0.016)	0.420 (0.016) ⁽¹⁾	0.110 (0.004)	0.150 (0.006)	0.260 (0.010)	0.300 (0.012)

Note

⁽¹⁾ ± 0.070 (± 0.003)

LAND PATTERN FOR F “FLIP CHIP” TERMINATIONS in millimeters (inches)			
CHIP SIZE	Z_{max.}	X_{max.}	G_{min.}
02016	0.53 (0.021)	0.44 (0.017)	0.15 (0.006)

Note

- Suggested land pattern: according to IPC-7351

PERFORMANCE (CHA02016 F/P TERMINATION)

TEST PROCEDURES AND REQUIREMENTS				
AEC-Q200 CLAUSE	TEST	PROCEDURE	GLOBAL PERFORMANCES	TYPICAL PERFORMANCES (25 Ω TO 250 Ω)
3	High temperature exposure	MIL-STD-202 method 108 1000 h at T = 125 °C, unpowered	± 2 % ± 0.05 Ω	± 0.2 % ± 0.05 Ω
4	Temperature cycling	JESD22 method JA-104 1000 cycles (-55 °C to +155 °C)	± 1.8 % ± 0.05 Ω	± 1.5 % ± 0.05 Ω
7	Biased humidity	MIL-STD-202 method 103 1000 h 85 °C / 85 % RH 10 % of operating power	± 2 % ± 0.05 Ω	± 0.75 % ± 0.05 Ω
8	Operational life	MIL-STD-202 method 108 condition D steady state T = 125 °C at rated power 90' on / 30' off / 1000 h	± 2.5 % ± 0.05 Ω	± 1 % ± 0.05 Ω
13	Mechanical shock	MIL-STD-202 method 213 condition C 100 g/6 ms 3.75 m/s 3 shock/direction, 2 directions along 3 axes (18 shocks)	± 0.05 % ± 0.05 Ω	± 0.015 % ± 0.05 Ω
14	Vibration	MIL-STD-202 method 204 5 g for 20 min, 12 cycles each of 3 orientations Test from 10 Hz to 2000 Hz	± 0.1 % ± 0.05 Ω	± 0.05 % ± 0.05 Ω
15	Resistance to soldering heat	MIL-STD-202 method 210 condition D Flux used: alpha 611 Solder temp.: 260 °C ± 5 °C Total immersion during 10 s	± 2.5 % ± 0.05 Ω	± 0.5 % ± 0.05 Ω
17	ESD	AEC-Q200-002	Classification 1C 1000 V _{DC} to 2000 V _{DC}	
18	Solderability	J-STD-002 - Preconditioning 4 h dry heat aging and 235 °C SnPb 5 s - 215 °C SnPb 5 s - 260 °C SnAgCu 10 s	Good tinning (≥ 95 % covered) No visible damage	
20	Flammability	UL 94	Class V-0 No burning	
21	Board flex	AEC-Q200-005	± 0.1 % ± 0.05 Ω	± 0.05 % ± 0.05 Ω
24	Flame retardance	AEC-Q200-001	No flame, no explosion, no temperature higher than 350 °C	



PREFERRED MODELS AND VALUES

Recommended Values:

10 Ω / 18 Ω / 25 Ω / 50 Ω / 75 Ω / 100 Ω / 150 Ω / 180 Ω / 200 Ω / 250 Ω / 330 Ω / 500 Ω

Those values are available with a **MOQ of 100 pieces.**

Other values can be ordered upon request, but higher MOQ will apply: 1000 pieces for CHA02016.

Recommended termination:

F

Recommended tolerance:

2 %

DESIGN KITS

Design kits are available ex stock in CHA02016. There are 20 pieces per recommended value. F termination.

5 % tolerance.

Those kits are packaged in pieces of tape and delivered in ESD bags.

TEST BOARDS

TRL (Thru Reflect Line) and DUT (Device Under Test) evaluation boards (50 Ω or 100 Ω) are available on request.

PACKAGING

Standard packaging is plastic tape and reel for all sizes.

Flip chip:

Tin / silver terminations (F termination option): Active face down in tape and reel.

Active face up in waffle pack.

One face:

Gold terminations (P termination option): Active face up.

Please use M termination code for active face down in tape and reel.

Notes

- CHA02016 with active face down in tape and reel have back-side blue marked to indicate right orientation
- Please refer to Vishay Sfernice Application Note "[Guidelines for Vishay Sfernice Resistive and Inductive Components](#)" for soldering recommendation (document number 52029, section "3. Guidelines for Surface Mounting Components (SMD)", profile number 3 applies

SIZE	MOQ	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
		WAFFLE PACK 2" x 2"	TAPE AND REEL		
			MIN.	MAX.	
02016	See MOQ mentioned on preferred models and values	484	100	5000	8 mm

PACKAGING RULES

Waffle Pack

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover. To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: please consult Vishay Sfernice for specific ordering code.

Tape and Reel

See Part Numbering information to get the quantity desired by tape.

In regard to the CHA02016 size only, up to 5 empty cavities can be found every 1000 parts in the reel. Nevertheless, the number of requested parts will be respected.

GLOBAL PART NUMBER INFORMATION

Part Number Example: CHA02016-100RGFTF (AEC-Q200 qualified CH series, 100 Ω, 2 % tolerance, 5000 pieces reels)

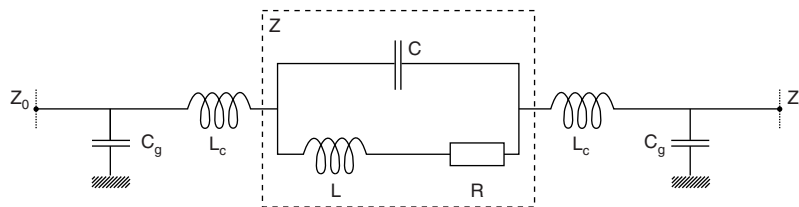
C	H	A	0	2	0	1	6	-	1	0	0	R	G	F	T	F
GLOBAL MODEL CHA			SIZE 02016		OHMIC VALUE 10R to 500R			TOLERANCE F = 1 % G = 2 % J = 5 %			TERMINATION F (flip chip): SnAg over nickel barrier P (one face) ⁽¹⁾ : gold bonding pads M (one face): gold bonding pads with active face down in tape and reel			PACKAGING For more information see "Codification of Packaging" table		

CHKIT Part Numbers: CHAKIT-02016
Note

(1) Gold termination for application in hermetic package: can also be mounted on PCB with SnAg solder paste

CODIFICATION OF PACKAGING

WAFFLE PACK	
W	100 min., 1 mult.; 100 pcs max.
PLASTIC TAPE	
T	100 min., 100 mult.; delivered in reels of 1000 pcs max.
TD	1000 min., 1000 mult.; delivered in reels of 1000 pcs
TF	5000 min., 5000 mult.; delivered in reels of 5000 pcs

TYPICAL HIGH FREQUENCY PERFORMANCE ELECTRICAL MODEL


C	Internal shunt capacitance
L	Internal inductance
R	Resistance
Z	Internal impedance (R, L, C)
L_c	External connection inductance
C_g	External capacitance to ground

The complex impedance of the chip resistor is given by the following equations:

$$Z = \frac{R + j\omega(L - R^2C - L^2C\omega^2)}{1 + C[(R^2C - 2L)\omega^2 + L^2C\omega^4]}$$

$$\frac{|Z|}{R} = \frac{1}{1 + C[(R^2C - 2L)\omega^2 + L^2C\omega^4]} \times \sqrt{1 + \left[\frac{\omega(L - R^2C - L^2C\omega^2)}{R}\right]^2}$$

$$\theta = \tan^{-1} \frac{\omega(L - R^2C - L^2C\omega^2)}{R}$$

Notes

- $\omega = 2 \times \pi \times f$
- f : frequency

R, L and C are relevant to the chip resistor itself.

L_c and C_g also depend on the way the chip resistor is mounted.

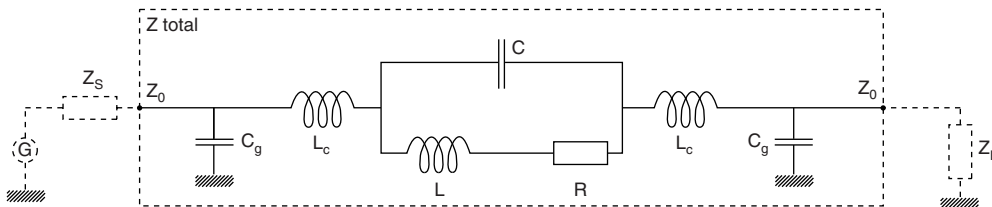
It is important to notice that after assembly the external reactance of L_c and C_g will be combined to internal reactance of L and C. This combination can upgrade or downgrade the HF behavior of the component.

This is why we are displaying three sets of data:

- $\frac{|Z|}{R}$ versus frequency curves which aim to show at a glance the intrinsic HF performance of a given chip resistor
- $\frac{|Z_{total}|}{R}$ versus frequency curves which aim to show the behavior of the chip resistor when mounted

These lines are terminated with adapted source and load impedance respectively Z_s and Z_l with $Z_0 = Z_L = Z_s$ (for others configurations please consult us).

Equivalent circuit for S-parameters:

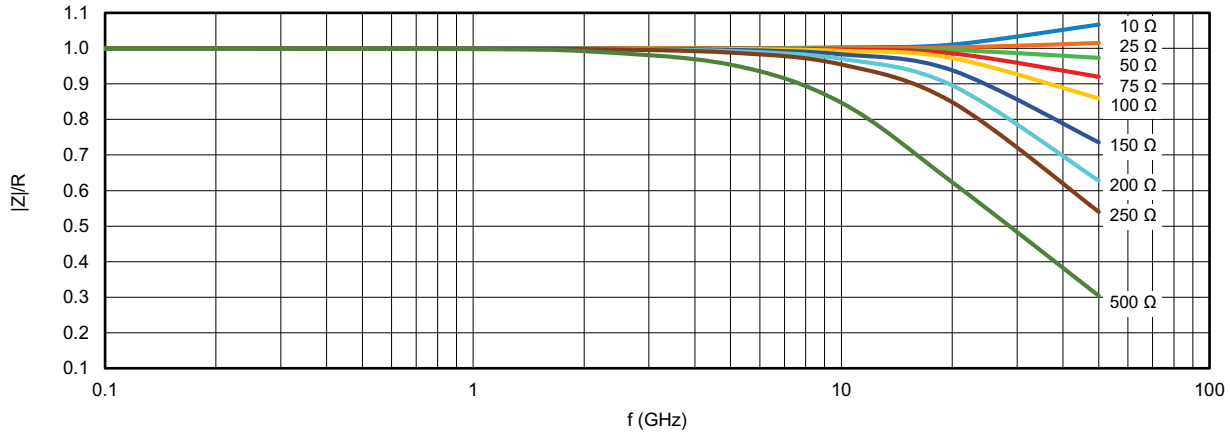


S-parameters are computed taking into account all the resistive, inductive and capacitive elements (Z_{total}) and $Z_0 = Z_L = Z_s = R$.

For simulation purposes, those S-parameter data are available for download here: www.vishay.com/doc?53061

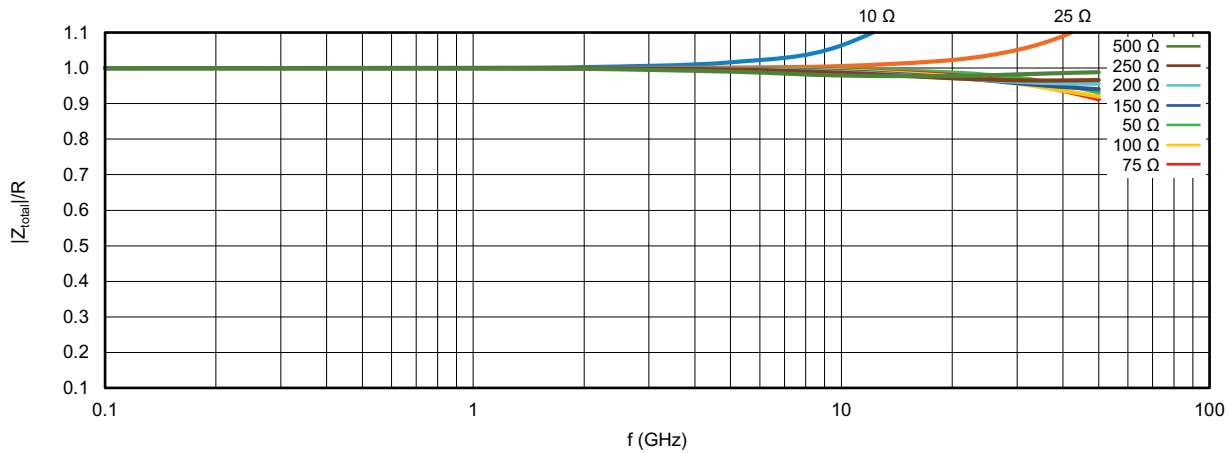


INTERNAL IMPEDANCE CURVES



Internal impedance curve for 02016 size (F and P terminations)

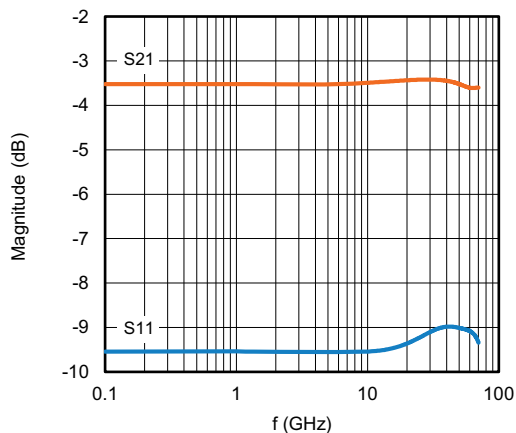
INTERNAL IMPEDANCE CURVES ($|Z_{TOTAL}| / R$)



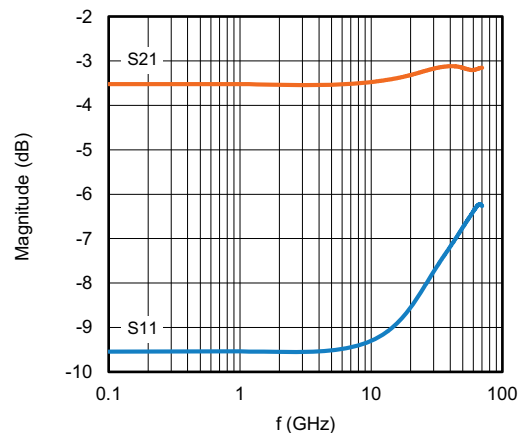
Internal impedance curve for 02016 size (F and P terminations)

S-PARAMETER

CHA02016 (F and P Terminations)



CHA02016 flip chip ($Z_0 = Z_1 = Z_s = R = 50 \Omega$)



CHA02016 flip chip ($Z_0 = Z_1 = Z_s = R = 100 \Omega$)



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Vishay products are not designed for use in life-saving or life-sustaining applications or any application in which the failure of the Vishay product could result in personal injury or death unless specifically qualified in writing by Vishay. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.