2-Mb parallel F-RAM with RADSTOP™ technology

128K × 16

Radiation performance

- Radiation data
  - Total dose:
    150 krad (50 rad(Si)/s)
    200 krad (10 rad(Si)/s)
  - Heavy-ion soft error rate immune up to 114 LET
  - Heavy-ion single event functional interrupt < 1.34×10^{-4} upsets/device-day (GEO - solar min)
  - Dose rate = 1.1×10^{8} rad(Si)/sec (dynamic)/1.1×10^{11} rad(Si)/sec (static)
  - Dose rate survivability (rad(Si)/sec) = 1.1×10^{11} rad(Si)/sec
  - Latch-up immunity = 96 MeV.cm^2/mg (115°C)
  - Neutron displacement > 5.0×10^{14} n/cm^2
- Prototyping options[1]
  - Non-qualified CYPT15B102N devices with same functional and timing characteristics in a 44-pin ceramic TSOP package

Features

- 2-Mbit ferroelectric random access memory (F-RAM) logically organized as 128K × 16
  - Configurable as 256K × 8 using $\overline{UB}$ and $\overline{LB}$
  - High-endurance 10 trillion (10^{13}) reads/writes
  - 121-year data retention (see **"Data retention and endurance"** on page 19)
  - Infineon instant non-volatile write technology
  - Page-mode operation for 30 ns cycle time
  - Advanced high-reliability ferroelectric process
- SRAM compatible
  - Industry-standard 128K × 16 SRAM pinout
  - 60 ns access time, 90 ns cycle time
- Advanced features
  - Software-programmable block write-protect
- Low power consumption (pre/post 150 krad TID radiation)
  - 20 mA/20 mA active current at 25 MHz
  - 700 µA/5 mA standby current
  - 20 µA/8 mA sleep mode current
- Low-voltage operation: V_{DD} = 2.0 V to 3.6 V
- Military temperature: –55°C to +125°C
- 44-pin ceramic TSOP package

Note
1. Data retention and endurance specifications are not guaranteed for prototype units.

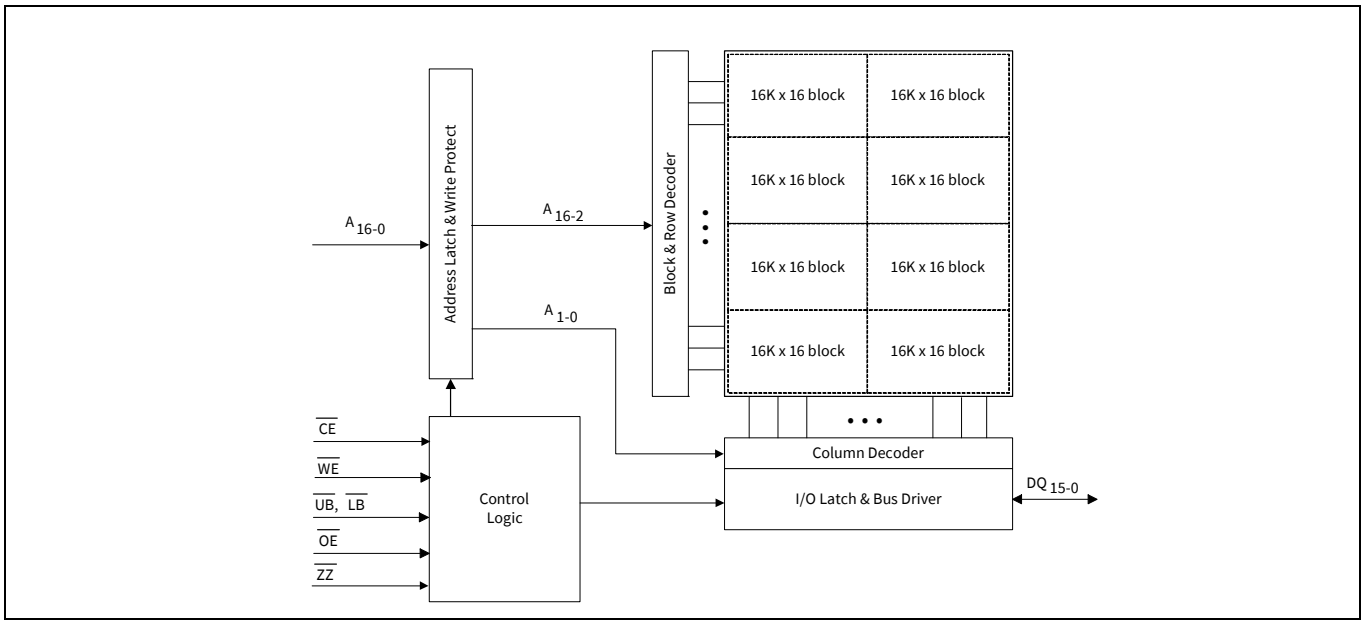
Functional description

The CYRS15B102N is a 128K × 16 non-volatile memory that reads and writes similar to a standard SRAM. A ferroelectric random access memory or F-RAM is non-volatile, which means that data is retained after power is removed. It provides data retention for over 121 years while eliminating the reliability concerns, system design complexities of EEPROM components. Fast write-timing and high write-endurance make the F-RAM superior to other types of memories.

The CYRS15B102N operation is similar to that of other RAM devices, and, therefore, it can be used as a drop-in replacement for a standard SRAM in a system. Read cycles may be triggered by $\overline{CE}$ or simply by changing the address and write cycles may be triggered by $\overline{CE}$ or $\overline{WE}$. The F-RAM memory is non-volatile due to its unique ferroelectric memory process. These features make the CYRS15B102N ideal for non-volatile memory applications requiring frequent or rapid writes.

The device is available in a 44-pin ceramic TSOP-II surface-mount package. Device specifications are guaranteed over the Military temperature range –55°C to +125°C.

Logic block diagram



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1 Pinout

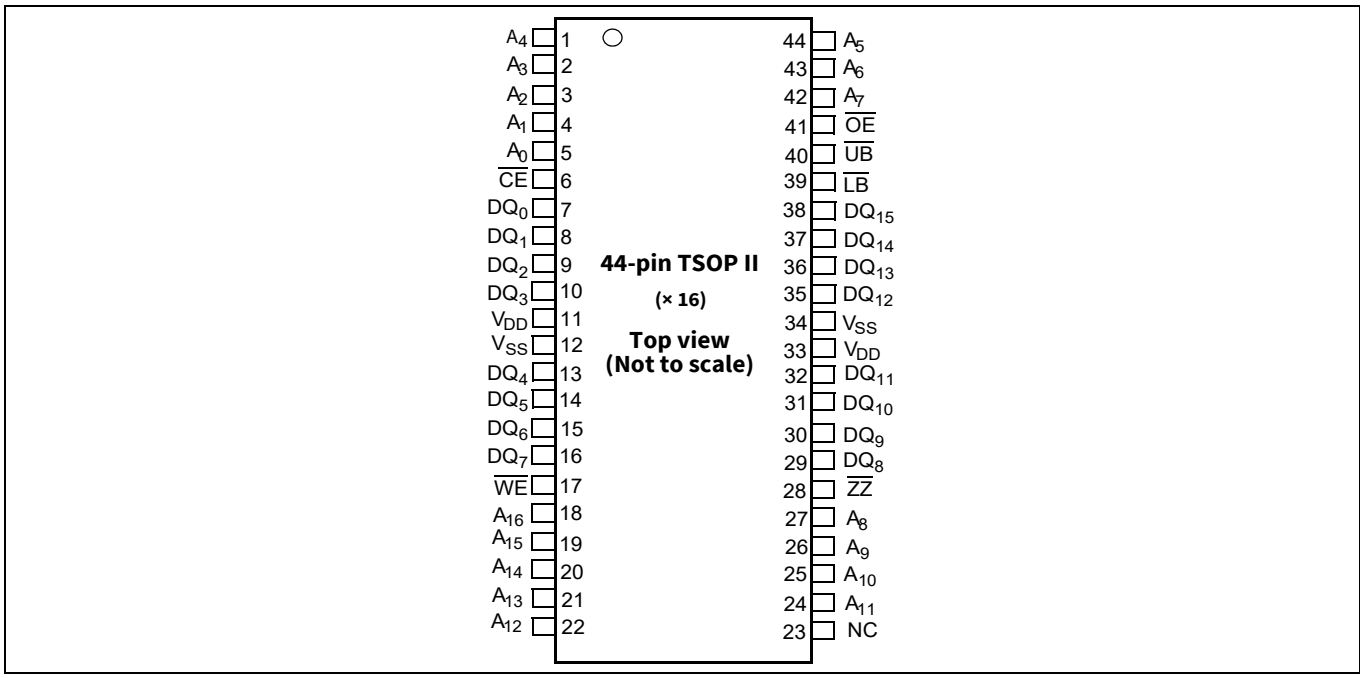


Figure 1 44-pin ceramic TSOP II pinout

2 Pin definitions

Table 1 Pin definitions

Pin name	I/O type	Description
A_0–A_{16}	Input	**Address inputs**: The 17 address lines select one of 128K words in the F-RAM array. The lowest two address lines A_1–A_0 may be used for page mode read and write operations.
DQ_0–DQ_{15}	Input/Output	**Data I/O Lines**: 16-bit bidirectional data bus for accessing the F-RAM array.
WE	Input	**Write Enable**: A write cycle begins when $\overline{WE}$ is asserted. The rising edge causes the CYRS15B102N to write the data on the DQ bus to the F-RAM array. The falling edge of $\overline{WE}$ latches a new column address for page mode write cycles.
CE	Input	**Chip Enable**: The device is selected and a new memory access begins on the falling edge of $\overline{CE}$. The entire address is latched internally at this point. Subsequent changes to the A_1–A_0 address inputs allow page mode operation.
OE	Input	**Output Enable**: When $\overline{OE}$ is LOW, the CYRS15B102N drives the data bus when the valid read data is available. Deasserting $\overline{OE}$ HIGH tristates the DQ pins.
UB	Input	**Upper Byte Select**: Enables DQ_{15}–DQ_8 pins during reads and writes. These pins are HI-Z if $\overline{UB}$ is HIGH. If the user does not perform byte writes and the device is not configured as a 256K × 8, the $\overline{UB}$ and $\overline{LB}$ pins may be tied to ground.
LB	Input	**Lower Byte Select**: Enables DQ_7–DQ_0 pins during reads and writes. These pins are HI-Z if $\overline{LB}$ is HIGH. If the user does not perform byte writes and the device is not configured as a 256 K × 8, the $\overline{UB}$ and $\overline{LB}$ pins may be tied to ground.
ZZ	Input	**Sleep**: When $\overline{ZZ}$ is LOW, the device enters a low-power sleep mode for the lowest supply current condition. $\overline{ZZ}$ must be HIGH for a normal read/write operation. This pin must be tied to V_{DD} if not used.
V_{SS}	Ground	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device
NC	No connect	**No connect**: This pin is not connected to the die.

3 Manufacturing flow

Table 2 Manufacturing flow

Step	Screen	Method	Requirement
1	Wafer lot acceptance test	TM 5007	–
2	Internal visual	TM 2010, Condition A	100%
3	Serialization	–	100%
4	Temperature cycling	TM 1010, Condition C, 10 cycles minimum	100%
5	Constant acceleration	TM 2001, YI orientation only, Condition D	100%
6	Particle impact noise detection (PIND)	TM 2020 Condition A	100%
7	Radiographic (X-ray)	TM 2012, one view only	–
8	Pre burn in electrical parameters	In accordance with applicable Infineon specification	100%
9	Static burn in	TM 1015, Condition C	100%
		72 hours at 125°C each polarity, 144 hours total	–
10	Interim (post static burn in) electricals	In accordance with applicable Infineon device specifications	100%
11	Dynamic burn in	TM 1015, Condition D, 240 hours at 125°C	100%
12	Interim (post Dynamic burn in) electricals	In accordance with applicable Infineon device specifications	100%
13	Final electrical test	In accordance with applicable Infineon device specifications	100%
	(1) 25°C	TM 5005, Table I, Subgroup 1, 2, 3, 7, 8a, 8b, 9	–
	Percent defective allowable (PDA) calculation	5% overall, 3% functional parameters at 25°C	All lots
	(2) –55°C and +125°C	TM 5005, Table I, Subgroup 1, 2, 3, 7, 8a, 8b, 9	–
14	Seal (fine and gross leak test)	TM 1014	100%
15	External visual	TM 2009	100%
16	QCI - Group A	**MIL-PRF 38535**, Table III	All lots
17	QCI - Group B	**MIL-PRF 38535**, Table II	All lots
18	QCI - Group C (1000 hour life test)	**MIL-PRF 38535**, Table IV	All wafer lots
19	QCI - Group D	**MIL-PRF 38535**, Table V	Every 12 mo
20	Radiation Lot Acceptance Test (Group E)	TM 1019, MIL-HDBK-814	All wafer lots

4 Device operation

The CYRS15B102N is a word-wide F-RAM memory logically organized as 131,072 × 16 and accessed using an industry-standard parallel interface. All data written to the part is immediately non-volatile with no delay. The device offers page-mode operation, which provides high-speed access to addresses within a page (row). Access to a different page requires that either $\overline{CE}$ transitions LOW or the upper address (A_{16}–A_2) changes. See the **Table 16** for a complete description of read and write modes.

4.1 Memory operation

Users access 131,072 memory locations, each with 16 data bits through a parallel interface. The F-RAM array is organized as eight blocks, each having 4096 rows. Each row has four column locations, which allow fast access in page-mode operation. When an initial address is latched by the falling edge of $\overline{CE}$, subsequent column locations may be accessed without the need to toggle $\overline{CE}$. When $\overline{CE}$ is deasserted (HIGH), a precharge operation begins. Writes occur immediately at the end of the access with no delay. The $\overline{WE}$ pin must be toggled for each write operation. The write data is stored in the non-volatile memory array immediately, which is a feature unique to F-RAM called “Infineon instant non-volatile write technology”.

4.2 Read operation

A read operation begins on the falling edge of $\overline{CE}$. The falling edge of $\overline{CE}$ causes the address to be latched and starts a memory read cycle if $\overline{WE}$ is HIGH. Data becomes available on the bus after the access time is met. When the address is latched and the access completed, a new access to a random location (different row) may begin while $\overline{CE}$ is still LOW. The minimum cycle time for random addresses is t_{RC}. Note that unlike SRAMs, the CYRS15B102N’s $\overline{CE}$-initiated access time is faster than the address access time.

The CYRS15B102N will drive the data bus when $\overline{OE}$ and at least one of the byte enables ($\overline{UB}$, $\overline{LB}$) is asserted LOW. The upper data byte is driven when $\overline{UB}$ is LOW, and the lower data byte is driven when $\overline{LB}$ is LOW. If $\overline{OE}$ is asserted after the memory access time is met, the data bus will be driven with valid data. If $\overline{OE}$ is asserted before completing the memory access, the data bus will not be driven until valid data is available. This feature minimizes the supply current in the system by eliminating transients caused by invalid data being driven to the bus. When $\overline{OE}$ is deasserted HIGH, the data bus will remain in a HI-Z state.

4.3 Write operation

In the CYRS15B102N, writes occur in the same interval as reads. The CYRS15B102N supports both $\overline{CE}$- and $\overline{WE}$-controlled write cycles. In both cases, the address A_{16}–A_2 is latched on the falling edge of $\overline{CE}$.

In a $\overline{CE}$-controlled write, the $\overline{WE}$ signal is asserted before beginning the memory cycle. That is, $\overline{WE}$ is LOW when $\overline{CE}$ falls. In this case, the device begins the memory cycle as a write. The CYRS15B102N will not drive the data bus regardless of the state of $\overline{OE}$ as long as $\overline{WE}$ is LOW. Input data must be valid when $\overline{CE}$ is deasserted HIGH. In a $\overline{WE}$-controlled write, the memory cycle begins on the falling edge of $\overline{CE}$. The $\overline{WE}$ signal falls some time later. Therefore, the memory cycle begins as a read. The data bus will be driven if $\overline{OE}$ is LOW; however, it will be HI-Z when $\overline{WE}$ is asserted LOW. The $\overline{CE}$- and $\overline{WE}$-controlled write timing cases are shown on the **Figure 9**.

Write access to the array begins on the falling edge of $\overline{WE}$ after the memory cycle is initiated. The write access terminates on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever comes first. A valid write operation requires the user to meet the access time specification before deasserting $\overline{WE}$ or $\overline{CE}$. The data setup time indicates the interval during which data cannot change before the end of the write access (rising edge of $\overline{WE}$ or $\overline{CE}$).

Unlike other non-volatile memory technologies, there is no write delay with F-RAM. Because the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

4.4 Page mode operation

The F-RAM array is organized as eight blocks, each having 4096 rows. Each row has four column-address locations. Address inputs A_1–A_0 define the column address to be accessed. An access can start on any column address, and other column locations may be accessed without the need to toggle the $\overline{CE}$ pin. For fast access reads, after the first data byte is driven to the bus, the column address inputs A_1–A_0 may be changed to a new value. A new data byte is then driven to the DQ pins no later than t_{AAP}, which is less than half the initial read access time. For fast access writes, the first write pulse defines the first write access. While $\overline{CE}$ is LOW, a subsequent write pulse along with a new column address provides a page mode write access.

4.5 Precharge operation

The precharge operation is an internal condition in which the memory state is prepared for a new access. Precharge is user-initiated by driving the $\overline{CE}$ signal HIGH. It must remain HIGH for at least the minimum precharge time, t_{PC}.

Precharge is also activated by changing the upper addresses, A_{16}–A_2. The current row is first closed before accessing the new row. The device automatically detects an upper order address change, which starts a precharge operation. The new address is latched and the new read data is valid within the t_{AA} address access time; see **Figure 8**. A similar sequence occurs for write cycles; see **Figure 13**. The rate at which random addresses can be issued is t_{RC} and t_{WC}, respectively.

4.6 Sleep mode

The device incorporates a sleep mode of operation, which allows the user to achieve the lowest-power-supply-current condition. It enters a low-power sleep mode by asserting the $\overline{ZZ}$ pin LOW. Read and write operations must complete before the $\overline{ZZ}$ pin going LOW. When $\overline{ZZ}$ is LOW, all pins are ignored except the $\overline{ZZ}$ pin. When $\overline{ZZ}$ is deasserted HIGH, there is some time delay (t_{ZZEX}) before the user can access the device.

If sleep mode is not used, the $\overline{ZZ}$ pin must be tied to V_{DD}.

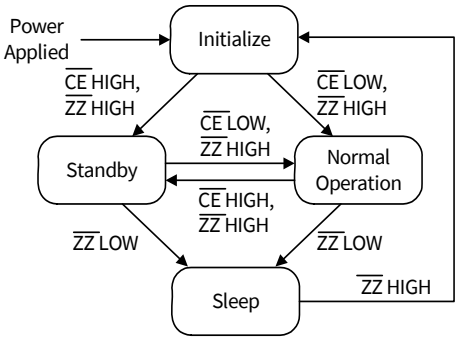


Figure 2 Sleep/standby state diagram

4.7 Software write protect

The 128K × 16 address space is divided into eight sectors (blocks) of 16K × 16 each. Each sector can be individually software write-protected and the settings are non-volatile. A unique address and command sequence invokes the write-protect mode.

To modify write protection, the system host must issue six read commands, three write commands, and a final read command. The specific sequence of read addresses must be provided to access the write-protect mode. Following the read address sequence, the host must write a data byte that specifies the desired protection state of each sector. For confirmation, the system must then write the complement of the protection byte immediately after the protection byte. Any error that occurs including read addresses in the wrong order, issuing a seventh read address, or failing to complement the protection value will leave the write protection unchanged.

The write-protect state machine monitors all addresses, taking no action until this particular read/write sequence occurs. During the address sequence, each read will occur as a valid operation and data from the corresponding addresses will be driven to the data bus. Any address that occurs out of sequence will cause the software protection state machine to start over. After the address sequence is completed, the next operation must be a write cycle. The lower data byte contains the write-protect settings. This value will not be written to the memory array, so the address is a don't-care. Rather it will be held pending the next cycle, which must be a write of the data complement to the protection settings. If the complement is correct, the write-protect settings will be adjusted. Otherwise, the process is aborted and the address sequence starts over. The data value written after the correct six addresses will not be entered into the memory.

The protection data byte consists of eight bits, each associated with the write-protect state of a sector. The data byte must be driven to the lower eight bits of the data bus, DQ_7–DQ_0. Setting a bit to '1' write-protects the corresponding sector; a 0 enables writes for that sector. The following table shows the write-protect sectors with the corresponding bit that controls the write-protect setting.

Table 3 Write protect sectors - 16K × 16 blocks

Sectors	Blocks
Sector 7	1FFFFh–1C000h
Sector 6	1BFFFh–18000h
Sector 5	17FFFh–14000h
Sector 4	13FFFh–10000h
Sector 3	0FFFFh–0C000h
Sector 2	0BFFFh–08000h
Sector 1	07FFFh–04000h
Sector 0	03FFFh–00000h

The write-protect address sequence follows:

1. Read address 12555h
2. Read address 1DAAAh
3. Read address 01333h
4. Read address 0ECCCh
5. Read address 000FFh
6. Read address 1FF00h
7. Write address 1DAAAh
8. Write address 0ECCCh
9. Write address 0FF00h
10. Read address 00000h

The address sequence provides a secure way of modifying the protection. The write-protect sequence has a one in 3×10^{32} chance of randomly accessing exactly the first six addresses. The odds are further reduced by requiring three more write cycles, one that requires an exact inversion of the data byte. **Figure 3** shows a flow chart of the entire write-protect operation. The write-protect settings are non-volatile. The factory default: all blocks are unprotected.

For example, the following sequence write-protects addresses from 0C000h to 13FFFh (sectors 3 and 4):

Table 4 Sequence

	Address	**Data**
Read	12555h	–
Read	1DAAAh	–
Read	01333h	–
Read	0ECCCh	–
Read	000FFh	–
Read	1FF00h	–
Write	1DAAAh	18h; bits 3 and 4 = 1
Write	0ECCCh	E7h; complement of 18 h
Write	0FF00h	Don’t care
Read	00000h	–

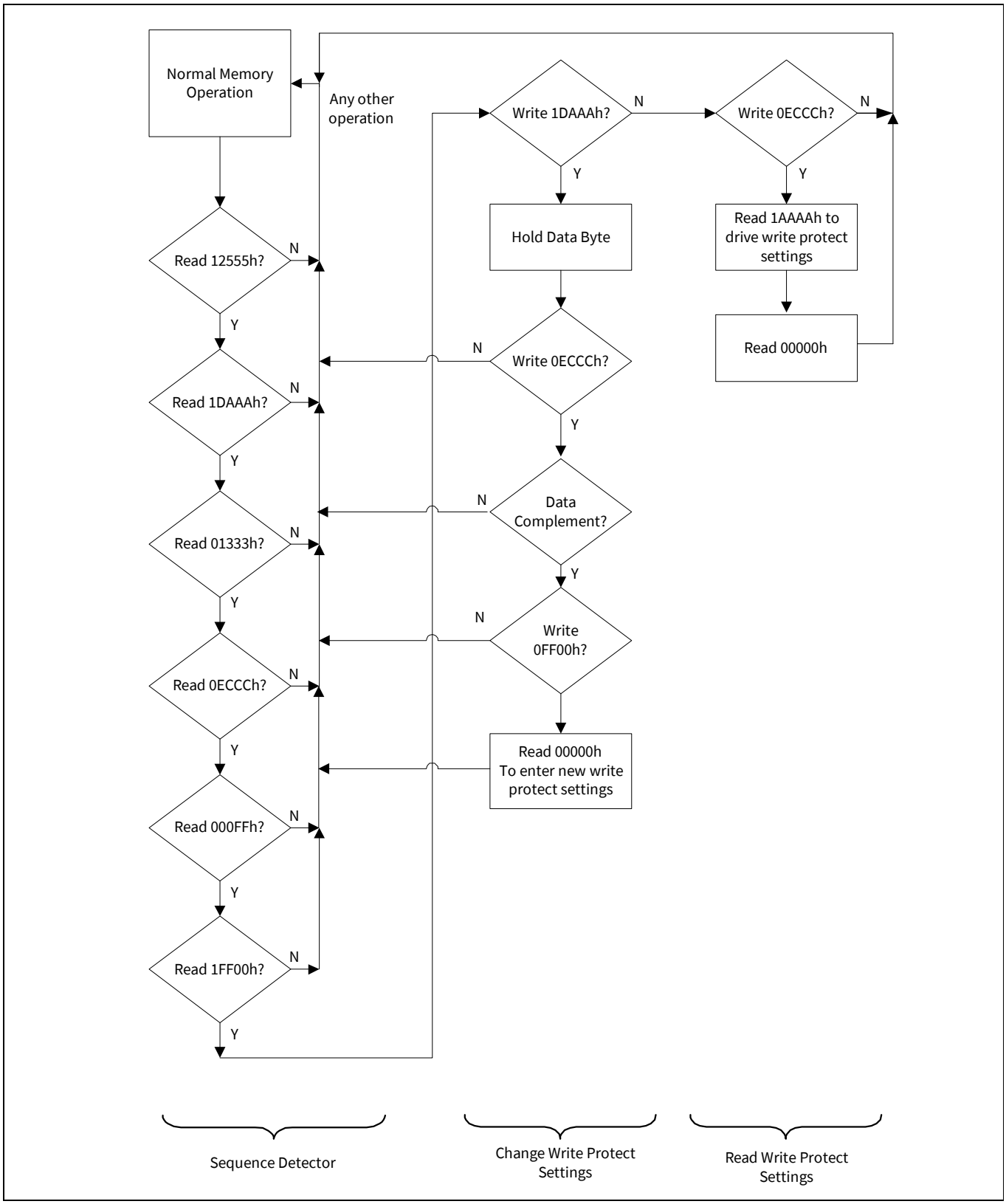


Figure 3 Write-protect state machine

4.8 Software write-protect timing

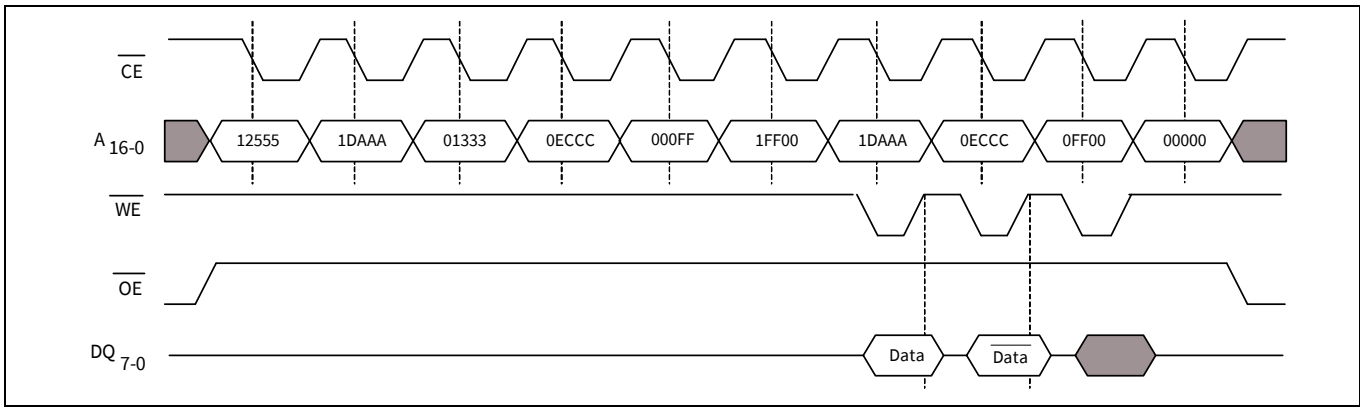


Figure 4 Sequence to set write-protect blocks[2]

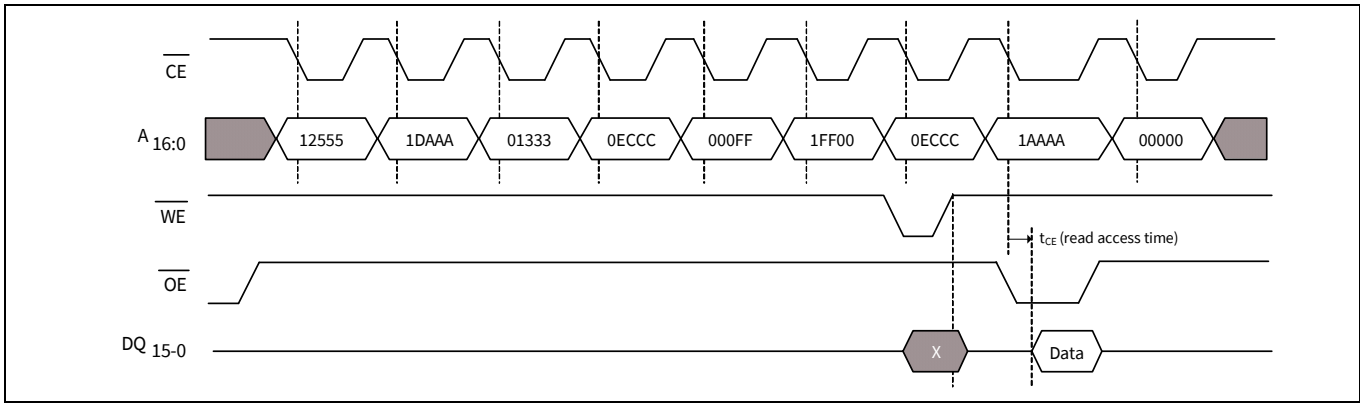


Figure 5 Sequence to read write-protect settings[2]

Note
2. This sequence requires $t_{AS} \geq 10$ ns and address must be stable while $\overline{CE}$ is LOW.

4.9 SRAM drop-in replacement

The CYRS15B102N is designed to be a drop-in replacement for standard asynchronous SRAMs. The device does not require $\overline{CE}$ to toggle for each new address. $\overline{CE}$ may remain LOW indefinitely. While $\overline{CE}$ is LOW, the device automatically detects address changes and a new access begins. This functionality allows $\overline{CE}$ to be grounded, similar to an SRAM. It also allows page mode operation at speeds up to 33 MHz. Note that if $\overline{CE}$ is tied to ground, the user must be sure $\overline{WE}$ is not LOW at power-up or power-down events. If $\overline{CE}$ and $\overline{WE}$ are both LOW during power cycles, data will be corrupted. **Figure 6** shows a pull-up resistor on $\overline{WE}$, which will keep the pin HIGH during power cycles, assuming the MCU/MPU pin tristates during the reset condition. The pull-up resistor value should be chosen to ensure the $\overline{WE}$ pin tracks V_{DD} to a high enough value, so that the current drawn when $\overline{WE}$ is LOW is not an issue. A 10 kΩ resistor draws 330 µA when $\overline{WE}$ is LOW and V_{DD} = 3.3 V. Note that software write-protect is not available if the chip enable pin is hard-wired.

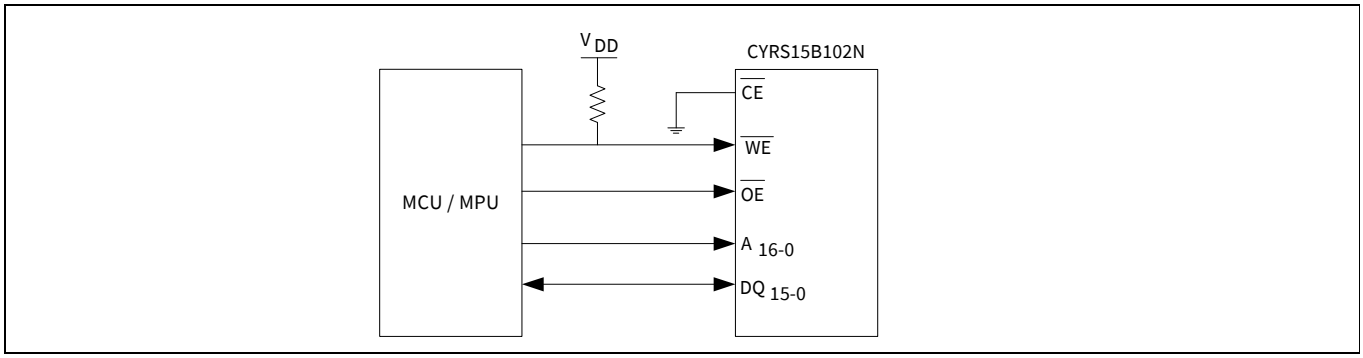


Figure 6 Use of pull-up resistor on $\overline{WE}$

For applications that require the lowest power consumption, the $\overline{CE}$ signal should be active (LOW) only during memory accesses. The CYRS15B102N draws supply current while $\overline{CE}$ is LOW, even if addresses and control signals are static. While $\overline{CE}$ is HIGH, the device draws no more than the maximum standby current, I_{SB}.

The CYRS15B102N is backward compatible with the 2 Mbit FM21L16 device. There are some differences in the timing specifications. Refer to the FM21L16 datasheet.

The $\overline{UB}$ and $\overline{LB}$ byte select pins are active for both read and write cycles. They may be used to allow the device to be wired as a 256K × 8 memory. The upper and lower data bytes can be tied together and controlled with the byte selects. Individual byte enables or the next higher address line A_{17} may be available from the system processor.

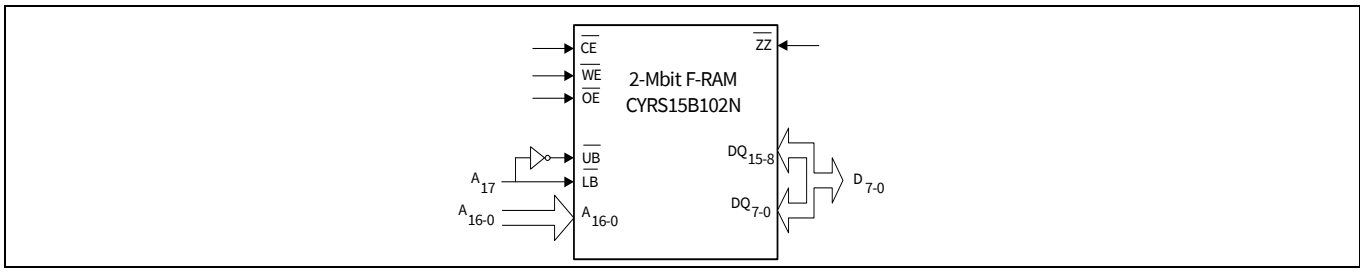


Figure 7 CYRS15B102N wired as 256K × 8

4.10 Endurance

The CYRS15B102N is capable of being accessed at least 10^{13} times – reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis. The F-RAM architecture is based on an array of rows and columns. Rows are defined by A_{16-2} and column addresses by A_{1-0}. The array is organized as 32K rows of four words each. The entire row is internally accessed once whether a single 16-bit word or all four words are read or written. Each word in the row is counted only once in an endurance calculation.

The user may choose to write CPU instructions and run them from a certain address space. **Table 5** shows endurance calculations for a 256 byte repeating loop, which includes a starting address, three-page mode accesses, and a $\overline{CE}$ precharge. The number of bus clock cycles needed to complete a four-word transaction is 4 + 1 at lower bus speeds, but 5 + 2 at 33 MHz due to initial read latency and an extra clock cycle to satisfy the device's precharge timing constraint t_{PC}. The entire loop causes each byte to experience only one endurance cycle. The F-RAM read and write endurance is virtually unlimited even at a 33 MHz system bus clock rate.

Table 5 Time to reach 10 trillion cycles for repeating 256-byte loop

Bus freq (MHz)	Bus cycle time (ns)	256-byte transaction time (µs)	Endurance cycles/sec	Endurance cycles/yr	Years to reach 10^{13} cycles
33	30	10.56	94,690	2.98×10^{12}	3.35
25	40	12.8	78,125	2.46×10^{12}	4.06
10	100	28.8	34,720	1.09×10^{12}	9.17
5	200	57.6	17,360	5.47×10^{11}	18.28

4.11 Qualification and screening

The 130 nm radiation-tolerant FRAM technology was qualified by Infineon after meeting the criteria of the general manufacturing standards. The test flow includes screening units with the defined flow (Class V) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the 130 nm process and the FRAM products are subject to period or lot-based technology conformance inspection (TCI) and quality conformance inspection (QCI) tests, respectively. Infineon offers both prototyping models and flight units of these product configurations.

Table 6 Qualification tests

Group	Tests
Group A	General electrical tests
Group B	Mechanical - Dimensions, bond strength, solvents, die shear, solderability, lead Integrity, seal, and acceleration
Group C	Life tests - 1000 hours at 125°C or equivalent
Group D	Package related mechanical tests - shock, vibration, acceleration, salt, seal, lead finish adhesion, lid torque, thermal shock, and moisture resistance
Group E	Radiation tests

4.12 Single event functional interrupt elimination

As outlined in the product feature section, the intrinsic Single Event Functional Interrupt (SEFI) rate of the CYRS15B102N device is 1.34×10^{-4} upsets/device-day, which equates to a SEFI event failure every 20 years at GEO orbit (solar min). To eliminate SEFI events, Infineon recommends entering the low-power sleep mode by asserting he $\overline{ZZ}$ pin to V_{SS}, followed by an immediate exit out of the sleep mode by deasserting he $\overline{ZZ}$ pin to V_{DD} before any Read/Write operation on the device. The entry/exit of the Deep Sleep mode will reset and initialize all execution/configuration registers and ensure correct addressing and configuration of the device. This procedure is recommended before the first Read/Write operation of consecutive operations.

Alternatively, the device can also be power cycled prior of the first read and after a prolonged radiation exposure. Power cycling and Sleep-Wakeup sequencing are equally effective to eliminate SEFI events. Details can be obtained from the SEE radiation report.

5 Maximum ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Table 7 Absolute maximum ratings

Parameter		Max ratings
Storage temperature		–65°C to +150°C
Maximum accumulated storage time	At 150°C ambient temperature	1000 h
	At 125°C ambient temperature	11000 h
	At 85°C ambient temperature	121 years
Ambient temperature with power applied		–55°C to +125°C
Supply voltage on V_{DD} relative to V_{SS}		–1.0 V to +4.5 V
Voltage applied to outputs in High Z state		–0.5 V to V_{DD} + 0.5 V
Input voltage		–1.0 V to +4.5 V and $V_{IN} < V_{DD}$ + 1.0 V
Transient voltage (< 20 ns) on any pin to ground potential		–2.0 V to V_{CC} + 2.0 V
Package power dissipation capability (T_A = 25°C)		1.0 W
Surface mount Pb soldering temperature (3 seconds)		+260°C
DC output current (1 output at a time, 1 s duration)		15 mA
Static discharge voltage Human body model (AEC-Q100-002 Rev. E) Charged device model (AEC-Q100-011 Rev. B)		 2 kV 500 V
Latch-up current		> 140 mA
Device weight		1.76 g (typical)

6 Operating range

Table 8 Operating range

Range	Ambient temperature (T_A)	V_{DD}
Military	–55°C to +125°C	2.0 V to 3.6 V

7 DC electrical characteristics

Table 9 DC electrical characteristics

Over the **Operating range**

Parameter	Description	Test conditions		Min	Typ[3]	Max	Unit
V_{DD}	Power supply voltage			2.0	3.3	3.6	V
I_{DD}	V_{DD} supply current	V_{DD} = 3.6 V, CE cycling at min. cycle time. All inputs toggling at CMOS levels (0.2 V or V_{DD} – 0.2 V), all DQ pins unloaded.		–	7	20	mA
I_{SB}	V_{DD} standby current	V_{DD} = 3.6 V, CE at V_{DD}, All other pins are static and at CMOS levels (0.2 V or V_{DD} – 0.2 V), ZZ is HIGH.	TID = 0 krad	–	100	700	µA
			TID = 150 krad	–	–	6	mA
I_{ZZ}	Sleep mode current	V_{DD} = 3.6 V, ZZ is LOW, All other inputs V_{SS} or V_{DD}.	TID = 0 krad	–	3	20	µA
			TID = 150 krad	–	–	8	mA
I_{LI}	Input leakage current	V_{IN} between V_{DD} and V_{SS}		–	–	±10	µA
I_{LO}	Output leakage current	V_{OUT} between V_{DD} and V_{SS}		–	–	±10	µA
V_{IH1}	Input HIGH voltage	V_{DD} = 2.7 V to 3.6 V		2.2	–	V_{DD} + 0.3	V
V_{IH2}	Input HIGH voltage	V_{DD} = 2.0 V to 2.7 V		0.7 × V_{DD}	–	–	V
V_{IL1}	Input LOW voltage	V_{DD} = 2.7 V to 3.6 V		–0.3	–	0.8	V
V_{IL2}	Input LOW voltage	V_{DD} = 2.0 V to 2.7 V		–0.3	–	0.3 × V_{DD}	V
V_{OH1}	Output HIGH voltage	I_{OH} = –1 mA, V_{DD} > 2.7 V		2.4	–	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA		V_{DD} – 0.2	–	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 2 mA, V_{DD} > 2.7 V		–	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 150 µA		–	–	0.2	V

Note
3. Typical values are at 25°C, V_{DD} = V_{DD} (typ). Not 100% tested.

8 Data retention and endurance

Table 10 Data retention and endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 125°C	11000	–	Hours
		T_A = 105°C	11	–	Years
		T_A = 85°C	121	–	Years
NV_C	Endurance	Over operating temperature	10^{13}	–	Cycles

9 Capacitance

Table 11 Capacitance

Parameter	Description	Test conditions	Max	Unit
$C_{I/O}$	Input/Output capacitance (DQ)	$T_A = 25°C, f = 1\,MHz, V_{DD} = V_{DD}(typ)$	8	pF
C_{IN}	Input capacitance		6	pF
C_{ZZ}	Input capacitance of $\overline{ZZ}$ pin		8	pF

10 Thermal resistance

Table 12 Thermal resistance

Parameter	Description	Test conditions	44-pin ceramic TSOP	Unit
Θ_{JC}	Thermal resistance (junction to case)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	25	°C/W

11 AC test conditions

Table 13 AC test conditions

Parameter and description	Values
Input pulse levels	0 V to 3 V
Input rise and fall times (10%–90%)	≤ 3 ns
Input and output timing reference levels	1.5 V
Output load capacitance	30 pF

12 AC switching characteristics

Table 14 AC switching characteristics

Over the **Operating range**

Parameters [4]		Description	V_{DD} = 2.0 V to 2.7 V		V_{DD} = 2.7 V to 3.6 V		Unit
Parameter	Alt parameter		Min	Max	Min	Max	
SRAM read cycle							
t_{CE}	t_{ACE}	Chip enable access time	–	70	–	60	ns
t_{RC}	–	Read cycle time	105	–	90	–	ns
t_{AA}	–	Address access time, A_{16-2}	–	105	–	90	ns
t_{OH}	t_{OHA}	Output hold time, A_{16-2}	20	–	20	–	ns
t_{AAP}	–	Page mode access time, A_{1-0}	–	40	–	30	ns
t_{OHP}	–	Page mode output hold time, A_{1-0}	3	–	3	–	ns
t_{CA}	–	Chip enable active time	70	–	60	–	ns
t_{PC}	–	Precharge time	35	–	30	–	ns
t_{BA}	t_{BW}	$\overline{UB}$, $\overline{LB}$ access time	–	25	–	15	ns
t_{AS}	t_{SA}	Address setup time (to $\overline{CE}$ LOW)	0	–	0	–	ns
t_{AH}	t_{HA}	Address hold time ($\overline{CE}$ Controlled)	70	–	60	–	ns
t_{OE}	t_{DOE}	Output enable access time	–	25	–	15	ns
t_{HZ} [5, 6]	t_{HZCE}	Chip enable to output HI-Z	–	15	–	10	ns
t_{OHZ} [5, 6]	t_{HZOE}	Output enable HIGH to output HI-Z	–	15	–	10	ns
t_{BHZ} [5, 6]	t_{HZBE}	$\overline{UB}$, $\overline{LB}$ HIGH to output HI-Z	–	15	–	10	ns
SRAM write cycle							
t_{WC}	t_{WC}	Write cycle time	105	–	90	–	ns
t_{CA}	–	Chip enable active time	70	–	70	–	ns
t_{CW}	t_{SCE}	Chip enable to write enable HIGH	70	–	70	–	ns
t_{PC}	–	Precharge time	35	–	30	–	ns
t_{PWC}	–	Page mode write enable cycle time	40	–	40	–	ns

Notes

4. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 0 to 3 V, output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance shown in **"AC test conditions"** on page 22.
5. t_{HZ}, t_{OHZ} and t_{BHZ} are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
6. This parameter is characterized but not 100% tested.
7. t_{WZ} is specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high-impedance state.

Table 14 AC switching characteristics *(continued)*

Over the **Operating range**

Parameters [4]		Description	V_{DD} = 2.0 V to 2.7 V		V_{DD} = 2.7 V to 3.6 V		Unit
Parameter	Alt parameter		Min	Max	Min	Max	
t_{WP}	t_{PWE}	Write enable pulse width	22	–	18	–	ns
t_{WP2}	t_{BW}	$\overline{UB}$, $\overline{LB}$ pulse width	22	–	18	–	ns
t_{WP3}	t_{PWE}	$\overline{WE}$ LOW to $\overline{UB}$, $\overline{LB}$ HIGH	22	–	18	–	ns
t_{AS}	t_{SA}	Address setup time (to $\overline{CE}$ LOW)	0	–	0	–	ns
t_{AH}	t_{HA}	Address hold time ($\overline{CE}$ Controlled)	70	–	60	–	ns
t_{ASP}	–	Page mode address setup time (to $\overline{WE}$ LOW)	8	–	5	–	ns
t_{AHP}	–	Page mode address hold time (to $\overline{WE}$ LOW)	20	–	15	–	ns
t_{WLC}	t_{PWE}	Write enable LOW to chip disabled	30	–	25	–	ns
t_{BLC}	t_{BW}	$\overline{UB}$, $\overline{LB}$ LOW to chip disabled	30	–	25	–	ns
t_{WLA}	–	Write enable LOW to address change, A_{16-2}	30	–	25	–	ns
t_{AWH}	–	Address change to write enable HIGH, A_{16-2}	105	–	90	–	ns
t_{DS}	t_{SD}	Data input setup time	20	–	15	–	ns
t_{DH}	t_{HD}	Data input hold time	0	–	0	–	ns
t_{WZ} [6, 7]	t_{HZWE}	Write enable LOW to output HI-Z	–	10	–	10	ns
t_{WX} [6]	–	Write enable HIGH to output driven	10	–	8	–	ns
t_{BDS}	–	Byte disable setup time (to $\overline{WE}$ LOW)	8	–	5	–	ns
t_{BDH}	–	Byte disable hold time (to $\overline{WE}$ HIGH)	8	–	5	–	ns

Notes

4. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 0 to 3 V, output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance shown in **"AC test conditions"** on page 22.
5. t_{HZ}, t_{OHZ} and t_{BHZ} are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
6. This parameter is characterized but not 100% tested.
7. t_{WZ} is specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high-impedance state.

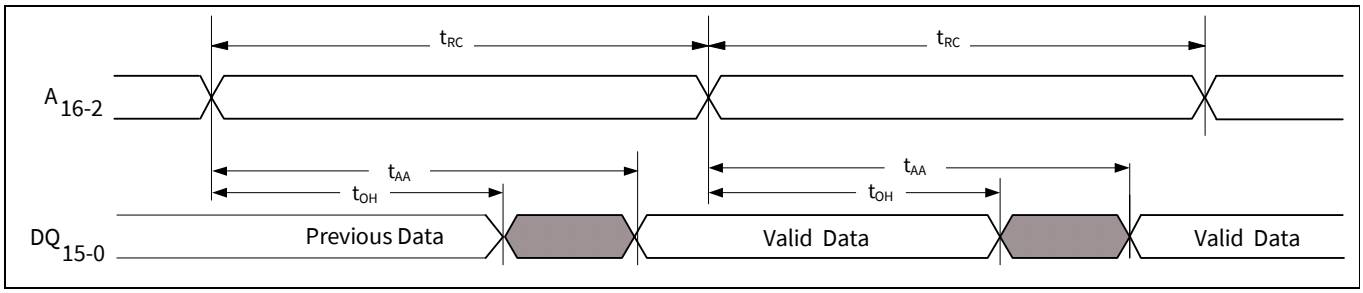


Figure 8 Read cycle timing no. 1 ($\overline{CE}$ LOW, $\overline{OE}$ LOW)

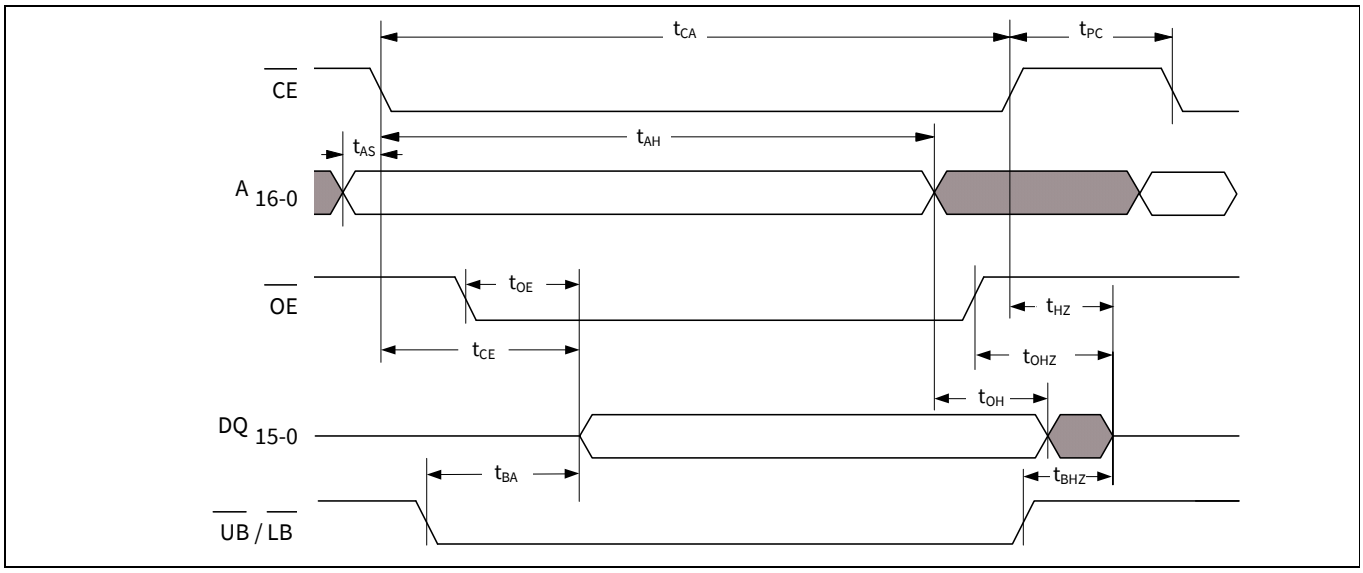


Figure 9 Read cycle timing no. 2 ($\overline{CE}$ controlled)

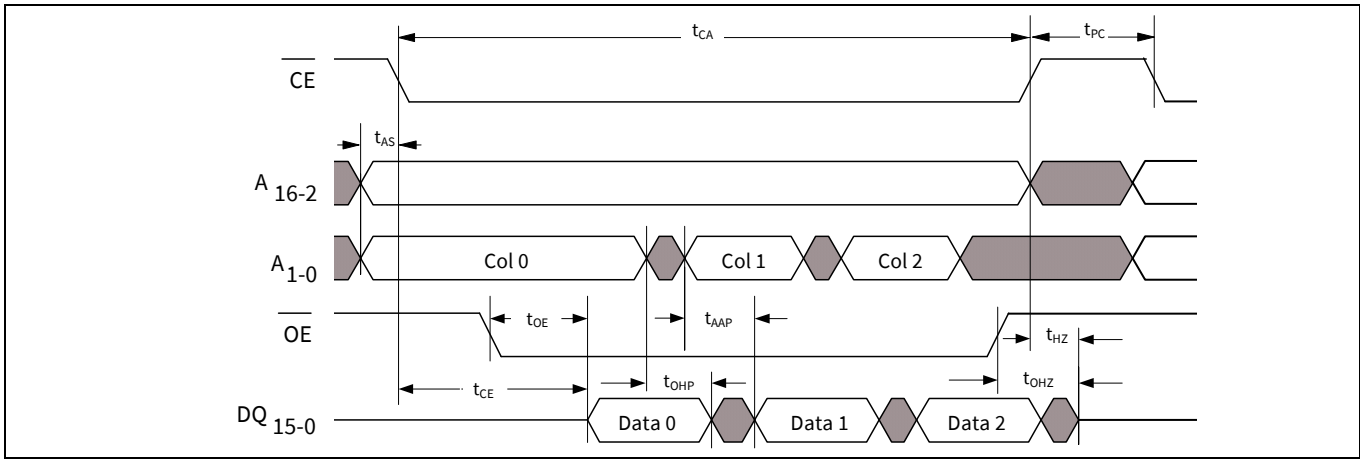


Figure 10 Page mode read cycle timing [8]

Note
8. Although sequential column addressing is shown, it is not required.

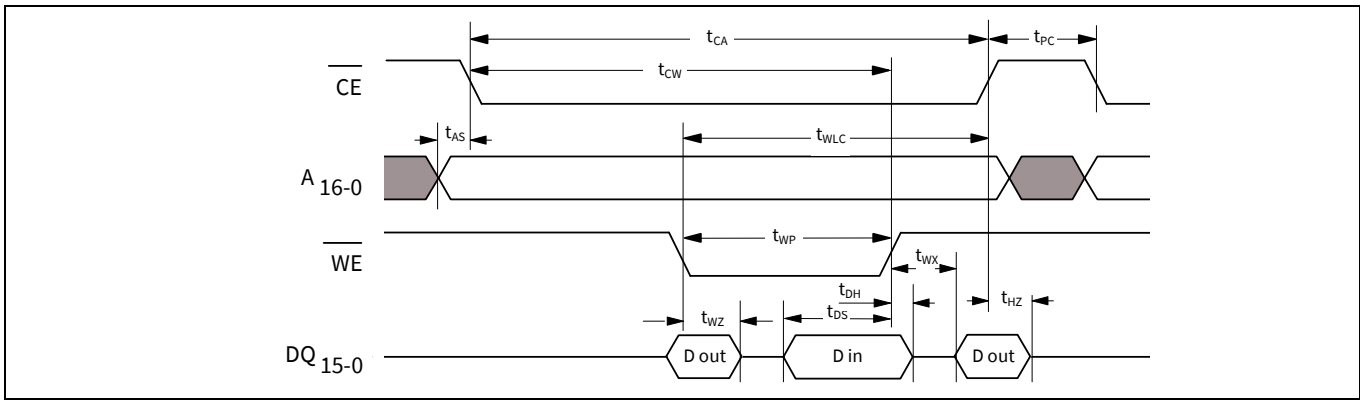


Figure 11 Write cycle timing no. 1 (WE controlled) [9]

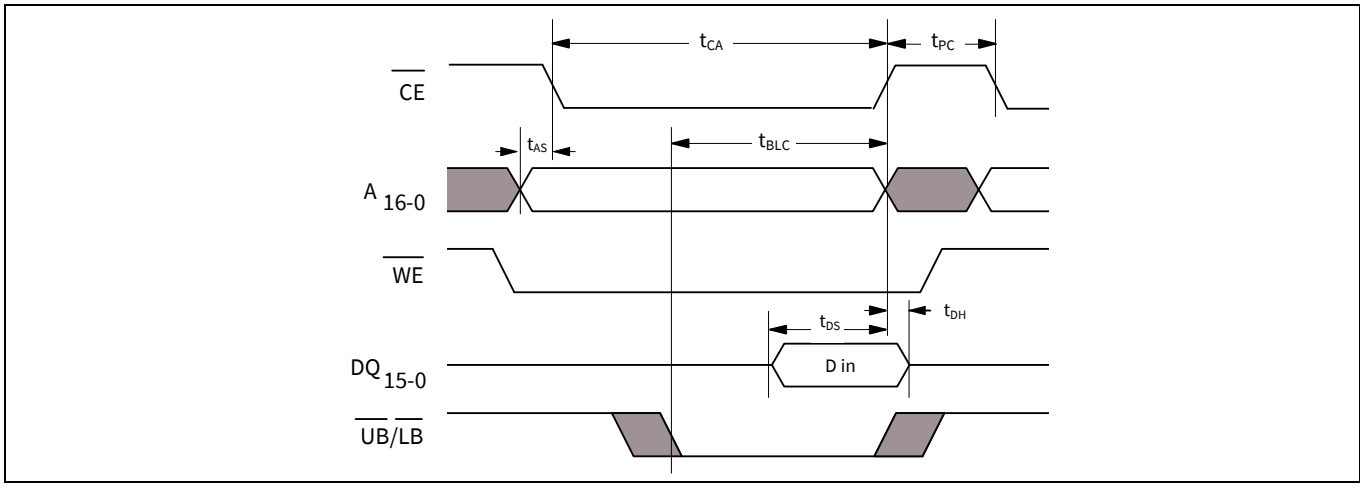


Figure 12 Write cycle timing no. 2 (CE controlled)

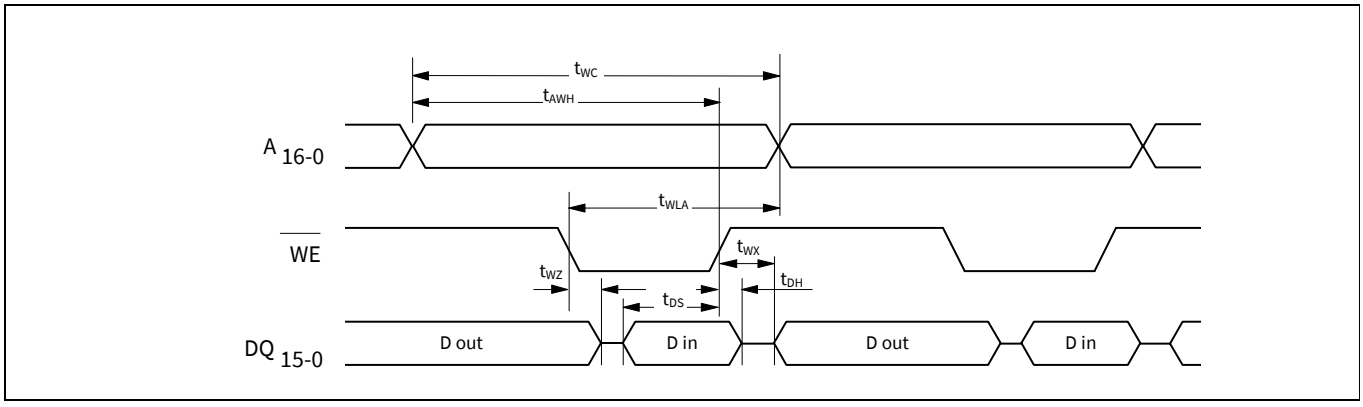


Figure 13 Write cycle timing no. 3 (CE LOW) [9]

Note
9. OE (not shown) is LOW only to show the effect of WE on DQ pins.

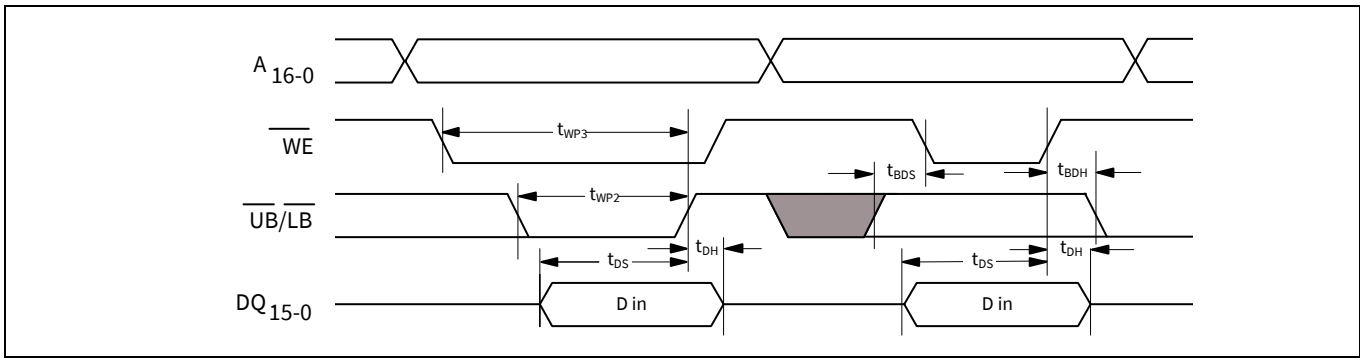


Figure 14 Write cycle timing no. 4 (CE LOW) [10]

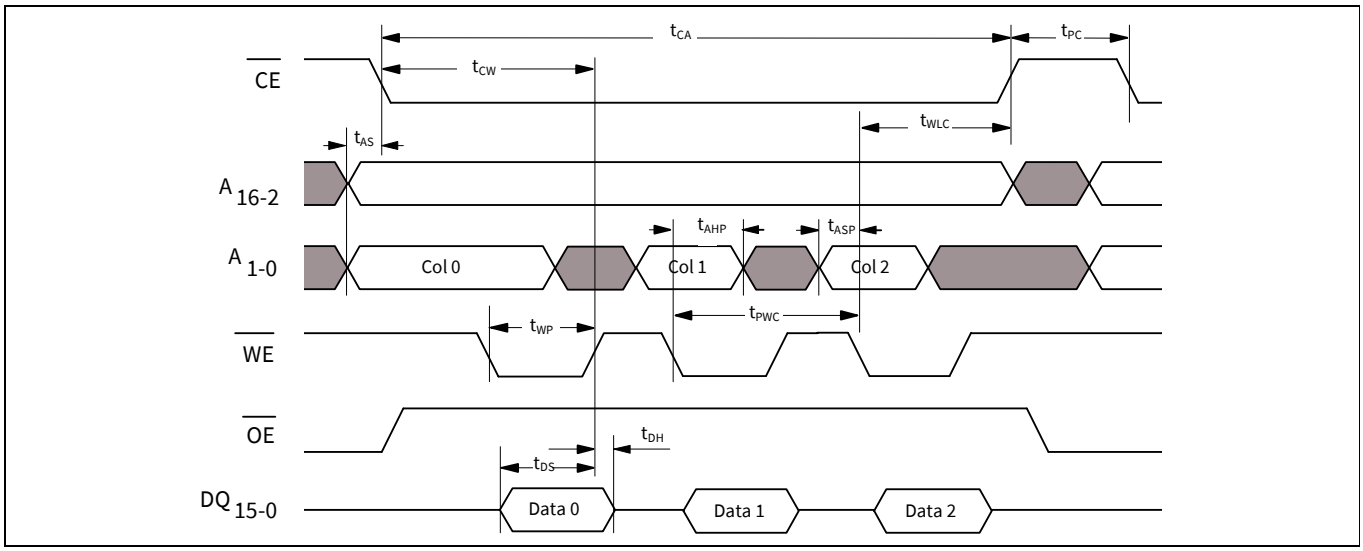


Figure 15 Page mode write cycle timing

Note
10. UB and LB to show byte enable and byte masking cases.

13 Power cycle and sleep mode timing

Table 15 Power cycle and sleep mode timing

Over the **Operating range**

Parameter	Description	Min	Max	Unit
t_{PU}	Power-up (after V_{DD} min. is reached) to first access time	1	–	ms
t_{PD}	Last write ($\overline{WE}$ HIGH) to power down time	0	–	ms
t_{VR}[11]	V_{DD} power-up ramp rate	50	–	µs/V
t_{VF}[11]	V_{DD} power-down ramp rate	100	–	µs/V
t_{ZZH}	$\overline{ZZ}$ active to DQ HI-Z time	–	20	ns
t_{WEZZ}	Last write to sleep mode entry time	0	–	µs
t_{ZZL}	$\overline{ZZ}$ active LOW time	1	–	µs
t_{ZZEN}	Sleep mode entry time ($\overline{ZZ}$ LOW to $\overline{CE}$ don't care)	–	0	µs
t_{ZZEX}	Sleep mode exit time ($\overline{ZZ}$ HIGH to 1st access after wakeup)	–	500	µs

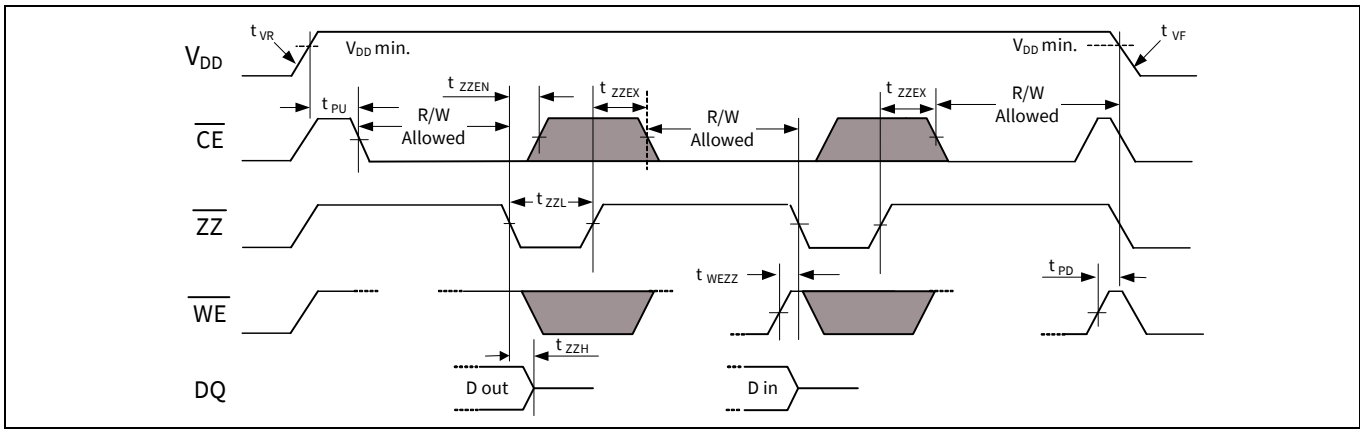


Figure 16 Power cycle and sleep mode timing

Note

11. Slope measured at any point on the V_{DD} waveform.

14 Functional truth table

Table 16 Functional truth table

CE	WE	A_{16-2}	A_{1-0}	ZZ	Operation [12, 13]
X	X	X	X	L	Sleep Mode
H	X	X	X	H	Standby/Idle
↓ L	H H	V V	V V	H H	Read
L	H	No change	Change	H	Page Mode Read
L	H	Change	V	H	Random Read
↓ L	L L	V V	V V	H H	$\overline{CE}$-Controlled Write[13]
L	↓	V	V	H	$\overline{WE}$-Controlled Write [13, 14]
L	↓	No change	V	H	Page Mode Write [15]
↑ L	X X	X X	X X	H H	Starts precharge

Notes
12. H = Logic HIGH, L = Logic LOW, V = Valid Data, X = Don't Care, ↓ = toggle LOW, ↑ = toggle HIGH.
13. For write cycles, data-in is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever comes first.
14. $\overline{WE}$-controlled write cycle begins as a Read cycle and then A_{16-2} is latched.
15. Addresses A_{1-0} must remain stable for at least 15 ns during page mode operation.

15 Byte select truth table

Table 17 Byte select truth table

WE	OE	LB	UB	Operation [16]
H	H	X	X	Read; Outputs disabled
	X	H	H	
H	L	H	L	Read upper byte; HI-Z lower byte
		L	H	Read lower byte; HI-Z upper byte
		L	L	Read both bytes
L	X	H	L	Write upper byte; Mask lower byte
		L	H	Write lower byte; Mask upper byte
		L	L	Write both bytes

Note
16. The $\overline{UB}$ and $\overline{LB}$ pins may be grounded if 1) the system does not perform byte writes and 2) the device is not configured as a 256K × 8.

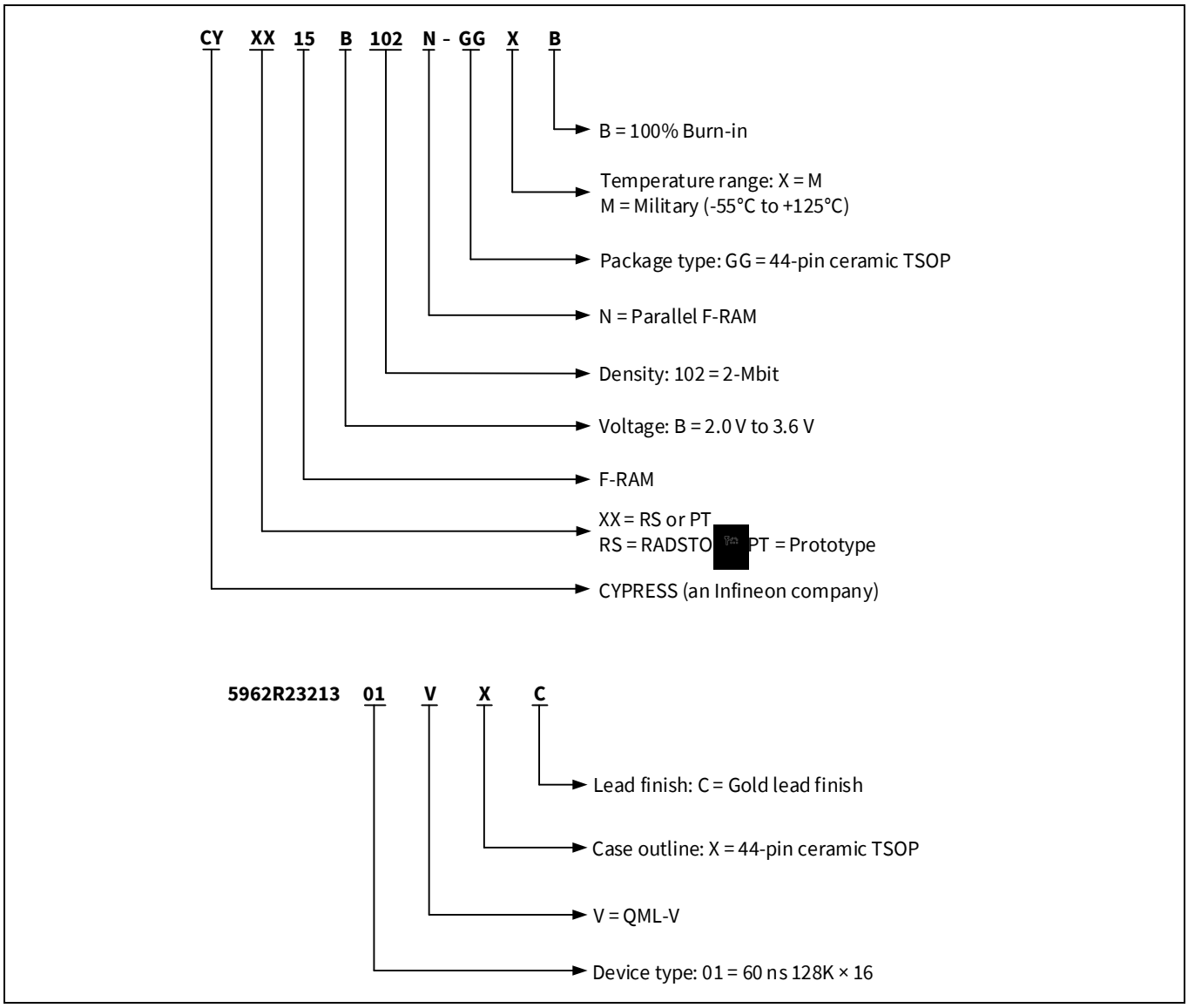
16 Ordering information

Table 18 Ordering information

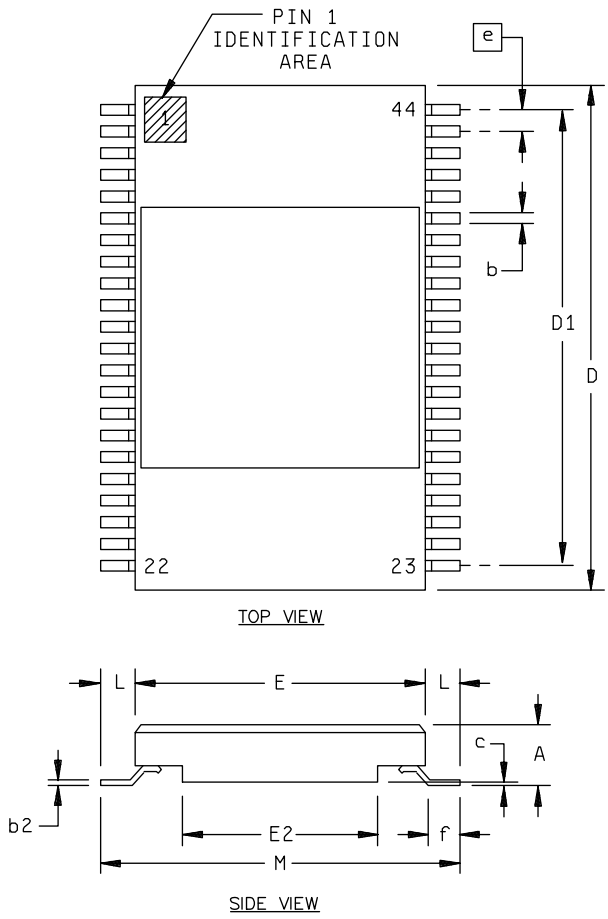
Access time (ns)	Product	Package diagram	Package type	Operating range
60	CYRS15B102N-GGMB	002-33895	44-pin ceramic TSOP package	Military
	CYPT15B102N-GGMB		44-pin ceramic TSOP package, Prototype unit	
	5962R2321301VXC		44-pin ceramic TSOP package, QML-V certified unit	

All the above parts are Pb-free.

16.1 Ordering code definitions



17 Package diagram



Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	2.986	3.842	E	9.96	10.36
b	0.300	0.400	E2	5.280	5.680
b2	0.150	0.250	e	0.80 BSC	
c	0.05	---	f	0.406	0.597
D	18.215	18.615	L	0.839 NOM (ref)	
D1	16.60	17.00	M	11.735	11.938
N	44				

NOTES:
1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.

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Figure 17 44-lead ceramic TSOP (10.16 × 18.415 × 3.842 mm) GG44A package outline, 002-33895

18 Acronyms

Table 19 Acronyms used in this document

Acronym	Description
$\overline{UB}$	upper byte
$\overline{LB}$	lower byte
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
EIA	Electronic Industries Alliance
F-RAM	ferroelectric random access memory
I/O	input/output
$\overline{OE}$	output enable
RoHS	Restriction of Hazardous Substances
RW	read and write
SRAM	static random access memory
TSOP	thin small outline package
$\overline{WE}$	write enable

19 Document conventions

19.1 Units of measure

Table 20 Units of measure

Symbol	Unit of measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohms
MHz	megahertz
MΩ	megaohms
µA	microamperes
µF	microfarads
µs	microseconds
mA	milliamperes
ms	milliseconds
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Revision history

Document version	Date of release	Description of changes
*C	2024-05-17	Release to web.
*D	2024-06-07	Updated “latch-up immunity” value in **Radiation performance**.

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