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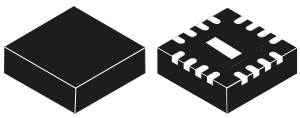
# A6983

Datasheet

# Automotive-grade 38 V, 3 A synchronous step-down converter with 25 µA quiescent current



QFN16 (3 x 3 mm)

| Maturity status link |
| --- |
| A6983 |

## Features

- AEC-Q100 qualified
- Operating temperature range: -40 °C to +150 °C for $T_j$
- 3.5 V to 38 V operating input voltage
- Load dump tolerant up to 40 V
- Output voltage from 0.85 V to $V_{IN}$
- 3.3 V and 5 V fixed output voltage versions
- 3 A DC output current
- 25 µA operating quiescent current
- Internal compensation network
- Two different versions: LCM for high efficiency at light-loads and LNM for noise-sensitive applications
- 2 µA shutdown current
- Internal soft-start
- High voltage $V_{IN}$ compatible enable
- Output overvoltage protection
- Output voltage sequencing
- Thermal protection
- 200 kHz to 2.3 MHz programmable switching frequency
- Optional spread spectrum for improved EMC
- Power Good
- Synchronization to external clock for LNM devices
- QFN16 (3 x 3 mm) package

## Applications

- Designed for automotive systems
- Battery-powered applications
- Car body applications (LCM)
- Car audio and low noise applications (LNM)
- Smart ambient lighting system supply

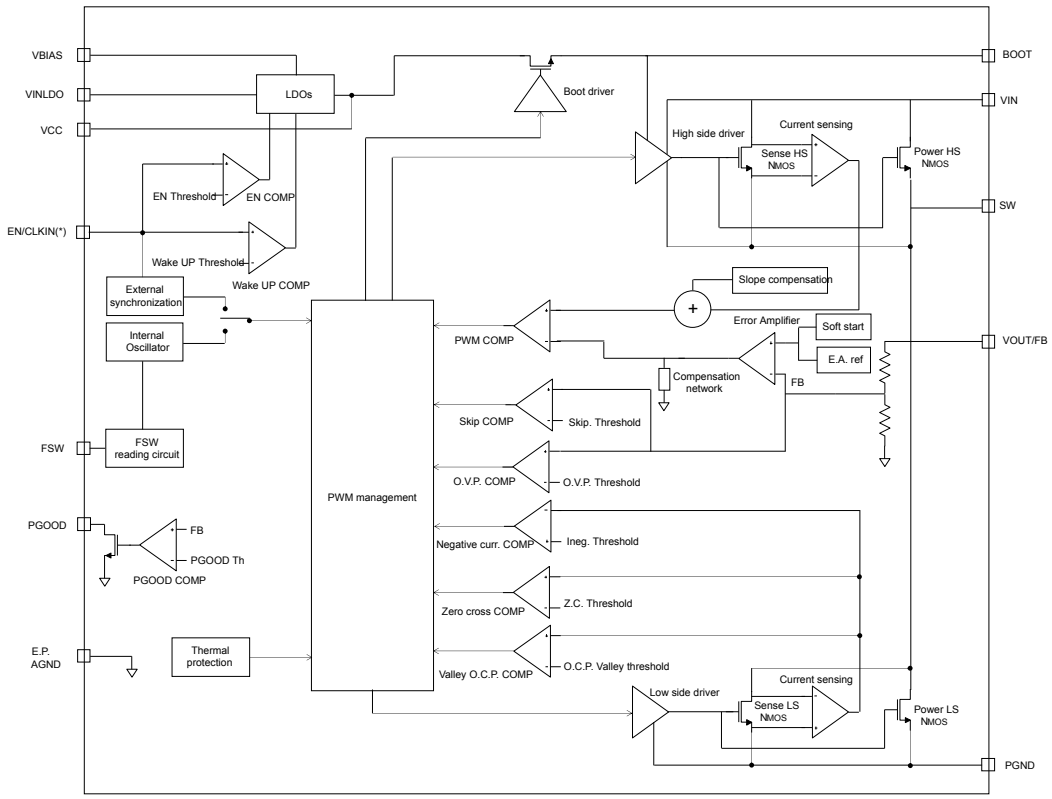
## Description

The A6983 is an easy-to-use synchronous monolithic step-down regulator capable of delivering up to 3 A DC to the load. The wide input voltage range makes the device suitable for a broad range of applications. The A6983 is based on peak current mode architecture and is packaged in a QFN16 (3 x 3 mm) with internal compensation thus minimizing design complexity and size. The “Low Consumption Mode” (LCM) is designed for applications active during car parking, so it maximizes the efficiency at the light-load with the controlled output voltage ripple. The “Low Noise Mode” (LNM) makes the switching frequency constant and minimizes the output voltage ripple overload current range, which meets the low noise application specification, such as for car audio. The A6983 allows the switching frequency to be selected in the 200 kHz to 2.3 MHz range with optional spread spectrum for improved EMC.

The EN pin provides enable/disable functionality. The typical shutdown current is 2 µA when disabled. As soon as the EN pin is pulled-up, the device is enabled, and the internal 1.3 ms soft-start takes place. The A6983 features a Power Good open collector that monitors the FB voltage. Pulse by pulse current sensing on both power elements implements an effective constant current protection, and thermal shutdown prevents thermal run-away.

# 1 Diagram

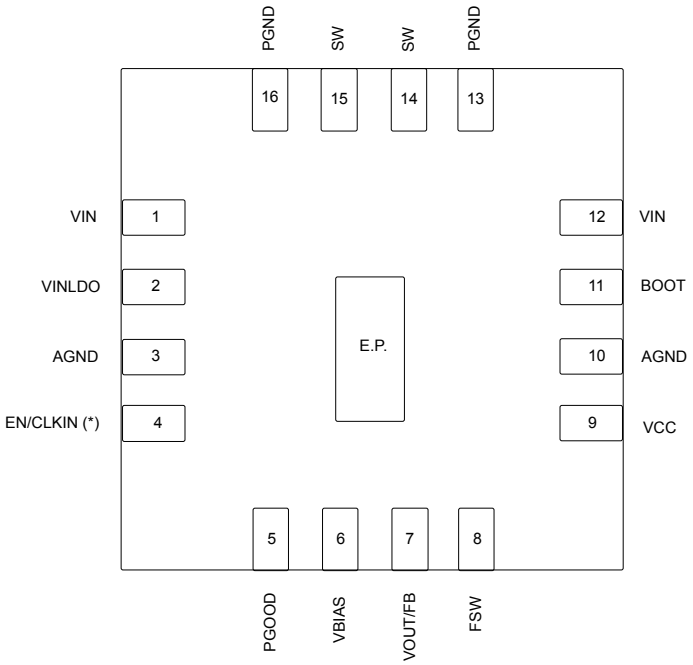
**Figure 1. Block diagram**




*Note: (*) External synchronization (available for low noise mode only).*

# 2 Pin configuration

**Figure 2. Pin connection QFN16 package (top view)**




*Note: (*) External synchronization (available for low noise mode only).*

**Table 1. Pin description**

| Pin n° | Symbol | Function |
|---|---|---|
| 1 | VIN | DC input voltage. |
| 2 | VINLDO | DC input voltage is connected to the supply rail by a simple RC filter. |
| 3 | AGND | Analog ground. |
| 4 | EN / CLKIN | Enable pin with internal voltage divider. Pull down/up to disable/enable the device.<br>In LNM versions, this pin is also use to provide an external clock signal, which synchronizes the device. |
| 5 | PGOOD | The PGOOD open collector output is driven to low impedance when the output voltage is out of regulation and released once the output voltage becomes valid. |
| 6 | VBIAS | Typically connected to the regulated output voltage, an external voltage source can be used to supply part of the analog circuitry to reduce current consumption at light-load. Connect to AGND if not used. |
| 7 | VOUT/FB | This pin operates as VOUT or FB according to the selected part number. In fixed output voltage versions, VOUT is the output voltage sensing with the selected internal voltage divider.<br>In adjustable versions, FB is output voltage sensing with the external voltage divider. |
| 8 | FSW | Connect an external resistor to program the oscillator frequency and enable optional dithering. |
| 9 | VCC | This pin supplies the embedded analog circuitry. Connect a ceramic capacitor (≥ 1 µF) to filter the internal voltage reference. |
| 10 | AGND | Analog ground. |
| 11 | BOOT | Connect an external capacitor (100 nF typ.) between the BOOT and SW pins. The gate charge required to drive the internal nMOS is refreshed during the low-side switch conduction time. |
| 12 | VIN | DC input voltage. |
| 13 | PGND | Power ground. |

| Pin n° | Symbol | Function |
|---|---|---|
| 14 | SW | Switching node. |
| 15 | SW | Switching node. |
| 16 | PGND | Power ground. |
| - | Exposed PAD | Exposed pad must be connected to AGND, PGND. |

# 3 Typical application circuit

Figure 3. **Basic application (adjustable version)**

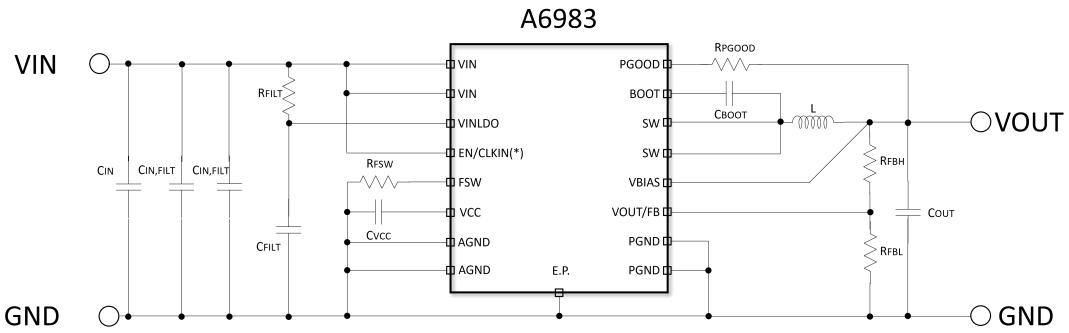



Figure 4. **Basic application (fixed $V_{OUT}$ version)**

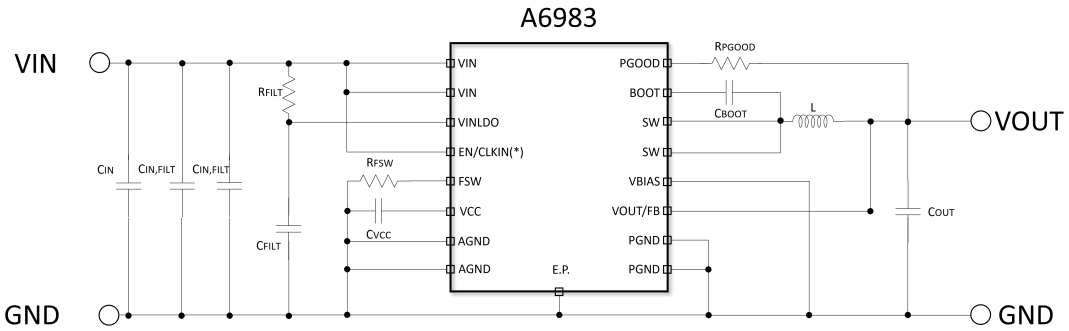



Table 2. **Typical application components**

| Symbol | Value | Description |
|---|---|---|
| $C_{IN}$ | 10 µF | Input capacitor |
| $R_{FILT}$ | 0.1 kΩ | VINLDO filter resistor |
| $C_{IN\ ,FILT}$ | 1 µF | VIN filter capacitor |
| $C_{FILT}$ | 1 µF | VINLDO filter capacitor |
| $C_{VCC}$ | 1 µF | VCC bypass capacitor |
| $C_{BOOT}$ | 100 nF | Bootstrap capacitor |
| $C_{OUT}$ | 40 µF | Output capacitor |
| $R_{FBH}$ | 400 kΩ | VOUT divider upper resistor (only for adjustable version) |
| $R_{FBL}$ | 82 kΩ | VOUT divider lower resistor (only for adjustable version) |
| L | 15 µH (Fsw = 0.4 MHz) | Output inductor |
| $R_{PGOOD}$ | 1 MΩ | PGOOD resistor |

# 4 Maximum ratings

## 4.1 Absolute maximum ratings

Stressing the device above the ratings listed in Table 3 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| VIN | Maximum pin voltage | -0.3 | 42 | V |
| AGND | Maximum pin voltage | 0 | 0 | V |
| PGND | Maximum pin voltage | -0.3 | 0.3 | V |
| BOOT | Maximum pin voltage | SW -0.3 | SW +4 | V |
| VCC | Maximum pin voltage | -0.3 | Min. (VIN +0.3; 4) | V |
| VOUT/FB | Maximum pin voltage | -0.3 | 8 | V |
| FSW | Maximum pin voltage | -0.3 | VCC +0.3 | V |
| VBIAS | Maximum pin voltage | -0.3 | VIN +0.3 | V |
| EN | Maximum pin voltage | -0.3 | VIN +0.3 | V |
| PGOOD | Maximum pin voltage | -0.3 | VIN +0.3 | V |
| SW | Maximum pin voltage | -0.85 | VIN +0.3 | V |
| | | -3.8 for 0.5 ns (1) | | V |
| TJ | Operating temperature range | -40 | 150 | °C |
| TSTG | Storage temperature range | -65 | 150 | °C |
| TLEAD | Lead temperature (soldering 10 sec.) | | 260 | °C |
| IHS, ILS | High-side/low-side RMS switch current | | 3 | A |

1. *Negative peak voltage during switching activities caused by parasitic layout elements.*

## 4.2 ESD protection

**Table 4. ESD performance**

| Symbol | Parameter | Test conditions | Value | Unit |
|---|---|---|---|---|
| ESD | ESD protection voltage | HBM | 2 | kV |
| | | CDM (corner pins) | 750 | V |
| | | CDM | 500 | |

## 4.3 Thermal characteristics

**Table 5. Thermal data**

| Symbol | Parameter | Package | Value | Unit |
|---|---|---|---|---|
| $R_{th\_JA}$ | Thermal resistance junction ambient (device soldered on the STMicroelectronics® demonstration board, refer to Section 11: Application board ) | QFN-16 WF | 40 | °C/W |

# 5 Electrical characteristics

$T_J$ = -40 to +150 °C, $V_{IN}$ = 12 V unless otherwise specified.

**Table 6. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Operating input voltage range | | 3.5 | | 38 | V |
| $V_{INH}$ | $V_{CC}$ rising threshold | | 2.3 | | 3.3 | V |
| $V_{INL}$ | $V_{CC\ UVLO}$ falling threshold | | 2.15 | | 3.15 | V |
| $I_{PK}$ (1) | Peak current limit | Duty cycle < 40% | 4.1 | 4.6 | | A |
| | | Duty cycle = 99%<br>Closed loop operation | 3.1 | 3.6 | | A |
| $I_{VY}$ (1) | Valley current limit | | 3.3 | 3.9 | 4.6 | A |
| $I_{SKIP}$ (1) (2) | Skip current limit | | | 0.6 | | A |
| $I_{VY\_SINK}$ (1) | Reverse current limit | LNM or VOUT overvoltage | 1.25 | 1.5 | 1.75 | A |
| $R_{DSON\_HS}$ | High-side RDSON | | | 0.130 | 0.26 | Ω |
| $R_{DSON\_LS}$ | Low-side RDSON | | | 0.085 | 0.18 | Ω |
| $T_{OFF\_MIN}$ | Minimum off time | | | 200 | | ns |
| $T_{ON\_MIN}$ | Minimum on time | | | 75 | 100 | ns |
| **Enable** | | | | | | |
| $V_{WAKE\_UP}$ | Wake-up threshold | Rising | | | 0.7 | V |
| | | Falling | 0.2 | | | V |
| $V_{EN}$ | Enable threshold | Rising | 1.08 | 1.2 | 1.32 | V |
| | | Hysteresis | | 0.2 | | V |
| **VCC regulator** | | | | | | |
| $V_{CC}$ | LDO output voltage | | 3.0 | 3.3 | 3.6 | V |
| **Power consumption** | | | | | | |
| $I_{SHTDWN}$ | Shutdown current from $V_{IN}$ | VEN = GND | | 2 | 3 | µA |
| **LCM device** | | | | | | |
| $I_{Q\_VIN}$ | Quiescent current from $V_{IN}$<br>Section 7.4.5 | VBIAS = GND | 20 | 35 | 70 | µA |
| | | VBIAS = 5 V | 1 | 3.5 | 6 | µA |
| $I_{Q\_VBIAS}$ | Quiescent current from VBIAS | VBIAS = 5 V | 20 | 35 | 70 | µA |
| **LNM device** | | | | | | |
| $I_{Q\_VIN}$ | Quiescent current from $V_{IN}$ | VBIAS = GND | 1.6 | 2.3 | 3 | mA |
| | | VBIAS = 5 V | 300 | 550 | 800 | µA |
| $I_{Q\_VBIAS}$ | Quiescent current from VBIAS | VBIAS = 5 V | 1.3 | 1.8 | 2.3 | µA |
| **Soft-start** | | | | | | |
| $T_{SS}$ | Internal soft-start | | 1 | 1.3 | 1.6 | ms |
| **Error amplifier** | | | | | | |
| $V_{FB}$ | Voltage feedback | Adjustable version<br>$T_J$ = 25 °C | 0.845 | 0.85 | 0.855 | V |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{FB}$ | Voltage feedback | Adjustable version<br>-40 °C ≤ $T_J$ ≤ +150 °C | 0.837 | 0.85 | 0.859 | V |
| | | Fixed 3.3 V version<br>$T_J$ = 25 °C | 3.27 | 3.3 | 3.33 | V |
| | | Fixed 3.3 V version<br>-40 °C ≤ $T_J$ ≤ +150 °C | 3.254 | 3.3 | 3.346 | V |
| | | Fixed 5.0 V version<br>$T_J$ = 25 °C | 4.955 | 5.0 | 5.045 | V |
| | | Fixed 5.0 V version<br>-40 °C ≤ $T_J$ ≤ +150 °C | 4.93 | 5 | 5.07 | V |
| **Overvoltage protection** | | | | | | |
| $V_{OVP}$ | Overvoltage trip ($V_{OVP}/V_{REF}$) | | 115 | 120 | 125 | % |
| $V_{OVP\_HYST}$ | Overvoltage hysteresis | | 1 | 2 | 6 | % |
| **Synchronization (LNM versions only)** | | | | | | |
| $f_{CLKIN}$ (3) | Synchronization range | | 200 | | 2200 | kHz |
| $V_{CLKIN\_TH}$ (3) | Amplitude of synchronization clock | | 2.3 | | | V |
| $V_{CLKIN\_T}$ (3) (5) | Synchronization pulse ON and OFF time 2.3 ≤ $V_{CLKIN\_TH}$ ≤ 2.5 V | $V_{CLKIN\_TH}$ = 2.3 V | 60 | | | ns |
| | Synchronization pulse ON and OFF time $V_{CLKIN\_TH}$ > 2.5 V | | 20 | | | ns |
| **Power Good** | | | | | | |
| $V_{THR}$ | PGOOD threshold | Adjustable output version<br>-40 °C ≤ $T_J$ ≤ +150 °C | 87 | 90 | 93 | % |
| | | Fixed 3.3 output version<br>-40 °C ≤ $T_J$ ≤ +150 °C | 87 | 90 | 93 | % |
| | | Fixed 5.0 output version<br>-40 °C ≤ $T_J$ ≤ +150 °C | 87 | 90 | 93 | % |
| $V_{THR\_HYST}$ (4) | PGOOD hysteresis<br>(QFN version only) | | | 3 | | % |
| $V_{PGOOD}$ | PGOOD open collector output | VIN > VINH and<br>VFB < VTH<br>4 mA sinking load | | | 0.4 | V |
| | | 2 < VIN < VINH<br>4 mA sinking load | | | 0.8 | V |
| $T_{SHDWN}$ (5) | Thermal shutdown temperature | | | 165 | | °C |
| $T_{HYS}$ (5) | Thermal shutdown hysteresis | | | 30 | | °C |

1. *Parameter tested in a static condition during the testing phase. The parameter value may change over a dynamic application condition.*
2. *LCM version.*
3. *LNM version.*
4. *Specifications in the -40 to +150 °C temperature range are assured by characterization and statistical correlation.*
5. *Not tested in production.*

## 5.1 Frequency selection table

All the populations are tested at $T_J$ = -40 to +150 °C, $V_{IN}$ = 12 V unless otherwise specified.

**Table 7. FSW selection**

| Symbol | Option | RVCC (KΩ) | RGND (KΩ) | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| FSW | Dithering | 1.8 | N.C. | | 200 | | kHz |
| | | 0 | N.C. | | 400 | | kHz |
| | | 3.3 | N.C. | | 500 | | kHz |
| | | 5.6 | N.C. | | 700 | | kHz |
| | | 10 | N.C. | | 1000 | | kHz |
| | | 18 | N.C. | | 1500 | | kHz |
| | | 33 | N.C. | | 2000 | | kHz |
| | | 56 | N.C. | | 2300 | | kHz |
| | No dithering | N.C. | 1.8 | | 200 | | kHz |
| | | N.C. | 0 | 360 | 400 | 440 | kHz |
| | | N.C. | 3.3 | | 500 | | kHz |
| | | N.C. | 5.6 | 630 | 700 | 770 | kHz |
| | | N.C. | 10 | | 1000 | | kHz |
| | | N.C. | 18 | | 1500 | | kHz |
| | | N.C. | 33 | 1800 | 2000 | 2300 | kHz |
| | | N.C. | 56 | 2000 | 2300 | 2600 | kHz |

# 6 Datasheet parameters over the temperature range

100% of the population in the production flow is tested at three different ambient temperatures (-40 °C, +25 °C, and +150 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C to +150 °C). The device operation is guaranteed when the junction temperature is inside the (-40 °C to +150 °C) temperature range. The designer can estimate the silicon temperature increase with respect to the ambient temperature, evaluating the internal power losses generated during the device's operation. However, the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the $T_{SHTDWN}$ (+165 °C typ.) temperature. All the datasheet parameters can be guaranteed to a maximum junction temperature of +150 °C to avoid triggering the thermal shutdown protection during the testing phase because of self-heating.

# 7 Functional description

The A6983 device is based on a “peak current mode" architecture with constant frequency control. Therefore, the intersection between the error amplifier output and the sensed inductor current generates the PWM control signal to drive the power switch.

According to the selected part number, the device can feature LNM (low noise mode) or LCM (low consumption mode).

LNM forces the regulator to work in forced PWM mode to reduce noise. LCM prevents the inductor current to go below zero and allows the regulator to skip pulses to increase the efficiency at light-load.

The main internal blocks shown in Figure 1 and Figure 2 are:

- Embedded power elements.
- A fully integrated adjustable oscillator, which is able to set eight different switching frequencies from 200 to 2300 kHz.
- The ramp for the slope compensation avoiding subharmonic instability.
- A transconductance error amplifier with integrated compensation network.
- The high-side current sense amplifier to sense the inductor current.
- A“Pulse Width Modulator” (PWM) comparator and the driving circuitry of the embedded power elements.
- The soft-start block, which ramps up the reference voltage on the error amplifier thus decreasing the inrush current at power-up. The EN pin inhibits the device when driven low.
- The EN/CLK pin section, which, for LNM versions, allows the synchronization of the device to an external clock generator.
- The pulse by pulse high-side/low-side switch current sensing to implement the constant current protection.
- A circuit to implement the thermal protection function.
- The OVP circuitry to discharge the output capacitor in case of an overvoltage event.
- The switchover capability of the internal regulator to supply a portion of the quiescent current when the VBIAS pin is connected to an external output voltage.
- An enable/disable dithering operation.

## 7.1 Enable

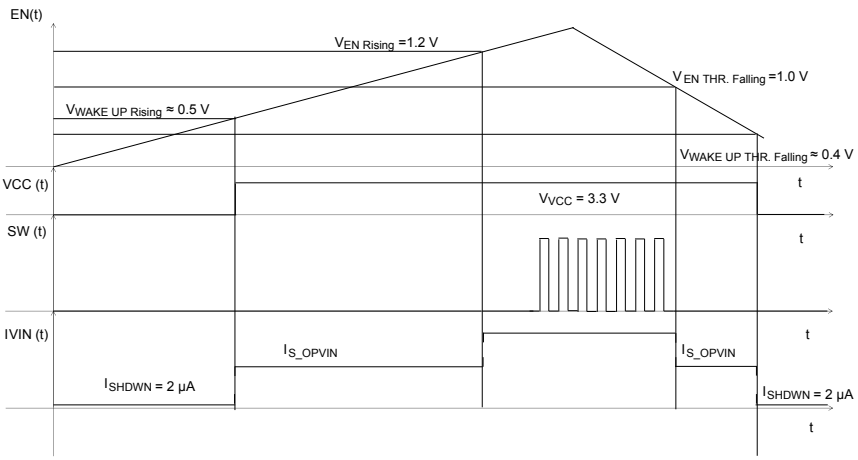
The EN pin is a digital input that turns the device on or off.

In order to maximize both the EN threshold accuracy and the current consumption, the device implements two different thresholds:

1. The wake-up threshold, VWAKE_UP = 0.5 V (see Table 6)
2. The start-up threshold, $V_{EN}$ = 1.2 V (see Table 6)

The following picture shows the device behavior:

**Figure 5. Power-up/down behavior**



When the voltage applied on the EN pin rises over $V_{WAKEUP, RISING}$, the device powers up the internal circuit thus increasing the current consumption.

As soon as the voltage rises over the $V_{EN, RISING}$, the device starts the switching activities as described in Section 7.2

Once the voltage becomes lower than $V_{EN, FALLING}$, the device interrupts the switching activities.

As soon as the voltage becomes lower than $V_{WAKEUP.FALLING}$, the device powers down the internal circuit reducing the current consumption.

The pin is $V_{IN}$ compatible.

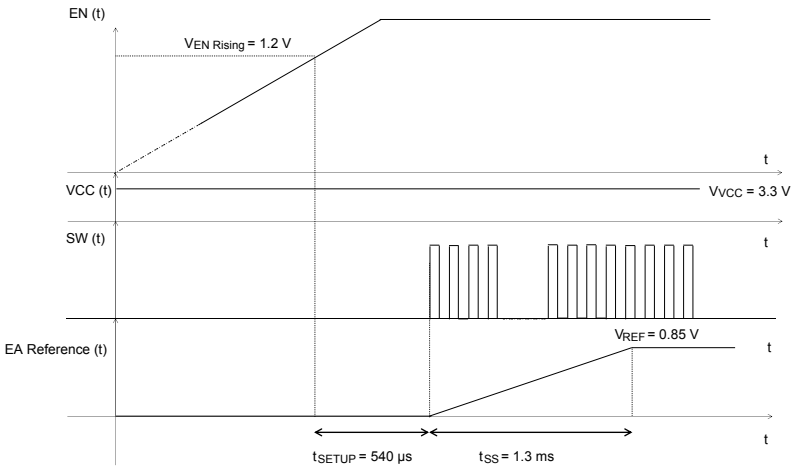
Refer to Table 6 for the reported thresholds.

## 7.2 Soft-start

The soft-start (SS) limits the inrush current surge and makes the output voltage increase monotonically.

The device implements the soft-start phase ramping the internal reference in very small steps. Once the SS ends, the error amplifier reference is switched to the internal value of 0.85 V, which comes directly from the bandgap cell.

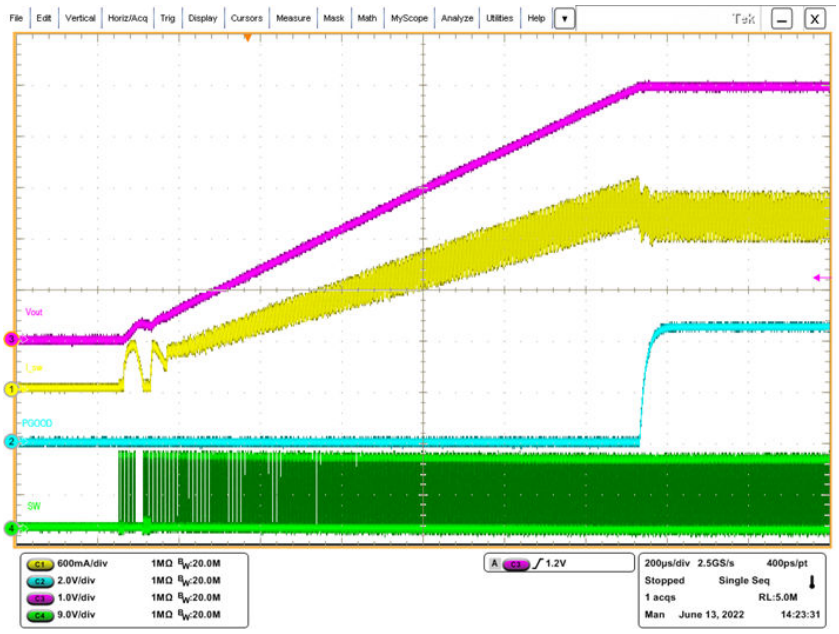
**Figure 6. Soft-start procedure**




During normal operation, a new soft-start cycle takes place in the case of a:

1. Thermal shutdown event
2. UVLO event
3. EN pin rising over the $V_{EN}$ threshold. Refer to Table 6

Figure 7. **Soft-start phase with $I_{OUT}$ = 2.0 A**




## 7.3 Undervoltage lockout

The device implements the undervoltage lockout (UVLO) by continuously sensing the voltage on the $V_{CC}$ pin. Thus, if the UVLO lasts more than 10 µs, the internal logic resets the device by turning off both LS and HS. After the reset, if the EN pin is still high, the device repeats the soft-start procedure.

## 7.4 Light-load operation

The A6983 implements two different light-load strategies:

1. Low consumption mode (LCM)
2. Low noise mode (LNM)

Please refer to Table 12 to select the part number with the preferred light-load strategy.

### 7.4.1 Low consumption mode (LCM)

The LCM maximizes the efficiency at light-load.

When the switch peak current request is lower than the $I_{SKIP}$ threshold (see Table 6), the device regulates $V_{OUT}$ by the skip threshold. The minimum voltage is given by:

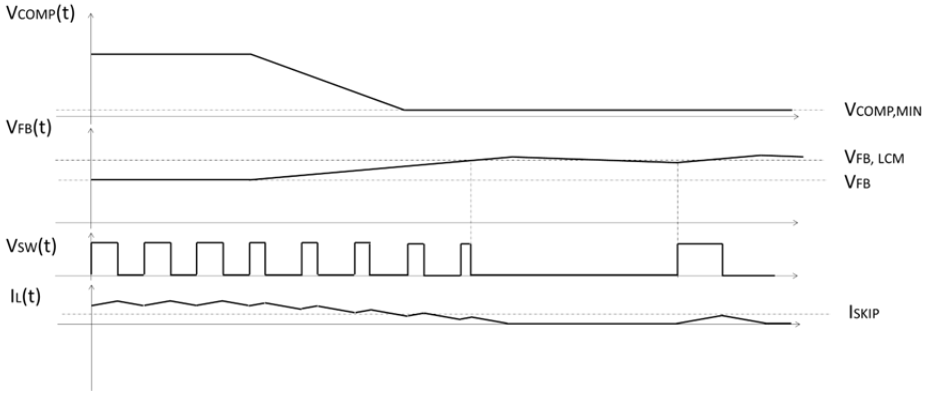
$$V_{OUT,\,LCM} = V_{FB,\,LCM} \cdot \frac{R_{PH} + R_{PL}}{R_{PL}} \quad (1)$$

Where $V_{FB,LCM}$ is 1.8% (typ.) higher than $V_{FB}$.

The device interrupts the switching activities when two conditions happen together:

1. The peak inductor current required is lower than $I_{SKIP}$
2. The voltage on the FB pin is higher than VFB, LCM

Figure 8. **Light-load operation**




A new switching cycle takes place once the voltage on the FB pin becomes lower than $V_{FB,LCM}$. The HS switch is kept on until the inductor current reaches $I_{SKIP}$.

Once the current on the HS reaches the defined value, the device turns the HS off and turns the LS on. The LS is kept enabled until one of the following conditions occurs:

1. The inductor current sensed by the LS becomes equal to zero
2. The switching period ends

If, at the end of the switching cycle, the voltage on the FB pin rises over the $V_{FB,LCM}$ threshold, the LS is kept enabled until the inductor current becomes equal to zero. Otherwise, the device turns on the HS again and starts a new switching pulse.

During the burst pulse, if the energy transferred to $C_{OUT}$ increases the VFB level over the threshold defined in Eq. (1), the device interrupts the switching activities. The new cycle takes place only when VFB becomes lower than the defined threshold. Otherwise, as soon as the LS is turned off, the HS is turned on.

Given the energy stored in the inductor during a burst, the voltage ripple depends on the capacitor value:

$$V_{OUT\ RIPPLE} = \frac{\Delta Q_{IL}}{C_{OUT}} = \frac{\int_0^{T_{BURST}} I_L(t)\,dt}{C_{OUT}} \quad (2)$$

Figure 9. **LCM operation with ISKIP = 600 mA typ. at zero load. L = 15 µH; COUT = 40 µF**

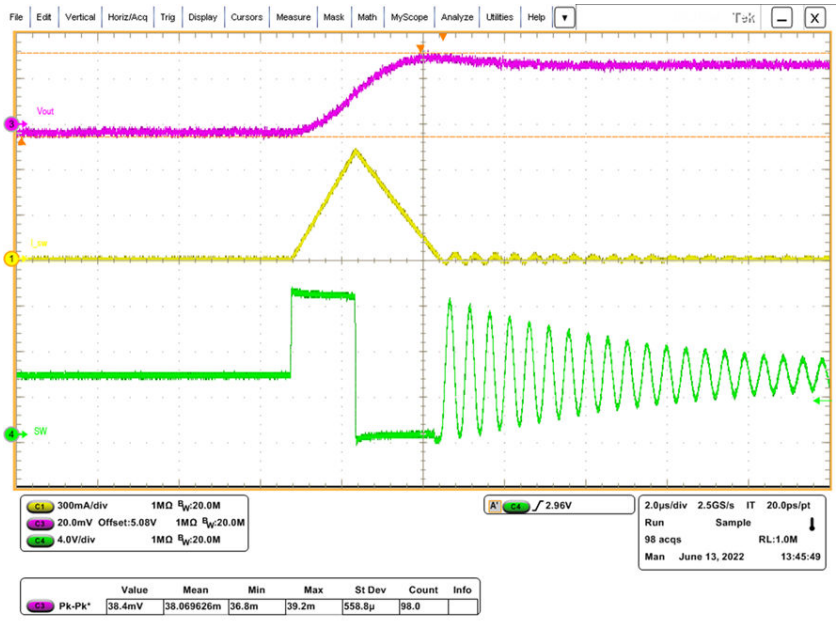


Figure 10. **LCM operation over loading condition (part 1-pulse skipping)**

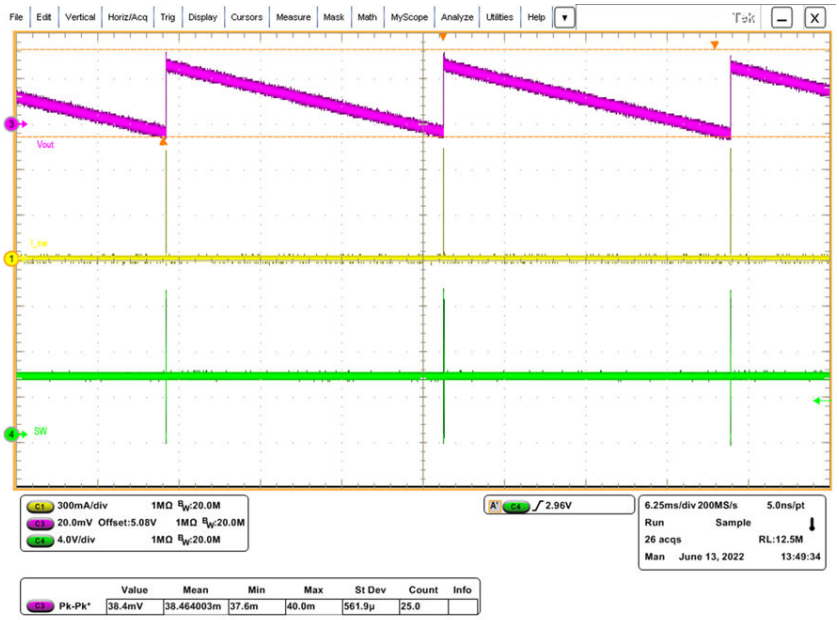



Figure 11. **LCM operation over 15 mA load condition (part 2-pulse skipping)**

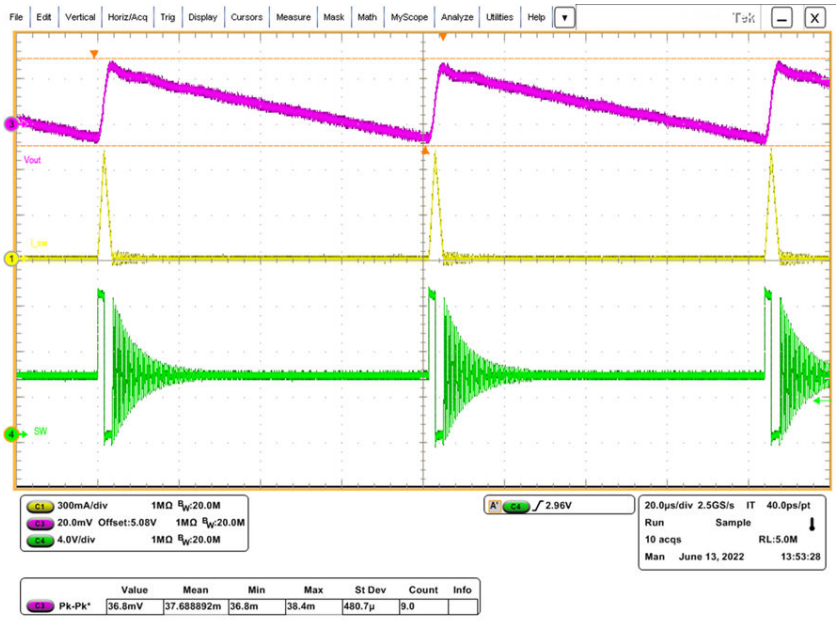


Figure 12. **LCM operation over 100 mA load condition (part 3-pulse skipping)**

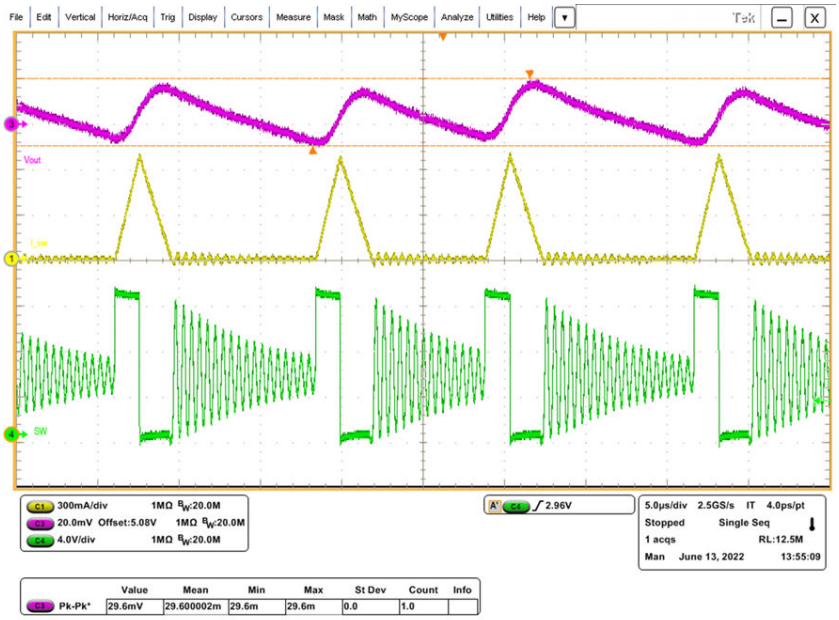
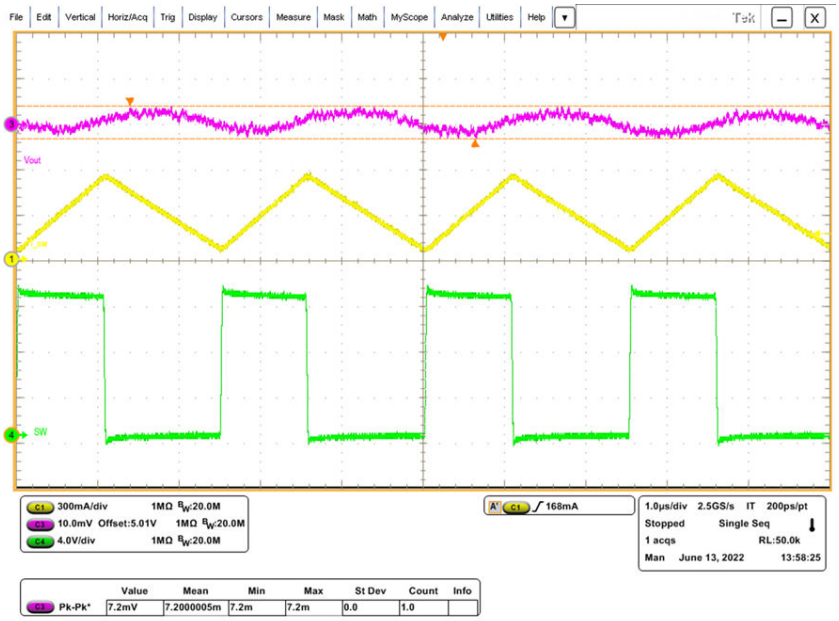



Figure 13. **LCM operation over 300 mA load condition (part 4-CCM)**




### 7.4.2 Low noise mode (LNM)

The LNM implements a forced PWM operation over the different loading conditions. The LNM features a constant switching frequency to minimize the noise in the final application and a constant voltage ripple at fixed $V_{IN}$.

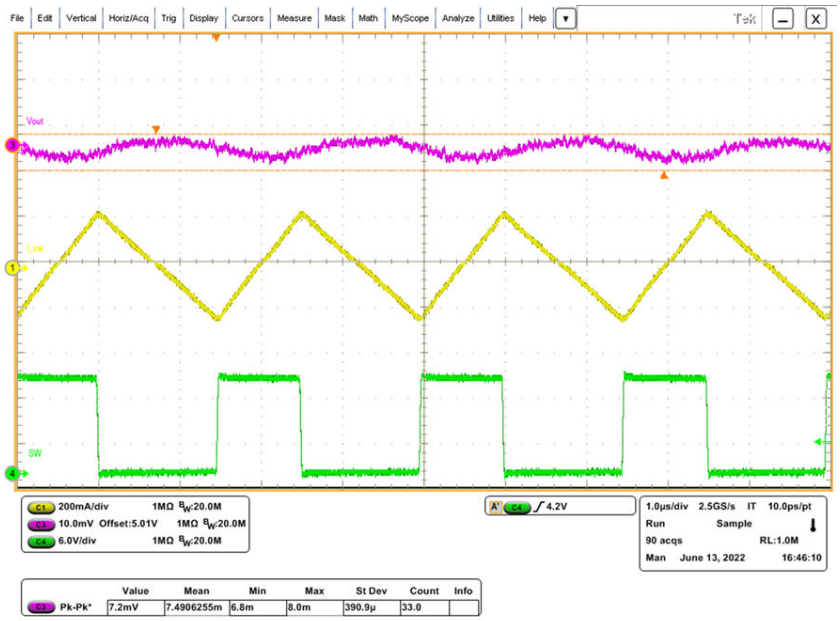
The regulator in steady loading conditions, operates in continuous conduction mode (CCM) in the different loading conditions.

The triangular-shaped current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, that depends on the capacitor value and the equivalent resistive component (ESR). Consequently, the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

$$V_{OUT\ RIPPLE} = ESR \cdot \Delta I_{LMAX} + \frac{\Delta I_{LMAX}}{8 \cdot C_{OUT} \cdot f_{SW}} \quad (3)$$

Usually, the resistive component of the ripple can be neglected if the selected output capacitor is a multilayer ceramic capacitor (MLCC).

**Figure 14. Low noise mode operation at zero load**




### 7.4.3 Efficiency for low consumption mode and low noise mode part number

Figure 15 and Figure 16 report the efficiency measurements to highlight the gap at the light-load between LNM and LCM part numbers. The graph also reports exactly the same efficiency at the medium/high-load.

**Figure 15. Light-load efficiency for low consumption mode and low noise mode - linear scale. VIN = 12 V; VOUT = 5 V; FSW = 400 kHz**

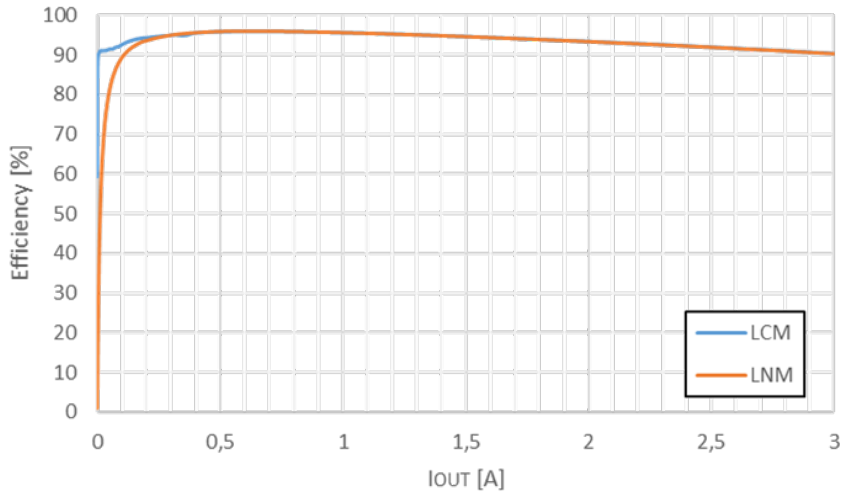
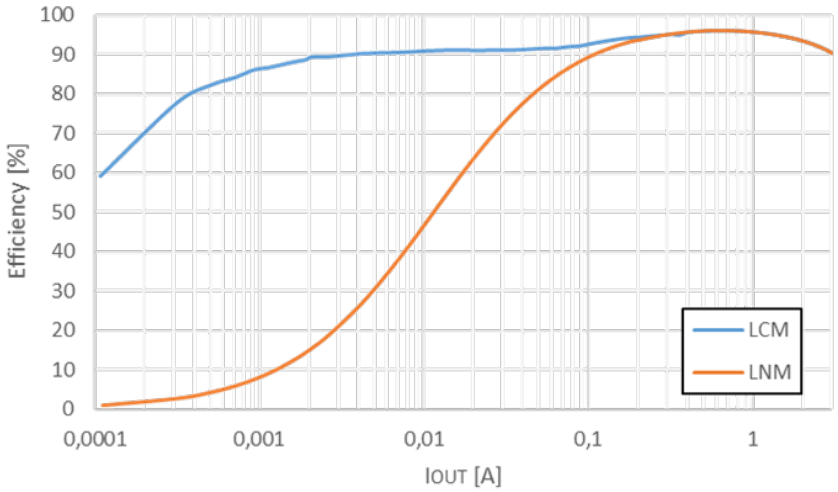


Figure 16. **Light-load efficiency for low consumption mode and low noise mode - log scale. VIN = 12 V; VOUT = 5 V; FSW = 400 kHz**




### 7.4.4 Load regulation for low consumption mode and low noise mode part number

Figure 17 and Figure 18 show the load regulation and highlight the gap between them. The gap is caused by the different regulation strategies used at the light-load between LNM and LCM part numbers. When the required $I_{OUT}$ is higher than the threshold defined in Section 7.4.1 the behavior of the different part number is exactly the same.

Figure 17. **Load regulation for LCM and LNM. VIN = 12 V; VOUT = 5 V; FSW = 400 kHz - linear scale**

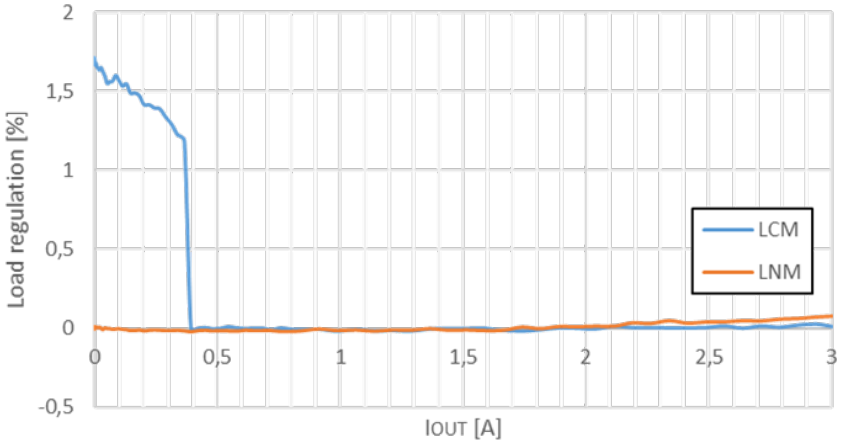
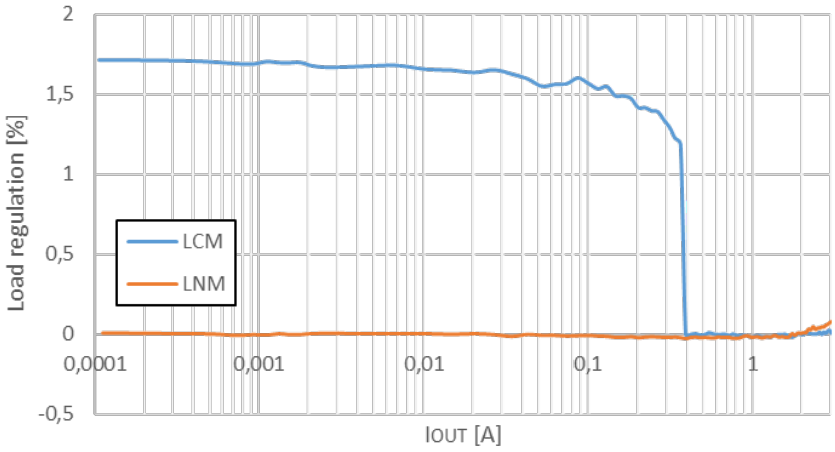


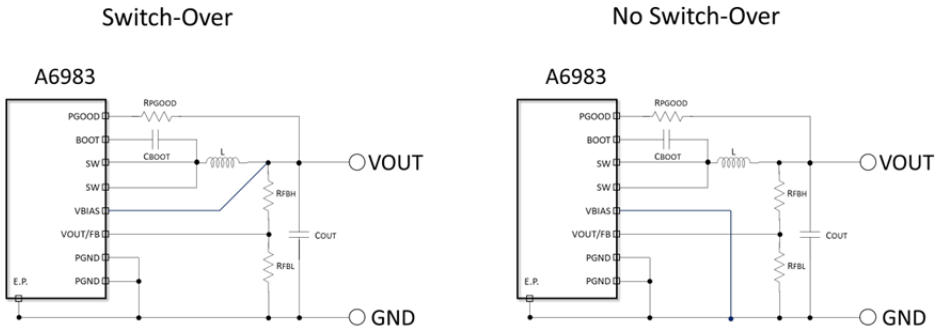
Figure 18. **Load regulation for LCM and LNM. VIN = 12 V; VOUT = 5 V; FSW = 400 kHz - log scale**




### 7.4.5 Switch-over feature

The switch-over maximizes the efficiency at the light-load that is crucial for low consumption applications.

Figure 19. **Switch-over**




In order to minimize the regulator quiescent current sink from the input voltage, the $V_{BIAS}$ pin can be connected to an external voltage source in the range of 3.0 V < $V_{BIAS}$ < $V_{IN}$. The external power supply connected to the $V_{BIAS}$ pin must be disabled when the voltage on the EN pin is lower than $V_{WAKE\_UP}$.

In the case that the $V_{BIAS}$ pin is connected to the regulated output voltage ($V_{OUT}$), the total current drawn from the input voltage is given by the following equation:

$$I_{QVIN} = I_{QOPVIN} + \frac{1}{\eta_{A6983}} \cdot \frac{V_{BIAS}}{V_{IN}} \cdot I_{QOPVBIAS} \quad (4)$$

### 7.4.6 Spread spectrum

The spread spectrum, helpful in improving EMC performance, is selectable by connecting the RFSW resistor to $V_{CC}$ (refer to Table 7).

The internal dithering circuit changes the switching frequency in a range of ±5%.

$$\Delta F_{SW} = 5\% \cdot F_{sw} \quad (5)$$

The device updates the frequency every clock period by fixed steps:

- Ramps up in 63 steps from minimum to maximum FSW
- Ramps down in 63 steps from maximum to minimum FSW

The modulation shape is almost triangular with a frequency of:

$$F_{Dithering} = \frac{F_{sw}}{126} \quad (6)$$

**Figure 20. Spread spectrum switching frequency time trend (FSW = 400 [kHz])**

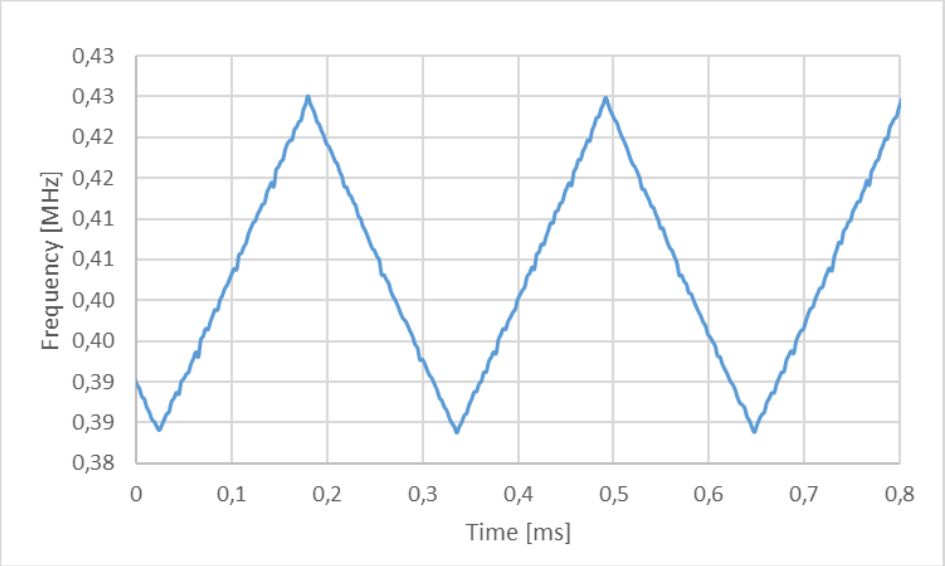
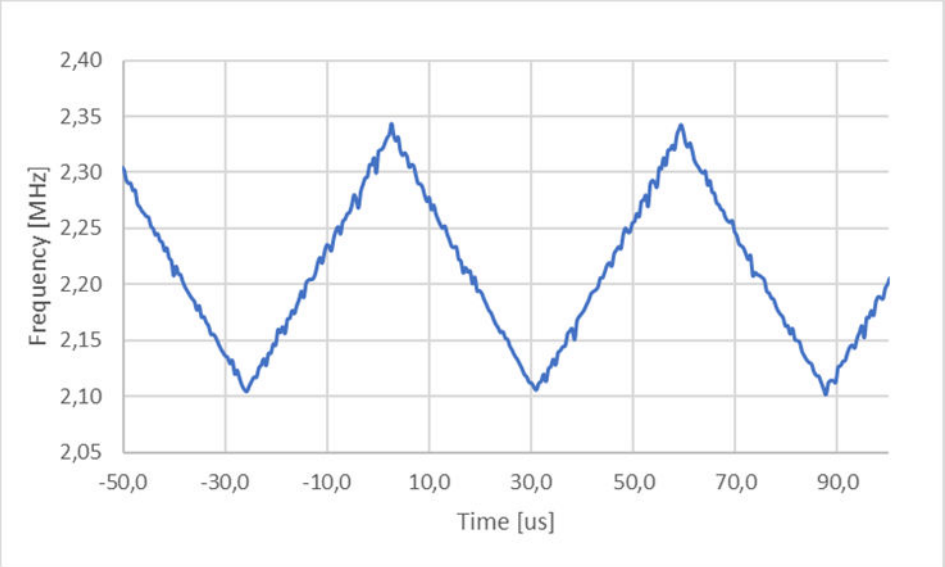



**Figure 21. Spread spectrum switching frequency time trend (FSW = 2.300 [MHz])**




### 7.4.7 Overvoltage protection

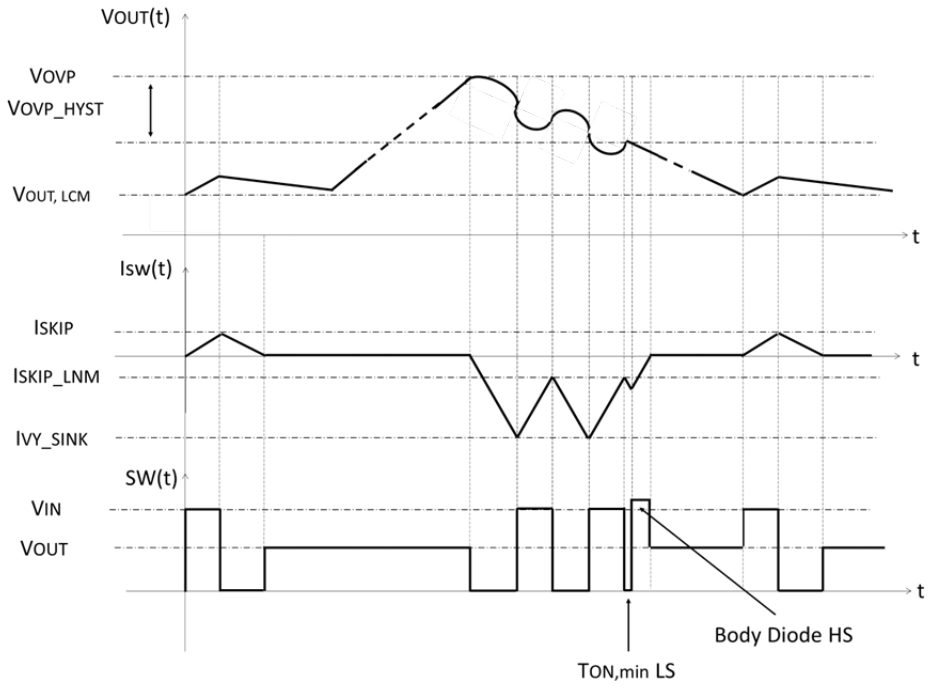
The overvoltage is a second level protection, and it should never be triggered in normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance determined by the compensation network should guarantee an output voltage regulation within the overvoltage threshold even during a worst-case scenario in terms of load transitions. The protection is reliable and able to operate even during normal load transitions for a system whose dynamic performance is not in line with the load dynamic request. Consequently, the output voltage regulation would be affected.

#### 7.4.7.1 *Low consumption mode part number*

The overvoltage protection continuously compares the FB pin with 120% nominal output voltage and enables the low-side MOSFET at the beginning of the switching cycle, keeping it active until the 1.5 A typ. negative current limitation is reached, in order to discharge the output capacitor.

The following graph shows the LCM part number behavior during an OVP event.

**Figure 22. Overvoltage protection behavior LCM part numbers**

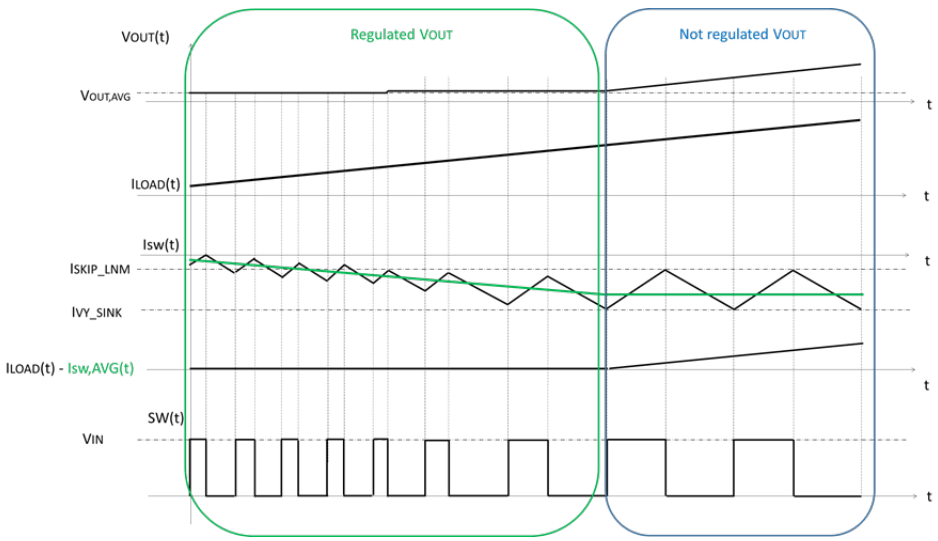



As soon as the output voltage goes out of the OVP hysteresis (typ. 2%) the A6983 device sets the switching node on high impedance. It restarts the switching activity accordingly with the main loop regulation of the peak current mode architecture.

#### 7.4.7.2 *Low noise mode part number*

The following graph shows the LNM part number behavior during an OVP event.

**Figure 23. Overvoltage protection behavior LNM part number**



The LNM device regulates the output voltage with a valley sinking capability down to the negative current limitation ($I_{VY\_SINK}$) in Figure 23.

This hysteretic operating mode between peak current mode threshold (ISKIP_LNM) and modulated low-side switch conduction time for VOUT regulation persists until the valley current level triggers the negative current limitation ($I_{VY\_SINK}$), that is the maximum sinking capability of the device (highlighted in green in Figure 23).

If the source injection further increases, the output voltage is a partitioning between the source impedance and maximum sinking capability described above (highlighted in blue in Figure 23).

### 7.4.8 Overcurrent protection

The current protection circuitry features a constant current protection, so the device limits the maximum peak current (refer to Table 6) in an overcurrent condition.

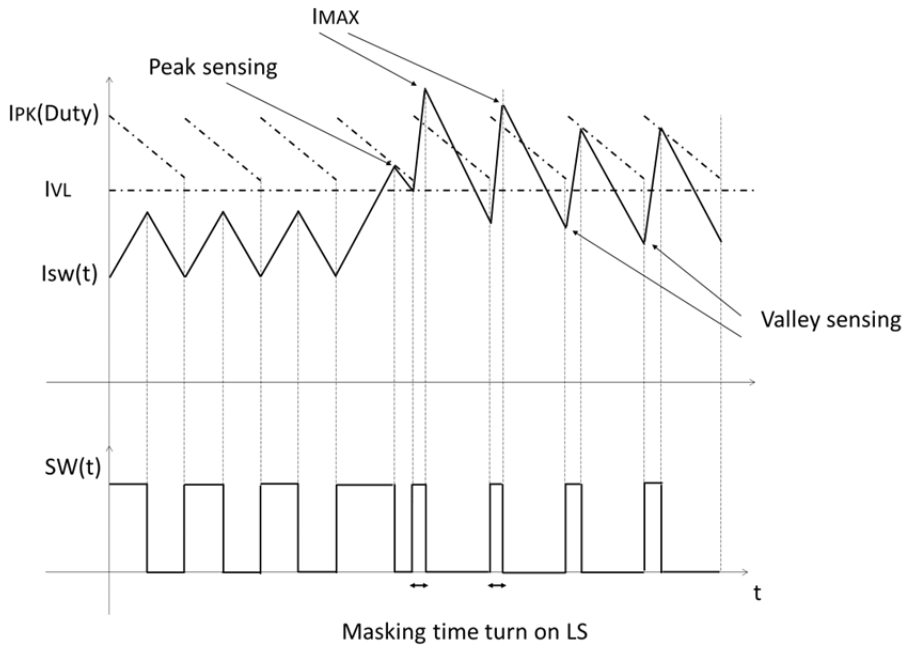
The A6983 device implements a pulse by pulse current sensing on both power elements (high-side and low-side switches) for effective current protection over the duty cycle range. The high-side current sensing is called “peak” and the low-side current sensing “valley.”

The internal noise generated during the switching activity makes the current sensing circuitry ineffective for a minimum conduction time of the power element. This time is called “masking time” because the information from the analog circuitry is masked by the logic to prevent an erroneous detection of the overcurrent event. Therefore, the peak current protection is disabled for a masking time after the high-side switch is turned on. The masking time for the valley sensing is activated after the low-side switch is turned on. In other words, the peak current protection can be ineffective at extremely low duty cycles, and the valley current protection at extremely high duty cycles.

The A6983 device assures an effective overcurrent protection sensing the current flowing in both power elements. In case one of the two current sensing circuitry is ineffective because of the masking time, the device is protected sensing the current on the opposite switch. Thus, the combination of the “peak” and “valley” current limits assure the effectiveness of the overcurrent protection even in extreme duty cycle conditions.

In case the current diverges because of the high-side masking time, the low-side power element is turned on until the switch current level drops below the valley current sense threshold. The low-side operation is able to prevent the high-side turn on, so the device can skip pulses decreasing the switching frequency.

**Figure 24. Overcurrent protection behavior**




In a worst case scenario, reported in Figure 24, the switch current is limited to:

$$I_{MAX} = I_{VY} + \frac{V_{IN} - V_{OUT}}{L} \cdot T_{MASKHS} \quad (7)$$

Where IVY is the current threshold of the valley sensing circuitry (refer to Table 6) and $T_{MASKHS}$ is the masking time of the high-side switch (75 ns typ.).

In most of the overcurrent conditions, the conduction time of the high-side switch is higher than the masking time and so the peak current protection limits the switch current.

$$I_{MAX} = I_{PK} \tag{8}$$

The DC current flowing in the load in overcurrent condition is:

$$I_{DCOUT} = I_{MAX} - \frac{I_{RIPPLE}(V_{OUT})}{2} = I_{MAX} - \left(\frac{V_{IN} - V_{OUT}}{2 \cdot L} \cdot T_{ON}\right) \tag{9}$$

Figure 25 shows the A6983 soft-start procedure with $V_{OUT}$ shorted to GND.

**Figure 25. Soft-start procedure with $V_{OUT}$ shorted to GND**

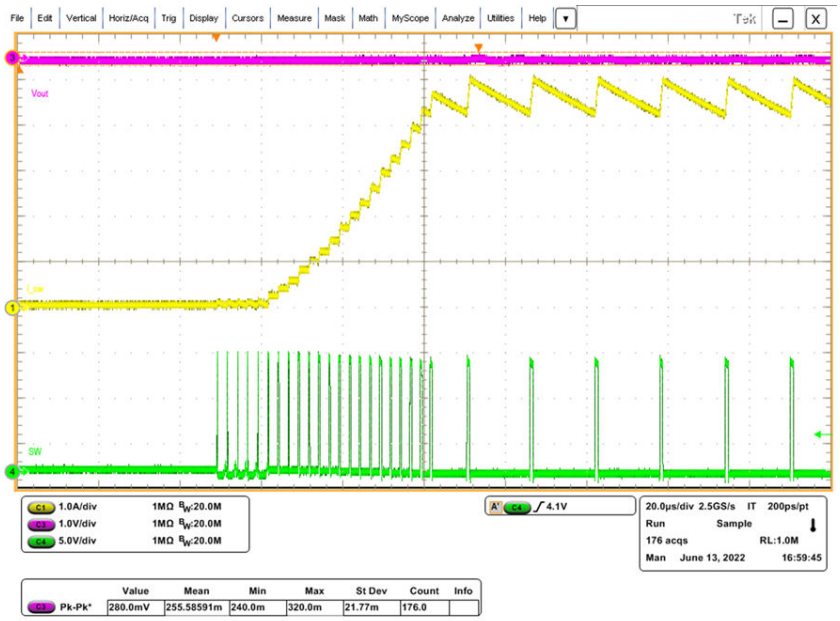
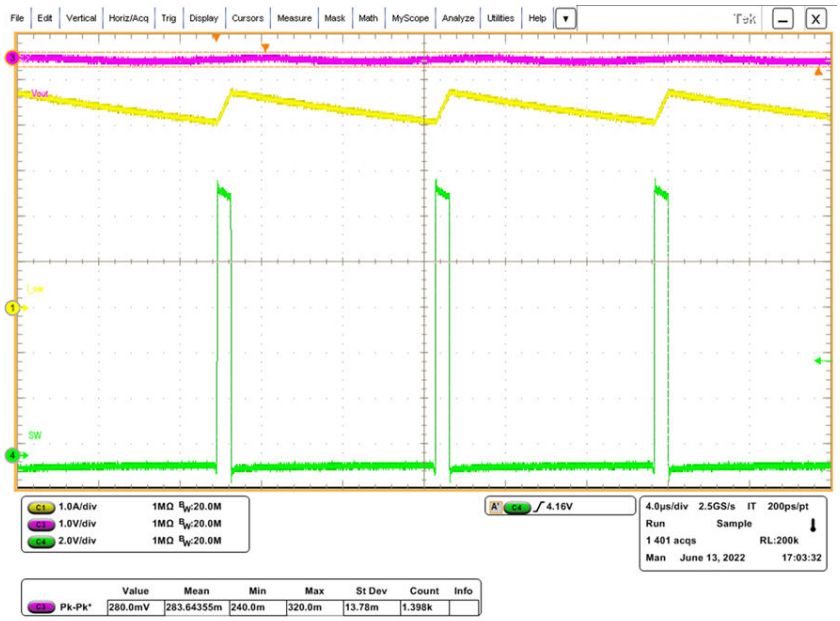



Figure 26 shows the A6983 overcurrent protection with a persistent short-circuit between $V_{OUT}$ and GND.

Figure 26. **Overcurrent procedure with persistent short circuit between $V_{OUT}$ and GND**




### 7.4.9 Thermal shutdown

The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold ($T_{SHDWN}$ refer to Table 6).

The thermal sensing element is close to the power elements, assuring fast and accurate temperature detection. A hysteresis of approximately 30 °C prevents the device from turning ON and OFF too fast. After a thermal protection event expires, the A6983 restarts with a new soft-start.

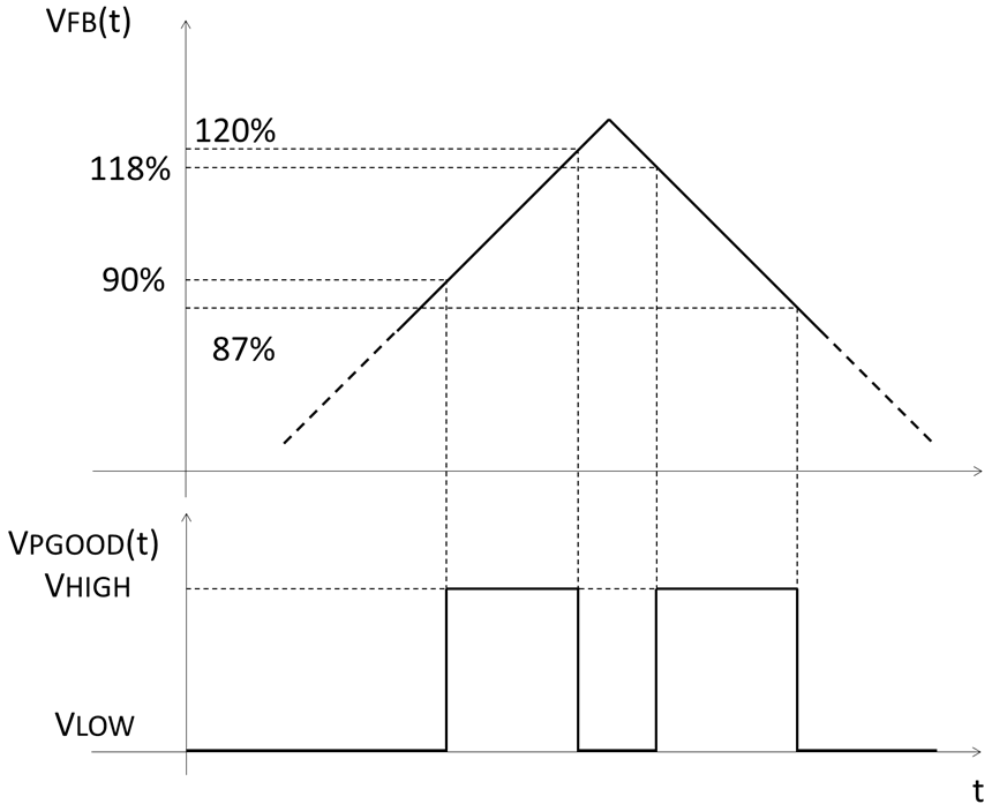
### 7.4.10 Power Good

The PGOOD pin indicates whether the output voltage is within its regulation level. PG goes in a high-impedance state during normal operations. The pin output is an open drain MOSFET. The PG is pulled low when:

- The FB pin voltage is lower than 90% (typ.) of the nominal internal reference for more than 10 µs.
- The FB pin voltage is higher than 120% (typ.) of the nominal internal reference for more than 10 µs (see Section 7.4.7).
- During the soft-start procedure also with pre-charged $V_{OUT}$.
- If a thermal shutdown event occurs.
- If a UVLO event occurs.

The PG pin is $V_{IN}$ compatible.

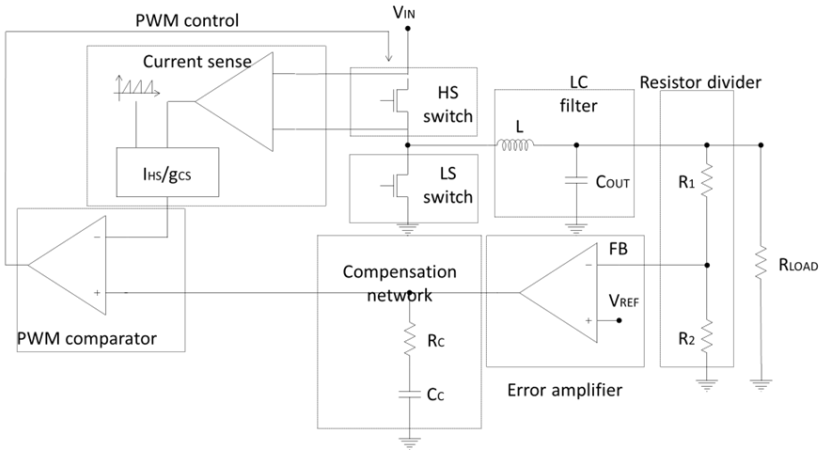
Figure 27. **PGOOD thresholds**



# 8 Closing the loop

The following picture shows the typical compensation network required to stabilize the system.

**Figure 28. Block diagram of the loop**




## 8.1 GCO(s) control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as follows:

$$G_{CO}(s) = R_{LOAD} \cdot g_{CS} \cdot \frac{1}{1 + \frac{R_{LOAD} \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0.5]} \cdot \frac{\left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)} \cdot F_H(s) \quad (10)$$

Where $R_{LOAD}$ represents the load resistance, the $g_{CS}$ equivalent sensing transconductance of the current sense circuitry, $\omega_P$ the single pole introduced by the power stage, and the $\omega_Z$ zero given by the ESR of the output capacitor. $F_H(s)$ considers the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}} \quad (11)$$

$$\omega_P = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1 - D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}} \quad (12)$$

Where:

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = I_{SLOPE} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \end{cases} \quad (13)$$

Where $I_{SLOPE}$ is equal to 1 A.

$S_n$ represents the on-time slope of the sensed inductor current, and $S_e$ the on-time slope of the external ramp that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

The sampling effect contribution $F_H$ (s) is:

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}} \quad (14)$$

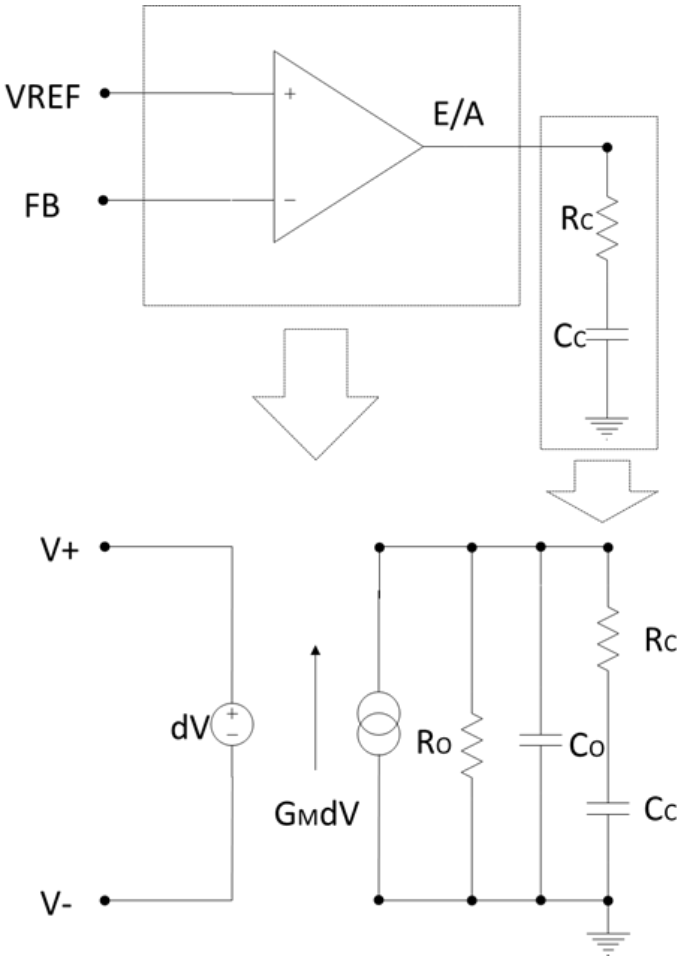
Where:

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]} \quad (15)$$

## 8.2 Error amplifier compensation network

The following figure shows the typical compensation network required to stabilize the system.

**Figure 29. Transconductance embedded error amplifier**




$R_C$ and $C_C$ introduce a pole and a zero in the open loop gain. The transfer function of the error amplifier and its compensation network is:

$$A_O(s) = \frac{A_{VO} \cdot (1 + s \cdot R_C \cdot C_C)}{s^2 \cdot R_O \cdot C_O \cdot R_C \cdot C_C + s \cdot (R_O \cdot C_C + R_O \cdot C_O + R_C \cdot C_C) + 1} \quad (16)$$

Where:

$$A_{VO} = G_m \cdot R_O \quad (17)$$

The poles of this transfer function are (if $C_C >> C_O$):

$$f_{PLF} = \frac{1}{2 \cdot \pi \cdot R_O \cdot C_C} \quad (18)$$

$$f_{PHF} = \frac{1}{2 \cdot \pi \cdot R_O \cdot C_O} \quad (19)$$

Whereas the zero is defined as:

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_C} \quad (20)$$

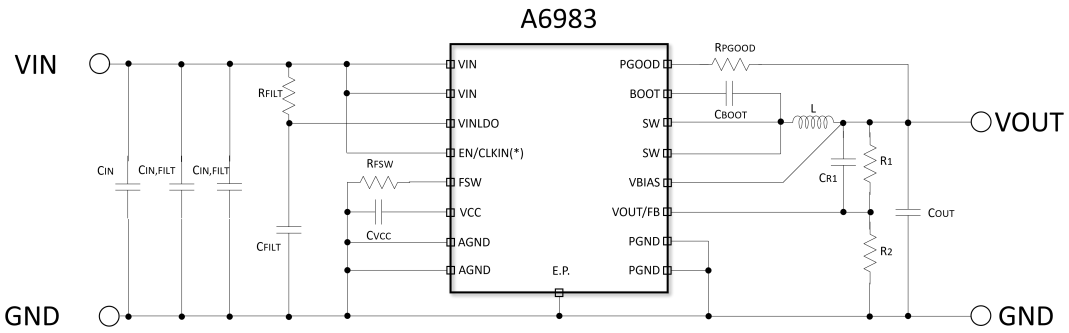
## 8.3 Voltage divider

The contribution of a simple voltage divider is:

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} \tag{21}$$

A small signal capacitor in parallel to the upper resistor (only for the adjustable part number) of the voltage divider implements a leading network ($f_{ZERO} < f_{POLE}$), sometimes necessary to improve the system phase margin:

**Figure 30. Leading network example**




The Laplace transformer of the leading network:

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} \cdot \frac{(1 + s \cdot R_1 \cdot C_{R1})}{\left(1 + s \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}\right)} \tag{22}$$

Where:

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_{R1}} \tag{23}$$

$$f_P = \frac{1}{2 \cdot \pi \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}} \tag{24}$$

$$f_Z < f_P \tag{25}$$

So, closing the loop, the loop gain is:

$$G(s) = G_{DIV}(s) \cdot G_{CO}(s) \cdot A_O(s) \tag{26}$$

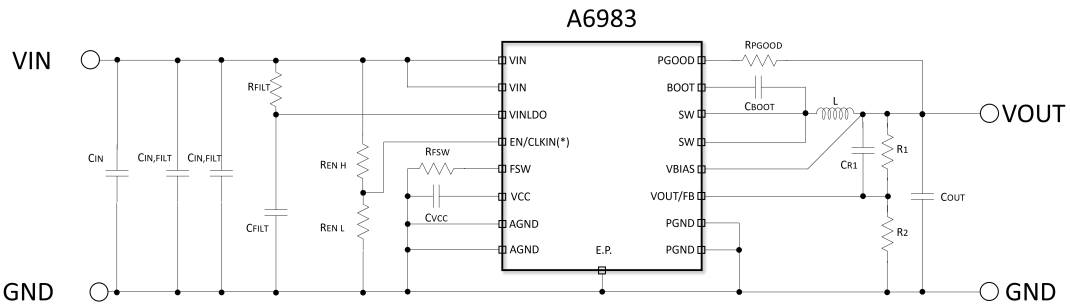
# 9 Application notes

## 9.1 Programmable power-up threshold

The enable rising threshold is equal to 1.2 V typical (refer to Table 6).The power-up threshold is adjusted according to the following equation

$$V_{Power\ Up} = 1.2V \cdot \left(1 + \frac{R_{EN\ H}}{R_{EN\ L}}\right) \quad (27)$$

**Figure 31. Leading network example**



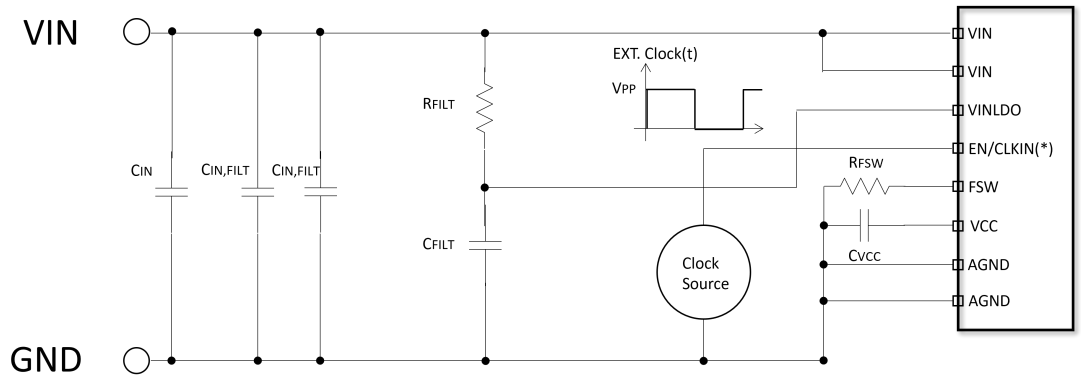

The enable falling threshold is equal to 1.0 V typical (refer to Table 6).The turn-off threshold is obtained according to the following equation:

$$V_{Power\ Up} = 1.0V \cdot \left(1 + \frac{R_{EN\ H}}{R_{EN\ L}}\right) \quad (28)$$

## 9.2 External synchronization (available for low noise mode only)

The device allows a direct connection between a clock source and the EN/CLKIN pin.

**Figure 32. External synchronization direct connection**




The device internally implements a low-pass filter connected to the EN/CLKIN pin that is able to acquire the average value of the applied signal.

The device turns on when the average of the signal applied is higher than VEN rising (refer to Table 6). The device turns off when the average of the signal is lower than VEN falling (refer to Table 6).

Considering, for example, a clock source with $V_{PP}$ = 5.0 V, the minimum duty cycle to guarantee the power-up is given by:

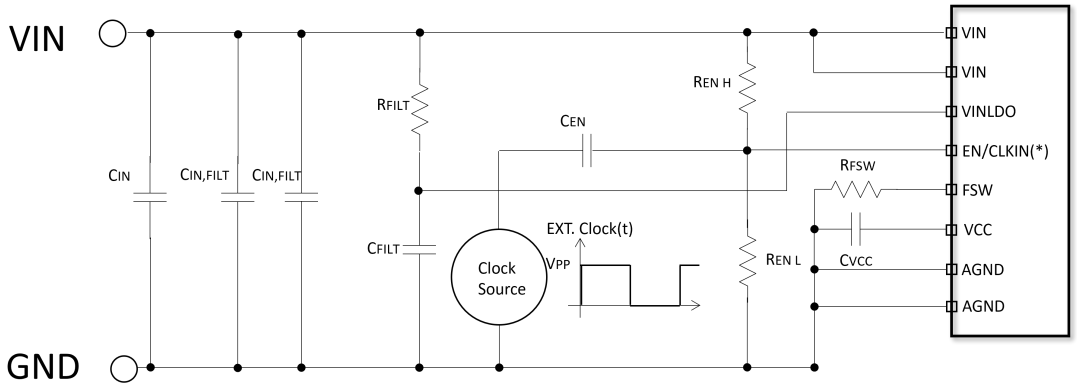
$$Duty_{min} = \frac{V_{EN,\ Rising}}{V_{PP}} = 0.24 \quad (29)$$

The maximum duty cycle to guarantee the turn-off is given by:

$$Duty_{MAX,} = \frac{V_{EN,\ Falling}}{V_{PP}} = 0.2 \quad (30)$$

The device also allows AC coupling.

**Figure 33. External synchronization AC coupling**




The AC-coupling allows the device to keep the power-up and down thresholds defined by the partition connected to the EN/CLKIN pin and described in Section 9.1.

The following table summarizes the minimum pulse duration for the external signal and maximum duty cycle that allows the synchronization by keeping the selected power-up and down thresholds.

**Table 8. External synchronization AC coupling suggested operation range**

| $V_{PP}$ [V] | TON, MIN, EXT $_{Clock}$ [ns] | DMAX, EXT $_{Clock}$ [%] |
|---|---|---|
| 2.3 | 60 | 45 |
| 3.3 | 20 | 30 |
| 5 | 20 | 20 |

The minimum amplitude for the external clock signal is, for both the configurations, equal to 2.3 V.

The network given by $C_{EN}$ and $R_{ENL}$ sets a high-pass filter. Considering a resistor in the order of 220 kΩ, a capacitor equal to 1 nF is a correct choice.

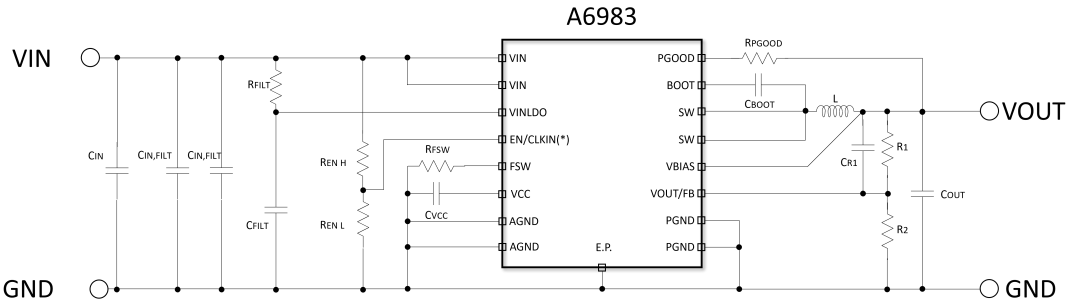
## 9.3 Output voltage adjustment

The error amplifier reference voltage is 0.85 V typical (refer to Table 6). The output voltage is adjustable as per the following equation:

$$V_{OUT} = 0.85V \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (31)$$

A CR1 capacitor is sometimes useful to increase the small signal phase margin (refer to Section 8).

Figure 34. **Application circuit**




## 9.4 Switching frequency

A resistor connected to the FSW pin features the selection of the switching frequency (refer to Table 7). Connecting the resistor between the pins FSW and $V_{CC}$, the internal dithering circuit is turned on (refer to Section 7.4.6).

# 10 Design of the power components

## 10.1 Input capacitor selection

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity a pulsed current flows into the input capacitor and so its RMS current capability must be selected according to the application conditions. Internal losses of the input filter depend on the ESR value, so usually low ESR capacitors (such as multilayer ceramic capacitors) have higher RMS current capability. On the other hand, given the RMS current value, a lower ESR input filter has lower losses and so it contributes to higher conversion efficiency.

The maximum RMS input current, flowing through the capacitor, can be calculated as follows:

$$I_{RMS} = I_{OUT} \cdot \sqrt{\left(1 - \frac{D}{\eta}\right) \cdot \frac{D}{\eta}} \quad (32)$$

Where $I_{OUT}$ is the maximum DC output current, D is the duty cycles, η is the efficiency. This function has a maximum at D = 0.5 and, considering η = 1, it is equal to $I_{OUT}/2$. In a specific application, the range of possible duty cycles has to be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

$$D_{MAX} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INmin} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}} \quad (33)$$

$$D_{min} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INMAX} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}} \quad (34)$$

Where $\Delta V_{HIGHSIDE}$ and $\Delta V_{LOWSIDE}$ are the voltage drops across the embedded switches. The peak-to-peak voltage across the input filter can be calculated as the equation below:

$$V_{PP} = \frac{I_{OUT}}{C_{IN} \cdot F_{SW}} \cdot \left(1 - \frac{D}{\eta}\right) \cdot \frac{D}{\eta} + ESR \cdot (I_{OUT} + \Delta I_L) \quad (35)$$

In the case of a negligible ESR (MLCC capacitor), the equation of $C_{IN}$ as a function of the target $V_{PP}$ can be written as follows:

$$C_{IN} = \frac{I_{OUT}}{V_{PP} \cdot F_{SW}} \cdot \left(1 - \frac{D}{\eta}\right) \cdot \frac{D}{\eta} \quad (36)$$

Considering η = 1 this function has its maximum in D = 0.5:

$$C_{INmin} = \frac{I_{OUT}}{4 \cdot V_{PPMAX} \cdot F_{SW}} \quad (37)$$

Typically, $C_{IN}$ is dimensioned to keep the maximum peak-peak voltage across the input filter in the order of 5% $V_{INMAX}$.

To minimize the spike on the $V_{IN}$ pins given by the stray inductance and the pulsed input current, it is necessary to add, for each one, a filter capacitor. A 1µF capacitor with a 0603 footprint is a good choice.

In the following table, some suitable capacitor part numbers are listed.

**Table 9. Capacitor part numbers**

| Manufacturer | Series | Size | Cap value (µF) | Rated voltage (V) |
|---|---|---|---|---|
| TDK | CGA5L1X7R1H106K160AE | 1206 | 10 | 50 |
| | CGA5L1X7R1H106K160AC | 1206 | 10 | 50 |
| Murata | GRT31CD71H106KE13 | 1206 | 10 | 50 |

## 10.2 Inductor selection

The inductor current ripple flowing into the output capacitor determines the output voltage ripple. Usually, the inductor value is selected in order to keep the current ripple lower than 20% to 40% of the output current over the input voltage range. The inductance value can be calculated by the following equation:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF} \quad (38)$$

Where $T_{ON}$ and $T_{OFF}$ are the on and off times of the internal power switch. The maximum current ripple, at fixed $V_{OUT}$, is obtained at maximum $T_{OFF}$ that is at minimum duty cycle. So fixing $\Delta I_L$ = 20% to 40% of the maximum output current, the minimum inductance value can be calculated:

$$L_{min} = \frac{V_{OUT}}{\Delta IL_{MAX}} \cdot \frac{1 - D_{min}}{F_{SW}} \quad (39)$$

For those applications requiring higher inductor value for minimized current ripple, pay attention to the maximum value to prevent sub-harmonic instability given the design of the internal slope compensation. As a consequence the inductor value must satisfy the quality factor range:

$$0.4 \leq Q_P \leq 1.33 \quad (40)$$

Where QP has been defined in Section 8.1. The peak current through the inductor is given by:

$$I_{L,PK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (41)$$

So, if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher the inductor value, the higher the average output current that can be delivered, without reaching the current limit.

## 10.3 Output capacitor selection

The triangular shape current ripple (with a zero average value) flowing into the output capacitor, gives the output voltage ripple, that depends on the capacitor value and the equivalent resistive component (ESR). Therefore, the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements. The voltage ripple equation can be calculated as:

$$\Delta V_{OUT} = ESR \cdot \Delta I_{L,MAX} + \frac{\Delta I_{L,MAX}}{8 \cdot C_{OUT} \cdot F_{SW}} \quad (42)$$

For a ceramic (MLCC) capacitor, the capacitive component of the ripple dominates the resistive one. While for an electrolytic capacitor, the opposite is true. Neglecting the ESR contribution, the minimum value of the output capacitor is given by the following equation:

$$C_{OUT,min,RIPPLE} = \frac{\Delta I_{L,MAX}}{8 \cdot \Delta V_{OUT} \cdot F_{SW}} \quad (43)$$

As the compensation network is internal, the output capacitor should be selected in order to have a proper phase margin and then a stable control loop. A good rule to obtain a proper dimensioning for the minimum amount of the output capacitor is to set the target system bandwidth equal to $F_{SW}/8$. The following equation takes into account the precedent consideration:

$$C_{OUT,BW,min} = \frac{8.04}{\frac{Fsw}{8} \cdot V_{OUT}} \quad (44)$$

The maximum amount of the output capacitor is given by:

$$C_{OUT,BW,MAX} = \frac{0.960 \cdot 10^{-3}}{V_{OUT}} \quad (45)$$

## 10.4 Layout consideration

The PC board layout of a switching DC-DC regulator is very important in order to minimize the noise injected in high impedance nodes, to reduce interferences generated by the high switching current loops, and to optimize the reliability of the device. In order to avoid EMC problems, the high switching current loops must be as short as possible.

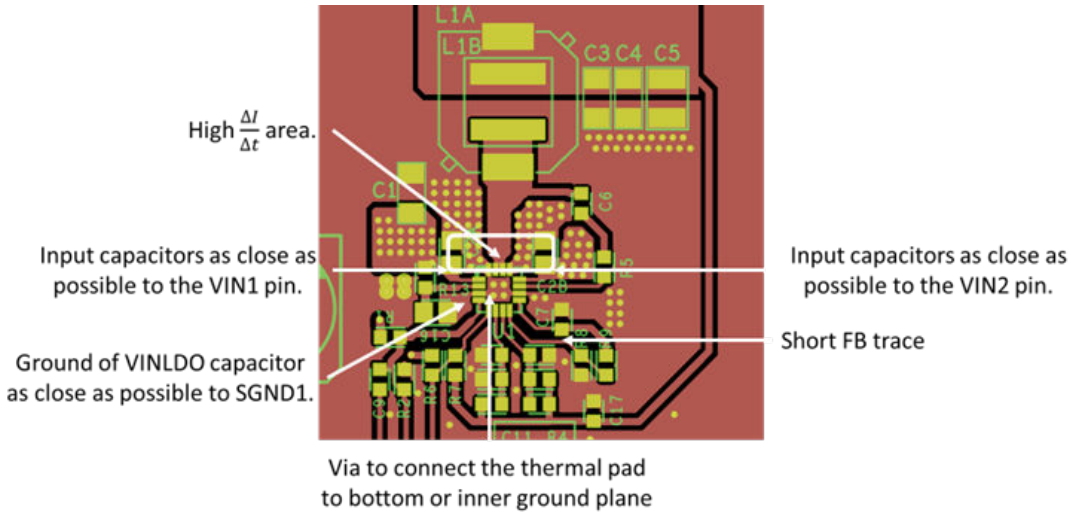
In the buck converter there are two high switching current loops: during the ON time, the pulsed current flows through the input capacitor, the high-side power switch, the inductor, and the output capacitor; during the OFF time, through the low-side power switch, the inductor, and the output capacitor.

The input capacitor connected to $V_{IN1}$ and $V_{IN2}$ must be placed as close as possible to the device, to avoid spikes due to the stray inductance and the pulsed input current.

The feedback pin (FB) connection to the external resistor divider is a high impedance node, so the interferences can be minimized through the routing of the feedback node with a very short trace and as far as possible from the high current paths.

Due to the exposed pad of the device, the ground plane helps to reduce the thermal resistance junction to ambient; so a large ground plane, soldered to the exposed pad, enhances the thermal performance of the converter allowing high power conversion.

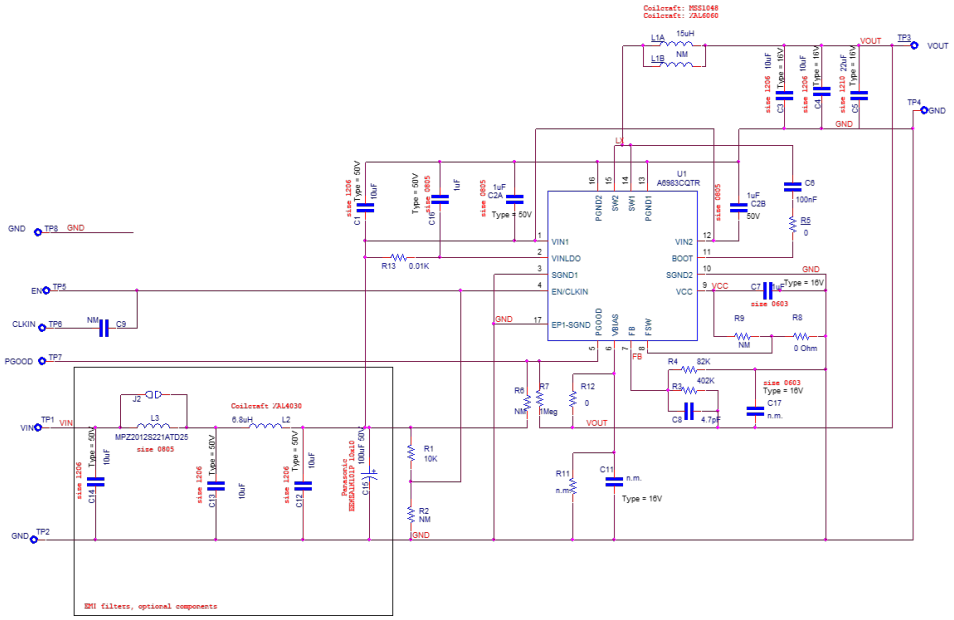
Figure 35.



# 11 Application board

The figure below shows the reference evaluation board schematic:

**Figure 36. Application circuit**




The additional input filter (C14, L3, C13, L2, C12, and C15) limits the conducted emission on the power supply.

Table 10. **Bill of materials**

| Reference | Part number | Description | Manufacturer |
|---|---|---|---|
| C1, C3, C4, C12, C13, C14 | CGA5L1X7R1H106K160AC | 10 µF 50 V | TDK |
| C2A, C2B, C16 | CGA4J3X7R1H105K125AB | 1 µF 50 V | TDK |
| C5 | CGA6P3X7R1E226M250AE | 22 µF 50 V | TDK |
| C6 | CGA3E2X7R1H104K080AA | 0.1 µF 50 V | TDK |
| C7, C11 | CGA3E1X7R1C105K080AC | 1 µF 16 V | TDK |
| C8, C9, C17 | n.m. | | |
| C8 | CGA3E2C0G1H4R7C080AA | 4.7 pF 50 V | TDK |
| C15 | EEHZA1H101P | 100 µF 50 V | Panasonic |
| L1A | XAL6060-153MEC | 15 µH | Coilcraft |
| L1B | n.m. | | |
| L2 | XAL4030-682ME | 6.8 µH | Coilcraft |
| L3 | MPZ2012S221ATD25 | 220 Ω 100 MHz | TDK |
| R1 | | 100 KΩ | |
| R2, R6, R9, R11 | n.m. | | |
| R3 | | 82 KΩ | |
| R4 | | 400 KΩ | |
| R5, R8, R12 | | 0 Ω | |
| R7 | | 1 MΩ | |
| R13 | | 10 Ω | |
| U1 | A6983CQTR | | STMicroelectronics |

Figure 37. **Top layer**

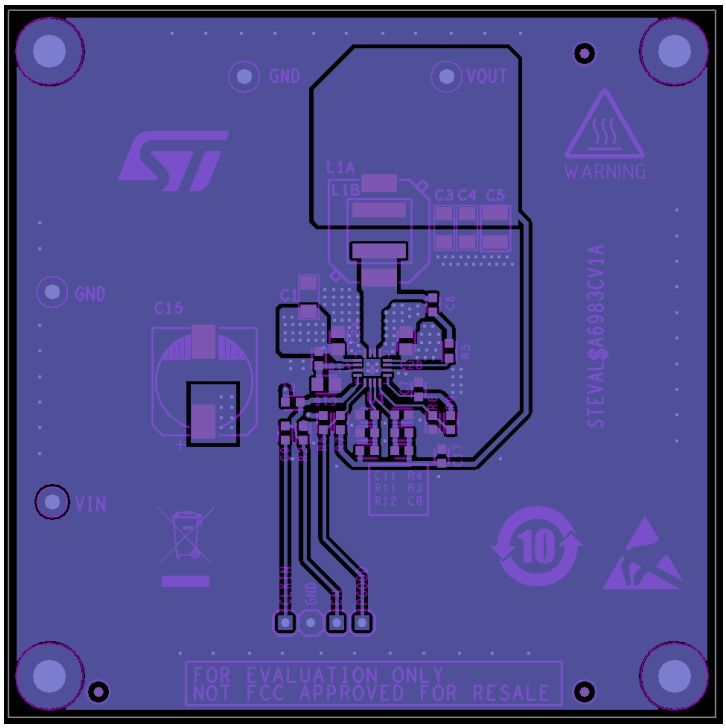
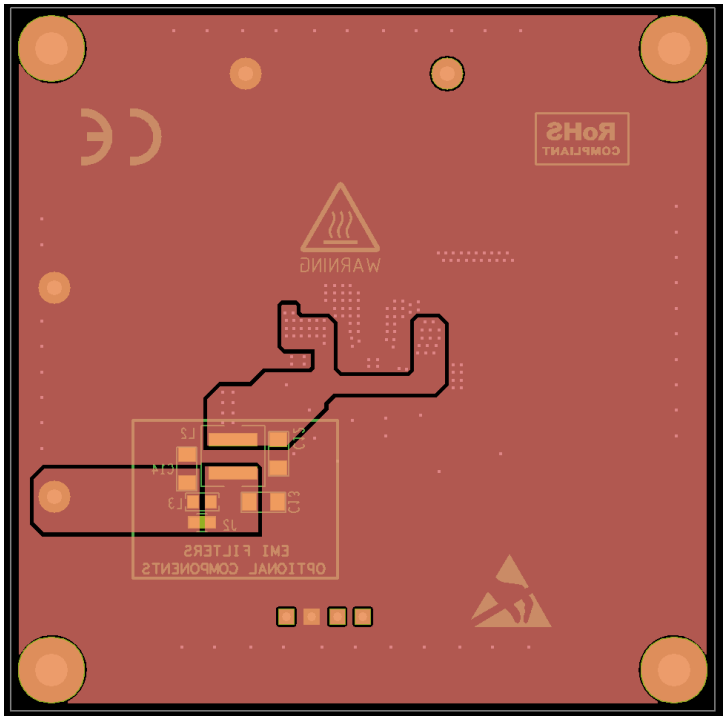


Figure 38. **Bottom layer**



# 12 Efficiency measures

### $V_{OUT}$ = 5 [V] FSW = 400 [kHz]

The following three figures show the efficiency and power losses acquired on the standard evaluation boards of the device, STEVAL-A6983CV1 and STEVAL-A6983NV1, selecting the following output filter:

- COUT:
  - 2 x 10 µF 50 V (CGA5L1X7R1H106K160AC, TDK).
  - 1 x 22 µF 50 V (CGA6P3X7R1E226M250AE, TDK).
- Inductor:

XAL6060-223ME (Coilcraft)

**Figure 39. Efficiency LCM linear scale**

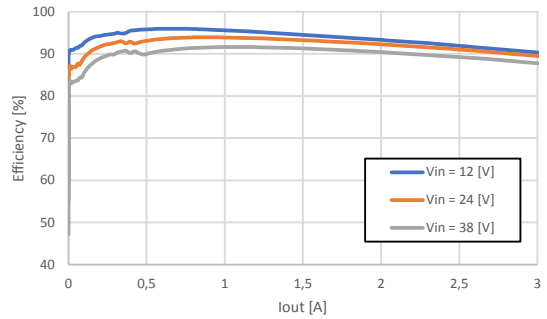



**Figure 40. Efficiency LNM linear scale**

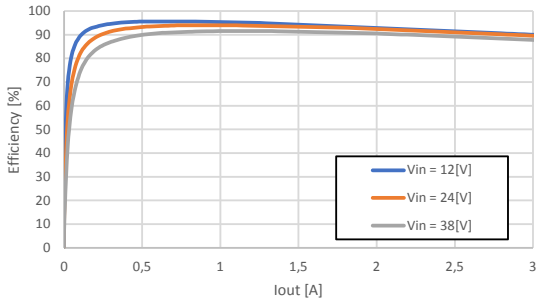



**Figure 41. Efficiency LCM log scale**

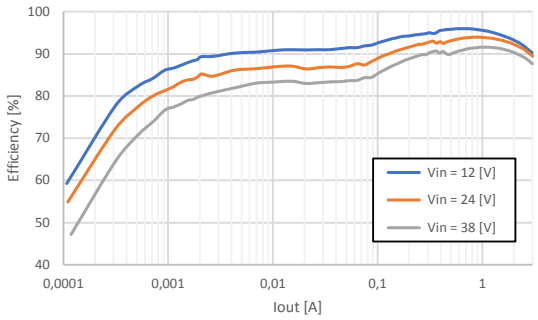



**Figure 42. Efficiency LNM log scale**

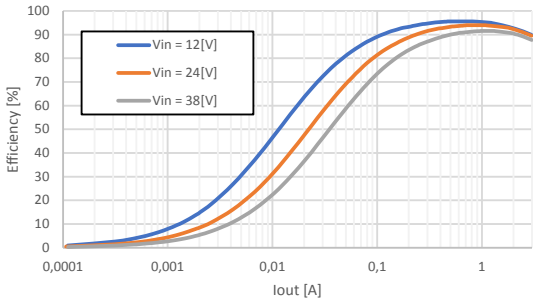



**Figure 43. Power losses LCM linear scale**

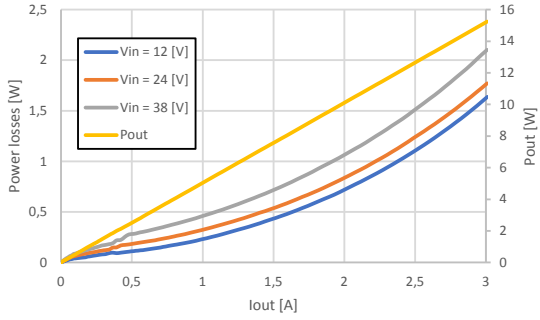
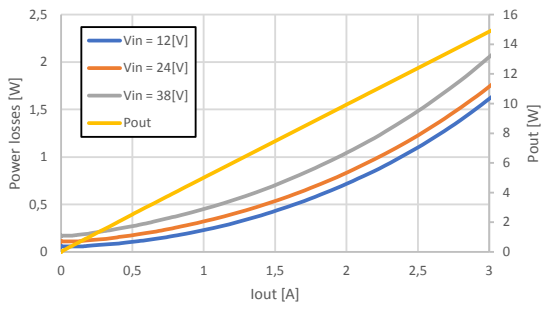



**Figure 44. Power losses LNM linear scale**



### $V_{OUT}$ = 3.3 [V] FSW = 400 [KHz]

The following three figures show the efficiency and power losses acquired on the standard evaluation boards of the device, STEVAL-A6983CV1 and STEVAL-A6983NV1, selecting the following output filter:

- COUT:
  - 1 x 10 µF 50V (CGA5L1X7R1H106K160AC, TDK).
  - 2 x 22 µF 50V (CGA6P3X7R1E226M250AE, TDK).
- Inductor:

XAL5050-822ME (Coilcraft)

**Figure 45. Efficiency LCM linear scale**

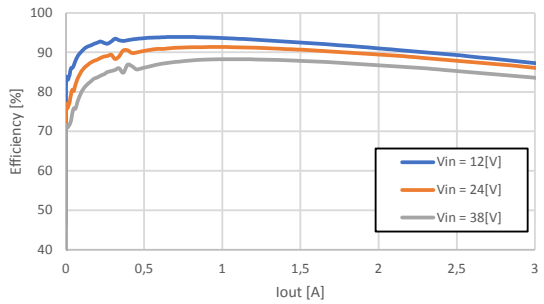



**Figure 46. Efficiency LNM linear scale**

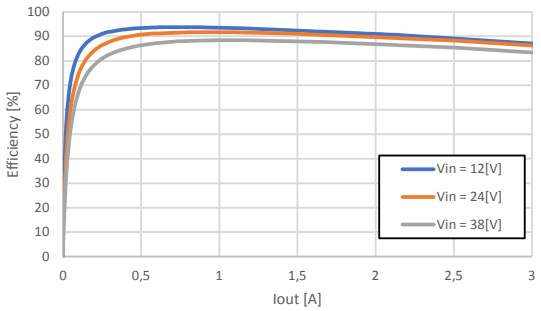



**Figure 47. Efficiency LCM log scale**

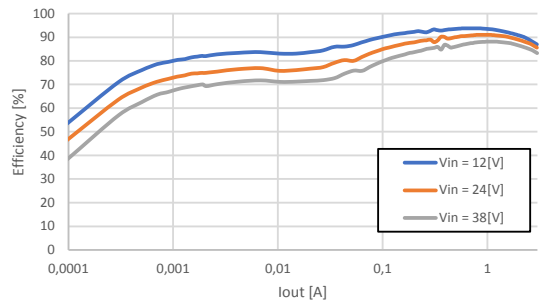



**Figure 48. Efficiency LNM log scale**

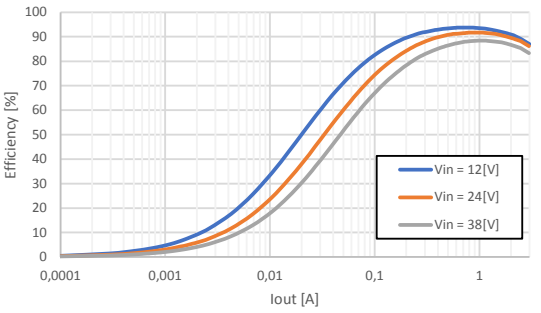



**Figure 49. Power losses LCM linear scale**

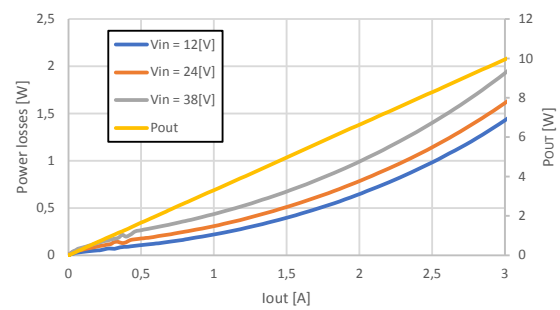
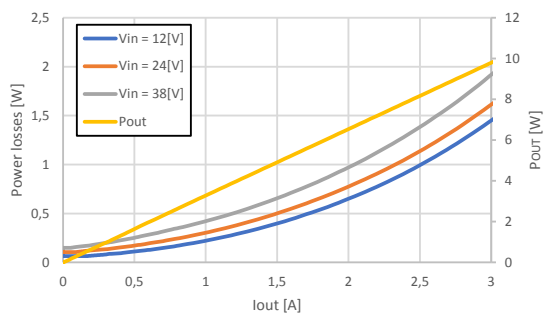



**Figure 50. Power losses LNM linear scale**



### $V_{OUT}$ = 5 [V] $F_{SW}$ = 2300 [KHz]

The following three figures show the efficiency and power losses acquired on the standard evaluation boards of the device, STEVAL-A6983CV1 and STEVAL-A6983NV1, selecting the following output filter:

- COUT:
  - 1 x 22 µF 50 V (CGA6P3X7R1E226M250AE, TDK).
- Inductor:
  - XAL4040-332ME (Coilcraft)

**Figure 51. Efficiency LCM linear scale**

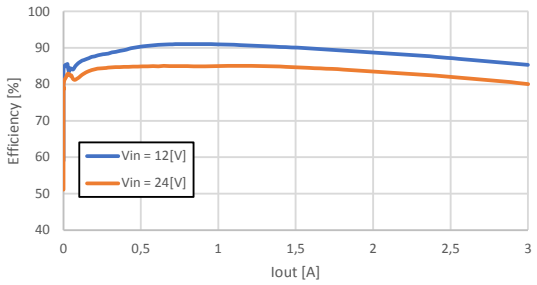



**Figure 52. Efficiency LNM linear scale**

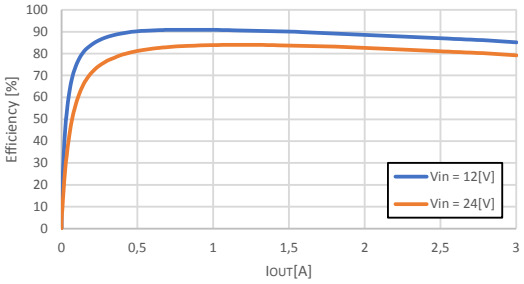



**Figure 53. Efficiency LNM log scale**

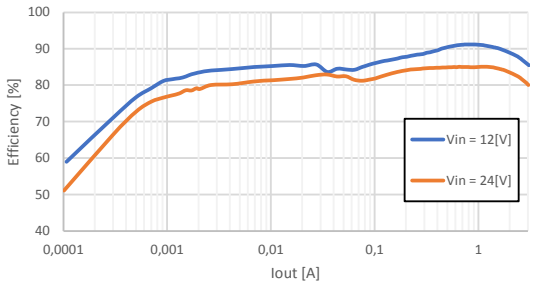



**Figure 54. Efficiency LNM log scale**

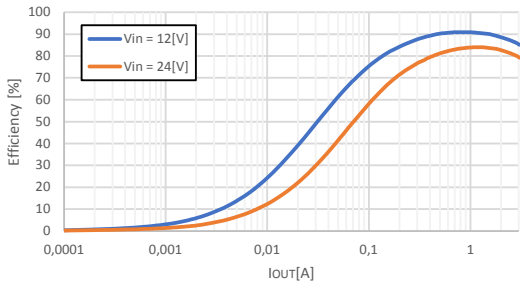



**Figure 55. Power losses LCM linear scale**

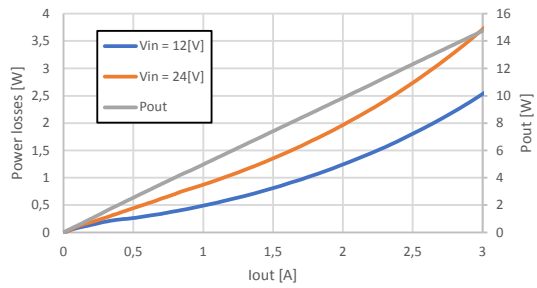
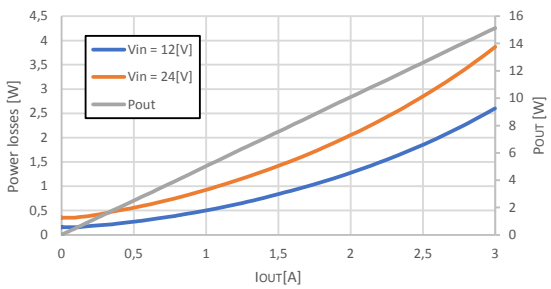



**Figure 56. Power losses LNM linear scale**




*Note: Measurements acquired with air forced convection.*

### $V_{OUT}$ = 3.3 [V] FSW = 2300 [KHz]

The following three figures show the efficiency and power losses acquired on the standard evaluation boards of the device, STEVAL-A6983CV1 and STEVAL-A6983NV1, selecting the following output filter:

- COUT:
  - 1 x 22 µF 50 V (CGA6P3X7R1E226M250AE, TDK).
- Inductor:
  - XAL4040-332ME (Coilcraft)

**Figure 57. Efficiency LCM linear scale**

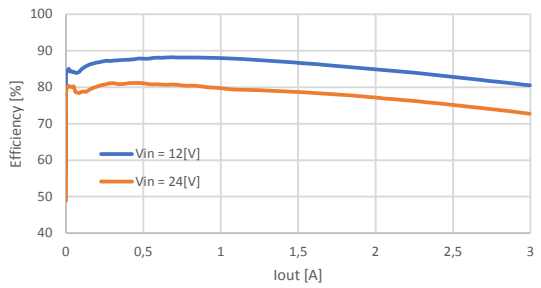



**Figure 58. Efficiency LNM linear scale**

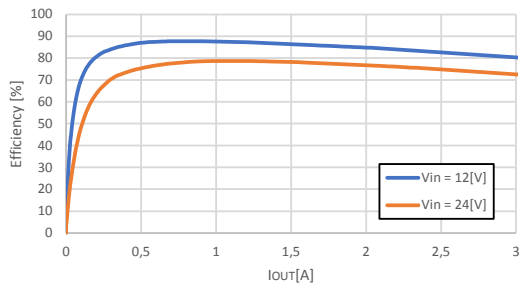



**Figure 59. Efficiency LNM log scale**

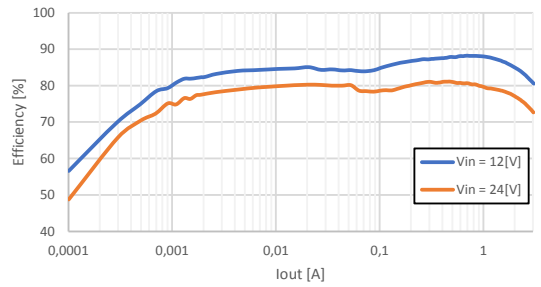



**Figure 60. Efficiency LNM log scale**

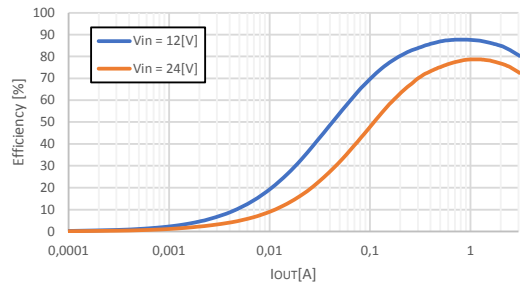



**Figure 61. Power losses LCM linear scale**

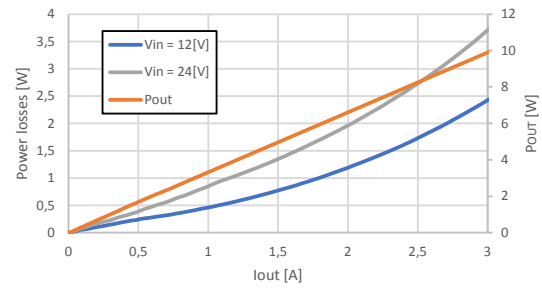
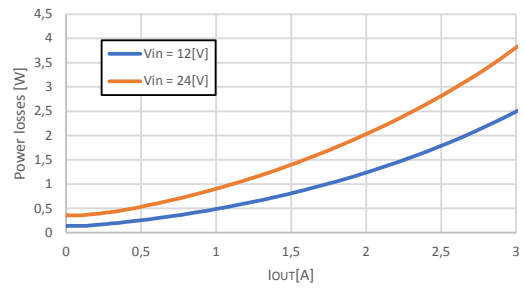



**Figure 62. Power losses LNM linear scale**




*Note: Measurements acquired with air forced convection.*

# 13 Thermal dissipation

The thermal design is important in order to prevent thermal shutdown of the device if the junction temperature goes above 165 °C. The three different sources of losses within the device are:

1. Conduction losses due to the on-resistance of the high-side switch ($R_{DSON\_HS}$) and low-side switch ($R_{DSON\_LS}$); these are equal to:

$$P_{COND} = R_{DSON\_HS} \cdot I_{OUT}^2 \cdot D + R_{DSON\_LS} \cdot I_{OUT}^2 \cdot \left(1 - D\right) \quad (46)$$

Where D is the duty cycle of the selected application and is given by the following formula:

$$D = \frac{V_{OUT} + \left(R_{DSON\_LS} + DCRl\right) \cdot I_{OUT}}{V_{IN} - \left(R_{DSON_{HS}} - R_{DSON\_LS}\right) \cdot I_{OUT}} \quad (47)$$

In order to obtain a more accurate estimate, it is necessary to take into account that the amount of resistance of the internal power MOSFET increases together with the temperature. For this reason, the value of $R_{DSONHS}$ and $R_{DSONLS}$, should be increased from the typical of a factor equal to 15%.

1. Switching losses due to high-side power MOSFET turn-ON and OFF; these can be calculated as per the formula below:

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW} \quad (48)$$

Where $T_{RISE}$ and $T_{FALL}$ are the overlap times of the voltage across the high-side power switch (VDS) and the current flowing into it during turn-ON and turn-OFF phases, as shown in shown in Figure 63

$T_{SW}$ is the equivalent switching time. For this device, the typical value for the equivalent switching time is 15 ns.

1. Quiescent current losses, calculated with the equation below:

$$P_Q = V_{IN} \cdot I_{Q,MAX} \quad (49)$$

Where $I_Q$ is the quiescent current and depends on the $V_{BIAS}$ connections. If $V_{BIAS}$ is connected to GND, the maximum is equal to 3 mA. Otherwise, if $V_{BIAS}$ is connected to $V_{OUT}$ the quiescent current is given by:

$$I_{Q,MAX} = 0.8\left[mA\right] + \frac{1}{\eta_{A6983}} \cdot \frac{V_{BIAS}}{V_{IN}} \cdot 2.3\left[mA\right] \quad (50)$$

The power losses are given by:

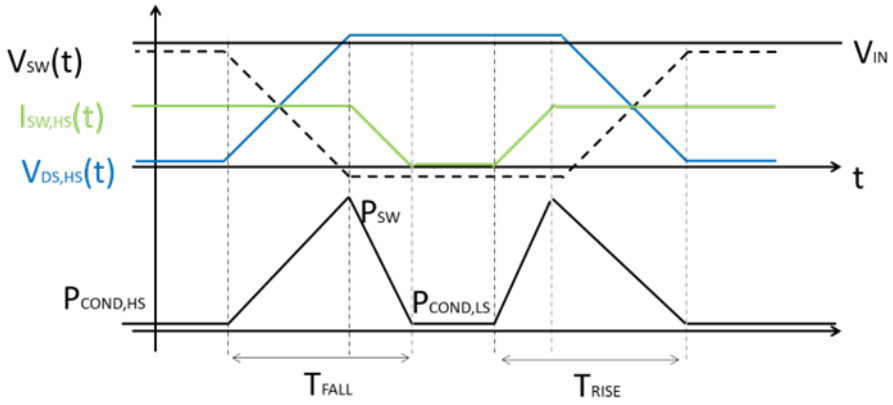
$$P_{LOSS} = P_{COND} + P_{SW} + P_Q \quad (51)$$

The junction temperature $T_J$ can be calculated as:

$$T_J = T_A + R_{thJA} \cdot P_{LOSS} \quad (52)$$

Where $T_A$ is the ambient temperature, and $R_{thJA}$ is the equivalent thermal resistance junction to ambient of the device, and it can be calculated as the parallel of many paths of heat conduction from the junctions to the ambient. For this device, the path through the exposed pad is the one conducting the largest amount of heat. The $R_{thJA}$ measured on the demonstration board described in the following section is about 40 °C/W.

Figure 63. **Switching losses**




It is also possible to estimate the junction temperature directly from the efficiency measurements acquired in a stationary application condition.

Considering that the power losses are given by:

$$P_{LOSS} = P_{IN} - P_{OUT} \tag{53}$$

Neglecting the AC losses of the selected inductor, the power losses related to the A6983 are given by:

$$P_{LOSS\,A6983} = V_{IN} \cdot I_{IN} - V_{OUT} \cdot I_{OUT} - DCRl \cdot I_{OUT}^2 \tag{54}$$

Therefore, the junction temperature $T_J$ can be calculated as:

$$T_J = T_A + R_{thJA} \cdot P_{LOSS,\,A6983} \tag{55}$$

# 14 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 14.1 QFN16 (3x3 mm) package information

**Figure 64. QFN16 (3x3 mm) package outline**

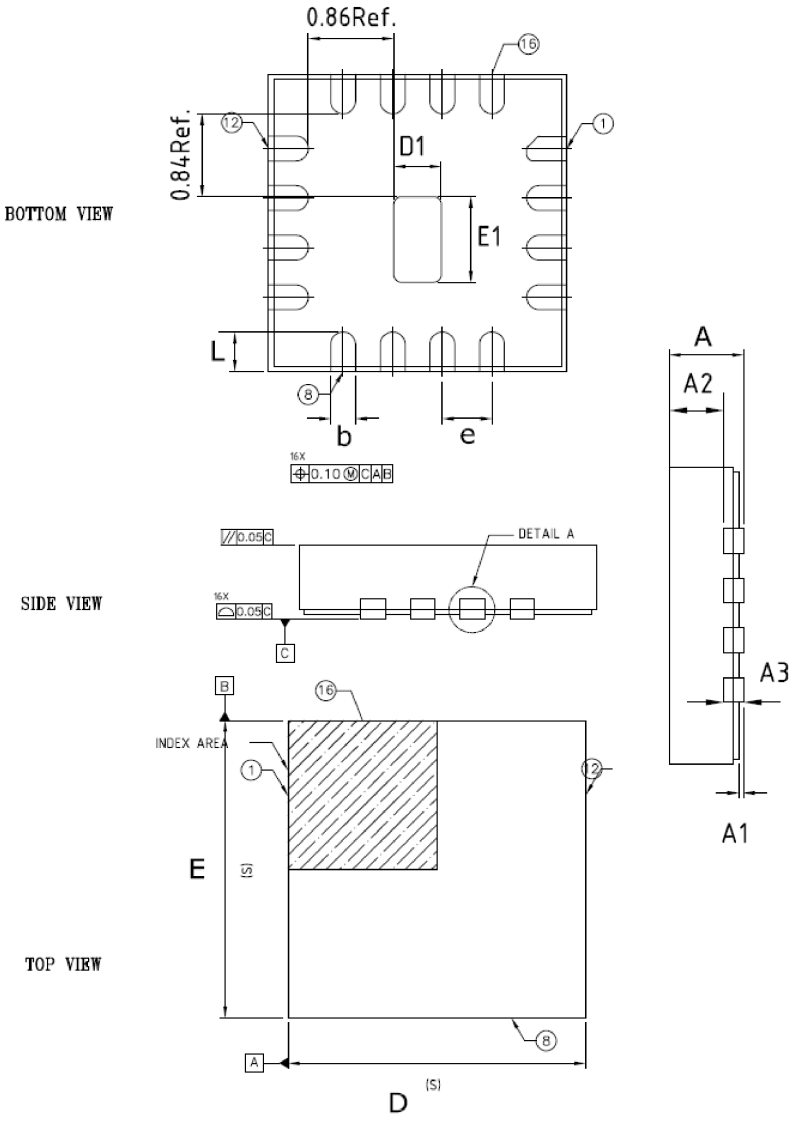


Figure 65. **QFN16 (3x3 mm) package outline. Detail A**

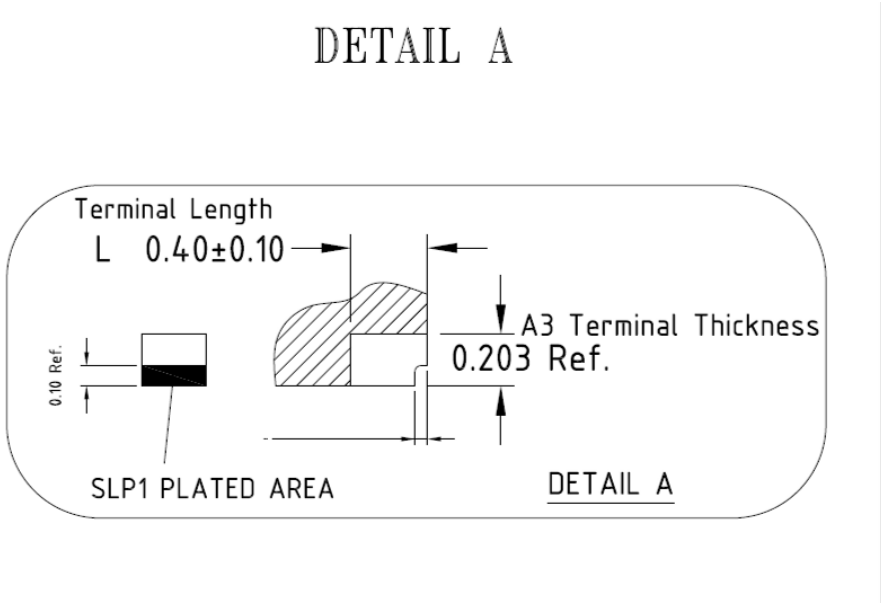
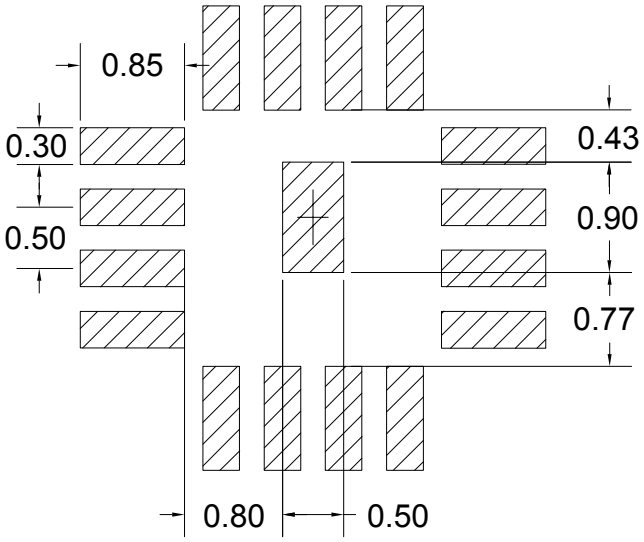



Table 11. **QFN16 (3x3 mm) mechanical data**

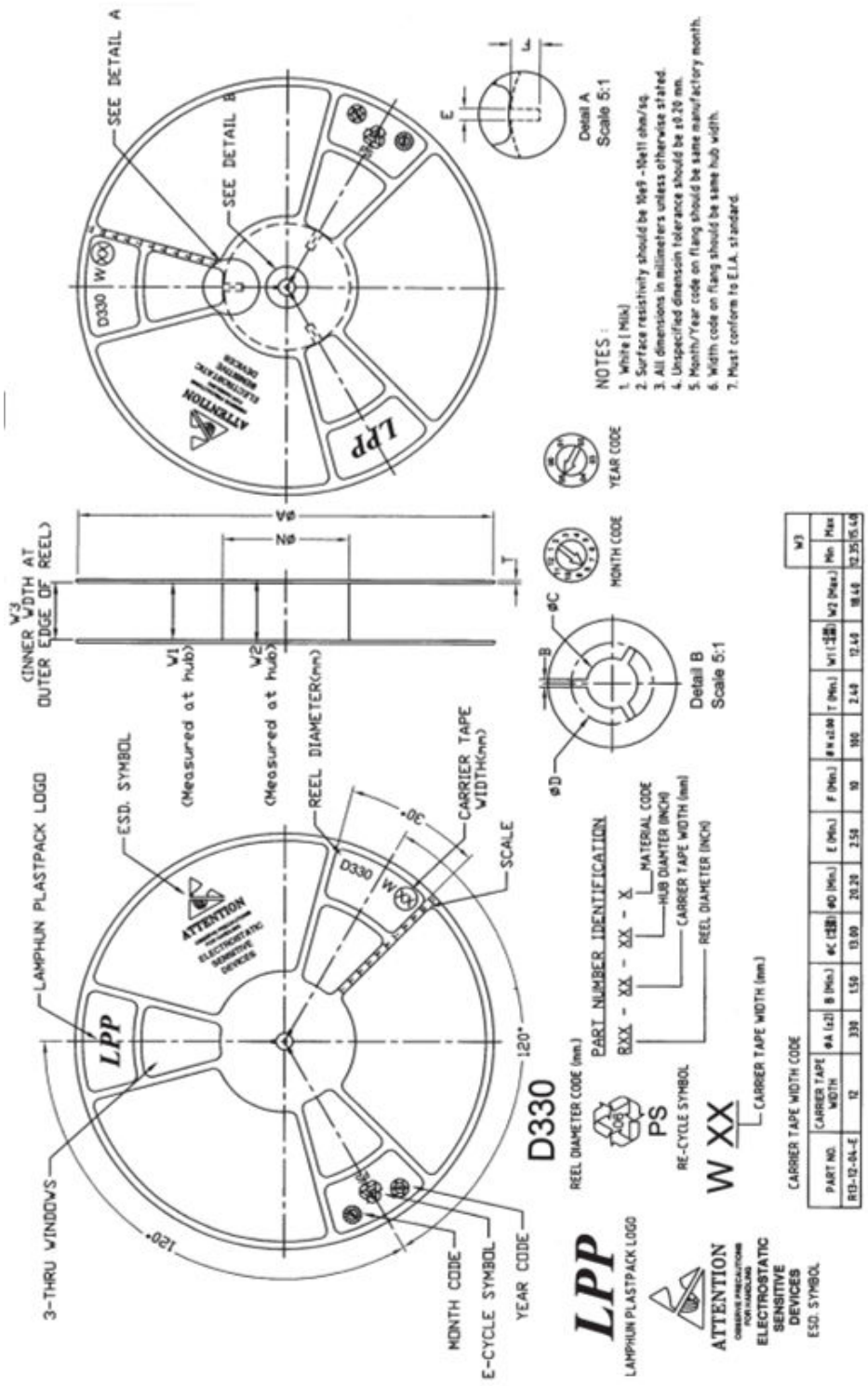
| Symbol | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.7 | 0.75 | 0.8 |
| A1 | 0 | | 0.05 |
| A2 | 0,5 | 0.55 | 0.6 |
| A3 | | 0,203 REEF | |
| b | 0.2 | 0.25 | 0.3 |
| L | 0.3 | 0.4 | 0.5 |
| e | | 0,50 BSC | |
| D | 2,95 | 3 | 3,05 |
| E | 2,95 | 3 | 3,05 |
| D1 | 0,43 | 0,48 | 0,53 |
| E1 | 0.81 | 0,86 | 0,91 |

Figure 66. **QFN16 (3x3 mm) recommended footprint**



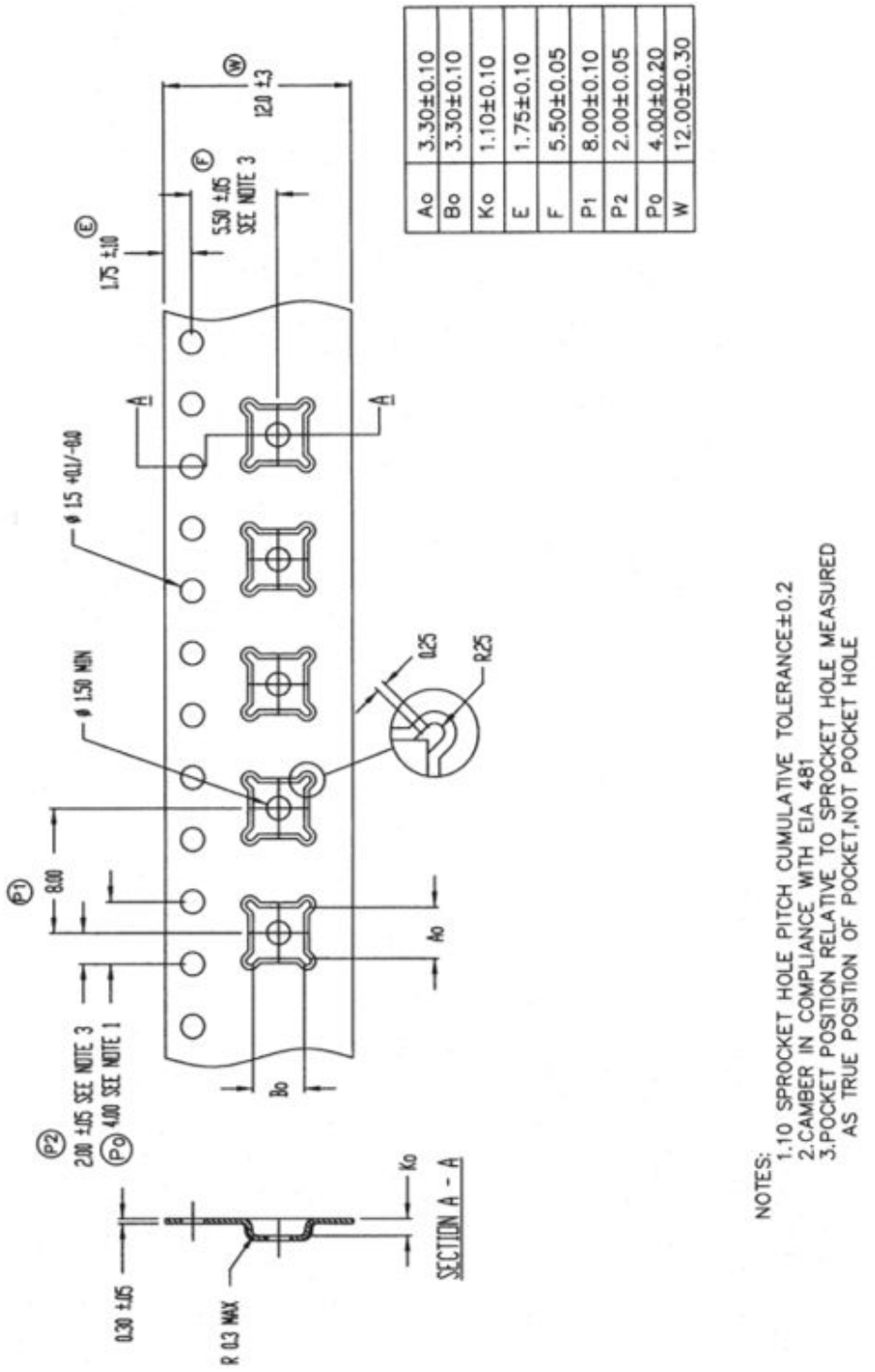
## 14.2 QFN16 (3x3 mm) packing information

Figure 67. **Carrier tape for QFN 3x3 mm**




| PART NO. | CARRIER TAPE WIDTH | ØA (±2) | B (Min.) | ØC (±2) | ØD (Min.) | E (Min.) | F (Min.) | P0 ±0.2 | T (Min.) | W1 (±2) | W2 (Max.) | W3 Min | W3 Max |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R13-12-04-E | 12 | 330 | 1.50 | 13.00 | 20.20 | 2.50 | 10 | 4.00 | 2.40 | 12.40 | 18.40 | 12.35 | 15.40 |

Figure 68. **QFN16 (3x3 mm) plastic reel 13"**



# 15 Ordering information

Table 12. **Ordering codes**

| Part Numbers | Output voltage | Light-load behavior | Package | Packaging |
|---|---|---|---|---|
| A6983CQTR | Adj. | LCM (Low consumption mode) | QFN16 | Tape and reel |
| A6983C50QTR | 5 | | | |
| A6983C33QTR | 3.3 | | | |
| A6983NQTR | Adj. | LNM (Low noise mode) | | |
| A6983N33QTR | 5 | | | |
| A6983N50QTR | 3.3 | | | |

## Revision history

Table 13. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 19-Dec-2023 | 1 | Initial release. |

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