ALPHA & OMEGA SEMICONDUCTOR

AONG36322

30V Dual Asymmetric N-Channel MOSFET

General Description

- Trench Power MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS 2.0 and Halogen-Free Compliant

Product Summary

	Q1	Q2
V_{DS}	30V	30V
I_D (at V_{GS}=10V)	83A	163A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 4.5mΩ	< 1.3mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 8mΩ	< 1.75mΩ

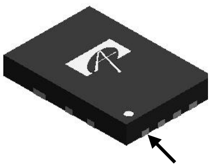
100% UIS Tested
100% Rg Tested

Applications

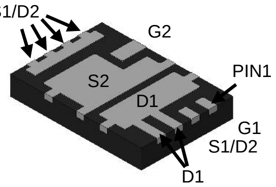
- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial
- See Note H

DFN 3.5x5

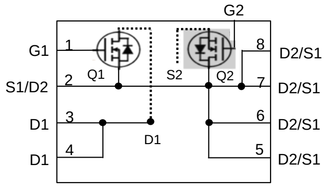
Top View



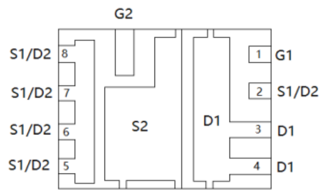
Bottom View



Top View



Bottom View



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONG36322	DFN 3.5x5	Tape & Reel	5000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±20	±12	V
Continuous Drain Current	T_C=25°C	I_D	83	163	A
	T_C=100°C		53	103	
Pulsed Drain Current [C]		I_{DM}	180	515	
Continuous Drain Current	T_A=25°C	I_{DSM}	20	37	A
	T_A=70°C		16	30	
Avalanche Current [C]		I_{AS}	60	80	A
Avalanche energy	L=0.01mH [C]	E_{AS}	18	32	mJ
Power Dissipation [B]	T_C=25°C	P_D	52	59	W
	T_C=100°C		20.8	23.8	
Power Dissipation [A]	T_A=25°C	P_{DSM}	3.1	3.1	W
	T_A=70°C		2	2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{θJA}$	30	30	40	40	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		50	50	65	65	°C/W
Maximum Junction-to-Case	Steady-State	$R_{θJC}$	1.9	1.7	2.4	2.1	°C/W

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V				1	µA
			T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA		1.3	1.7	2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A			3.7	4.5	mΩ
			T_J=125°C		5.6	6.8	
		V_{GS}=4.5V, I_D=20A			6	8	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A			57		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V			0.7	1	V
I_S	Maximum Body-Diode Continuous Current					60	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz			1150		pF
C_{oss}	Output Capacitance				380		pF
C_{rss}	Reverse Transfer Capacitance				55		pF
R_g	Gate resistance	f=1MHz		0.6	1.2	2	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A			16	25	nC
Q_g(4.5V)	Total Gate Charge				7.5	15	nC
Q_{gs}	Gate Source Charge				2.5		nC
Q_{gd}	Gate Drain Charge				3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω			6.5		ns
t_r	Turn-On Rise Time				4.5		ns
$t_{D(off)}$	Turn-Off DelayTime				19		ns
t_f	Turn-Off Fall Time				3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, di/dt=500A/µs			11.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, di/dt=500A/µs			20		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.
G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.
H. For application requiring slow >1ms turn-on/turn-off, please consult AOS FAE for proper product selection.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

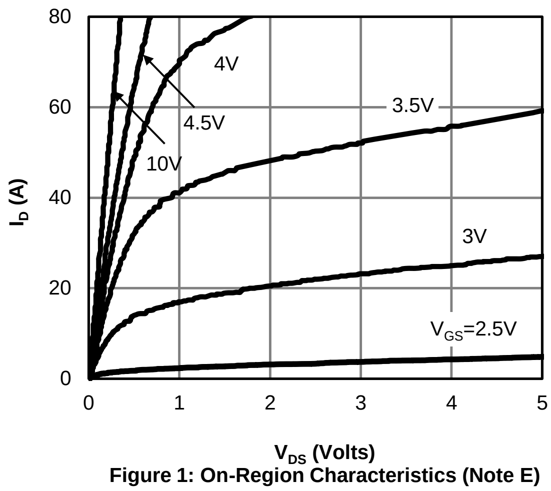


Figure 1: On-Region Characteristics (Note E)

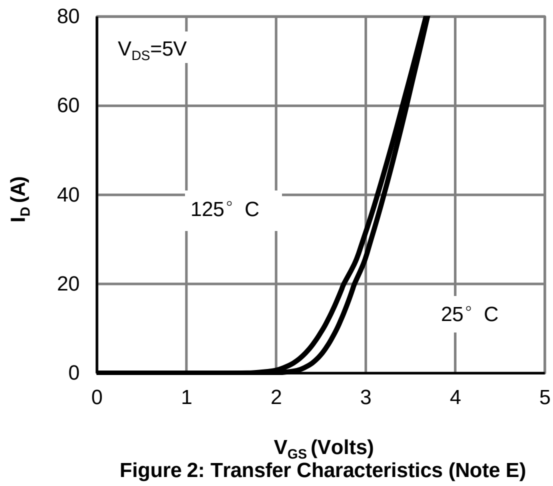


Figure 2: Transfer Characteristics (Note E)

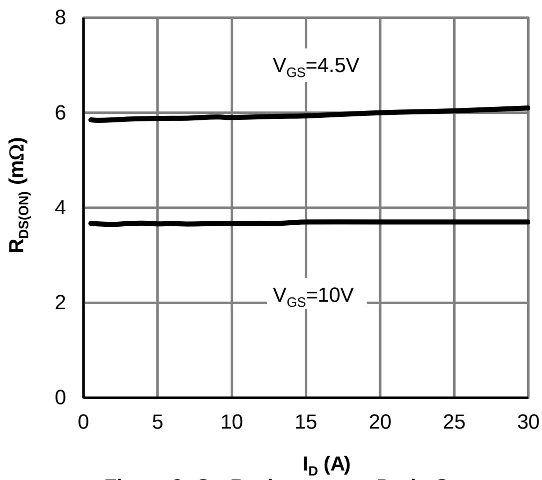


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

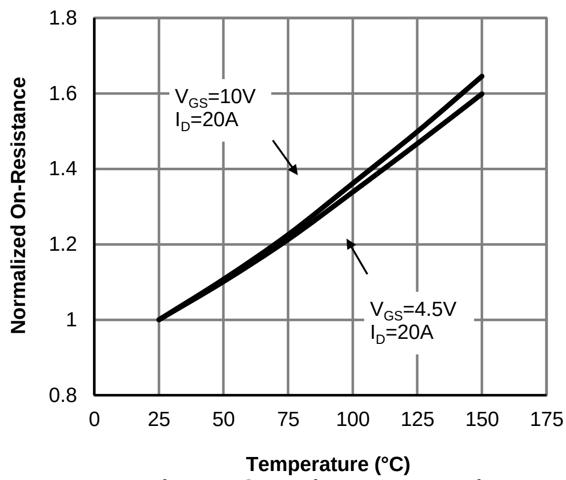


Figure 4: On-Resistance vs. Junction Temperature (Note E)

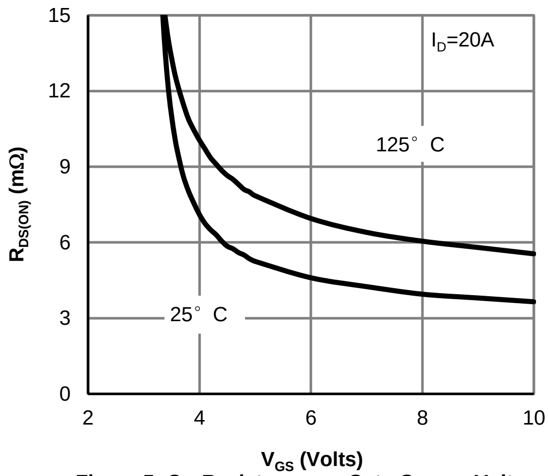


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

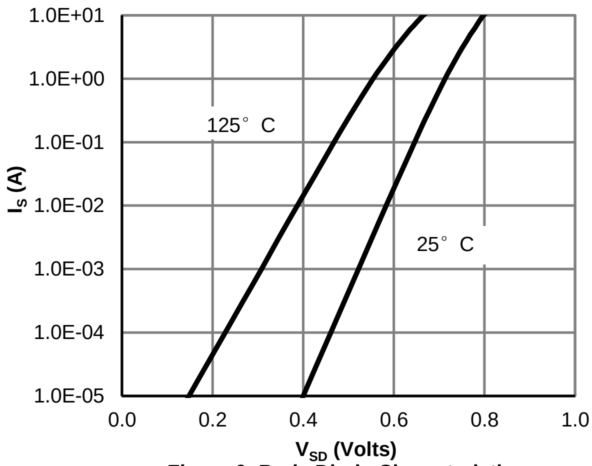


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

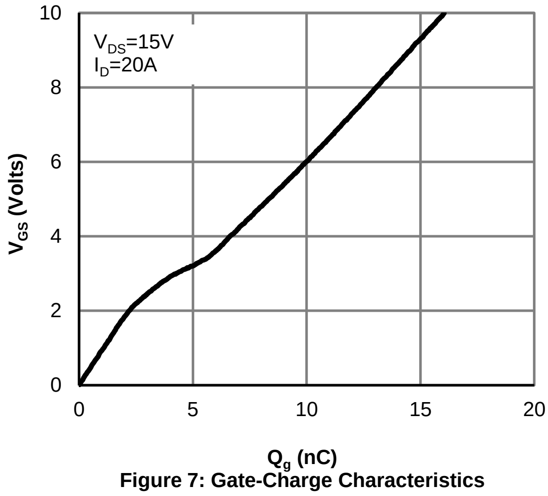


Figure 7: Gate-Charge Characteristics

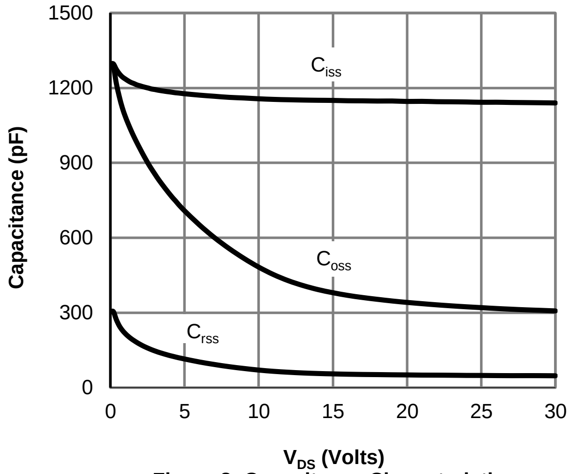


Figure 8: Capacitance Characteristics

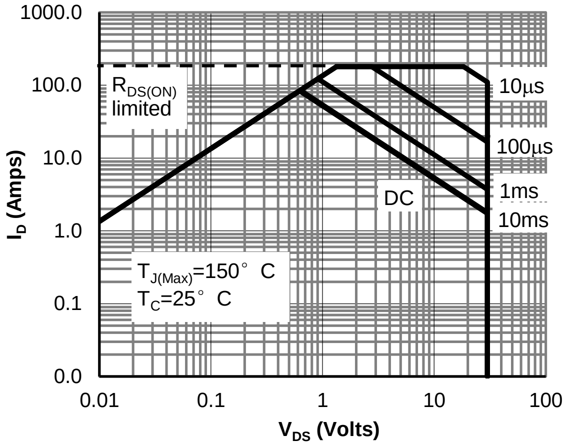


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

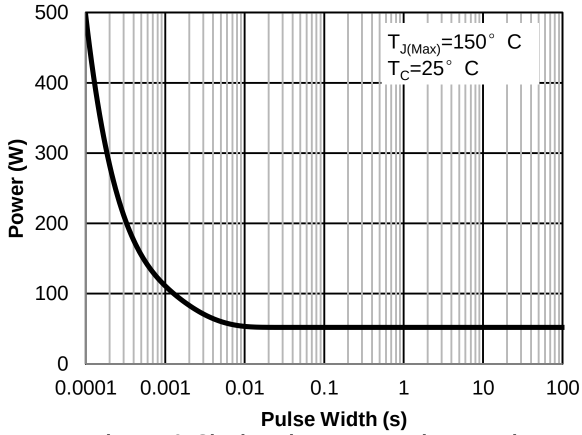


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

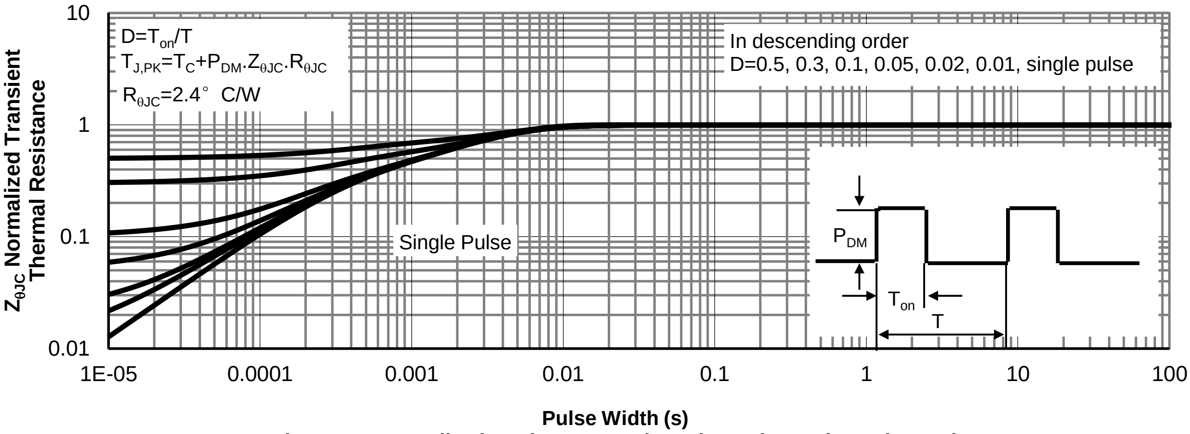


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

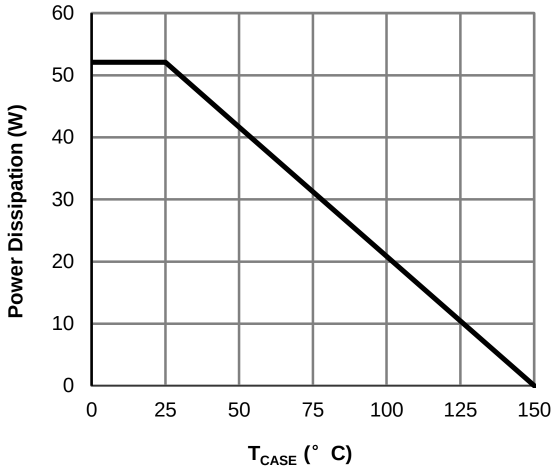


Figure 12: Power De-rating (Note F)

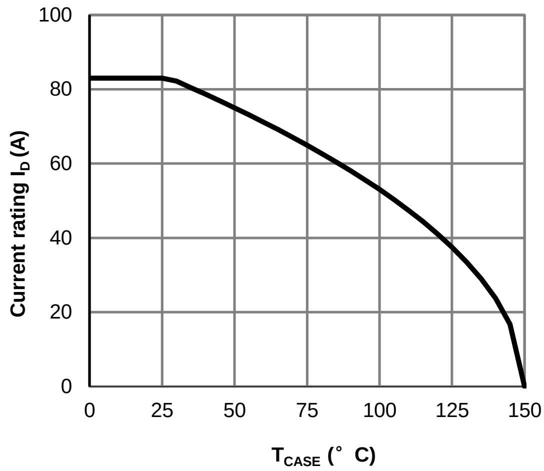


Figure 13: Current De-rating (Note F)

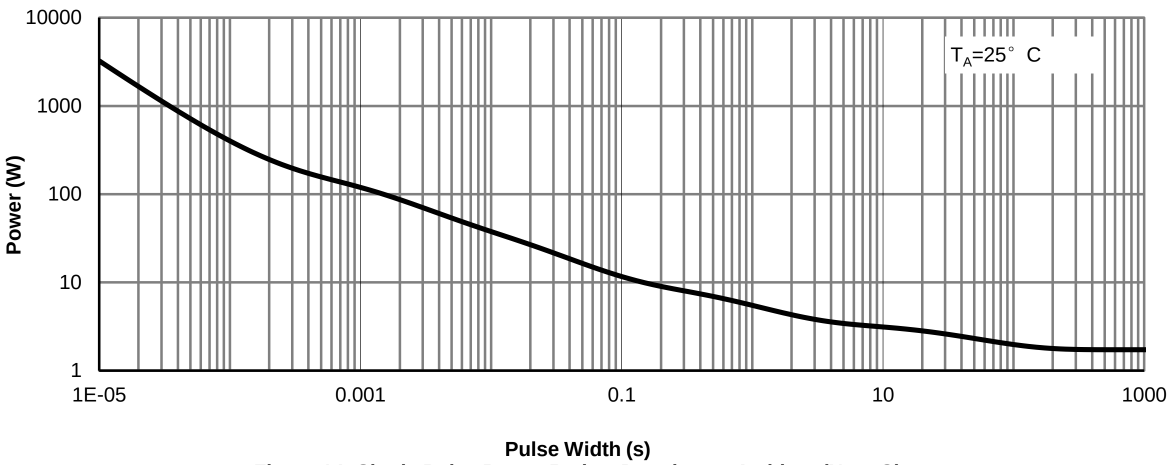


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

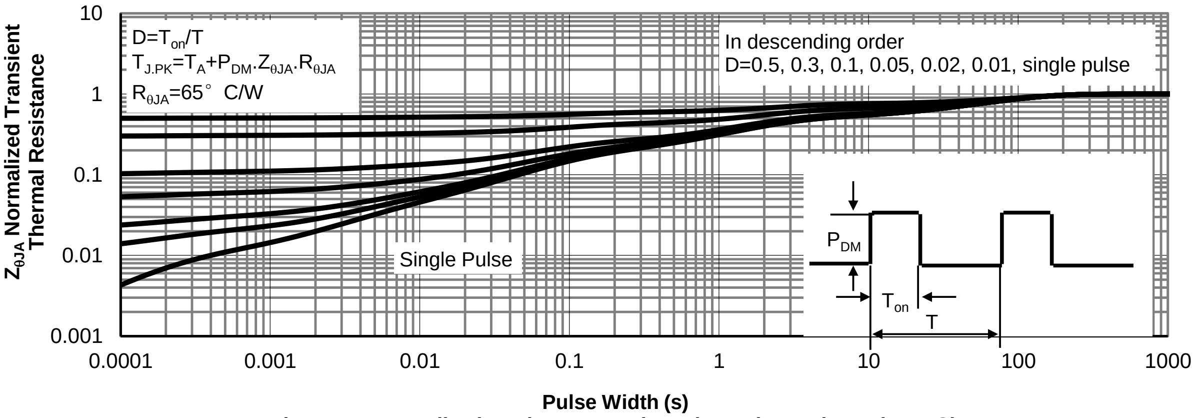


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V				1	µA
			T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250µA		1.2	1.5	1.9	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A			1	1.3	mΩ
			T_J=125°C		1.4	1.8	
		V_{GS}=4.5V, I_D=20A			1.3	1.75	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A			200		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V			0.7	1	V
I_S	Maximum Body-Diode Continuous Current					70	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz			4180		pF
C_{oss}	Output Capacitance				880		pF
C_{rss}	Reverse Transfer Capacitance				125		pF
R_g	Gate resistance	f=1MHz		0.6	1.3	2.2	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A			65	100	nC
Q_g(4.5V)	Total Gate Charge				30	50	nC
Q_{gs}	Gate Source Charge				9.5		nC
Q_{gd}	Gate Drain Charge				7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω			9		ns
t_r	Turn-On Rise Time				8		ns
$t_{D(off)}$	Turn-Off DelayTime				50.5		ns
t_f	Turn-Off Fall Time				8.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, di/dt=500A/µs			17		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, di/dt=500A/µs			42		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R $_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.
H. For application requiring slow >1ms turn-on/turn-off, please consult AOS FAE for proper product selection.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

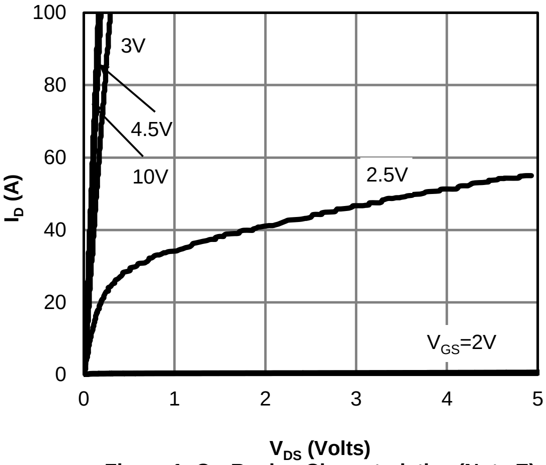


Figure 1: On-Region Characteristics (Note E)

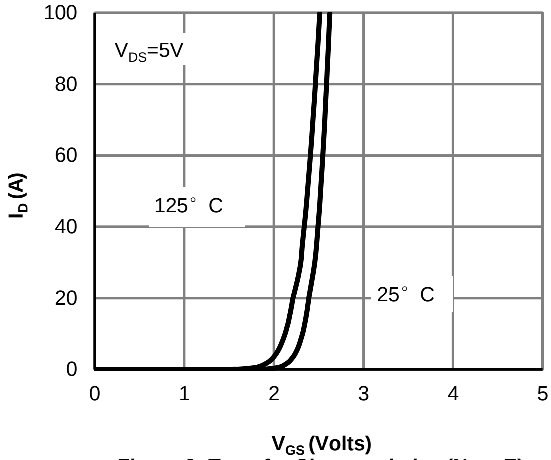


Figure 2: Transfer Characteristics (Note E)

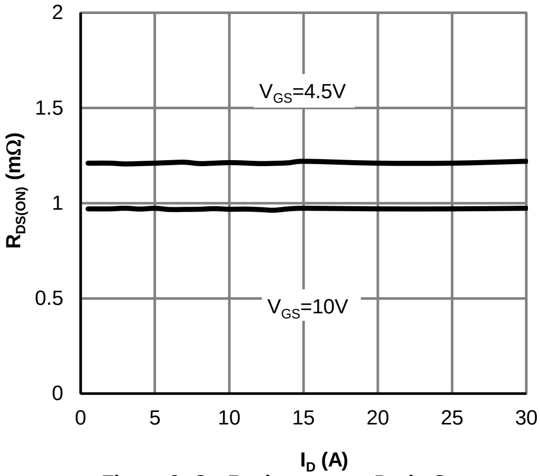


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

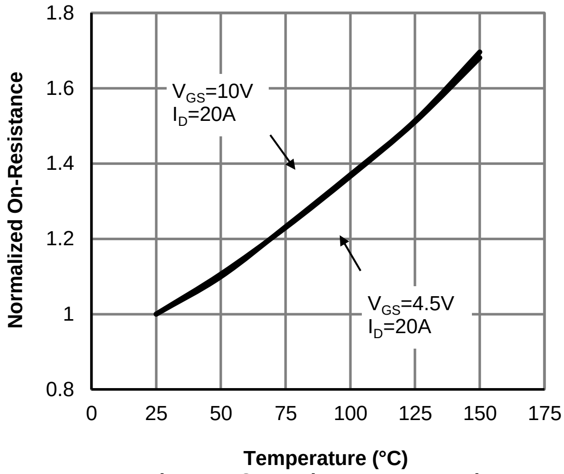


Figure 4: On-Resistance vs. Junction Temperature (Note E)

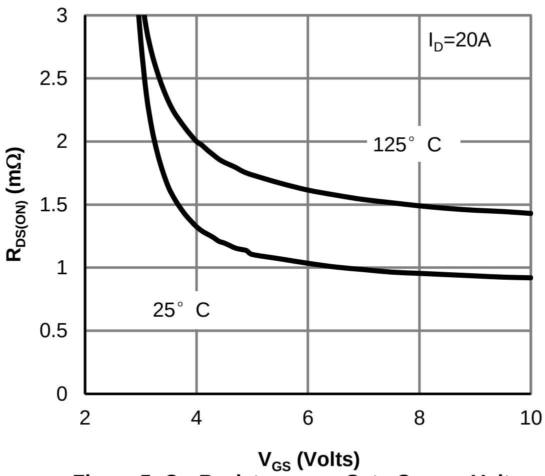


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

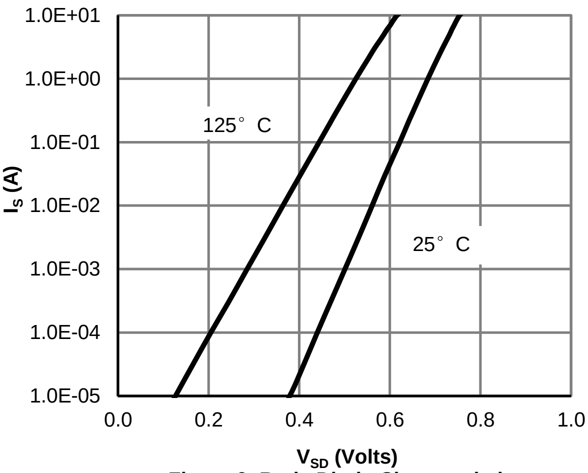


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

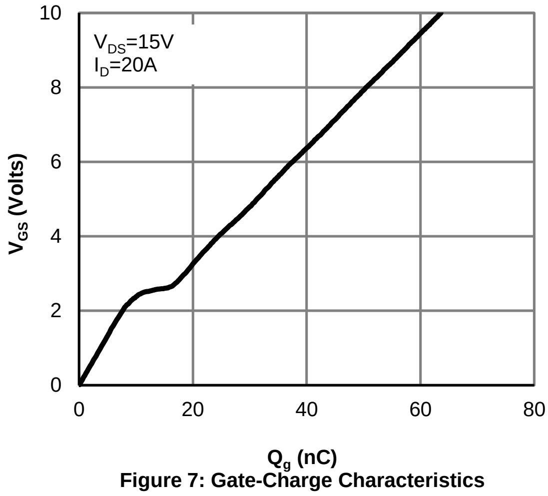


Figure 7: Gate-Charge Characteristics

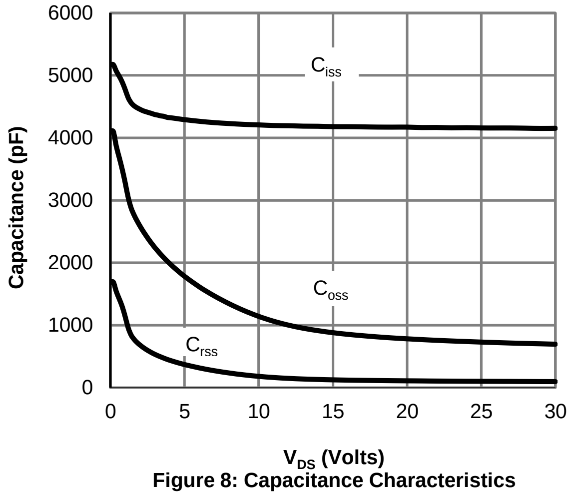


Figure 8: Capacitance Characteristics

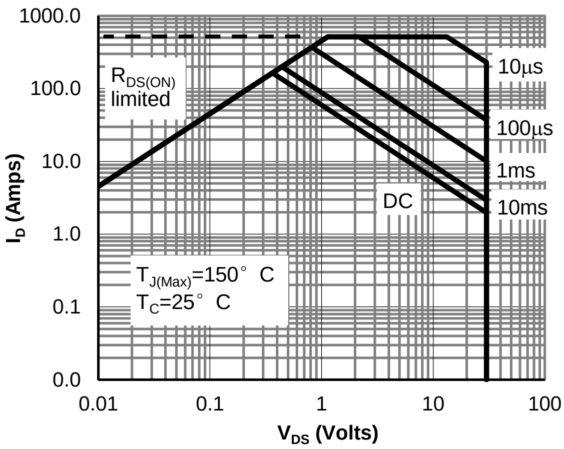


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

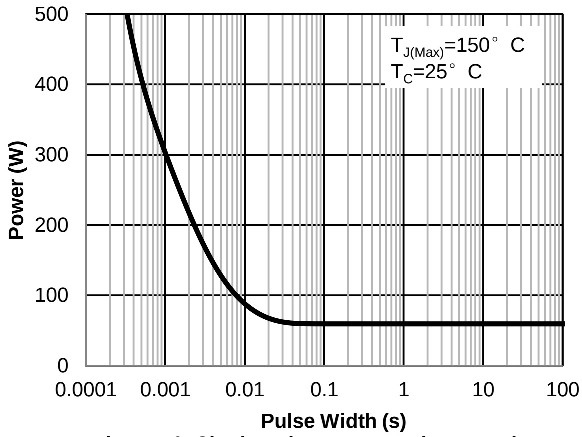


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

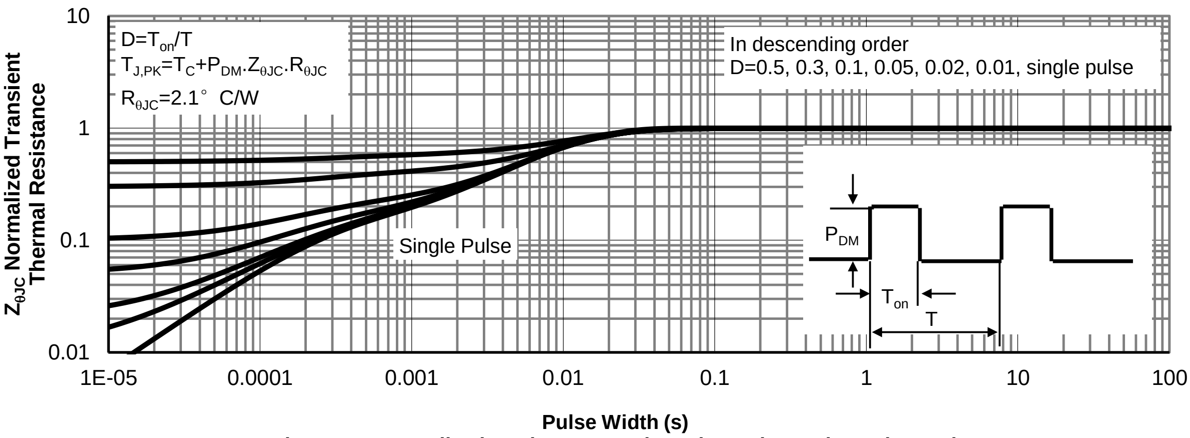


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

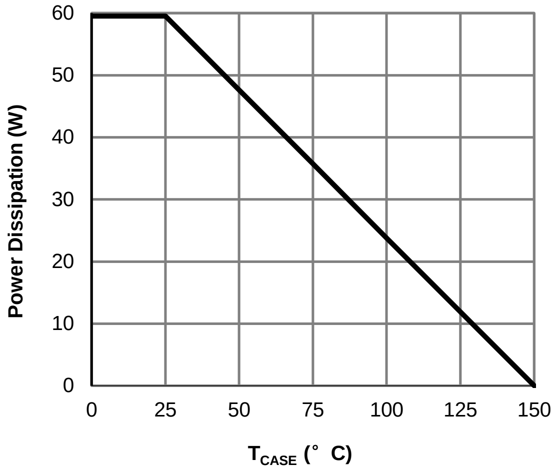


Figure 12: Power De-rating (Note F)

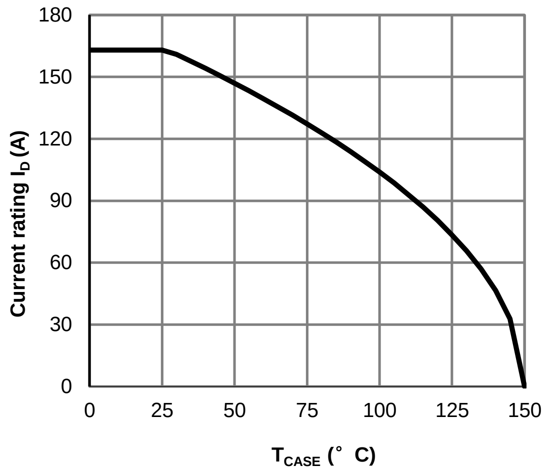


Figure 13: Current De-rating (Note F)

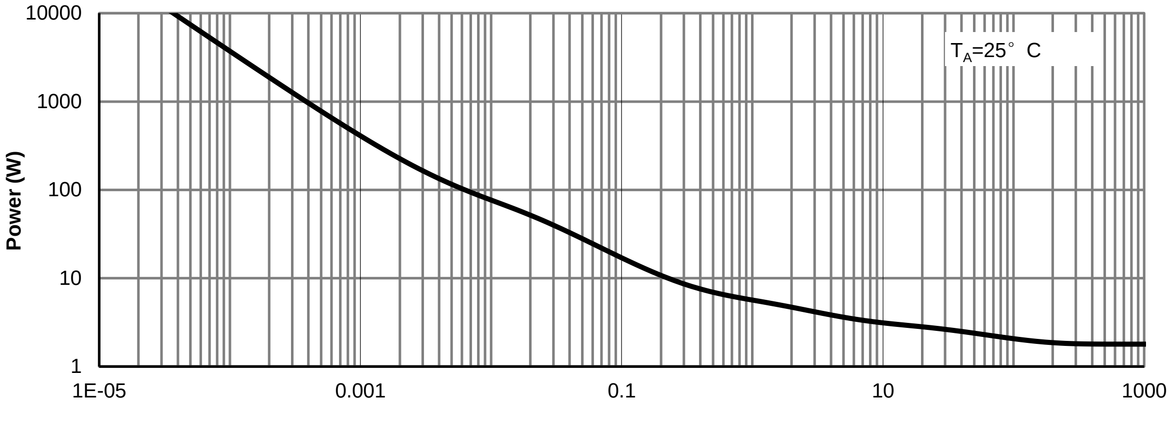


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

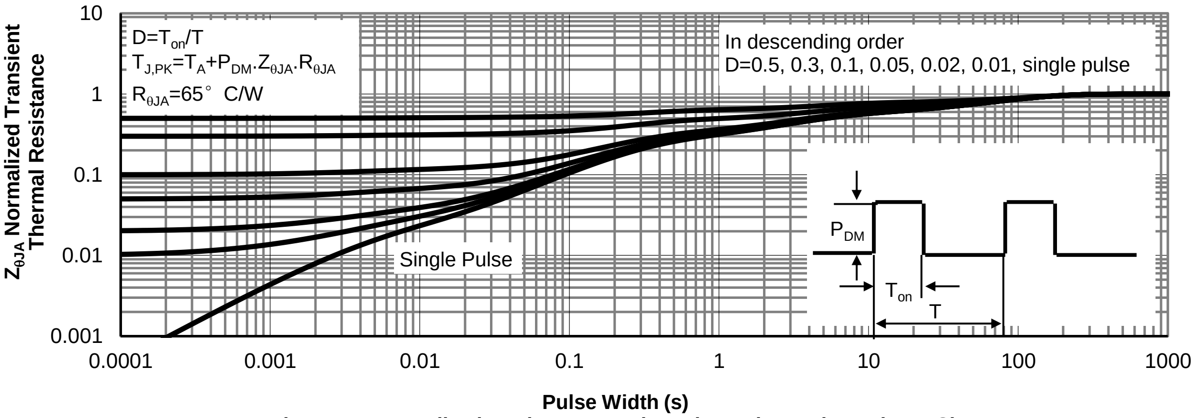


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

Figure A: Gate Charge Test Circuit & Waveforms

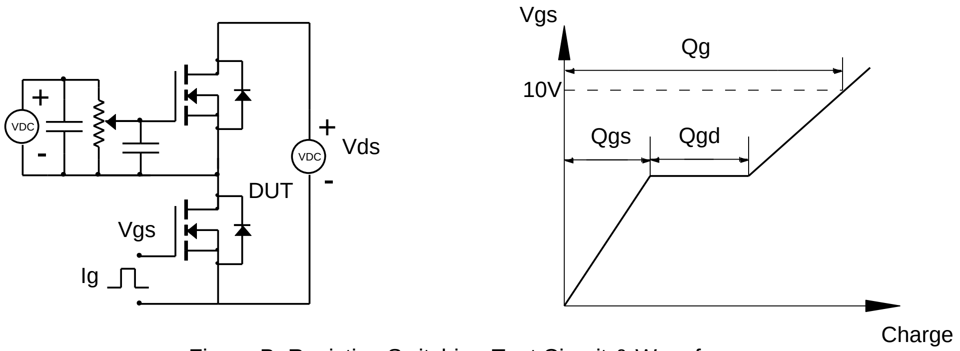


Figure B: Resistive Switching Test Circuit & Waveforms

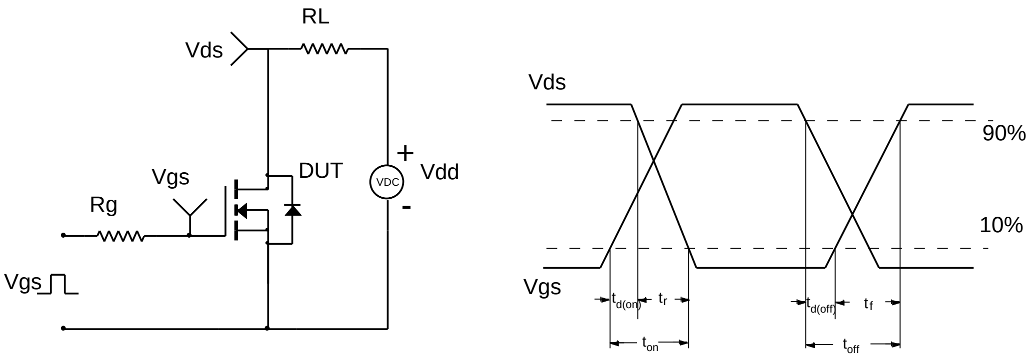


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

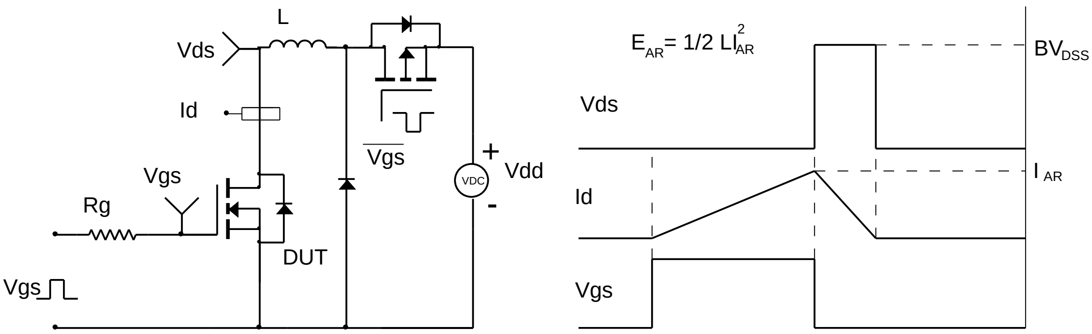


Figure D: Diode Recovery Test Circuit & Waveforms