

Operational Amplifier

Automotive Ultra Low Power Low Offset Voltage Rail-to-Rail Input/Output CMOS Operational Amplifiers

LMR1901YG-M

General Description

LMR1901YG-M single CMOS operational amplifier features ultra low power, low offset voltage and Rail-to-Rail Input/Output that suitable for battery-powered equipment, portable equipment and sensor amplifiers.

Features

- Nano Energy™ Integrated OPAMP
 - AEC-Q100 Qualified^(Note 1)
 - Ultra Low Supply Current
 - Low Input Offset Voltage
 - Rail-to-Rail Input/Output
- (Note 1) Grade 2

Applications

- Battery-powered Equipment
- Portable Equipment
- Sensor Amplifiers
- Car Navigation System
- Car Audio
- Current Monitoring Amplifier
- Human Detection Sensor Amplifier
- Gas Sensor Amplifier
- Photodiode Amplifier

Key Specifications

- Supply Current: 160 nA (Typ)
- Input Offset Voltage: 0.55 mV (Max)
- Common-mode Input Voltage Range: V_{SS} to V_{DD}
- Input Bias Current: 0.5 pA (Typ)
- Operating Supply Voltage Range
 - Single Supply: 1.7 V to 5.5 V
 - Dual Supply: ± 0.85 V to ± 2.75 V
- Operating Temperature Range: -40 °C to +105 °C

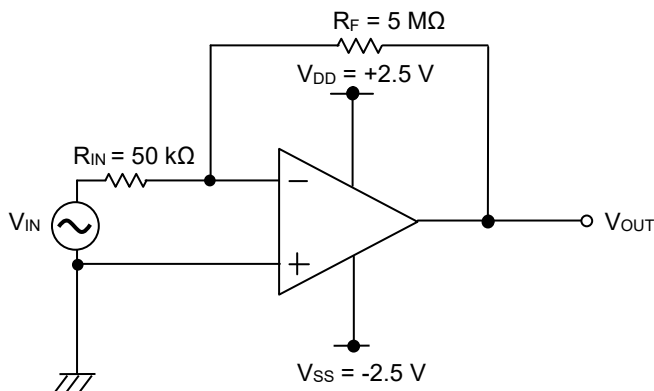
Package
SSOP5

W (Typ) x D (Typ) x H (Max)
2.9 mm x 2.8 mm x 1.25 mm



SSOP5

Typical Application Circuit

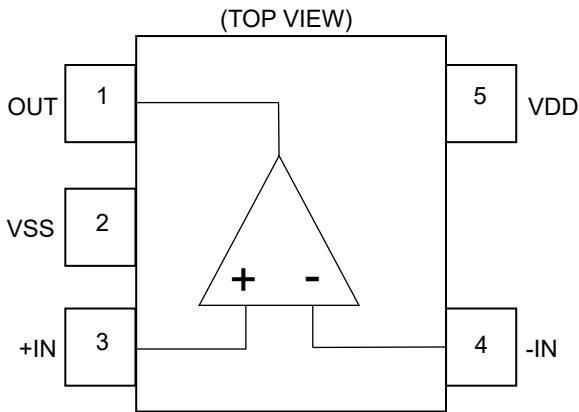


$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

Nano Energy™ is a trademark or a registered trademark of ROHM Co., Ltd.

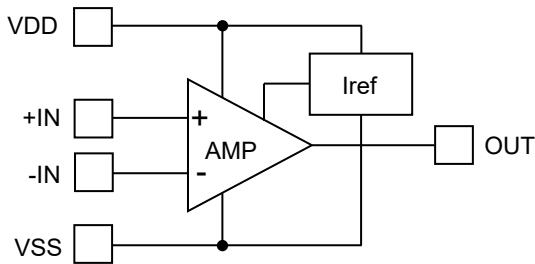
○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration



Pin No.	Pin Name	Function
1	OUT	Output
2	VSS	Negative power supply / Ground
3	+IN	Non-inverting input
4	-IN	Inverting input
5	VDD	Positive power supply

Block Diagram



Description of Blocks

1. AMP:
This block is a Rail-to-Rail input/output operational amplifier with class-AB output circuit and high-precision differential input stage.
2. Iref:
This block supplies reference current which is needed to operate AMP block.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage (V _{DD} - V _{SS})	V _S	7.0	V
Input Pin Voltage (+IN, -IN)	V _I	(V _{SS} - 0.3) to (V _{DD} + 0.3)	V
Input Pin Current (+IN, -IN)	I _I	±10	mA
Maximum Junction Temperature	T _{Jmax}	150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operate over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 3)	2s2p ^(Note 4)	
SSOP5				
Junction to Ambient	θ _{JA}	376.5	185.4	°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ _{JT}	40	30	°C/W

(Note 1) Based on JESD51-2A(Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (V _{DD} - V _{SS})	Single Supply	1.7	3.0	5.5	V
	Dual Supply	±0.85	±1.50	±2.75	
Operating Temperature	Topr	-40	+25	+105	°C

Function Explanation

- Nano Energy™
Nano Energy™ is a combination of technologies which realizes ultra low quiescent current operation.

Electrical Characteristics

(Unless otherwise specified $V_S = 3\text{ V}$, $V_{SS} = 0\text{ V}$, $V_{ICM} = 1.5\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Offset Voltage	V_{IO}	-	0.01	0.55	mV	No load, Absolute value
		-	-	0.75		No load, Absolute value, $T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-	0.6	7.0	$\mu\text{V}/^\circ\text{C}$	No load, Absolute value, $T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Input Offset Current	I_{IO}	-	0	-	pA	Absolute value
Input Bias Current	I_B	-	0.5	-	pA	Absolute value
Common-mode Input Voltage Range	V_{ICMR}	0	-	3	V	V_{SS} to V_{DD}
Supply Current	I_{DD}	-	160	280	nA	No load, $G = 0\text{ dB}$
		-	-	380		No load, $G = 0\text{ dB}$, $T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Output Voltage High	V_{OH}	-	2.5	60	mV	$R_L = 100\text{ k}\Omega$ $V_{OH} = V_{DD} - V_{OUT}$ $T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Output Voltage Low	V_{OL}	-	1	30	mV	$R_L = 100\text{ k}\Omega$ $T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Output Source Current ^(Note 1)	I_{OH}	2.5	6.0	-	mA	$V_{OUT} = V_{SS}$, Absolute value
Output Sink Current ^(Note 1)	I_{OL}	6	14	-	mA	$V_{OUT} = V_{DD}$, Absolute value
Large Signal Voltage Gain	A_v	80	120	-	dB	-
		75	-	-		$T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Gain Bandwidth Product	GBW	-	0.8	-	kHz	$G = 20\text{ dB}$, $C_L = 25\text{ pF}$
Phase Margin	θ	-	70	-	deg	$G = 20\text{ dB}$, $C_L = 25\text{ pF}$
Common-mode Rejection Ratio	CMRR	60	100	-	dB	-
Power Supply Rejection Ratio	PSRR	70	100	-	dB	-
Slew Rate	SR	-	0.3	-	V/ms	$C_L = 25\text{ pF}$
Input-referred Noise Voltage Density	V_n	-	740	-	nV/ $\sqrt{\text{Hz}}$	$f = 10\text{ Hz}$

(Note 1) Consider the power dissipation of the IC under high temperature environment when selecting the output current value. When the output pin is short-circuited continuously, the output current may decrease due to the temperature rise by the heat generation of inside the IC.

Electrical Characteristics - continued

(Unless otherwise specified $V_S = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $V_{ICM} = 2.5\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input Offset Voltage	V_{IO}	-	0.01	0.55	mV	No load, Absolute value
		-	-	0.75		No load, Absolute value, $T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-	0.6	7.0	$\mu\text{V}/^\circ\text{C}$	No load, Absolute value, $T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Input Offset Current	I_{IO}	-	0	-	pA	Absolute value
Input Bias Current	I_B	-	0.5	-	pA	Absolute value
Common-mode Input Voltage Range	V_{ICMR}	0	-	5	V	V_{SS} to V_{DD}
Supply Current	I_{DD}	-	175	280	nA	No load, $G = 0\text{ dB}$
		-	-	380		No load, $G = 0\text{ dB}$, $T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Output Voltage High	V_{OH}	-	2.5	60	mV	$R_L = 100\text{ k}\Omega$ $V_{OH} = V_{DD} - V_{OUT}$ $T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Output Voltage Low	V_{OL}	-	1	30	mV	$R_L = 100\text{ k}\Omega$ $T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Output Source Current ^(Note 1)	I_{OH}	10	20	-	mA	$V_{OUT} = V_{SS}$, Absolute value
Output Sink Current ^(Note 1)	I_{OL}	18	35	-	mA	$V_{OUT} = V_{DD}$, Absolute value
Large Signal Voltage Gain	A_v	80	135	-	dB	-
		75	-	-		$T_a = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$
Gain Bandwidth Product	GBW	-	1	-	kHz	$G = 20\text{ dB}$, $C_L = 25\text{ pF}$
Phase Margin	θ	-	70	-	deg	$G = 20\text{ dB}$, $C_L = 25\text{ pF}$
Common-mode Rejection Ratio	CMRR	60	115	-	dB	-
Power Supply Rejection Ratio	PSRR	70	100	-	dB	-
Slew Rate	SR	-	0.3	-	V/ms	$C_L = 25\text{ pF}$
Input-referred Noise Voltage Density	V_n	-	690	-	nV/ $\sqrt{\text{Hz}}$	$f = 10\text{ Hz}$

(Note 1) Consider the power dissipation of the IC under high temperature environment when selecting the output current value. When the output pin is short-circuited continuously, the output current may decrease due to the temperature rise by the heat generation of inside the IC.

Typical Performance Curves

$V_{SS} = 0\text{ V}$

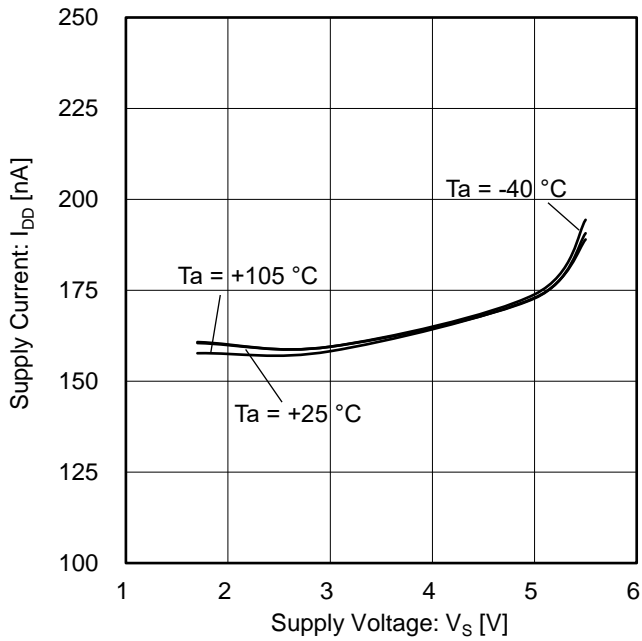


Figure 1. Supply Current vs Supply Voltage

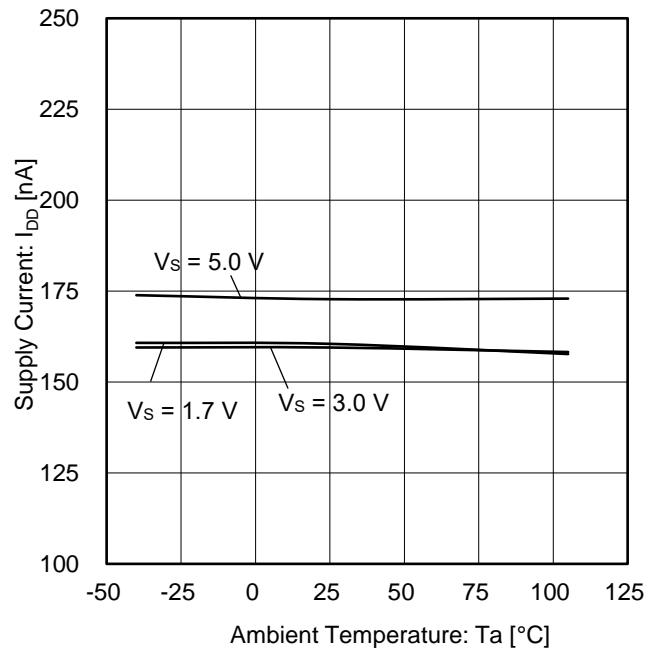


Figure 2. Supply Current vs Ambient Temperature

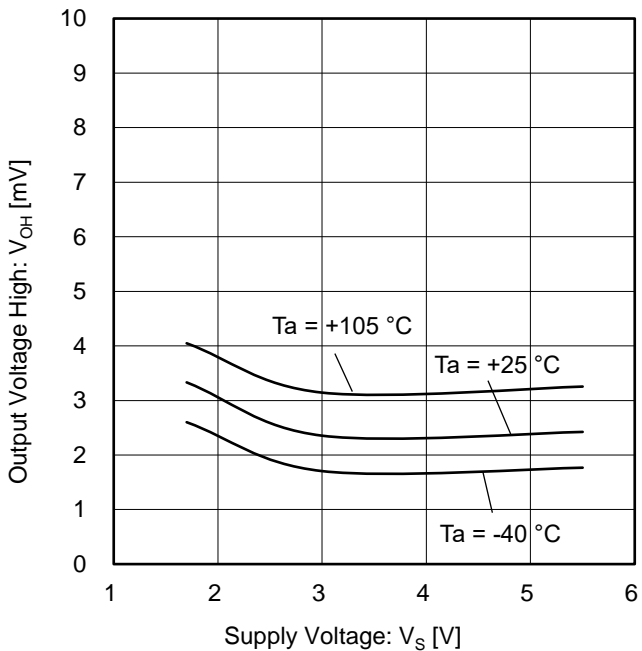


Figure 3. Output Voltage High vs Supply Voltage
($R_L = 100\text{ k}\Omega$)

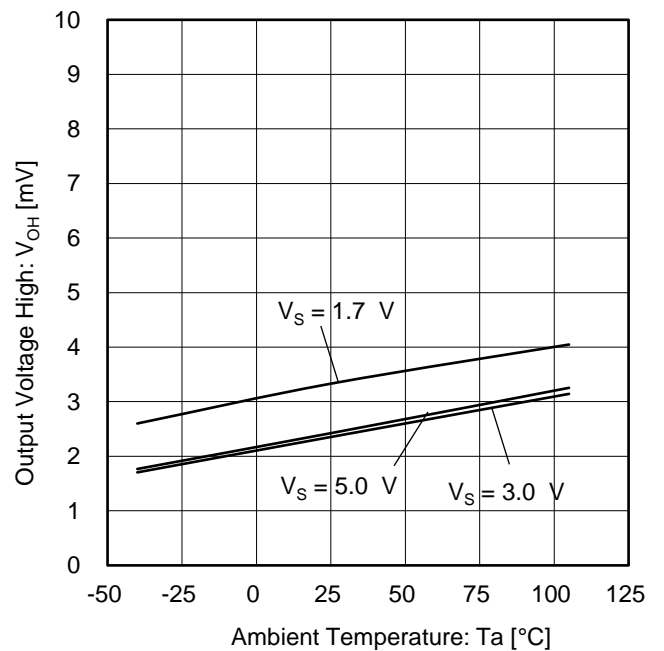


Figure 4. Output Voltage High vs Ambient Temperature
($R_L = 100\text{ k}\Omega$)

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

$V_{SS} = 0\text{ V}$

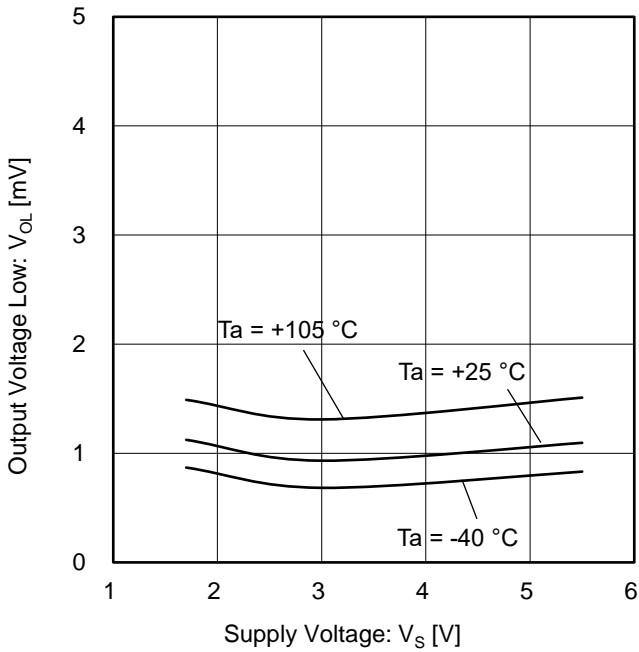


Figure 5. Output Voltage Low vs Supply Voltage ($R_L = 100\text{ k}\Omega$)

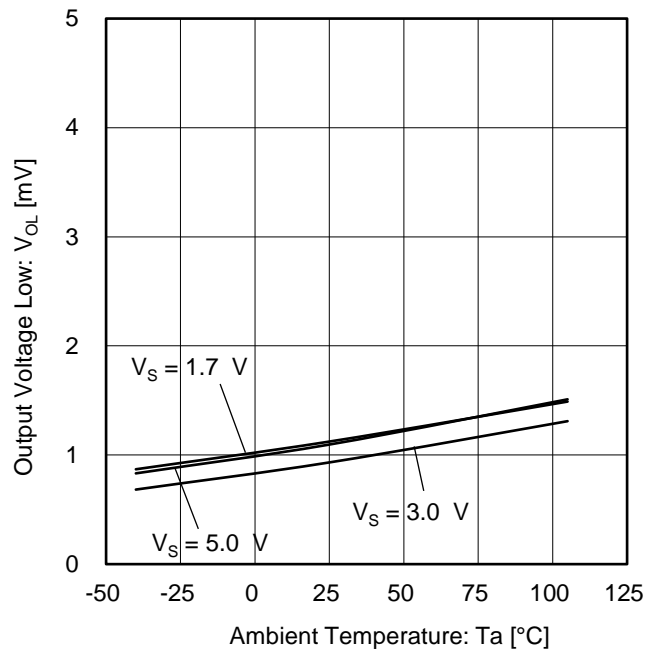


Figure 6. Output Voltage Low vs Ambient Temperature ($R_L = 100\text{ k}\Omega$)

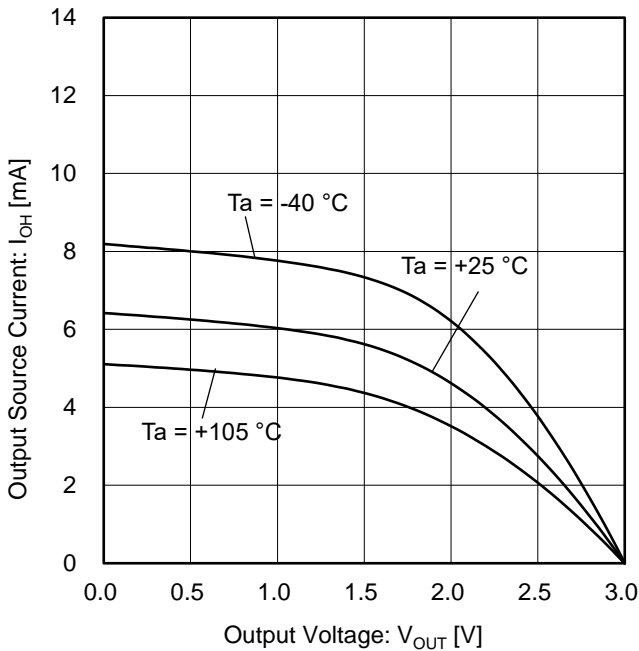


Figure 7. Output Source Current vs Output Voltage ($V_S = 3\text{ V}$)

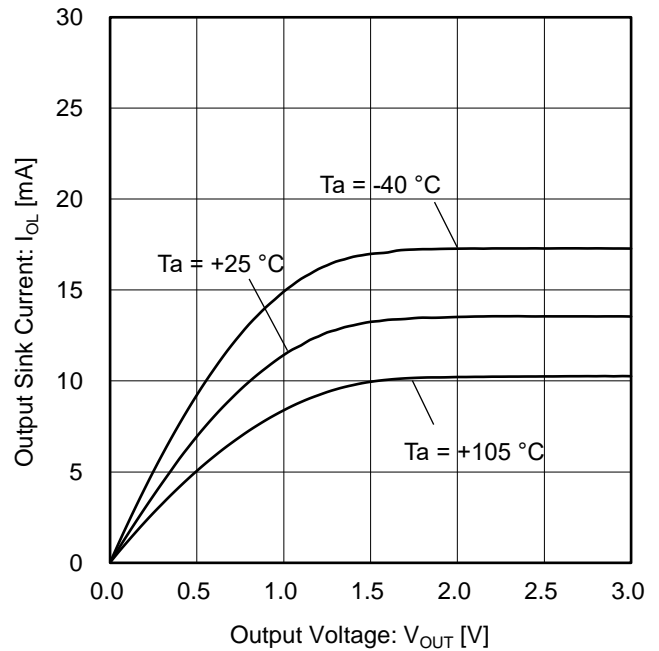


Figure 8. Output Sink Current vs Output Voltage ($V_S = 3\text{ V}$)

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

$V_{SS} = 0\text{ V}$

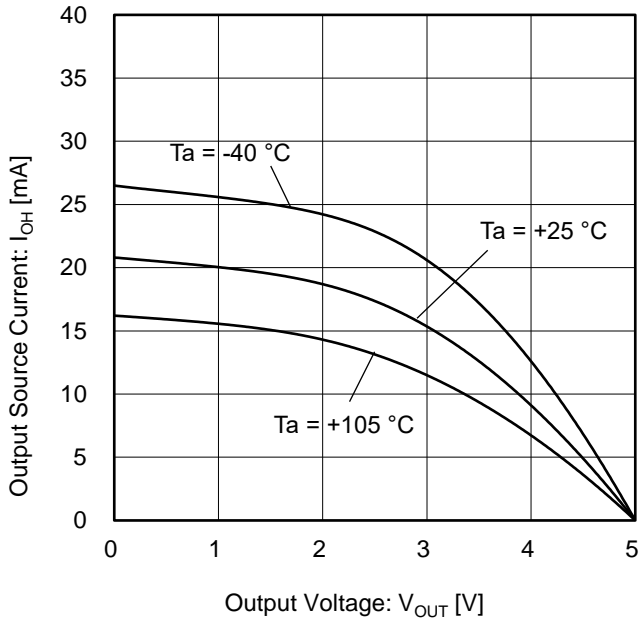


Figure 9. Output Source Current vs Output Voltage ($V_S = 5\text{ V}$)

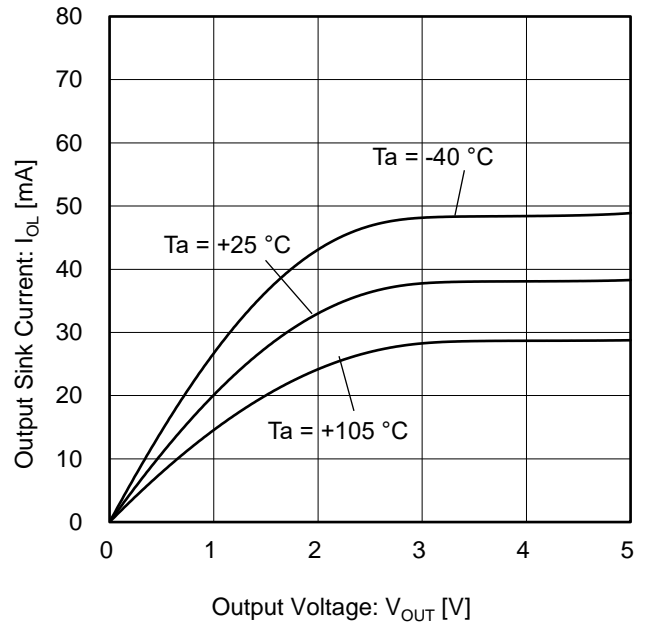


Figure 10. Output Sink Current vs Output Voltage ($V_S = 5\text{ V}$)

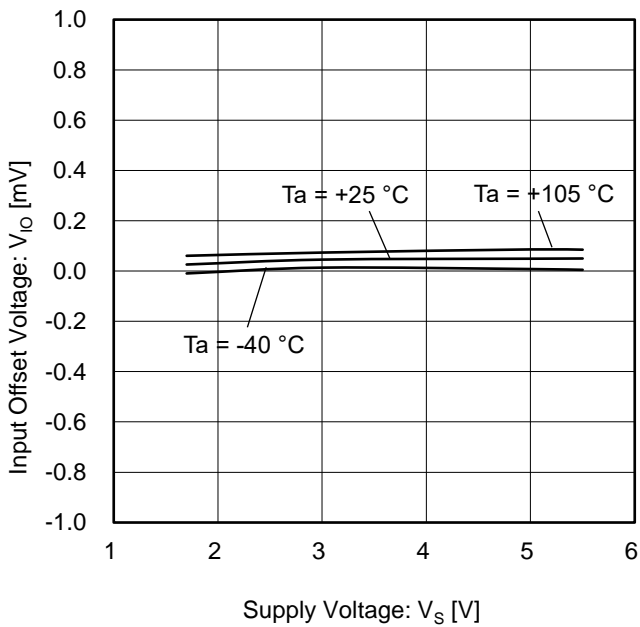


Figure 11. Input Offset Voltage vs Supply Voltage ($V_{ICM} = 0\text{ V}$)

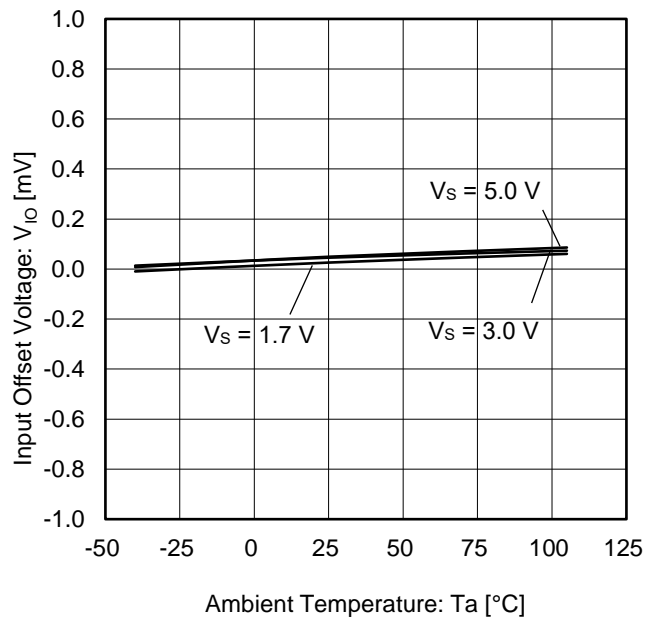


Figure 12. Input Offset Voltage vs Ambient Temperature ($V_{ICM} = 0\text{ V}$)

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

$V_{SS} = 0\text{ V}$

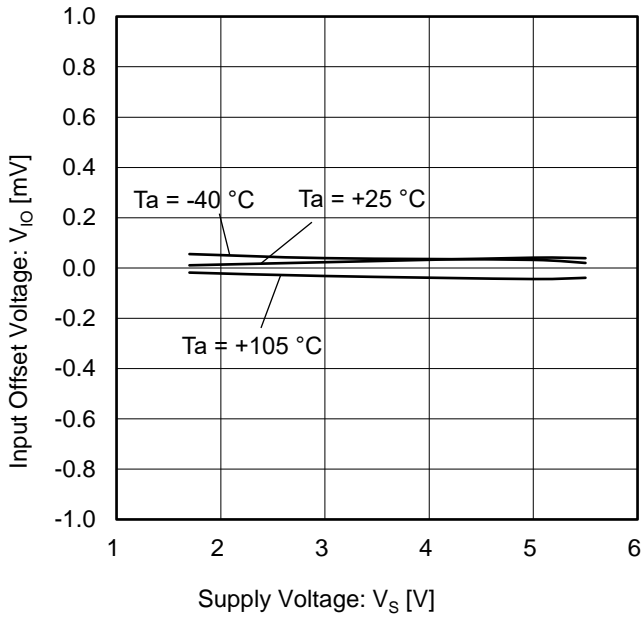


Figure 13. Input Offset Voltage vs Supply Voltage ($V_{ICM} = V_{DD}$)

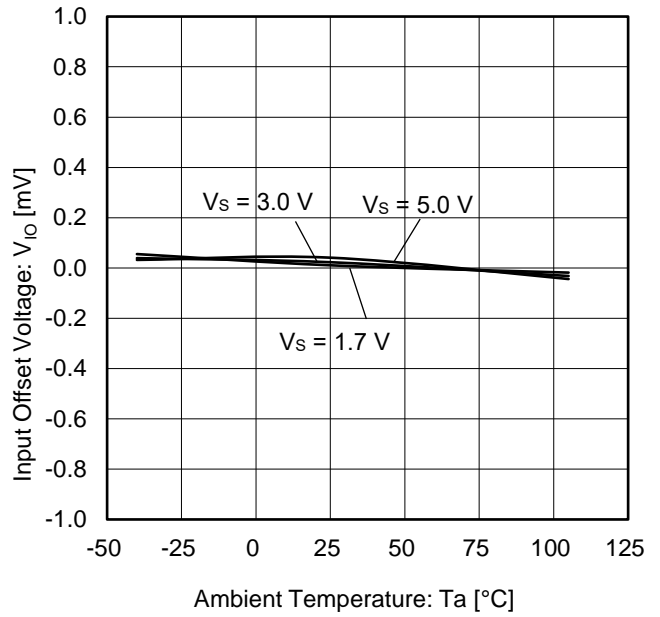


Figure 14. Input Offset Voltage vs Ambient Temperature ($V_{ICM} = V_{DD}$)

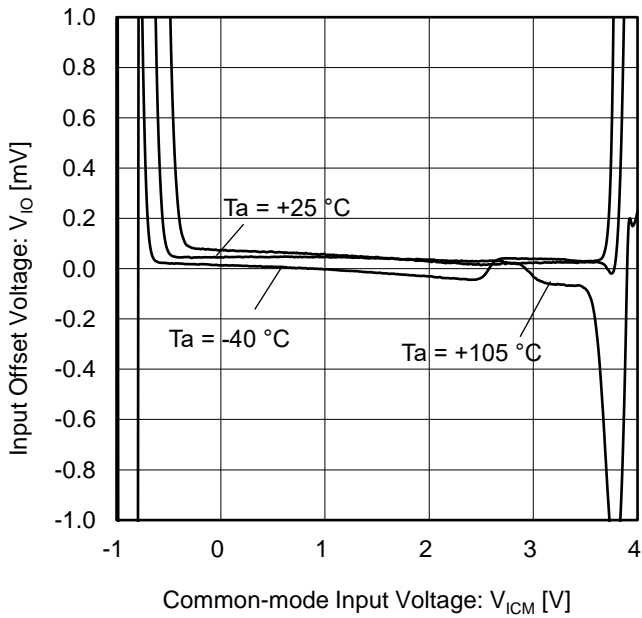


Figure 15. Input Offset Voltage vs Common-mode Input Voltage ($V_S = 3\text{ V}$)

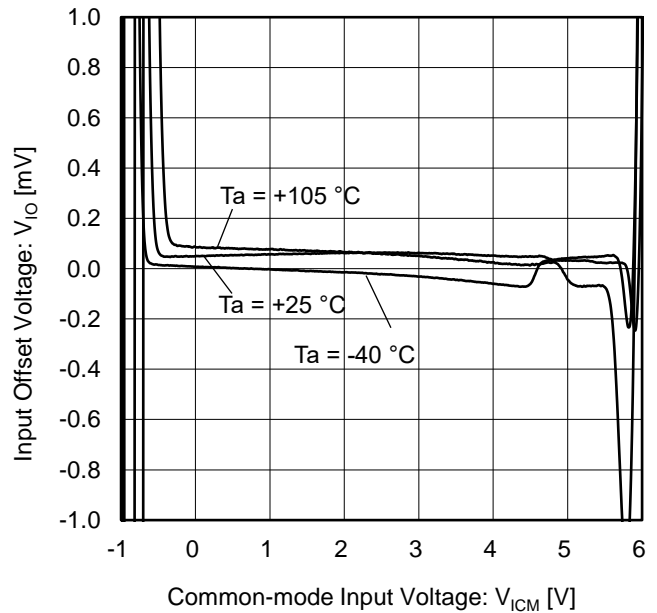


Figure 16. Input Offset Voltage vs Common-mode Input Voltage ($V_S = 5\text{ V}$)

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

$V_{SS} = 0\text{ V}$

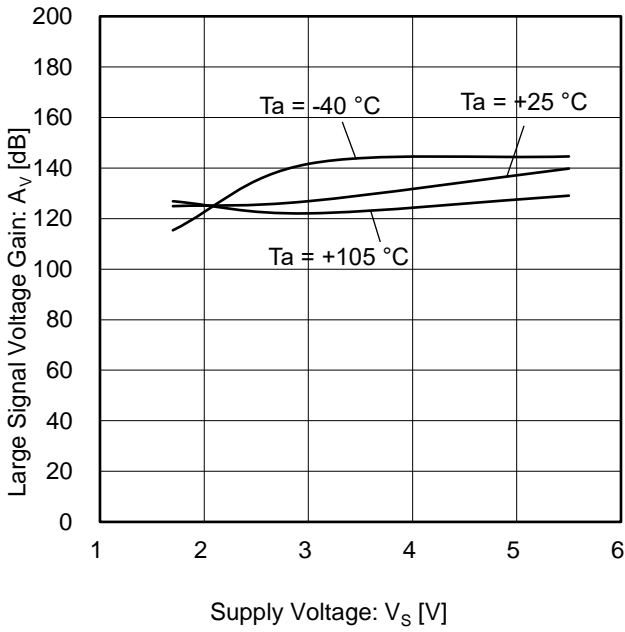


Figure 17. Large Signal Voltage Gain vs Supply Voltage

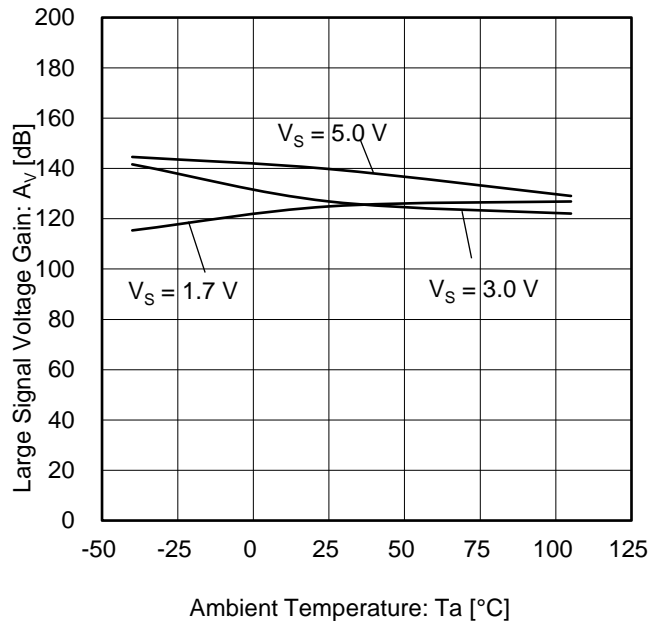


Figure 18. Large Signal Voltage Gain vs Ambient Temperature

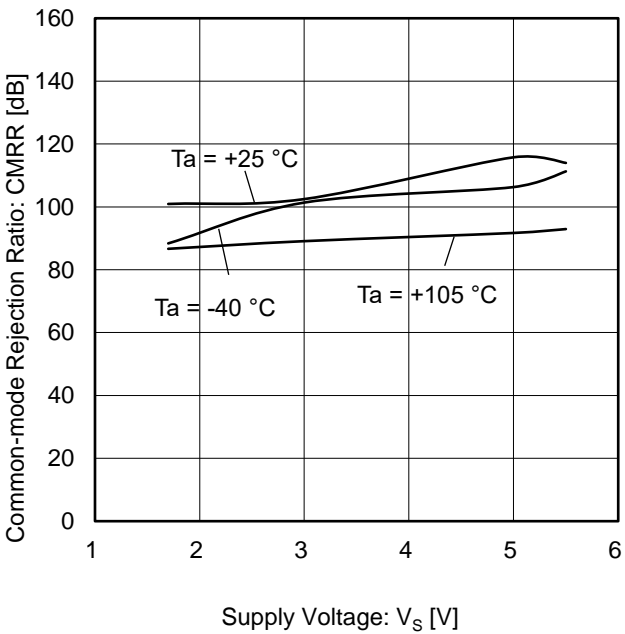


Figure 19. Common-mode Rejection Ratio vs Supply Voltage

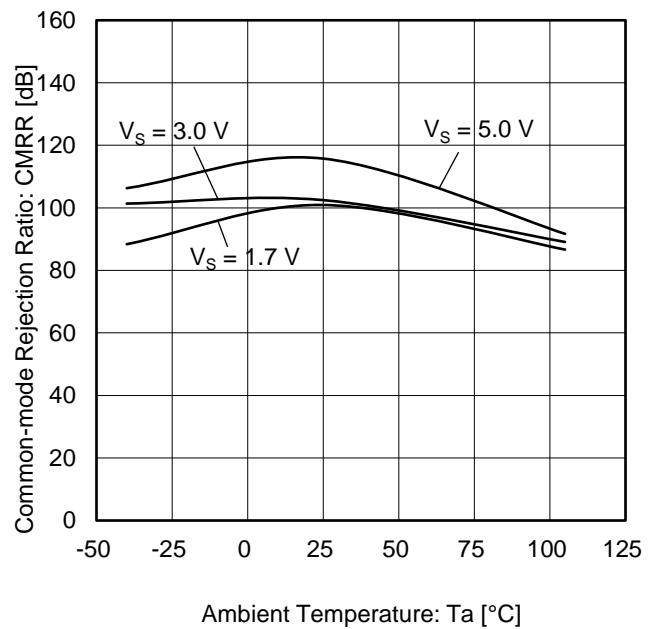


Figure 20. Common-mode Rejection Ratio vs Ambient Temperature

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

$V_{SS} = 0\text{ V}$

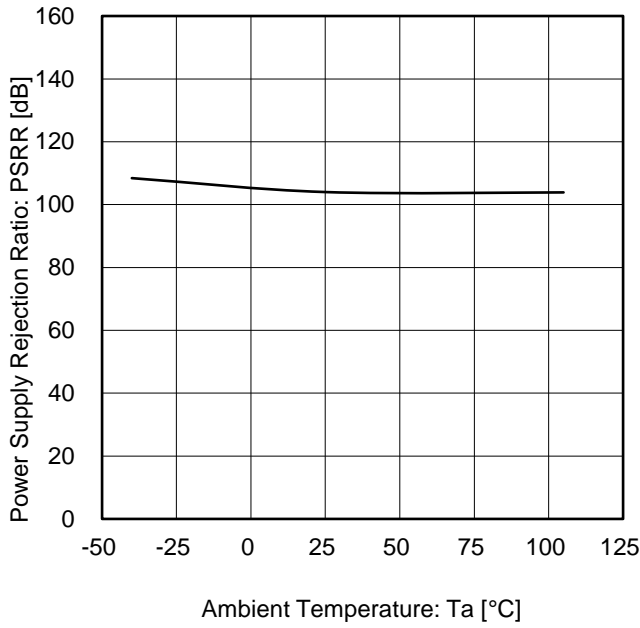


Figure 21. Power Supply Rejection Ratio vs Ambient Temperature

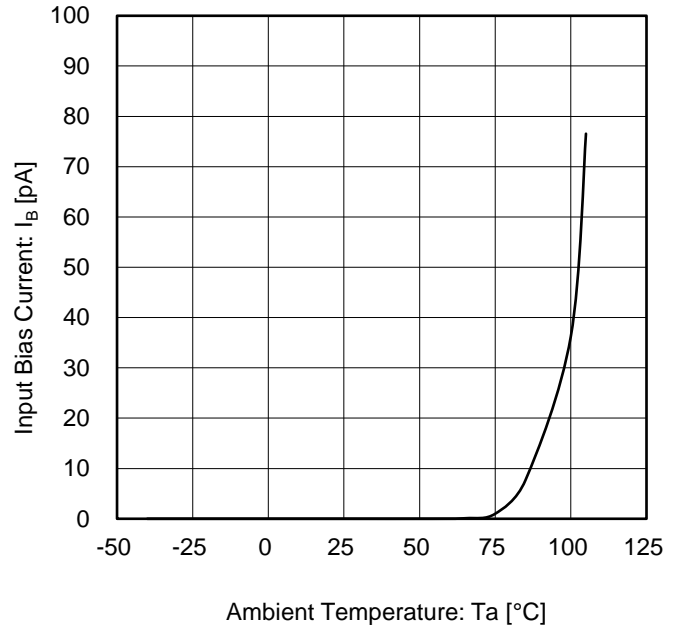


Figure 22. Input Bias Current vs Ambient Temperature

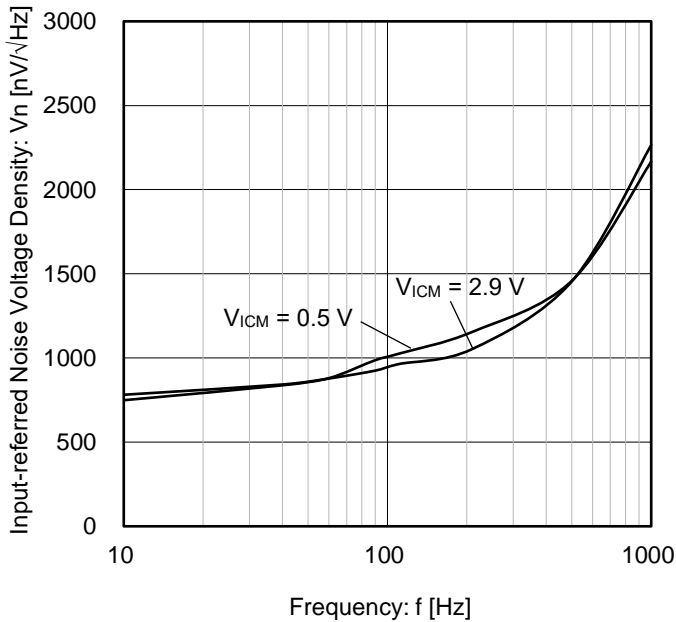


Figure 23. Input-referred Noise Voltage Density vs Frequency ($V_S = 3\text{ V}$)

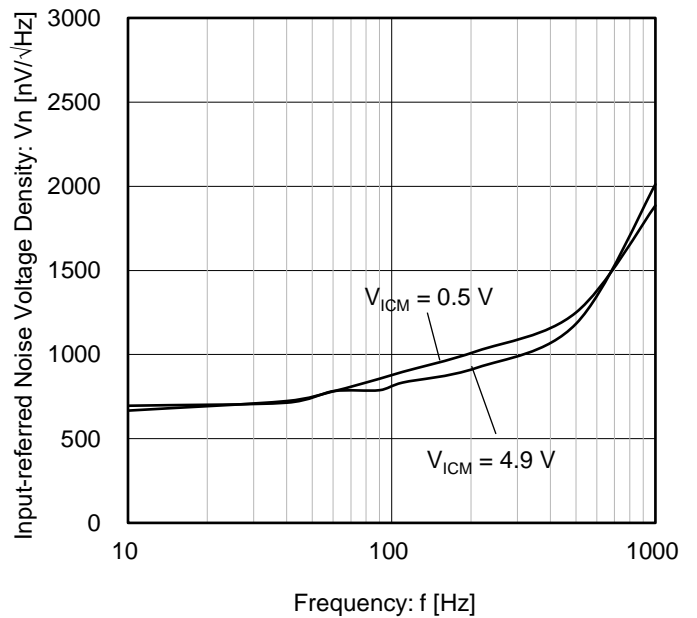


Figure 24. Input-referred Noise Voltage Density vs Frequency ($V_S = 5\text{ V}$)

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

$V_{SS} = 0\text{ V}$

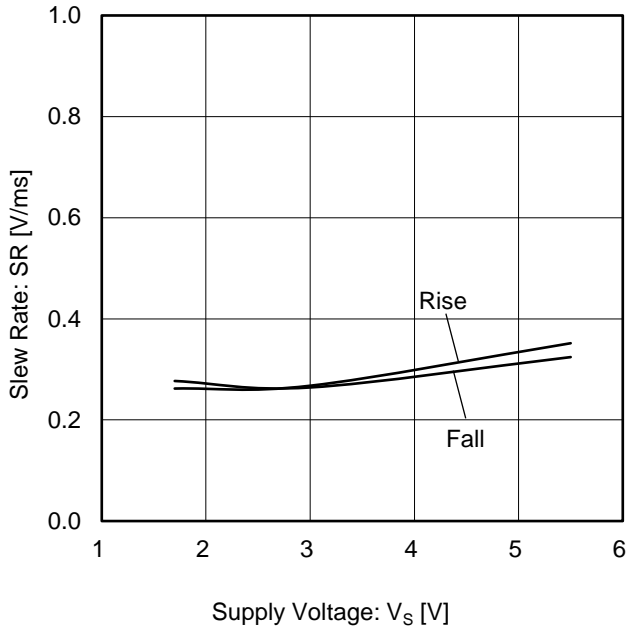


Figure 25. Slew Rate vs Supply Voltage

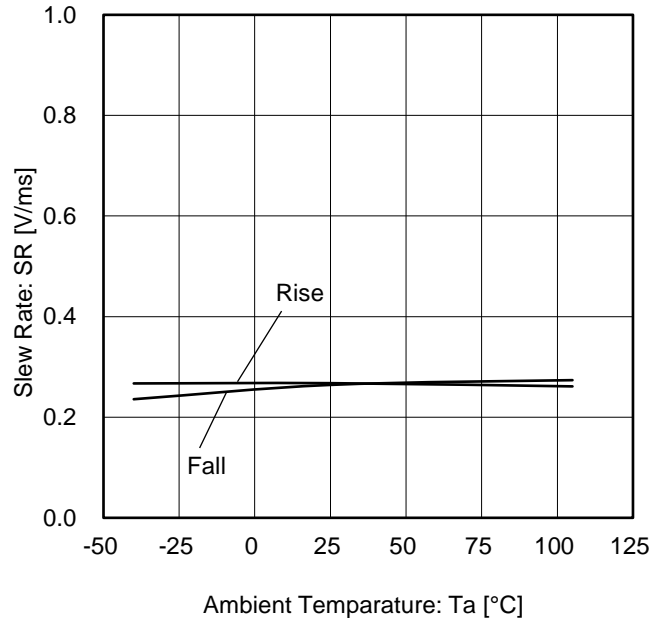


Figure 26. Slew Rate vs Ambient Temperature ($V_S = 3\text{ V}$)

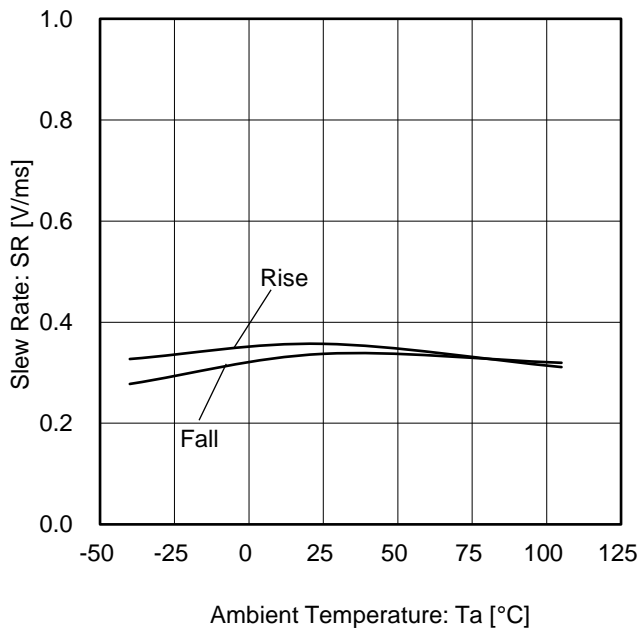


Figure 27. Slew Rate vs Ambient Temperature ($V_S = 5\text{ V}$)

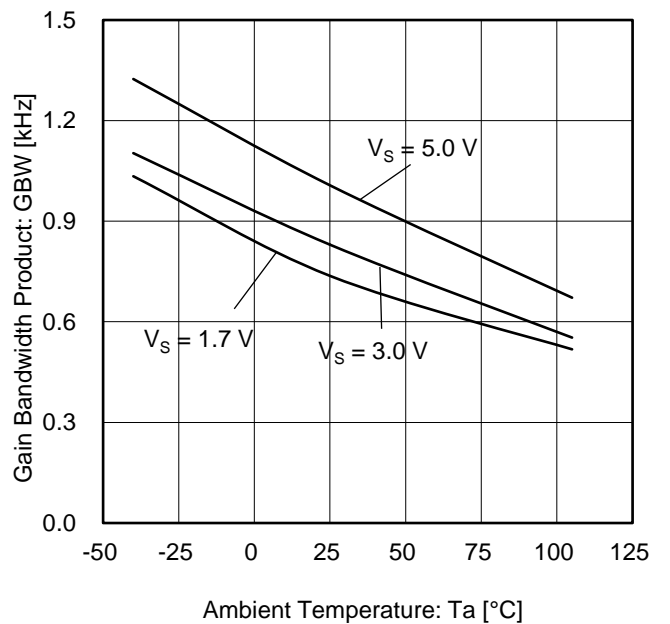


Figure 28. Gain Bandwidth Product vs Ambient Temperature

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

$V_{SS} = 0\text{ V}$

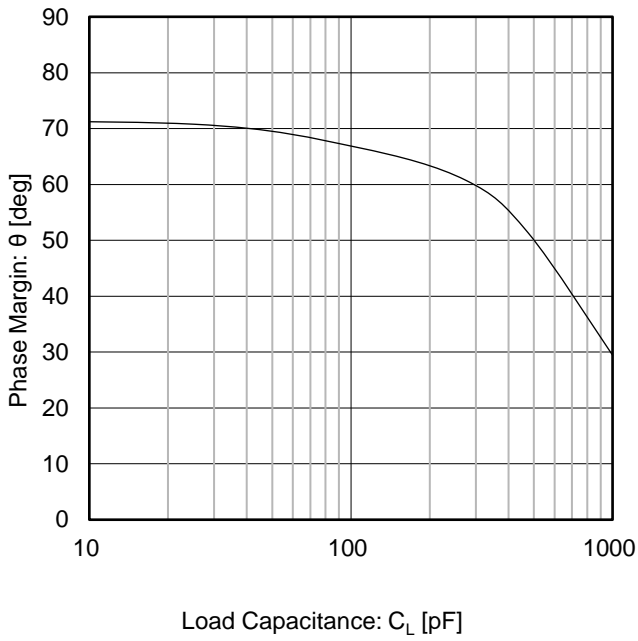


Figure 29. Phase Margin vs Load Capacitance
($V_S = 3\text{ V}$, $R_F = 5\text{ M}\Omega$, $G = 20\text{ dB}$)

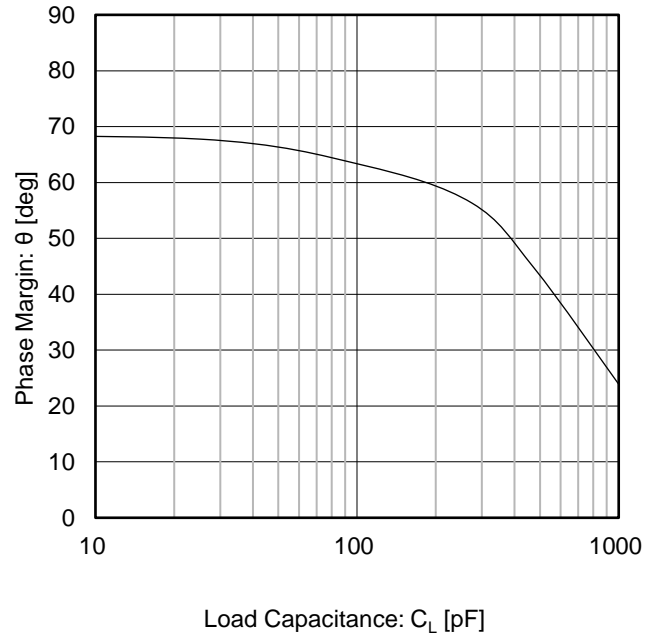


Figure 30. Phase Margin vs Load Capacitance
($V_S = 5\text{ V}$, $R_F = 5\text{ M}\Omega$, $G = 20\text{ dB}$)

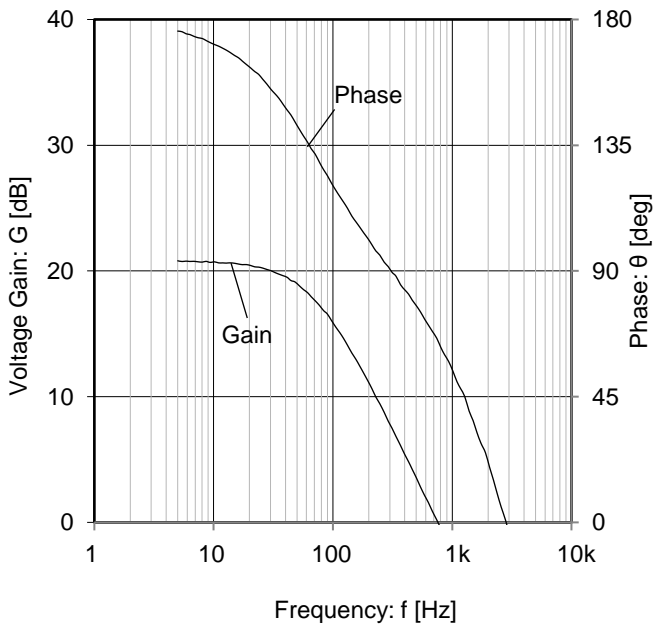


Figure 31. Voltage Gain, Phase vs Frequency
($V_S = 3\text{ V}$)

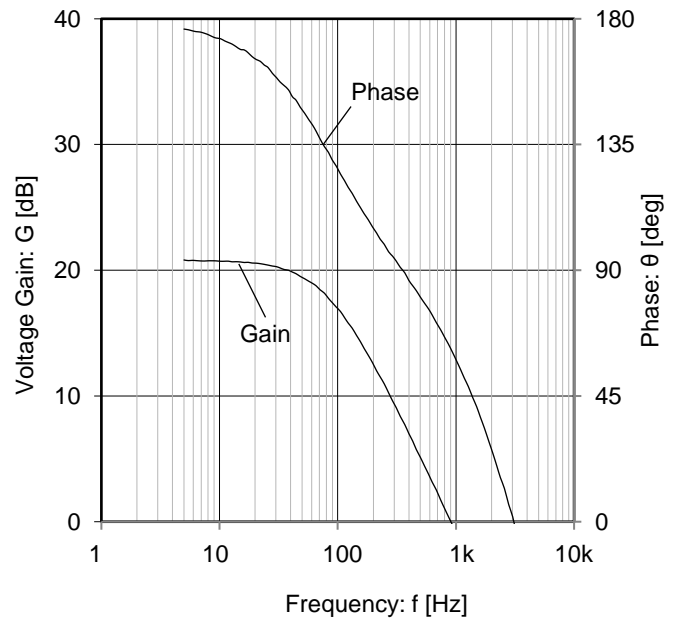


Figure 32. Voltage Gain, Phase vs Frequency
($V_S = 5\text{ V}$)

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Typical Performance Curves - continued

V_{SS} = 0 V

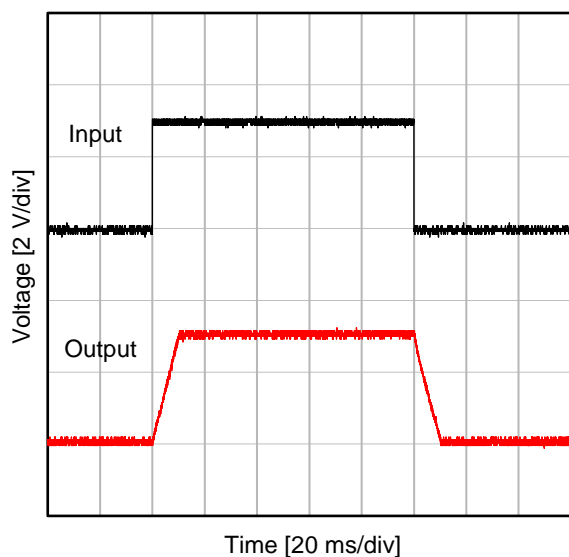


Figure 33. Large-Signal Step Response
(V_s = 3 V, G = 0 dB, R_L = 1 MΩ, C_L = 25 pF)

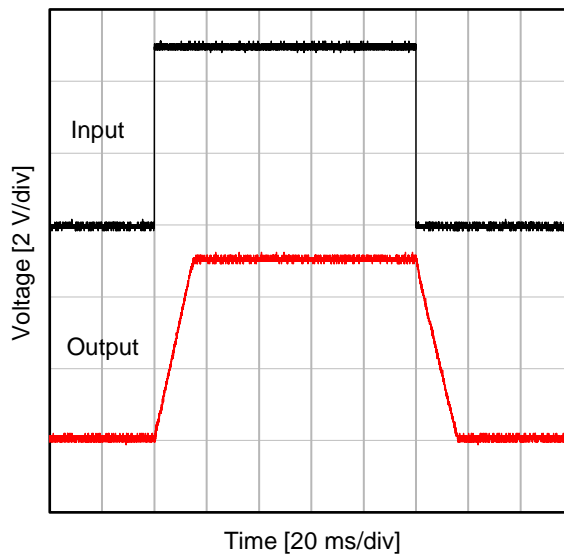


Figure 34. Large-Signal Step Response
(V_s = 5 V, G = 0 dB, R_L = 1 MΩ, C_L = 25 pF)

(Note) The above data is measurement value of typical sample, it is not guaranteed.

Application Examples

oVoltage Follower

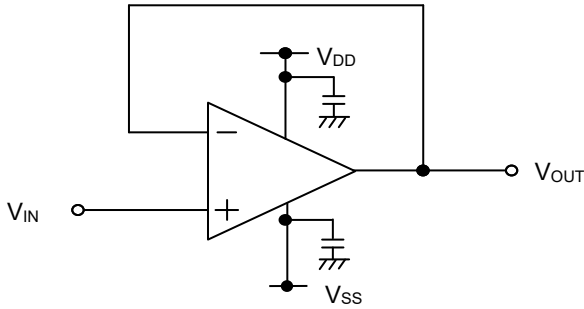


Figure 35. Voltage Follower Circuit

Using this circuit, the output voltage (V_{OUT}) is configured to be equal to the input voltage (V_{IN}). This circuit also stabilizes the output voltage due to high input impedance and low output impedance. Computation for output voltage is shown below.

$$V_{OUT} = V_{IN}$$

oInverting Amplifier

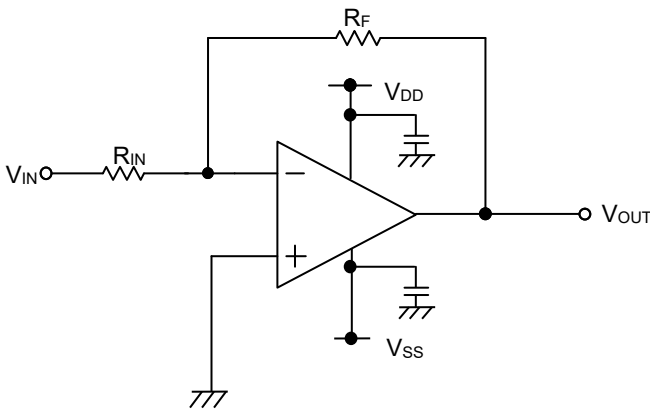


Figure 36. Inverting Amplifier Circuit

For inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain which depends on the ratio of R_{IN} and R_F , and then it outputs phase-inverted voltage. The output voltage is shown in the next expression.

$$V_{OUT} = -\frac{R_F}{R_{IN}} V_{IN}$$

This circuit has input impedance equal to R_{IN} .

oNon-inverting Amplifier

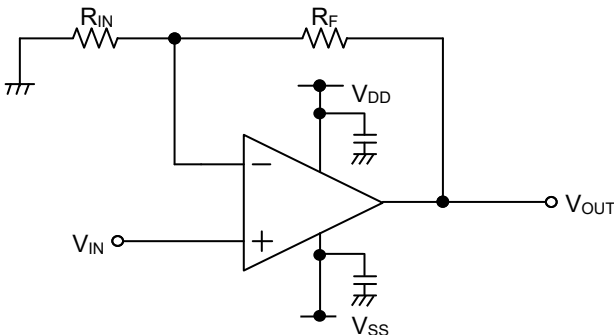


Figure 37. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain, which depends on the ratio of R_{IN} and R_F . The output voltage (V_{OUT}) is in-phase with the input voltage and is shown in the next expression.

$$V_{OUT} = \left(1 + \frac{R_F}{R_{IN}}\right) V_{IN}$$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

I/O Equivalence Circuits

Pin No.	Pin Name	Pin Description	Equivalence Circuit
1	OUT	Output	
3 4	+IN -IN	Input	

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

- When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.
- When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

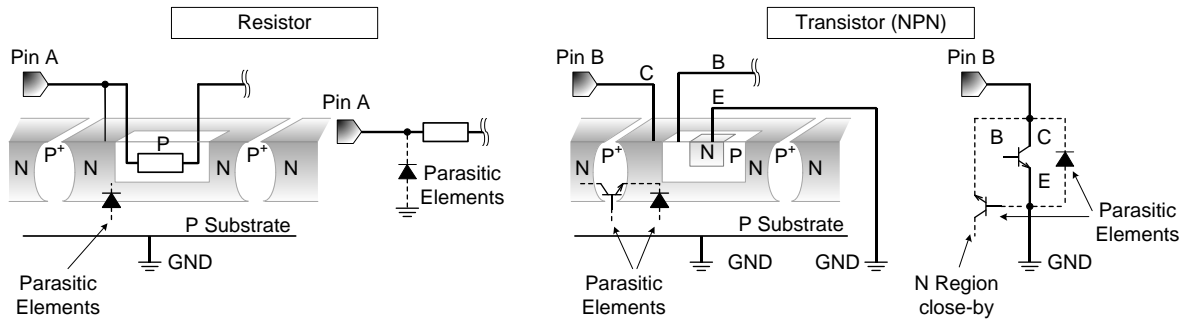
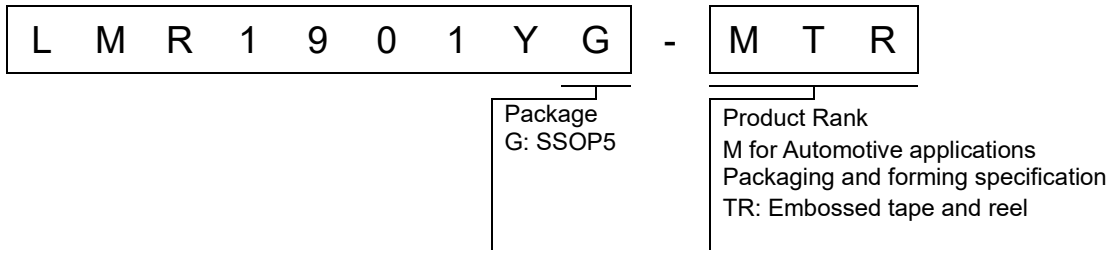


Figure 38. Example of Monolithic IC Structure

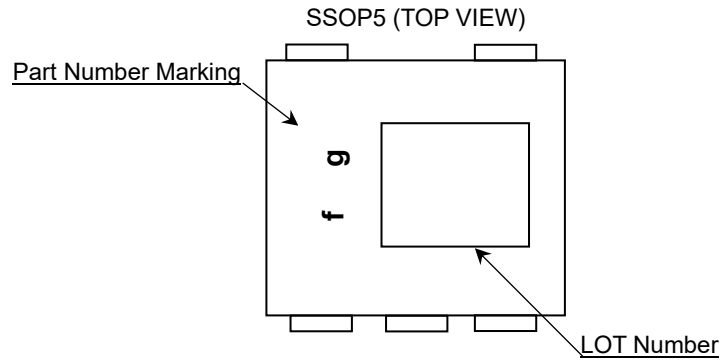
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

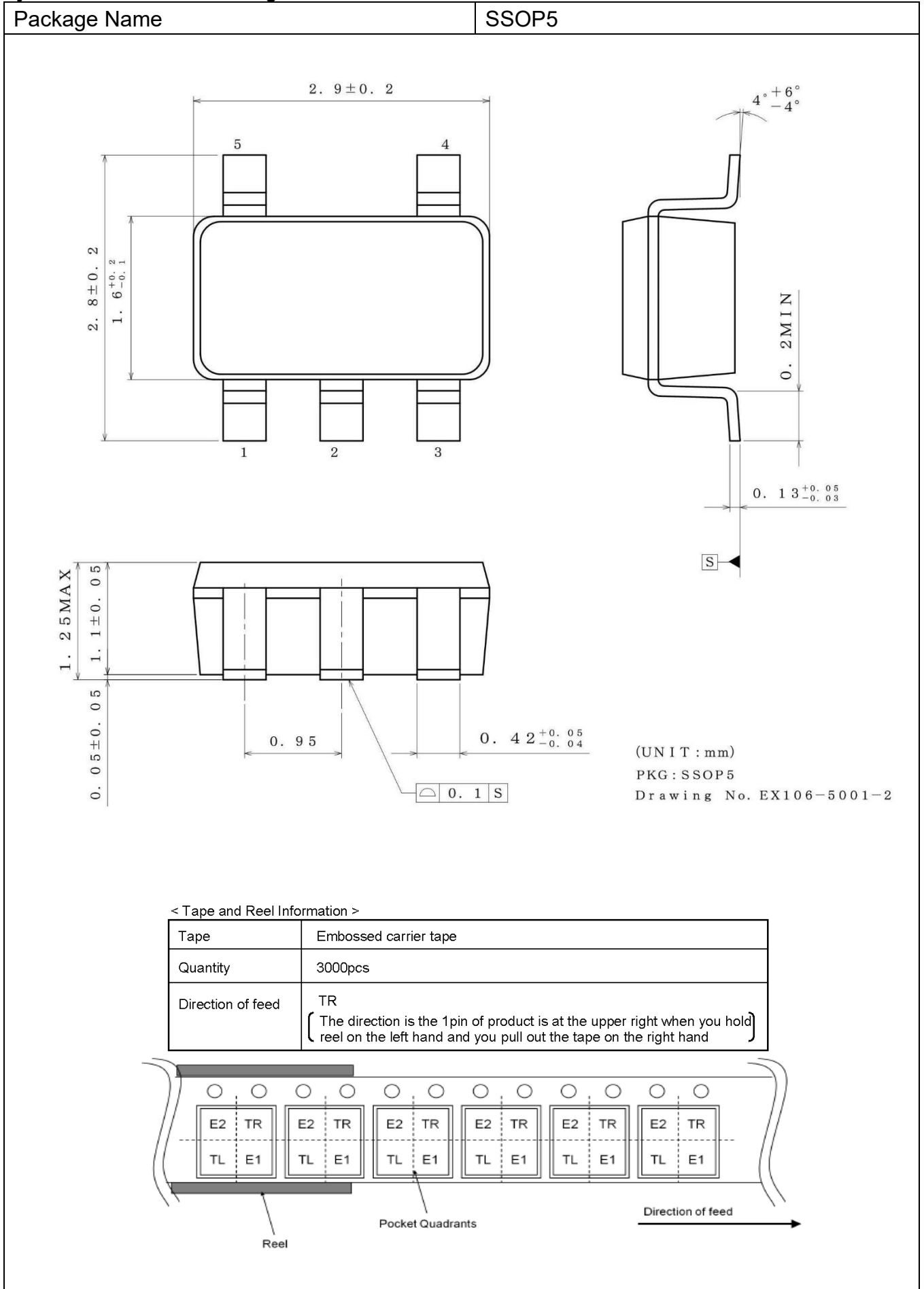
Ordering Information



Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
04.Aug.2023	001	New Release

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CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
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