RA2A2 Group
Renesas Microcontrollers

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Ultra low power 48 MHz Arm® Cortex®-M23 core, up to 512-KB code flash memory, 48-KB SRAM, 12-bit A/D Converter, 24-bit Sigma-Delta A/D Converter, LCD Controller/driver, Independent power supply RTC, On-chip 32-bit multiplier and multiply-accumulator, Security and Safety features.

Features

Arm Cortex-M23 Core

- Armv8-M architecture
- Maximum operating frequency: 48 MHz
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: DWT, FPB, CoreSight™ MTB-M23
- CoreSight Debug Port: SW-DP

Memory

- Up to 512-KB code flash memory
- Bank Swap
- Dual bank flash (256 KB × 2 banks)
- 8-KB data flash memory (100,000 program/erase (P/E) cycles)
- 48-KB SRAM
- Memory Protection Units (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

Connectivity

- Serial Communications Interface (SCI) × 5
  - Asynchronous interfaces
  - 8-bit clock synchronous interface
  - Simple IIC
  - Simple SPI
  - Smart card interface
- Serial Peripheral Interface (SPI) × 1
- I^2C bus interface (IIC) × 2

Analog

- 24-bit Sigma-Delta A/D Converter (SDADC24)
  - Sampling rate is 7.813 kHz/8.333 kHz or 3.906 kHz/4.166 kHz
  - Differential/Single-ended input mode, up to 7 ch
  - Main clock oscillator (MOSC) 12 MHz or 16 MHz
  - PLL clock multiplied from Sub-clock oscillator (SOSC) (32.768 kHz)
  - High-speed on-chip oscillator (HOCO) (24/32/48/64 MHz)
- 12-bit A/D Converter (ADC12)
- Temperature Sensor (TSN)

Timers

- General PWM Timer 16-bit (GPT16) × 6
- 16-bit Low Power Asynchronous General Purpose Timer (AGT) × 8
- 32-bit Low Power Asynchronous General Purpose Timer (AGTW) × 2
- Watchdog Timer (WDT)

Human Machine Interface (HMI)

- Segment LCD Controller (SLCDC)
  - Internal voltage boosting method, capacitor split method, and external resistance division method are switchable
  - Segment signal output: 21 to 45 (when 8 com is not used)
  - Segment signal output: 17 to 41 (when 8 com is used)
  - Common signal output: 4 (when 8 com is not used)
  - Common signal output: 8 (when 8 com is used)
  - Waveform A or B selectable

On-Chip 32-Bit Multiplier and Multiply-Accumulator (MACL)

- 32 bits × 32 bits = 64 bits (unsigned or signed)
- 32 bits × 32 bits + 64 bits = 64 bits (unsigned or signed)
- The results of multiply-and-accumulate operations (cumulative values) can be retained in any of 24 buffer channels and can be accessed with independent address.

Safety

- ECC in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC)
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Sub and main oscillation stop detection circuit for SDADC24 clock switch
- Illegal memory access

Security and Encryption

- AES
  - Cipher modes of operation: ECB/CBC/CTR/GCM/CMAC/CCM
  - Encryption key length: 128/256 bits
- True Random Number Generator (TRNG)

System and Power Management

- Low power modes
- Event Link Controller (ELC)
- Data Transfer Controller (DTC)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings
- Low Voltage Detection for EXLVDVBAT pin (select interrupt from 7 levels)
- Low Voltage Detection for VRTC pin (select interrupt from 4 levels)
- Low Voltage Detection for EXLVD pin (select interrupt from 1 level)
- Independent power supply RTC × 1 (calendar for 99 years, alarm function, and clock correction function)
- On-chip RTC power-on-reset (RTCPOR) circuit for VRTC power supply

Multiple Clock Sources

- Main clock oscillator (MOSC) (1 to 20 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (24/32/48/64 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- IWDT-dedicated on-chip oscillator (15 kHz)
- PLL clock for SDADC24
- Clock out support

Up to 77 Pins for General I/O Ports, Including 3 Pins Input Only and 1 Pin Output Only

- 5-V tolerance, open drain, input pull-up

Operating Voltage

- VCC: 1.6 to 5.5 V

Operating Temperature and Packages

- Ta = -40°C to +105°C
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
  - 80-pin LQFP (12 mm × 12 mm, 0.5 mm pitch)
  - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability.

The MCU in this series incorporates an energy-efficient Arm Cortex®-M23 32-bit core, that is particularly well suited for cost-sensitive and low-power applications, with the following features:

- Up to 512-KB (256 KB × 2 banks) code flash memory
- 48-KB SRAM
- Memory Mirror Function (MMF)
- 12-bit A/D Converter (ADC12)
- 24-bit Sigma-Delta A/D Converter (SDADC24)
- Segment LCD Controller/driver
- Independent power supply RTC
- On-chip 32-bit multiplier and multiply-accumulator
- Security features

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M23 core	• Maximum operating frequency: up to 48 MHz • Arm Cortex-M23 core: – Revision: r1p0-00rel0 – Armv8-M architecture profile – Single-cycle integer multiplier – 19-cycle integer divider • Arm Memory Protection Unit (Arm MPU): – Armv8 Protected Memory System Architecture – 8 protect regions • SysTick timer: – Driven by SYSTICCLK (LOCO) or ICLK

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 512 KB (512 KB in 2 banks) of code flash memory.
Data flash memory	8 KB of data flash memory.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset.
Memory Mirror Function (MMF)	The Memory Mirror Function (MMF) can be configured to mirror the desired application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC).

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: • Single-chip mode • SCI boot mode
Resets	The MCU provides 14 resets.

Table 1.3 System (2 of 2)

Feature	Functional description
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin, EXLVDVBAT pin, VRTC pin, and EXLVD pin, and the detection level can be selected using a software program. The LVD module consists of six separate voltage level detectors (LVD0, LVD1, LVD2, LVD_VBAT, LVD_VRTC, and EXLVD). LVD0, LVD1, and LVD2 measure the voltage level input to the VCC pin. LVD_VBAT measures the voltage level input to the EXLVDVBAT pin. LVD_VRTC measures the voltage level input to the VRTC pin. EXLVD measures the voltage level input to the EXLVD pin. LVD registers allow your application to configure detection of VCC, Battery Backup Power Supply, and VRTC changes at various voltage thresholds.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • IWDT-dedicated on-chip oscillator (IWDTLOCO) • 12.0 MHz/12.8 MHz PLL clock for Sigma-Delta A/D Multiplied from 32.768 kHz • Clock out support
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.
Low power modes	Power consumption can be reduced in multiple ways, including setting clock dividers, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes.
Register write protection	The register write protection function protects important registers from being overwritten due to software errors. The registers to be protected are set with the Protect Register (PRCR).
Memory Protection Unit (MPU)	The MCU has four Memory Protection Units (MPUs) and a CPU stack pointer monitor function is provided.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt or watchdog timer reset.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request.

Table 1.6 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 16-bit timer with GPT16 × 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer.
Port Output Enable for GPT (POEG)	The Port Output Enable (POEG) function can place the General PWM Timer (GPT) output pins in the output disable state
Low Power Asynchronous General Purpose Timer (AGT)	The Low Power Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.
Low Power Asynchronous General Purpose Timer (AGTW)	The Low Power Asynchronous General Purpose Timer (AGTW) is a 32-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events. This timer consists of a reload register and a down counter. The reload register and the down counter are allocated to the same address, and can be accessed with the AGT register.
Realtime Clock (RTC)	The realtime clock (RTC) has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.

Table 1.7 Communication interfaces

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) × 5 channels have asynchronous and synchronous serial interfaces: ● Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) ● 8-bit clock synchronous interface ● Simple IIC (master-only) ● Simple SPI ● Smart card interface The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCIn (n = 0) has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.
I^2C bus interface (IIC)	The I^2C bus interface (IIC) has 2 channels. The IIC module conforms with and provides a subset of the NXP I^2C (Inter-Integrated Circuit) bus interface functions.
Serial Peripheral Interface (SPI)	The Serial Peripheral Interface (SPI) has one channel. The SPI provides high-speed full-duplex synchronous serial communications with multiple processors and peripheral devices.

Table 1.8 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	A 12-bit successive approximation A/D converter is provided. Up to 4 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion.
24-bit Sigma-Delta A/D Converter (SDADC24)	A 24-bit Sigma-Delta A/D Converter (SDADC24) with a programmable gain amplifier is provided. Up to 7 differential or single-ended analog input channels are selectable. Analog input is input to the sigma-delta A/D converter by the programmable gain amplifier (PGA). The A/D conversion result is passed through the phase adjustment circuit, the digital filter, and the high-pass filter, and then stored into the conversion result registers. Each time conversion is completed, the interrupt request signal is generated to notify the CPU that the conversion result can be read.
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can be further used by the end application.

Table 1.9 Human machine interfaces

Feature	Functional description
Segment LCD Controller/Driver (SLCDC)	The SLCDC provides the following functions: ● Internal voltage boosting method, capacitor split method, and external resistance division method are switchable ● VL1 or VL2 reference mode is selectable under internal voltage boosting method ● VCC or VL4 reference mode is selectable under capacitor split method ● Segment signal output: 21 (17) to 45 (41) ● Common signal output: 4 (8) ● Waveform A or B selectable ● The LCD can be made to blink Note: The values in parentheses are the number of signal outputs when 8 com is used.

Table 1.10 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC)	The Cyclic Redundancy Check (CRC) generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generation polynomials are available. The snoop function allows to monitor the access to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated.
32-bit Multiply-accumulator (MACL)	The 32-bit multiply-accumulator has the following functions: ● 32 bits × 32 bits = 64 bits (unsigned or signed) ● 32 bits × 32 bits + 64 bits = 64 bits (unsigned or signed) Cumulative values of product operation can be retained by 24 channel buffers and can be read out with independent address.

Table 1.11 I/O ports

Feature	Functional description
I/O ports	● I/O ports for the 100-pin, 7-channel LQFP – I/O pins: 67 – Input pins: 3 – Output pins: 1 – Pull-up resistors: 64 – N-ch open-drain outputs: 58 – 5-V tolerance: 2 – 5-V tolerance/RTCICn (n = 0 to 2): 3 ● I/O ports for the 100-pin, 4-channel LQFP – I/O pins: 73 – Input pins: 3 – Output pins: 1 – Pull-up resistors: 70 – N-ch open-drain outputs: 64 – 5-V tolerance: 2 – 5-V tolerance/RTCICn (n = 0 to 2): 3 ● I/O ports for the 80-pin LQFP – I/O pins: 55 – Input pins: 3 – Output pins: 1 – Pull-up resistors: 52 – N-ch open-drain outputs: 46 – 5-V tolerance: 2 – 5-V tolerance/RTCICn (n = 0 to 2): 3 ● I/O ports for the 64-pin LQFP – I/O pins: 39 – Input pins: 3 – Output pins: 1 – Pull-up resistors: 37 – N-ch open-drain outputs: 33 – 5-V tolerance: 2 – 5-V tolerance/RTCICn (n = 1 to 2): 2

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

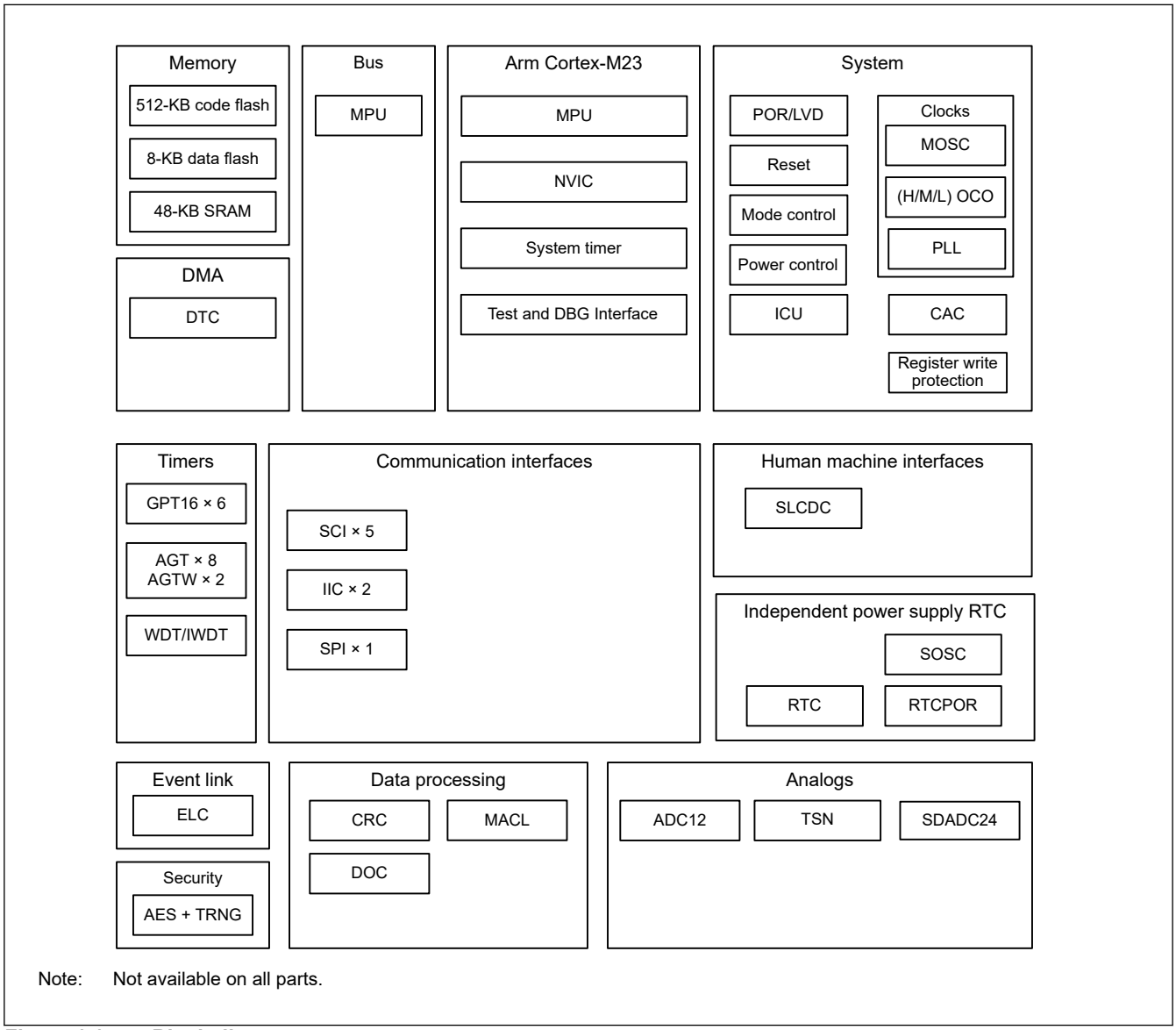
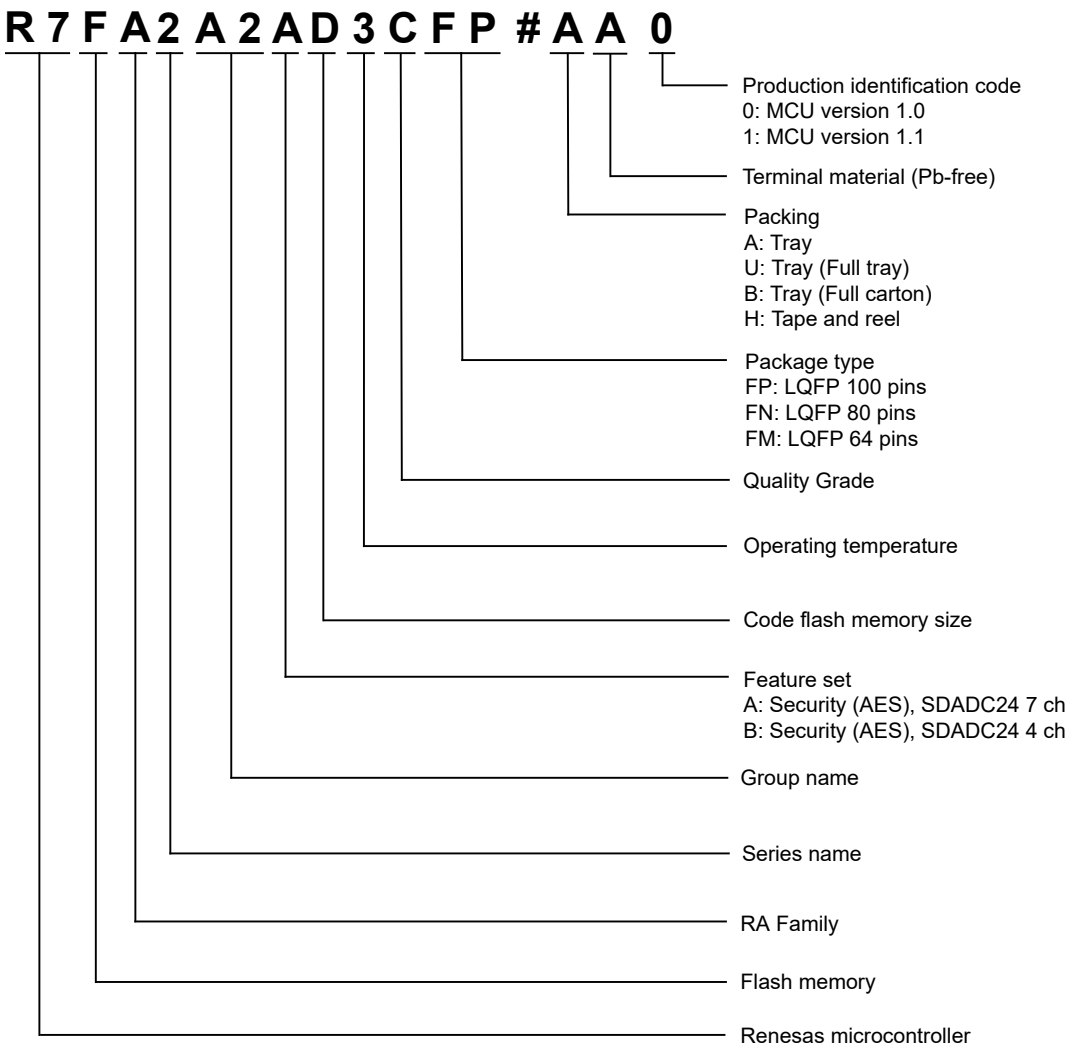


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows the product part number information, including memory capacity and package type. Table 1.12 shows a list of products.



Note: Check the order screen for each product on the Renesas website for valid symbols after the #.

Figure 1.2 Part numbering scheme

Table 1.12 Product list

Product part number	Package code	SDADC24	Code flash	Data flash	SRAM	Operating temperature
R7FA2A2AD3CFP	PLQP0100KB-B	7 ch	512 KB	8 KB	48 KB	-40 to +105°C
R7FA2A2BD3CFP	PLQP0100KB-B	4 ch				
R7FA2A2BD3CFN	PLQP0080KB-B					
R7FA2A2BD3CFM	PLQP0064KB-C					

1.4 Function Comparison

Table 1.13 Function comparison

Parts number		R7FA2A2AD3CFP	R7FA2A2BD3CFP	R7FA2A2BD3CFN	R7FA2A2BD3CFM
Pin count		100		80	64
Package		LQFP			
Code flash memory		512 KB			
Data flash memory		8 KB			
SRAM		48 KB			
	Parity	32 KB			
	ECC	16 KB			
System	CPU clock	48 MHz			
	Sub-clock oscillator	Yes			
	PLL	Yes			
	ICU	Yes			
Event control	ELC	Yes			
DMA	DTC	Yes			
Timers	GPT16	6			5
	AGT	8			
	AGTW	2			
	RTC	Yes			
	WDT/IWDT	Yes			
Communication	SCI	5			4
	IIC	2			1
	SPI	1			
Analog	ADC12	4			2
	SDADC24	7 ch	4 ch		
	TSN	Yes			
HMI	SLCDC	39 seg × 4 com 35 seg × 8 com	45 seg × 4 com 41 seg × 8 com	32 seg × 4 com 28 seg × 8 com	21 seg × 4 com 17 seg × 8 com
Data processing	CRC	Yes			
	MACL	Yes (24 ch buffer readable with independent address)			
	DOC	Yes			
Security		AES and TRNG			
I/O ports	I/O pins	67	73	55	39
	Input pins	3	3	3	3
	Output pins	1	1	1	1
	Pull-up resistors	64	70	52	37
	N-ch open-drain outputs	58	64	46	32
	5-V tolerance	2	2	2	2
	5-V tolerance/ RTCICn (n = 0 to 2)	3	3	3	2

1.5 Pin Functions

Table 1.14 Pin functions (1 of 3)

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1-μF capacitor. Place the capacitor close to the pin.
	VCL	I/O	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VRTC	Input	Independent Power Supply for Sub-clock oscillator (XCIN, XCOUT) and RTC (RTCIC0-RTCIC2)
Voltage detector	EXLVD	Input	Low voltage detector for external pin
	EXLVDVBAT	Input	Low Voltage detector for battery backup
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
On-chip debug	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ11	Input	Maskable interrupt request pins
GPT	GTETRGA, GTETRGB	Input	External trigger input pins
	GTIOCnA (n = 4 to 9), GTIOCnB (n = 4 to 9)	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEEn (n = 0 to 7)	Input	External event input enable signals
	AGTIOn (n = 0 to 7)	I/O	External event input and pulse output pins
	AGTOn (n = 0 to 7)	Output	Pulse output pins
	AGTOAn (n = 0 to 7)	Output	Output compare match A output pins
	AGTOBn (n = 0 to 7)	Output	Output compare match B output pins

Table 1.14 Pin functions (2 of 3)

Function	Signal	I/O	Description
AGTW	AGTWEEn (n = 0 to 1)	Input	External event input enable signals
	AGTWIOn (n = 0 to 1)	I/O	External event input and pulse output pins
	AGTWOn (n = 0 to 1)	Output	Pulse output pins
	AGTWOAn (n = 0 to 1)	Output	Output compare match A output pins
	AGTWOBn (n = 0 to 1)	Output	Output compare match B output pins
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCICn (n = 0 to 2)	Input	RTC time capture event input
SCI	SCKn (n = 0 to 3, 9)	I/O	Input/output pins for the clock (clock synchronous mode)
	RXDn (n = 0 to 3, 9)	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXDn (n = 0 to 3, 9)	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTSn_RTSn (n = 0 to 3, 9)	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low.
	SCLn (n = 0 to 3, 9)	I/O	Input/output pins for the IIC clock (simple IIC mode)
	SDAn (n = 0 to 3, 9)	I/O	Input/output pins for the IIC data (simple IIC mode)
	SCKn (n = 0 to 3, 9)	I/O	Input/output pins for the clock (simple SPI mode)
	MISOn (n = 0 to 3, 9)	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSIn (n = 0 to 3, 9)	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SSn (n = 0 to 3, 9)	Input	Chip-select input pins (simple SPI mode), active-low
IIC	SCLn (n = 0, 1)	I/O	Input/output pins for the clock
	SDAn (n = 0, 1)	I/O	Input/output pins for data
SPI	RSPCKA	I/O	Clock input/output pin
	MOSIA	I/O	Input or output pins for data output from the master
	MISOA	I/O	Input or output pins for data output from the slave
	SSLA0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3	Output	Output pins for slave selection
Analog power supply	AVCC	Input	Analog voltage supply pin for the ADC12, SDADC24, TSN
	AVSS	Input	Analog ground pin for the ADC12, SDADC24, TSN
	AVCM	Input	Common mode voltage for 24-bit Sigma-Delta A/D converter
	AREGC	I/O	Regulator capacitance for 24-bit Sigma-Delta A/D converter
	AVRT	Output	Reference voltage for 24-bit Sigma-Delta A/D converter
	VREFH0	Input	Analog reference voltage supply pin for the ADC12. Connect this pin to AVCC when not using the ADC12.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to AVSS when not using the ADC12.
ADC12	AN000 to AN003	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0	Input	Input pin for the external trigger signals that start the A/D conversion, active-low.
SDADC24	ANIN0 to ANIN6	Input	24-bit Sigma-Delta A/D converter analog input. These are the negative input pins. (Differential/Single-end)
	ANIP0 to ANIP6	Input	24-bit Sigma-Delta A/D converter analog input. These are the positive input pins. (Differential/Single-end)

Table 1.14 Pin functions (3 of 3)

Function	Signal	I/O	Description
LCD	VL1 to VL4	I/O	Voltage for Driving LCD
	CAPH, CAPL	I/O	Capacitor Connection for Segment LCD Controller/Driver
	COM0 to COM7	Output	Segment LCD controller/driver common signal outputs
	SEG0 to SEG44	Output	Segment LCD controller/driver segment signal outputs
I/O ports	P001, P002, P004 to P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201, P203 to P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300 to P313	I/O	General-purpose input/output pins
	P400 to P405, P408 to p411	I/O	General-purpose input/output pins
	P500 to P506	I/O	General-purpose input/output pins
	P600	Output	General-purpose output pin

1.6 Pin Assignments

Figure 1.3 to Figure 1.6 show the pin assignments from the top view.

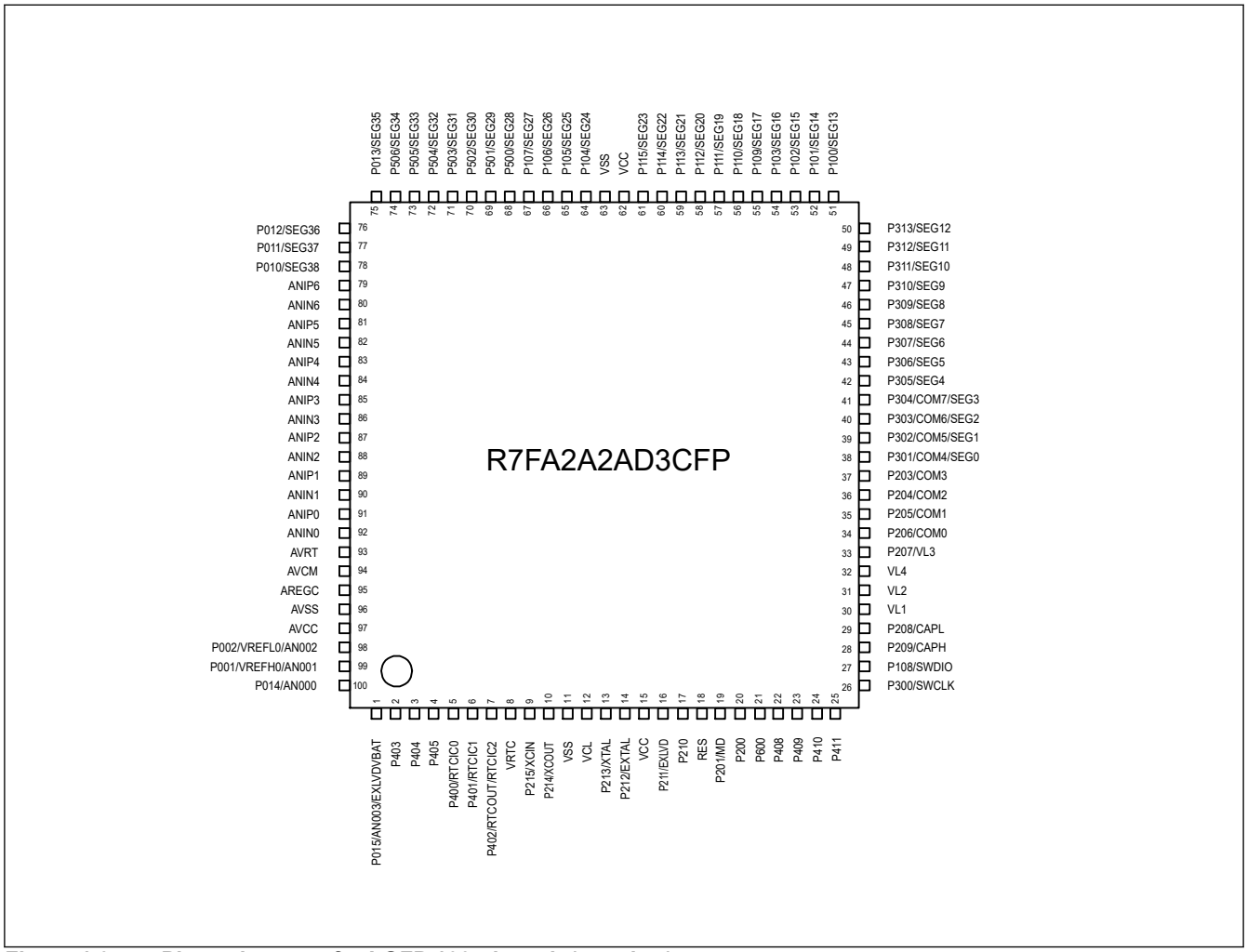


Figure 1.3 Pin assignment for LQFP 100-pin 7 ch (top view)

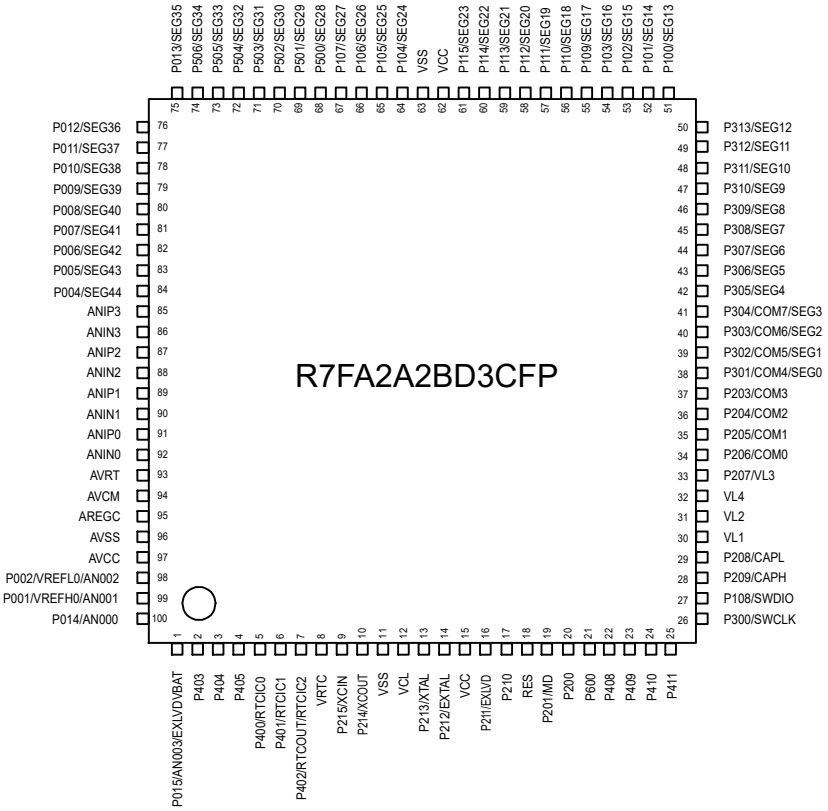


Figure 1.4 Pin assignment for LQFP 100-pin 4 ch (top view)

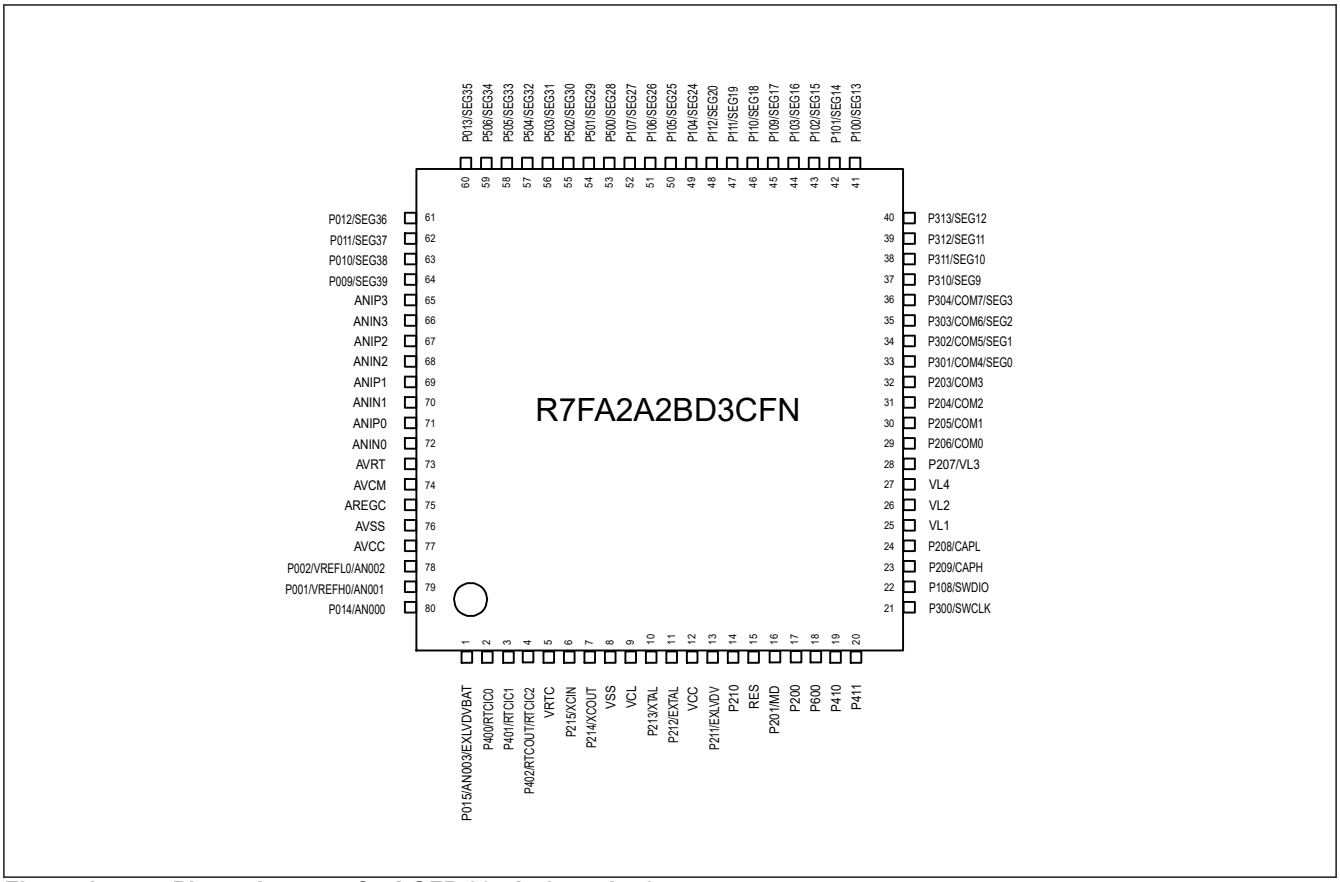


Figure 1.5 Pin assignment for LQFP 80-pin (top view)

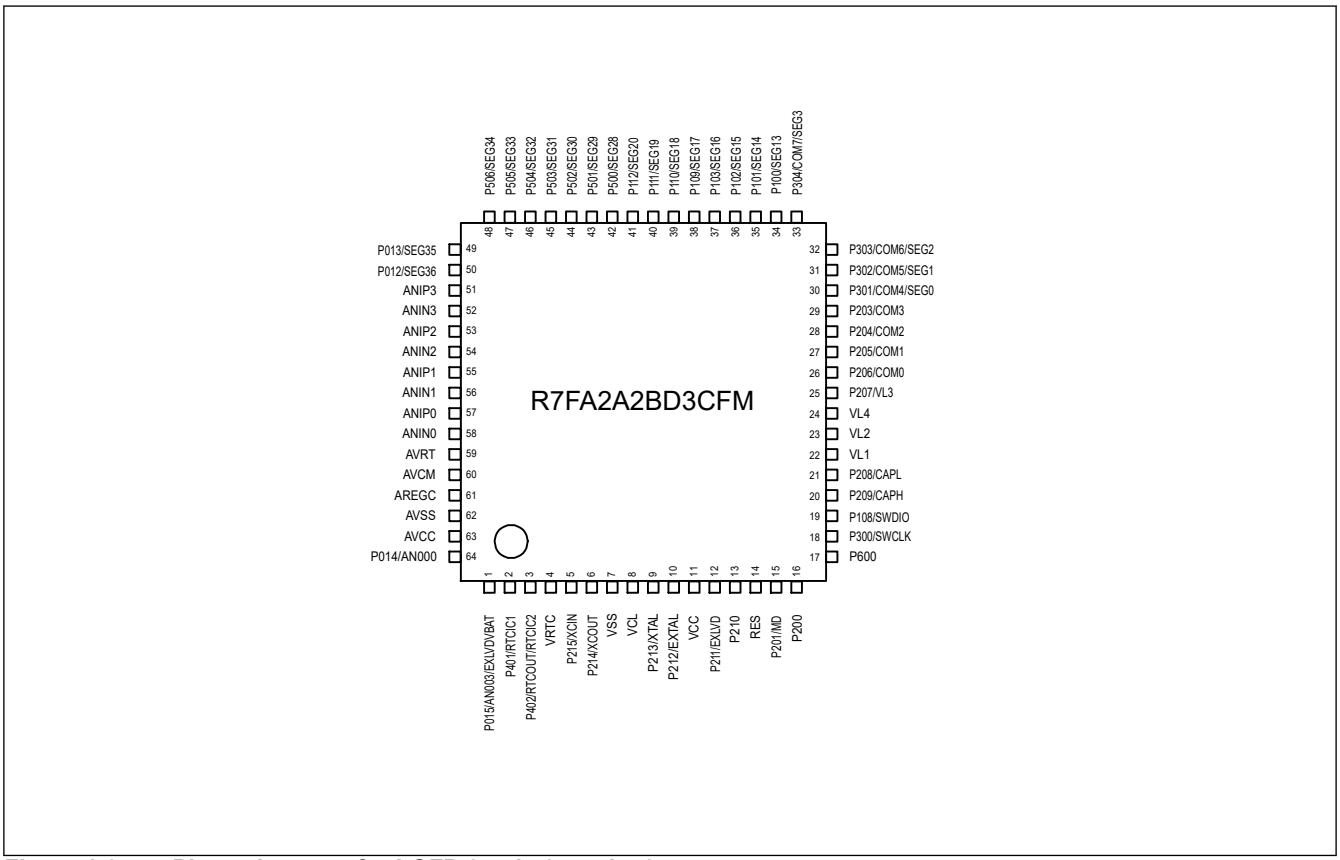


Figure 1.6 Pin assignment for LQFP 64-pin (top view)

1.7 Pin Lists

Table 1.15 Pin list (1 of 4)

Num.						Timers					Communication interfaces			Analogs		HMI	
LQFP100 (7ch)	LQFP100 (4ch)	LQFP80	LQFP64	Power, System, Clock, Debug, CAC	I/O ports	AGTW	AGT	GPT_OPS, POEG	GPT	RTC	SCI	IIC	SPI	12-bit ADC	24-bit SDADC	Segment LCDC	Interrupt
1	1	1	1	EXLVDVBAT	P015	—	—	—	—	—	—	—	—	AN003	—	—	—
2	2	—	—	—	P403	—	—	—	GTIOC4B	—	—	—	MISOA_B	—	—	—	—
3	3	—	—	—	P404	—	—	—	—	—	—	—	MOSIA_B	—	—	—	—
4	4	—	—	—	P405	—	—	—	—	—	—	—	RSPCKA_B	—	—	—	—
5	5	2	—	—	P400	—	—	—	—	RTCIC0	—	—	—	—	—	—	IRQ9
6	6	3	2	—	P401	—	—	—	—	RTCIC1	—	—	—	—	—	—	IRQ10
7	7	4	3	—	P402	—	—	—	—	RTCIC2/RTCOUT_A	—	—	—	—	—	—	IRQ11
8	8	5	4	VRTC	—	—	—	—	—	—	—	—	—	—	—	—	—
9	9	6	5	XCIN	P215	—	—	—	—	—	—	—	—	—	—	—	—
10	10	7	6	XCOUT	P214	—	—	—	—	—	—	—	—	—	—	—	—
11	11	8	7	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—
12	12	9	8	VCL	—	—	—	—	—	—	—	—	—	—	—	—	—
13	13	10	9	XTAL	P213	—	—	—	—	—	—	—	—	—	—	—	—
14	14	11	10	EXTAL	P212	—	—	—	—	—	—	—	—	—	—	—	—
15	15	12	11	VCC	—	—	—	—	—	—	—	—	—	—	—	—	—
16	16	13	12	EXLVD	P211	—	—	—	—	—	—	—	—	—	—	—	—
17	17	14	13	CLKOUT_A	P210	—	—	—	GTIOC5B_A	—	—	—	—	ADTRG0_B	—	—	IRQ8
18	18	15	14	RES	—	—	—	—	—	—	—	—	—	—	—	—	—
19	19	16	15	MD	P201	—	—	—	—	—	—	—	—	—	—	—	—
20	20	17	16	—	P200	—	—	—	—	—	—	—	—	—	—	—	NMI
21	21	18	17	—	P600	—	—	—	—	—	—	—	—	—	—	—	—
22	22	—	—	—	P408	—	—	—	GTIOC9A_B	—	—	—	SSLA0_B	—	—	—	—
23	23	—	—	—	P409	—	—	—	GTIOC9B_B	—	—	—	SSLA1_B	—	—	—	—
24	24	19	—	—	P410	—	—	—	GTIOC6A_A	—	—	SDA0	—	—	—	—	—
25	25	20	—	—	P411	—	—	—	GTIOC7A	—	—	SCL0	—	—	—	—	—
26	26	21	18	SWCLK	P300	—	—	—	GTIOC6B_A	—	—	—	—	—	—	—	—
27	27	22	19	SWDIO	P108	—	—	—	GTIOC7B	RTCOUT_B	—	—	—	—	—	—	—
28	28	23	20	—	P209	—	—	—	—	—	—	—	—	—	—	CAPH	—

Table 1.15 Pin list (2 of 4)

Num.				Power, System, Clock, Debug, CAC	I/O ports	Timers					Communication interfaces			Analogs		HMI	
LQFP100 (7ch)	LQFP100 (4ch)	LQFP80	LQFP64			AGTW	AGT	GPT_OPS, POEG	GPT	RTC	SCI	IIC	SPI	12-bit ADC	24-bit SDADC	Segment LCDC	Interrupt
29	29	24	21	—	P208	—	—	—	—	—	—	—	—	—	—	CAPL	—
30	30	25	22	—	—	—	—	—	—	—	—	—	—	—	—	VL1	—
31	31	26	23	—	—	—	—	—	—	—	—	—	—	—	—	VL2	—
32	32	27	24	—	—	—	—	—	—	—	—	—	—	—	—	VL4	—
33	33	28	25	—	P207	—	—	—	—	—	—	—	—	—	—	VL3	—
34	34	29	26	—	P206	—	—	—	—	—	—	—	—	—	—	COM0	—
35	35	30	27	—	P205	—	—	—	—	—	—	—	—	—	—	COM1	—
36	36	31	28		P204	—	—	—	—	—	—	—	—	—	—	COM2	—
37	37	32	29		P203	—	—	—	—	—	—	—	—	—	—	COM3	—
38	38	33	30	—	P301	—	—	—	—	—	—	—	—	—	—	COM4/ SEG0	—
39	39	34	31	—	P302	—	—	—	—	—	—	—	—	—	—	COM5/ SEG1	—
40	40	35	32	—	P303	—	—	—	—	—	—	—	—	—	—	COM6/ SEG2	—
41	41	36	33	—	P304	—	—	—	—	—	—	—	—	—	—	COM7/ SEG3	—
42	42	—	—	—	P305	—	—	—	—	—	—	—	—	—	—	SEG4	—
43	43	—	—	—	P306	—	—	—	—	—	—	—	—	—	—	SEG5	IRQ0_B
44	44	—	—	—	P307	—	—	—	—	—	—	—	—	—	—	SEG6	IRQ1_B
45	45	—	—	—	P308	—	—	—	—	—	—	—	—	—	—	SEG7	IRQ2_B
46	46	—	—	—	P309	—	—	—	—	—	—	—	—	—	—	SEG8	IRQ3_B
47	47	37	—	—	P310	—	—	—	—	—	—	—	—	—	—	SEG9	IRQ4_B
48	48	38	—	—	P311	—	—	—	—	—	—	—	—	—	—	SEG10	IRQ5_B
49	49	39	—	—	P312	—	—	—	—	—	—	—	—	—	—	SEG11	IRQ6_B
50	50	40	—	—	P313	—	—	—	—	—	—	—	—	—	—	SEG12	IRQ7_B
51	51	41	34	—	P100	—	AGTO0/ AGTOA0/ AGTOB0/ AGTEE0	GTIU	GTIOC8A_A	—	TXD0/ MOSI0/ SDA0	—	—	—	—	SEG13	—
52	52	42	35	—	P101	AGTWO0	AGTO1/ AGTOA1/ AGTOB1/ AGTEE1	GTIV	GTIOC8B_A	—	RXD0/ MISO0/ SCL0	—	—	—	—	SEG14	—
53	53	43	36	—	P102	AGTWEE0	AGTO2/ AGTOA2/ AGTOB2/ AGTEE2	GTIW	GTIOC6A_B	—	SCK0	—	—	ADTRG0_A	—	SEG15	—
54	54	44	37	—	P103	AGTWIO0	AGTO3/ AGTOA3/ AGTOB3/ AGTEE3	GTOUUP	GTIOC6B_B	—	CTS0_RTS0/SS0	—	SSLA3	—	—	SEG16	—

Table 1.15 Pin list (3 of 4)

Num.				Power, System, Clock, Debug, CAC	I/O ports	Timers					Communication interfaces			Analogs		HMI	
LQFP100 (7ch)	LQFP100 (4ch)	LQFP80	LQFP64			AGTW	AGT	GPT_OPS, POEG	GPT	RTC	SCI	IIC	SPI	12-bit ADC	24-bit SDADC	Segment LCDC	Interrupt
55	55	45	38	CLKOUT_B	P109	AGTWOB0	AGTO4/ AGTOA4/ AGTOB4/ AGTEE4	GTOULO	—	—	TXD9/ MOSI9/ SDA9	—	—	—	—	SEG17*1	—
56	56	46	39	—	P110	AGTWOA0	AGTO5/ AGTOA5/ AGTOB5/ AGTEE5	GTOVUP	—	—	RXD9/ MISO9/ SCL9	—	—	—	—	SEG18	—
57	57	47	40	—	P111	—	AGTO6/ AGTOA6/ AGTOB6/ AGTEE6	GTOVLO	GTIOC5A_B	—	SCK9	—	—	—	—	SEG19	—
58	58	48	41	—	P112	—	AGTO7/ AGTOA7/ AGTOB7/ AGTEE7	GTOWUP	GTIOC5B_B	—	CTS9_RTS9/SS9	—	SSLA2	—	—	SEG20	—
59	59	—	—	—	P113	—	—	—	—	—	—	—	—	—	—	SEG21	—
60	60	—	—	—	P114	—	—	—	—	—	—	—	—	—	—	SEG22	—
61	61	—	—	—	P115	—	—	—	—	—	—	—	—	—	—	SEG23	—
62	62	—	—	VCC	—	—	—	—	—	—	—	—	—	—	—	—	—
63	63	—	—	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—
64	64	49	—	—	P104	—	—	—	GTIOC8A_B	—	SCK2	—	—	—	—	SEG24	—
65	65	50	—	—	P105	—	—	—	GTIOC8B_B	—	CTS2_RTS2/SS2	—	—	—	—	SEG25	—
66	66	51	—	—	P106	—	—	—	—	—	TXD2/ MOSI2/ SDA2	—	—	—	—	SEG26	—
67	67	52	—	—	P107	—	—	—	—	—	RXD2/ MISO2/ SCL2	—	SSLA1_A	—	—	SEG27	—
68	68	53	42	—	P500	AGTWEE1	AGTIO0	GTOWLO	—	—	RXD3/ MISO3/ SCL3	—	—	—	—	SEG28	IRQ4_A
69	69	54	43	—	P501	AGTWIO1	AGTIO1	GTETRGA	—	—	TXD3/ MOSI3/ SDA3	—	—	—	—	SEG29	IRQ5_A
70	70	55	44	—	P502	AGTWO1	AGTIO2	GTETRGB	GTIOC9A_A	—	SCK3	—	RSPCKA_A	—	—	SEG30	IRQ6_A
71	71	56	45	—	P503	AGTWOA1	AGTIO3	—	GTIOC9B_A	—	CTS3_RTS3/SS3	—	SSLA0_A	—	—	SEG31	IRQ7_A
72	72	57	46	—	P504	AGTWOB1	AGTIO4	—	—	—	SCK1	—	MOSIA_A	—	—	SEG32	—
73	73	58	47	—	P505	—	AGTIO5	—	—	—	CTS1_RTS1/SS1	—	MISOA_A	—	—	SEG33	—
74	74	59	48	—	P506	—	AGTIO6	—	—	—	TXD1/ MOSI1/ SDA1	—	—	—	—	SEG34	IRQ0_A
75	75	60	49	—	P013	—	AGTIO7	—	—	—	RXD1/ MISO1/ SCL1	SDA1	—	—	—	SEG35	IRQ1_A
76	76	61	50	CACREF_A	P012	—	—	—	GTIOC5A_A	—	—	SCL1	—	—	—	SEG36	IRQ2_A

Table 1.15 Pin list (4 of 4)

Num.						Timers					Communication interfaces			Analogs		HMI	
LQFP100 (7ch)	LQFP100 (4ch)	LQFP80	LQFP64	Power, System, Clock, Debug, CAC	I/O ports	AGTW	AGT	GPT_OPS, POEG	GPT	RTC	SCI	IIC	SPI	12-bit ADC	24-bit SDADC	Segment LCDC	Interrupt
77	77	62	—	—	P011	—	—	—	GTIOC4A	—	—	—	—	—	—	SEG37	—
78	78	63	—	—	P010	—	—	—	—	—	—	—	—	—	—	SEG38	—
—	79	64	—	—	P009	—	—	—	—	—	—	—	—	—	—	SEG39	—
—	80	—	—	—	P008	—	—	—	—	—	—	—	—	—	—	SEG40	—
—	81	—	—	—	P007	—	—	—	—	—	—	—	—	—	—	SEG41	—
—	82	—	—	—	P006	—	—	—	—	—	—	—	—	—	—	SEG42	—
—	83	—	—	—	P005	—	—	—	—	—	—	—	—	—	—	SEG43	—
—	84	—	—	—	P004	—	—	—	—	—	—	—	—	—	—	SEG44	—
79	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANIP6	—	—
80	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANIN6	—	—
81	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANIP5	—	—
82	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANIN5	—	—
83	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANIP4	—	—
84	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANIN4	—	—
85	85	65	51	—	—	—	—	—	—	—	—	—	—	—	ANIP3	—	—
86	86	66	52	—	—	—	—	—	—	—	—	—	—	—	ANIN3	—	—
87	87	67	53	—	—	—	—	—	—	—	—	—	—	—	ANIP2	—	—
88	88	68	54	—	—	—	—	—	—	—	—	—	—	—	ANIN2	—	—
89	89	69	55	—	—	—	—	—	—	—	—	—	—	—	ANIP1	—	—
90	90	70	56	—	—	—	—	—	—	—	—	—	—	—	ANIN1	—	—
91	91	71	57	—	—	—	—	—	—	—	—	—	—	—	ANIP0	—	—
92	92	72	58	—	—	—	—	—	—	—	—	—	—	—	ANIN0	—	—
93	93	73	59	—	—	—	—	—	—	—	—	—	—	—	AVRT	—	—
94	94	74	60	—	—	—	—	—	—	—	—	—	—	—	AVCM	—	—
95	95	75	61	—	—	—	—	—	—	—	—	—	—	—	AREGC	—	—
96	96	76	62	AVSS	—	—	—	—	—	—	—	—	—	—	—	—	—
97	97	77	63	AVCC	—	—	—	—	—	—	—	—	—	—	—	—	—
98	98	78	—	—	P002	—	—	—	—	—	—	—	—	VREFL0/AN002	—	—	—
99	99	79	—	—	P001	—	—	—	—	—	—	—	—	VREFH0/AN001	—	—	—
100	100	80	64	CACREF_B	P014	—	—	—	—	—	—	—	—	AN000	—	—	IRQ3_A

Note: Several pin names have the added suffix of _A and _B. The suffix can be ignored when assigning functionality.

Note 1. MCU Version 1.0 has the following restriction. The restriction is not required for MCU Version 1.1.
When using SEG17 with the internal voltage boost method, stop the voltage boosting circuit operation when the VCC voltage is lower than the LCD drive voltage V_{L4} (V_{L4} > VCC).

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC[*1] = AVCC = 1.6 to 5.5 V, VRTC = 1.6 to 5.5 V, VREFH0 = 1.6 V to VCC

VSS = AVSS = VREFL0 = 0 V, Ta = T_{opr}

Note 1. The typical condition is set to VCC = 3.3 V.

Figure 2.1 shows the timing conditions.

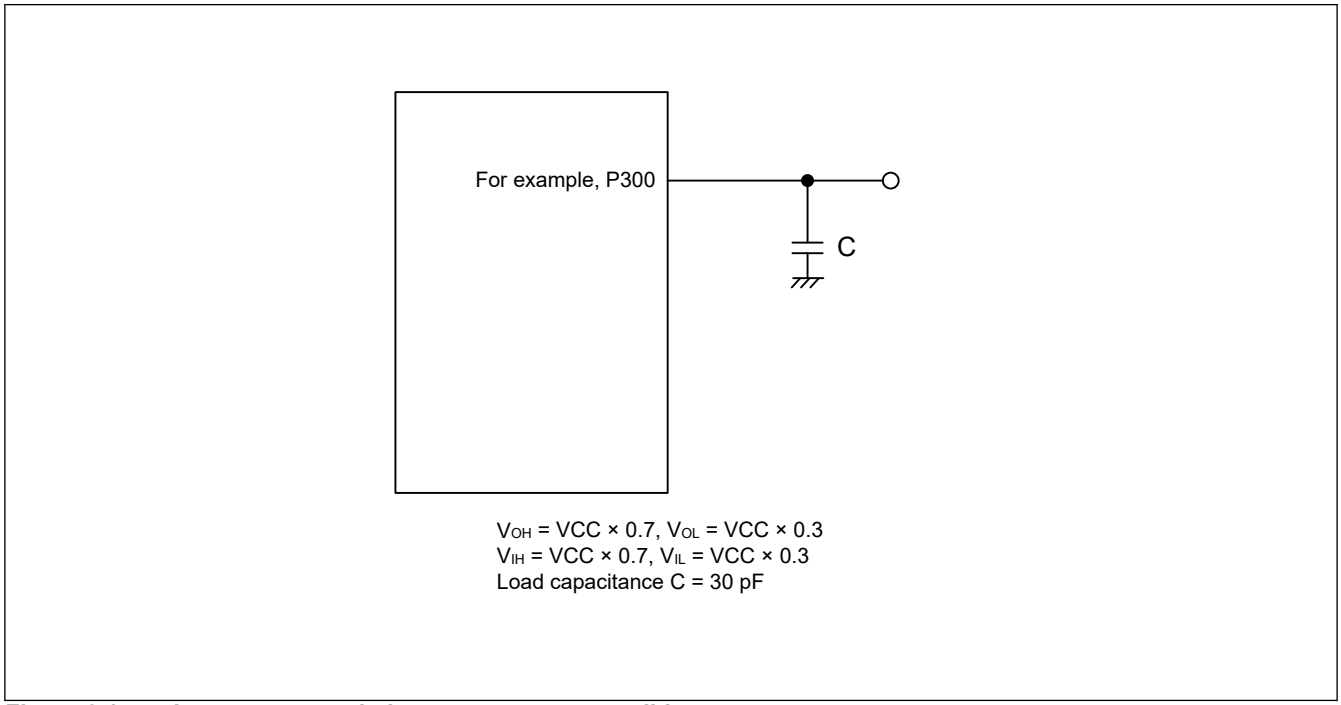


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of the timing specifications for each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities for each pin to meet the conditions of your system.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC characteristics of each function are not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
RTC power supply voltage		VRTC	-0.5 to +6.5	V
Input voltage	5V-tolerant ports[*1]	V_{in}	-0.3 to +6.5	V
	P400 to P402 (N-ch open-drain)	V_{in}	-0.3 to +6.5	V
	P001, P002, P014 to P015	V_{in}	-0.3 to AVCC + 0.3	V
	P214, P215	V_{in}	-0.3 to V_{RTC} + 0.3 [*5]	V
	Others	V_{in}	-0.3 to VCC + 0.3	V
Reference power supply voltage		VREFH0	-0.3 to +6.5	V
	AREGC, AVCM, AVRT	V_{ISDAD}	-0.3 to +2.1[*6]	V
Analog power supply voltage		AVCC	-0.5 to +6.5	V

Table 2.1 Absolute maximum ratings (2 of 2)

Parameter			Symbol	Value	Unit
Analog input voltage	When AN000 to AN003 are used		V_{AN}	-0.3 to AVCC + 0.3	V
	When ANINn and ANIPn (n = 0 to 6) are used			-0.6 to AVCC + 0.3*7	V
LCD voltage	VL1 voltage		V_{L1}	-0.3 to +2.1 and -0.3 to V_{L4} + 0.3	V
	VL2 voltage		V_{L2}	-0.3 to +6.5	V
	VL3 voltage		V_{L3}	-0.3 to +6.5	V
	VL4 voltage		V_{L4}	-0.3 to +6.5	V
	CAPL, CAPH voltage *8		V_{LCAP}	-0.3 to VL4 + 0.3*5	V
	COM0 to COM7, SEG0 to SEG44, output voltage	External resistance division method	V_{OUT}	-0.3 to VCC + 0.3*5	V
		Capacitor split method (VCC reference)		-0.3 to VCC + 0.3*5	V
		Capacitor split method (V_{L4} reference)		-0.3 to VL4 + 0.3*5	V
		Internal voltage boosting method (V_{L1} reference)		-0.3 to VL4 + 0.3*5	V
		Internal voltage boosting method (V_{L2} reference)		-0.3 to VL4 + 0.3*5	V
Operating temperature*2 *3 *4			T_{opr}	-40 to +105	°C
Storage temperature			T_{stg}	-55 to +125	°C

Note 1. Ports P410 and P411 are 5V-tolerant.
When the ports are used as the IIC function, there is no problem even if the input pull-up power supply while the device is not powered. However, the current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.
Note 2. See section 2.2.1. Tj/Ta Definition.
Note 3. Contact Renesas Electronics sales office for information on derating operation under Ta = +105°C.
Derating is the systematic reduction of load for improved reliability.
Note 4. The upper limit of the operating temperature is 105°C, depending on the product.
Note 5. Must be 6.5 V or lower.
Note 6. This value defines the absolute maximum rating of AREGC, AVCM, and AVRT terminal. Do not use with voltage applied.
Note 7. The SDADC24 conversion target pin must not exceed AREGC +0.3 V.
Note 8. When using the internal voltage boosting method or capacitance split method, connect these VL1 to VL4 pins to VSS with a capacitor (0.47 µF ± 30%), and connect a capacitor (0.47 µF ± 30%) between the CAPL and CAPH pins.

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC and AVSS pins, and between the VREFH0 and VREFL0 pins when VREFH0 is selected as the high potential reference voltage for the ADC12. Place capacitors of the following value as close as possible to every power supply pin and use the shortest and heaviest possible traces:

- **VCC and VSS: about 0.1 µF**
- **VRTC and VSS: about 0.1 µF**
- **AVCC and AVSS: about 0.1 µF and 10 µF in parallel**
- **VREFH0 and VREFL0: about 0.1 µF**

Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin by a 4.7 µF capacitor. Each capacitor must be placed close to the pin.

- **VCL and VSS: 4.7 µF**
- **AREGC and AVSS: 0.47 µF**
- **AVCM and AVSS: 0.47 µF**
- **AVRT and AVSS: 0.47 µF**

Table 2.2 Recommended operating conditions

Parameter	Symbol		Min	Typ	Max	Unit
Power supply voltages	VCC*1 *2		1.6	—	5.5	V
	VSS		—	0	—	V
RTC power supply voltage	V_{RTC}		1.6	—	5.5	V
Analog power supply voltages	AVCC*1 *2		1.6	—	5.5	V
	AVSS		—	0	—	V
	VREFH0	When used as ADC12 Reference	1.6	—	AVCC	V
	VREFL0		—	0	—	V

Note 1. Use AVCC and VCC under the following conditions:
AVCC = VCC

Note 2. When powering on the VCC and AVCC pins, power them on at the same time or the VCC pin first and then the AVCC pins.
When powering off the VCC and AVCC pins, power them off at the same time or the AVCC pin first and then the VCC pins.

2.2 DC Characteristics

2.2.1 Tj/Ta Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (Ta) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	Tj	—	125*1	°C	High-speed mode Middle-speed mode Low-speed mode Subosc-speed mode

Note: Make sure that $Tj = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.

Note 1. The upper limit of operating temperature is 105°C, depending on the product. If the part number shows the operation temperature at 105°C, then the maximum value of Tj is 125°C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL}

Conditions: VCC = AVCC = 1.6 to 5.5 V, VRTC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	Input port pins P001, P002, P014, P015		V_{IH}	AVCC × 0.8	—	—	V	—
			V_{IL}	—	—	AVCC × 0.2		
	Input port pins except for P214, P215		V_{IH}	VRTC × 0.8	—	—		
			V_{IL}	—	—	VRTC × 0.2		
	Input port pins except for P001, P002, P014, P015, P214, P215		V_{IH}	VCC × 0.8	—	—		
			V_{IL}	—	—	VCC × 0.2		
	EXTAL		V_{IH}	VCC × 0.8	—	—		
			V_{IL}	—	—	VCC × 0.2		
	5V-tolerant ports*3		V_{IH}	VCC × 0.8	—	5.8		
			V_{IL}	—	—	VCC × 0.2		
	RES, NMI, IRQ*4		V_{IH}	VCC × 0.8	—	—		
			V_{IL}	—	—	VCC × 0.2		
			ΔV_T*6	VCC × 0.10	—	—		VCC = 2.7 V to 5.5 V
				VCC × 0.05	—	—		VCC = 1.6 V to 2.7 V
	Peripheral functions*5	AGT, AGTW, GPT, SPI, Others*4	V_{IH}	VCC × 0.8	—	—		—
			V_{IL}	—	—	VCC × 0.2		
			ΔV_T*6	VCC × 0.10	—	—		VCC = 2.7 V to 5.5 V
				VCC × 0.05	—	—		VCC = 1.6 V to 2.7 V
		RTCIC0-2*7	V_{IH}	VRTC × 0.8	—	5.8		—
			V_{IL}	0	—	VRTC × 0.2		
			ΔV_T*6	—	0.71	—		
		IIC (except for SMBus)*1	V_{IH}	VCC × 0.7	—	5.8		—
			V_{IL}	—	—	VCC × 0.3		
			ΔV_T*6	VCC × 0.10	—	—		VCC = 2.7 V to 5.5 V
				VCC × 0.05	—	—		VCC = 1.6 V to 2.7 V
		IIC (SMBus)*2	V_{IH}	2.2	—	—		VCC = 3.6 V to 5.5 V
			V_{IL}	2.0	—	—		VCC = 2.7 V to 3.6 V
			V_{IL}	—	—	0.8		VCC = 3.6 V to 5.5 V
			V_{IL}	—	—	0.5		VCC = 2.7 V to 3.6 V

Note 1. SCL0, SDA0 (total 2 pins). 5V-tolerant ports are used as N-ch open-drain ports.
Note 2. SCL0, SCL1, SDA0, SDA1 (total 4 pins)
Note 3. P410, P411 (total 2 pins). 5V-tolerant ports are used as normal CMOS ports.
Note 4. PmnPFS.ISEL = 1.

Note 5. PmnPFS.PMR = 1.
Note 6. This is the hysteresis characteristic of the Schmitt Trigger circuit.
Note 7. When inputting a high level to P400 to P402 (RTCIC0 to RTCIC2), connect the pins individually to the higher voltage of VCC and VRTC through a resistor.

2.2.3 I/O I_{OH}, I_{OL}

Table 2.5 I/O I_{OH}, I_{OL} (1 of 3)

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (average value per pin)	Ports P001, P002, P014, P015, P212, P213, P410, P411	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	8.0	mA	
	Ports P400 to P402	I_{OL}	—	—	15.0	mA	
	Other output pins*1	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	20.0	mA	
Permissible output current (max value per pin)	Ports P001, P002, P014, P015, P212, P213, P410, P411	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	8.0	mA	
	Ports P400 to P402	I_{OL}	—	—	15.0	mA	
	Other output pins*1	I_{OH}	—	—	-4.0	mA	
		I_{OL}	—	—	20.0	mA	

Table 2.5 I/O I_{OH}, I_{OL} (2 of 3)

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	Total of ports P001, P002, P014, P015		$\Sigma I_{OH\ (max)}$	—	—	-16	mA	AVCC = 2.7 to 5.5 V
				—	—	-4	mA	AVCC = 1.8 to 2.7 V
				—	—	-2	mA	AVCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	32	mA	AVCC = 2.7 to 5.5 V
				—	—	2.4	mA	AVCC = 1.8 to 2.7 V
				—	—	1.2	mA	AVCC = 1.6 to 1.8 V
	Total of ports P212, P213		ΣI_{OH}	—	—	-8	mA	VCC = 2.7 to 5.5 V
				—	—	-2	mA	VCC = 1.8 to 2.7 V
				—	—	-1	mA	VCC = 1.6 to 1.8 V
	Total of ports P212, P213, P400 to P402		ΣI_{OL}	—	—	20.0	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of ports P403 to P405		ΣI_{OH}	—	—	-12	mA	VCC = 2.7 to 5.5 V
				—	—	-3	mA	VCC = 1.8 to 2.7 V
				—	—	-1.5	mA	VCC = 1.6 to 1.8 V
			ΣI_{OL}	—	—	50	mA	VCC = 4.0 to 5.5 V
				—	—	24	mA	VCC = 2.7 to 4.0 V
				—	—	1.8	mA	VCC = 1.8 to 2.7 V
				—	—	0.9	mA	VCC = 1.6 to 1.8 V
	Total of ports P108, P201, P204 to P211, P300, P408 to P411, P600	100-pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V

Table 2.5 I/O I_{OH}, I_{OL} (3 of 3)

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Permissible output current (max value total pins)*2	Total of ports P100 to P103, P109 to P115, P203, P301 to P313	100-pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of ports P004 to P013, P104 to P107, P500 to P506	100-pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of all output pin	100-pin products	$\Sigma I_{OH\ (max)}$	—	—	-90	mA	
			$\Sigma I_{OL\ (max)}$	—	—	100	mA	
	Total of ports P009 to P013, P100 to P112, P201, P203 to P211, P300 to P304, P310 to P313, P410, P411, P500 to P506, P600	80-pin products 64-pin products	$\Sigma I_{OH\ (max)}$	—	—	-30	mA	VCC = 2.7 to 5.5 V
				—	—	-8	mA	VCC = 1.8 to 2.7 V
				—	—	-4	mA	VCC = 1.6 to 1.8 V
			$\Sigma I_{OL\ (max)}$	—	—	50	mA	VCC = 2.7 to 5.5 V
				—	—	4	mA	VCC = 1.8 to 2.7 V
				—	—	2	mA	VCC = 1.6 to 1.8 V
	Total of all output pin	80-pin products 64-pin products	$\Sigma I_{OH\ (max)}$	—	—	-60	mA	
			$\Sigma I_{OL\ (max)}$	—	—	100	mA	

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Note 2. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
<Example> Where n = 80% and I_{OH} = −30.0 mA
Total output current of pins = (−30.0 × 0.7)/(80 × 0.01) ≅ −26.2 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in Table 2.5.

2.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 2.6 I/O V_{OH}, V_{OL} (1)

Conditions: VCC = AVCC = 4.0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P001, P002, P014, P015	V_{OH}	AVCC - 0.8	—	—	V	I_{OH} = -4.0 mA
	Output pins except for P001, P002, P014, P015*1	V_{OH}	VCC - 0.8	—	—		I_{OH} = -4.0 mA
	Ports P001, P002, P014, P015	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Ports P212, P213, P410, P411	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Ports P400 to P402	V_{OL}	—	—	2.0		I_{OL} = 15.0 mA
	Output pins except for P001, P002, P014, P015, P212, P213, P410, P411, and P400 to P402*1	V_{OL}	—	—	1.2		I_{OL} = 20.0 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.7 I/O V_{OH}, V_{OL} (2)

Conditions: VCC = AVCC = 2.7 to 4.0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P001, P002, P014, P015	V_{OH}	AVCC - 0.8	—	—	V	I_{OH} = -4.0 mA
	Output pins except for P001, P002, P014, P015*1	V_{OH}	VCC - 0.8	—	—		I_{OH} = -4.0 mA
	Ports P001, P002, P014, P015	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA
	Ports P400 to P402	V_{OL}	—	—	0.4		I_{OL} = 3.0 mA
	Output pins except for P001, P002, P014, P015, P400 to P402 *1	V_{OL}	—	—	0.8		I_{OL} = 8.0 mA

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.8 I/O V_{OH}, V_{OL} (3)

Conditions: VCC = AVCC = 1.6 to 2.7 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P001, P002, P014, P015	V_{OH}	AVCC - 0.5	—	—	V	I_{OH} = -1.0 mA AVCC = 1.8 to 2.7 V
			AVCC - 0.5	—	—		I_{OH} = -0.5 mA AVCC = 1.6 to 1.8 V
	Output pins except for P001, P002, P014, P015*1	V_{OH}	VCC - 0.5	—	—		I_{OH} = -1.0 mA VCC = 1.8 to 2.7 V
			VCC - 0.5	—	—		I_{OH} = -0.5 mA VCC = 1.6 to 1.8 V
	Ports P001, P002, P014, P015	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA AVCC = 1.8 to 2.7 V
			—	—	0.4		I_{OL} = 0.3 mA AVCC = 1.6 to 1.8 V
	Ports P400 to P402		—	—	0.4		I_{OL} = 2 mA VCC = 1.8 to 2.7 V
			—	—	0.4		I_{OL} = 1 mA VCC = 1.6 to 1.8 V
	Output pins except for P001, P002, P014, P015, P400 to P402 *1	V_{OL}	—	—	0.4		I_{OL} = 0.6 mA VCC = 1.8 to 2.7 V
			—	—	0.4		I_{OL} = 0.3 mA VCC = 1.6 to 1.8 V

Note 1. Except for Ports P200, P214, and P215, which are input ports.

Table 2.9 I/O other characteristics

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, ports P200	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = VCC
	Ports P214, P215		—	—	1.0	μA	V_{in} = 0 V V_{in} = VRTC
Three-state leakage current (off state)	5V-tolerant ports*1	$\lvert I_{TSI} \rvert$	—	—	1.0	μA	V_{in} = 0 V V_{in} = 5.8 V
	Ports P400 to P402 (N-ch open drain, 5V-tolerant)		—	—	1.0		V_{in} = 0 V V_{in} = 5.8 V
	Other ports (except for P200, P214, P215, and 5V-tolerant ports, P400 to P402)		—	—	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up resistor	All ports (except for P200, P214, P215, P400 to P402, P600)	R_U	10	20	100	kΩ	V_{in} = 0 V
Input capacitance	P200	C_{in}	—	—	30	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Other input pins		—	—	15		

Note 1. P410-411 (total 2 pins)

2.2.5 Operating and Standby Current

Table 2.10 Operating and standby current (1) (1 of 2)

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter					Symbol	LDO mode		Unit
						Typ*10	Max	
Supply current*1	High-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 48 MHz*7	I_{CC}	4.80*11	—	mA
				ICLK = 32 MHz*7		3.45	—	
				ICLK = 16 MHz*7		2.10	—	
				ICLK = 8 MHz*7		1.45	—	
			All peripheral clocks enabled, code executing from flash*5	ICLK = 48 MHz*9		—	12.9*11	
		Sleep mode	All peripheral clocks disabled*5	ICLK = 48 MHz*7		1.06	—	
				ICLK = 32 MHz*7		1.00	—	
				ICLK = 16 MHz*7		0.75	—	
				ICLK = 8 MHz*7		0.65	—	
			All peripheral clocks enabled*5	ICLK = 48 MHz*9		4.45	—	
				ICLK = 32 MHz*8		4.40	—	
				ICLK = 16 MHz*8		2.50	—	
				ICLK = 8 MHz*8		1.30	—	
		Increase during BGO operation*6				2.1	—	

Table 2.10 Operating and standby current (1) (2 of 2)

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter						Symbol	LDO mode		Unit
							Typ*10	Max	
Supply current*1	Middle-speed mode*2	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 24 MHz*7		I_{CC}	2.65	—	mA
				ICLK = 4 MHz*7			0.90	—	
			All peripheral clocks enabled, code executing from flash*5	ICLK = 24 MHz*8			—	9.0	
		Sleep mode	All peripheral clocks disabled*5	ICLK = 24 MHz*7			0.80	—	
				ICLK = 4 MHz*7			0.60	—	
			All peripheral clocks enabled*5	ICLK = 24 MHz*8			3.35	—	
				ICLK = 4 MHz*8			1.05	—	
		Increase during BGO operation*6					1.75	—	
Supply current*1	Low-speed mode*3	Normal mode	All peripheral clocks disabled, CoreMark code executing from flash*5	ICLK = 2 MHz*7		I_{CC}	0.3	—	mA
			All peripheral clocks enabled, code executing from flash*5	ICLK = 2 MHz*8			—	3.3	
		Sleep mode	All peripheral clocks disabled*5	ICLK = 2 MHz*7			0.13	—	
			All peripheral clocks enabled*5	ICLK = 2 MHz*8			0.35	—	
	Subosc-speed mode*4	Normal mode	All peripheral clocks disabled, while (1) code executing from flash*5	ICLK = 32.768 kHz*8		I_{CC}	4.40	—	µA
			All peripheral clocks enabled, while (1) code executing from flash*5	ICLK = 32.768 kHz			7.80	—	
			All peripheral clocks enabled, code executing from flash*5	ICLK = 32.768 kHz*8	T_a = 25°C		9.3	—	
					T_a = 55°C		10.6	—	
					T_a = 70°C		11.5	—	
					T_a = 85°C		13.0	—	
					T_a = 105°C		17.6	156	
		Sleep mode	All peripheral clocks disabled*5	ICLK = 32.768 kHz*8	—		2.40	—	
			All peripheral clocks enabled*5	ICLK = 32.768 kHz*8	T_a = 25°C		5.80	—	
					T_a = 55°C		6.8	—	
					T_a = 70°C		7.65	—	
					T_a = 85°C		9.1	—	
					T_a = 105°C		15.6	—	

Note 1. Supply current is the total current flowing into VCC and VRTC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The clock source is HOCO.
Note 3. The clock source is MOCO.

Note 4. The clock source is the sub-clock oscillator.
Note 5. This does not include BGO and A/D operation.
Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.
Note 7. PCLKB and PCLKD are set to divided by 64.
Note 8. PCLKB and PCLKD are the same frequency as that of ICLK.
Note 9. PCLKB are set to be divided by 2 and PCLKD is the same frequency as that of ICLK.
Note 10. VCC = 3.3 V.
Note 11. The prefetch is operating.

Table 2.11 Operating and standby current (2)

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter				Symbol	Typ*3	Max	Unit
Supply current*1	Software Standby mode*2	All SRAMs(0x2000_4000 to 0x2000_BFFF) are on	T_a = 25°C	I_{CC}	0.40	2.5	µA
			T_a = 55°C		0.85	9.8	
			T_a = 70°C		1.35	25	
			T_a = 85°C		2.60	40	
			T_a = 105°C		6.05	63	
		Only 8KB SRAM (0x2000_4000 to 0x2000_5FFF) is on	T_a = 25°C		0.35	2.5	
			T_a = 55°C		0.75	9.8	
			T_a = 70°C		1.20	25	
			T_a = 85°C		2.25	40	
			T_a = 105°C		5.35	63	
	Increment for independent power supply RTC operation in normal operation mode with sub-clock oscillator*4		SOMCR.SODRV[1:0] are 11b (Low power mode 3)		0.15	—	
			SOMCR.SODRV[1:0] are 00b (normal mode)		0.95	—	

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.
Note 2. The IWDT and LVD are not operating.
Note 3. VCC = 3.3 V.
Note 4. Current flowing to VRTC pin, includes RTC power supply, sub-oscillation circuit current, and RTC.

Table 2.12 Operating and standby current (3)

Conditions: VCC = AVCC = 0 V, VRTC = 1.6 to 5.5 V, VSS = AVSS = 0 V

Parameter				Symbol	Typ*3	Max*3	Unit
Supply current*1	Increment for independent power supply RTC operation when VCC is off *2*3	VRTC = 3.3 V SOMCR.SODRV[1:0] are 11b (Low power mode 3)	T_a = 25°C	I_{CC}	0.46	—	µA
			T_a = 55°C		0.50	—	
			T_a = 85°C		0.60	—	
			T_a = 105°C		0.65	—	
		VRTC = 3.3 V SOMCR.SODRV[1:0] are 00b (Normal mode)	T_a = 25°C		1.25	—	
			T_a = 55°C		1.35	—	
			T_a = 85°C		1.55	—	
			T_a = 105°C		1.70	—	
		VRTC = 3.3V SOMCR.SODRV[1:0] are 10b (Low power mode 2)	T_a = 25°C		0.65	—	
			T_a = 55°C		0.70	—	
			T_a = 85°C		0.80	—	
			T_a = 105°C		0.85	—	
		VRTC = 3.3 V SOMCR.SODRV[1:0] are 01b (Low power mode 1)	T_a = 25°C		0.80	—	
			T_a = 55°C		0.90	—	
			T_a = 85°C		1.00	—	
			T_a = 105°C		1.10	—	

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOS transistors are in the off state. The supply current is total current flowing into VRTC.
Note 2. Current flowing to VRTC pin, including RTC power supply, sub-oscillation circuit current, and RTC.
Note 3. Typ Ta = 25℃, max Ta = 105℃.

Table 2.13 Operating and standby current (4) (1 of 2)

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Analog power supply current	During 12-bit A/D conversion (at high-speed A/D conversion mode)		I_{AVCC}	—	—	1.44	mA
	During 12-bit A/D conversion (at low-power A/D conversion mode)			—	—	0.78	mA
	Waiting for 12-bit A/D conversion (all units)*1			—	—	1.0	µA
	During 24-bit sigma-delta A/D conversion (normal conversion) (AVCC = 2.4 to 5.5 V)*2	7 ch + Regulator, 16 MHz, 8 kHz sampling mode		—	4.1	5.5	mA
		4 ch + Regulator, 16 MHz, 8 kHz sampling mode		—	2.5	3.4	mA
		3 ch + Regulator, 16 MHz, 8 kHz sampling mode		—	2.0	2.7	mA
		1 ch + Regulator, 16 MHz, 8 kHz sampling mode		—	0.9	1.3	mA
		1 ch + Regulator, 16 MHz, 8 kHz/4 kHz hybrid sampling mode		—	0.9	1.3	mA
		1 ch + Regulator, PLL (12.8 MHz) 8 kHz sampling mode*3		—	0.9	1.3	mA
	During 24-bit sigma-delta A/D conversion (power down) (AVCC = 2.4 to 5.5 V)	7 ch SDADMR.PONn (n = 0 to 6), Regulator, 16 MHz, 8 kHz sampling mode		—	—	1.60	µA
	Waiting for 24-bit sigma-delta A/D conversion *4 (AVCC = 2.4 to 5.5 V)			—	—	1.5	µA
Reference power supply current	During 12-bit A/D conversion		I_{REFH0}	—	—	120	µA
	Waiting for 12-bit A/D conversion			—	—	60	nA
Temperature Sensor (TSN) operating current			I_{TNS}	—	95	—	µA
Watchdog timer operating current	Current flowing to VCC including ILOCO, main clock is stopped		I_{WDT}	—	0.2	—	µA
LVDVBAT operating current	Current flowing to EXLVDVBAT		$I_{LVDVBAT}$	—	0.033	—	µA
	Current flowing to VCC			—	0.04	—	µA
LVDVRTC operating current	Current flowing to VRTC		$I_{LVDVRTC}$	—	0.15	—	µA
	Current flowing to VCC			—	0.04	—	µA
LVDEXLVD operating current	Current flowing to EXLVD		$I_{LVDEXLVD}$	—	0.083	—	µA
	Current flowing to VCC			—	0.04	—	µA
LVD0 operating current	Current flowing to VCC		I_{LVD0}	—	0.045	—	µA
LVD1 operating current	Current flowing to VCC		I_{LVD1}	—	0.141	—	µA
LVD2 operating current	Current flowing to VCC		I_{LVD2}	—	0.120	—	µA
Sub oscillation stop detection for SDADCCLK operating current			I_{SOSTD}	—	0.1	—	µA
Main oscillation stop detection for SDADCCLK operating current			I_{MOSTD}	—	29	—	µA
Bank programming operating current			I_{BNKP}	—	2.05	13.5	mA

Table 2.13 Operating and standby current (4) (2 of 2)

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter				Symbol	Min	Typ	Max	Unit
LCD operating current	External resistance division method	$f_{LCD} = f_{SUB}$ (32.768 kHz) LCD clock = 128 Hz 1/3 bias, four-time-slices	VCC = 5.0 V, V_{L4} = 5.0 V	I_{LCD1} *5*6	—	0.05	—	µA
	Internal voltage boosting method	$f_{LCD} = f_{SUB}$ (32.768 kHz) LCD clock = 128 Hz 1/3 bias, four-time-slices V_{L1} reference, VL1AMP enabled	VCC = 3.0 V, V_{L4} = 3.0 V (VLCD = 04H)	I_{LCD2} *5	—	1.00	—	µA
			VCC = 5.0 V, V_{L4} = 5.1 V (VLCD = 19H)		—	1.20	—	µA
		$f_{LCD} = f_{SUB}$ (32.768 kHz) LCD clock = 128 Hz 1/3 bias, four-time-slices V_{L2} reference, VL2AMP enabled	VCC = 3.0 V, V_{L4} = 3.0 V (VLCD = 84H)	I_{LCD4} *5	—	0.80	—	µA
			VCC = 5.0 V, V_{L4} = 5.1 V (VLCD = 99H)		—	1.00	—	µA
	Capacitor split method	$f_{LCD} = f_{SUB}$ (32.768 kHz) LCD clock = 128 Hz 1/3 bias, four-time-slices V_{CC} reference,	VCC = 3.0 V, V_{L4} = 3.0 V	I_{LCD3} *5	—	0.20	—	µA
		$f_{LCD} = f_{SUB}$ (32.768 kHz) LCD clock = 128 Hz 1/3 bias, four-time-slices V_{L4} reference, VL4AMP enabled	VCC = 3.2 V, V_{L4} = 3.0 V	I_{LCD5} *5	—	0.80	—	µA

Note 1. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 module-stop bit) is in the module-stop state.
Note 2. Typ condition is 3.0 V, 25°C, and the current is the current flowing to AVDD pin.
Note 3. Not including the current of PLL.
Note 4. When the MCU is in the MSTPCRD.MSTPD17 (SDADC24 module-stop bit) is in the module-stop state.
Note 5. Conditions of the Typ. value and Max. value are as follows:

- Setting 20 pins as the segment function and blinking all
- Selecting f_{SUB} for system clock when LCD clock = 128 Hz (LCDC0 = 07H)
- Setting four time slices and 1/3 bias.

Note 6. Not including the current flowing into the external division resistor when using the external resistance division method.

2.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.14 VCC rise and fall gradient characteristics

Conditions: VCC = AVCC = 0 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.02	—	2	ms/V	—
	Voltage monitor 0 reset enabled at startup*1 *2				—		
	SCI boot mode*2				2		

Note 1. When OFS1.LVDAS = 0.
Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.

Table 2.15 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = AVCC = 1.6 to 5.5 V
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).
When the VCC change exceeds VCC ± 10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r(VCC)}$	—	—	10	kHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.2$
		—	—	1	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.08$
		—	—	10	MHz	Figure 2.2 $V_{r\ (VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ± 10%

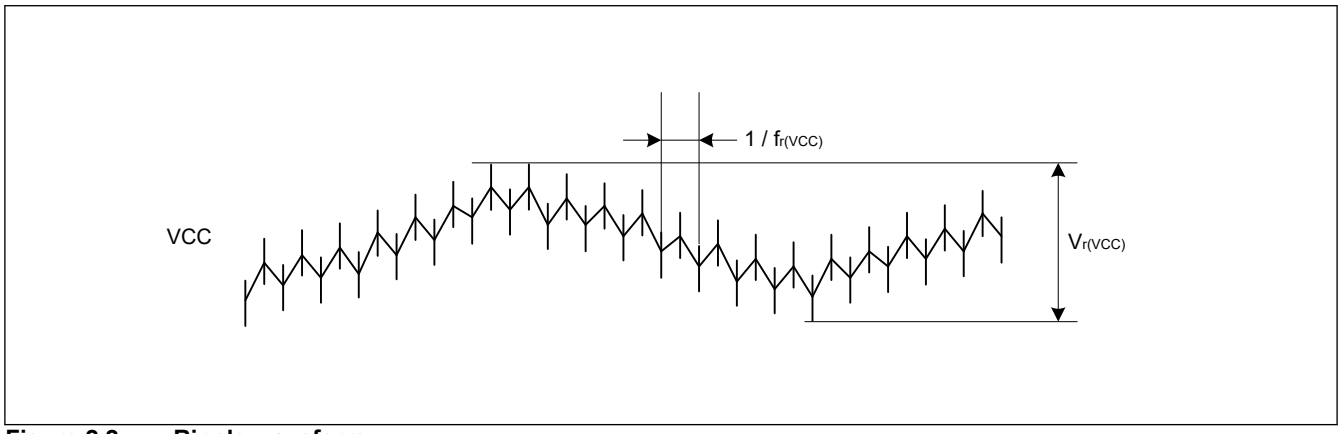


Figure 2.2 Ripple waveform

2.2.7 VRTC Rise and Fall Gradient

Table 2.16 VRTC rise and fall gradient characteristics

Conditions: VRTC = AVCC = 0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Power-on VRTC rising gradient	SrVRTC	0.02	—	20	ms/V	—

2.3 AC Characteristics

2.3.1 Frequency

Table 2.17 Operation frequency in high-speed operating mode

Conditions: VCC = AVCC = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.8 to 5.5 V	f	0.032768	—	48	MHz
	Peripheral module clock (PCLKB)	1.8 to 5.5 V		—	—	32	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		—	—	64	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.

Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.21.
Note 5. The lower-limit frequency of PCLKB is 1 MHz when the SDADC24 is in use.

Table 2.18 Operation frequency in middle-speed mode

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.8 to 5.5 V	f	0.032768	—	24	MHz
		1.6 to 1.8 V		0.032768	—	4	
	Peripheral module clock (PCLKB)	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		—	—	24	
		1.6 to 1.8 V		—	—	4	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory. When using ICLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of ICLK must be ± 1.0% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.21.
Note 5. The lower-limit frequency of PCLKB is 1 MHz when the SDADC24 is in use.

Table 2.19 Operation frequency in low-speed mode

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*1*2	1.6 to 5.5 V	f	0.032768	—	2	MHz
	Peripheral module clock (PCLKB) *5	1.6 to 5.5 V		—	—	2	
	Peripheral module clock (PCLKD)*3	1.6 to 5.5 V		—	—	2	

Note 1. The lower-limit frequency of ICLK is 1 MHz while programming or erasing the flash memory.
Note 2. The frequency accuracy of ICLK must be ± 1.0% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKD is 1 MHz when the ADC12 is in use.
Note 4. The maximum value of operation frequency does not include internal oscillator errors. For details on the range for guaranteed operation, see Table 2.21.
Note 5. The lower-limit frequency of PCLKB is 1 MHz when the SDADC24 is in use.

Table 2.20 Operation frequency in Subosc-speed mode

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*1	1.6 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	Peripheral module clock (PCLKB) *3	1.6 to 5.5 V		—	—	37.6832	
	Peripheral module clock (PCLKD)*2	1.6 to 5.5 V		—	—	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The ADC12 cannot be used.
Note 3. The SDADC24 cannot be used when PCLKB is selected to subosc, but operating clock of SDADC24 can use PLL clock multiplied from subosc.

2.3.2 Clock Timing

Table 2.21 Clock timing (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 2.3
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rising time	t_{Xr}	—	—	5	ns	
EXTAL external clock falling time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{EXWT}	0.3	—	—	μs	—
EXTAL external clock input frequency	f_{EXTAL}	—	—	20	MHz	1.8 ≤ VCC ≤ 5.5
		—	—	4		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	1.8 ≤ VCC ≤ 5.5
		1	—	4		1.6 ≤ VCC < 1.8
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	—
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	100	μs	Figure 2.4
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	—
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	—
MOCO clock oscillation stabilization time	t_{MOCO}	—	—	1	μs	—
HOCO clock oscillation frequency*5 100-pin LQFP	f_{HOCO24}	23.76	24	24.24	MHz	Ta =-20 to 85°C, 1.6 ≤ VCC ≤ 5.5
		23.64		24.36		Ta =-40 to 105°C, 1.6 ≤ VCC ≤ 5.5
	f_{HOCO32}	31.68	32	32.32		Ta =-20 to 85°C, 1.6 ≤ VCC ≤ 5.5
		31.52		32.48		Ta =-40 to 105°C, 1.6 ≤ VCC ≤ 5.5
	f_{HOCO48}	47.52	48	48.48		Ta =-20 to 85°C, 1.6 ≤ VCC ≤ 5.5
		47.28		48.72		Ta =-40 to 105°C, 1.6 ≤ VCC ≤ 5.5
	f_{HOCO64}	63.36	64	64.64		Ta =-20 to 85°C, 1.6 ≤ VCC ≤ 5.5
		63.04		64.96		Ta =-40 to 105°C, 1.6 ≤ VCC ≤ 5.5

Table 2.21 Clock timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
HOCO clock oscillation frequency*5 80-pin LQFP 64-pin LQFP	f_{HOCO24}	23.76	24	24.24	MHz	Ta =-10 to 70°C, 1.6 ≤ VCC ≤ 5.5
		23.72		23.29		Ta =-20 to 85°C, 1.6 ≤ VCC ≤ 5.5
		23.57		24.44		Ta =-40 to 105°C, 1.6 ≤ VCC ≤ 5.5
	f_{HOCO32}	31.68	32	32.32		Ta =-10 to 70°C, 1.6 ≤ VCC ≤ 5.5
		31.62		32.39		Ta =-20 to 85°C, 1.6 ≤ VCC ≤ 5.5
		31.43		32.58		Ta =-40 to 105°C, 1.6 ≤ VCC ≤ 5.5
	f_{HOCO48}	47.52	48	48.48		Ta =-10 to 70°C, 1.6 ≤ VCC ≤ 5.5
		47.43		48.58		Ta =-20 to 85°C, 1.6 ≤ VCC ≤ 5.5
		47.14		48.87		Ta =-40 to 105°C, 1.6 ≤ VCC ≤ 5.5
	f_{HOCO64}	63.36	64	64.64		Ta =-10 to 70°C, 1.6 ≤ VCC ≤ 5.5
		63.24		64.77		Ta =-20 to 85°C, 1.6 ≤ VCC ≤ 5.5
		62.85		65.16		Ta =-40 to 105°C, 1.6 ≤ VCC ≤ 5.5
HOCO clock oscillation stabilization time*3 *4	t_{HOCO24} t_{HOCO32} t_{HOCO48} t_{HOCO64}	—	1.9	—	µs	Figure 2.5
Sub-clock oscillator oscillation frequency*6	f_{SUB}	—	32.768	—	kHz	—
Sub-clock oscillation stabilization time*2	t_{SUBOSC}	—	0.5	—	s	Figure 2.6
PLL input frequency*7	f_{PLLIN}	—	32.768	—	kHz	—
PLL clock frequency	f_{PLL}	10	12.8	13	MHz	—
PLL clock oscillation stabilization time*8	t_{PLLWT}	—	—	10	ms	Figure 2.7

Note 1. Time until the clock can be used after the Main Clock Oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.
Note 2. After changing the setting of the SOSCCR.SOSTP bit to start sub-clock oscillator operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapsed. Use the oscillator wait time value recommended by the oscillator manufacturer.
Note 3. This is a characteristic when the HOCOCR.HCSTP bit is set to 0 (oscillation) in the MOCO stop state. When the HOCOCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 µs.
Note 4. Check OSCSF.HOCOSF to confirm whether stabilization time has elapsed.
Note 5. Accuracy at production test.
Note 6. The power supply of sub-clock oscillator is VRTC.
Note 7. The VCC range that the PLL can be used is 2.4 to 5.5 V (same as the power supply range of 24-bit Sigma-Delta A/D converter).
Note 8. This is a characteristic when PLLCR.PLLSTP bit is set to 0 (operation) in SUBOSC operation state. After setting the PLLSTP bit to 0, confirm that the OSCSF.PLLSF bit is set to 1 before using the PLL clock for 24-bit Sigma-Delta A/D converter clock (SDADCCLK).

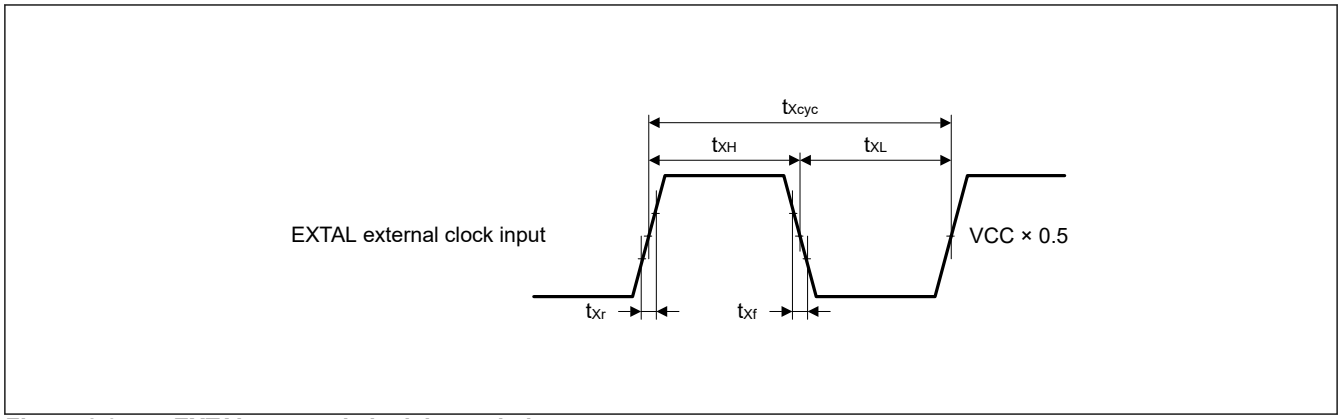


Figure 2.3 EXTAL external clock input timing

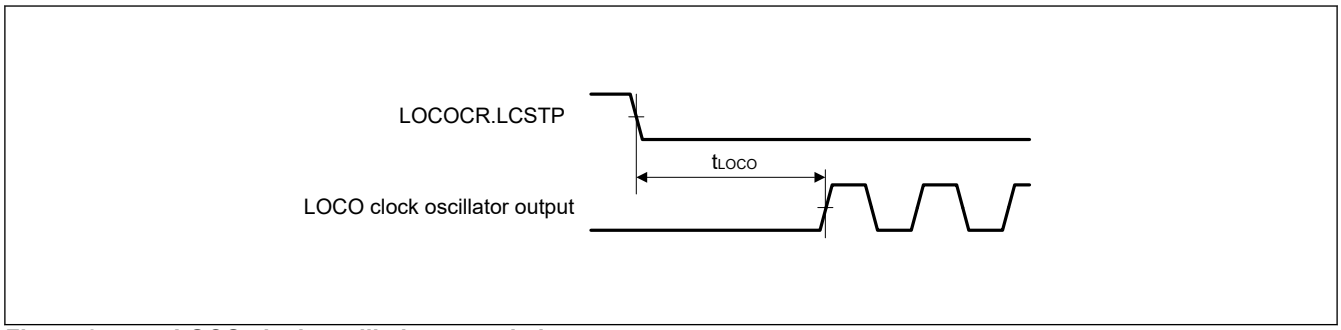
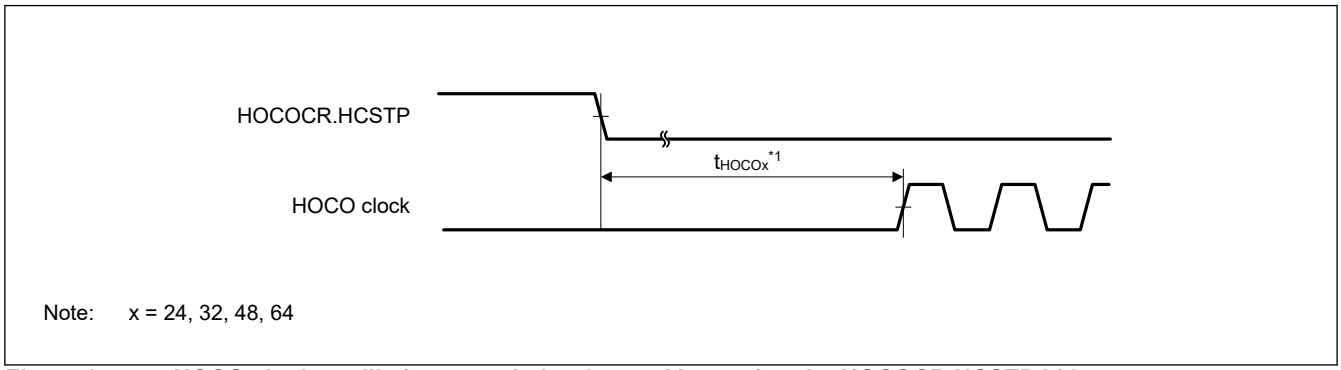


Figure 2.4 LOCO clock oscillation start timing



Note: x = 24, 32, 48, 64

Figure 2.5 HOCO clock oscillation start timing (started by setting the HOCOCR.HCSTP bit)

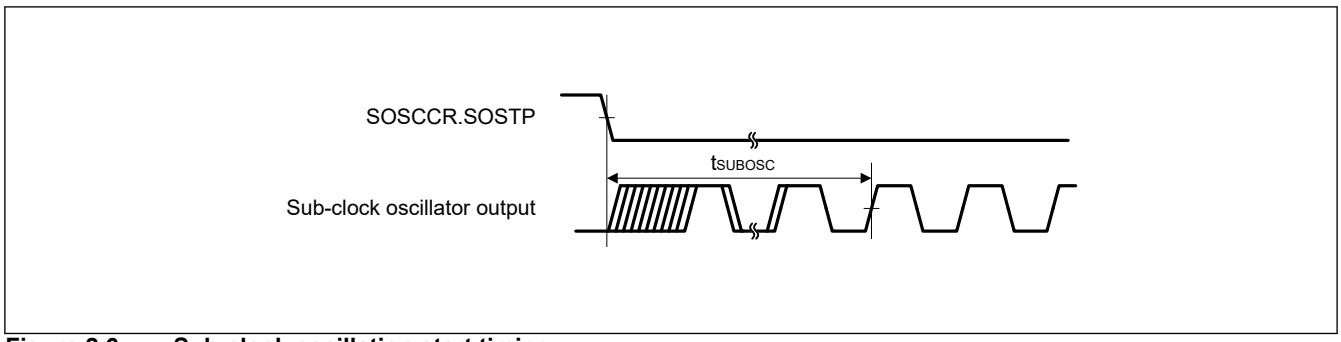


Figure 2.6 Sub-clock oscillation start timing

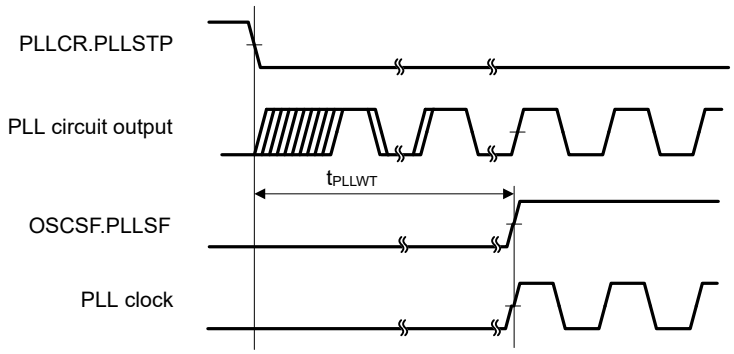


Figure 2.7 PLL clock oscillation start timing

2.3.3 Reset Timing

Table 2.22 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on (POR)	t_{RESWP}	10	—	—	ms	Figure 2.8
	Not at power-on	t_{RESW}	30	—	—	µs	Figure 2.9
Wait time after RES cancellation (at power-on)	LVD0 enabled*1	t_{RESWT}	—	0.9	—	ms	Figure 2.8
	LVD0 disabled*2		—	0.2	—		
Wait time after RES cancellation (during powered-on state)	LVD0 enabled*1	t_{RESWT2}	—	0.9	—	ms	Figure 2.9
	LVD0 disabled*2		—	0.2	—		
Wait time after internal reset cancellation (Watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset, software reset)	LVD0 enabled*1	t_{RESWT3}	—	0.9	—	ms	Figure 2.10
	LVD0 disabled*2		—	0.15	—		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

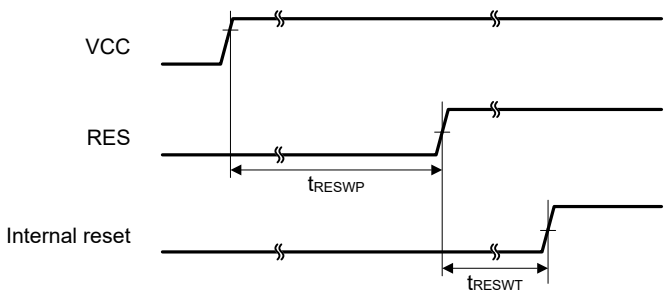


Figure 2.8 Reset input timing at power-on

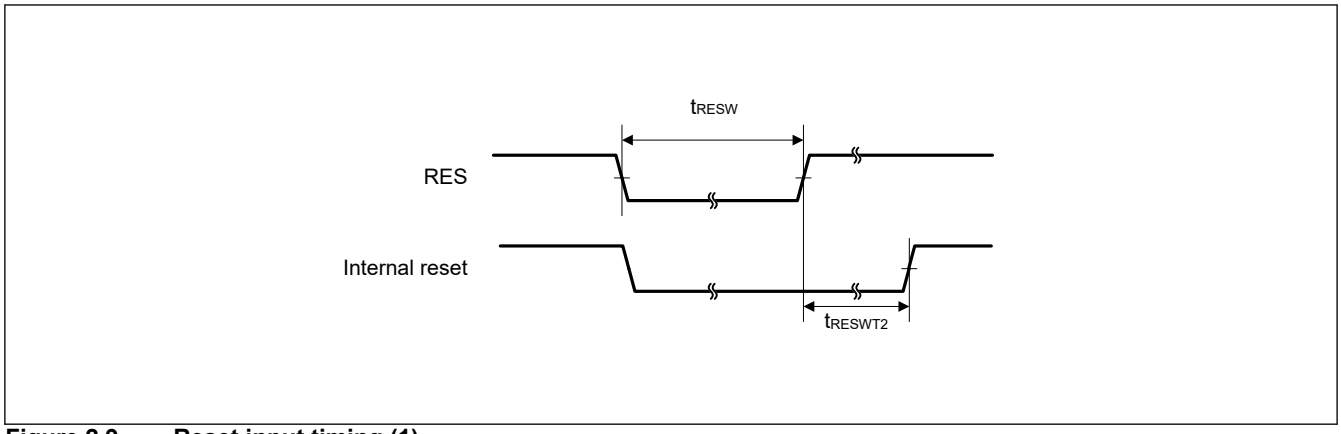


Figure 2.9 Reset input timing (1)

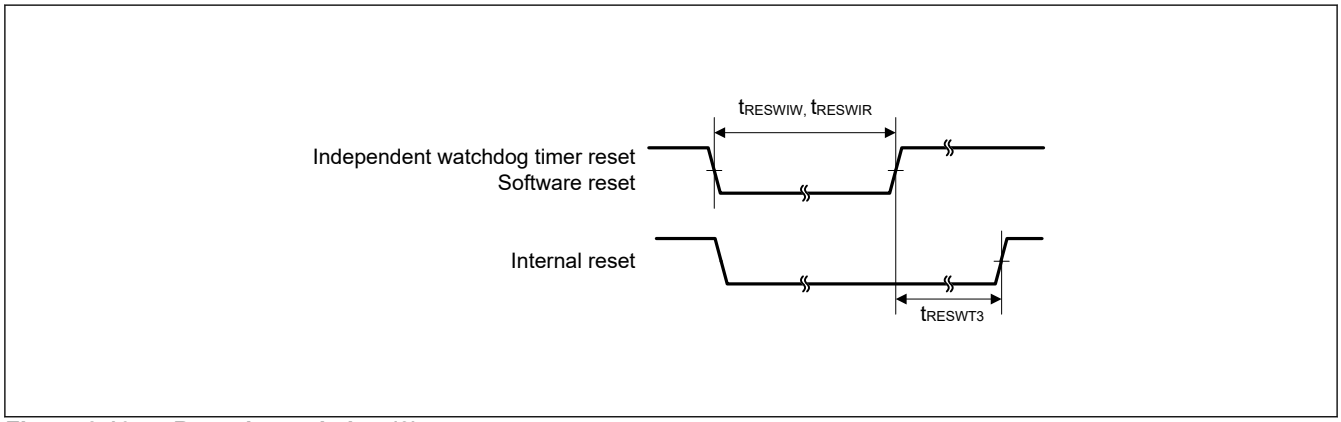


Figure 2.10 Reset input timing (2)

2.3.4 Wakeup Time

Table 2.23 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 2.11
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3	t_{SBYEX}	—	2.4	3.1	µs	
		System clock source is HOCO (HOCO clock is 32 MHz)		t_{SBYHO}	—	4.9	6.2	µs	
		System clock source is HOCO (HOCO clock is 48 MHz)		t_{SBYHO}	—	4.8	6	µs	
		System clock source is HOCO (HOCO clock is 64 MHz)		t_{SBYHO}	—	4.9	6.2	µs	
		System clock source is MOCO (8 MHz)		t_{SBYMO}	—	4	5	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

Table 2.24 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t_{SBYMC}	—	2	3	ms	
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3 VCC = 1.8 V to 5.5 V	t_{SBYEX}	—	2.4	3.1	µs	
			System clock source is main clock oscillator (20 MHz)*3 VCC = 1.6 V to 1.8 V		—	11.7	13		
		System clock source is HOCO*4	VCC = 1.8 V to 5.5 V	t_{SBYHO}	—	5.2	6.5	µs	Figure 2.11
			VCC = 1.6 V to 1.8 V		—	13.2	15		
		System clock source is MOCO (8 MHz)	VCC = 1.8 V to 5.5 V	t_{SBYMO}	—	4	5	µs	
			VCC = 1.6 V to 1.8 V		—	7.2	9		

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.
Note 4. The system clock is 24 MHz.

Table 2.25 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (2 MHz)*2	t_{SBYMC}	—	2	3	ms	Figure 2.11
		External clock input to main clock oscillator	System clock source is main clock oscillator (2 MHz)*3	t_{SBYEX}	—	14.5	16	µs	
		System clock source is MOCO (2 MHz)		t_{SBYMO}	—	12	15	µs	

Note 1. The division ratio of ICLK and PCLKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.
Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x05.
Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 0x00.

Table 2.26 Timing of recovery from low power modes (4)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t_{SBYSC}	—	0.85	1	ms	Figure 2.11
		System clock source is LOCO (32.768 kHz)	t_{SBYLO}	—	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues oscillating in Software Standby mode during Subosc-speed mode.

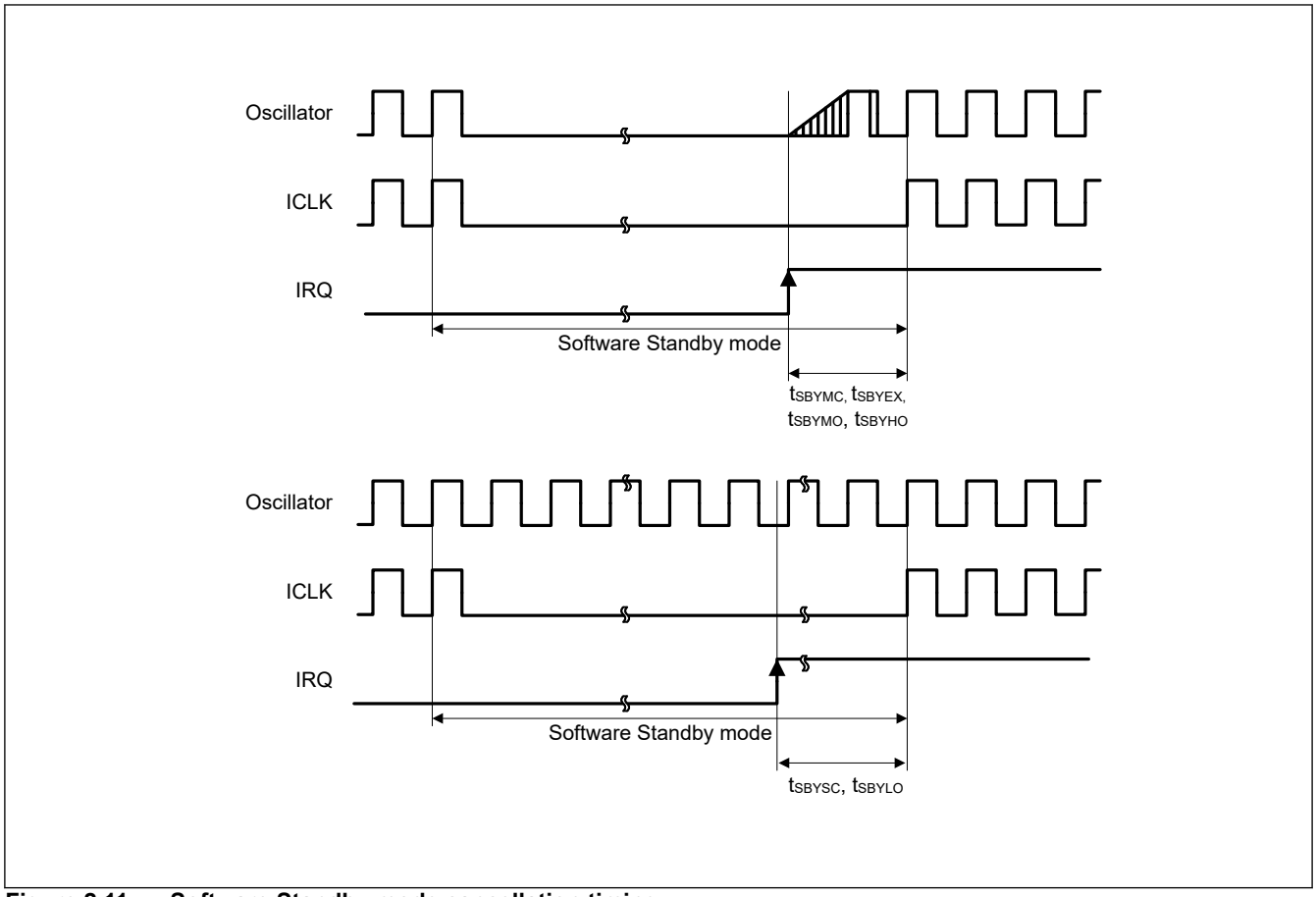
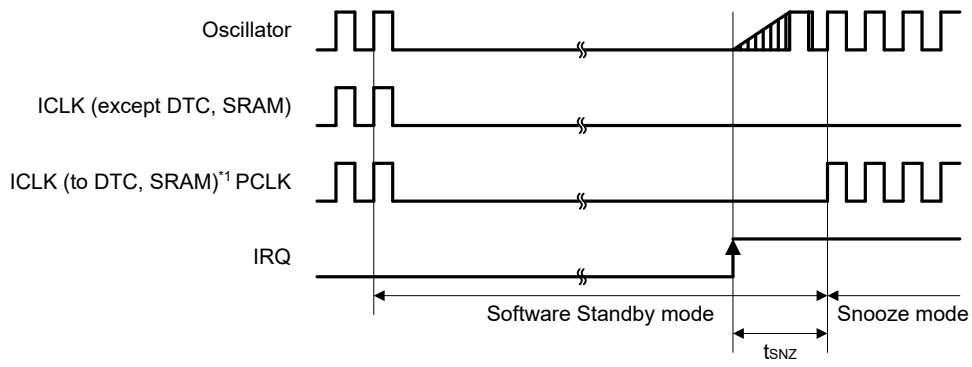


Figure 2.11 Software Standby mode cancellation timing

Table 2.27 Timing of recovery from low power modes (5)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	—	4.1	5.2	µs	Figure 2.12
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.8 V to 5.5 V	t_{SNZ}	—	4.2	5.3	µs	
	Middle-speed mode System clock source is HOCO (24 MHz) VCC = 1.6 V to 1.8 V	t_{SNZ}	—	8.3	10	µs	
	Low-speed mode System clock source is MOCO (2 MHz)	t_{SNZ}	—	6.7	8.0	µs	



Note 1. When SNZCR.SNZDTCEN bit is set to 1, ICLK is supplied to DTC and SRAM.

Figure 2.12 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.28 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5^{*2}$	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2^{*1}$	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5^{*3}$	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is being switched it is needed to add 4 clock cycle of switched source.
Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

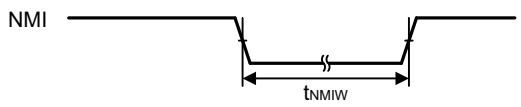


Figure 2.13 NMI interrupt input timing

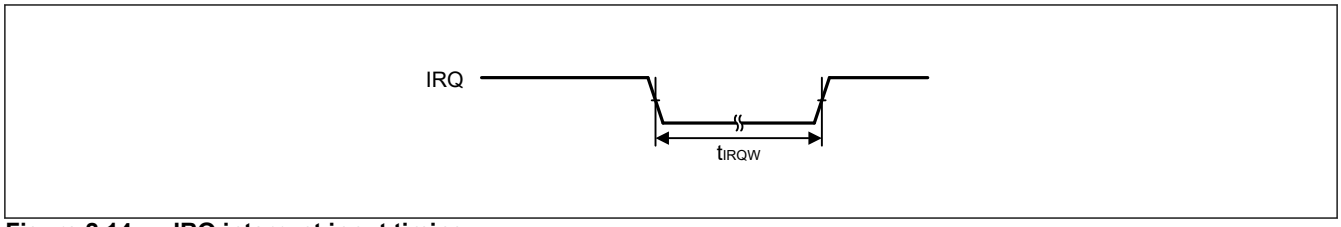


Figure 2.14 IRQ interrupt input timing

2.3.6 I/O Ports, POEG, GPT, AGT/AGTW, and ADC12 Trigger Timing

Table 2.29 I/O Ports, POEG, GPT, AGT/AGTW, and ADC12 trigger timing

Parameter			Symbol	Min	Max	Unit	Test conditions
I/O Ports	Input data pulse width	2.7 V ≤ VCC ≤ 5.5 V	t_{PRW}	2	—	t_{Pcyc}	Figure 2.15
		2.4 V ≤ VCC < 2.7 V		3			
		1.6 V ≤ VCC < 2.4 V		4			
POEG	POEG input trigger pulse width		t_{POEW}	3	—	t_{Pcyc}	Figure 2.16
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	—	t_{PDcyc}	Figure 2.17
		Dual edge		2.5	—		
AGT/AGTW	AGTIO/AGTWIO, AGTEE/ AGTWEE input cycle	1.8 V ≤ VCC ≤ 5.5 V	t_{ACYC}*1	250	—	ns	Figure 2.18
		1.6 V ≤ VCC < 1.8 V		2000	—	ns	
	AGTIO/AGTWIO, AGTEE/ AGTWEE input high-level width, low-level width	1.8 V ≤ VCC ≤ 5.5 V	t_{ACKWH}, t_{ACKWL}	100	—	ns	
		1.6 V ≤ VCC < 1.8 V		800	—	ns	
	AGTIO/AGTWIO, AGTO/ AGTWO, AGTOA/ AGTWOA,AGTOB/AGTWOB output cycle	2.7 V ≤ VCC ≤ 5.5 V	t_{ACYC2}	62.5	—	ns	Figure 2.18
		2.4 V ≤ VCC < 2.7 V		125	—	ns	
		1.8 V ≤ VCC < 2.4 V		250	—	ns	
		1.6 V ≤ VCC < 1.8 V		500	—	ns	
ADC12	12-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 2.19

Note 1. Constraints on AGTIO input: t_{Pcyc} × 2 (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

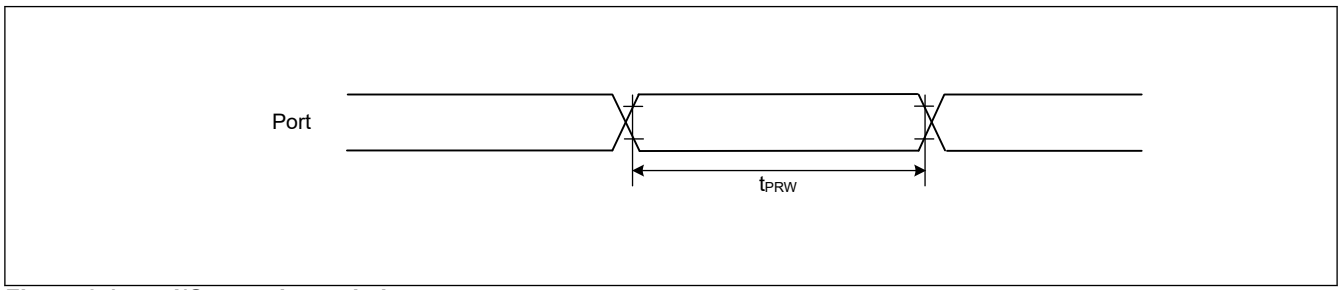


Figure 2.15 I/O ports input timing

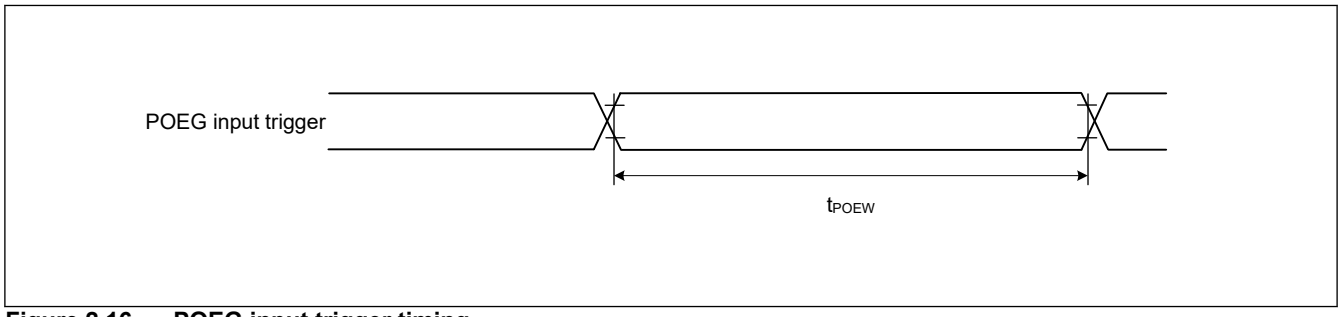


Figure 2.16 POEG input trigger timing

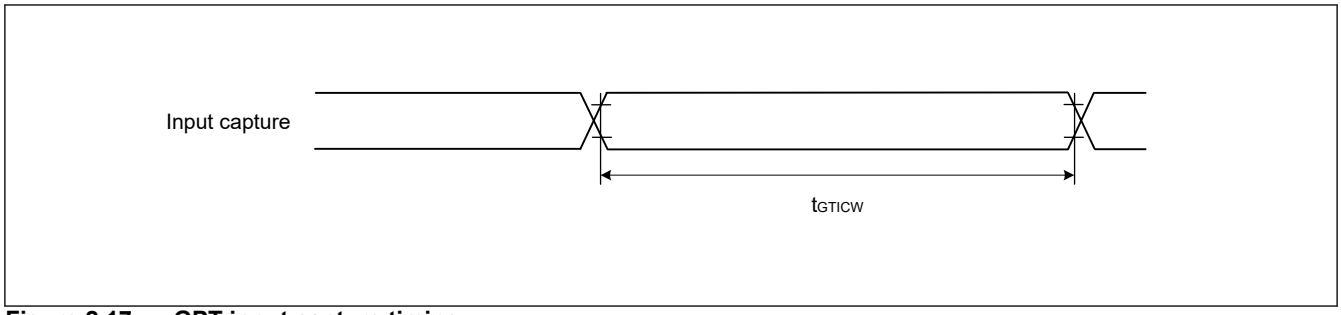


Figure 2.17 GPT input capture timing

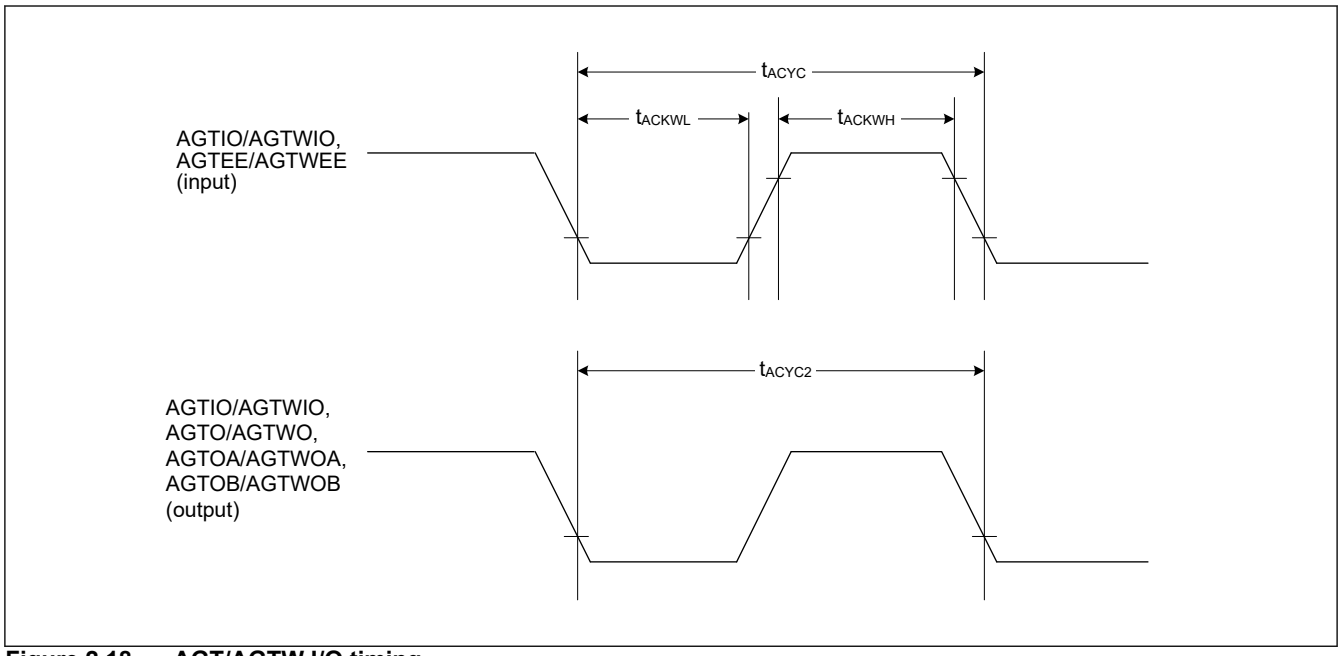


Figure 2.18 AGT/AGTW I/O timing

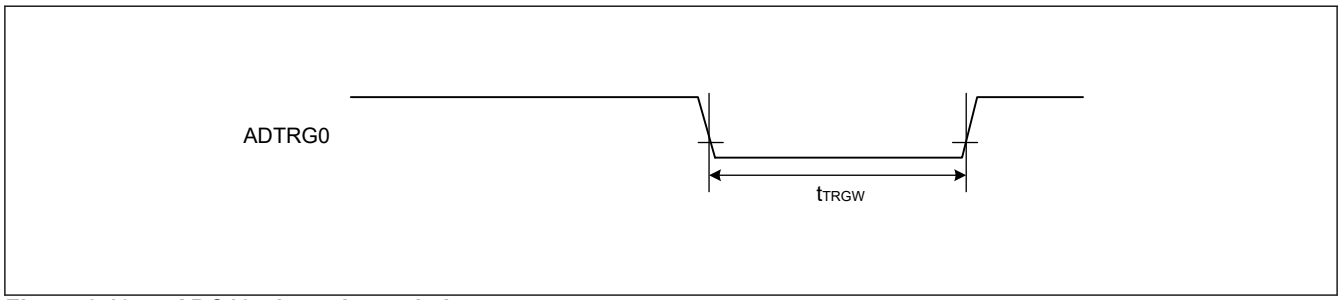


Figure 2.19 ADC12 trigger input timing

2.3.7 CAC Timing

Table 2.30 CAC timing

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	t_{Pcyc}*1 ≤ t_{CAC}*2	t_{CACREF}	4.5 × t_{CAC} + 3 × t_{Pcyc}	—	—	ns	—
		t_{Pcyc}*1 > t_{CAC}*2		5 × t_{CAC} + 6.5 × t_{Pcyc}	—	—	ns	

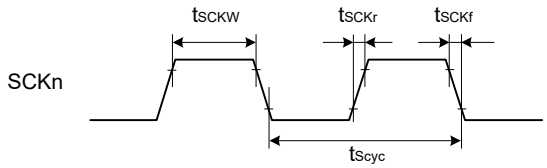
Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. t_{CAC}: CAC count clock source cycle.

2.3.8 SCI Timing

Table 2.31 SCI timing (1)

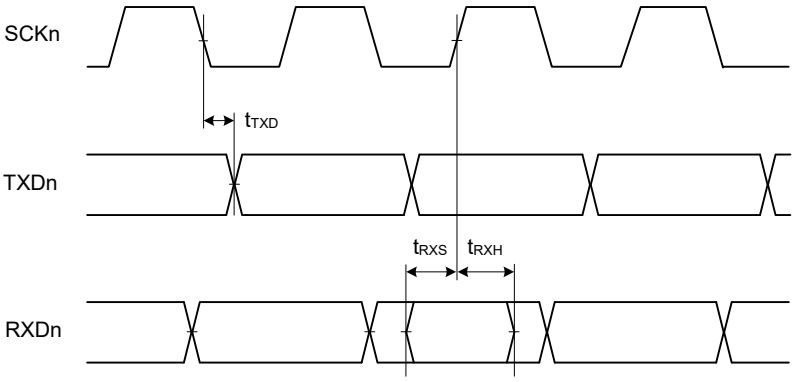
Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit	Test conditions
SCI	Input clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	125	—	ns	Figure 2.20
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{Scyc}	187.5	—	ns	
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
		Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		125	—		
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKr}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Output clock fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Transmit data delay time (master)	Clock synchronous	1.8 V ≤ VCC ≤ 5.5 V	t_{TXD}	—	40	ns	Figure 2.21
			1.6 V ≤ VCC < 1.8 V		—	45		
	Transmit data delay time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		—	55	ns	
			2.4 V ≤ VCC < 2.7 V		—	60		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Receive data setup time (master)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V	t_{RXS}	45	—	ns	
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		90	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
	Receive data setup time (slave)	Clock synchronous	2.7 V ≤ VCC ≤ 5.5 V		40	—	ns	
			1.6 V ≤ VCC < 2.7 V		45	—		
	Receive data hold time (master)	Clock synchronous		t_{RXH}	5	—	ns	
	Receive data hold time (slave)	Clock synchronous		t_{RXH}	40	—	ns	



Note: n = 0 to 3, 9

Figure 2.20 SCK clock input timing



Note: n = 0 to 3, 9

Figure 2.21 SCI input/output timing in clock synchronous mode

Table 2.32 SCI timing (2) (1 of 2)

Conditions: VCC = AVCC = 1.6 to 5.5 V

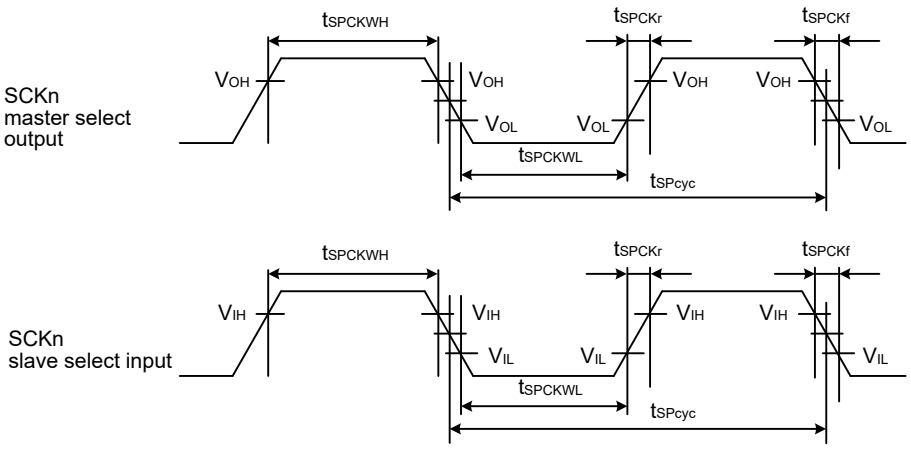
Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	SCK clock cycle output (master)		2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	125	—	ns	Figure 2.22
			2.4 V ≤ VCC < 2.7 V		250	—		
			1.8 V ≤ VCC < 2.4 V		500	—		
			1.6 V ≤ VCC < 1.8 V		1000	—		
	SCK clock cycle input (slave)		2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	SCK clock high pulse width			t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width			t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		1.8 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SU}	45	—	ns	Figure 2.23 to Figure 2.26
			2.4 V ≤ VCC < 2.7 V		55	—		
			1.8 V ≤ VCC < 2.4 V		80	—		
			1.6 V ≤ VCC < 1.8 V		110	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		40	—		
			1.6 V ≤ VCC < 2.7 V		45	—		
	Data input hold time	Master		t_H	33.3	—	ns	
		Slave			40	—		
	SS input setup time			t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time			t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{OD}	—	40	ns	
			1.6 V ≤ VCC < 1.8 V		—	50		
		Slave	2.4 V ≤ VCC ≤ 5.5 V		—	65		
			1.8 V ≤ VCC < 2.4 V		—	100		
			1.6 V ≤ VCC < 1.8 V		—	125		
	Data output hold time	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{OH}	-10	—	ns	
			2.4 V ≤ VCC < 2.7 V		-20	—		
			1.8 V ≤ VCC < 2.4 V		-30	—		
			1.6 V ≤ VCC < 1.8 V		-40	—		
		Slave			-10	—		
	Data rise and fall time	Master	1.8 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	20	ns	
			1.6 V ≤ VCC < 1.8 V		—	30		
		Slave	1.8 V ≤ VCC ≤ 5.5 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		

Table 2.32 SCI timing (2) (2 of 2)

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter				Symbol	Min	Max	Unit*1	Test conditions
Simple SPI	Slave access time	2.4 V ≤ VCC ≤ 5.5 V		t_{SA}	—	6	t_{Pcyc}	Figure 2.26
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		
	Slave output release time	2.4 V ≤ VCC ≤ 5.5 V		t_{REL}	—	6	t_{Pcyc}	
		1.8 V ≤ VCC < 2.4 V	24 MHz ≤ PCLKB ≤ 32 MHz		—	7		
			PCLKB < 24 MHz		—	6		
		1.6 V ≤ VCC < 1.8 V			—	6		

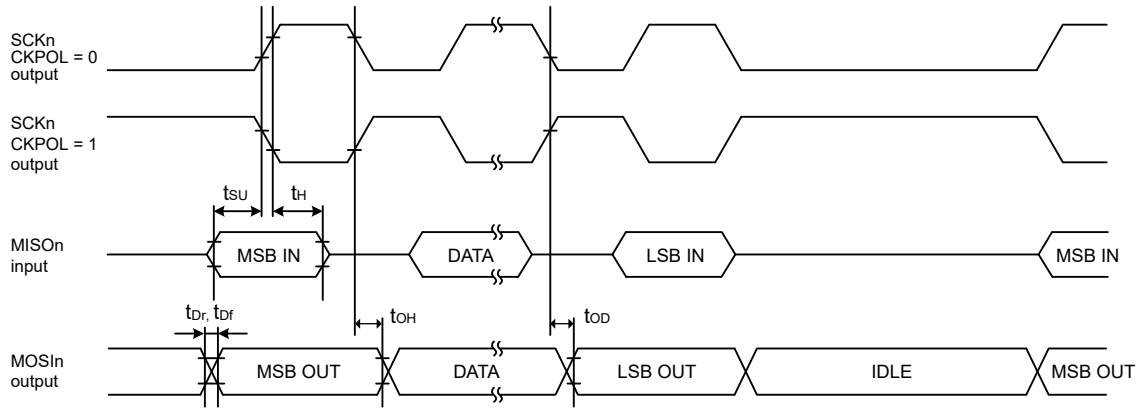
Note 1. t_{Pcyc}: PCLKB cycle.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

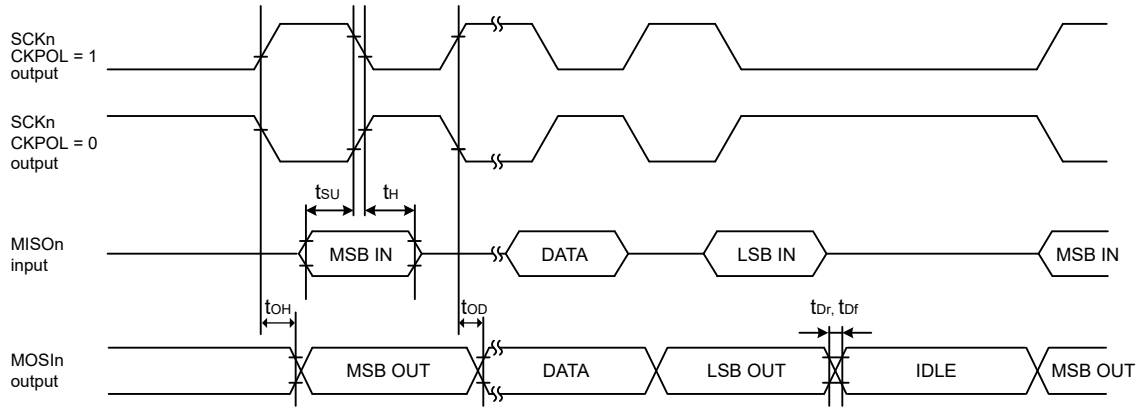
Note: n = 0 to 3, 9

Figure 2.22 SCI simple SPI mode clock timing



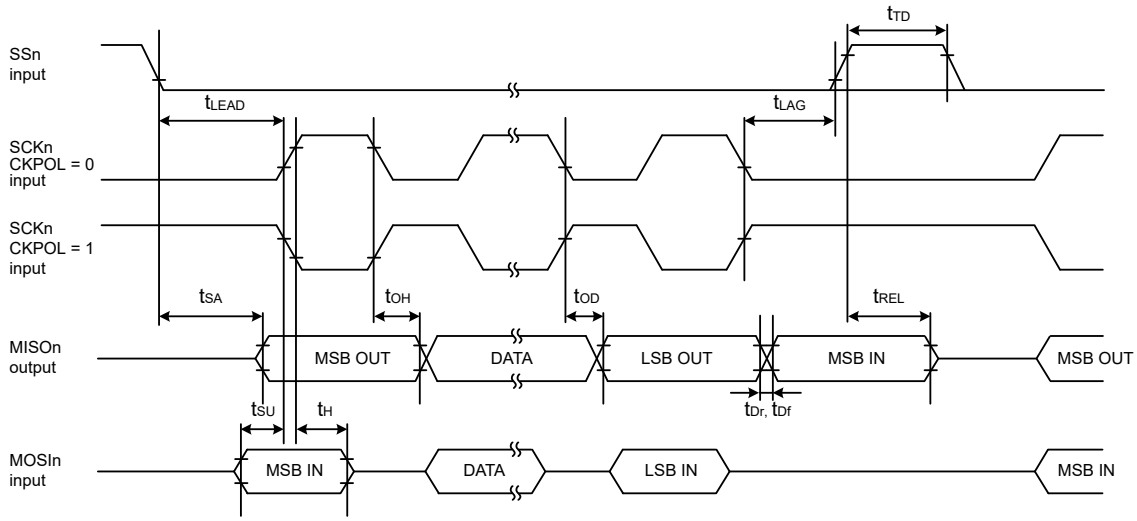
Note: n = 0 to 3, 9

Figure 2.23 SCI simple SPI mode timing (master, CKPH = 1)



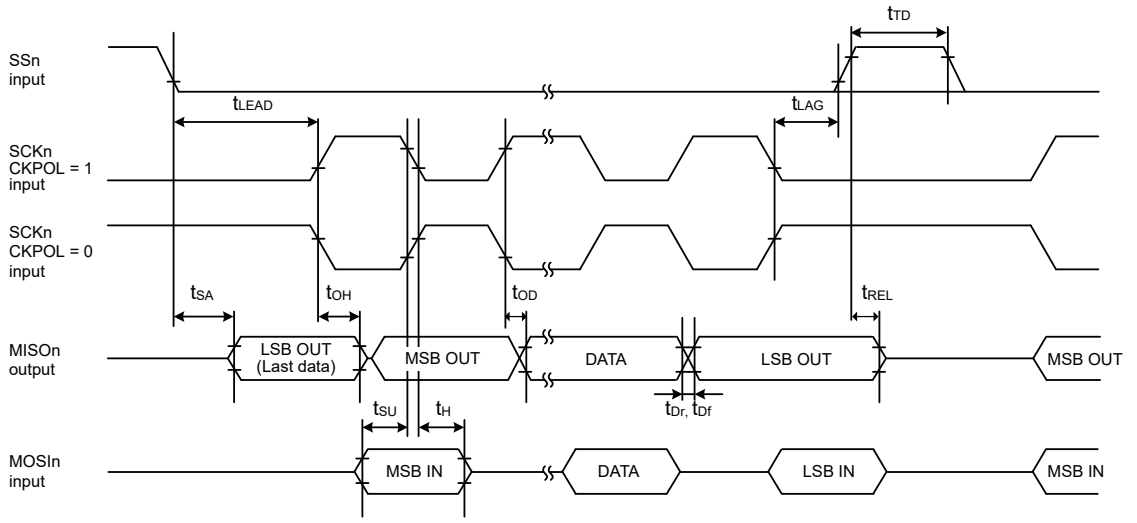
Note: n = 0 to 3, 9

Figure 2.24 SCI simple SPI mode timing (master, CKPH = 0)



Note: n = 0 to 3, 9

Figure 2.25 SCI simple SPI mode timing (slave, CKPH = 1)



Note: n = 0 to 3, 9

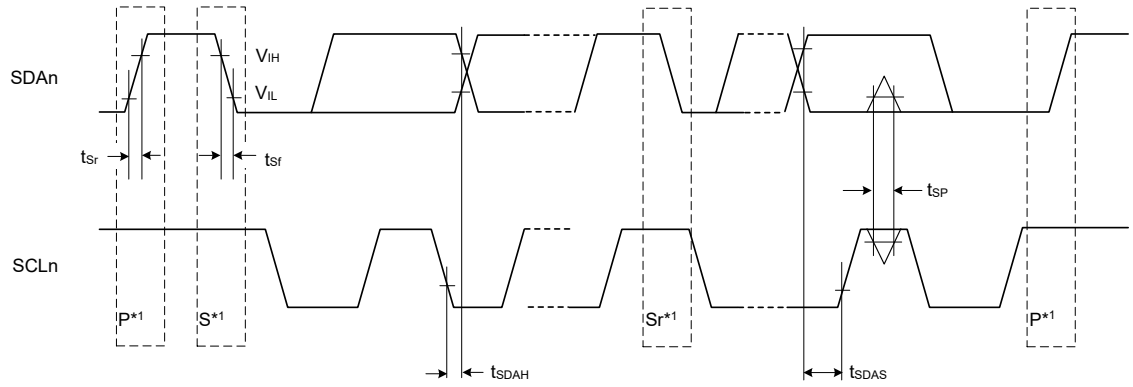
Figure 2.26 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.33 SCI timing (3)

Conditions: VCC = AVCC = 2.7 to 5.5 V

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	—	1000	ns	Figure 2.27
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	—	300	ns	Figure 2.27
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc} *1	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b *2	—	400	pF	

Note 1. t_{IICcyc}: Clock cycle selected by the SMR.CKS[1:0] bits.
Note 2. C_b indicates the total capacity of the bus line.



Test conditions:
V_{IH} = VCC × 0.7, V_{IL} = VCC × 0.3
V_{OL} = 0.6 V, I_{OL} = 6 mA

Note: n = 0 to 3, 9
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 2.27 SCI simple IIC mode timing

2.3.9 SPI Timing

Table 2.34 SPI timing (1 of 3)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	RSPCK clock cycle	Master	2.7 V ≤ VCC ≤ 5.5 V	t_{SPcyc}	62.5	—	ns	Figure 2.28 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		125	—		
			1.8 V ≤ VCC < 2.4 V		250	—		
			1.6 V ≤ VCC < 1.8 V		500	—		
		Slave	2.7 V ≤ VCC ≤ 5.5 V		187.5	—		
			2.4 V ≤ VCC < 2.7 V		375	—		
			1.8 V ≤ VCC < 2.4 V		750	—		
			1.6 V ≤ VCC < 1.8 V		1500	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$3 \times t_{Pcyc}$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave			$3 \times t_{Pcyc}$	—		
	RSPCK clock rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC ≤ 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	0.1	µs/V	

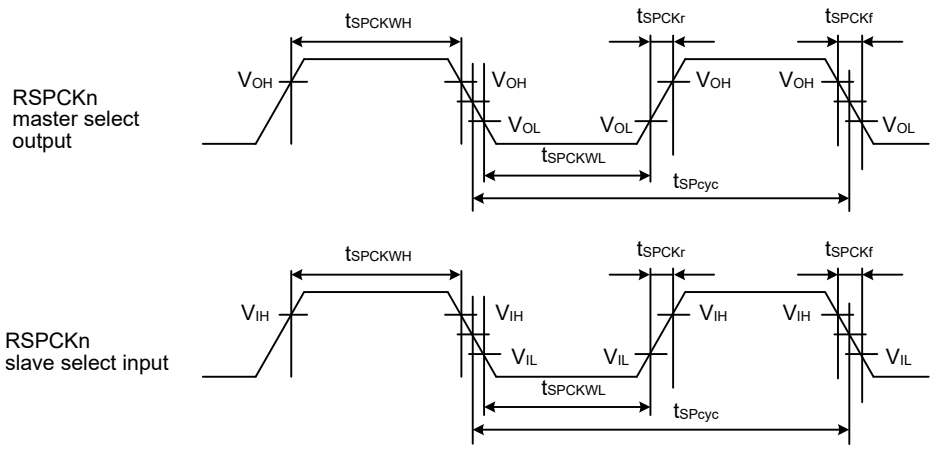
Table 2.34 SPI timing (2 of 3)

Parameter					Symbol	Min	Max	Unit*1	Test conditions
SPI	Data input setup time	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{SU}	10	—	ns	Figure 2.29 to Figure 2.34 C = 30 pF
			2.4 V ≤ VCC < 2.7 V	16 MHz < PCLKB ≤ 32 MHz		30	—		
				PCLKB ≤ 16 MHz		10	—		
			1.8 V ≤ VCC < 2.4 V	16 MHz < PCLKB ≤ 32 MHz		55	—		
				8 MHz < PCLKB ≤ 16 MHz		30	—		
				PCLKB ≤ 8 MHz		10	—		
			1.6 V ≤ VCC < 1.8 V			10	—		
		Slave	2.4 V ≤ VCC ≤ 5.5 V			10	—		
			1.8 V ≤ VCC < 2.4 V			15	—		
			1.6 V ≤ VCC < 1.8 V			20	—		
	Data input hold time	Master (RSPCK is PCLKB/2)			t_{HF}	0	—	ns	
		Master (RSPCK is not PCLKB/2)			t_{H}	t_{Pcyc}	—		
		Slave			t_{H}	20	—		
SPI	SSL setup time	Master	1.8 V ≤ VCC ≤ 5.5 V		t_{LEAD}	-30 + N × t_{SPcyc} *2	—	ns	
			1.6 V ≤ VCC < 1.8 V			-50 + N × t_{SPcyc} *2	—		
		Slave				6 × t_{Pcyc}	—	ns	
	SSL hold time	Master			t_{LAG}	-30 + N × t_{SPcyc} *3	—	ns	
		Slave				6 × t_{Pcyc}	—	ns	
	Data output delay time	Master	2.7 V ≤ VCC ≤ 5.5 V		t_{OD}	—	14	ns	
			2.4 V ≤ VCC < 2.7 V			—	20		
			1.8 V ≤ VCC < 2.4 V			—	25		
			1.6 V ≤ VCC < 1.8 V			—	30		
		Slave	2.7 V ≤ VCC ≤ 5.5 V			—	50		
			2.4 V ≤ VCC < 2.7 V			—	60		
			1.8 V ≤ VCC < 2.4 V			—	85		
			1.6 V ≤ VCC < 1.8 V			—	110		
	Data output hold time	Master			t_{OH}	0	—	ns	
		Slave				0	—		
	Successive transmission delay time	Master			t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave				6 × t_{Pcyc}	—		

Table 2.34 SPI timing (3 of 3)

Parameter				Symbol	Min	Max	Unit*1	Test conditions
SPI	MOSI and MISO rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{Dr}, t_{Df}	—	10	ns	Figure 2.29 to Figure 2.34 C = 30 pF
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	SSL rise and fall time	Output	2.7 V ≤ VCC ≤ 5.5 V	t_{SSLr}, t_{SSLf}	—	10	ns	
			2.4 V ≤ VCC < 2.7 V		—	15		
			1.8 V ≤ VCC < 2.4 V		—	20		
			1.6 V ≤ VCC < 1.8 V		—	30		
		Input			—	1	µs	
	Slave access time		2.4 V ≤ VCC ≤ 5.5 V	t_{SA}	—	2 × t_{Pcyc} + 100	ns	Figure 2.33 and Figure 2.34 C = 30 pF
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		
	Slave output release time		2.4 V ≤ VCC ≤ 5.5 V	t_{REL}	—	2 × t_{Pcyc} + 100	ns	
			1.8 V ≤ VCC < 2.4 V		—	2 × t_{Pcyc} + 140		
			1.6 V ≤ VCC < 1.8 V		—	2 × t_{Pcyc} + 180		

Note 1. t_{Pcyc}: PCLKB cycle.
Note 2. N is set as an integer from 1 to 8 by the SPCKD register.
Note 3. N is set as an integer from 1 to 8 by the SSLND register.



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Note: n = A

Figure 2.28 SPI clock timing

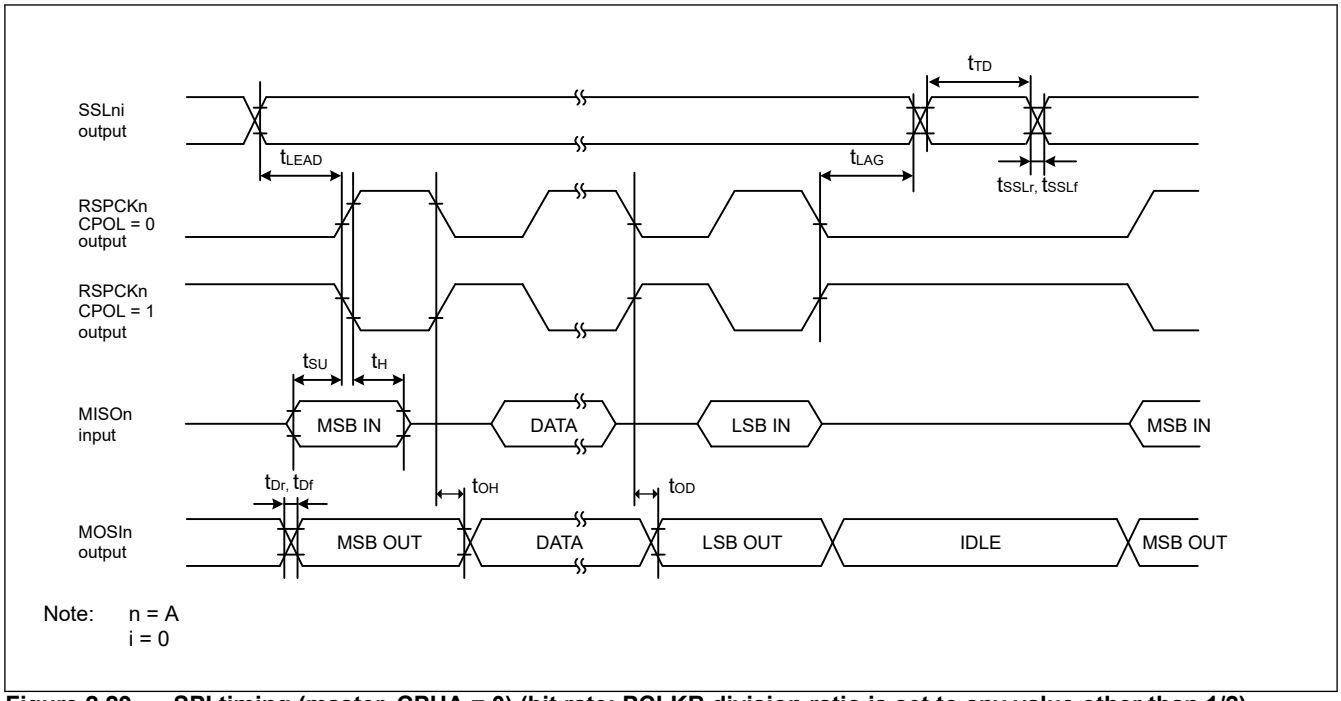


Figure 2.29 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to any value other than 1/2)

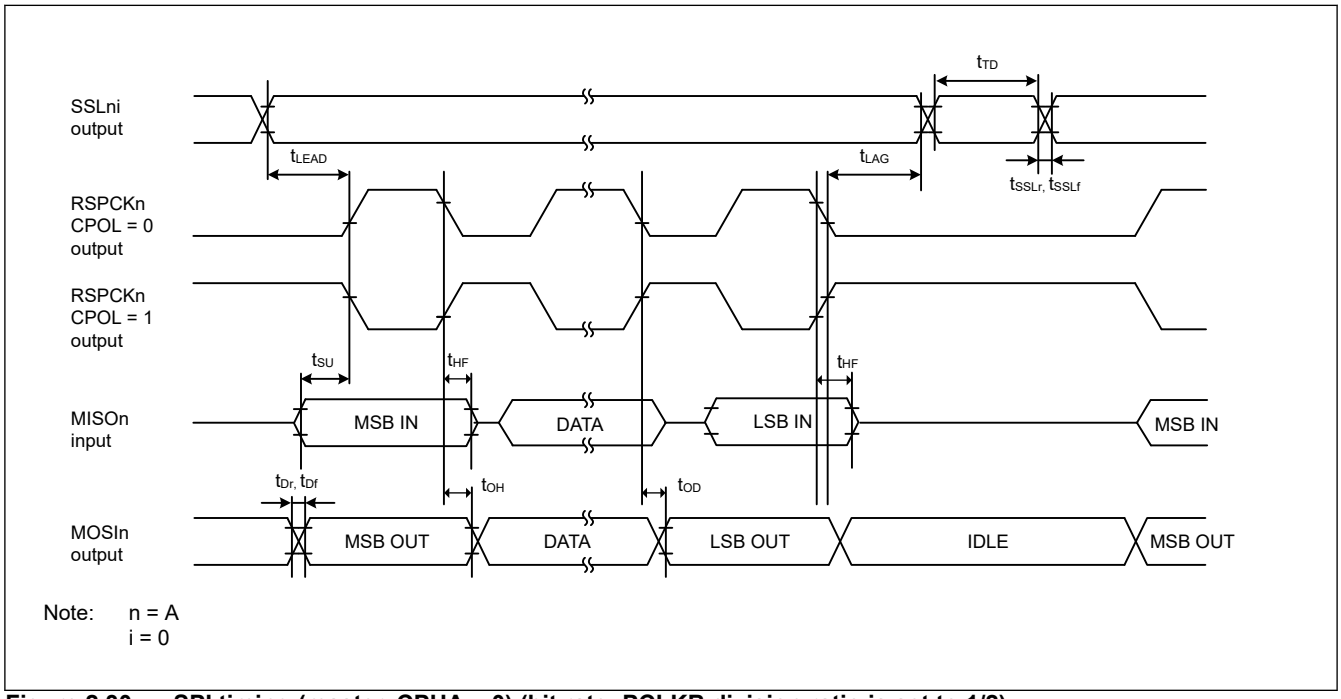


Figure 2.30 SPI timing (master, CPHA = 0) (bit rate: PCLKB division ratio is set to 1/2)

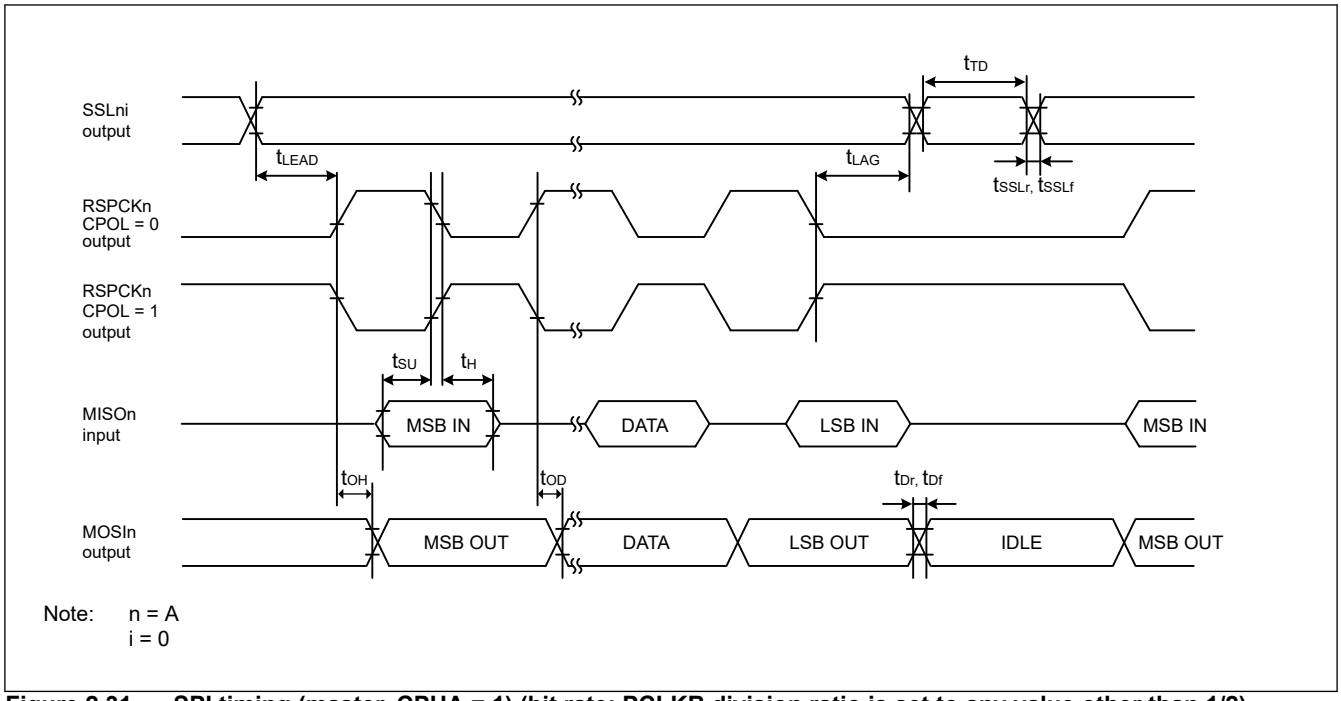


Figure 2.31 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to any value other than 1/2)

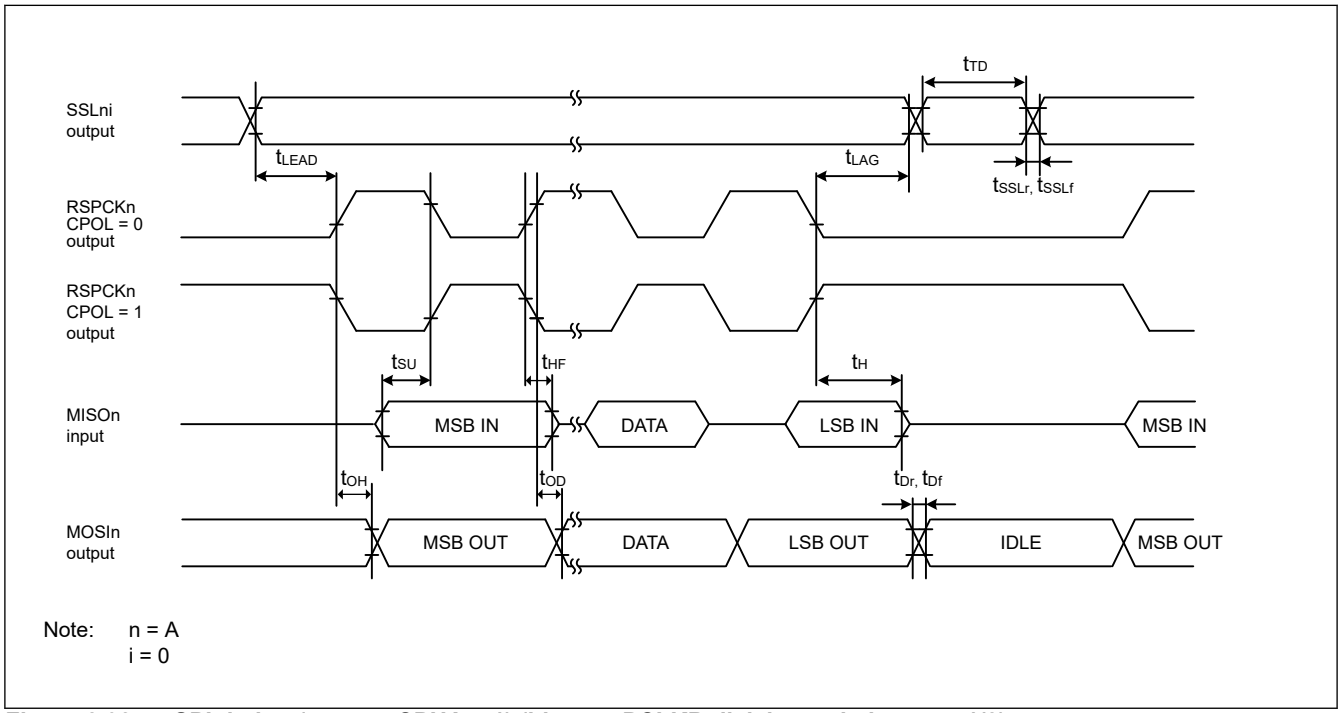


Figure 2.32 SPI timing (master, CPHA = 1) (bit rate: PCLKB division ratio is set to 1/2)

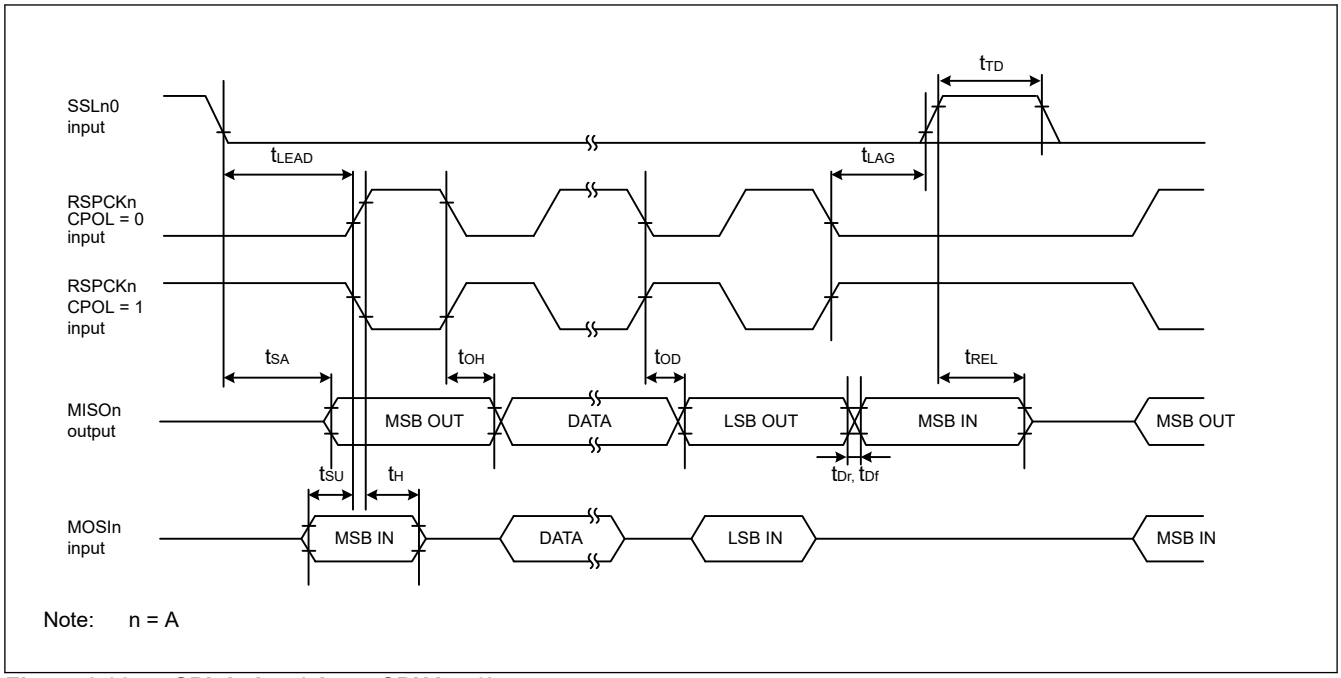


Figure 2.33 SPI timing (slave, CPHA = 0)

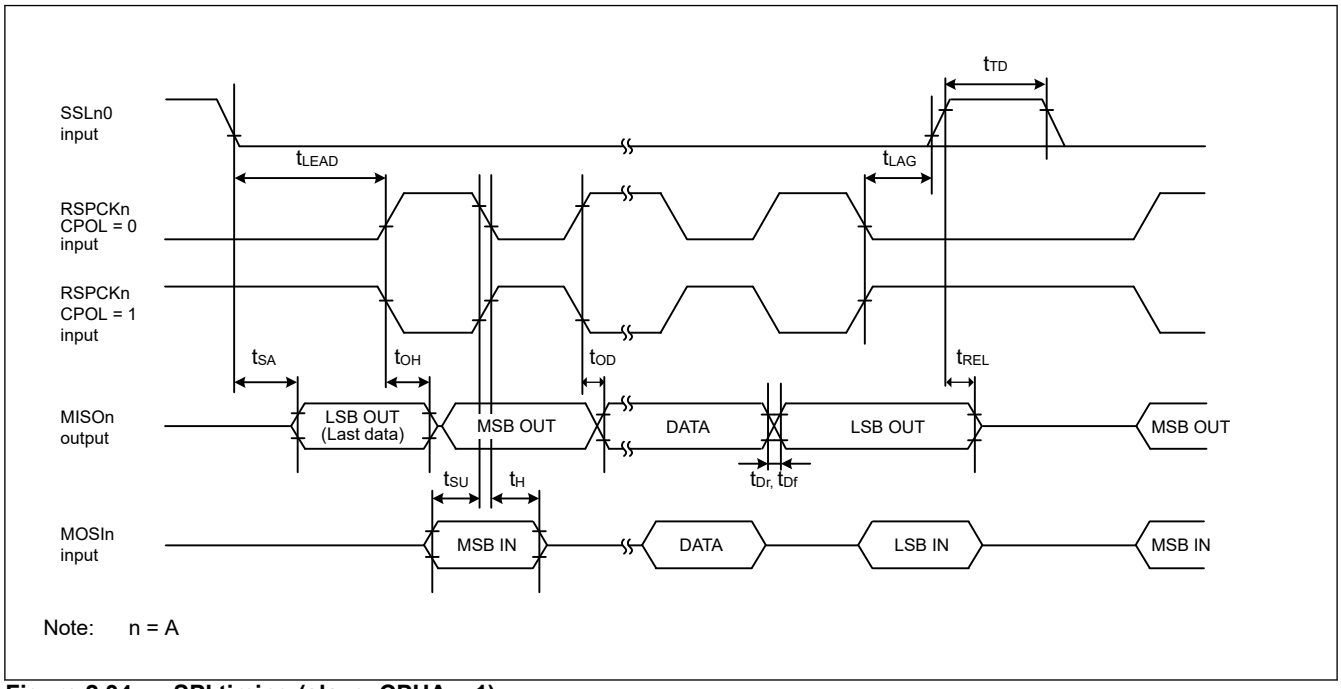


Figure 2.34 SPI timing (slave, CPHA = 1)

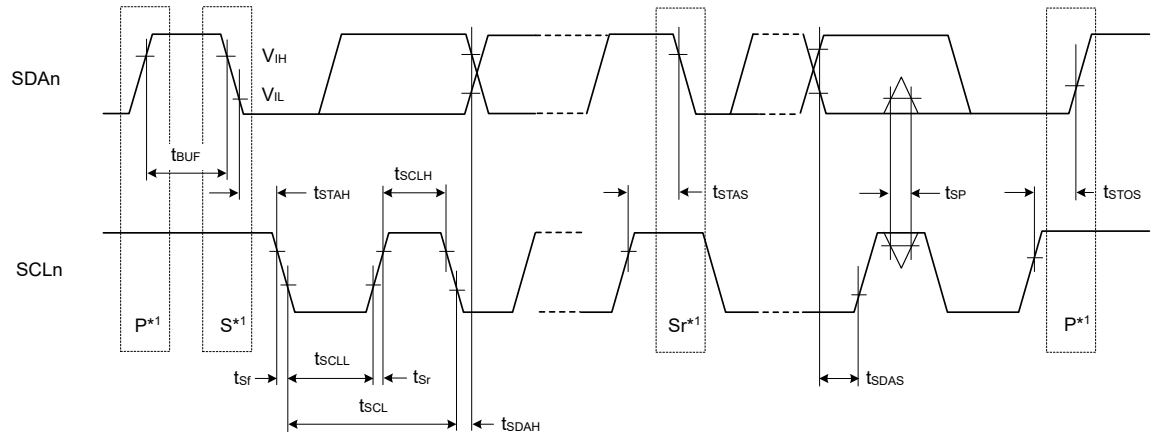
2.3.10 IIC Timing

Table 2.35 IIC timing

Conditions: VCC = AVCC = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 2.35
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (when wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time (when wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	—	ns	
	START condition input hold time (when wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time (when wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 2.35
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	300	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc}+ 300	—	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	t_{IICcyc} + 300	—	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.



Note: n = 0, 1
Note 1. S, P, and Sr indicate the following conditions:
S: Start condition
P: Stop condition
Sr: Restart condition

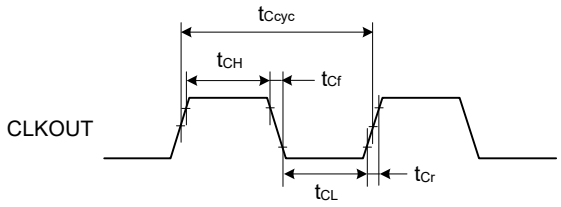
Figure 2.35 I^2C bus interface input/output timing

2.3.11 CLKOUT Timing

Table 2.36 CLKOUT timing

Parameter			Symbol	Min	Max	Unit	Test conditions
CLKOUT	CLKOUT pin output cycle*1	2.7 V ≤ VCC ≤ 5.5 V	t_{Ccyc}	62.5	—	ns	Figure 2.36
		1.8 V ≤ VCC < 2.7 V		125	—		
		1.6 V ≤ VCC < 1.8 V		250	—		
	CLKOUT pin high pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CH}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin low pulse width*2	2.7 V ≤ VCC ≤ 5.5 V	t_{CL}	15	—	ns	
		1.8 V ≤ VCC < 2.7 V		30	—		
		1.6 V ≤ VCC < 1.8 V		150	—		
	CLKOUT pin output rise time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cr}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		
	CLKOUT pin output fall time	2.7 V ≤ VCC ≤ 5.5 V	t_{Cf}	—	12	ns	
		1.8 V ≤ VCC < 2.7 V		—	25		
		1.6 V ≤ VCC < 1.8 V		—	50		

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, specifications in Table 2.36 should be satisfied with 45% to 55% of input duty cycle.
Note 2. When MOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 001b), set the clock output division ratio to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).



Test conditions: V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 2.36 CLKOUT output timing

2.4 ADC12 Characteristics

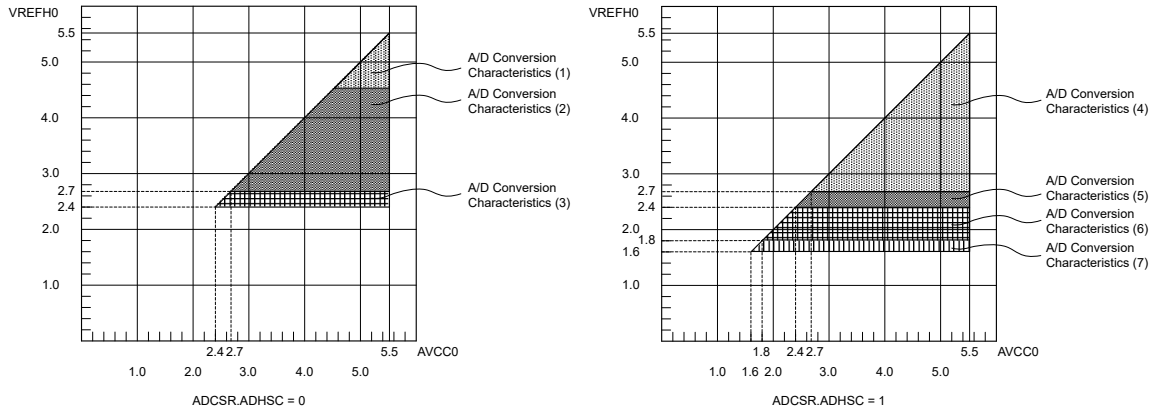


Figure 2.37 AVCC to VREFH0 voltage range

Table 2.37 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC = VREFH0 = 4.5 to 5.5 V*5, VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	64	MHz	ADACSR.ADSAC = 0
				48	MHz	ADACSR.ADSAC = 1
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
Analog input resistance	Rs	—	—	1.3*3	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70 (0.211)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0D ADACSR.ADSAC = 0

Table 2.37 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC = VREFH0 = 4.5 to 5.5 V[*5], VSS = AVSS0 = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time[*1] (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.0	±4.5	LSB	High-precision channel
Full-scale error		—	±1.0	±4.5	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±5.0	LSB	High-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC and VREFH0, it should be added ±0.5 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.38 A/D conversion characteristics (2) in high-speed A/D conversion mode

Conditions: VCC = AVCC = VREFH0 = 2.7 to 5.5 V[*5], VSS = AVSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	48	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
Analog input resistance	Rs	—	—	1.9[*3]	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.5	LSB	High-precision channel
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±6.0	LSB	High-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC and VREFH0, it should be added ±0.5 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.39 A/D conversion characteristics (3) in high-speed A/D conversion mode

Conditions: VCC = AVCC = VREFH0 = 2.4 to 5.5 V*5, VSS = AVSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min		Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	32	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
Analog input resistance	Rs	—	—	2.2*3	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.00 (0.328)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.5	LSB	High-precision channel
Full-scale error		—	±1.0	±5.5	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.50	±6.0	LSB	High-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC and VREFH0, it should be added ±0.5 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.40 A/D conversion characteristics (4) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC = VREFH0 = 2.7 to 5.5 V*5, VSS = AVSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	24	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 2.40 A/D conversion characteristics (4) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC = VREFH0 = 2.7 to 5.5 V[*5], VSS = AVSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time[*1] (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	1.58 (0.438)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.25	±6.0	LSB	High-precision channel
Full-scale error		—	±1.0	±6.0	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±7.0	LSB	High-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC and VREFH0, it should be added ±0.5 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.41 A/D conversion characteristics (5) in low-power A/D conversion mode

Conditions: VCC = AVCC = VREFH0 = 2.4 to 5.5 V[*5], VSS = AVSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	16	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
Analog input resistance	Rs	—	—	2.2[*3]	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	2.38 (0.656)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.25	±6.0	LSB	High-precision channel
Full-scale error		—	±1.0	±6.0	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±7.0	LSB	High-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC and VREFH0, it should be added ±0.5 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.42 A/D conversion characteristics (6) in low-power A/D conversion mode

Conditions: VCC = AVCC = VREFH0 = 1.8 to 5.5 V[*5] , VSS = AVSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	8	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
Analog input resistance	Rs	—	—	6[*3]	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	4.75 (1.313)[*4]	—	—	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.5	LSB	High-precision channel
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.0	±9.5	LSB	High-precision channel
DNL differential nonlinearity error		—	±1.25	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC and VREFH0, it should be added ±0.5 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.43 A/D conversion characteristics (7) in low-power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC = VREFH0 = 1.6 to 5.5 V[*5], VSS = AVSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	4	MHz	—
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
Analog input resistance	Rs	—	—	12[*3]	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	VREFH0	V	—
Resolution		—	—	12	Bit	—

Table 2.43 A/D conversion characteristics (7) in low-power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC = VREFH0 = 1.6 to 5.5 V[*5], VSS = AVSS = VREFL0 = 0 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time[*1] (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	9.5 (2.625)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.5	LSB	High-precision channel
Full-scale error		—	±1.5	±7.5	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±9.5	LSB	High-precision channel
DNL differential nonlinearity error		—	±3.5	—	LSB	—
INL integral nonlinearity error		—	±2.25	±3.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.
Note 5. When VREFH0 < AVCC, the MAX. values are as follows.
Absolute accuracy/Offset error/Full-scale error:
For voltage difference between AVCC and VREFH0, it should be added ±0.5 LSB/V to the Max spec.
INL integral non-linearity error:
For voltage difference between AVCC and VREFH0, it should be added ±0.2 LSB/V to the Max spec.

Table 2.44 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC = 2.7 to 5.5 V, VSS = AVSS = 0 V
Reference voltage range applied to the AVCC and AVSS.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	64	MHz	ADACSR.ADSAC = 0
				48	MHz	ADACSR.ADSAC = 1
Analog input capacitance[*2]	Cs	—	—	9[*3]	pF	High-precision channel
Analog input resistance	Rs	—	—	1.3[*3]	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	AVCC	V	—
Resolution		—	—	12	Bit	—
Conversion time[*1] (Operation at PCLKD = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.70 (0.211)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0D ADACSR.ADSAC = 0
Conversion time[*1] (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)[*4]	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.0	±5.0	LSB	High-precision channel
Full-scale error		—	±1.0	±5.0	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±5.5	LSB	High-precision channel

Table 2.44 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC = 2.7 to 5.5 V, VSS = AVSS = 0 V
Reference voltage range applied to the AVCC and AVSS.

Parameter	Min	Typ	Max	Unit	Test conditions
DNL differential nonlinearity error	—	±1.0	—	LSB	—
INL integral nonlinearity error	—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.

Table 2.45 A/D conversion characteristics (2) in high-speed A/D conversion mode

Conditions: VCC = AVCC = 2.7 to 5.5 V, VSS = AVSS = 0 V
Reference voltage range applied to the AVCC and AVSS.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	48	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	AVCC	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.67 (0.219)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.0	±6.5	LSB	High-precision channel
Full-scale error		—	±1.0	±6.5	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.5	±7.0	LSB	High-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.

Table 2.46 A/D conversion characteristics (3) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V
Reference voltage range applied to the AVCC and AVSS.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	32	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
Analog input resistance	Rs	—	—	2.2*3	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	AVCC	V	—
Resolution		—	—	12	Bit	—

Table 2.46 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V
Reference voltage range applied to the AVCC and AVSS.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.00 (0.328)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.0	±6.5	LSB	High-precision channel
Full-scale error		—	±1.0	±6.5	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±2.50	±7.0	LSB	High-precision channel
DNL differential nonlinearity error		—	±1.0	—	LSB	—
INL integral nonlinearity error		—	±1.5	±3.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.

Table 2.47 A/D conversion characteristics (4) in low-power A/D conversion mode

Conditions: VCC = AVCC = 2.7 to 5.5 V, VSS = AVSS = 0 V
Reference voltage range applied to the AVCC and AVSS.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	24	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
Analog input resistance	Rs	—	—	1.9*3	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	AVCC	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	1.58 (0.438)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.0	LSB	High-precision channel
Full-scale error		—	±1.25	±7.0	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.25	±8.0	LSB	High-precision channel
DNL differential nonlinearity error		—	±1.5	—	LSB	—
INL integral nonlinearity error		—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.

Table 2.48 A/D conversion characteristics (5) in low-power A/D conversion mode

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V
Reference voltage range applied to the AVCC and AVSS.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	16	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
Analog input resistance	Rs	—	—	2.2*3	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	AVCC	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	2.38 (0.656)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.25	±7.0	LSB	High-precision channel
Full-scale error		—	±1.25	±7.0	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.25	±8.0	LSB	High-precision channel
DNL differential nonlinearity error		—	±1.5	—	LSB	—
INL integral nonlinearity error		—	±1.75	±4.0	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.

Table 2.49 A/D conversion characteristics (6) in low-power A/D conversion mode

Conditions: VCC = AVCC = 1.8 to 5.5 V, VSS = AVSS = 0 V
Reference voltage range applied to the AVCC and AVSS.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	8	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
Analog input resistance	Rs	—	—	6*3	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	AVCC	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	4.75 (1.313)*4	—	—	µs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.25	±8.5	LSB	High-precision channel
Full-scale error		—	±1.5	±8.5	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±10.5	LSB	High-precision channel
DNL differential nonlinearity error		—	±2.0	—	LSB	—
INL integral nonlinearity error		—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.

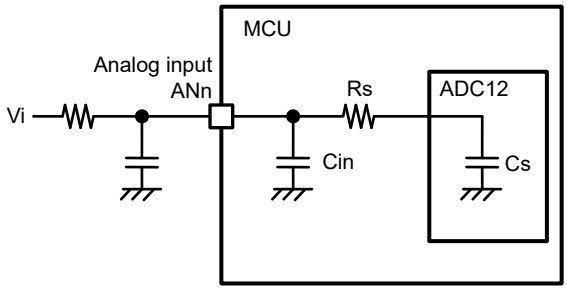
Table 2.50 A/D conversion characteristics (7) in low-power A/D conversion mode

Conditions: VCC = AVCC = 1.6 to 5.5 V, VSS = AVSS = 0 V
Reference voltage range applied to the AVCC and AVSS.

Parameter		Min	Typ	Max	Unit	Test conditions
PCLKD (ADCLK) frequency		1	—	4	MHz	—
Analog input capacitance*2	Cs	—	—	9*3	pF	High-precision channel
Analog input resistance	Rs	—	—	12*3	kΩ	High-precision channel
Analog input voltage range	Ain	0	—	AVCC	V	—
Resolution		—	—	12	Bit	—
Conversion time*1 (Operation at PCLKD = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	9.5 (2.625)*4	—	—	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0x0A ADACSR.ADSAC = 1
Offset error		—	±1.25	±8.5	LSB	High-precision channel
Full-scale error		—	±1.5	±8.5	LSB	High-precision channel
Quantization error		—	±0.5	—	LSB	—
Absolute accuracy		—	±3.75	±10.5	LSB	High-precision channel
DNL differential nonlinearity error		—	±2.0	—	LSB	—
INL integral nonlinearity error		—	±2.25	±4.5	LSB	—

Note: The characteristics apply when no pin functions other than 12-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.
Note 2. Except for I/O input capacitance (Cin), see section 2.2.4. I/O VOH, VOL, and Other Characteristics.
Note 3. Reference data.
Note 4. ( ) lists sampling time.

Figure 2.38 shows the equivalent circuit for analog input.



Note: Terminal leakage current is not shown in this figure.

Figure 2.38 Equivalent circuit for analog input

Table 2.51 12-bit A/D converter channel classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN003	AVCC = 1.6 to 5.5 V	Pins AN000 to AN003 cannot be used as general I/O, TS transmission, when the A/D converter is in use.
Internal reference voltage input channel	Internal reference voltage	AVCC = 1.8 to 5.5 V	—
Temperature sensor input channel	Temperature sensor output	AVCC = 1.8 to 5.5 V	—

Table 2.52 A/D internal reference voltage characteristics

Conditions: VCC = AVCC = VREFH0 = 1.8 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.42	1.48	1.54	V	—
PCLKD (ADCLK) frequency*3	1	—	2	MHz	—
Sampling time*4	5.0	—	—	µs	—

Note 1. The internal reference voltage cannot be selected for input channels when AVCC < 1.8 V.
Note 2. The 12-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 12-bit A/D converter.
Note 3. When the internal reference voltage is selected as the high-potential reference voltage.
Note 4. When the internal reference voltage is converted.

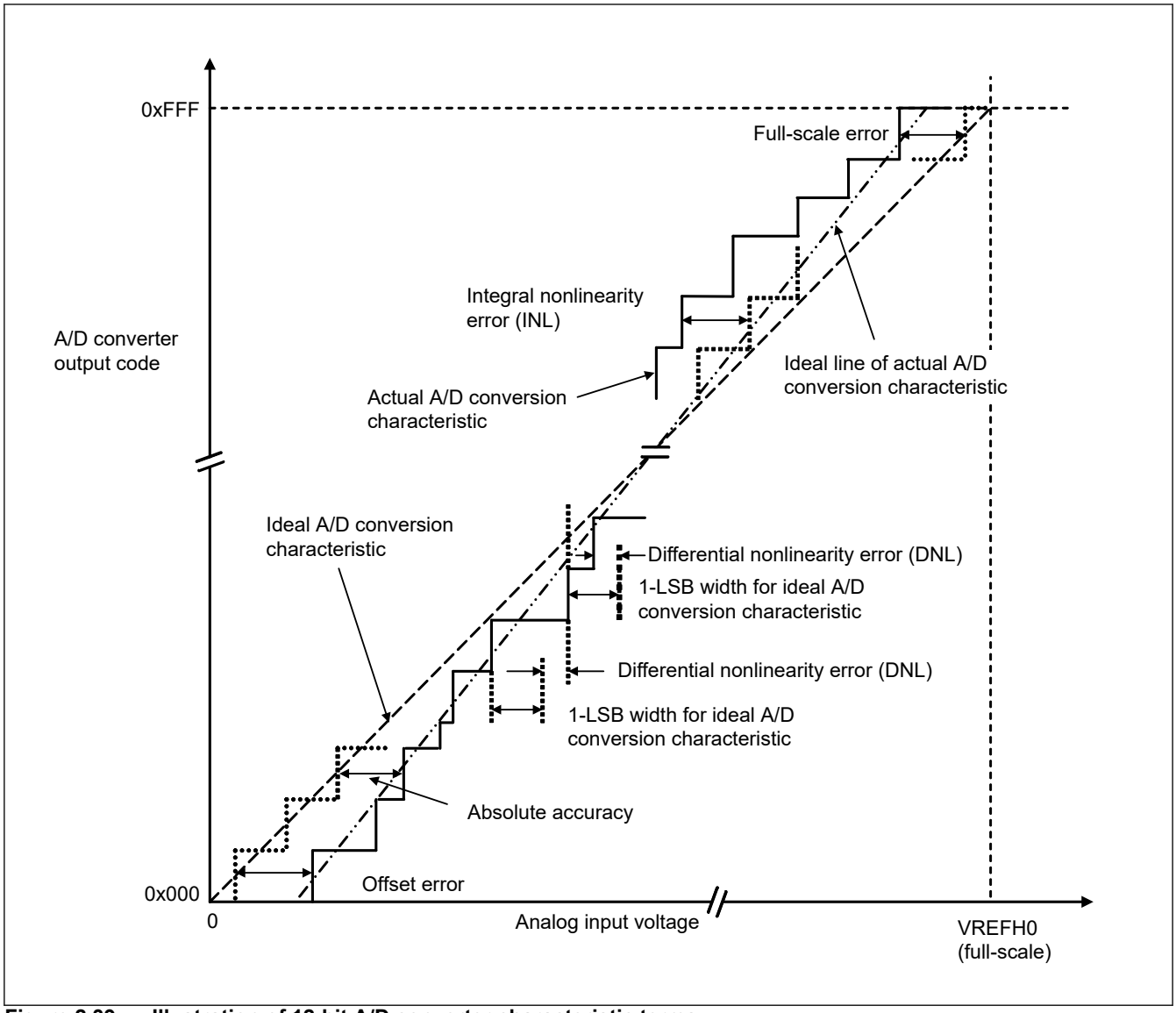


Figure 2.39 Illustration of 12-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 0x003 to 0x00D, though an output code of 0x008 can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.5 SDADC24 Characteristics

2.5.1 Reference Voltage

Table 2.53 Reference voltage characteristics

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Internal reference voltage	V_{AVRTO}	—	0.69	—	V	—
Temperature coefficient for internal reference voltage*1	TC_{BOX}	—	10	—	ppm/°C	0.47 µF capacitor connected to AREGC, AVRT, and AVCM pins
AVCM output voltage	V_{AVCM}	—	0.45	—	V	0.47 µF capacitor connected to AVSS pin

Note 1. This is as stipulated by the BOX method.
Tj = -40 to 120°C after trimming.

$$TC_{BOX} = \frac{1}{V_{min}} \times \frac{V_{max} - V_{min}}{\Delta Ta}$$

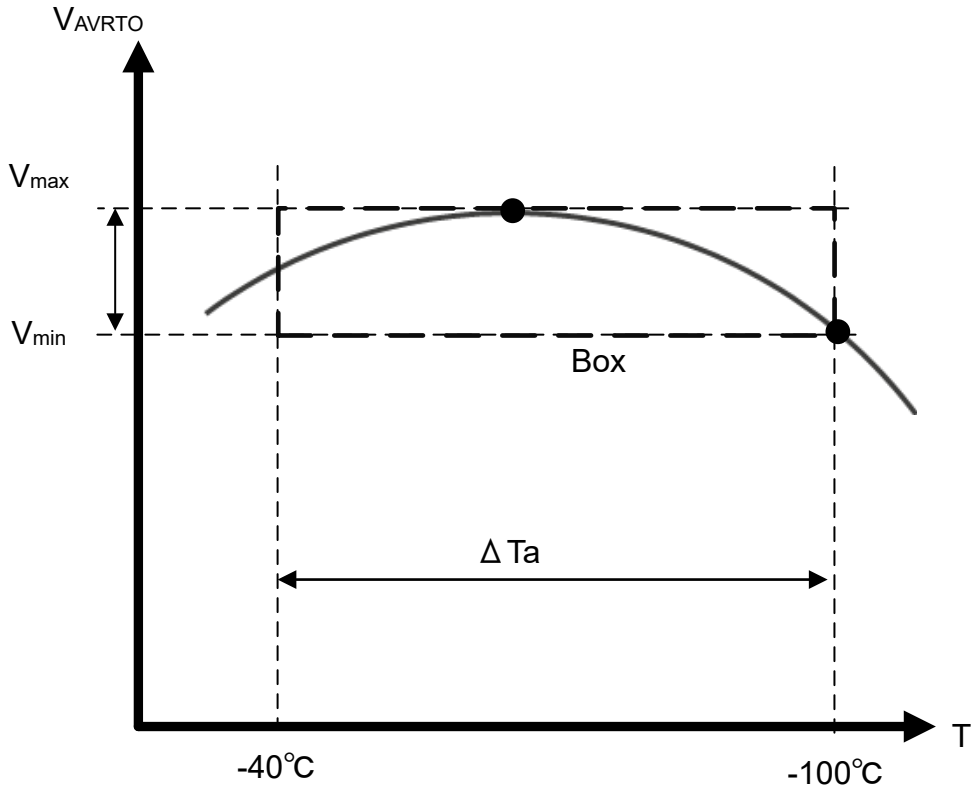


Figure 2.40 Temperature coefficient evaluation using box method

2.5.2 Analog Input

Table 2.54 Analog input characteristics (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage range (differential or Single-ended)*1	V_{AIN}	-500	—	500	mV	x1 gain
		-250	—	250		x2 gain
		-125	—	125		x4 gain
		-62.5	—	62.5		x8 gain
		-31.25	—	31.25		x16 gain
		-15.625	—	15.625		x32 gain

Table 2.54 Analog input characteristics (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input gain	ainGAIN	—	1	—	Times	x1 gain
		—	2	—		x2 gain
		—	4	—		x4 gain
		—	8	—		x8 gain
		—	16	—		x16 gain
		—	32	—		x32 gain
Input impedance	ainRIN	150	360	—	kΩ	Differential voltage
		100	240	—		Single-ended voltage

Note 1. Differential voltage (AINP - AINN), single-ended input AINP, AINN = PGA input common voltage.

2.5.3 4 kHz Sampling Mode (f_{OS} = 1.5 MHz)

Table 2.55 4 kHz sampling mode (f_{OS} = 1.5 MHz) characteristics

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V, ANINn and ANIPn (n = 0 to 6)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating clock (SDADCCLK)*1	f_{SDAD}	—	12	—	MHz	*1
Sampling frequency	f_S	—	3906	—	Hz	*1
Oversampling frequency	f_{OS}	—	1.5	—	MHz	*1
Output data rate	T_{DATA}	—	256	—	µs	*1
Data width	RES	—	24	—	bit	—
SNDR*2	SNDR	81	86	—	dB	x1 gain
		79	83	—		x2 gain
		77	81	—		x4 gain
		74	78	—		x8 gain
		69	74	—		x16 gain
Passband (low pass band)	f_{Chpf}	—	0.607	—	Hz	At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 00b.
		—	1.214	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 01b.
		—	2.427	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 10b.
		—	4.855	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 11b.
In-band ripple 1	rp1	-0.01	—	0.01	dB	45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz
In-band ripple 2	rp2	-0.1	—	0.1	dB	45 Hz to 275 Hz @50 Hz 54 Hz to 330 Hz @60 Hz
In-band ripple 3	rp3	-0.1	—	0.1	dB	45 Hz to 1100 Hz @50 Hz 54 Hz to 1320 Hz @60 Hz
Passband (high pass band)	f_{Clpf}	—	1673	—	Hz	-3 dB
Stopband (high pass band)	f_{att}	—	2552	—	Hz	-80 dB
Out-band attenuation	ATT1	-80	—	—	dB	f_S
	ATT2	-80	—	—	dB	2 f_S

Note 1. The operating clock frequency should be selected to 12 MHz at this mode for 24-bit Sigma-Delta A/D converter.
When external clock input (12 MHz) or high- speed on-chip oscillator (24 MHz / 2 or 48 MHz / 4) or PLL clock of sub oscillation (12 MHz) is used as SDADC clock frequency (SDADCCLK), set bits [1:0] (CK[1:0]) of register SDADCCR to 10b and bits [29:28] (FR[1:0]) of register SDADMR to 00b.
Note 2. It is not guaranteed value but only a design target.

2.5.4 4 kHz Sampling Mode (f_{OS} = 1.6 MHz)

Table 2.56 4 kHz sampling mode (f_{OS} = 1.6 MHz) characteristics

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V, ANINn and ANIPn (n = 0 to 6)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating clock (SDADCCLK)*1	f_{SDAD}	—	16	—	MHz	*1
		—	12.8	—		
Sampling frequency	f_S	—	4167	—	Hz	*1
Oversampling frequency	f_{OS}	—	1.6	—	MHz	*1
Output data rate	T_{DATA}	—	240	—	µs	*1
Data width	RES	—	24	—	bit	—
SNDR*2	SNDR	81	86	—	dB	x1 gain
		79	83	—		x2 gain
		77	81	—		x4 gain
		74	78	—		x8 gain
		69	74	—		x16 gain
Passband (low pass band)	f_{Chpf}	—	0.647	—	Hz	At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 00b.
		—	1.295	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 01b.
		—	2.589	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 10b.
		—	5.179	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 11b.
In-band ripple 1	rp1	-0.01	—	0.01	dB	45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz
In-band ripple 2	rp2	-0.1	—	0.1	dB	45 Hz to 275 Hz @50 Hz 54 Hz to 330 Hz @60 Hz
In-band ripple 3	rp3	-0.1	—	0.1	dB	45 Hz to 1100 Hz @50 Hz 54 Hz to 1320 Hz @60 Hz
Passband (high pass band)	f_{Clpf}	—	1785	—	Hz	-3 dB
Stopband (high pass band)	f_{att}	—	2722	—	Hz	-80 dB
Out-band attenuation	ATT1	-80	—	—	dB	f_S
	ATT2	-80	—	—	dB	2 f_S

Note 1. The operating clock frequency should be selected to 16 MHz or 12.8 MHz at this mode for 24-bit Sigma-Delta A/D converter.
When external clock input (16 MHz) or high-speed on-chip oscillator (32 MHz / 2 or 64 MHz / 4) is used as SDADC clock frequency (SDADCCLK), set bits [1:0] (CK[1:0]) of register SDADCCR to 11b and bits [29:28] (FR[1:0]) of register SDADMR to 00b.
When PLL clock of sub oscillation (12.8 MHz) is used as SDADC clock frequency (SDADCCLK), set bits [1:0] (CK[1:0]) of register SDADCCR to 10b and bits [29:28] (FR[1:0]) of register SDADMR to 00b.
Note 2. It is not guaranteed value but only a design target.

2.5.5 8 kHz Sampling Mode (f_{OS} = 3.0 MHz)

Table 2.57 8 kHz Sampling Mode (f_{OS} = 3.0 MHz) characteristics

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V, ANINn and ANIPn (n = 0 to 6)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating clock (SDADCCLK)*1	f_{SDAD}	—	12	—	MHz	*1
Sampling frequency	f_S	—	7813	—	Hz	*1
Oversampling frequency	f_{OS}	—	3.0	—	MHz	*1
Output data rate	T_{DATA}	—	128	—	µs	*1
Data width	RES	—	24	—	bit	—
SNDR*2	SNDR	81	86	—	dB	x1 gain
		79	83	—		x2 gain
		76	80	—		x4 gain
		73	77	—		x8 gain
		69	73	—		x16 gain
Passband (low pass band)	f_{Chpf}	—	1.214	—	Hz	At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 00b.
		—	2.427	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 01b.
		—	4.855	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 10b.
		—	9.710	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 11b.
In-band ripple 1	rp1	-0.01	—	0.01	dB	45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz
In-band ripple 2	rp2	-0.1	—	0.1	dB	45 Hz to 550 Hz @50 Hz 54 Hz to 660 Hz @60 Hz
In-band ripple 3	rp3	-0.1	—	0.1	dB	45 Hz to 2200 Hz @50 Hz 54 Hz to 2640 Hz @60 Hz
Passband (high pass band)	f_{Clpf}	—	3346	—	Hz	-3 dB
Stopband (high pass band)	f_{att}	—	5104	—	Hz	-80 dB
Out-band attenuation	ATT1	-80	—	—	dB	f_S
	ATT2	-80	—	—	dB	2 f_S

Note 1. The operating clock frequency should be selected to 12 MHz at this mode for 24-bit Sigma-Delta A/D converter. When external clock input (12 MHz) or high-speed on-chip oscillator (24 MHz / 2 or 48 MHz / 4) or PLL clock of sub oscillation (12 MHz) is used as SDADC clock frequency (SDADCCLK), set bits [1:0] (CK[1:0]) of register SDADCCR to 10b and bits [29:28] (FR[1:0]) of register SDADMR to 01b.

Note 2. It is not guaranteed value but only a design target.

2.5.6 8 kHz Sampling Mode (f_{OS} = 3.2 MHz)

Table 2.58 8 kHz Sampling Mode (f_{OS} = 3.2 MHz) characteristics (1 of 2)

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V, ANINn and ANIPn (n = 0 to 6)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating clock (SDADCCLK)*1	f_{SDAD}	—	16	—	MHz	*1
		—	12.8	—		
Sampling frequency	f_S	—	8333	—	Hz	*1

Table 2.58 8 kHz Sampling Mode (f_{OS} = 3.2 MHz) characteristics (2 of 2)

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V, ANINn and ANIPn (n = 0 to 6)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Oversampling frequency	f_{OS}	—	3.2	—	MHz	*1
Output data rate	T_{DATA}	—	120	—	µs	*1
Data width	RES	—	24	—	bit	—
SNDR*2	SNDR	81	86	—	dB	x1 gain
		79	83	—		x2 gain
		76	80	—		x4 gain
		73	77	—		x8 gain
		68	73	—		x16 gain
Passband (low pass band)	f_{Chpf}	—	1.295	—	Hz	At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 00b.
		—	2.589	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 01b.
		—	5.179	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 10b.
		—	10.357	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 11b.
In-band ripple 1	rp1	-0.01	—	0.01	dB	45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz
In-band ripple 2	rp2	-0.1	—	0.1	dB	45 Hz to 550 Hz @50 Hz 54 Hz to 660 Hz @60 Hz
In-band ripple 3	rp3	-0.1	—	0.1	dB	45 Hz to 2200 Hz @50 Hz 54 Hz to 2640 Hz @60 Hz
Passband (high pass band)	f_{Clpf}	—	3569	—	Hz	-3 dB
Stopband (high pass band)	f_{att}	—	5444	—	Hz	-80 dB
Out-band attenuation	ATT1	-80	—	—	dB	f_S
	ATT2	-80	—	—	dB	2 f_S

Note 1. The operating clock frequency should be selected to 12.8 MHz at this mode for 24-bit Sigma-Delta A/D converter.
When high-speed on-chip oscillator (32 MHz / 2 or 64 MHz / 4) is used as SDADC clock frequency (SDADCCLK), set bits [1:0] (CK[1:0]) of register SDADCCR to 11b and bits [29:28] (FR[1:0]) of register SDADMR to 01b.
When PLL clock of sub oscillation (12.8 MHz) is used as SDADC clock frequency (SDADCCLK), set bits [1:0] (CK[1:0]) of register SDADCCR to 10b and bits [29:28] (FR[1:0]) of register SDADMR to 01b.

Note 2. It is not guaranteed value but only a design target.

2.5.7 8 kHz/4 kHz Hybrid Sampling Mode (f_{OS} = 3.0 MHz)

Table 2.59 8 kHz/4 kHz hybrid sampling mode (f_{OS} = 3.0 MHz) characteristics (1 of 3)

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V, ANINn and ANIPn (n = 0 to 3)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Operating clock (SDADCCLK)*1		f_{SDAD}	—	12	—	MHz	*1
Sampling frequency	8 kHz sampling mode (Type 1)	f_S	—	7813	—	Hz	*1
	4 kHz hybrid sampling mode (Type 2)		—	3906	—		
Oversampling frequency		f_{OS}	—	3.0	—	MHz	*1

Table 2.59 8 kHz/4 kHz hybrid sampling mode (f_{OS} = 3.0 MHz) characteristics (2 of 3)

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V, ANINn and ANIPn (n = 0 to 3)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Output data rate	8 kHz sampling mode (Type 1)	T_{DATA}	—	128	—	µs	*1
	4 kHz hybrid sampling mode (Type 2)		—	256	—		
Data width		RES	—	24	—	bit	—
SNDR*2	8 kHz sampling mode (Type 1)	SNDR	81	86	—	dB	x1 gain
			79	83	—		x2 gain
			76	80	—		x4 gain
			73	77	—		x8 gain
			69	73	—		x16 gain
	4 kHz hybrid sampling mode (Type 2)		81	86	—		x1 gain
			79	83	—		x2 gain
			77	81	—		x4 gain
			74	78	—		x8 gain
			69	74	—		x16 gain
Passband (low pass band)	8 kHz sampling mode (Type 1)	f_{Chpf}	—	1.214	—	Hz	At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 00b.
	4 kHz hybrid sampling mode (Type 2)		—	1.214	—		
	8 kHz sampling mode (Type 1)		—	2.427	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 01b.
	4 kHz hybrid sampling mode (Type 2)		—	2.427	—		
	8 kHz sampling mode (Type 1)		—	4.855	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 10b.
	4 kHz hybrid sampling mode (Type 2)		—	4.855	—		
	8 kHz sampling mode (Type 1)		—	1.214	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 11b.
	4 kHz hybrid sampling mode (Type 2)		—	0.607	—		
In-band ripple 1	8 kHz sampling mode (Type 1)	rp1	-0.01	—	0.01	dB	45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz
	4 kHz hybrid sampling mode (Type 2)						45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz
In-band ripple 2	8 kHz sampling mode (Type 1)	rp2	-0.1	—	0.1	dB	45 Hz to 550 Hz @50 Hz 54 Hz to 660 Hz @60 Hz
	4 kHz hybrid sampling mode (Type 2)						45 Hz to 275 Hz @50 Hz 54 Hz to 330 Hz @60 Hz
In-band ripple 3	8 kHz sampling mode (Type 1)	rp3	-0.1	—	0.1	dB	45 Hz to 2200 Hz @50 Hz 54 Hz to 2640 Hz @60 Hz
	4 kHz hybrid sampling mode (Type 2)						45 Hz to 1100 Hz @50 Hz 54 Hz to 1320 Hz @60 Hz
Passband (high pass band)	8 kHz sampling mode (Type 1)	f_{Clpf}	—	3346	—	Hz	-3 dB
	4 kHz hybrid sampling mode (Type 2)			1673			

Table 2.59 8 kHz/4 kHz hybrid sampling mode (f_{OS} = 3.0 MHz) characteristics (3 of 3)

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V, ANINn and ANIPn (n = 0 to 3)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Stopband (high pass band)	8 kHz sampling mode (Type 1)	f_{att}	—	5104	—	Hz	-80 dB
	4 kHz hybrid sampling mode (Type 2)			2552			
Out-band attenuation		ATT1	-80	—	—	dB	f_S
		ATT2	-80	—	—	dB	2 f_S

Note 1. The operating clock frequency should be selected to 12 MHz at this mode for 24-bit Sigma-Delta A/D converter.
Note 2. It is not guaranteed value but only a design target.

2.5.8 8 kHz/4 kHz Hybrid Sampling Mode (f_{OS} = 3.2 MHz)

Table 2.60 8 kHz/4 kHz hybrid sampling mode (f_{OS} = 3.2 MHz) characteristics (1 of 2)

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V, ANINn and ANIPn (n = 0 to 3)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Operating clock (SDADCCLK)*1		f_{SDAD}	—	16	—	MHz	*1
			—	12.8	—		
Sampling frequency	8 kHz sampling mode (Type 1)	f_S	—	8333	—	Hz	*1
	4 kHz hybrid sampling mode (Type 2)		—	4167	—		
Oversampling frequency		f_{OS}	—	3.2	—	MHz	*1
Output data rate	8 kHz sampling mode (Type 1)	T_{DATA}	—	120	—	µs	*1
	4 kHz hybrid sampling mode (Type 2)		—	240	—		
Data width		RES	—	24	—	bit	—
SNDR*2	8 kHz sampling mode (Type 1)	SNDR	81	86	—	dB	x1 gain
			79	83	—		x2 gain
			76	80	—		x4 gain
			73	77	—		x8 gain
			68	73	—		x16 gain
	4 kHz hybrid sampling mode (Type 2)		81	86	—		x1 gain
			79	83	—		x2 gain
			77	81	—		x4 gain
			74	78	—		x8 gain
			69	74	—		x16 gain

Table 2.60 8 kHz/4 kHz hybrid sampling mode (f_{OS} = 3.2 MHz) characteristics (2 of 2)

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V, ANINn and ANIPn (n = 0 to 3)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Passband (low pass band)	8 kHz sampling mode (Type 1)	f_{Chpf}	—	1.295	—	Hz	At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 00b.
	4 kHz hybrid sampling mode (Type 2)		—	1.295	—		
	8 kHz sampling mode (Type 1)		—	2.589	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 01b.
	4 kHz hybrid sampling mode (Type 2)		—	2.589	—		
	8 kHz sampling mode (Type 1)		—	5.179	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 10b.
	4 kHz hybrid sampling mode (Type 2)		—	5.179	—		
	8 kHz sampling mode (Type 1)		—	1.295	—		At -3 dB (phase in high-pass filter not adjusted). SDADHPFCR.COF[1:0] = 11b.
	4 kHz hybrid sampling mode (Type 2)		—	0.647	—		
In-band ripple 1	8 kHz sampling mode (Type 1)	rp1	-0.01	—	0.01	dB	45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz
	4 kHz hybrid sampling mode (Type 2)						45 Hz to 55 Hz @50 Hz 54 Hz to 66 Hz @60 Hz
In-band ripple 2	8 kHz sampling mode (Type 1)	rp2	-0.1	—	0.1	dB	45 Hz to 550 Hz @50 Hz 54 Hz to 660 Hz @60 Hz
	4 kHz hybrid sampling mode (Type 2)						45 Hz to 275 Hz @50 Hz 54 Hz to 330 Hz @60 Hz
In-band ripple 3	8 kHz sampling mode (Type 1)	rp3	-0.1	—	0.1	dB	45 Hz to 2200 Hz @50 Hz 54 Hz to 2640 Hz @60 Hz
	4 kHz hybrid sampling mode (Type 2)						45 Hz to 1100 Hz @50 Hz 54 Hz to 1320 Hz @60 Hz
Passband (high pass band)	8 kHz sampling mode (Type 1)	f_{Clpf}	—	3569	—	Hz	-3 dB
	4 kHz hybrid sampling mode (Type 2)			1785			
Stopband (high pass band)	8 kHz sampling mode (Type 1)	f_{att}	—	5444	—	Hz	-80 dB
	4 kHz hybrid sampling mode (Type 2)			2722			
Out-band attenuation		ATT1	-80	—	—	dB	f_S
		ATT2	-80	—	—	dB	2 f_S

Note 1. The operating clock frequency should be selected to 12.8 MHz at this mode for 24-bit Sigma-Delta A/D converter.
When high-speed on-chip oscillator (32 MHz / 2 or 64 MHz / 4) is used as SDADC clock frequency (SDADCCLK), set bits [1:0] (CK[1:0]) of register SDADCCR to 11b and bits [29:28] (FR[1:0]) of register SDADMR to 10b.
When PLL clock of sub oscillation (12.8 MHz) is used as SDADC clock frequency (SDADCCLK), set bits [1:0] (CK[1:0]) of register SDADCCR to 10b and bits[29:28] (FR[1:0]) of register SDADMR to 10b.

Note 2. It is not guaranteed value but only a design target.

2.5.9 Other Characteristics for SDADC24

Table 2.61 Other characteristics for SDADC24

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0V
The electrical specifications are applied at the differential input mode, with MOSC used as source clock, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Gain error*1	E_G	-3	—	3	%	x1 to x8 gain, excluding AVRT error
		-4	—	4	%	x16 gain, excluding AVRT error
Gain drift*1 *2	dE_G	—	15	—	ppm/°C	excluding AVRT error
Offset error*1	E_{OS}	-10	—	10	mV	x1 gain, excluding AVRT error, referred to input
Offset drift*1 *3	dE_{OS}	—	4	—	µV/°C	x1 gain, excluding AVRT error, referred to input
Integral non-linearity*1	INL	—	20	—	ppm of FSR	x1 gain
		—	50	—		x16 gain
Common mode Rejection ratio*1	CMRR	—	80	—	dB	
Power supply Rejection ratio*1	PSRR	—	70	—	dB	Analog input = 0 V
Input impedance*1	Z_{IN}	—	360	—	kΩ	differential input
		—	240	—		single-ended input

Note 1. This is not tested in production, but the design guarantees the characteristic.
Note 2. Gain drift is calculated by (Max(E_G(T)) - Min(E_G(T))) / (Max(T) - Min(T)) with T range from -40°C to +105°C
Note 3. Offset drift is calculated by (Max(E_{OS}(T)) - Min(E_{OS}(T))) / (Max(T) - Min(T)) with T range from -40°C to +105°C

2.5.10 Regulator for SDADC24 (AREGC) Characteristics

Table 2.62 Regulator for SDADC24 (AREGC) characteristics

Conditions: VCC = AVCC = 2.4 to 5.5 V, VSS = AVSS = 0 V
Connect the AREGC pin to AVSS pin by a 0.47 µF capacitor.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
AREGC output voltage	VADREG	1.5	1.55	1.6	V	0.47 µF capacitor connected to AVSS pin

2.6 TSN Characteristics

Table 2.63 TSN characteristics

Conditions: VCC = AVCC = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	—	—	± 1.5	—	°C	2.4 V or above
		—	± 2.0	—	°C	Below 2.4 V
Temperature slope	—	—	-3.3	—	mV/°C	—
Output voltage (at 25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	—
Sampling time	—	5	—	—	µs	

2.7 OSC Stop Detect Characteristics

Table 2.64 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.41

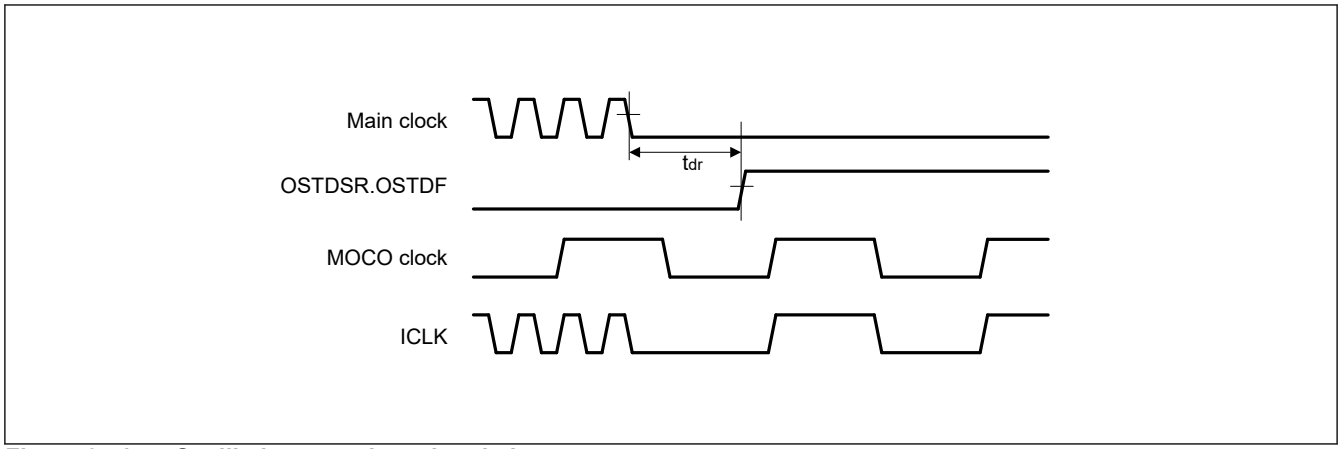


Figure 2.41 Oscillation stop detection timing

2.8 POR and LVD Characteristics

Table 2.65 Power-on reset circuit and voltage detection circuit characteristics (1) (1 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Power-on reset (POR)	When power supply rise	V_{POR}	1.47	1.51	1.55	V	Figure 2.42
		When power supply fall	V_{PDR}	1.46	1.50	1.54		Figure 2.43
	Voltage detection circuit (LVD0)*2	When power supply rise	V_{det0_0}	3.74	3.91	4.06	V	Figure 2.44 At falling edge VCC
		When power supply fall		3.68	3.85	4.00		
		When power supply rise	V_{det0_1}	2.73	2.9	3.01		
		When power supply fall		2.68	2.85	2.96		
		When power supply rise	V_{det0_2}	2.44	2.59	2.70		
		When power supply fall		2.38	2.53	2.64		
		When power supply rise	V_{det0_3}	1.83	1.95	2.07		
		When power supply fall		1.78	1.90	2.02		
		When power supply rise	V_{det0_4}	1.66	1.75	1.88		
		When power supply fall		1.60	1.69	1.82		
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_0}	4.23	4.39	4.55	V	Figure 2.45 At falling edge VCC
		When power supply fall		4.13	4.29	4.45		
		When power supply rise	V_{det1_1}	4.07	4.25	4.39		
		When power supply fall		3.98	4.16	4.30		
		When power supply rise	V_{det1_2}	3.97	4.14	4.29		
		When power supply fall		3.86	4.03	4.18		
		When power supply rise	V_{det1_3}	3.74	3.92	4.06		
		When power supply fall		3.68	3.86	4.00		
		When power supply rise	V_{det1_4}	3.05	3.17	3.29		
		When power supply fall		2.98	3.10	3.22		
		When power supply rise	V_{det1_5}	2.95	3.06	3.17		
		When power supply fall		2.89	3.00	3.11		
		When power supply rise	V_{det1_6}	2.86	2.97	3.08		
		When power supply fall		2.79	2.90	3.01		
		When power supply rise	V_{det1_7}	2.74	2.85	2.96		
		When power supply fall		2.68	2.79	2.90		

Table 2.65 Power-on reset circuit and voltage detection circuit characteristics (1) (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level*1	Voltage detection circuit (LVD1)*3	When power supply rise	V_{det1_8}	2.63	2.75	2.85	V	Figure 2.45 At falling edge VCC
		When power supply fall		2.58	2.68	2.78		
		When power supply rise	V_{det1_9}	2.54	2.64	2.75		
		When power supply fall		2.48	2.58	2.68		
		When power supply rise	V_{det1_A}	2.43	2.53	2.63		
		When power supply fall		2.38	2.48	2.58		
		When power supply rise	V_{det1_B}	2.16	2.26	2.36		
		When power supply fall		2.10	2.20	2.30		
		When power supply rise	V_{det1_C}	1.88	2	2.09		
		When power supply fall		1.84	1.96	2.05		
		When power supply rise	V_{det1_D}	1.78	1.9	1.99		
		When power supply fall		1.74	1.86	1.95		
		When power supply rise	V_{det1_E}	1.67	1.79	1.88		
		When power supply fall		1.63	1.75	1.84		
		When power supply rise	V_{det1_F}	1.65	1.7	1.78		
		When power supply fall		1.60	1.65	1.73		
Voltage detection level*1	Voltage detection circuit (LVD2)*4	When power supply rise	V_{det2_0}	4.20	4.40	4.57	V	Figure 2.46 At falling edge VCC
		When power supply fall		4.11	4.31	4.48		
		When power supply rise	V_{det2_1}	4.05	4.25	4.42		
		When power supply fall		3.97	4.17	4.34		
		When power supply rise	V_{det2_2}	3.91	4.11	4.28		
		When power supply fall		3.83	4.03	4.20		
		When power supply rise	V_{det2_3}	3.71	3.91	4.08		
		When power supply fall		3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.
Note 2. # in the symbol $V_{det0\_\#}$ denotes the value of the OFS1.VDSEL0[2:0] bits.
Note 3. # in the symbol $V_{det1\_\#}$ denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.
Note 4. # in the symbol $V_{det2\_\#}$ denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.

Table 2.66 Power-on reset circuit and voltage detection circuit characteristics (2) (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Wait time after power-on reset cancellation	LVD0: enable	t_{POR}	—	4.3	—	ms	—
	LVD0: disable	t_{POR}	—	3.7	—	ms	—
Wait time after voltage monitor 0, 1, 2 reset cancellation	LVD0: enable*1	$t_{LVD0,1,2}$	—	1.4	—	ms	—
	LVD0: disable*2	$t_{LVD1,2}$	—	0.7	—	ms	—
Power-on reset response delay time*3		t_{det}	—	—	500	µs	Figure 2.42, Figure 2.43
LVD0 response delay time*3		t_{det}	—	—	500	µs	Figure 2.44
LVD1 response delay time*3		t_{det}	—	—	350	µs	Figure 2.45
LVD2 response delay time*3		t_{det}	—	—	600	µs	Figure 2.46
Minimum VCC down time		t_{VOFF}	500	—	—	µs	Figure 2.42, VCC = 1.0 V or above
Power-on reset enable time		$t_{W\ (POR)}$	1	—	—	ms	Figure 2.43, VCC = below 1.0 V

Table 2.66 Power-on reset circuit and voltage detection circuit characteristics (2) (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
LVD1 operation stabilization time (after LVD1 is enabled)	$T_{d\ (E-A)}$	—	—	300	µs	Figure 2.45
LVD2 operation stabilization time (after LVD2 is enabled)	$T_{d\ (E-A)}$	—	—	1200	µs	Figure 2.46
Hysteresis width (POR)	V_{PORH}	—	10	—	mV	—
Hysteresis width (LVD0, LVD1 and LVD2)	V_{LVH}	—	60	—	mV	LVD0 selected
		—	110	—		V_{det1_0} to V_{det1_2} selected
		—	70	—		V_{det1_3} to V_{det1_9} selected
		—	60	—		V_{det1_A} to V_{det1_B} selected
		—	50	—		V_{det1_C} to V_{det1_F} selected
		—	90	—		LVD2 selected

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, V_{det1}, and V_{det2} for the POR/LVD.

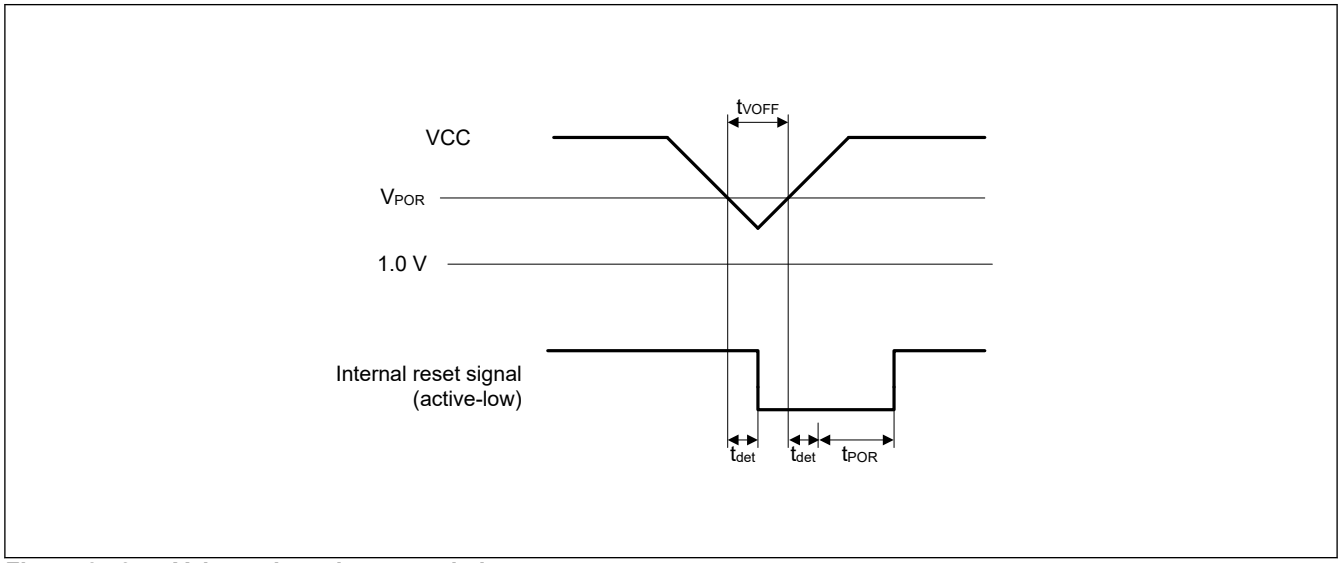
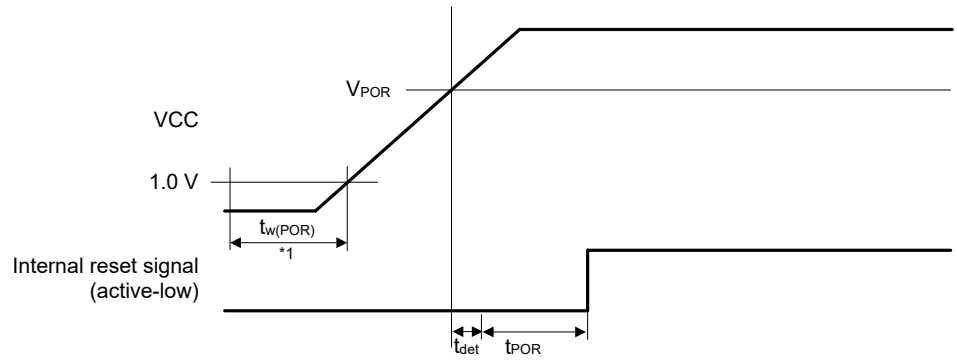


Figure 2.42 Voltage detection reset timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{w(POR)}$ for 1.0 ms or more.

Figure 2.43 Power-on reset timing

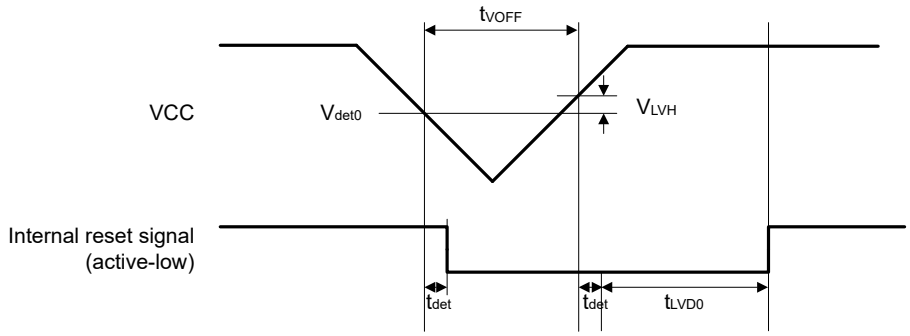


Figure 2.44 Voltage detection circuit timing (V_{det0})

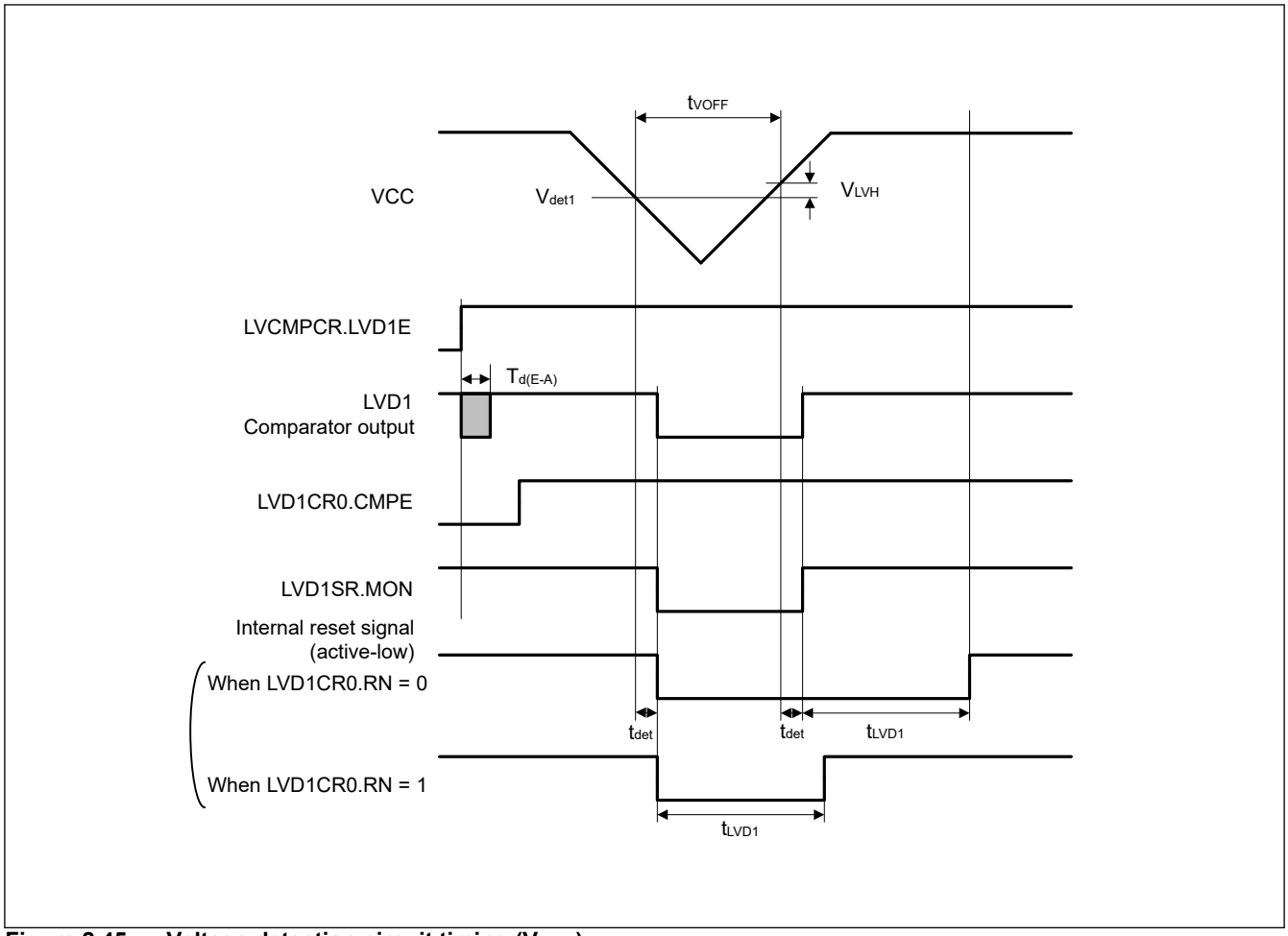


Figure 2.45 Voltage detection circuit timing (V_{det1})

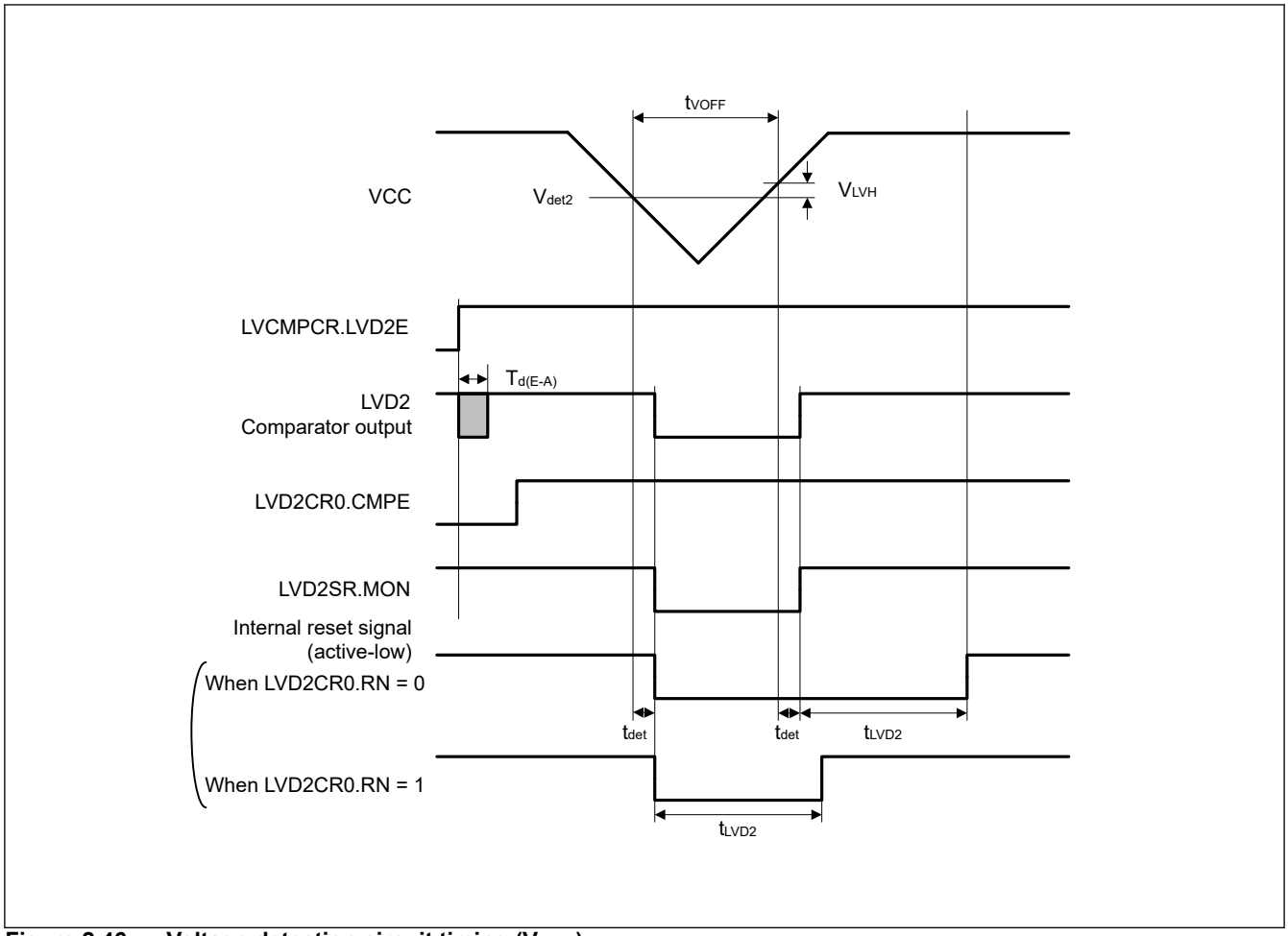


Figure 2.46 Voltage detection circuit timing (V_{det2})

2.9 VRTC POR Characteristics

Table 2.67 Power-on reset circuit of VRTC characteristics

Parameter				Symbol	Min	Typ	Max	Unit	Test Conditions
Voltage detection level	Power-on reset of VRTC (VRTC_POR)	When power supply rise	—	V_{RTCPOR}	1.51	1.55	1.59	V	Figure 2.47
			VCC < 1.0 V and Ta ≤ 85°C		1.48	1.55	1.59		
			VCC < 1.0 V and Ta > 85°C		1.51	1.55	1.78		
		When power supply fall	—	V_{RTCPDR}	1.49	1.53	1.57		
			VCC < 1.0 V and Ta ≤ 85°C		1.46	1.53	1.59		
			VCC < 1.0 V and Ta > 85°C		1.49	1.53	1.78		
Hysteresis width of VRTC (VRTC_POR)				$V_{RTCPORH}$	—	20	—	mV	—
Wait time after power-on reset cancellation				t_{RTCPOR}	—	—	12	ms	Figure 2.47
Power-on reset of VRTC response delay time *1				t_{rtcdet}	—	—	500	µs	Figure 2.47
Power-on reset of VRTC enable time*1				$t_{W\ (VRTC\_POR)}$	1	—	—	ms	Figure 2.47, VRTC = below 1.0 V

Note 1. The minimum VRTC down time indicates the time when VRTC is below the minimum value of voltage detection level of VRTC_POR.

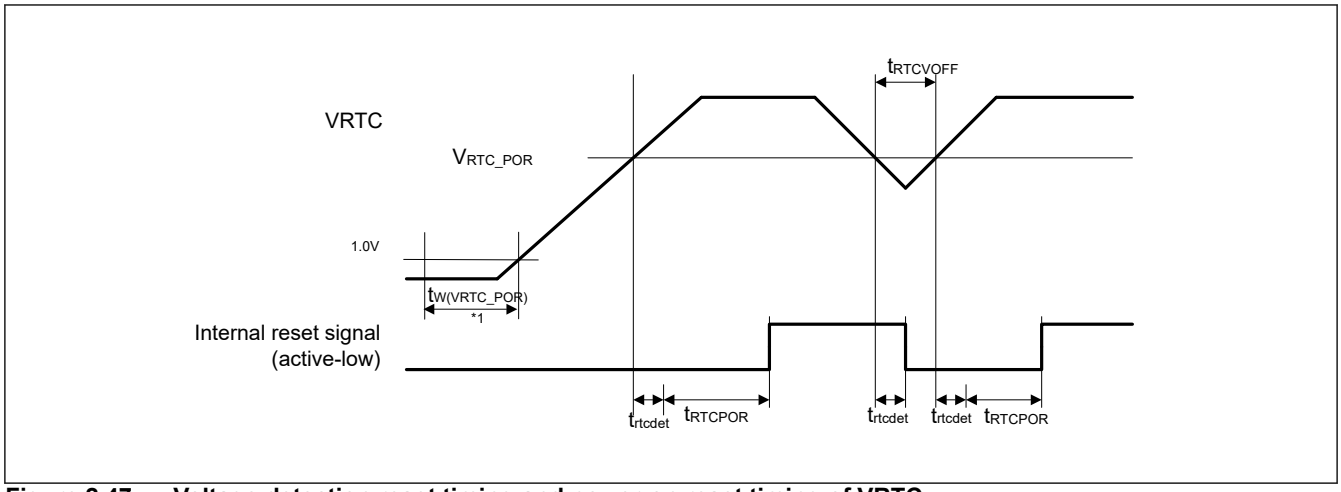


Figure 2.47 Voltage detection reset timing and power-on reset timing of VRTC

2.10 EXLVDVBAT Pin Voltage Detection Characteristics

Table 2.68 EXLVDVBAT pin voltage detection characteristics

Conditions: VCC = AVCC = 1.8 to 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
Internal reference voltage	$V_{LVDVBAT0}$	VBTLVDCR.LVL [2:0] = 000	Rising	2.17	2.24	2.31	V	—
			Falling	2.12	2.18	2.24		—
	$V_{LVDVBAT1}$	VBTLVDCR.LVL [2:0] = 001	Rising	2.37	2.44	2.51		—
			Falling	2.31	2.38	2.45		—
	$V_{LVDVBAT2}$	VBTLVDCR.LVL [2:0] = 010	Rising	2.56	2.64	2.72		—
			Falling	2.50	2.58	2.66		—
	$V_{LVDVBAT3}$	VBTLVDCR.LVL [2:0] = 011	Rising	2.66	2.74	2.82		—
			Falling	2.60	2.68	2.76		—
	$V_{LVDVBAT4}$	VBTLVDCR.LVL [2:0] = 100	Rising	2.76	2.84	2.92		—
			Falling	2.70	2.78	2.86		—
	$V_{LVDVBAT5}$	VBTLVDCR.LVL [2:0]=101	Rising	2.85	2.94	3.03		—
			Falling	2.80	2.88	2.96		—
	$V_{LVDVBAT6}$	VBTLVDCR.LVL [2:0] = 110	Rising	3.05	3.14	3.23		—
			Falling	2.99	3.08	3.17		—
Minimum pulse width	$t_{pw\_lvdvbat}$	—	—	500	—	—	µs	Figure 2.48
Detection delay time	$t_{d\_lvdvbat}$	—	—	—	—	500	µs	Figure 2.48
Pin resistor	$r_{in\_lvdvbat}$	—	VBTLVDCR.LVDE = 1	80	150	280	MΩ	—

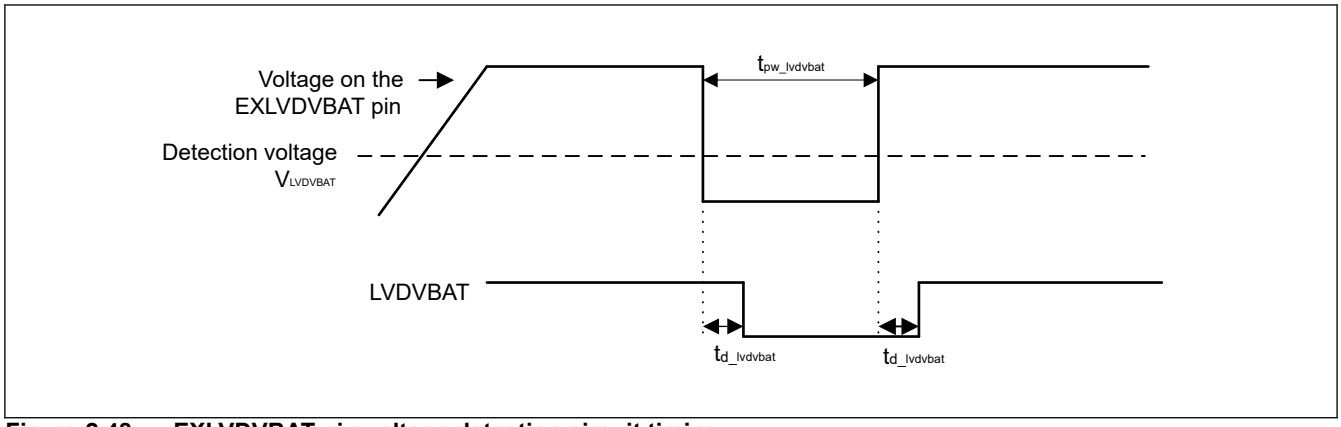


Figure 2.48 EXLVDVBAT pin voltage detection circuit timing

2.11 VRTC Pin Voltage Detection Characteristics

Table 2.69 VRTC pin voltage detection characteristics

Conditions: VCC = AVCC = 1.8 to 5.5 V, VSS = AVSS = 0 V, VRTC = 1.8 to 5.5 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
Internal reference voltage	$V_{LVDVRTC0}$	VRTLVDCR.LVL [1:0] = 00	Rising	2.16	2.22	2.28	V	—
			Falling	2.10	2.16	2.22		—
	$V_{LVDVRTC1}$	VRTLVDCR.LVL [1:0] = 01	Rising	2.36	2.43	2.50		—
			Falling	2.30	2.37	2.44		—
	$V_{LVDVRTC2}$	VRTLVDCR.LVL [1:0] = 10	Rising	2.56	2.63	2.70		—
			Falling	2.50	2.57	2.64		—
	$V_{LVDVRTC3}$	VRTLVDCR.LVL [1:0] = 11	Rising	2.76	2.84	2.92		—
			Falling	2.70	2.78	2.86		—
Minimum pulse width	$t_{pw\_lvdvrtc}$	—	—	500	—	—	µs	Figure 2.49
Detection delay time	$t_{d\_lvdvrrtc}$	—	—	—	—	500	µs	Figure 2.49

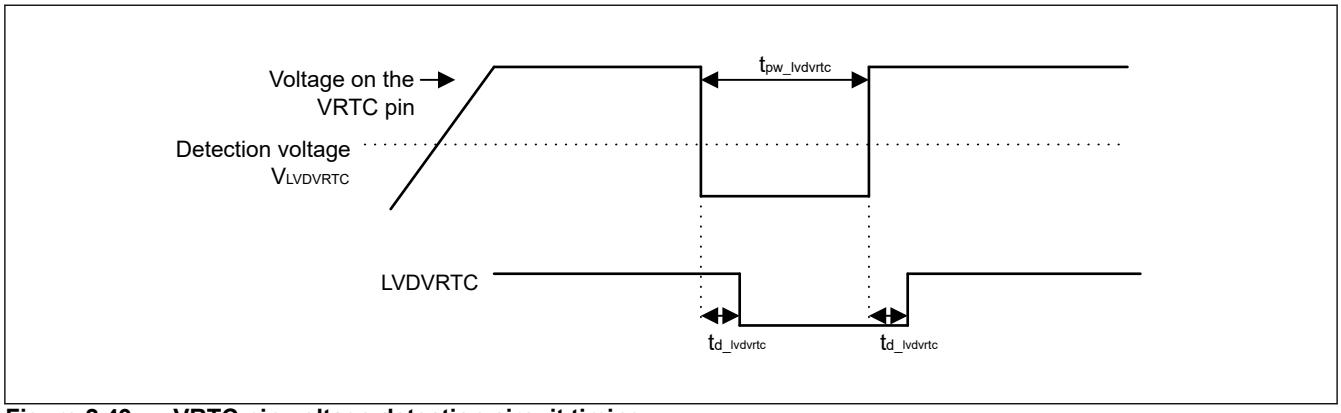


Figure 2.49 VRTC pin voltage detection circuit timing

2.12 EXLVD Pin Voltage Detections

Table 2.70 EXLVD pin voltage detection characteristics (1 of 2)

Conditions: VCC = AVCC = 1.8 to 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
Internal reference voltage	$V_{LVDEXLVD}$	—	Rising	1.25	1.33	1.41	V	—
			Falling	1.20	1.28	1.36		—

Table 2.70 EXLVD pin voltage detection characteristics (2 of 2)

Conditions: VCC = AVCC = 1.8 to 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
Minimum pulse width	$t_{pw\_lvdexlvd}$	—	—	500	—	—	µs	Figure 2.50
Detection delay time	t_{d_exlvd}	—	—	—	—	500	µs	Figure 2.50
Pin resistor	r_{in_exlvd}	—	EXLVDCR.LVDE = 1	30	60	115	MΩ	—

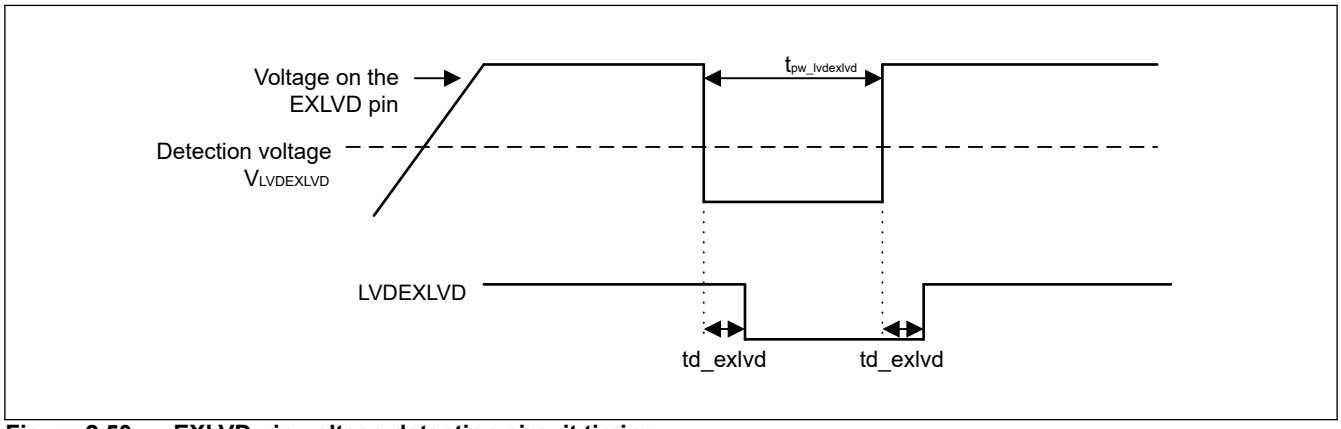


Figure 2.50 EXLVD pin voltage detection circuit timing

2.13 Segment LCD Controller Characteristics

2.13.1 External Resistance Division Method

(1) Static display mode

Table 2.71 External resistance division method LCD characteristics (1)

Conditions: VL4 (Min) ≤ VCC = AVCC ≤ 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.0	—	VCC	V	—

(2) 1/2 bias method, 1/4 bias method

Table 2.72 External resistance division method LCD characteristics (2)

Conditions: VL4 (Min) ≤ VCC = AVCC ≤ 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.7	—	VCC	V	—

(3) 1/3 bias method

Table 2.73 External resistance division method LCD characteristics (3)

Conditions: VL4 (Min) ≤ VCC = AVCC ≤ 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.5	—	VCC	V	—

2.13.2 Internal Voltage Boosting Method (VL1 Reference)

(1) 1/3 bias method

Table 2.74 Internal voltage boosting method LCD characteristics (1)

Conditions: VCC = AVCC = 1.8 V to 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C4[*5] = 0.47 µF	VLCD[*1] = 0x04	0.97	1.01	1.04	V	—
			VLCD = 0x05	1.00	1.04	1.08	V	—
			VLCD = 0x06	1.04	1.07	1.11	V	—
			VLCD = 0x07	1.07	1.11	1.14	V	—
			VLCD = 0x08	1.10	1.14	1.18	V	—
			VLCD = 0x09	1.13	1.17	1.21	V	
			VLCD = 0x0A	1.16	1.21	1.25	V	—
			VLCD = 0x0B	1.20	1.24	1.28	V	—
			VLCD = 0x0C	1.23	1.27	1.32	V	—
			VLCD = 0x0D	1.26	1.31	1.35	V	—
			VLCD = 0x0E	1.29	1.34	1.38	V	—
			VLCD = 0x0F	1.33	1.37	1.42	V	
			VLCD = 0x10	1.36	1.40	1.45	V	—
			VLCD = 0x11	1.39	1.44	1.49	V	—
			VLCD = 0x12	1.42	1.47	1.52	V	—
			VLCD = 0x13	1.45	1.50	1.55	V	—
			VLCD = 0x14	1.49	1.54	1.59	V	—
			VLCD = 0x15	1.52	1.57	1.62	V	
			VLCD = 0x16	1.55	1.60	1.66	V	—
			VLCD = 0x17	1.58	1.64	1.69	V	—
			VLCD = 0x18	1.61	1.67	1.73	V	—
			VLCD = 0x19	1.65	1.70	1.76	V	—
			VLCD = 0x1A[*4]	1.68	1.74	1.79	V	—
Double output voltage	V_{L2}	C1 to C4[*5] = 0.47 µF		$2 \times V_{L1}$ - 5%	$2 \times V_{L1}$	$2 \times V_{L1}$ + 5%	V	—
Triple output voltage	V_{L4}	C1 to C4[*5] = 0.47 µF		$3 \times V_{L1}$ - 6%	$3 \times V_{L1}$	$3 \times V_{L1}$ + 6%	V	—
Reference voltage setup time[*2]	t_{VL1S}	—		10	—	—	ms	Figure 2.51
Voltage boost wait time[*3]	t_{VLWT}	—		500	—	—	ms	Figure 2.51

Note: 0x0E to 0x1A setting is permitted when using 5V LCD panel, 0x04 to 0x07 setting is permitted when using 3V LCD panel at 1/3 bias.

Note 1. Bit [7] (MDSET[2]) of register VLCD is set to 0 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 01 for internal voltage boosting method (VL1 reference), and bits [4:0] (VLCD4-0) of register VLCD are used for voltage variation setting.

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits of the LCDM0 register to 01b and MDSET[2] of the register VLCD to 0) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 4. This setting is only available when VCC ≥ VL1.

Note 5. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

(2) 1/4 bias method

Table 2.75 Internal voltage boosting method LCD characteristics (2)

Conditions: VCC = AVCC = 1.8 V to 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L1}	C1 to C5*1 = 0.47 µF	VLCD*2 = 0x04	0.97	1.01	1.04	V	—
			VLCD = 0x05	1.00	1.04	1.08	V	—
			VLCD = 0x06	1.04	1.07	1.11	V	—
			VLCD = 0x07	1.07	1.11	1.14	V	—
			VLCD = 0x08	1.10	1.14	1.18	V	—
			VLCD = 0x09	1.13	1.17	1.21	V	
			VLCD = 0x0A	1.16	1.21	1.25	V	—
			VLCD = 0x0B	1.20	1.24	1.28	V	—
			VLCD = 0x0C	1.23	1.27	1.32	V	—
			VLCD = 0x0D	1.26	1.31	1.35	V	—
Double output voltage	V_{L2}	C1 to C5*1 = 0.47 µF		2 × V_{L1} - 5%	2 × V_{L1}	2 × V_{L1} + 5%	V	—
Triple output voltage	V_{L3}	C1 to C5*1 = 0.47 µF		3 × V_{L1} - 6%	3 × V_{L1}	3 × V_{L1} + 6%	V	—
Quadruple output voltage	V_{L4}*5	C1 to C5*1 = 0.47 µF		4 × V_{L1} - 6%	4 × V_{L1}	4 × V_{L1} + 6%	V	—
Reference voltage setup time*3	t_{VL1S}	—		10	—	—	ms	Figure 2.51
Voltage boost wait time*4	t_{VLWT}	—		500	—	—	ms	Figure 2.51

Note 1. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL3 and GND

C5: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = C5 = 0.47 µF ±30%

Note 2. Bit [7] (MDSET[2]) of register VLCD is set to 0 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 01 for internal voltage boosting method (VL1 reference), and bits [4:0] (VLCD4-0) of register VLCD are used for voltage variation setting.

Note 3. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits of the LCDM0 register to 01b and MDSET[2] of the register VLCD to 0) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 4. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 5. V_{L4} must be 5.5 V or lower.

2.13.3 Internal Voltage Boosting Method (VL2 Reference)

(1) 1/3 bias method

Table 2.76 Internal voltage boosting method LCD characteristics (3) (1 of 2)

Conditions: VCC = AVCC = VL2 (Max) + 0.1 to 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
Half output voltage	V_{L1}	C1 to C4*1 = 0.47 µF	1/2 × VL2 - 5%	1/2 × VL2	1/2 × VL2 + 5%	V	—

Table 2.76 Internal voltage boosting method LCD characteristics (3) (2 of 2)

Conditions: VCC = AVCC = VL2 (Max) + 0.1 to 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions		Min	Typ	Max	Unit	Test conditions
LCD output voltage variation range	V_{L2}	C1 to C4[*1] = 0.47 µF	VLCD[*2] = 0x84	1.94	2.02	2.11	V	—
			VLCD = 0x85	2.00	2.09	2.18	V	—
			VLCD = 0x86	2.07	2.16	2.25	V	—
			VLCD = 0x87	2.13	2.22	2.32	V	—
			VLCD = 0x88	2.19	2.29	2.39	V	—
			VLCD = 0x89	2.26	2.36	2.46	V	—
			VLCD = 0x8A	2.32	2.42	2.53	V	—
			VLCD = 0x8B	2.39	2.49	2.59	V	—
			VLCD = 0x8C	2.45	2.56	2.66	V	—
			VLCD = 0x8D	2.51	2.62	2.73	V	—
			VLCD = 0x8E	2.58	2.69	2.80	V	—
			VLCD = 0x8F	2.64	2.76	2.87	V	—
			VLCD = 0x90	2.70	2.82	2.94	V	—
			VLCD = 0x91	2.77	2.89	3.01	V	—
			VLCD = 0x92	2.83	2.96	3.08	V	—
			VLCD = 0x93	2.90	3.02	3.15	V	—
			VLCD = 0x94	2.96	3.09	3.22	V	—
			VLCD = 0x95	3.02	3.15	3.29	V	—
			VLCD = 0x96	3.09	3.22	3.35	V	—
			VLCD = 0x97	3.15	3.29	3.42	V	—
			VLCD = 0x98	3.21	3.35	3.49	V	—
			VLCD = 0x99	3.28	3.42	3.56	V	—
			VLCD = 0x9A	3.34	3.49	3.63	V	—
Two-thirds output voltage	V_{L4}[*5]	C1 to C4[*1] = 0.47 µF		2/3 × V_{L2} - 6%	2/3 × V_{L2}	2/3 × V_{L2} + 6%	V	—
Reference voltage setup time[*3]	t_{VL2S}	—		10	—	—	ms	Figure 2.51
Voltage boost wait time[*4]	t_{VLWT}	—		500	—	—	ms	Figure 2.51

Note: 0x8E to 0x9A setting is permitted when using 5V LCD panel, 0x84 to 0x87 setting is permitted when using 3V LCD panel at 1/3 bias.

Note 1. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

Note 2. Bit [7] (MDSET[2]) of register VLCD is set to 1 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 01 for internal voltage boosting method (VL2 reference), and bits [4:0] (VLCD4-0) of register VLCD are used for voltage variation setting.

Note 3. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits of the LCDM0 register to 01b and MDSET[2] of the register VLCD to 1) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 4. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 5. V_{L4} must be 5.5 V or lower.

2.13.4 Capacitor Split Method (VCC Reference)

(1) 1/3 bias method

Table 2.77 Capacitor split method LCD characteristics (1)

Conditions: VCC = AVCC = 2.2 V to 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
VL4 voltage	V_{L4}	C1 to C4*2 = 0.47 µF	—	VCC	—	V	—
VL2 voltage	V_{L2}	C1 to C4*2 = 0.47 µF	2 / 3 × V_{L4} - 3%	2 / 3 × V_{L4}	2 / 3 × V_{L4} + 3%	V	—
VL1 voltage	V_{L1}	C1 to C4*2 = 0.47 µF	1 / 3 × V_{L4} - 3%	1 / 3 × V_{L4}	1 / 3 × V_{L4} + 3%	V	—
Capacitor split wait time*1	t_{WAIT}	—	100	—	—	ms	Figure 2.51

Note: Bit [7] (MDSET[2]) of register VLCD is set to 0 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 10 for capacitor split method (VCC reference).
Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).
Note 2. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

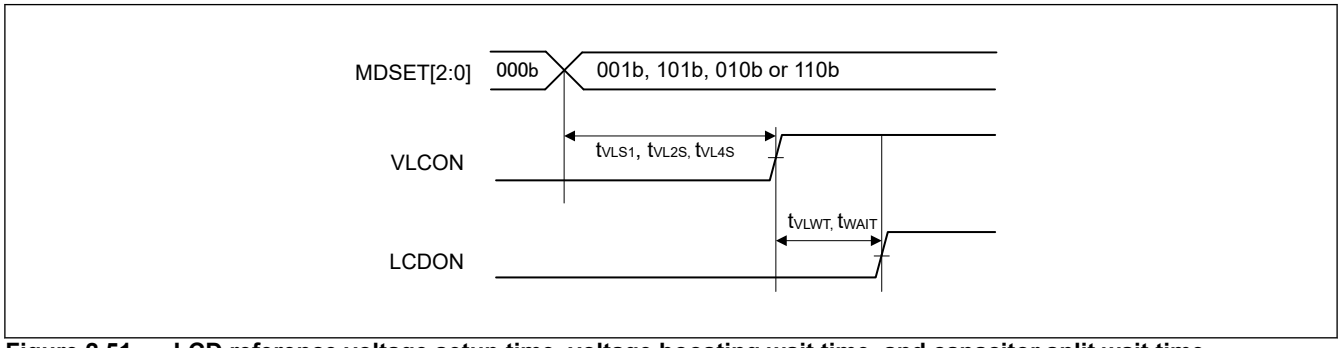


Figure 2.51 LCD reference voltage setup time, voltage boosting wait time, and capacitor split wait time

2.13.5 Capacitor Split Method (VL4 Reference)

(1) 1/3 bias method

Table 2.78 Capacitor split method LCD characteristics (3)

Conditions: VCC = AVCC = 3.2 V to 5.5 V, VSS = AVSS = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
VL4 voltage	V_{L4}	C1 to C4*2 = 0.47 µF	2.89	3.04	3.20	V	—
VL2 voltage	V_{L2}	C1 to C4*2 = 0.47 µF	1.89	2.03	2.17	V	—
VL1 voltage	V_{L1}	C1 to C4*2 = 0.47 µF	0.94	1.01	1.08	V	—
Reference voltage setup time*3	t_{VL4S}	—	10	—	—	ms	Figure 2.51
Capacitor split wait time*1	t_{WAIT}	—	100	—	—	ms	Figure 2.51

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).
Note 2. This is a capacitor that is connected between the voltage pins that are used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 µF ±30%

Note 3. Bit [7] (MDSET[2]) of register VLCD is set to 1 and bits [7:6] (MDSET[1:0]) of register LCDM0 are set to 10 for capacitor split method (VL4 reference).

2.14 Flash Memory Characteristics

2.14.1 Code Flash Memory Characteristics

Table 2.79 Code flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{PEC}	10000	—	—	Times	—
Data hold time	After 1000 times N_{PEC}	t_{DRP}	20*2 *3	—	—	Year	T_a = +85°C T_a = +105°C
	After 10000 times N_{PEC}		10*2 *3	—	—	Year	

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 512 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 2.80 Code flash characteristics (2)

High-speed operating mode

Conditions: VCC = AVCC = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	34	321	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	5.6	215	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	8.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	240	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	10.5	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	11.4	423	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	45.3	1690	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 1. Total time of four commands.

Table 2.81 Code flash characteristics (3) (1 of 2)

Middle-speed operating mode

Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 8 MHz*2			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	39	356	µs

Table 2.81 Code flash characteristics (3) (2 of 2)

Middle-speed operating mode
Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 8 MHz*2			Unit
			Min	Typ	Max	Min	Typ	Max	
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	6.2	227	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	11.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	534	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	11.7	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	12.2	435	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	48.7	1740	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.
Note 2. When 1.8 V ≤ VCC = AVCC ≤ 5.5 V

Table 2.82 Code flash characteristics (4)

Low-speed operating mode
Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	4-byte	t_{P4}	—	86	732	—	57	502	µs
Erasure time	2-KB	t_{E2K}	—	12.5	355	—	8.8	280	ms
Blank check time	4-byte	t_{BC4}	—	—	46.5	—	—	23.3	µs
	2-KB	t_{BC2K}	—	—	3681	—	—	1841	µs
Erase suspended time		t_{SED}	—	—	22.3	—	—	16.2	µs
Access window information program Start-up area selection and security setting time		t_{AWSSAS}	—	21.2	570	—	15.9	491	ms
OCD/serial programmer ID setting time*1		t_{OSIS}	—	84.7	2280	—	63.5	1964	ms
Flash memory mode transition wait time 1		t_{DIS}	2	—	—	2	—	—	µs
Flash memory mode transition wait time 2		t_{MS}	15	—	—	15	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. Total time of four commands.

2.14.2 Data Flash Memory Characteristics

Table 2.83 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	—
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2 *3	—	—	Year	Ta = +105°C
	After 100000 times of N_{DPEC}		5*2 *3	—	—	Year	
	After 1000000 times of N_{DPEC}		—	1*2 *3	—	Year	Ta = +25°C

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,024 times for different addresses in 1-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).
Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 2.84 Data flash characteristics (2)

High-speed operating mode
Conditions: VCC = AVCC = 1.8 to 5.5 V

Parameter		Symbol	ICLK = 4 MHz			ICLK = 48 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	45	404	—	34	321	µs
Erasure time	1-KB	t_{DE1K}	—	8.8	280	—	6.1	224	ms
Blank check time	1-byte	t_{DBC1}	—	—	15.2	—	—	8.3	µs
	1-KB	t_{DBC1K}	—	—	1832	—	—	466	µs
Suspended time during erasing		t_{DSED}	—	—	13.2	—	—	10.5	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Table 2.85 Data flash characteristics (3)

Middle-speed operating mode
Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 4 MHz			ICLK = 8 MHz*1			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	45	404	—	39	356	µs
Erasure time	1-KB	t_{DE1K}	—	8.8	280	—	7.3	248	ms
Blank check time	1-byte	t_{DBC1}	—	—	15.2	—	—	11.3	µs
	1-KB	t_{DBC1K}	—	—	1.84	—	—	1.06	ms
Suspended time during erasing		t_{DSED}	—	—	13.2	—	—	11.7	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 1. When 1.8 V ≤ VCC = AVCC ≤ 5.5 V

Table 2.86 Data flash characteristics (4)

Low-speed operating mode
Conditions: VCC = AVCC = 1.6 to 5.5 V

Parameter		Symbol	ICLK = 1 MHz			ICLK = 2 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t_{DP1}	—	86	732	—	57	502	µs
Erasure time	1-KB	t_{DE1K}	—	19.7	504	—	12.4	354	ms
Blank check time	1-byte	t_{DBC1}	—	—	46.5	—	—	23.3	µs
	1-KB	t_{DBC1K}	—	—	7.3	—	—	3.66	ms
Suspended time during erasing		t_{DSED}	—	—	22.3	—	—	16.2	µs
Data flash STOP recovery time		t_{DSTOP}	250	—	—	250	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of ICLK is 1 MHz during programming or erasing the flash memory. When using ICLK at below 2 MHz, the frequency can be set to 1 MHz or 2 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of ICLK must be ± 1.0% during programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

2.14.3 Serial Wire Debug (SWD)

Table 2.87 SWD characteristics (1)

Conditions: VCC = AVCC = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	80	—	—	ns	Figure 2.52
SWCLK clock high pulse width	t_{SWCKH}	35	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	35	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	16	—	—	ns	Figure 2.53
SWDIO hold time	t_{SWDH}	16	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	70	ns	

Table 2.88 SWD characteristics (2)

Conditions: VCC = AVCC = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	250	—	—	ns	Figure 2.52
SWCLK clock high pulse width	t_{SWCKH}	120	—	—	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	—	—	ns	
SWCLK clock rise time	t_{SWCKr}	—	—	5	ns	
SWCLK clock fall time	t_{SWCKf}	—	—	5	ns	
SWDIO setup time	t_{SWDS}	50	—	—	ns	Figure 2.53
SWDIO hold time	t_{SWDH}	50	—	—	ns	
SWDIO data delay time	t_{SWDD}	2	—	170	ns	

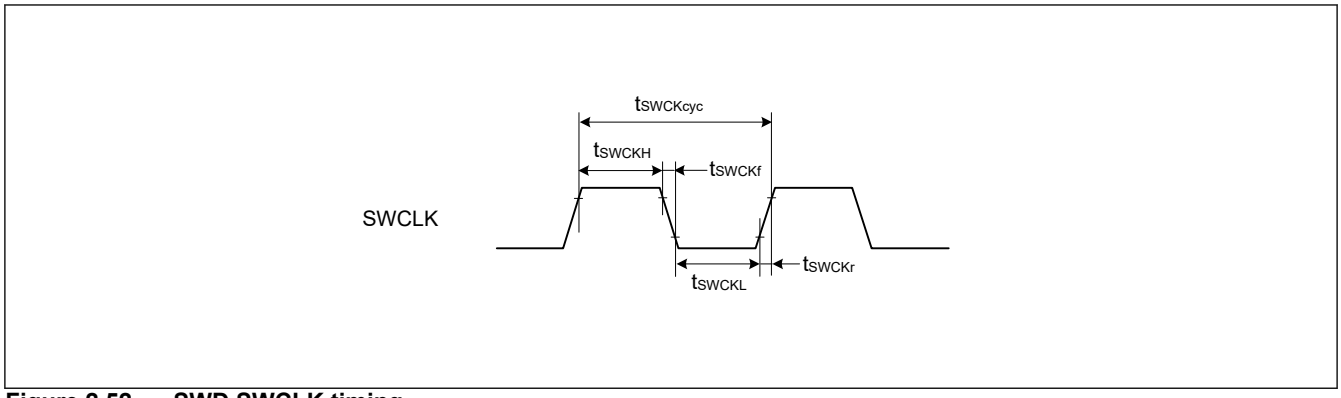


Figure 2.52 SWD SWCLK timing

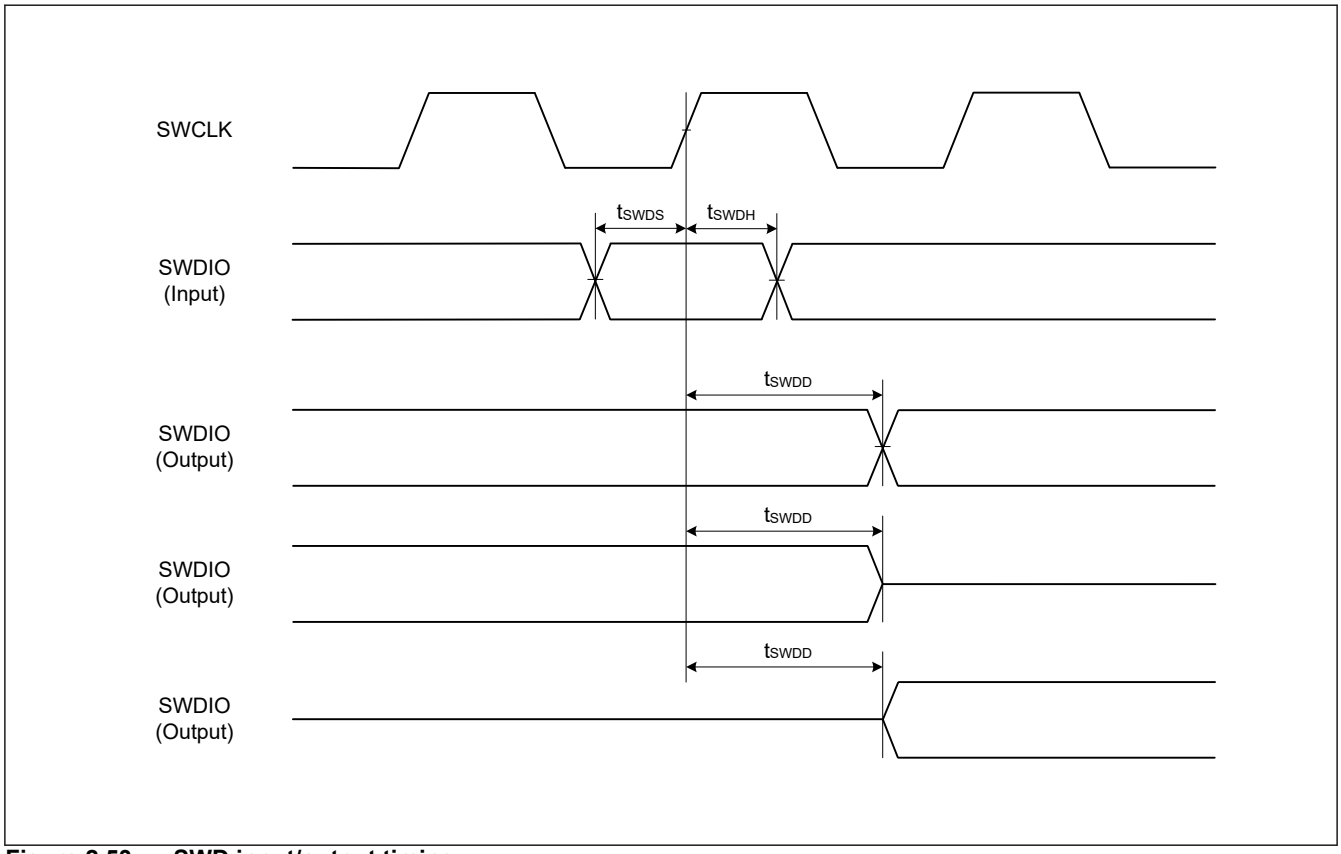


Figure 2.53 SWD input/output timing

Appendix 1. Port States in each Processing Mode

Table 1.1 Port states in each processing mode (1 of 4)

Port name	Reset	Software Standby Mode
P001/VREFH0/AN001	Hi-Z	Keep-O
P002/VREFL0/AN002	Hi-Z	Keep-O
P004/SEG44	Hi-Z	Keep-O
P005/SEG43	Hi-Z	Keep-O
P006/SEG42	Hi-Z	Keep-O
P007/SEG41	Hi-Z	Keep-O
P008/SEG40	Hi-Z	Keep-O
P009/SEG39	Hi-Z	Keep-O
P010/SEG38	Hi-Z	Keep-O
P011/SEG37/GTIOC4A	Hi-Z	Keep-O
P012/CACREF_A/SEG36/GTIOC5A_A/IRQ2_A/SCL1	Hi-Z	Keep-O*1
P013/SEG35/RXD1/MISO1/SCL1/AGTIO7/IRQ1_A/SDA1	Hi-Z	[AGTIO7 output selected] AGTIO7 output*2 [Other than the above] Keep-O*1
P014/CACREF_B/AN000/IRQ3_A	Hi-Z	Keep-O*1
P015/AN003/EXLVDVBAT	Hi-Z	Keep-O
P100/SEG13/TXD0/MOSI0/SDA0/AGTO0/AGTOA0/AGTOB0/AGTEE0/GTIU/GTIOC8A_A	Hi-Z	[AGTO0/AGTOA0/AGTOB0 output selected] AGTO0/AGTOA0/AGTOB0 output*2 [Other than the above] Keep-O
P101/SEG14/RXD0/MISO0/SCL0/AGTO1/AGTOA1/AGTOB1/AGTEE1/AGTWO0/GTIV/GTIOC8B_A	Hi-Z	[AGTO1/AGTOA1/AGTOB1/AGTWO0 output selected] AGTO1/AGTOA1/AGTOB1/AGTWO0 output*2 [Other than the above] Keep-O
P102/SEG15/ADTRG0_A/SCK0/AGTO2/AGTOA2/AGTOB2/AGTEE2/AGTWEE0/GTIW/GTIOC6A_B	Hi-Z	[AGTO2/AGTOA2/AGTOB2 output selected] AGTO2/AGTOA2/AGTOB2 output*2 [Other than the above] Keep-O
P103/SEG16/CTS0_RTS0/SS0/SSLA3/AGTO3/AGTOA3/AGTOB3/AGTEE3/AGTWIO0/GTOUUP/GTIOC6B_B	Hi-Z	[AGTO3/AGTOA3/AGTOB3/AGTWIO0 output selected] AGTO3/AGTOA3/AGTOB3/AGTWIO0 output*2 [Other than the above] Keep-O
P104/SEG24/SCK2/GTIOC8A_B	Hi-Z	Keep-O
P105/SEG25/CTS2_RTS2/SS2/GTIOC8B_B	Hi-Z	Keep-O
P106/SEG26/TXD2/MOSI2/SDA2	Hi-Z	Keep-O
P107/SEG27/RXD2/MISO2/SCL2/SSLA1_A	Hi-Z	Keep-O
P108/SWDIO/GTIOC7B/RTCOUT_B	Pull-up	[RTCOUT_B selected] RTCOUT_B output [Other than the above] Keep-O

Table 1.1 Port states in each processing mode (2 of 4)

Port name	Reset	Software Standby Mode
P109/SEG17/TXD9/MOSI9/SDA9/AGTO4/AGTOA4/AGTOB4/AGTEE4/ AGTWOB0/GTOULO/CLKOUT_B	Hi-Z	[AGTO4/AGTOA4/AGTOB4/ AGTWOB0 output selected] AGTO4/AGTOA4/AGTOB4/ AGTWOB0 output*2 [CLKOUT_B selected] CLKOUT_B output [Other than the above] Keep-O
P110/SEG18/RXD9/MISO9/SCL9/AGTO5/AGTOA5/AGTOB5/AGTEE5/ AGTWOA0/GTOVUP	Hi-Z	[AGTO5/AGTOA5/AGTOB5/ AGTWOA0 output selected] AGTO5/AGTOA5/AGTOB5/ AGTWOA0 output*2 [Other than the above] Keep-O
P111/SEG19/SCK9/AGTO6/AGTOA6/AGTOB6/AGTEE6/GTOVLO/ GTIOC5A_B	Hi-Z	[AGTO6/AGTOA6/AGTOB6 output selected] AGTO6/AGTOA6/AGTOB6 output*2 [Other than the above] Keep-O
P112/SEG20/CTS9_RTS9/SS9/SSLA2/AGTO7/AGTOA7/AGTOB7/AGTEE7/ GTOWUP/GTIOC5B_B	Hi-Z	[AGTO7/AGTOA7/AGTOB7 output selected] AGTO7/AGTOA7/AGTOB7 output*2 [Other than the above] Keep-O
P113/SEG21	Hi-Z	Keep-O
P114/SEG22	Hi-Z	Keep-O
P115/SEG23	Hi-Z	Keep-O
P200/NMI	Hi-Z	Hi-Z
P201/MD	Pull-up	Keep-O
P203/COM3	Hi-Z	Keep-O
P204/COM2	Hi-Z	Keep-O
P205/COM1	Hi-Z	Keep-O
P206/COM0	Hi-Z	Keep-O
P207/VL3	Hi-Z	Keep-O
P208/CAPL	Hi-Z	Keep-O
P209/CAPH	Hi-Z	Keep-O
P210/ADTRG0_B/GTIOC5B_A/IRQ8/CLKOUT_A	Hi-Z	[CLKOUT_A selected] CLKOUT_A output [Other than the above] Keep-O*1
P211/EXLVD	Hi-Z	Keep-O
P212/EXTAL	Hi-Z	Keep-O
P213/XTAL	Hi-Z	Keep-O
P214/XCOUT, P215/XCIN	Hi-Z	[Sub-clock Oscillator selected] Sub-clock Oscillator is operating [Other than the above] Hi-Z
P300/SWCLK /GTIOC6B_A	Pull-up	Keep-O
P301/COM4/SEG00	Hi-Z	Keep-O
P302/COM5/SEG01	Hi-Z	Keep-O
P303/COM6/SEG02	Hi-Z	Keep-O

Table 1.1 Port states in each processing mode (3 of 4)

Port name	Reset	Software Standby Mode
P304/COM7/SEG03	Hi-Z	Keep-O
P305/SEG04	Hi-Z	Keep-O
P306/SEG05/IRQ0_B	Hi-Z	Keep-O*1
P307/SEG06/IRQ1_B	Hi-Z	Keep-O*1
P308/SEG07/IRQ2_B	Hi-Z	Keep-O*1
P309/SEG08/IRQ3_B	Hi-Z	Keep-O*1
P310/SEG09/IRQ4_B	Hi-Z	Keep-O*1
P311/SEG10/IRQ5_B	Hi-Z	Keep-O*1
P312/SEG11/IRQ6_B	Hi-Z	Keep-O*1
P313/SEG12/IRQ7_B	Hi-Z	Keep-O*1
P400/RTCIC0/IRQ9	Hi-Z	Keep-O*1
P401/RTCIC1/IRQ10	Hi-Z	Keep-O*1
P402/RTCIC2/RTCOUT_A/IRQ11	Hi-Z	[RTCOUT_A output selected] RTCOUT_A output [Other than the above] Keep-O*1
P403/GTIOC4B/MISOA_B	Hi-Z	Keep-O
P404/MOSIA_B	Hi-Z	Keep-O
P405/RSPCKA_B	Hi-Z	Keep-O
P408/GTIOC9A_B/SSLA0_B	Hi-Z	Keep-O
P409/GTIOC9B_B/SSLA1_B	Hi-Z	Keep-O
P410(Nch OD)/SDA0/GTIOC6A_A	Hi-Z	Keep-O
P411(Nch OD)/SCL0/GTIOC7A	Hi-Z	Keep-O
P500/SEG28/RXD3/MISO3/SCL3/AGTIO0/AGTWEE1/GTOWLO/IRQ4_A	Hi-Z	[AGTIO0 output selected] AGTIO0 output*2 [Other than the above] Keep-O*1
P501/SEG29/TXD3/MOSI3/SDA3/AGTIO1/AGTWIO1/GTETRGA/IRQ5_A	Hi-Z	[AGTIO1/AGTWIO1 output selected] AGTIO1/AGTWIO1 output*2 [Other than the above] Keep-O*1
P502/SEG30/SCK3/RSPCKA_A/AGTIO2/AGTWO1/GTETRGB/GTIOC9A_A/IRQ6_A	Hi-Z	[AGTIO2/AGTWO1 output selected] AGTIO2/AGTWO1 output*2 [Other than the above] Keep-O*1
P503/SEG31/CTS3_RTS3/SS3/SSLA0_A/AGTIO3/AGTWOA1/GTIOC9B_A/IRQ7_A	Hi-Z	[AGTIO3/AGTWOA1 output selected] AGTIO3/AGTWOA1 output*2 [Other than the above] Keep-O*1
P504/SEG32/SCK1/MOSIA_A/AGTIO4/AGTWOB1	Hi-Z	[AGTIO4/AGTWOB1 output selected] AGTIO4/AGTWOB1 output*2 [Other than the above] Keep-O
P505/SEG33/CTS1_RTS1/SS1/MISOA_A/AGTIO5	Hi-Z	[AGTIO5 output selected] AGTIO5 output*2 [Other than the above] Keep-O

Table 1.1 Port states in each processing mode (4 of 4)

Port name	Reset	Software Standby Mode
P506/SEG34/TXD1/MOSI1/SDA1/AGTIO6/IRQ0_A	Hi-Z	[AGTIO6 output selected] AGTIO6 output*2 [Other than the above] Keep-O*1
P600	L output	Keep-O

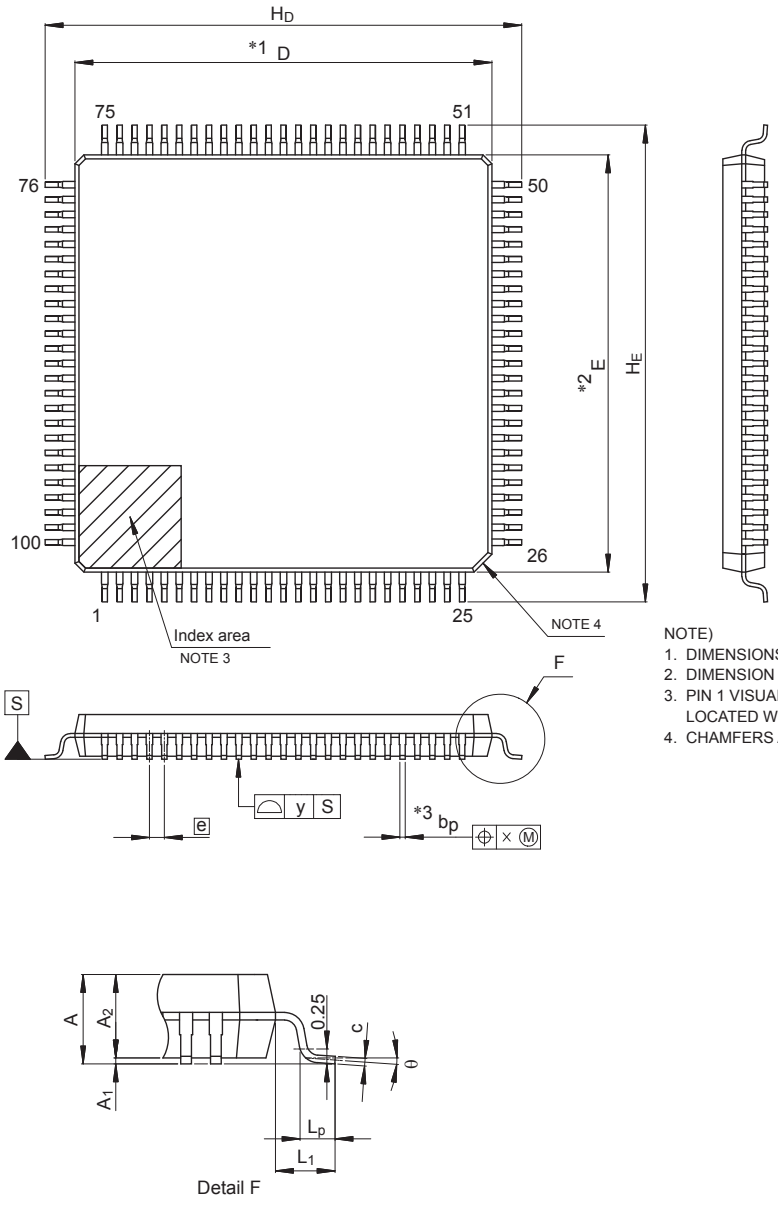
Note: Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins become high-impedance.
Retains LCD output when the LCD controller/driver pin functions (COM0 to COM7 and SEG0 to SEG44) are set and LOCO or SOSC is selected in the SLCDSCKCR.LCDSCKSEL[2:0] bits.
Note 1. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 2. AGTIO output is enabled while LOCO or SOSC is selected as a count source.

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



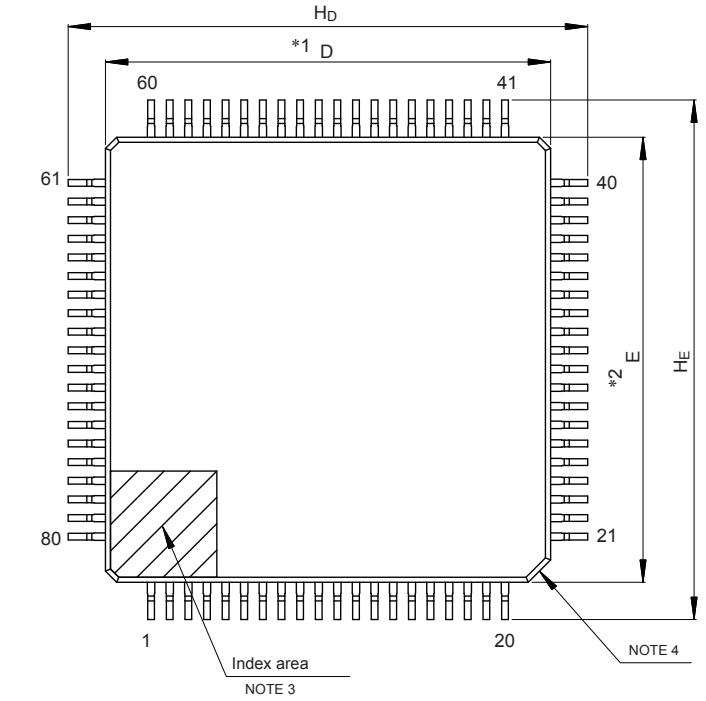
NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

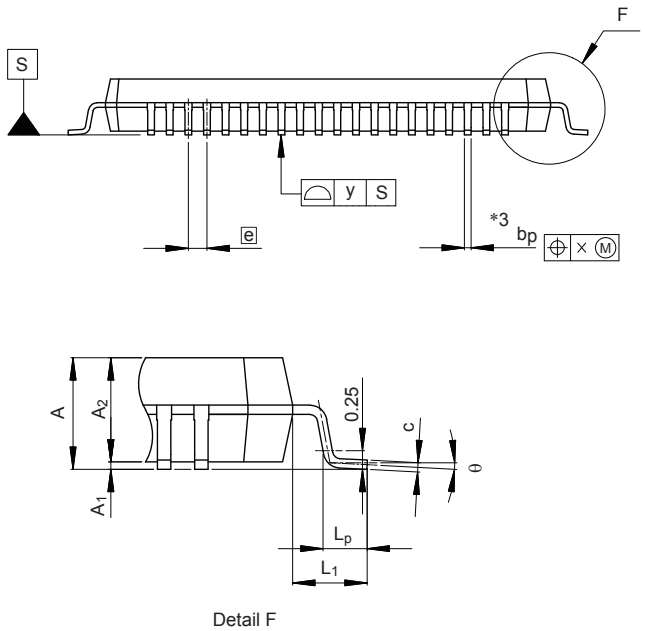
Figure 2.1 LQFP 100-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



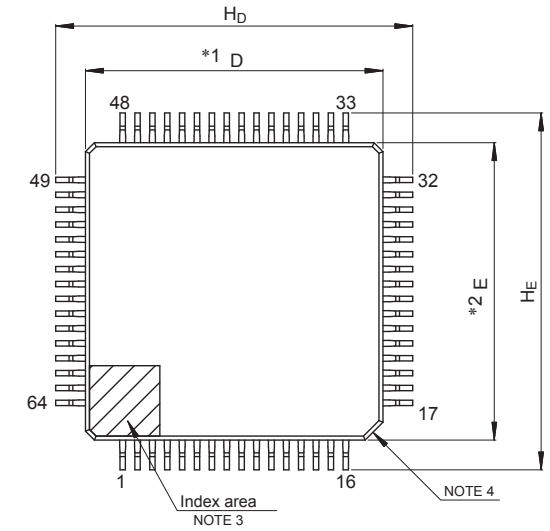
Detail F

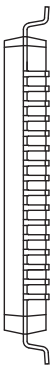
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

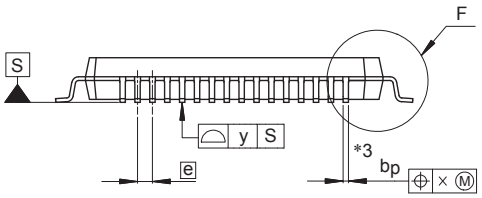
Figure 2.2 LQFP 80-pin

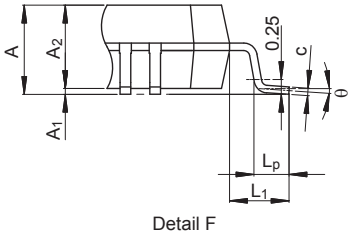
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm









Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 2.3 LQFP 64-pin

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 2)

Name	Description	Base address
MPU	Memory Protection Unit	0x4000_0000
MMF	Memory Mirror Function	0x4000_1000
SRAM	SRAM Control	0x4000_2000
BUS	BUS Control	0x4000_3000
DTC	Data Transfer Controller	0x4000_5400
ICU	Interrupt Controller	0x4000_6000
DBG	Debug Function	0x4001_B000
SYSC	System Control	0x4001_E000
PORT0	Port 0 Control Registers	0x4004_0000
PORT1	Port 1 Control Registers	0x4004_0020
PORT2	Port 2 Control Registers	0x4004_0040
PORT3	Port 3 Control Registers	0x4004_0060
PORT4	Port 4 Control Registers	0x4004_0080
PORT5	Port 5 Control Registers	0x4004_00A0
PORT6	Port 6 Control Registers	0x4004_00C0
PFS	Pmn Pin Function Control Register	0x4004_0800
ELC	Event Link Controller	0x4004_1000
POEG	Port Output Enable Module for GPT	0x4004_2000
RTC	Realtime Clock	0x4004_4000
WDT	Watchdog Timer	0x4004_4200
IWDT	Independent Watchdog Timer	0x4004_4400
CAC	Clock Frequency Accuracy Measurement Circuit	0x4004_4600
MSTP	Module Stop Control A, B, C, D	0x4004_7000
IIC0	Inter-Integrated Circuit 0	0x4005_3000
IIC0WU	Inter-Integrated Circuit 0 Wakeup Unit	0x4005_3014
IIC1	Inter-Integrated Circuit 1	0x4005_3100
DOC	Data Operation Circuit	0x4005_4100
ADC12	12-bit A/D Converter	0x4005_C000
SCI0	Serial Communication Interface 0	0x4007_0000
SCI1	Serial Communication Interface 1	0x4007_0020
SCI2	Serial Communication Interface 2	0x4007_0040
SCI3	Serial Communication Interface 3	0x4007_0060
SCI9	Serial Communication Interface 9	0x4007_0120
SPI0	Serial Peripheral Interface 0	0x4007_2000
CRC	CRC Calculator	0x4007_4000

Table 3.1 Peripheral base address (2 of 2)

Name	Description	Base address
GPT164	General PWM Timer 4 (16-bit)	0x4007_8400
GPT165	General PWM Timer 5 (16-bit)	0x4007_8500
GPT166	General PWM Timer 6 (16-bit)	0x4007_8600
GPT167	General PWM Timer 7 (16-bit)	0x4007_8700
GPT168	General PWM Timer 8 (16-bit)	0x4007_8800
GPT169	General PWM Timer 9 (16-bit)	0x4007_8900
GPT_OPS	Output Phase Switching Controller	0x4007_8FF0
SLCDC*1	Segment LCD Controller/Driver	0x4008_2000
AGTW0	32-bit Low Power Asynchronous General Purpose Timer 0	0x4008_4000
AGTW1	32-bit Low Power Asynchronous General Purpose Timer 1	0x4008_4100
AGT0	16-bit Low Power Asynchronous General Purpose Timer 0	0x4008_4200
AGT1	16-bit Low Power Asynchronous General Purpose Timer 1	0x4008_4300
AGT2	16-bit Low Power Asynchronous General Purpose Timer 2	0x4008_4400
AGT3	16-bit Low Power Asynchronous General Purpose Timer 3	0x4008_4500
AGT4	16-bit Low Power Asynchronous General Purpose Timer 4	0x4008_4600
AGT5	16-bit Low Power Asynchronous General Purpose Timer 5	0x4008_4700
AGT6	16-bit Low Power Asynchronous General Purpose Timer 6	0x4008_4800
AGT7	16-bit Low Power Asynchronous General Purpose Timer 7	0x4008_4900
SDADC24_B	24-Bit Sigma-Delta A/D Converter	0x4009_C000
MACL	32-bit Multiply-Accumulator	0x400A_0000
FLCN	Flash I/O Registers	0x407E_C000

Note: Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral
Note 1. The LCD Display Data registers are mapped from 0x4008_2100.

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table 3.2:

- Registers are grouped by associated module.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed.
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus master such as DTC.

Table 3.2 shows the register access cycles for non-GPT modules.

Table 3.2 Access cycles for non-GPT modules

Peripherals	Address		Number of access cycles				Cycle unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
MPU, MMF, SRAM, BUS, DTC, ICU, DBG	0x4000_2000	0x4001_BFFF	3				ICLK	Memory Protection Unit, Memory Mirror Function, SRAM, Buses, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory
SYSC	0x4001_E000	0x4001_E6FF	4				ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
PORTn, PFS, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	0x4004_0000	0x4004_7FFF	3		2 to 3		PCLKB	I/O Ports, Event Link Controller, Port Output Enable for GPT, Realtime Clock, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control
IICn (n = 0, 1), IIC0WU, DOC, ADC12	0x4005_3000	0x4005_CFFF	3		2 to 3		PCLKB	I^2C Bus Interface, Data Operation Circuit, 12-bit A/D Converter
SCIn (n = 0*2 to 3, 9)	0x4007_0000	0x4007_0EFF	5		2 to 3		PCLKB	Serial Communications Interface
SPI0*3	0x4007_2000	0x4007_2FFF	5		2 to 3		PCLKB	Serial Peripheral Interface
CRC	0x4007_4000	0x4007_4FFF	3		2 to 3		PCLKB	CRC Calculator
GPT16n (n = 4 to 9), GPT_OPS	0x4007_8000	0x4007_BFFF	See Table 3.3.				PCLKB	General PWM Timer
SLCDC	0x4008_0000	0x4008_2FFF	2		1 to 2		PCLKB	Segment LCD Controller/Driver
AGTWn (n = 0 to 1), AGTn (n = 0 to 7)	0x4008_4000	0x4008_4FFF	3		2 to 3		PCLKB	Low Power Asynchronous General Purpose Timer
SDADC24	0x4009_C000	0x4009_CFFF	2		1 to 2		PCLKB	24-Bit Sigma-Delta A/D Converter
MACL	0x400A_0000	0x400A_0FFF	2		2		ICLK	32-bit Multiply-Accumulator
FLCN	0x407E_C000	0x407E_FFFF	7		7		ICLK	Data Flash, Temperature Sensor, Flash Control

Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2.5 is 1 to 3.
Note 2. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.
Note 3. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.

Table 3.3 shows register access cycles for GPT modules.

Table 3.3 Access cycles for GPT modules

Frequency ratio between ICLK and PCLK	Number of access cycles		Cycle unit
	Read	Write	
ICLK > PCLKD = PCLKB	5 to 6	3 to 4	PCLKB
ICLK > PCLKD > PCLKB	3 to 4	2 to 3	PCLKB
PCLKD = ICLK = PCLKB	6	4	PCLKB
PCLKD = ICLK > PCLKB	2 to 3	1 to 2	PCLKB
PCLKD > ICLK = PCLKB	4	3	PCLKB
PCLKD > ICLK > PCLKB	2 to 3	1 to 2	PCLKB

Appendix 4. Peripheral Variant

Table 4.1 shows the correspondence between the module name used in this manual and the Peripheral Variant.

Table 4.1 Module name vs Peripheral Variant

Module name	Peripheral Variant
SDADC24	SDADC24_B

Revision History

Revision 1.00 — September 8, 2023

Initial release

Revision 1.10 — December 8, 2023

1. Overview:
- Removed NMI in Table1.16 Pin list.

41. Electrical Characteristics:
- Changed Note 1 in Table 41.1 Absolute maximum ratings.
- Changed structure of Table 41.4 I/O Table 41.4 I/O VIH, VIL
- Added Table 41.44 to Table 41.50

Appendix 3. I/O Registers:
- Changed from Module Stop Control B, C, D to Module Stop Control A, B, C, D.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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