

General Description

The AOZ2295QI-05 is a high-efficiency, easy-to-use DC/DC buck regulator that targeted for system-power supply solution. The devices are capable of supplying 12A of continuous output current with 5.1V output voltage.

The AOZ2295QI-05 integrates an independent internal linear regulator to generate 5.0V V_{REG5} from input. If input voltage is lower than 5.0V, the linear regulator operates at low drop output mode, which allows the V_{REG5} voltage is equal to input voltage minus the drop-output voltage of the internal linear regulator. When the buck regulator is enabled, the V_{REG5} will be switch-over to output for saving LDO power consumption.

A proprietary constant on-time PWM control with input feed-forward results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input voltage range.

The device features multiple protection functions such as LDO under-voltage lockout, cycle-by-cycle current limit, output over-voltage protection, short-circuit protection, and thermal shutdown.

The AOZ2295QI-05 is available in a 4mm×4mm QFN-31L package and is rated over a -40°C to +85°C ambient temperature range.

Features

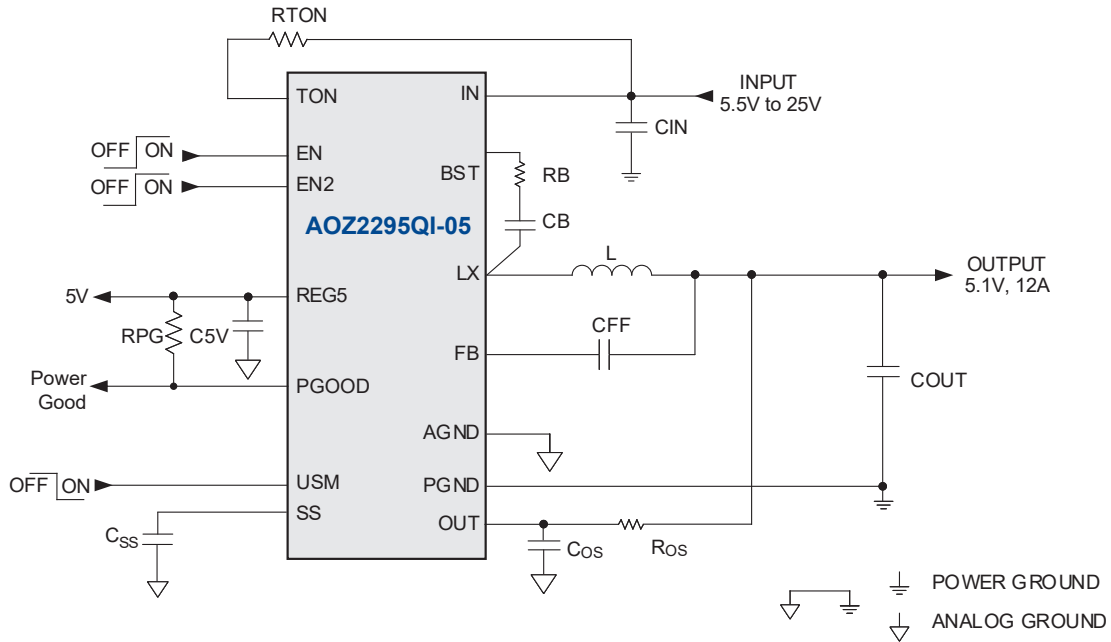
- Wide input voltage range
 - 5.5V to 25V
- 12A continuous output current
- 16A output peak current
- Output voltage: 5.1V ±2.5%
- Low RDS(ON) internal NFETs
 - 7mΩ high-side
 - 3.6mΩ low-side
- 5V LDO Output
- Constant On-Time with input feed-forward
- Ripple Reduction at light load
- Ton Extension Mode
- Ultrasonic Mode
- Ceramic capacitor stable
- Adjustable soft start
- Power Good output
- Integrated bootstrap diode
- Cycle-by-cycle current limit
- Short-circuit protection
- Thermal shutdown
- Thermally enhanced 31-pin 4mm× 4mm QFN

Applications

- Notebook computers
- Tablet computers



Typical Application



Recommended BOM List

Part	Value
CIN	20 μ F
COUT	132 μ F
RTON	430k Ω
RPG	100k Ω
C5V	4.7 μ F
CSS	10nF
CFF	75pF
RB	3.3 Ω
CB	100nF
L	1.0 μ H
ROS	1 Ω
COS	100nF

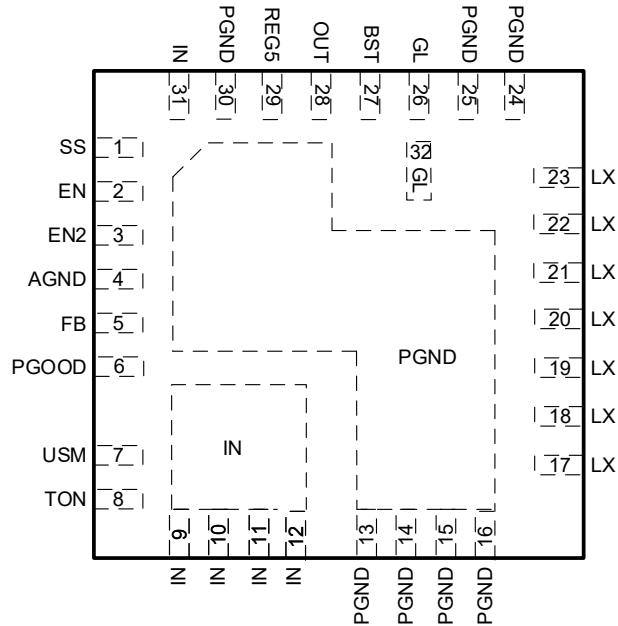
Ordering Information

Part Number	Temperature Range	Package	Environmental
AOZ2295QI-05	-40°C to +85°C	31-Pin 4mm x 4mm QFN	Green



AOS products are offered in packages with Pb-free plating and compliant to RoHS standards. Please visit <https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf> for additional information.

Pin Configuration



AOZ2295QI-05
31-Pin 4mm x 4mm QFN

Pin Description

Pin Number	Pin Name	Pin Function
1	SS	Soft-Start Time Setting Pin. Connect a capacitor between SS and AGND to set the soft-start time.
2	EN	Enable Input. The device is enabled when EN is pulled high. The device shuts down when EN is pulled low. Assert EN to high for power-up after IN is supplied.
3	EN2	Internal 5V LDO Enable Input. The 5V LDO is enabled when EN2 is pulled high. The 5V LDO shuts down when EN2 is pulled low. Connect this pin with EN signal if individually LDO control is no needed.
4	AGND	Analog Ground.
5	FB	Feedback Input. Adjust the output voltage with a resistive voltage-divider between the regulator's output and AGND.
6	PGOOD	Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 10% lower than the nominal regulation voltage or 20% higher than the nominal regulation voltage. PGOOD is pulled low during soft-start and shut down.
7	USM	Ultrasonic mode selection. Pull this pin low to enable ultrasonic mode. Connect this pin to REG5 directly to disable ultrasonic mode.
8	TON	On-Time Setting Input. Connect a resistor between VIN and TON to set the on time.
9, 10, 11, 12, 31	IN	Supply Input. IN is the regulator input. All IN pins must be connected together.
13, 14, 15, 16, 24, 25, 30	PGND	Power Ground.
17, 18, 19, 20, 21, 22, 23	LX	Switching Node.
26, 32	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
27	BST	Bootstrap Capacitor Connection. The device includes an internal bootstrap diode. Connect an external capacitor between BST and LX.
28	OUT	Output Voltage Input.
29	REG5	Internal 5V LDO output for analog functions. Bypass REG5 to AGND with a 4.7 μ F~10 μ F ceramic capacitor. Place the capacitor close to REG5 pin.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
IN, TON to AGND	-0.3V to 27V
LX to AGND ⁽¹⁾	-0.7V to 27V
BST to AGND	-0.3V to 33V
PGND to AGND	-0.3V to +0.3V
Other Pins to AGND	-0.3V to 6V
Junction Temperature (T _J)	+150°C
Storage Temperature (T _S)	-65°C to +150°C
ESD Rating-HBM ⁽²⁾	2kV
ESD Rating-CDM	1kV

Notes:

- LX to PGND Transient (t<20ns) ----- -7V to Vin+7V.
- Devices are inherently ESD sensitive, handling precautions are required.
Human body model rating: 1.5KΩ in series with 100pF.

Maximum Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

Parameter	Rating
Supply Voltage (V _{IN})	5.5V to 25V
Ambient Temperature (T _A)	-40°C to +85°C
Package Thermal Resistance (θ _{JA}) (θ _{JC})	32°C/W 4°C/W

Electrical Characteristics

T_A = 25°C, V_{IN} = 12V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

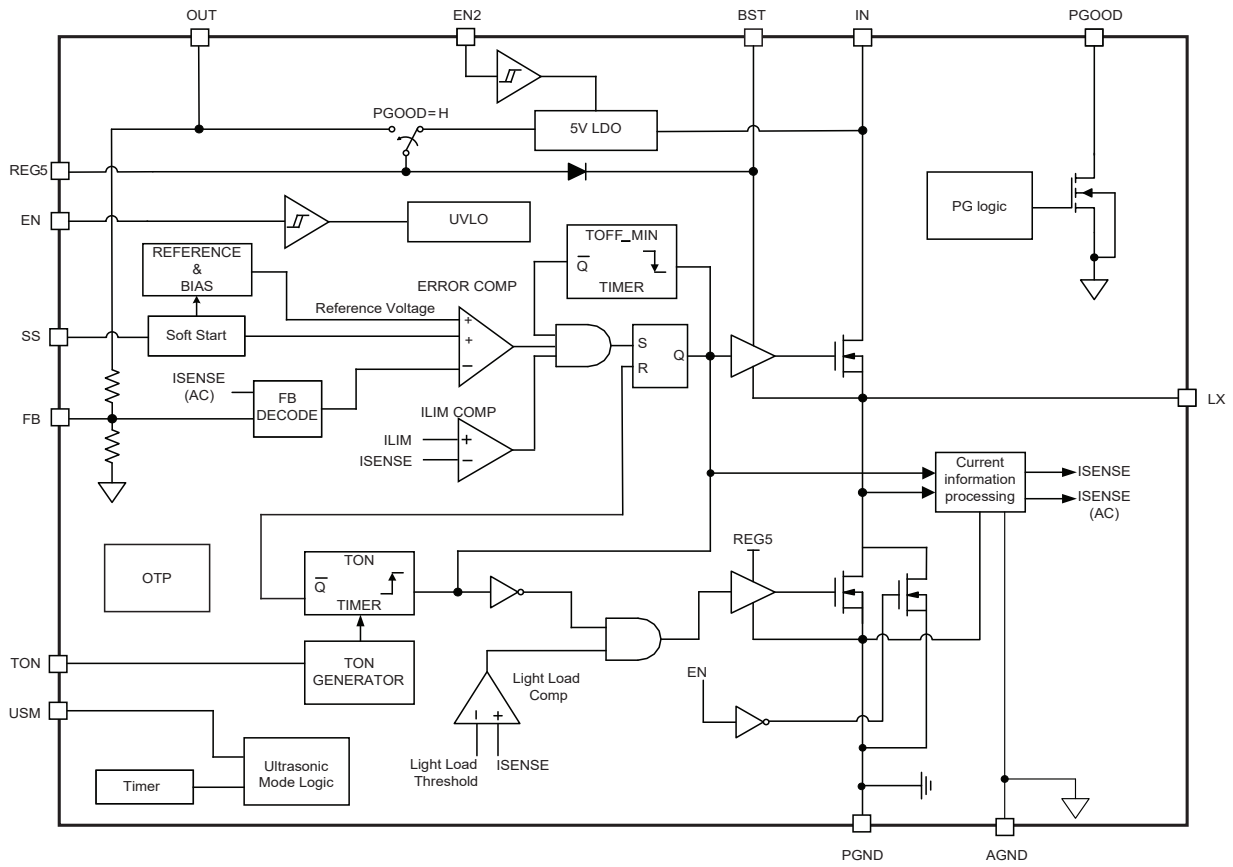
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IN}	IN Supply Voltage		5.5		25	V
V _{UVLO}	Under-Voltage Lockout Threshold of V _{REG5}	V _{REG5} rising V _{REG5} falling	3.4	4.2 3.9	4.7	V
I _q	Quiescent Supply Current of V _{REG5}	I _{OUT} = 0A, V _{EN} > 2V, PFM mode		200		μA
I _{OFF}	Shutdown Supply Current of V _{IN}	V _{EN} = 0V, V _{EN2} = 0V		20		μA
V _{FB}	Reference Voltage			2.04		V
V _{OUT}	Output Voltage	C _{OUT} = 88μF	4.947	5.1	5.253	V
Enable						
V _{EN}	EN Input Threshold (5.1V Converter)	Off threshold On threshold	1.6		0.5	V
V _{EN_HYS}	EN Input Hysteresis			300		mV
V _{EN2}	EN2 Input Threshold (5V LDO)	Off threshold On threshold	1.6		0.5	V
V _{EN2_HYS}	EN2 Input Hysteresis			300		mV
Ultrasonic Mode						
V _{USM}	USM Input Threshold	Off threshold On threshold	1.6		0.5	V
V _{USM_HYS}	USM Input Hysteresis			300		mV
T _{USM}	Switching Period at Ultrasonic Mode	USM pin = L		30		μs
V _{USM_OUT}	Threshold for Exit Ultrasonic Mode	USM pin = L, FB falling		1.96		V

Electrical Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $EN = 5\text{V}$, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to $+85^\circ\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Modulator						
T_{ON_MIN}	Minimum On Time			100		ns
T_{ON_MAX}	Maximum On Time			5000		ns
T_{OFF_MIN}	Minimum Off Time			300		ns
Soft-Start						
I_{SS_OUT}	SS Source Current	$V_{SS} = 0$, $C_{SS} = 0.001\mu\text{F}$ to $0.1\mu\text{F}$	7	10	13	μs
Power Good Signal						
V_{PG_LOW}	PGOOD Low Voltage	$I_{OL} = 500\mu\text{A}$			0.5	V
	PGOOD Leakage Current				± 1	μs
V_{PGH}	PGOOD Threshold (Low level to High level)	FB rising		95		%
V_{PGL}	PGOOD Threshold (High level to Low level)	FB rising FB falling		120 80		
Under Voltage and Over Voltage Protection						
V_{PL}	Under Voltage Threshold	FB falling		50		%
V_{PH}	Over Voltage Threshold	FB rising		120		%
Power Stage Output						
$R_{DS(ON)}$	High-Side NFET On-Resistance	$V_{IN} = 12\text{V}$, $V_{REG5} = 5\text{V}$		7		$\text{m}\Omega$
	High-Side NFET Leakage	$V_{EN} = 0\text{V}$, $V_{LX} = 0$			10	μA
$R_{DS(ON)}$	Low-Side NFET On-Resistance	$V_{LX} = 12\text{V}$, $V_{REG5} = 5\text{V}$		3.6		$\text{m}\Omega$
	Low-Side NFET Leakage	$V_{EN} = 0\text{V}$			10	μA
Over-current and Thermal Protection						
I_{LIM}	Current Limit	$V_{OUT} = 5.1\text{V}$	18			A
	Thermal Shutdown Threshold	T_J rising T_J falling		150 100		$^\circ\text{C}$
LDO Output						
V_{REG5}	LDO Output Voltage	$V_{EN} = 5\text{V}$, $V_{REG5} = 5\text{V}$, $I_{CC} < 35\text{mA}$	4.85	5.0	5.10	V
I_{REG5_lim}	LDO Current Limit	$V_{OUT} = 0\text{V}$, $V_{REG5} = 5\text{V}$	50	100		mA
Output Discharge						
R_{DIS}	Discharge Resistance	$V_{EN} = 0\text{V}$, $V_{LX} = 0.1\text{V}$,		100		Ω
TON Extension Mode						
TON Extension Mode Threshold	V_{TEM}	V_{IN} falling		7.0		V

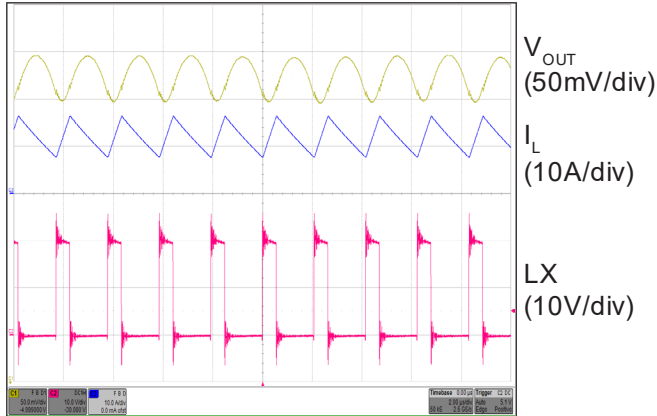
Functional Block Diagram



Typical Characteristics

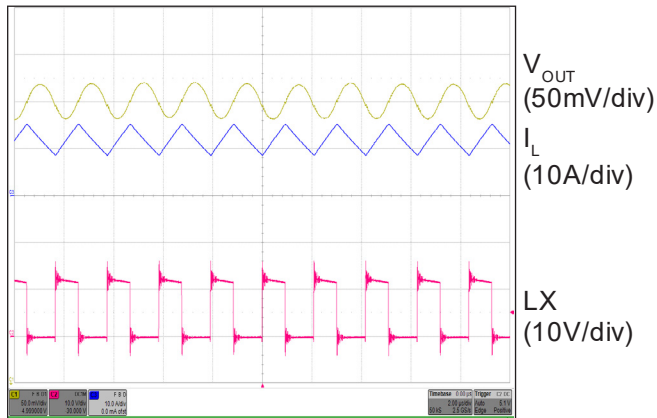
$T_A = 25^\circ\text{C}$, $V_{IN} = 6\text{V}/8\text{V}/12\text{V}/20\text{V}$, $V_{OUT} = 5.1\text{V}$, $f_s = 500\text{kHz}$, $L = 1.0\mu\text{H}$, $C_{OUT} = 22\mu\text{F} \times 6$, unless otherwise specified.

Normal Operation
($V_{IN} = 20\text{V}$, $I_{OUT} = 12\text{A}$)



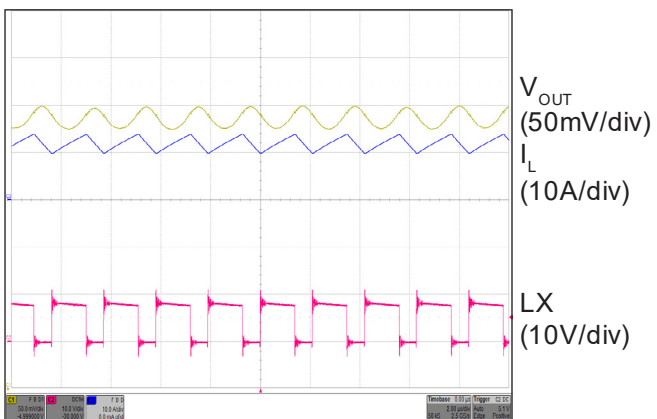
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Normal Operation
($V_{IN} = 12\text{V}$, $I_{OUT} = 12\text{A}$)



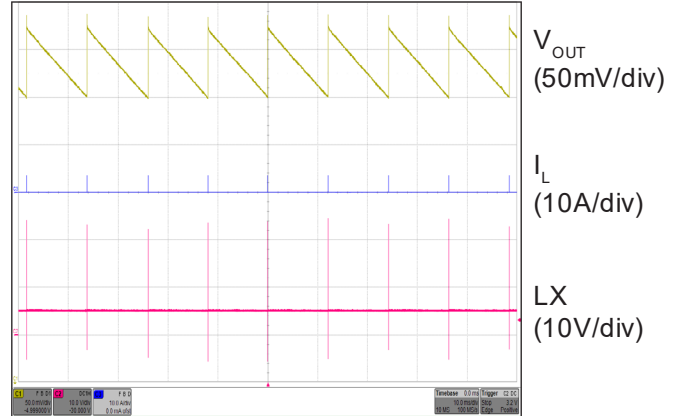
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Normal Operation
($V_{IN} = 8\text{V}$, $I_{OUT} = 12\text{A}$)



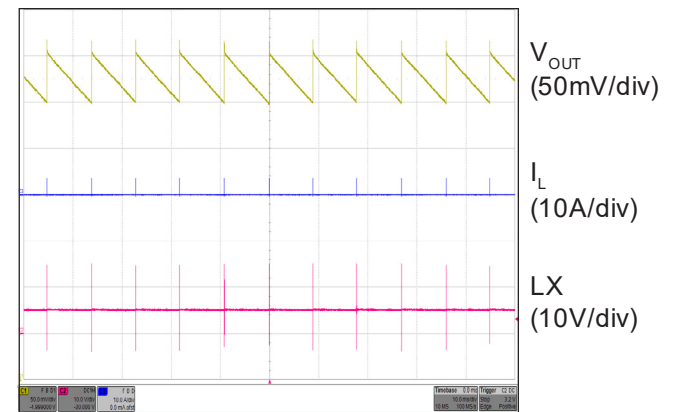
2.0µs/div

Normal Operation
($V_{IN} = 20\text{V}$, $I_{OUT} = 0\text{A}$)



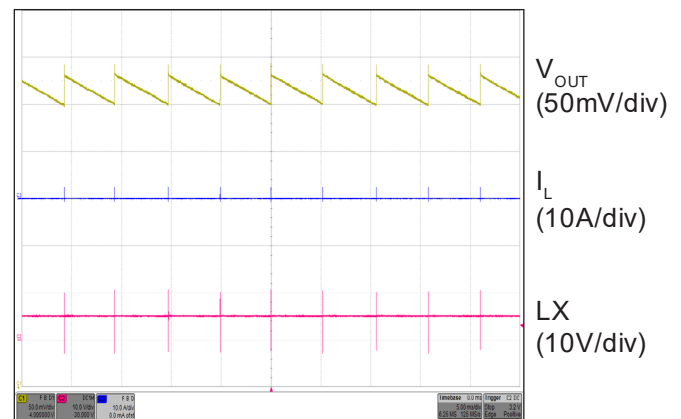
10.0ms/div

Normal Operation
($V_{IN} = 12\text{V}$, $I_{OUT} = 0\text{A}$)



10.0ms/div

Normal Operation
($V_{IN} = 8\text{V}$, $I_{OUT} = 0\text{A}$)

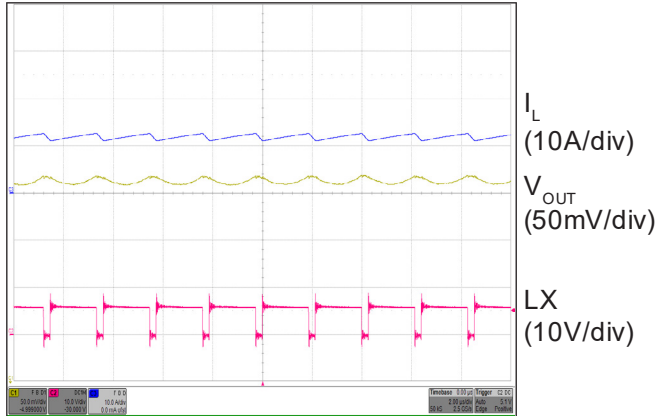


5.00ms/div

Typical Characteristics

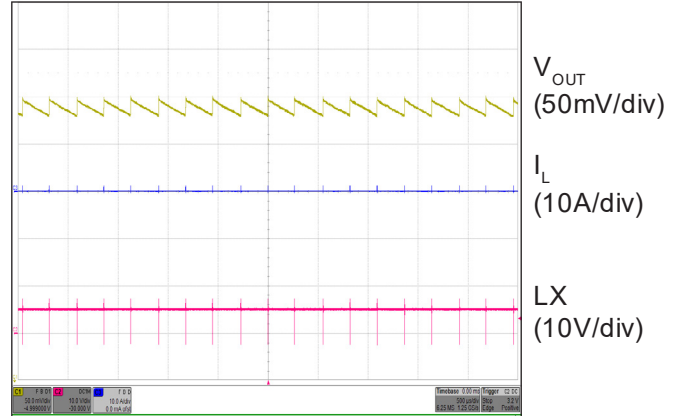
$T_A = 25^\circ\text{C}$, $V_{IN} = 6\text{V}/8\text{V}/12\text{V}/20\text{V}$, $V_{OUT} = 5.1\text{V}$, $f_s = 500\text{kHz}$, $L = 1.0\mu\text{H}$, $C_{OUT} = 22\mu\text{F} \times 6$, unless otherwise specified.

Normal Operation
($V_{IN} = 6\text{V}$, $I_{OUT} = 12\text{A}$)



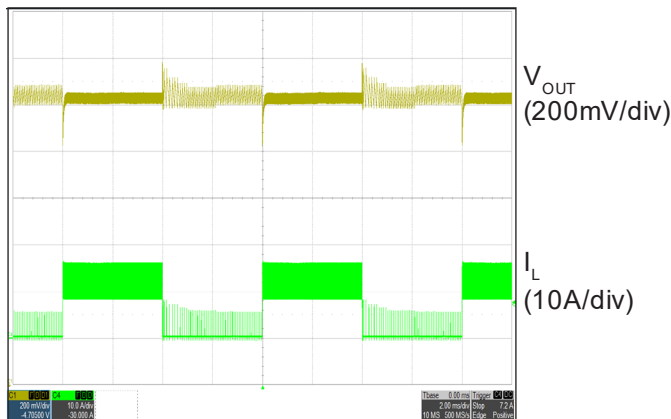
2.00 $\mu\text{s}/\text{div}$

Normal Operation
($V_{IN} = 6\text{V}$, $I_{OUT} = 0\text{A}$)



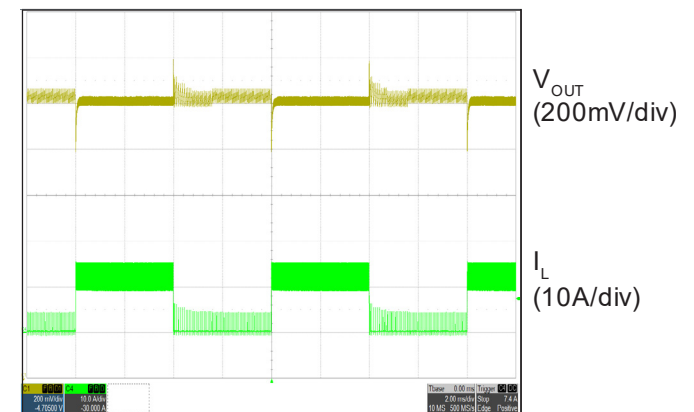
500 $\mu\text{s}/\text{div}$

Load Transient
($V_{IN} = 20\text{V}$, $I_{OUT} = 0\text{A} \sim 12\text{A}$ @ $\text{SR} = 2.5\text{A}/\mu\text{s}$)



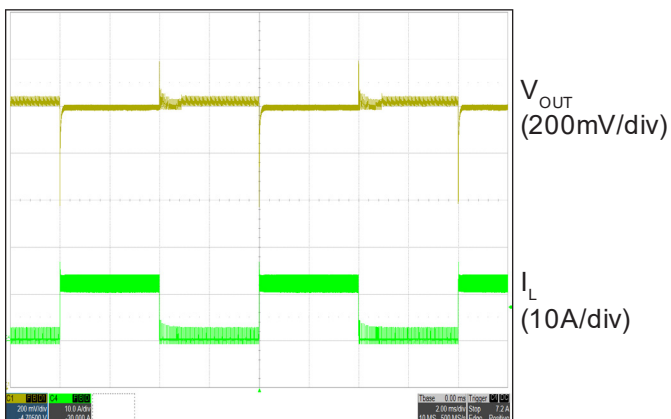
2.00ms/div

Load Transient
($V_{IN} = 12\text{V}$, $I_{OUT} = 0\text{A} \sim 12\text{A}$ @ $\text{SR} = 2.5\text{A}/\mu\text{s}$)



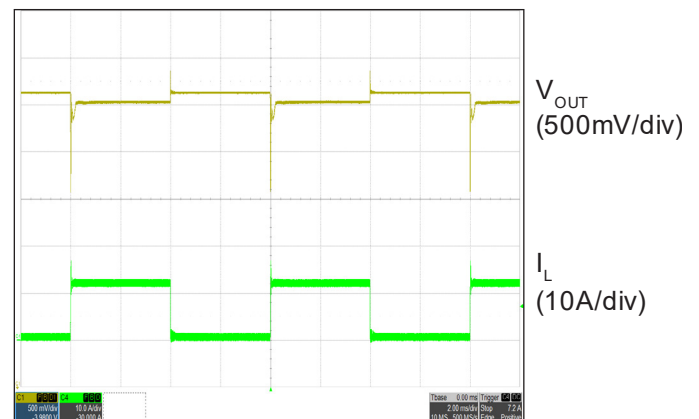
2.00ms/div

Load Transient
($V_{IN} = 8\text{V}$, $I_{OUT} = 0\text{A} \sim 12\text{A}$ @ $\text{SR} = 2.5\text{A}/\mu\text{s}$)



2.00ms/div

Load Transient
($V_{IN} = 6\text{V}$, $I_{OUT} = 0\text{A} \sim 12\text{A}$ @ $\text{SR} = 2.5\text{A}/\mu\text{s}$)

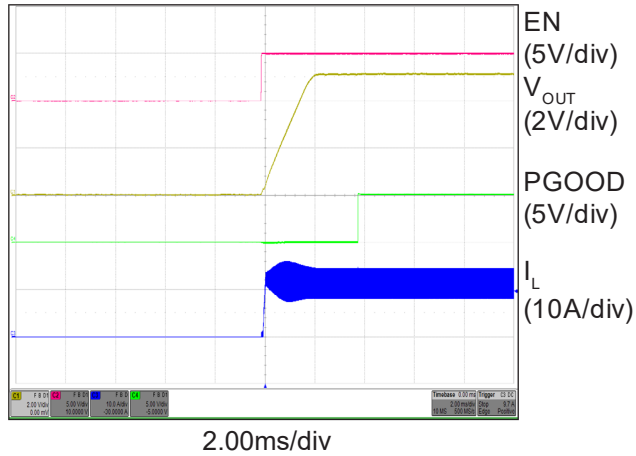


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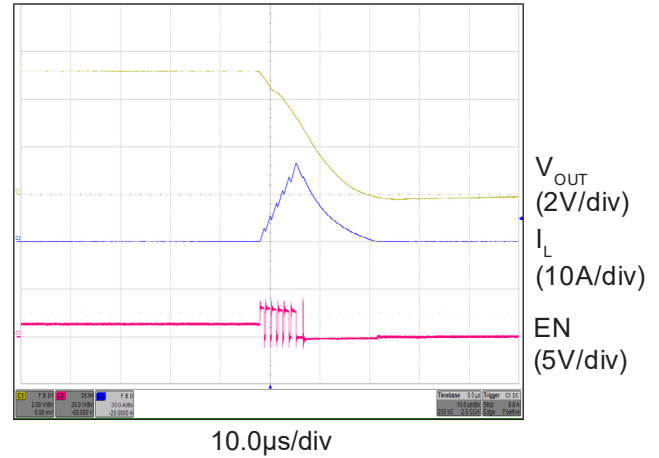
Typical Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 6\text{V}/8\text{V}/12\text{V}/20\text{V}$, $V_{OUT} = 5.1\text{V}$, $f_s = 500\text{kHz}$, $L = 1.0\mu\text{H}$, $C_{OUT} = 22\mu\text{F} \times 6$, unless otherwise specified.

Soft Start Delay Time
($V_{IN} = 5\text{V}$, $R_{OUT} = 0.6\Omega$)



Soft Start Delay Time
($V_{IN} = 20\text{V}$, $R_{OUT} = 2.8\Omega$)



Typical Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN} = 6\text{V}/8\text{V}/12\text{V}/20\text{V}$, $V_{OUT} = 5.1\text{V}$, $f_s = 500\text{kHz}$, $L = 1.0\mu\text{H}$, $C_{OUT} = 22\mu\text{F} \times 6$, unless otherwise specified.

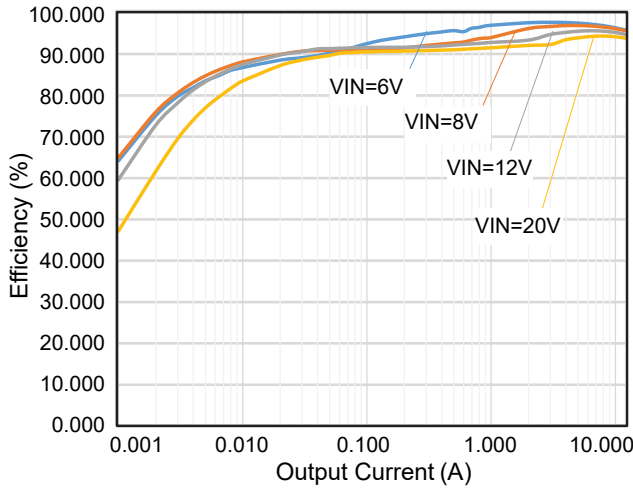


Figure 1. Efficiency
 $V_{OUT} = 6\text{V}/8\text{V}/12\text{V}/20\text{V}$, $I_{OUT} = 1\text{mA} \sim 12\text{A}$

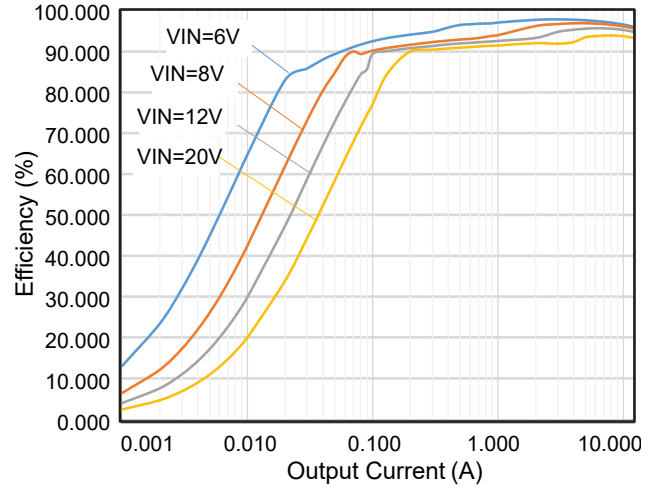


Figure 2. Efficiency (USM)
 $V_{OUT} = 6\text{V}/8\text{V}/12\text{V}/20\text{V}$, $I_{OUT} = 1\text{mA} \sim 12\text{A}$

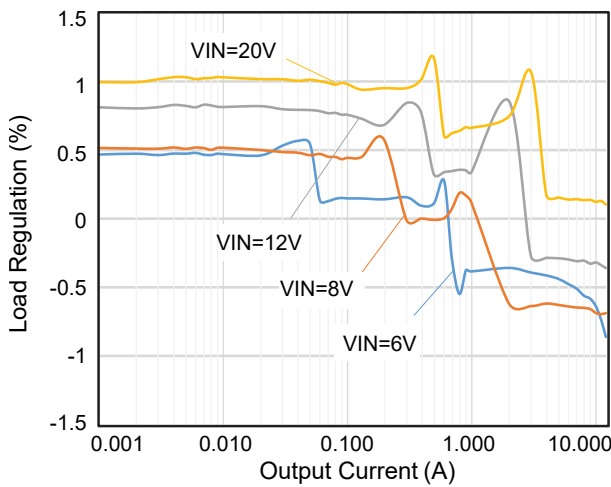


Figure 3. Load Regulation
 $V_{OUT} = 6\text{V}/8\text{V}/12\text{V}/20\text{V}$, $I_{OUT} = 1\text{mA} \sim 12\text{A}$

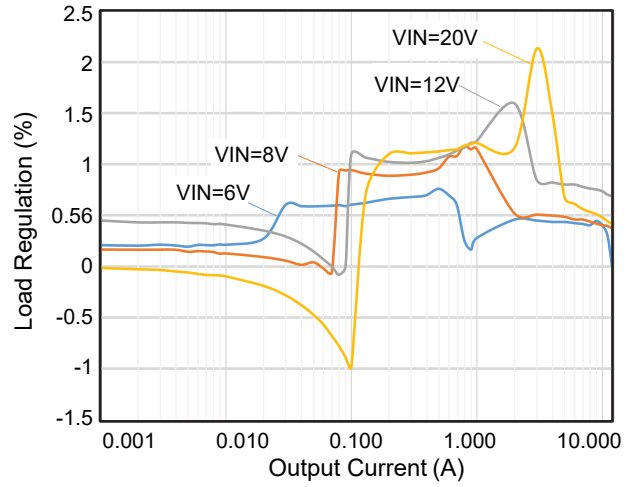


Figure 4. Load Regulation (USM)
 $V_{OUT} = 6\text{V}/8\text{V}/12\text{V}/20\text{V}$, $I_{OUT} = 1\text{mA} \sim 12\text{A}$

Detailed Description

The AOZ2295QI-05 is a high-efficiency, easy-to-use DC/DC buck regulator that targeted for system-power supply solution. The devices are capable of supplying 12A of continuous output current with 5.1V output voltage.

The input voltage of AOZ2295QI-05 can be as low as 5.5V. The highest input voltage of AOZ2295QI-05 can be 25V. Constant on-time PWM with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. True AC current mode control scheme guarantees the regulators can be stable with ceramics output capacitor. Protection features include LDO under-voltage lockout, cycle-by-cycle current limit, output over voltage and under-voltage protection, short-circuit protection, and thermal shutdown.

The AOZ2295QI-05 is available in 31-pin 4mm×4mm QFN package

Enable and Soft Start

The AOZ2295QI-05 has external soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulate voltage. A soft start process begins when V_{REG5} rises to over than UVLO threshold and the EN pin voltage is HIGH. An internal current source charges the external soft-start capacitor; the FB voltage follows the voltage of soft-start pin (V_{SS}) when it is lower than 2.04V. When V_{SS} is higher than 2.04V, the FB voltage is regulated by internal precise band-gap voltage (2.04V). When V_{SS} is higher than 3.8V, the PGOOD signal is pulled high. The soft-start time for PGOOD can be calculated by the following formula:

$$T_{SS}(\mu s) = 420 * C_{SS}(nF)$$

If C_{SS} is 1nF, the PGOOD high time will be 420μ seconds;
if C_{SS} is 10nF, the PGOOD high time will be 4.2m seconds.

The soft-start time for VOUT ready can be calculated by the following formula:

$$T_{SS}(\mu s) = 220 * C_{SS}(nF)$$

If C_{SS} is 1nF, the VOUT ready time will be 220μ second;
if C_{SS} is 10nF, the VOUT ready time will be 2.2m second.

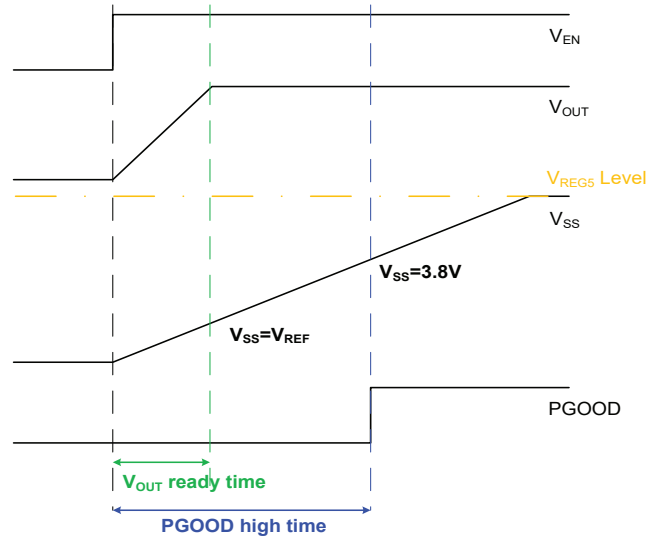


Figure 5. Soft Start Sequence of AOZ2295QI-05

Constant-On-Time PWM Control with Input Feed-Forward

The control algorithm of AOZ2295QI-05 is constant-on-time PWM control with input feed-forward. The simplified control schematic is shown in Figure 6. The high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage (I_N). The one-shot is triggered when the internal V_{REF} is higher than the combined information of FB voltage and the AC current information of inductor, which is processed and obtained through the sensed low-side MOSFET current once it turns-on. The added AC current information can help the stability of constant-on time control even with pure ceramic output capacitors, which have very low ESR. The AC current information has no DC offset, which does not cause offset with output load change, which is fundamentally different from other V^2 constant-on time control schemes.

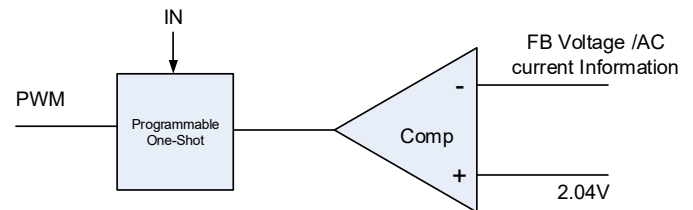


Figure 6. Simplified Control Schematic of AOZ2295QI-05

The constant-on-time PWM control architecture is a pseudo-fixed frequency with input voltage feed-forward. The internal circuit of AOZ2295QI-05 sets the on-time of high-side switch inversely proportional to the I_N .

$$T_{on} \propto \frac{R_{ton} (\Omega)}{V_{in} (V)}$$

To achieve the flux balance of inductor, the buck converter has the equation:

$$F_{sw} = \frac{V_{out}}{V_{in} * T_{on}}$$

Once the product of $V_{in} * T_{on}$ is constant, the switching frequency keeps constant and is independent with input voltage.

An external resistor between the IN and TON pin sets the switching on-time according to the following equation:

$$T_{on} (ns) = \frac{R_{TON} (k\Omega)}{V_{in} (V)} \cdot 25$$

A further simplified equation will be:

$$F_{sw} (KHz) = \frac{V_{out}}{V_{in} * T_{on} (ns)} \cdot 10^6 = \frac{V_{out} (V)}{R_{TON} (k\Omega)} \cdot 4 \cdot 10^4$$

If V_{OUT} is 5.1V, and set $F_{SW}=500$ kHz. According to the above equation, we can find out R_{TON} is 408k Ω . Notice that the frequency would be slightly increased due to the voltage dropping at the resistance of power trace.

This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator.

True Current Mode Control

The constant-on-time control scheme is intrinsically unstable if output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually cannot be used as output capacitor. The AOZ2295QI-05 senses the low-side MOSFET current and processes it into DC current and AC current information using AOS proprietary technique. The AC current information is decoded and added on the FB pin on phase. With AC current information, the stability of constant-on-time control is significantly improved even without the help of output capacitor's ESR; and thus the pure ceramic capacitor solution can be applicant. The pure ceramic capacitor solution can significantly reduce the output ripple (no ESR caused overshoot and undershoot) and less board area design.

Current-Limit Setting

The AOZ2295QI-05 has the current-limit protection by using R_{dson} of the low-side MOSFET to be as current sensing. To detect real current information, a minimum constant off time (300ns typical) is implemented after a constant-on time. If the current exceeds the current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by

an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and input and output voltages. The current limit will keep the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces below the current limit.

After 16 switching cycles, the AOZ2295QI-05 considers this is a true failed condition and thus turns-off both high-side and low-side MOSFET and latches off. Only when triggered, the enable can restart the AOZ2295QI-05 again.

Output Voltage Under-voltage Protection

If the output voltage is lower than 50% by over-current or short circuit, AOZ2295QI-05 will turns-off both high-side and low-side MOSFET immediately then latches off. Only when triggered, the enable can restart the AOZ2295QI-05 again.

Output Voltage Over-voltage Protection

The threshold of OVP is set 20% higher than 2V. When the VFB voltage exceeds the OVP threshold, high-side MOSFET is turned-off and low-side MOSFETs is turned-on 1 μ s, then latch-off.

Power Good Output

The power good (PGOOD) output, which is an open drain output, requires the pull-up resistor. When the output voltage is 20% below than the nominal regulation voltage for, the PGOOD is pulled low. When the output voltage is 20% higher than the nominal regulation voltage, the PGOOD is also pulled low. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance

PFM Mode Operation

The AOZ2295QI-05 enables pulse-frequency modulation (PFM) mode when the inductor current decreases to be across zero. In PFM operation, the conduction period of low-side MOSFET is ended at the moment that inductor current approaches zero. The output voltage slowly decreases without the low-side MOSFET discharge path until FB voltage reaches V_{REF} . As a result, the switching frequency is decreased along with the load current decreases. PFM mode increases output voltage ripple but reduces switching loss to improve efficiency for light-load.

Ripple Reduction

When switching frequency at PFM mode is down to 50% of the original setting, AOZ2295QI-05 actively decreases on-time pulse width to reduce inductor current ripple and output voltage ripple. On-time pulse width can shrink to 70% of origin after this mechanism executes 3 times at most.

Ultrasonic Mode

In PFM mode operation, the switching frequency is possibly in the audible range (20Hz~20kHz) at an extreme low load current. The AOZ2295QI-05 provides ultrasonic mode to prevent audible noise problem. When USM pin is pulled low, the AOZ2295QI-05 allows to enable ultrasonic mode when the switching frequency of PFM mode decreased to be closed to audible range. The judgments and actions of this mode are described as below:

1. PFM mode: Once the switching period is detected to be over than 40μS, the mode moves to ultrasonic mode from next cycle.
2. Ultrasonic mode: Disable FB judgment in this mode. The controller is forced to enter next switching cycle once the switching period reaches 30μS. Meanwhile, the conduction time of low-side MOSFET is also increased to release excessive energy. When output voltage drops to V_{USM_OUT} because of load current rising, the operating mode moves to PFM mode immediately.

TON Extension Mode

When AOZ2295QI-05 works with a low input voltage (ex. low battery mode), the output voltage would drop due to the limitation of minimum off-time. In order to remain output voltage in target level, if the input voltage is lower than V_{TEM} , AOZ2295QI-05 enables TON extension mode to extend on-time until the feedback voltage rise back to the reference voltage.

Application Information

The basic AOZ2295QI-05 application circuit is shown in Typical Application section. Component selection is explained below.

Input Capacitor

The input capacitor must be connected to the IN pins and PGND pin of the AOZ2295QI-05 to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor, usually 4.7μF, should be connected to the V_{REG5} pin and AGND pin for stable operation of the AOZ2295QI-05. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_{OUT}}{f \times C_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

if let m equal the conversion ratio:

$$\frac{V_{OUT}}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure. 7. It can be seen that when V_{OUT} is half of V_{IN} , C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_{OUT}$.

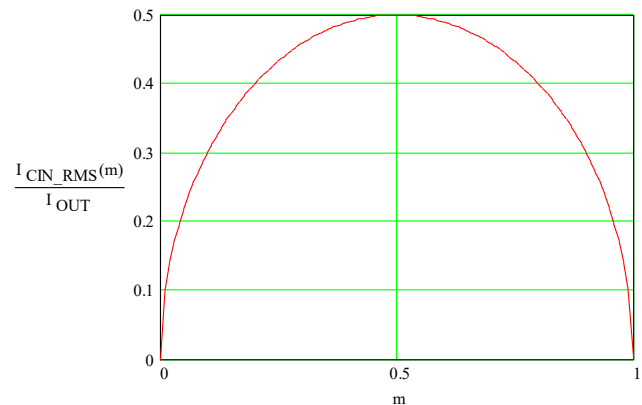


Figure 7. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than I_{CIN_RMS} at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is,

$$\Delta I_L = \frac{V_{OUT}}{f \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{L_{peak}} = I_{OUT} + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_{OUT} = \Delta I_L \times \frac{1}{8 \times f \times C_{OUT}}$$

where C_{OUT} is output capacitor value and $ESR_{C_{OUT}}$ is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_{OUT} = \Delta I_L \times (ESR_{C_{OUT}} + \frac{1}{8 \times f \times C_{OUT}})$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{C_{OUT}}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{C_{OUT_RMS}} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Thermal Management and Layout Consideration

In the AOZ2295QI-05 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the IN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low side switch. Current flows in the second loop when the low side low side switch is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ2295QI-05.

In the AOZ2295QI-05 buck regulator circuit, the major power dissipating components are the AOZ2295QI-05 and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total_loss} = V_{IN} \cdot I_{IN} - V_{OUT} \cdot I_{OUT}$$

The power dissipation of inductor can be approximately calculated by DCR of inductor and output current.

$$P_{inductor_loss} = I_{OUT}^2 \cdot R_{inductor} \cdot I.I$$

The actual junction temperature can be calculated with power dissipation in the AOZ2295QI-05 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total_loss} - P_{inductor_loss}) \cdot \theta_{JA} + T_A$$

The maximum junction temperature of AOZ2295QI-05 is 150°C, which limits the maximum load current capability.

When AOZ2295QI-05 operates at the ambient temperature -40°C condition, the external components must cover the -40°C temperature condition. For example: the capacitor must use X-series type components to cover -40°C temperature condition, which can avoid the system unstable by capacitance reduction.

The thermal performance of the AOZ2295QI-05 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions

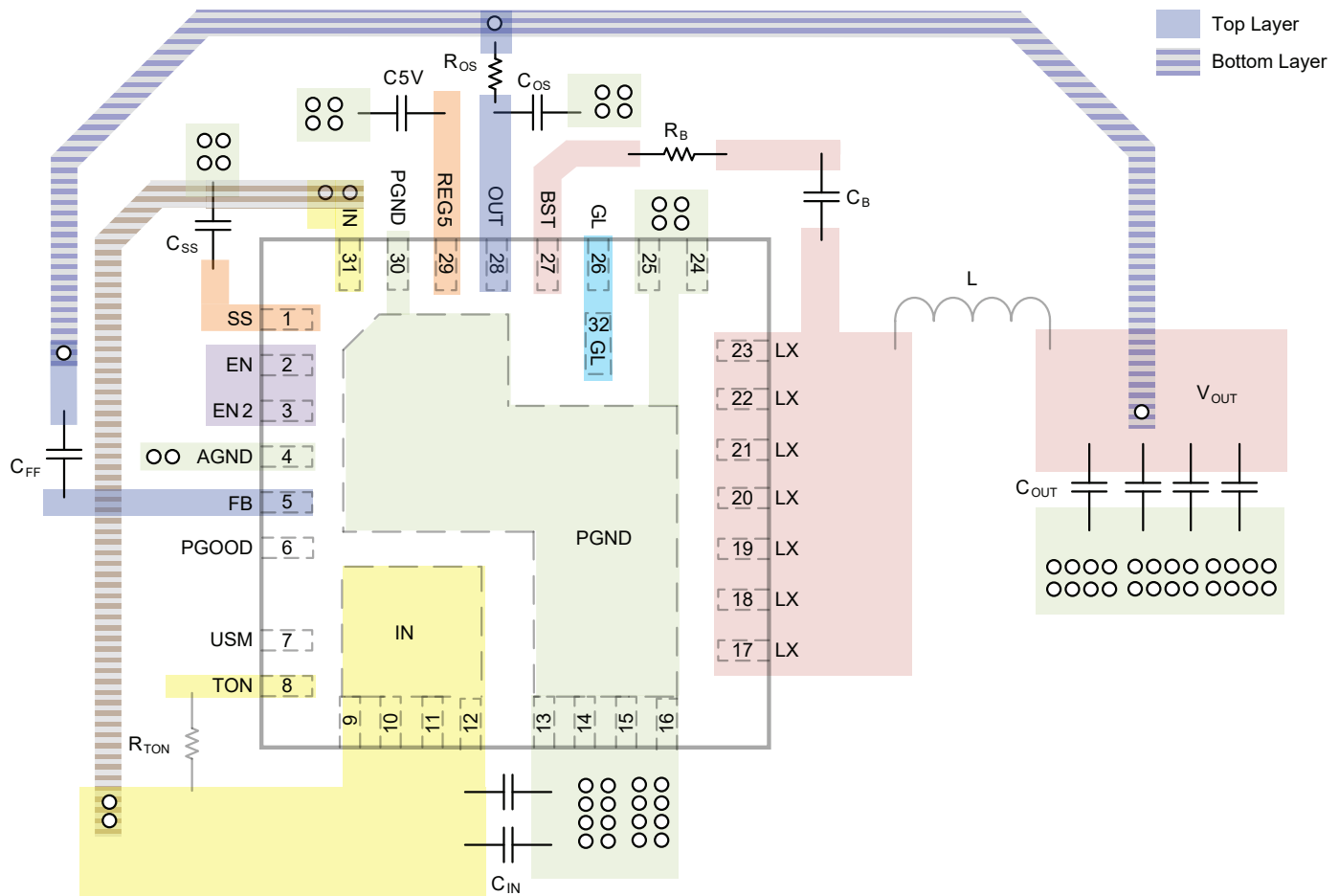
Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

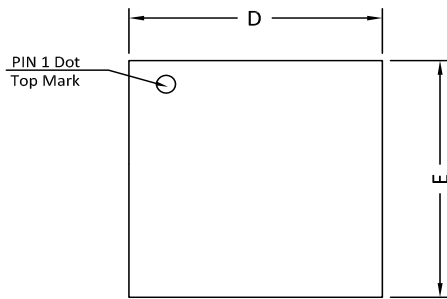
1. Several layout tips are listed below for the best electric and thermal performance.
2. Connected a small copper plane to LX pin to have lower noise interference area.
3. The IN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to IN pins to help thermal dissipation.
4. Input capacitors should be connected to the IN pin

and the PGND pin as close as possible to reduce the switching spikes.

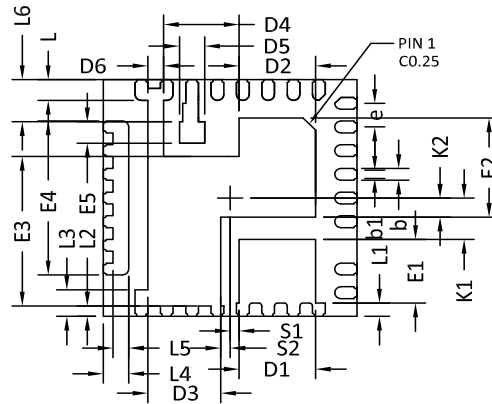
5. Decoupling capacitor C5V should be connected to V_{REG5} and AGND as close as possible.
6. A large ground plane is preferred.
7. Keep sensitive signal traces such as feedback trace far away from the LX pins.
8. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
9. Place via to connect AGND pin and ground layer, the via must be placed as close as possible to AGND pin. Place via as close as possible to PGND pins and the ground side of output capacitor, too.



Package Dimensions, QFN4x4-31L



TOP VIEW

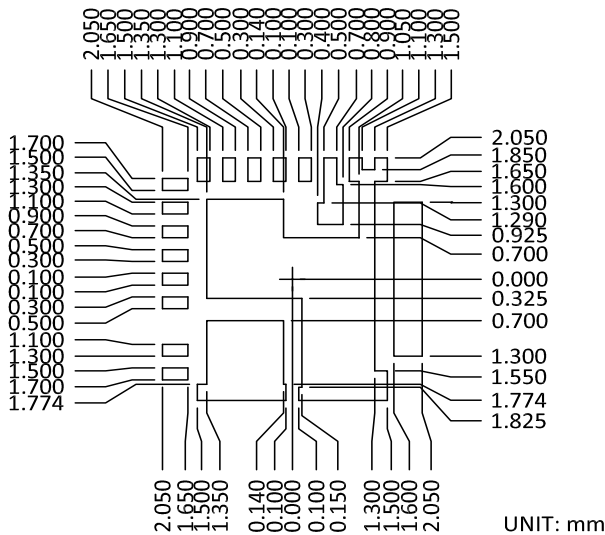


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN

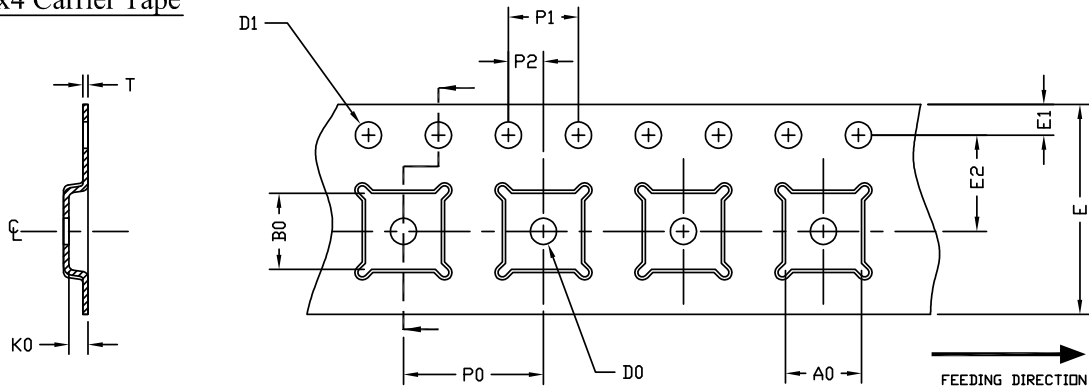


SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20REF			0.008REF		
D	3.90	4.00	4.10	0.154	0.157	0.161
E	3.90	4.00	4.10	0.154	0.157	0.161
D1	1.16	1.21	1.26	0.046	0.048	0.050
D2	1.16	1.21	1.26	0.046	0.048	0.050
D3	1.10	1.15	1.20	0.043	0.045	0.047
D4	1.14	1.19	1.24	0.045	0.047	0.049
D5	0.35	0.40	0.45	0.014	0.016	0.018
D6	0.20	0.25	0.30	0.008	0.010	0.012
E1	1.02	1.07	1.12	0.040	0.042	0.044
E2	1.63	1.68	1.73	0.064	0.066	0.068
E3	2.48	2.53	2.58	0.097	0.099	0.101
E4	2.55	2.60	2.65	0.100	0.102	0.104
E5	0.32	0.37	0.42	0.012	0.014	0.016
K1	0.65	0.70	0.75	0.026	0.028	0.030
K2	0.28	0.33	0.38	0.011	0.013	0.015
S1	0.09	0.14	0.19	0.004	0.006	0.007
S2	0.10	0.15	0.20	0.004	0.006	0.008
L	0.30	0.35	0.40	0.012	0.014	0.016
L1	0.18	0.23	0.28	0.007	0.009	0.011
L2	0.13	0.18	0.23	0.005	0.007	0.009
L3	0.40	0.45	0.50	0.016	0.018	0.020
L4	0.35	0.40	0.45	0.014	0.016	0.018
L5	0.20	0.25	0.30	0.008	0.010	0.012
L6	0.66	0.71	0.76	0.026	0.028	0.030
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.09	0.14	0.19	0.004	0.006	0.007
e	0.40BSC			0.016BSC		

NOTE:
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN4x4-31L

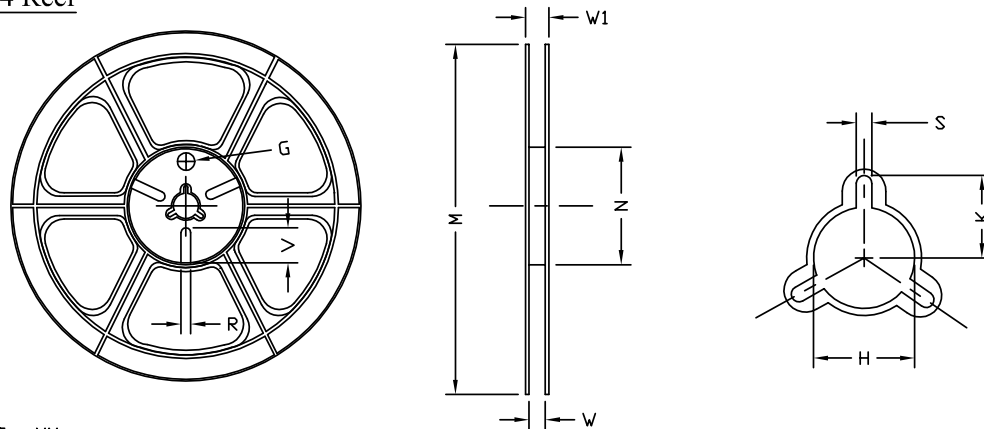
QFN4x4 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN4x4 (12 mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 ^{+0.1} _{-0.0}	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

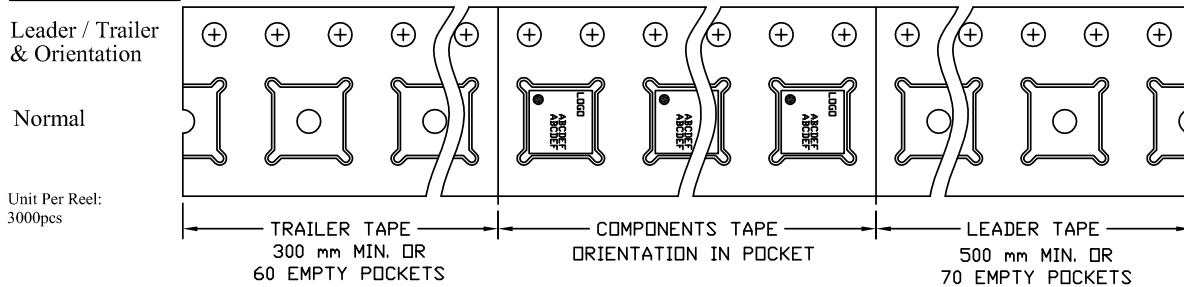
QFN4x4 Reel



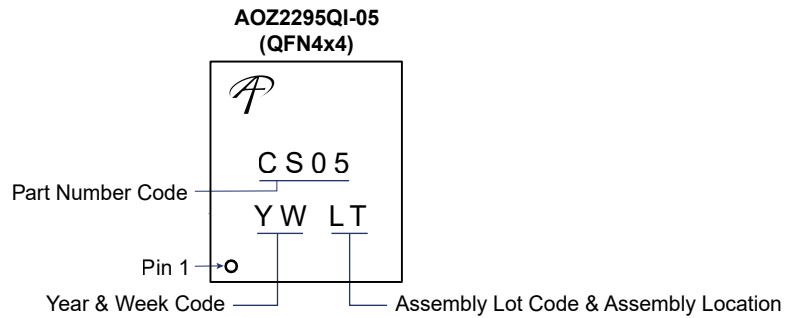
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	∅330	∅330.0 ±2.0	∅79.0 ±1.0	12.4 ^{+2.0} _{-0.0}	17.0 ^{+2.0} _{-1.2}	∅13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

QFN4x4 Tape



Part Marking



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