EQCO510

Automotive Dual Channel USB 3.2 Gen 1 Reclocker/Redriver Product Brief

Features

- Extending the reach of USB 3.2 Gen 1 (SuperSpeed) up to 15m
- Cable types supported are STP (Shielded Twisted Pair) and Coax
- Cable lengths supported
  - Up to 5m when USB 2.0 signaling included in cable
  - Up to 15m when USB 3.2 only
- *EyeOpen*™ technology automatically performs cable compensation 0 - 20 dB with 1 dB steps
- *MarginLink*™ integrated signal integrity test capability
- CDR (Clock-Data Recovery) restores signal timing integrity in both directions
- Reference Clock-free operation (no crystal or clock needed)
- Internal terminations for low external component count
- Transparent for all USB 3.2 SuperSpeed signaling including LFPS and electrical-idle
- Dual Channel Single Lane
- 20 pin 4 mm QFN package with wettable flanks
- Low power consumption / single supply @ 1.2V
- Ultra low power sleep mode when link is idle for a sustained period
- Spread Spectrum modulation applied to LFPS signal output to reduce EMI
- AEC-Q100 Grade 2 (-40°C to +105°C)

Applications

- Automotive media hub / breakout box
- Automotive head unit
- Automotive data communication module
- Automotive real time video systems

General Description

The EQCO510 is the first fully automotive qualified single chip USB 3.2 Reclocker/Redriver with *EyeOpen*™ and *MarginLink*™ technology in the automotive industry. The EQCO510 will reclock and drive a USB 3.2 SuperSpeed signal over a cable up to 15m reliably for the lifetime of a car. Furthermore, the EQCO510 extends max cable length from a recommended 1m to 5m to meet the maximum length of USB 2.0 and up to 15m for USB 3.2 links in a car. Now designers can easily modify an existing USB 2.0 media box design to also support USB 3.2 SuperSpeed without changing the physical position of the breakout box using low cost cable.

The EQCO510 is a single chip (equalizer, driver, reclocker) that repeats high speed data signals with a rate of 5 Gbps. From a cable or PCB trace pair, the signal is received by an auto-adaptive equalizer that compensates for higher-frequency gain losses in the preceding channel. A reference-less clock-data recovery (CDR) subsequently resets jitter back to meet USB 3.2 specifications for maintaining signal integrity. A cable driver launches this clean signal back onto a cable or PCB trace pair. When placed in series as a repeater, a signal can travel through several EQCO510 devices to the destination. The EQCO510 CDR restores signal timing integrity at each link along the way.

MARCH 2023

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1.0 EQCO510 PINOUT

FIGURE 1-1: EQCO510 PIN DIAGRAM (VIEWED FROM TOP)

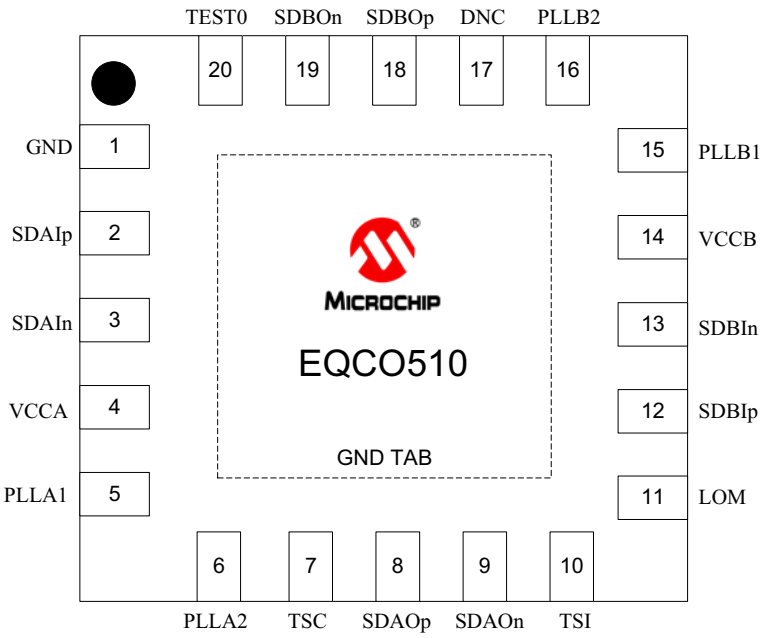


TABLE 1-1: EQCO510 PIN DESCRIPTIONS TABLE

Pin Number	Name	Type	Description
(TAB)	**GND**	Power	Connect to Ground. This pad should be connected to ground with in-pad vias.
1	**GND**	Power	Connect to GND TAB directly.
2,3	**SDAIp/SDAIn**	Differential Input	USB Cable side differential serial input pair.
4	**VCCA**	Power	Connect to +1.2V of power supply.
5	**PLLA1**	Power	Connect to +1.2V of power supply through a ferrite bead.
6	**PLLA2**	Power	Connect to PLLA1 through a capacitor.
7	**TSC**	Digital Input	Test Select Channel input. This pin selects the channel (A or B) that the TSI and LOM pins are associated with, High = Chan A, Low = Chan B.
8,9	**SDAOp/SDAOn**	Differential Output	PCB side differential serial output pair.
10	**TSI**	Analog Input	Test Signal Integrity input for channel A or channel B (selected by TSC pin). This pin has a weak internal pull down (20 kΩ) so it can be left unconnected if not used.
11	**LOM**	Digital Output	Low Margin. A low to high pulse indicates when a bit error is detected on channel A or channel B (selected by TSC pin).
12,13	**SDBIp/SDBIn**	Differential Input	PCB side differential serial input pair.
14	**VCCB**	Power	Connect to +1.2V of power supply.
15	**PLLB1**	Power	Connect to +1.2V of power supply through a ferrite bead.
16	**PLLB2**	Power	Connect to PLLB1 through a capacitor.
17	**DNC**	-	Do Not Connect. The pin must be left floating externally.
18,19	**SDBOp/SDBOn**	Differential Output	USB Cable side differential serial output pair.
20	**TEST0**	Input	Tie directly to GND.

2.0 BASIC APPLICATION INFORMATION

The EQCO510 is a USB Reclocker/Redriver intended to increase the cable distances of USB 3.2 SuperSpeed ports in automotive environments. A typical EQCO510 Link Set-up is shown in Figure 2-1 along with an internal block diagram showing pin connections in Figure 2-2.

FIGURE 2-1: TYPICAL EQCO510 LINK SET_UP

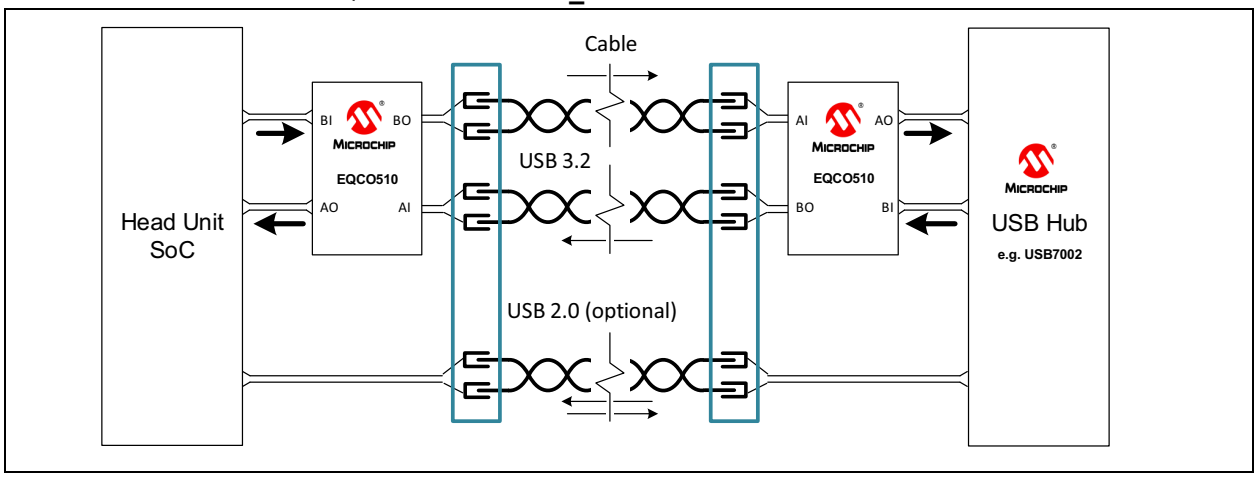
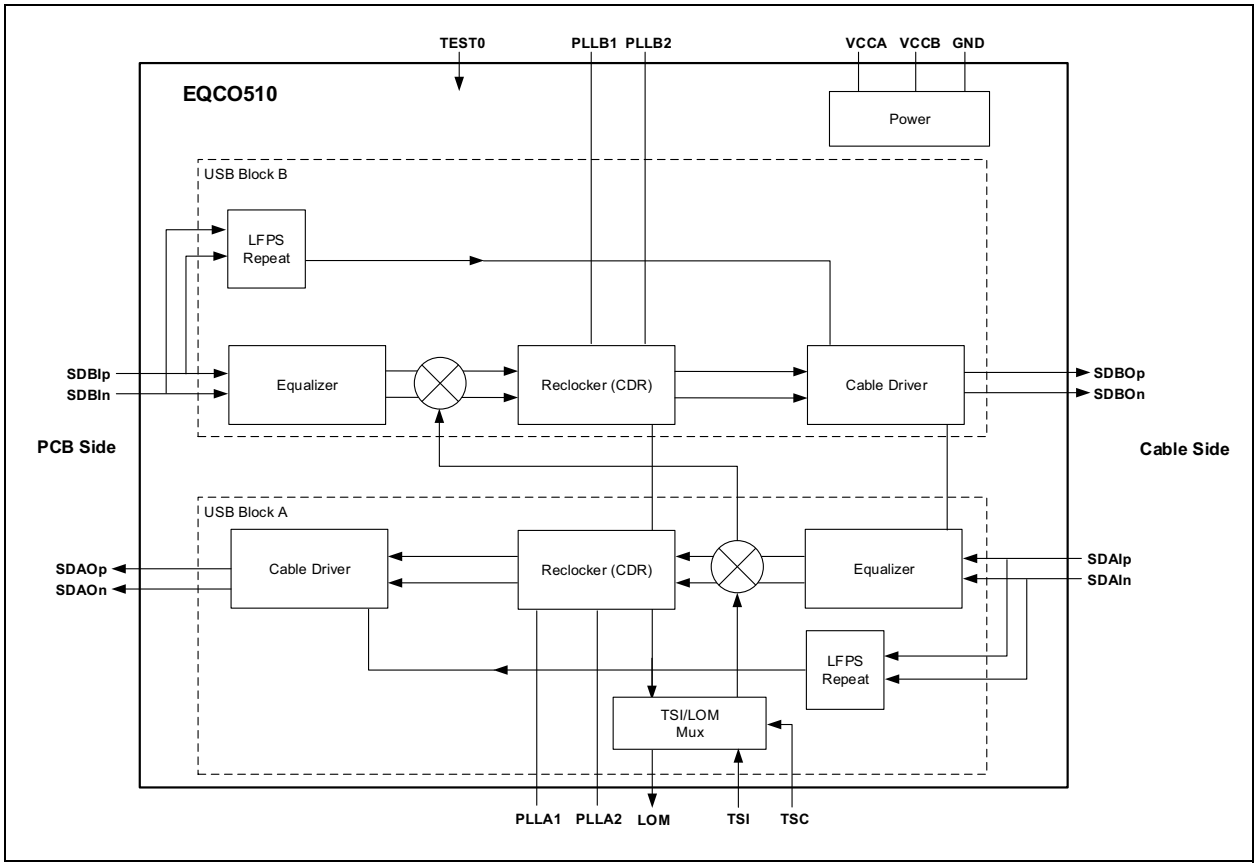


FIGURE 2-2: EQCO510 BLOCK DIAGRAM SHOWING PIN CONNECTIONS



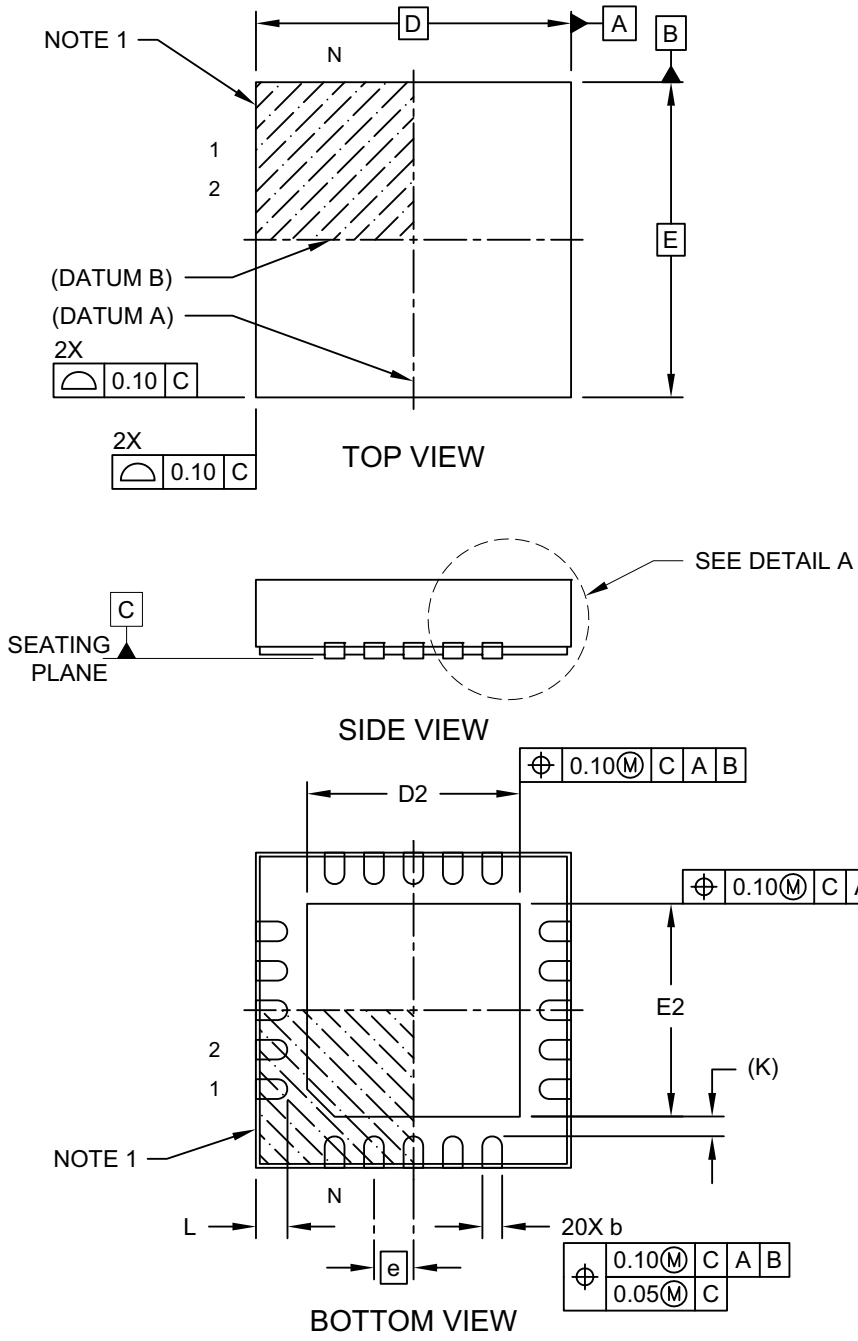
Note: The EQCO510 has two sides: the Cable side, which is typically routed to a cable connector, and the PCB side which is typically routed on a PCB to an IC. The cores in each direction are identical and each can drive cable or PCB traces.

3.0 PACKAGING INFORMATION

3.1 Package Drawings

20-Lead Plastic Quad Flat, No Lead Package (6N) - 4x4x1.0 mm Body [VQFN] Wettable Flanks (Stepped), 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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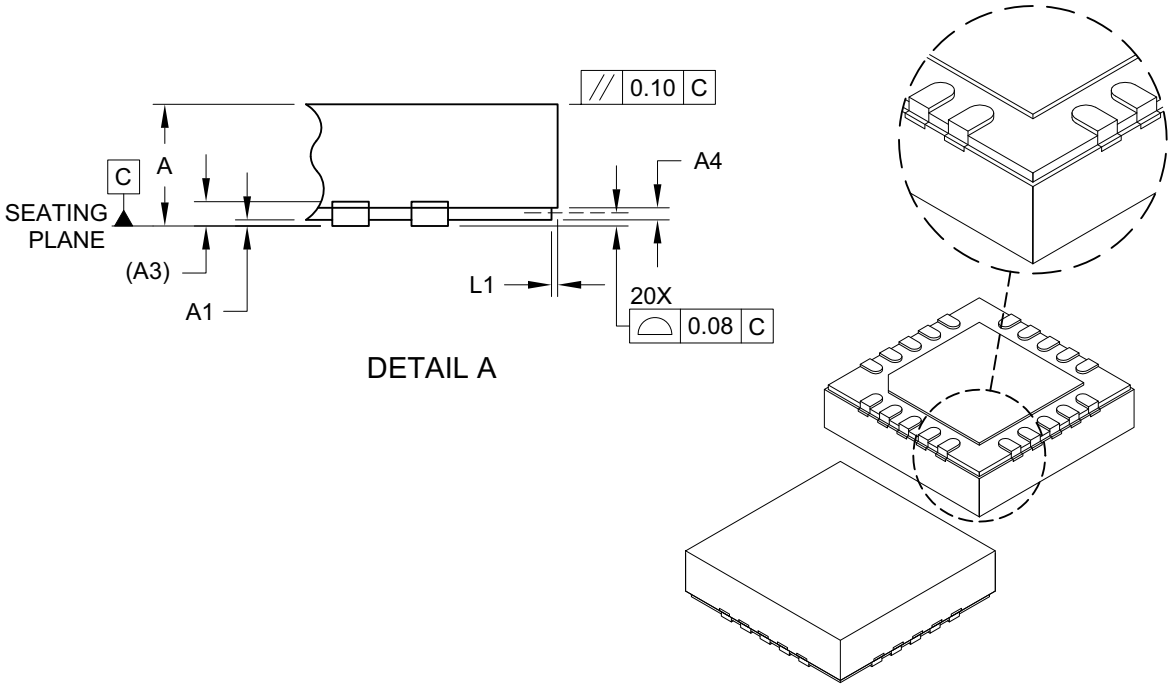

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Step Height	A4	0.05	0.12	0.19
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Step Length	L1	0.035	0.060	0.085
Terminal-to-Exposed Pad	K		0.25 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

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ISBN: 978-1-6683-2144-7

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