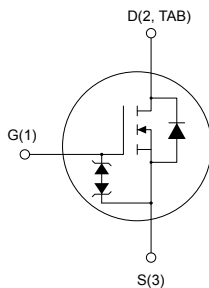
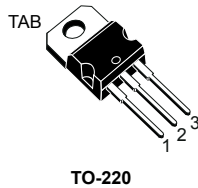


N-channel 800 V, 197 mΩ typ., 16 A MDmesh K6 Power MOSFET in a TO-220 package



AM01476v1_tab



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STP80N240K6	800 V	220 mΩ	16 A

- Worldwide best R_{DS(on)} x area
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Recommended for flyback topology, based applications such as LED lighting, chargers and adapters. Provide more power density reducing both BOM cost and size of the board.

Description

This very high voltage N-channel Power MOSFET is designed using the ultimate MDmesh K6 technology based on 20 years STMicroelectronics experience on super junction technology. The result is the best-in-class on-resistance per area and gate charge for applications requiring superior power density and high efficiency.

Product status link

[STP80N240K6](#)

Product summary

Order code	STP80N240K6
Marking	80N240K6
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	16	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	10	A
$I_{DM}^{(1)}$	Drain current (pulsed)	35	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	140	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	5	V/ns
$dv/dt^{(2)}$	Peak diode recovery current slope	100	A/μs
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 4\text{ A}$; $V_{DS}(\text{peak}) = 400\text{ V}$

3. $V_{DS} \leq 640\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.89	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	3.3	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	200	mJ

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$, $T_C = 125\text{ }^\circ\text{C}^{(1)}$			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 1	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	3.5	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 7\text{ A}$		197	220	m Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1350	-	pF
C_{oss}	Output capacitance		-	22	-	pF
$C_{o(er)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }640\text{ V}$, $V_{GS} = 0\text{ V}$	-	25	-	pF
$C_{o(tr)}^{(2)}$	Equivalent capacitance energy related		-	139	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	1.8	-	Ω
Q_g	Total gate charge	$V_{DD} = 640\text{ V}$, $I_D = 7\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 19. Test circuit for gate charge behavior)	-	25.9	-	nC
Q_{gs}	Gate-source charge		-	6.9	-	nC
Q_{gd}	Gate-drain charge		-	8.4	-	nC

1. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

2. $C_{o(tr)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 7\text{ A}$, $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$	-	16	-	ns
t_r	Rise time		-	5.3	-	ns
$t_{d(off)}$	Turn-off delay time	see (Figure 17. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	47.8	-	ns
t_f	Fall time		-	12	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		14	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		35	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 14\text{ A}, V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 14\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V}$	-	335		ns
Q_{rr}	Reverse recovery charge	(see Figure 20. Test circuit for inductive load switching and diode recovery times)	-	5.4		μC
I_{RRM}	Reverse recovery current		-	27.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 14\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V},$	-	430		ns
Q_{rr}	Reverse recovery charge	$T_J = 150\text{ }^\circ\text{C}$	-	7.4		μC
I_{RRM}	Reverse recovery current	(see Figure 20. Test circuit for inductive load switching and diode recovery times)	-	28		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

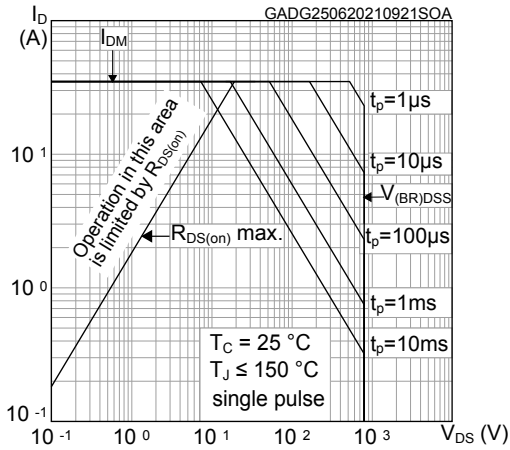


Figure 2. Maximum transient thermal impedance

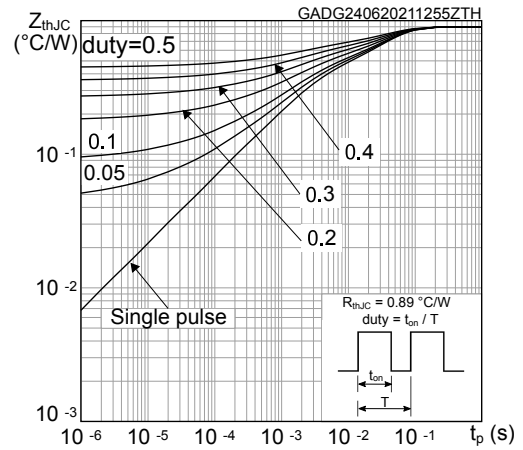


Figure 3. Typical output characteristics

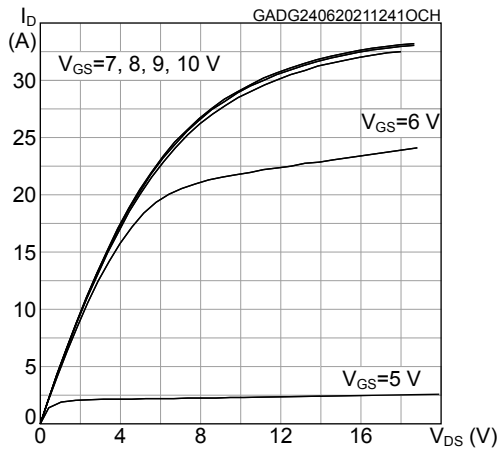


Figure 4. Typical transfer characteristics

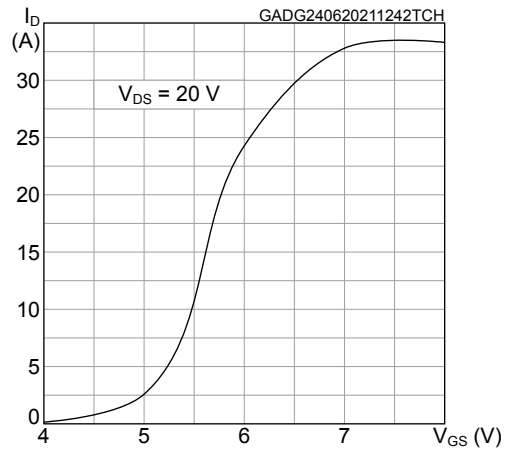


Figure 5. Typical gate charge characteristics

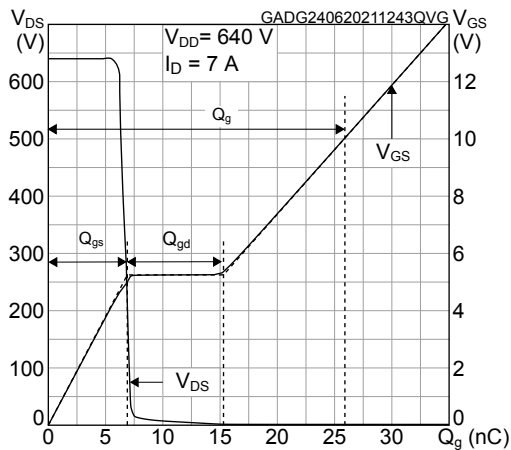


Figure 6. Typical drain-source on-resistance

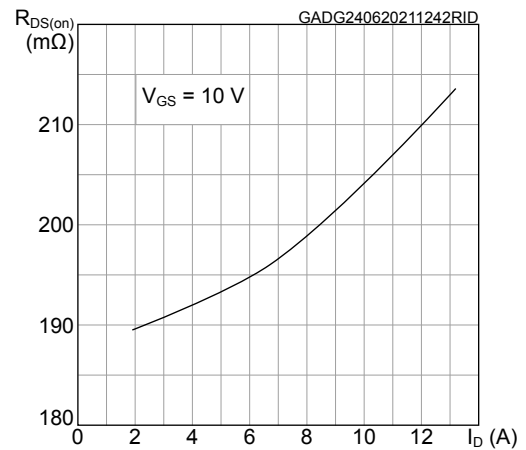


Figure 7. Typical capacitance characteristics

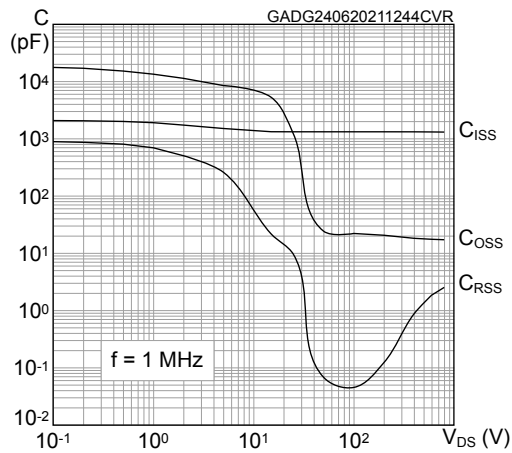


Figure 8. Typical output capacitance stored energy

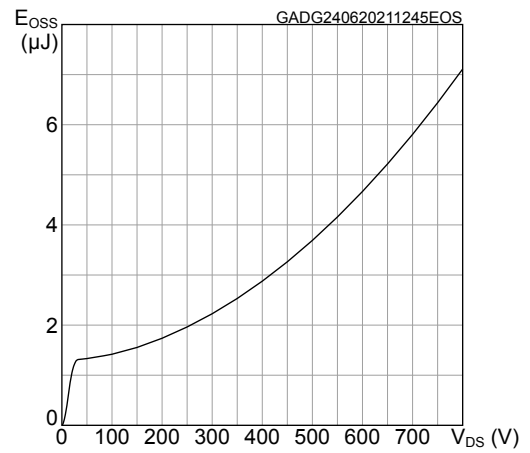


Figure 9. Normalized gate threshold vs temperature

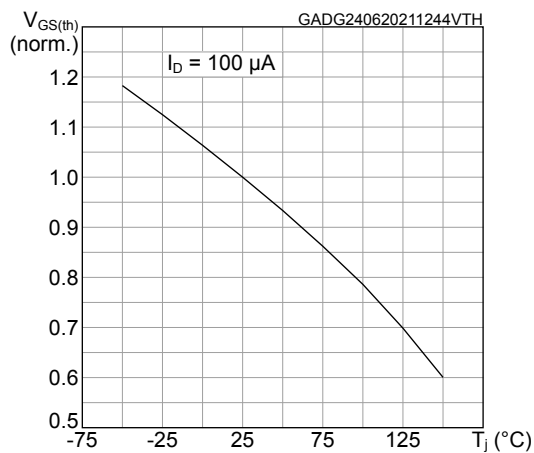


Figure 10. Normalized on-resistance vs temperature

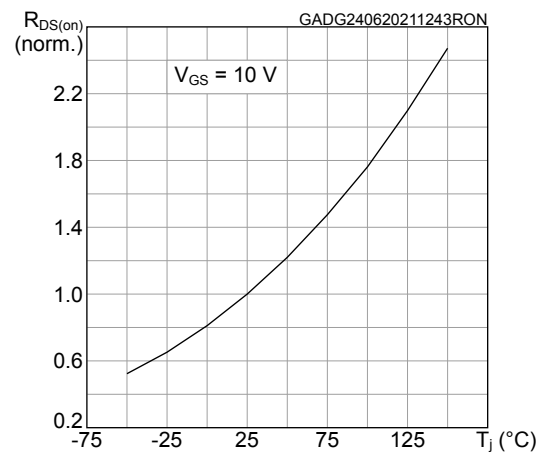


Figure 11. Normalized breakdown voltage vs temperature

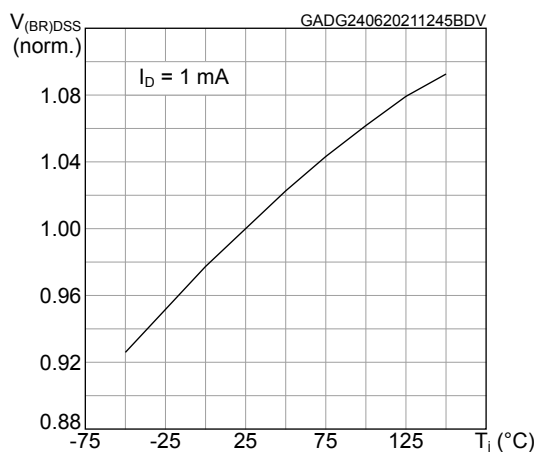


Figure 12. Typical reverse diode forward characteristics

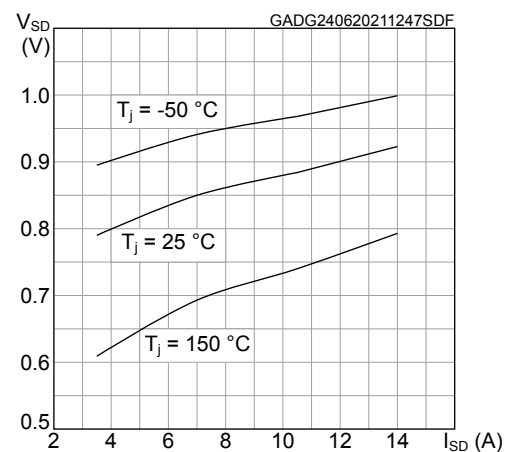


Figure 13. Maximum avalanche energy vs temperature

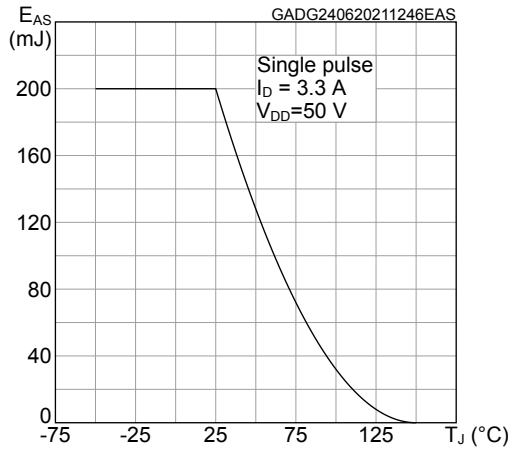


Figure 14. Typical output capacitance stored energy

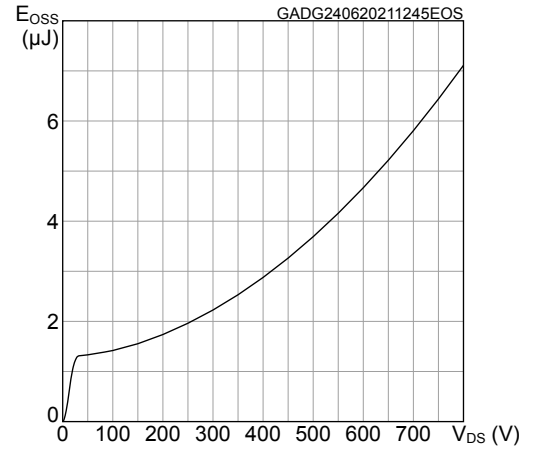


Figure 15. Inductive load: energy losses vs I_D

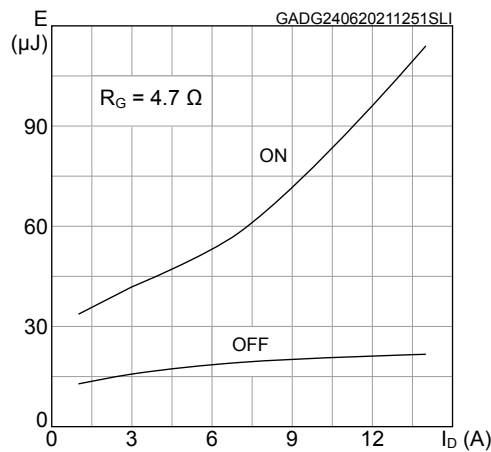
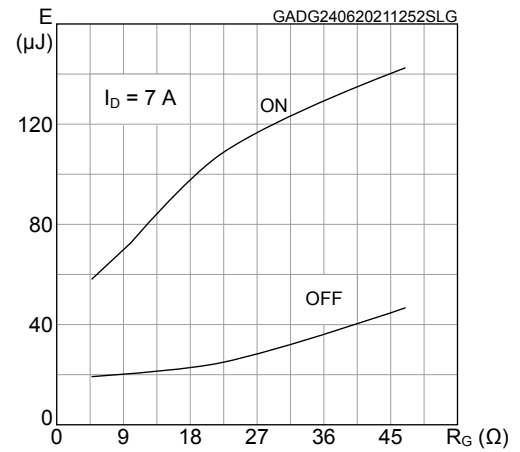
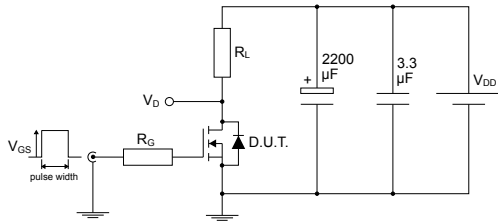


Figure 16. Inductive load: energy losses vs R_G



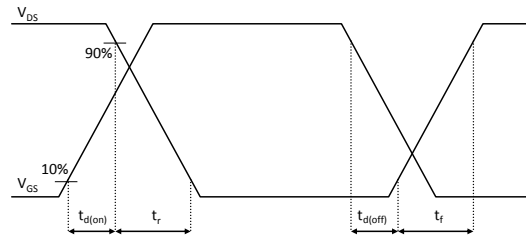
3 Test circuits

Figure 17. Test circuit for resistive load switching times



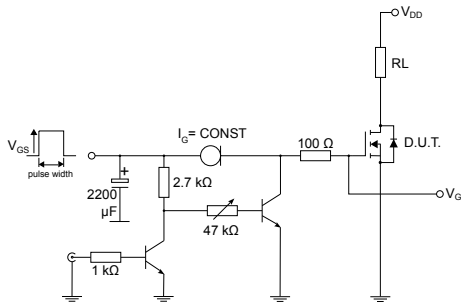
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Figure 18. Switching time waveform



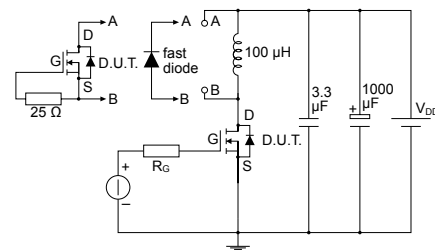
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Figure 19. Test circuit for gate charge behavior



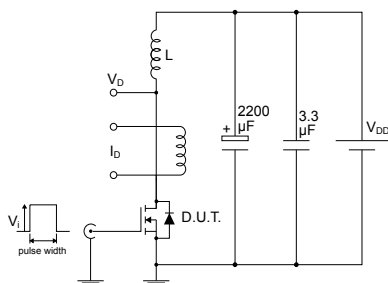
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Figure 20. Test circuit for inductive load switching and diode recovery times



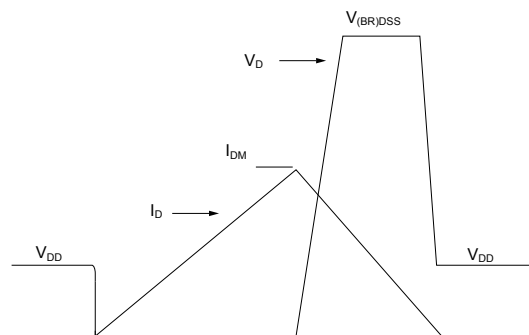
AM01470v1

Figure 21. Unclamped inductive load test circuit



AM01471v1

Figure 22. Unclamped inductive waveform



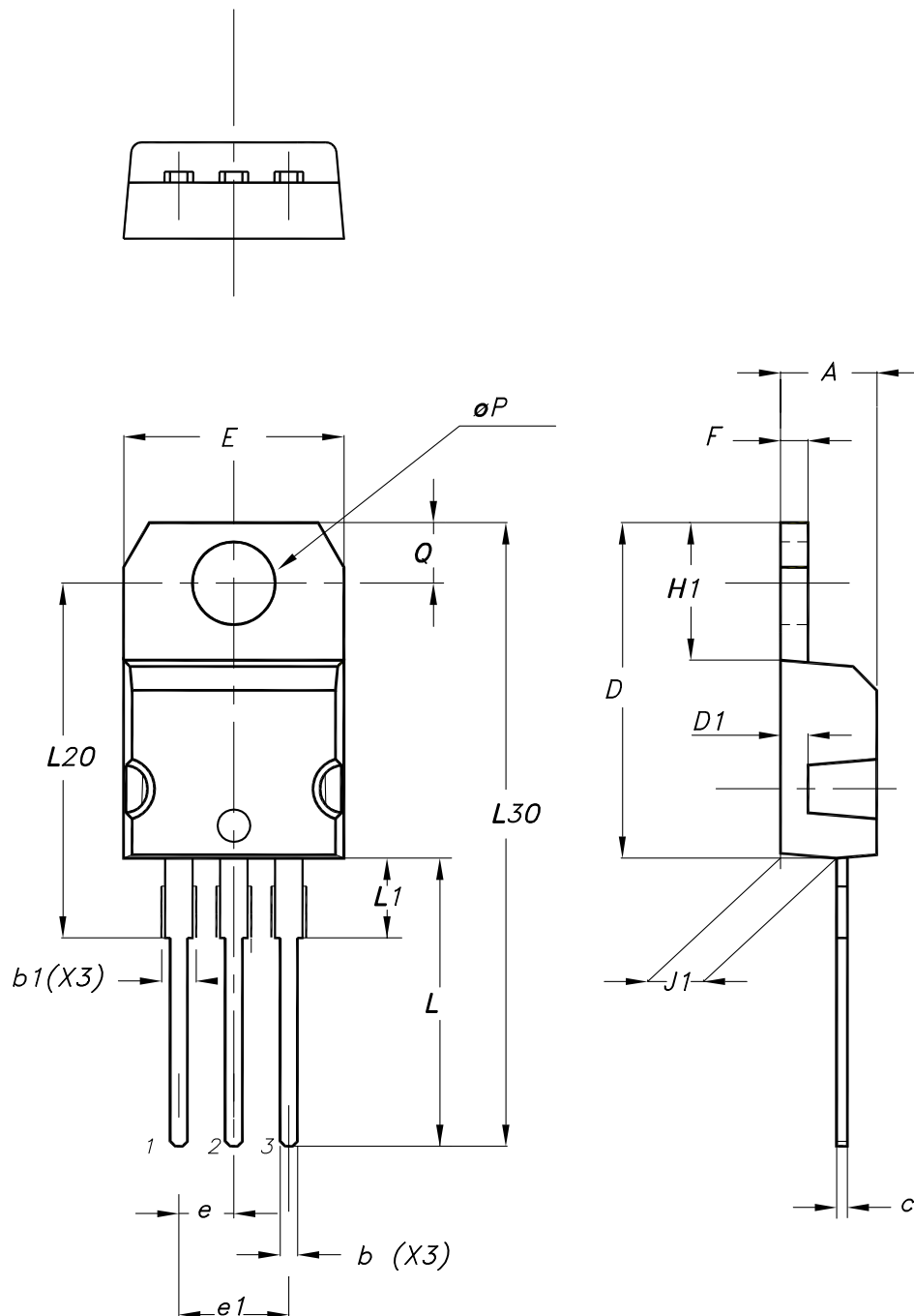
AM01472v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 23. TO-220 type A package outline



0015988_typeA_Rev_23

Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 9. Document revision history

Date	Revision	Changes
30-Jun-2021	1	Initial release.

Contents

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