

## AM243x Sitara™ Microcontrollers

### 1 Features

#### Processor cores:

- Up to 2× Dual-core Arm® Cortex®-R5F MCU subsystems operating at up to 800 MHz, highly-integrated for real-time processing
  - Dual-core Arm® Cortex®-R5F clusters support dual-core and single-core operation
  - 32KB ICache and 32KB DCache per R5F core with SECDED ECC on all memories
  - Single-core: 128KB TCM per cluster (128KB TCM per R5F core)
  - Dual-core: 128KB TCM per cluster (64KB TCM per R5F core)
- 1× Single-core Arm® Cortex®-M4F MCU subsystem at up to 400 MHz
  - 256KB SRAM with SECDED ECC

#### Memory subsystem:

- Up to 2MB of On-chip RAM (OCSRAM) with SECDED ECC:
  - Can be divided into smaller banks in increments of 256KB for as many as 8 separate memory banks
  - Each memory bank can be allocated to a single core to facilitate software task partitioning
- DDR Subsystem (DDRSS)
  - Supports LPDDR4, DDR4 memory types
  - 16-Bit data bus with inline ECC
  - Supports speeds up to 1600 MT/s

#### Industrial subsystem:

- 2× Gigabit Industrial Communication Subsystems (PRU\_ICSSG)
  - Optional support for Profinet IRT, Profinet RT, EtherNet/IP, EtherCAT, Time-Sensitive Networking (TSN), and other Networking Protocols
  - Backwards compatibility with 10/100Mb PRU\_ICSS
  - Each PRU\_ICSSG contains:
    - 3× PRU RISC Cores per Slice (2× Slice per PRU\_ICSSG)
      - PRU General Use core (PRU)
      - PRU Real-Time Unit core (PRU-RTU)
      - PRU Transmit core (PRU-TX)
    - Each PRU core supports the following features:
      - Instruction RAM with ECC
      - Broadside RAM

- Multiplier with optional accumulator (MAC)
- CRC16/32 hardware accelerator
- Byte swap for Big/Little Endian conversion
- SUM32 hardware accelerator for UDP checksum
- Task Manager for preemption support
- Up to 2× 10/100/1000 Ethernet ports
- Three Data RAMs with ECC
- 8 banks of 30 × 32-bit register scratchpad memory
- Interrupt controller and task manager
- 2× 64-bit Industrial Ethernet Peripherals (IEPs) for time stamping and other time synchronization functions
- 18× Sigma-Delta filters
  - Short circuit logic
  - Over-current logic
- 6× Multi-protocol position encoder interfaces
- One Enhanced Capture Module (ECAP)
- 16550-compatible UART with a
  - Dedicated 192-MHz clock to support 12-Mbps PROFIBUS

#### System on Chip (SoC) Services:

- Device Management Security Controller (DMSC-L)
  - Centralized SoC system controller
  - Manages system services including initial boot, security, and clock/reset/power management
  - Communication with various processing units over message manager
  - Simplified interface for optimizing unused peripherals
  - On-Chip Debug functionality through JTAG and Trace interfaces)
- Data Movement Subsystem (DMSS)
  - Block Copy DMA (BCDMA)
  - Packet DMA (PKTDMA)
  - Secure Proxy (SEC\_PROXY)
  - Ring Accelerator (RINGACC)
- Time Sync Subsystem
  - Central Platform Time Sync (CPTS) module
  - Timer Manager (TIMERMANAGER) with 1024 timers
  - Time Sync and Compare event interrupt routers

#### Security:

- Secure Boot supported
  - Hardware-enforced Root-of-Trust (RoT)
  - Support to switch RoT via backup key



- Support for takeover protection, IP protection, and anti-roll back protection
- Support for cryptographic acceleration
  - Session-aware cryptographic engine with ability to auto-switch key-material based on incoming data stream
  - Supports cryptographic cores
    - AES – 128/192/256 Bits key sizes
    - 3DES – 56/112/168 Bits key sizes
    - MD5, SHA1
    - SHA2 – 224/256/384/512
    - DRBG with true random number generator
    - PKA (Public Key Accelerator) to Assist in RSA/ECC processing
  - DMA support
- Debugging security
  - Secure software controlled debug access
  - Security aware debugging
- Trusted Execution Environment (TEE) supported
  - Arm TrustZone® based TEE
  - Extensive firewall support for isolation
  - Secure DMA Path and Interconnect
  - Secure watchdog/timer/IPC
- Secure storage support
- On-the-Fly encryption (OTFE) support for OSPI interface in XIP mode
- Networking security support for data (Payload) encryption/authentication via packet based hardware cryptographic engine
- Security co-processor (DMSC-L) for key and security management, with dedicated device level interconnect for security

#### High-speed serial interfaces:

- 1× Integrated Ethernet switch supporting up to 2 external ports (CPSW3G)
  - Up to 2 RGMII (10/100/1000)
  - IEEE 1588 (2008 Annex D, Annex E, Annex F) with 802.1AS PTP
  - Clause 45 MDIO PHY management
  - Energy efficient Ethernet (802.3az)
- 1× PCI-Express® Gen2 controller (PCIE)
  - Supports Gen2 operation
  - Supports Single Lane operation
- 1× USB 3.1-Gen1 Dual-role Device (DRD) Subsystem (USBSS)
  - One shared USBSS port for enhanced SuperSpeed Gen1 or USB 2.0
  - Port configurable as USB host, USB peripheral, or USB Dual-role Device
  - Integrated USB VBUS detection
- 1× Serializer/Deserializer (SERDES)
  - One SERDES lane to support PCI-Express® Gen2 and USB SuperSpeed Gen1

#### General connectivity peripherals:

- 6× Inter-Integrated Circuit (I2C) ports
- 9× configurable Universal Asynchronous Receive/Transmit (UART) modules
- 1× 12-bit Analog-to-Digital Converters (ADC)
  - Up to 4 MSPS
  - 8× multiplexed analog inputs
- 7× Multichannel Serial Peripheral Interfaces (MCSPI) controllers
- 3× General-Purpose I/O (GPIO) modules

#### Industrial and control interfaces:

- 9× Enhanced Pulse-Width Modulator (EPWM) modules
- 3× Enhanced Capture (ECAP) modules
- 3× Enhanced Quadrature Encoder Pulse (EQEP) modules
- 2× Modular Controller Area Network (MCAN) modules with full CAN-FD support
- 2× Fast Serial Interface Transmitter (FSI\_TX) cores
- 6× Fast Serial Interface Receiver (FSI\_RX) cores

#### Memory controllers:

- 2× MultiMedia Card/Secure Digital (MMC/SD) interfaces
  - One 4-bit for SD/SDIO
  - One 8-bit for eMMC
  - Integrated analog switch for voltage switching between 3.3V to 1.8V for high-speed cards
- 1× General-Purpose Memory Controller (GPMC)
  - 16-bit parallel bus with 133 MHz clock or
  - 32-bit parallel bus with 100 MHz clock
  - Error Location Module (ELM) support
- 1× Flash Subsystem (FSS) that can be configured as Octal SPI (OSPI) flash interfaces or one Quad SPI (QSPI)

#### Power Management:

- Simplified power sequence
- Dual-voltage I/O Support
- Integrated SDIO LDO for handling automatic voltage transition for SD interface
- Integrated voltage supervisor for safety monitoring of over-under voltage conditions
- Integrated power supply glitch detector for detecting fast supply transients

### Functional Safety:

- **Functional Safety-Compliant** Targeted
  - Developed for functional safety applications
  - Documentation will be available to aid IEC 61508 functional safety system design
  - Systematic capability up to SIL 3
  - Hardware integrity up to SIL 2 targeted for MCU domain
  - Quality-managed MAIN Domain
  - Safety-related certification
    - IEC 61508 certification planned
  - ECC or parity on calculation-critical memories
  - ECC and parity on select internal bus interconnects
  - Built-In Self-Test (BIST) for CPU and on-chip RAM
  - Error Signaling Module (ESM) with external error pin
  - Run-time safety diagnostics, including:
    - Voltage, Temperature, and Clock Monitoring
    - Windowed Watchdog Timers
    - CRC Engine for memory integrity checks
  - MCU Domain with dedicated memory, interfaces, and M4FSS capable of being isolated from the larger SoC with Freedom From Interference (FFI) features
    - Separate interconnect
    - Firewalls and timeout gaskets
    - Dedicated PLL
    - Dedicated I/O supply
    - Separate reset

### SoC Architecture:

- Supports primary boot from UART, I2C, OSPI/QSPI Flash, SPI Flash, parallel NOR Flash, parallel NAND Flash, SD, eMMC, USB 2.0, PCIe, and Ethernet interfaces
- 16-nm FinFET technology

### Package options:

- ALV FCBGA (441-pin) (Lidded) Flip-Chip Ball Grid Array package, 17.2 mm × 17.2 mm, 0.8-mm pitch
- ALX FC/CSP (293-pin) (SiP) Flip-Chip Chip Scale Package package, 11 mm × 11 mm, 0.5-mm pitch

## 2 Applications

- [Programmable Logic Controller \(PLC\)](#)
- [Motor Drives](#)
- [Remote I/O](#)
- [Industrial Robots](#)

## 3 Description

AM243x is an extension of Sitara's industrial-grade portfolio into high-performance microcontrollers. The AM243x device is built for industrial applications, such as motor drives and remote I/O modules, which require a combination of real-time communications and processing. The AM243x family provides scalable performance with up to four Cortex-R5F MCUs and one Cortex-M4F.

The AM243x SoC architecture was designed to provide best-in-class real-time performance through the high-performance Arm Cortex-R5F cores, Tightly-Coupled Memory banks, configurable SRAM partitioning, and dedicated low-latency paths to and from peripherals for rapid data movement in and out of the SoC. This deterministic architecture allows for AM243x to handle the tight control loops found in servo drives while the peripherals like FSI, GPMC, PWMs, sigma delta decimation filters, and absolute encoder interfaces help enable a number of different architectures found in these systems.

The PRU-ICSSG in AM243x provides the flexible industrial communications capability necessary to run gigabit TSN, EtherCAT, PROFINET, EtherNet/IP, and various other protocols. In addition, the PRU-ICSSG also enables additional interfaces in the SoC including sigma delta decimation filters and absolute encoder interfaces.

Functional safety features can be enabled through the integrated Cortex-M4F along with its dedicated peripherals which can all be isolated from the rest of the SoC. AM243x also supports secure boot.

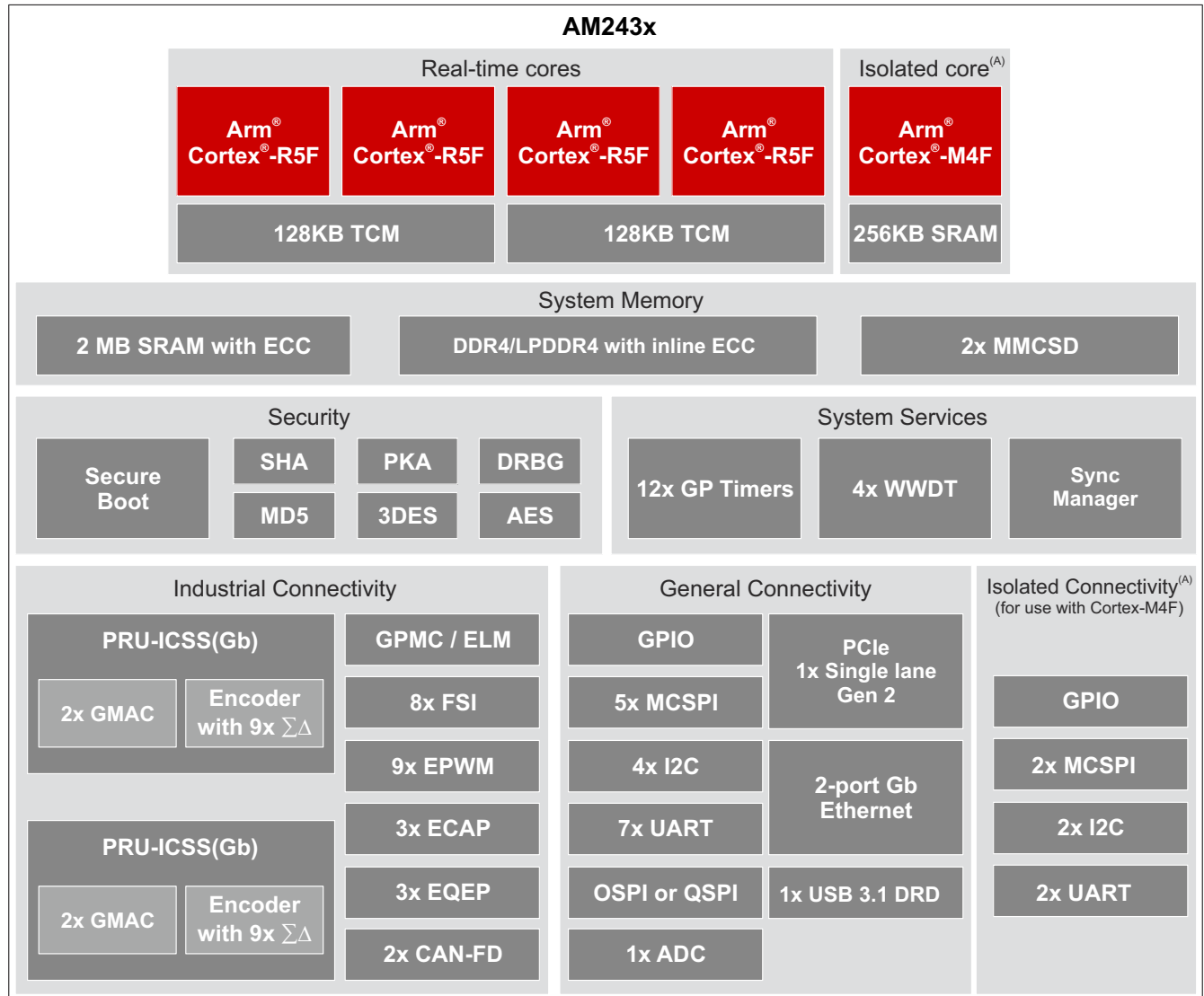
### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE
AM2434...ALV	FCBGA (441) [Lidded]	17.2 mm × 17.2 mm
AM2434...ALX	FC/CSP (293) [SiP]	11 mm × 11 mm
AM2432...ALV	FCBGA (441) [Lidded]	17.2 mm × 17.2 mm
AM2432...ALX	FC/CSP (293) [SiP]	11 mm × 11 mm
AM2431..ALV	FCBGA (441) [Lidded]	17.2 mm × 17.2 mm
AM2431..ALX	FC/CSP (293) [SiP]	11 mm × 11 mm

(1) For more information, see [Section 11, Mechanical, Packaging, and Orderable Information](#).

### 3.1 Functional Block Diagram

Figure 3-1 is the functional block diagram for the device.



- A. Isolation of peripherals and M4F core is an optional feature. MCU domain resources are shared across SoC when in non-isolated configuration.
- B. USB3.1 and PCIe share a common SerDes lane.

**Figure 3-1. Functional Block Diagram**

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## 4 Revision History

### Changes from April 26, 2021 to June 30, 2021 (from Revision \* (April 2021) to Revision A (June 2021))

	Page
• (Description) Updated paragraph describing industrial communications capability.....	4
• (Functional Block Diagram): Updated I2C count under General Connectivity block.....	5
• (eMMCPHY Electrical Characteristics): Updated electrical parameters associated with eMMCPHY IOs.....	187
• (Recommended Operating Conditions for OTP eFuse Programming): Applied the "See Recommended Operating Conditions" reference to MIN, NOM, and MAX columns of the VDD_CORE parameter.....	192
• (Input Clocks / Oscillators): Updated input clock descriptions.....	203
• (Input Clocks Interface): Updated/Changed the image; correcting signal naming.....	203
• (Output Clocks): Updated output clock descriptions.....	208

## 5 Device Comparison

Table 5-1 shows a comparison between devices, highlighting the differences.

**Table 5-1. Device Comparison**

FEATURES <sup>(1)</sup>	REFERENCE NAME	AM2434 (ALV)	AM2432 (ALV)	AM2431 (ALV)	AM2434 (ALX)	AM2432 (ALX)	AM2431 (ALX)
<b>JTAG DEVICE ID Comparison (Features)</b>							
CTRLMMR_JTAG_DEVICE_ID[31:13] DEVICE_ID register bit-field value <sup>(2)</sup>	C: -----	C: 0x19023	C: 0x19003	C: -----	C: 0x19023	C: 0x19003	C: 0x19003
	D: 0x19064	D: 0x19024	D: 0x19004	D: 0x19064	D: 0x19024	D: 0x19004	D: 0x19004
	E: 0x19065	E: 0x19025	E: -----	E: 0x19065	E: 0x19025	E: -----	E: -----
	F: 0x19066	F: 0x19026	F: -----	F: 0x19066	F: 0x19026	F: -----	F: -----
<b>PROCESSORS AND ACCELERATORS</b>							
Speed Grades		See Table 7-2					
Arm Cortex-R5F Processor	R5FSS	2 × Dual Core Cluster	2 × Single Core Cluster	1 × Single Core Cluster	2 × Dual Core Cluster	2 × Single Core Cluster	1 × Single Core Cluster
Arm Cortex-M4F Processor	M4FSS	1 × Single Core			1 × Single Core		
Device Management Security Controller	DMSC-L	Yes			Yes		
Crypto Accelerators	Security	Yes			Yes		
Functional Safety-capable MCU Domain with M4FSS	Safety	Yes			No		
<b>PROGRAM AND DATA STORAGE</b>							
Shared On-Chip Memory (OCSRAM) in MAIN Domain	OCSRAM	2MB			2MB		
R5F Tightly Coupled Memory (TCM) <sup>(3)</sup>	TCM	256KB	256KB	128KB	256KB	256KB	128KB
Shared On-Chip Memory (OCSRAM) in MCU Domain	MCU_MSRAM	256KB			256KB		
DDR4/LPDDR4 DDR Subsystem	DDRSS	Up to 2GB (16-bit data) with inline ECC			-		
General-Purpose Memory Controller w/Error Location Module (ELM)	GPMC w/ELM	Up to 1GB with ECC			-		
<b>PERIPHERALS</b>							
Modular Controller Area Network Interface	MCAN	2			2		
Full CAN-FD Support	MCAN	Optional			Optional		
General-Purpose I/O	GPIO	Up to 198			Up to 148		
Inter-Integrated Circuit Interface	I2C	6 (2 in MCU Domain)			3 (MAIN Domain Only)		
Analog-to-Digital Converter	ADC	1			1		
Multichannel Serial Peripheral Interface	MCSPI	7 (2 in MCU Domain)			4 (MAIN Domain Only)		
MultiMedia Card/ Secure Digital Interface	MMC0	eMMC (8-bits)			-		
	MMC1	SD/SDIO (4-bits)			SD/SDIO (4-bits)		
Fast Serial Interface	FSI_TX	2			1		
	FSI_RX	6			4		
Flash Subsystem (FSS)	OSPI/QSPI	Yes <sup>(4)</sup>			QSPI-Mode Only		
PCI Express Port with Integrated PHY	PCIE	Single Lane			-		
Programmable Real-Time Unit Subsystem (PRU Cores, eGPIO, UART, ECAP, EPWM)	PRU_ICSSG	2			2		



**Table 5-1. Device Comparison (continued)**

FEATURES <sup>(1)</sup>	REFERENCE NAME	AM2434 (ALV)	AM2432 (ALV)	AM2431 (ALV)	AM2434 (ALX)	AM2432 (ALX)	AM2431 (ALX)
Industrial Communication Subsystem Support (RGMII/MII and additional Networking Interfaces)	PRU_ICSSG	Optional			Optional		
Gigabit Ethernet Interface	CPSW3G	Yes (2 External Ports)			Yes (2 External Ports)		
General-Purpose Timers	TIMER	16 (4 in MCU Domain)			16 (4 in MCU Domain)		
Enhanced Pulse-Width Modulation Module	EPWM	9			7 <sup>(5)</sup>		
Enhanced Capture Module	ECAP	3			3		
Enhanced Quadrature Encoder Pulse Module	EQEP	3			3		
Universal Asynchronous Receiver/Transmitter	UART	9 (2 in MCU Domain)			8 (1 in MCU Domain)		
Universal Serial Bus (USB3.1 Gen1) SuperSpeed Dual-Role-Device (DRD) Port with SS PHY	USB	Yes			No USB SuperSpeed Support (USB2 Only)		

- (1) Features noted as “not supported” or “-”, must not be used. Their functionality is not supported by TI for this family of devices. These features are subject to removal without notice on future device revisions. Any information regarding the unsupported features has been retained in the documentation solely for the purpose of clarifying signal names or for consistency with previous feature descriptions.
- (2) For more details about the CTRLMMR\_JTAG\_DEVICE\_ID register and DEVICE\_ID bit field, see the device's associated *Technical Reference Manual*.
- (3) The R5F cores share Tightly Coupled Memory within a cluster and can be allocated per system requirements.
- (4) One simultaneous flash interface configured as OSPI0 or QSPI0.
- (5) Only the A output signal is available for the EHRPWM5 instance of the ALX package type.

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## 5.1 Related Products

**Sitara™ processors** Broad family of scalable processors based on Arm® Cortex® cores with flexible accelerators, peripherals, connectivity and unified software support – perfect for sensors to servers. Sitara processors have the reliability needed for use in industrial applications.

**AM243x Sitara™ microcontrollers** AM243x microcontrollers enable gigabit industrial Ethernet networks, robust operation with extensive ECC on memories, and enhanced security features.

**Sitara™ processors - Applications** Sitara™ processors provide scalable solutions for a wide range of applications from HMI and gateways to more complex equipment such as drives and substation automation equipment. Sitara processors also offer multi-protocol support for industrial communication protocols such as EtherCAT®, Ethernet/IP, and Profinet.

**Sitara™ processors - Reference designs** TI provides many reference designs containing 'building block' solutions to enable customers to rapidly develop their own unique products and solutions.

**Companion Products for AM243x** Review products that are frequently purchased or used in conjunction with this product to complete your design.

## 6 Terminal Configuration and Functions

### 6.1 Pin Diagram

#### Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

The diagrams in this section are used in conjunction with the other Terminal Configuration and Functions tables to locate signal names and ball grid numbers.

#### 6.1.1 AM243x ALV Pin Diagram

ALV FCBGA-N441 Pin Diagram shows the ball locations for the lidded 441-ball flip chip ball grid array (FCBGA) package.

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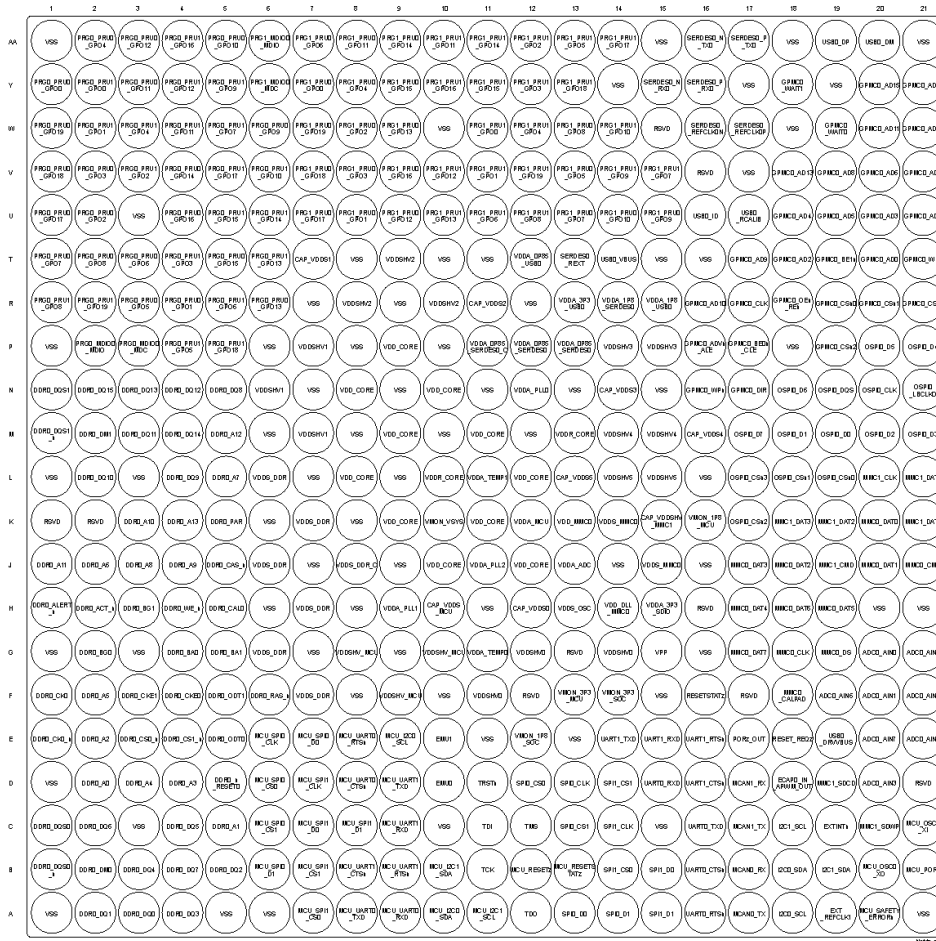


Figure 6-1. ALV FCBGA-N441 Pin Diagram (Bottom View)

### 6.1.2 AM243x ALX Pin Diagram

ALX FCBGA-N293 Pin Diagram shows the ball locations for the non-lidded 293-ball flip chip ball grid array (FCBGA) package.

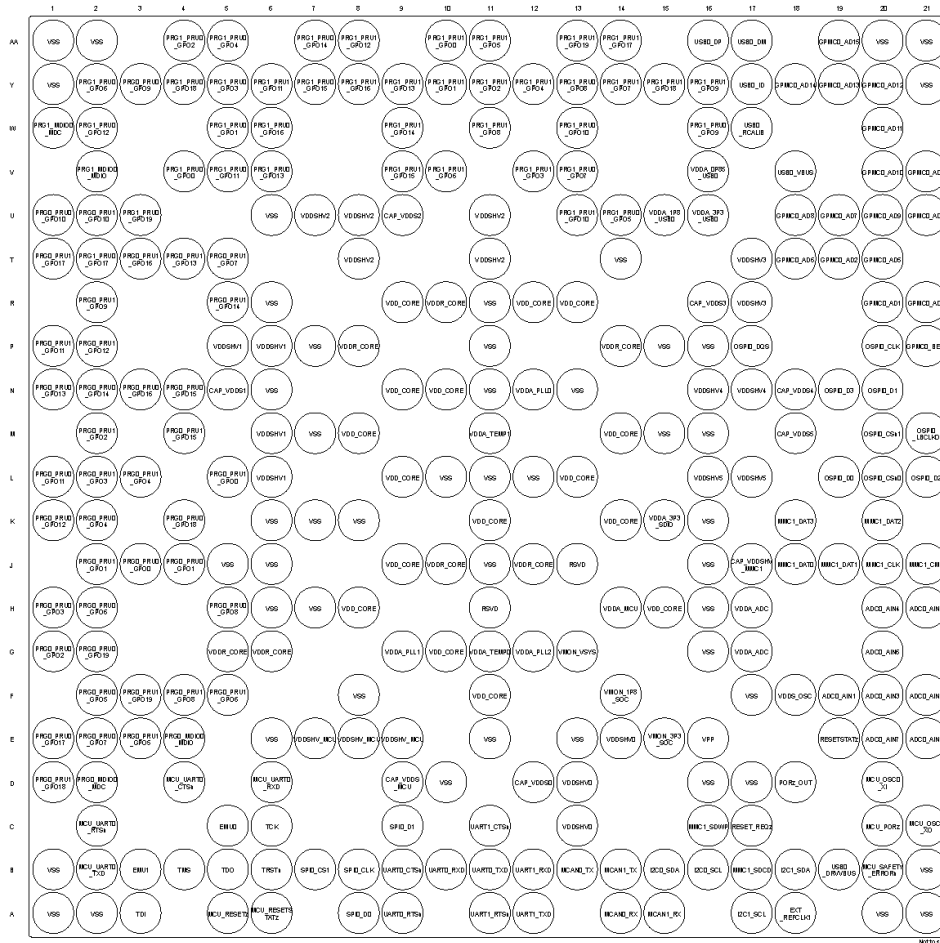


Figure 6-2. ALX FCBGA-N293 Pin Diagram (Bottom View)

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## 6.2 Pin Attributes (ALV Package)

The following list describes the contents of each column in the *Pin Attributes* table:

1. **BALL NUMBER:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **BALL NAME:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **SIGNAL NAME:** Signal name(s) of all dedicated and pin multiplexed signal functions associated with a ball.

---

### Note

The *Pin Attributes* table, defines the pin multiplexed signal functions implemented at the pin and does not define secondary multiplexing of signal functions implemented in device subsystems. Secondary multiplexing of signal functions are not described in this table. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

---

4. **MUX MODE:** The MUXMODE value associated with each pin multiplexed signal function:
  - a. MUXMODE 0 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.

---

### Note

The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when MCU\_PORz is deasserted.

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- b. MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only valid values of MUXMODE should be used.
  - c. Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz\_OUT. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
  - d. An empty box or "-" means Not Applicable.
5. **TYPE:** Signal type and direction:
  - I = Input
  - O = Output
  - IO = Input, Output, or simultaneously Input and Output
  - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
  - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
  - OZ = Output with three-state output function
  - A = Analog
  - PWR = Power
  - GND = Ground
  - CAP = LDO Capacitor.

6. **DSIS:** The deselected input state (DSIS) indicates the state driven to the subsystem input (logic "0", logic "1", or "pad" level) when the pin multiplexed signal function is not selected by MUXMODE.
  - 0: Logic 0 driven to the subsystem input.
  - 1: Logic 1 driven to the subsystem input.
  - pad: Logic state of the pad is driven to the subsystem input.
  - An empty box or "-" means Not Applicable.
7. **BALL STATE DURING RESET (RX/TX/PULL):** State of the terminal while MCU\_PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
  - RX (Input buffer)
    - Off: The input buffer is disabled.
    - On: The input buffer is enabled.
  - TX (Output buffer)
    - Off: The output buffer is disabled.
    - Low: The output buffer is enabled and drives  $V_{OL}$ .
  - PULL (Internal pull resistors)
    - Off: Internal pull resistors are turned off.
    - Up: Internal pull-up resistor is turned on.
    - Down: Internal pull-down resistor is turned on.
  - An empty box or "-" means Not Applicable.
8. **BALL STATE AFTER RESET (RX/TX/PULL):** State of the terminal after MCU\_PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
  - RX (Input buffer)
    - Off: The input buffer is disabled.
    - On: The input buffer is enabled.
  - TX (Output buffer)
    - Off: The output buffer is disabled.
    - SS: The subsystem selected with MUXMODE determines the output buffer state.
  - PULL (Internal pull resistors)
    - Off: Internal pull resistors are turned off.
    - Up: Internal pull-up resistor is turned on.
    - Down: Internal pull-down resistor is turned on.
  - An empty box or "-" means Not Applicable.
9. **MUX MODE AFTER RESET:** The value found in this column defines the default pin multiplexed signal function after MCU\_PORz is deasserted. An empty box means Not Applicable.
10. **I/O VOLTAGE VALUE:** This column describes I/O operating voltage options of the respective power supply, when applicable. An empty box or "-" means Not Applicable.

For more information, see valid operating voltage range(s) defined for each power supply in *Recommended Operating Conditions*.
11. **POWER:** The power supply of the associated I/O, when applicable.

An empty box or "-" means Not Applicable.

12. **HYS:** Indicates if the input buffer associated with this I/O has hysteresis:
- Yes: With hysteresis
  - No: Without hysteresis
  - An empty box or "-" means Not Applicable.

For more information, see the hysteresis values in *Electrical Characteristics*.

13. **BUFFER TYPE:** This column defines the buffer type associated with a terminal. This information can be used to determine which Electrical Characteristics table is applicable.

An empty box or "-" means Not Applicable.

For electrical characteristics, refer to the appropriate buffer type table in *Electrical Characteristics*.

14. **PULL UP/DOWN TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
- PU: Internal pull-up
  - PD: Internal pull-down
  - PU/PD: Internal pull-up and pull-down
  - An empty box or "-" means No internal pull.

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**Note**

Configuring two pins to the same pin multiplexed signal function is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration.

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**Note**

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

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**Table 6-1. Pin Attributes (ALV Package)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
G20	ADC0_AIN0	ADC0_AIN0	0	A					1.8 V	VDDA_ADC0	Yes	ADC12B	
F20	ADC0_AIN1	ADC0_AIN1	0	A					1.8 V	VDDA_ADC0	Yes	ADC12B	
E21	ADC0_AIN2	ADC0_AIN2	0	A					1.8 V	VDDA_ADC0	Yes	ADC12B	
D20	ADC0_AIN3	ADC0_AIN3	0	A					1.8 V	VDDA_ADC0	Yes	ADC12B	

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
G21	ADC0_AIN4	ADC0_AIN4	0	A					1.8 V	VDDA_ADC0	Yes	ADC12B	
F21	ADC0_AIN5	ADC0_AIN5	0	A					1.8 V	VDDA_ADC0	Yes	ADC12B	
F19	ADC0_AIN6	ADC0_AIN6	0	A					1.8 V	VDDA_ADC0	Yes	ADC12B	
E20	ADC0_AIN7	ADC0_AIN7	0	A					1.8 V	VDDA_ADC0	Yes	ADC12B	
H12	CAP_VDDS0	CAP_VDDS0		CAP									
T7	CAP_VDDS1	CAP_VDDS1		CAP									
R11	CAP_VDDS2	CAP_VDDS2		CAP									
N14	CAP_VDDS3	CAP_VDDS3		CAP									
M16	CAP_VDDS4	CAP_VDDS4		CAP									
L13	CAP_VDDS5	CAP_VDDS5		CAP									
K15	CAP_VDDSHV_MMC1	CAP_VDDSHV_MMC1		CAP									
H10	CAP_VDDS_MCU	CAP_VDDS_MCU		CAP									
H2	DDR0_ACT_n	DDR0_ACT_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H1	DDR0_ALERT_n	DDR0_ALERT_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J5	DDR0_CAS_n	DDR0_CAS_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K5	DDR0_PAR	DDR0_PAR		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F6	DDR0_RAS_n	DDR0_RAS_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H4	DDR0_WE_n	DDR0_WE_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D2	DDR0_A0	DDR0_A0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
C5	DDR0_A1	DDR0_A1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E2	DDR0_A2	DDR0_A2		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D4	DDR0_A3	DDR0_A3		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D3	DDR0_A4	DDR0_A4		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F2	DDR0_A5	DDR0_A5		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J2	DDR0_A6	DDR0_A6		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	



Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
L5	DDR0_A7	DDR0_A7		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J3	DDR0_A8	DDR0_A8		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J4	DDR0_A9	DDR0_A9		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K3	DDR0_A10	DDR0_A10		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
J1	DDR0_A11	DDR0_A11		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M5	DDR0_A12	DDR0_A12		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
K4	DDR0_A13	DDR0_A13		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G4	DDR0_BA0	DDR0_BA0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G5	DDR0_BA1	DDR0_BA1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
G2	DDR0_BG0	DDR0_BG0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H3	DDR0_BG1	DDR0_BG1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
H5	DDR0_CAL0	DDR0_CAL0		A					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F1	DDR0_CK0	DDR0_CK0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E1	DDR0_CK0_n	DDR0_CK0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F4	DDR0_CKE0	DDR0_CKE0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F3	DDR0_CKE1	DDR0_CKE1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E3	DDR0_CS0_n	DDR0_CS0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E4	DDR0_CS1_n	DDR0_CS1_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B2	DDR0_DM0	DDR0_DM0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M2	DDR0_DM1	DDR0_DM1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
A3	DDR0_DQ0	DDR0_DQ0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
A2	DDR0_DQ1	DDR0_DQ1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B5	DDR0_DQ2	DDR0_DQ2		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
A4	DDR0_DQ3	DDR0_DQ3		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B3	DDR0_DQ4	DDR0_DQ4		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	

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Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
C4	DDR0_DQ5	DDR0_DQ5		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
C2	DDR0_DQ6	DDR0_DQ6		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B4	DDR0_DQ7	DDR0_DQ7		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N5	DDR0_DQ8	DDR0_DQ8		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L4	DDR0_DQ9	DDR0_DQ9		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
L2	DDR0_DQ10	DDR0_DQ10		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M3	DDR0_DQ11	DDR0_DQ11		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N4	DDR0_DQ12	DDR0_DQ12		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N3	DDR0_DQ13	DDR0_DQ13		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M4	DDR0_DQ14	DDR0_DQ14		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N2	DDR0_DQ15	DDR0_DQ15		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
C1	DDR0_DQS0	DDR0_DQS0		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
B1	DDR0_DQS0_n	DDR0_DQS0_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
N1	DDR0_DQS1	DDR0_DQS1		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
M1	DDR0_DQS1_n	DDR0_DQS1_n		IO					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
E5	DDR0_ODT0	DDR0_ODT0		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
F5	DDR0_ODT1	DDR0_ODT1		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D5	DDR0_RESET0_n	DDR0_RESET0_n		O					1.1 V/1.2 V	VDDS_DDR, VDDS_DDR_C		DDR	
D18	ECAP0_IN_APWM_OUT	ECAP0_IN_APWM_OUT	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SYNC0_OUT	1	O				7					
		CPTS0_RFT_CLK	2	I	0			7					
		CP_GEMAC_CPTS0_RFT_CLK	5	I	0			7					
		SPI4_CS3	6	IO	1			7					
		GPIO1_68	7	IO	pad			7					
D10	EMU0	EMU0	0	IO		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
E10	EMU1	EMU1	0	IO		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_OBSCLK0	15	O				0					
C19	EXTINTn	EXTINTn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS	
		GPIO1_70	7	IO	pad			7					
A19	EXT_REFCLK1	EXT_REFCLK1	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SYNC1_OUT	1	O				7					
		SPI2_CS3	2	IO	1			7					
		CLKOUT0	5	O				7					
		GPIO1_69	7	IO	pad			7					
P16	GPMC0_ADVn_ALE	GPMC0_ADVn_ALE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX5_CLK	1	I	0			7					
		UART5_RXD	2	I	1			7					
		EHRPWM_TZn_IN3	3	I	0			7					
		TRC_DATA15	6	O				7					
		GPIO0_32	7	IO	pad			7					
		PRG0_PWM3_TZ_IN	9	I	0			7					
R17	GPMC0_CLK	GPMC0_CLK	0	O	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX4_CLK	1	I	0			7					
		UART4_RTSn	2	O				7					
		EHRPWM3_SYNCO	3	O				7					
		GPMC0_FCLK_MUX	4	O				7					
		TRC_DATA14	6	O				7					
		GPIO0_31	7	IO	pad			7					
		PRG0_PWM3_TZ_OUT	9	O				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
N17	GPMC0_DIR	GPMC0_DIR	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		EQEP0_B	3	I	0			7					
		GPI00_40	7	IO	pad			7					
		EHRPWM6_B	8	IO	0			7					
		PRG1_PWM2_B0	9	IO	1			7					
R18	GPMC0_OEn_REn	GPMC0_OEn_REn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX5_D0	1	I	0			7					
		UART5_TXD	2	O				7					
		EHRPWM4_A	3	IO	0			7					
		TRC_DATA16	6	O				7					
		GPI00_33	7	IO	pad			7					
		PRG0_PWM3_A1	9	IO	0			7					
T21	GPMC0_WEn	GPMC0_WEn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX5_D1	1	I	0			7					
		UART5_RTSn	2	O				7					
		EHRPWM4_B	3	IO	0			7					
		TRC_DATA17	6	O				7					
		GPI00_34	7	IO	pad			7					
		PRG0_PWM3_B1	9	IO	1			7					

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
N16	GPMC0_WPn	GPMC0_WPn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_TX1_CLK	1	O				7					
		EQEP0_A	3	I	0			7					
		GPMC0_A22	4	OZ				7					
		TRC_DATA22	6	O				7					
		GPIO0_39	7	IO	pad			7					
		EHRPWM6_A	8	IO	0			7					
PRG1_PWM2_A0	9	IO	0			7							
T20	GPMC0_AD0	GPMC0_AD0	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX2_CLK	1	I	0			7					
		UART2_RXD	2	I	1			7					
		EHRPWM0_SYNCI	3	I	0			7					
		TRC_CLK	6	O				7					
		GPIO0_15	7	IO	pad			7					
		BOOTMODE00	Bootstra p	I				7					
U21	GPMC0_AD1	GPMC0_AD1	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX2_D0	1	I	0			7					
		UART2_TXD	2	O				7					
		EHRPWM0_SYNCO	3	O				7					
		TRC_CTL	6	O				7					
		GPIO0_16	7	IO	pad			7					
		PRG0_PWM2_TZ_OUT	9	O				7					
BOOTMODE01	Bootstra p	I				7							

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
T18	GPMC0_AD2	GPMC0_AD2	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX2_D1	1	I	0			7					
		UART2_RTSn	2	O				7					
		EHRPWM_TZn_IN0	3	I	0			7					
		TRC_DATA0	6	O				7					
		GPIOD_17	7	IO	pad			7					
		PRG0_PWM2_TZ_IN	9	I	0			7					
		BOOTMODE02	Bootstra p	I				7					
U20	GPMC0_AD3	GPMC0_AD3	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX3_CLK	1	I	0			7					
		UART3_RXD	2	I	1			7					
		EHRPWM0_A	3	IO	0			7					
		TRC_DATA1	6	O				7					
		GPIOD_18	7	IO	pad			7					
		PRG0_PWM2_A0	9	IO	0			7					
		BOOTMODE03	Bootstra p	I				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
U18	GPMC0_AD4	GPMC0_AD4	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX3_D0	1	I	0			7					
		UART3_TXD	2	O				7					
		EHRPWM0_B	3	IO	0			7					
		TRC_DATA2	6	O				7					
		GPIO0_82	7	IO	pad			7					
		PRG0_PWM2_B0	9	IO	1			7					
BOOTMODE04	Bootstra p	I				7							
U19	GPMC0_AD5	GPMC0_AD5	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX3_D1	1	I	0			7					
		UART3_RTSn	2	O				7					
		EHRPWM1_A	3	IO	0			7					
		TRC_DATA3	6	O				7					
		GPIO0_83	7	IO	pad			7					
		PRG0_PWM2_A1	9	IO	0			7					
BOOTMODE05	Bootstra p	I				7							

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
V20	GPMC0_AD6	GPMC0_AD6	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX4_D0	1	I	0			7					
		UART4_RXD	2	I	1			7					
		EHRPWM1_B	3	IO	0			7					
		TRC_DATA4	6	O				7					
		GPIO0_21	7	IO	pad			7					
		PRG0_PWM2_B1	9	IO	1			7					
		BOOTMODE06	Bootstra p	I				7					
V21	GPMC0_AD7	GPMC0_AD7	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX4_D1	1	I	0			7					
		UART4_TXD	2	O				7					
		EHRPWM_TZn_IN1	3	I	0			7					
		EHRPWM8_A	4	IO	0			7					
		TRC_DATA5	6	O				7					
		GPIO0_22	7	IO	pad			7					
		PRG1_PWM2_A2	9	IO	0			7					
		BOOTMODE07	Bootstra p	I				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
V19	GPMC0_AD8	GPMC0_AD8	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX0_CLK	1	I	0			7					
		UART2_CTSn	2	I	1			7					
		EHRPWM2_A	3	IO	0			7					
		TRC_DATA6	6	O				7					
		GPIOD_23	7	IO	pad			7					
		PRG0_PWM2_A2	9	IO	0			7					
BOOTMODE08	Bootstra p	I				7							
T17	GPMC0_AD9	GPMC0_AD9	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX0_D0	1	I	0			7					
		UART3_CTSn	2	I	1			7					
		EHRPWM2_B	3	IO	0			7					
		TRC_DATA7	6	O				7					
		GPIOD_24	7	IO	pad			7					
		PRG0_PWM2_B2	9	IO	1			7					
BOOTMODE09	Bootstra p	I				7							

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
R16	GPMC0_AD10	GPMC0_AD10	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX0_D1	1	I	0			7					
		UART4_CTSn	2	I	1			7					
		EHRPWM_TZn_IN2	3	I	0			7					
		EHRPWM8_B	4	IO	0			7					
		TRC_DATA8	6	O				7					
		GPI00_25	7	IO	pad			7					
		PRG1_PWM2_B2	9	IO	1			7					
		BOOTMODE10	Bootstra p	I			7						
W20	GPMC0_AD11	GPMC0_AD11	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX1_CLK	1	I	0			7					
		UART5_CTSn	2	I	1			7					
		EQEP1_A	3	I	0			7					
		TRC_DATA9	6	O				7					
		GPI00_26	7	IO	pad			7					
		EHRPWM7_A	8	IO	0			7					
				BOOTMODE11	Bootstra p	I							

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
W21	GPMC0_AD12	GPMC0_AD12	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX1_D0	1	I	0			7					
		UART6_CTSn	2	I	1			7					
		EQEP1_B	3	I	0			7					
		TRC_DATA10	6	O				7					
		GPIO0_27	7	IO	pad			7					
		EHRPWM7_B	8	IO	0			7					
BOOTMODE12	Bootstra p	I				7							
V18	GPMC0_AD13	GPMC0_AD13	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_RX1_D1	1	I	0			7					
		EHRPWM3_A	3	IO	0			7					
		TRC_DATA11	6	O				7					
		GPIO0_28	7	IO	pad			7					
		PRG0_PWM3_A0	9	IO	0			7					
		BOOTMODE13	Bootstra p	I				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
Y21	GPMC0_AD14	GPMC0_AD14	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_TX0_D0	1	O				7					
		UART6_RXD	2	I	1			7					
		EHRPWM3_B	3	IO	0			7					
		TRC_DATA12	6	O				7					
		GPIO0_29	7	IO	pad			7					
		PRG0_PWM3_B0	9	IO	1			7					
BOOTMODE14	Bootstra p	I				7							
Y20	GPMC0_AD15	GPMC0_AD15	0	IO	0	On / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_TX0_D1	1	O				7					
		UART6_TXD	2	O				7					
		EHRPWM3_SYNCI	3	I	0			7					
		TRC_DATA13	6	O				7					
		GPIO0_30	7	IO	pad			7					
		BOOTMODE15	Bootstra p	I				7					
P17	GPMC0_BE0n_CLE	GPMC0_BE0n_CLE	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_TX1_D0	1	O				7					
		UART6_RTSn	2	O				7					
		EHRPWM_TZn_IN4	3	I	0			7					
		EHRPWM7_A	5	IO	0			7					
		TRC_DATA18	6	O				7					
		GPIO0_35	7	IO	pad			7					
		PRG1_PWM2_A1	9	IO	0			7					

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
T19	GPMC0_BE1n	GPMC0_BE1n	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FSI_TX0_CLK	1	O				7					
		EHRPWM5_A	3	IO	0			7					
		TRC_DATA19	6	O				7					
		GPIO0_36	7	IO	pad			7					
		PRG0_PWM3_A2	9	IO	0			7					
R19	GPMC0_CSn0	GPMC0_CSn0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		EQEP0_S	3	IO	0			7					
		TRC_DATA23	6	O				7					
		GPIO0_41	7	IO	pad			7					
		EHRPWM6_SYNCI	8	I	0			7					
R20	GPMC0_CSn1	GPMC0_CSn1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		EQEP0_I	3	IO	0			7					
		EHRPWM_TZn_IN2	5	I	0			7					
		GPIO0_42	7	IO	pad			7					
		EHRPWM6_SYNCO	8	O				7					
		PRG1_PWM2_TZ_OUT	9	O				7					
P19	GPMC0_CSn2	GPMC0_CSn2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C2_SCL	1	IOD	1			7					
		TIMER_IO8	2	IO	0			7					
		EQEP1_S	3	IO	0			7					
		EHRPWM_TZn_IN4	5	I	0			7					
		GPIO0_43	7	IO	pad			7					
		PRG1_PWM2_TZ_IN	9	I	0			7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
R21	GPMC0_CSn3	GPMC0_CSn3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		I2C2_SDA	1	IOD	1			7					
		TIMER_IO9	2	IO	0			7					
		EQEP1_I	3	IO	0			7					
		GPMC0_A20	4	OZ				7					
		EHRPWM_TZn_IN5	5	I	0			7					
		GPIO0_44	7	IO	pad			7					
W19	GPMC0_WAIT0	GPMC0_WAIT0	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		EHRPWM5_B	3	IO	0			7					
		TRC_DATA20	6	O				7					
		GPIO0_37	7	IO	pad			7					
		PRG0_PWM3_B2	9	IO	1			7					
Y18	GPMC0_WAIT1	GPMC0_WAIT1	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD
		FS1_TX1_D1	1	O				7					
		EHRPWM_TZn_IN5	3	I	0			7					
		GPMC0_A21	4	OZ				7					
		EHRPWM7_B	5	IO	0			7					
		TRC_DATA21	6	O				7					
		GPIO0_38	7	IO	pad			7					
		PRG1_PWM2_B1	9	IO	1			7					
A18	I2C0_SCL	I2C0_SCL	0	IOD	1	Off / Off / Off	On / SS / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS	
		UART6_CTSn	4	I	1			7					
		GPIO1_64	7	IO	pad			7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
B18	I2C0_SDA	I2C0_SDA	0	IOD	1	Off / Off / Off	On / SS / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS	
		UART6_RTSn	4	O			7						
		GPIO1_65	7	IO	pad		7						
C18	I2C1_SCL	I2C1_SCL	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CPTS0_HW1TSPUSH	1	I	0		7						
		TIMER_IO0	2	IO	0		7						
		SPI2_CS1	3	IO	1		7						
		GPIO1_66	7	IO	pad		7						
B19	I2C1_SDA	I2C1_SDA	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CPTS0_HW2TSPUSH	1	I	0		7						
		TIMER_IO1	2	IO	0		7						
		SPI2_CS2	3	IO	1		7						
		GPIO1_67	7	IO	pad		7						
B17	MCAN0_RX	MCAN0_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART4_TXD	1	O			7						
		TIMER_IO3	2	IO	0		7						
		SYNC3_OUT	3	O			7						
		SPI4_CS2	6	IO	1		7						
		GPIO1_61	7	IO	pad		7						
		EQEP2_S	8	IO	0		7						
		UART0_RIn	9	I	1		7						

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
A17	MCAN0_TX	MCAN0_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART4_RXD	1	I	1			7					
		TIMER_IO2	2	IO	0			7					
		SYNC2_OUT	3	O				7					
		SPI4_CS1	6	IO	1			7					
		GPI01_60	7	IO	pad			7					
		EQEP2_I	8	IO	0			7					
		UART0_DTRn	9	O				7					
D17	MCAN1_RX	MCAN1_RX	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		I2C3_SDA	1	IOD	1			7					
		ECAP2_IN_APWM_OUT	2	IO	0			7					
		OBSCLK0	3	O				7					
		TIMER_IO5	4	IO	0			7					
		UART5_TXD	5	O				7					
		EHRPWM_SOCB	6	O				7					
		GPI01_63	7	IO	pad			7					
		EQEP2_B	8	I	0			7					
		UART0_DSRn	9	I	1			7					
		OBSCLK0	15	O				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
C17	MCAN1_TX	MCAN1_TX	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		I2C3_SCL	1	IOD	1			7					
		ECAP1_IN_APWM_OUT	2	IO	0			7					
		SYSCLKOUT0	3	O				7					
		TIMER_IO4	4	IO	0			7					
		UART5_RXD	5	I	1			7					
		EHRPWM_SOCA	6	O				7					
		GPIO1_62	7	IO	pad			7					
		EQEP2_A	8	I	0			7					
UART0_DCDn	9	I	1			7							
E9	MCU_I2C0_SCL	MCU_I2C0_SCL	0	IOD	1	Off / Off / Off	On / SS / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
		MCU_GPIO0_18	7	IO	pad			7					
A10	MCU_I2C0_SDA	MCU_I2C0_SDA	0	IOD	1	Off / Off / Off	On / SS / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	I2C OD FS	
		MCU_GPIO0_19	7	IO	pad			7					
A11	MCU_I2C1_SCL	MCU_I2C1_SCL	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_20	7	IO	pad			7					
B10	MCU_I2C1_SDA	MCU_I2C1_SDA	0	IOD	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_21	7	IO	pad			7					
C21	MCU_OSC0_XI	MCU_OSC0_XI		I					1.8 V	VDDS_OSC	Yes	HFOSC	
B20	MCU_OSC0_XO	MCU_OSC0_XO		O					1.8 V	VDDS_OSC	Yes	HFOSC	
B21	MCU_PORz	MCU_PORz	0	I				0	1.8 V	VDDS_OSC	Yes	FS RESET	
B13	MCU_RESETSTATz	MCU_RESETSTATz	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_22	7	IO	pad			0					
B12	MCU_RESETz	MCU_RESETz	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
A20	MCU_SAFETY_ERRORn	MCU_SAFETY_ERRORn	0	IO		Off / Off / Down	On / SS / Down	0	1.8 V	VDDS_OSC	Yes	LVCMOS	PU/PD

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
E6	MCU_SPI0_CLK	MCU_SPI0_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_11	7	IO	pad			7					
D7	MCU_SPI1_CLK	MCU_SPI1_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_7	7	IO	pad			7					
D6	MCU_SPI0_CS0	MCU_SPI0_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_13	7	IO	pad			7					
C6	MCU_SPI0_CS1	MCU_SPI0_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_OBSCLK0	1	O				7					
		MCU_SYSCLKOUT0	2	O				7					
		MCU_GPIO0_12	7	IO	pad			7					
E7	MCU_SPI0_D0	MCU_SPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_10	7	IO	pad			7					
B6	MCU_SPI0_D1	MCU_SPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_4	7	IO	pad			7					
A7	MCU_SPI1_CS0	MCU_SPI1_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_5	7	IO	pad			7					
B7	MCU_SPI1_CS1	MCU_SPI1_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_EXT_REFCLK0	1	I	0			7					
		MCU_GPIO0_6	7	IO	pad			7					
C7	MCU_SPI1_D0	MCU_SPI1_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_8	7	IO	pad			7					
C8	MCU_SPI1_D1	MCU_SPI1_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_9	7	IO	pad			7					

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
D8	MCU_UART0_CTSn	MCU_UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO0	1	IO	0			7					
		MCU_SPI0_CS2	2	IO	1			7					
		MCU_GPIO0_1	7	IO	pad			7					
E8	MCU_UART0_RTSn	MCU_UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO1	1	IO	0			7					
		MCU_SPI1_CS2	2	IO	1			7					
		MCU_GPIO0_0	7	IO	pad			7					
A9	MCU_UART0_RXD	MCU_UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_3	7	IO	pad			7					
A8	MCU_UART0_TXD	MCU_UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_2	7	IO	pad			7					
B8	MCU_UART1_CTSn	MCU_UART1_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO2	1	IO	0			7					
		MCU_SPI0_CS3	2	IO	1			7					
		MCU_GPIO0_16	7	IO	pad			7					
B9	MCU_UART1_RTSn	MCU_UART1_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_TIMER_IO3	1	IO	0			7					
		MCU_SPI1_CS3	2	IO	1			7					
		MCU_GPIO0_17	7	IO	pad			7					
C9	MCU_UART1_RXD	MCU_UART1_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_14	7	IO	pad			7					
D9	MCU_UART1_TXD	MCU_UART1_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
		MCU_GPIO0_15	7	IO	pad			7					

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
F18	MMC0_CALPAD	MMC0_CALPAD		A					1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
G18	MMC0_CLK	MMC0_CLK		IO					1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
J21	MMC0_CMD	MMC0_CMD		IO	1				1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
G19	MMC0_DS	MMC0_DS		IO	1				1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
L20	MMC1_CLK	MMC1_CLK	0	IO		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART2_CTSn	1	I	1			7					
		TIMER_IO4	2	IO	0			7					
		UART4_RXD	3	I	1			7					
		GPIO1_75	7	IO	pad			7					
J19	MMC1_CMD	MMC1_CMD	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		UART2_RTSn	1	O				7					
		TIMER_IO5	2	IO	0			7					
		UART4_TXD	3	O				7					
		GPIO1_76	7	IO	pad			7					
D19	MMC1_SDCD	MMC1_SDCD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART3_CTSn	1	I	1			7					
		TIMER_IO6	2	IO	0			7					
		UART5_RXD	3	I	1			7					
		GPIO1_77	7	IO	pad			7					

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Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
C20	MMC1_SDWP	MMC1_SDWP	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		UART3_RTSn	1	O				7					
		TIMER_IO7	2	IO	0			7					
		UART5_TXD	3	O			7						
		GPIO1_78	7	IO	pad		7						
K20	MMC0_DAT0	MMC0_DAT0		IO	1				1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
J20	MMC0_DAT1	MMC0_DAT1		IO	1				1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
J18	MMC0_DAT2	MMC0_DAT2		IO	1				1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
J17	MMC0_DAT3	MMC0_DAT3		IO	1				1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
H17	MMC0_DAT4	MMC0_DAT4		IO	1				1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
H19	MMC0_DAT5	MMC0_DAT5		IO	1				1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
H18	MMC0_DAT6	MMC0_DAT6		IO	1				1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
G17	MMC0_DAT7	MMC0_DAT7		IO	1				1.8 V	VDDS_MMC0, VDD_MMC0, VDD_DLL_MMC0		eMMCPHY	PU/PD
K21	MMC1_DAT0	MMC1_DAT0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_HW2TSPUSH	1	I	0			7					
		TIMER_IO3	2	IO	0			7					
		UART3_TXD	3	O			7						
		GPIO1_74	7	IO	pad		7						

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
L21	MMC1_DAT1	MMC1_DAT1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_HW1TSPUSH	1	I	0			7					
		TIMER_IO2	2	IO	0			7					
		UART3_RXD	3	I	1			7					
		GPIO1_73	7	IO	pad			7					
K19	MMC1_DAT2	MMC1_DAT2	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_TS_SYNC	1	O				7					
		TIMER_IO1	2	IO	0			7					
		UART2_TXD	3	O				7					
		GPIO1_72	7	IO	pad			7					
K18	MMC1_DAT3	MMC1_DAT3	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD
		CP_GEMAC_CPTS0_TS_COMP	1	O				7					
		TIMER_IO0	2	IO	0			7					
		UART2_RXD	3	I	1			7					
		GPIO1_71	7	IO	pad			7					
N20	OSPI0_CLK	OSPI0_CLK	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_0	7	IO	pad			7					
N19	OSPI0_DQS	OSPI0_DQS	0	I	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_2	7	IO	pad			7					
N21	OSPI0_LBCLKO	OSPI0_LBCLKO	0	IO	0	Off / Off / Off	On / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_1	7	IO	pad			7					
L19	OSPI0_CSn0	OSPI0_CSn0	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_11	7	IO	pad			7					
L18	OSPI0_CSn1	OSPI0_CSn1	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_12	7	IO	pad			7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
K17	OSPI0_CSn2	OSPI0_CSn2	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		OSPI0_RESET_OUT1	2	O				7					
		GPIO0_13	7	IO	pad			7					
L17	OSPI0_CSn3	OSPI0_CSn3	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		OSPI0_RESET_OUT0	1	O				7					
		OSPI0_ECC_FAIL	2	I	1			7					
		GPIO0_14	7	IO	pad			7					
M19	OSPI0_D0	OSPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_3	7	IO	pad			7					
M18	OSPI0_D1	OSPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_4	7	IO	pad			7					
M20	OSPI0_D2	OSPI0_D2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_5	7	IO	pad			7					
M21	OSPI0_D3	OSPI0_D3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_6	7	IO	pad			7					
P21	OSPI0_D4	OSPI0_D4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_7	7	IO	pad			7					
P20	OSPI0_D5	OSPI0_D5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_8	7	IO	pad			7					
N18	OSPI0_D6	OSPI0_D6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_9	7	IO	pad			7					
M17	OSPI0_D7	OSPI0_D7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD
		GPIO0_10	7	IO	pad			7					
E17	PORz_OUT	PORz_OUT	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
P3	PRG0_MDIO0_MDC	PRG0_MDIO0_MDC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO1_41	7	IO	pad			7					
		GPMC0_A13	9	OZ				7					
P2	PRG0_MDIO0_MDIO	PRG0_MDIO0_MDIO	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		GPIO1_40	7	IO	pad			7					
		GPMC0_A12	9	OZ				7					
Y1	PRG0_PRU0_GPO0	PRG0_PRU0_GPO0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI0	1	I	0			7					
		PRG0_RGMII1_RD0	2	I	0			7					
		PRG0_PWM3_A0	3	IO	0			7					
		GPIO1_0	7	IO	pad			7					
		UART2_CTSn	10	I	1			7					
R4	PRG0_PRU0_GPO1	PRG0_PRU0_GPO1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI1	1	I	0			7					
		PRG0_RGMII1_RD1	2	I	0			7					
		PRG0_PWM3_B0	3	IO	1			7					
		GPIO1_1	7	IO	pad			7					
		UART2_TXD	10	O				7					
U2	PRG0_PRU0_GPO2	PRG0_PRU0_GPO2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI2	1	I	0			7					
		PRG0_RGMII1_RD2	2	I	0			7					
		PRG0_PWM2_A0	3	IO	0			7					
		GPIO1_2	7	IO	pad			7					
		GPMC0_A0	9	OZ				7					
		UART2_RTSn	10	O				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
V2	PRG0_PRU0_GPO3	PRG0_PRU0_GPO3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI3	1	I	0			7					
		PRG0_RGMII1_RD3	2	I	0			7					
		PRG0_PWM3_A2	3	IO	0			7					
		GPIO1_3	7	IO	pad			7					
		UART3_CTSn	10	I	1			7					
AA2	PRG0_PRU0_GPO4	PRG0_PRU0_GPO4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI4	1	I	0			7					
		PRG0_RGMII1_RX_CTL	2	I	0			7					
		PRG0_PWM2_B0	3	IO	1			7					
		GPIO1_4	7	IO	pad			7					
		GPMC0_A1	9	OZ				7					
		UART3_TXD	10	O				7					
R3	PRG0_PRU0_GPO5	PRG0_PRU0_GPO5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI5	1	I	0			7					
		PRG0_PWM3_B2	3	IO	1			7					
		GPIO1_5	7	IO	pad			7					
		UART3_RTSn	10	O				7					
T3	PRG0_PRU0_GPO6	PRG0_PRU0_GPO6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI6	1	I	0			7					
		PRG0_RGMII1_RXC	2	I	0			7					
		PRG0_PWM3_A1	3	IO	0			7					
		GPIO1_6	7	IO	pad			7					
		UART4_CTSn	10	I	1			7					

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
T1	PRG0_PRU0_GPO7	PRG0_PRU0_GPO7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI7	1	I	0			7					
		PRG0_IEP0_EDC_LATCH_IN1	2	I	0			7					
		PRG0_PWM3_B1	3	IO	1			7					
		CPTS0_HW2TSPUSH	4	I	0			7					
		CP_GEMAC_CPTS0_HW2TSPUSH	5	I	0			7					
		TIMER_IO6	6	IO	0			7					
		GPI01_7	7	IO	pad			7					
		UART4_TXD	10	O				7					
T2	PRG0_PRU0_GPO8	PRG0_PRU0_GPO8	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI8	1	I	0			7					
		PRG0_PWM2_A1	3	IO	0			7					
		GPI01_8	7	IO	pad			7					
		GPMC0_A2	9	OZ				7					
		UART4_RTSn	10	O				7					
		W6	PRG0_PRU0_GPO9	PRG0_PRU0_GPO9	0	IO	0	Off / Off / Off					
PRG0_PRU0_GPI9	1	I	0			7							
PRG0_UART0_CTSn	2	I	1			7							
PRG0_PWM3_TZ_IN	3	I	0			7							
RGMII1_RX_CTL	4	I	0			7							
RMII1_RX_ER	5	I	0			7							
PRG0_IEP0_EDIO_DATA_IN_OUT28	6	IO	0			7							
GPI01_9	7	IO	pad			7							
UART2_RXD	10	I	1			7							

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
AA5	PRG0_PRU0_GPO10	PRG0_PRU0_GPO10	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI10	1	I	0			7					
		PRG0_UART0_RTSn	2	O				7					
		PRG0_PWM2_B1	3	IO	1			7					
		RGMII1_RXC	4	I	0			7					
		RMII_REF_CLK	5	I	0			7					
		PRG0_IEP0_EDIO_DATA_IN_OUT29	6	IO	0			7					
		GPIO1_10	7	IO	pad			7					
		UART3_RXD	10	I	1			7					
Y3	PRG0_PRU0_GPO11	PRG0_PRU0_GPO11	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI11	1	I	0			7					
		PRG0_RGMII1_TD0	2	O				7					
		PRG0_PWM3_TZ_OUT	3	O				7					
		GPIO1_11	7	IO	pad			7					
				UART4_RXD	10	I	1						
AA3	PRG0_PRU0_GPO12	PRG0_PRU0_GPO12	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI12	1	I	0			7					
		PRG0_RGMII1_TD1	2	O				7					
		PRG0_PWM0_A0	3	IO	0			7					
		GPIO1_12	7	IO	pad			7					
				GPMC0_A14	9	OZ							

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
R6	PRG0_PRU0_GPO13	PRG0_PRU0_GPO13	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI13	1	I	0			7					
		PRG0_RGMII1_TD2	2	O				7					
		PRG0_PWM0_B0	3	IO	1			7					
		SPI3_D0	6	IO	0			7					
		GPI01_13	7	IO	pad			7					
		GPMC0_A15	9	OZ				7					
V4	PRG0_PRU0_GPO14	PRG0_PRU0_GPO14	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI14	1	I	0			7					
		PRG0_RGMII1_TD3	2	O				7					
		PRG0_PWM0_A1	3	IO	0			7					
		SPI3_D1	6	IO	0			7					
		GPI01_14	7	IO	pad			7					
		GPMC0_A3	9	OZ				7					
T5	PRG0_PRU0_GPO15	PRG0_PRU0_GPO15	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI15	1	I	0			7					
		PRG0_RGMII1_TX_CTL	2	O				7					
		PRG0_PWM0_B1	3	IO	1			7					
		SPI3_CS1	6	IO	1			7					
		GPI01_15	7	IO	pad			7					
		GPMC0_A16	9	OZ				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
U4	PRG0_PRU0_GPO16	PRG0_PRU0_GPO16	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI16	1	I	0			7					
		PRG0_RGMII1_TXC	2	IO	0			7					
		PRG0_PWM0_A2	3	IO	0			7					
		SPI3_CLK	6	IO	0			7					
		GPI01_16	7	IO	pad			7					
		GPMC0_A4	9	OZ				7					
U1	PRG0_PRU0_GPO17	PRG0_PRU0_GPO17	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI17	1	I	0			7					
		PRG0_IEP0_EDC_SYNC_OUT1	2	O				7					
		PRG0_PWM0_B2	3	IO	1			7					
		CPTS0_TS_SYNC	4	O				7					
		CP_GEMAC_CPTS0_TS_SYNC	5	O				7					
		SPI3_CS0	6	IO	1			7					
		GPI01_17	7	IO	pad			7					
		TIMER_IO11	8	IO	0			7					
GPMC0_A17	9	OZ				7							

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
V1	PRG0_PRU0_GPO18	PRG0_PRU0_GPO18	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI18	1	I	0			7					
		PRG0_IEP0_EDC_LATCH_IN0	2	I	0			7					
		PRG0_PWM0_TZ_IN	3	I	0			7					
		CPTS0_HW1TSPUSH	4	I	0			7					
		CP_GEMAC_CPTS0_HW1TSPUSH	5	I	0			7					
		EHRPWM8_A	6	IO	0			7					
		GPIO1_18	7	IO	pad			7					
		UART4_CTSn	8	I	1			7					
		GPMC0_A5	9	OZ				7					
UART2_RXD	10	I	1			7							
W1	PRG0_PRU0_GPO19	PRG0_PRU0_GPO19	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU0_GPI19	1	I	0			7					
		PRG0_IEP0_EDC_SYNC_OUT0	2	O				7					
		PRG0_PWM0_TZ_OUT	3	O				7					
		CPTS0_TS_COMP	4	O				7					
		CP_GEMAC_CPTS0_TS_COMP	5	O				7					
		EHRPWM8_B	6	IO	0			7					
		GPIO1_19	7	IO	pad			7					
		UART4_RTSn	8	O				7					
		GPMC0_A6	9	OZ				7					
UART3_RXD	10	I	1			7							

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
Y2	PRG0_PRU1_GPO0	PRG0_PRU1_GPO0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI0	1	I	0			7					
		PRG0_RGMII2_RD0	2	I	0			7					
		GPI01_20	7	IO	pad			7					
		EQEP0_A	8	I	0			7					
		UART5_CTSn	10	I	1			7					
W2	PRG0_PRU1_GPO1	PRG0_PRU1_GPO1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI1	1	I	0			7					
		PRG0_RGMII2_RD1	2	I	0			7					
		GPI01_21	7	IO	pad			7					
		EQEP0_B	8	I	0			7					
		UART5_TXD	10	O				7					
V3	PRG0_PRU1_GPO2	PRG0_PRU1_GPO2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI2	1	I	0			7					
		PRG0_RGMII2_RD2	2	I	0			7					
		PRG0_PWM2_A2	3	IO	0			7					
		GPI01_22	7	IO	pad			7					
		EQEP0_S	8	IO	0			7					
		UART5_RTSn	10	O				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
T4	PRG0_PRU1_GPO3	PRG0_PRU1_GPO3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI3	1	I	0			7					
		PRG0_RGMII2_RD3	2	I	0			7					
		GPIO1_23	7	IO	pad			7					
		EQEP1_A	8	I	0			7					
		GPMC0_A18	9	OZ				7					
		UART6_CTSn	10	I	1			7					
W3	PRG0_PRU1_GPO4	PRG0_PRU1_GPO4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI4	1	I	0			7					
		PRG0_RGMII2_RX_CTL	2	I	0			7					
		PRG0_PWM2_B2	3	IO	1			7					
		GPIO1_24	7	IO	pad			7					
		EQEP1_B	8	I	0			7					
		UART6_TXD	10	O				7					
P4	PRG0_PRU1_GPO5	PRG0_PRU1_GPO5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI5	1	I	0			7					
		GPIO1_25	7	IO	pad			7					
		EQEP1_S	8	IO	0			7					
		UART6_RTSn	10	O				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
R5	PRG0_PRU1_GPO6	PRG0_PRU1_GPO6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI6	1	I	0			7					
		PRG0_RGMII2_RXC	2	I	0			7					
		GPIO1_26	7	IO	pad			7					
		EQEP2_A	8	I	0			7					
		GPMC0_A19	9	OZ				7					
		UART4_CTSn	10	I	1			7					
W5	PRG0_PRU1_GPO7	PRG0_PRU1_GPO7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI7	1	I	0			7					
		PRG0_IEP1_EDC_LATCH_IN1	2	I	0			7					
		RGMII1_RD0	4	I	0			7					
		RMII1_RXD0	5	I	0			7					
		GPIO1_27	7	IO	pad			7					
		EQEP2_B	8	I	0			7					
		UART4_TXD	10	O				7					
R1	PRG0_PRU1_GPO8	PRG0_PRU1_GPO8	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI8	1	I	0			7					
		PRG0_PWM2_TZ_OUT	3	O				7					
		GPIO1_28	7	IO	pad			7					
		EQEP2_S	8	IO	0			7					
		UART4_RTSn	10	O				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
Y5	PRG0_PRU1_GPO9	PRG0_PRU1_GPO9	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI9	1	I	0			7					
		PRG0_UART0_RXD	2	I	1			7					
		RGMI1_RD1	4	I	0			7					
		RMII1_RXD1	5	I	0			7					
		PRG0_IEP0_EDIO_DATA_IN_OUT30	6	IO	0			7					
		GPI01_29	7	IO	pad			7					
		EQEP0_I	8	IO	0			7					
		UART5_RXD	10	I	1			7					
V6	PRG0_PRU1_GPO10	PRG0_PRU1_GPO10	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI10	1	I	0			7					
		PRG0_UART0_TXD	2	O				7					
		PRG0_PWM2_TZ_IN	3	I	0			7					
		RGMI1_RD2	4	I	0			7					
		RMII1_TXD0	5	O				7					
		PRG0_IEP0_EDIO_DATA_IN_OUT31	6	IO	0			7					
		GPI01_30	7	IO	pad			7					
		EQEP1_I	8	IO	0			7					
		UART6_RXD	10	I	1			7					
W4	PRG0_PRU1_GPO11	PRG0_PRU1_GPO11	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI11	1	I	0			7					
		PRG0_RGMII2_TD0	2	O				7					
		GPI01_31	7	IO	pad			7					
		EQEP2_I	8	IO	0			7					
		UART4_RXD	10	I	1			7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
Y4	PRG0_PRU1_GPO12	PRG0_PRU1_GPO12	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI12	1	I	0			7					
		PRG0_RGMII2_TD1	2	O				7					
		PRG0_PWM1_A0	3	IO	0			7					
		GPIO1_32	7	IO	pad			7					
		EQEP2_B	8	I	0			7					
		GPMC0_A7	9	OZ				7					
		UART4_TXD	10	O				7					
T6	PRG0_PRU1_GPO13	PRG0_PRU1_GPO13	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI13	1	I	0			7					
		PRG0_RGMII2_TD2	2	O				7					
		PRG0_PWM1_B0	3	IO	1			7					
		GPIO1_33	7	IO	pad			7					
		EQEP0_I	8	IO	0			7					
		GPMC0_A8	9	OZ				7					
		UART5_RXD	10	I	1			7					
U6	PRG0_PRU1_GPO14	PRG0_PRU1_GPO14	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI14	1	I	0			7					
		PRG0_RGMII2_TD3	2	O				7					
		PRG0_PWM1_A1	3	IO	0			7					
		GPIO1_34	7	IO	pad			7					
		EQEP1_I	8	IO	0			7					
		GPMC0_A9	9	OZ				7					
		UART6_RXD	10	I	1			7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
U5	PRG0_PRU1_GPO15	PRG0_PRU1_GPO15	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI15	1	I	0			7					
		PRG0_RGMII2_TX_CTL	2	O				7					
		PRG0_PWM1_B1	3	IO	1			7					
		GPIO1_35	7	IO	pad			7					
		GPMC0_A10	9	OZ				7					
		PRG0_ECAP0_IN_APWM_OUT	10	IO	0			7					
AA4	PRG0_PRU1_GPO16	PRG0_PRU1_GPO16	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI16	1	I	0			7					
		PRG0_RGMII2_TXC	2	IO	0			7					
		PRG0_PWM1_A2	3	IO	0			7					
		GPIO1_36	7	IO	pad			7					
		GPMC0_A11	9	OZ				7					
		PRG0_ECAP0_SYNC_OUT	10	O				7					
V5	PRG0_PRU1_GPO17	PRG0_PRU1_GPO17	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI17	1	I	0			7					
		PRG0_IEP1_EDC_SYNC_OUT1	2	O				7					
		PRG0_PWM1_B2	3	IO	1			7					
		RGMII1_RD3	4	I	0			7					
		RMII1_TXD1	5	O				7					
		GPIO1_37	7	IO	pad			7					
		PRG0_ECAP0_SYNC_OUT	8	O				7					
		PRG0_ECAP0_SYNC_IN	10	I	0			7					

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
P5	PRG0_PRU1_GPO18	PRG0_PRU1_GPO18	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI18	1	I	0			7					
		PRG0_IEP1_EDC_LATCH_IN0	2	I	0			7					
		PRG0_PWM1_TZ_IN	3	I	0			7					
		MDIO0_MDIO	4	IO	0			7					
		RMII1_TX_EN	5	O				7					
		EHRPWM7_A	6	IO	0			7					
		GPIO1_38	7	IO	pad			7					
		PRG0_ECAP0_SYNC_IN	8	I	0			7					
R2	PRG0_PRU1_GPO19	PRG0_PRU1_GPO19	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD
		PRG0_PRU1_GPI19	1	I	0			7					
		PRG0_IEP1_EDC_SYNC_OUT0	2	O				7					
		PRG0_PWM1_TZ_OUT	3	O				7					
		MDIO0_MDC	4	O				7					
		RMII1_CRSDV	5	I	0			7					
		EHRPWM7_B	6	IO	0			7					
		GPIO1_39	7	IO	pad			7					
		PRG0_ECAP0_IN_APWM_OUT	8	IO	0			7					
Y6	PRG1_MDIO0_MDC	PRG1_MDIO0_MDC	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MDIO0_MDC	4	O				7					
		GPIO0_86	7	IO	pad			7					
AA6	PRG1_MDIO0_MDIO	PRG1_MDIO0_MDIO	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		MDIO0_MDIO	4	IO	0			7					
		GPIO0_85	7	IO	pad			7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
Y7	PRG1_PRU0_GPO0	PRG1_PRU0_GPO0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI0	1	I	0			7					
		PRG1_RGMII1_RD0	2	I	0			7					
		PRG1_PWM3_A0	3	IO	0			7					
		GPIO0_45	7	IO	pad			7					
		GPMC0_AD16	8	IO	0			7					
U8	PRG1_PRU0_GPO1	PRG1_PRU0_GPO1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI1	1	I	0			7					
		PRG1_RGMII1_RD1	2	I	0			7					
		PRG1_PWM3_B0	3	IO	1			7					
		GPIO0_46	7	IO	pad			7					
		GPMC0_AD17	8	IO	0			7					
W8	PRG1_PRU0_GPO2	PRG1_PRU0_GPO2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI2	1	I	0			7					
		PRG1_RGMII1_RD2	2	I	0			7					
		PRG1_PWM2_A0	3	IO	0			7					
		GPIO0_47	7	IO	pad			7					
		GPMC0_AD18	8	IO	0			7					
V8	PRG1_PRU0_GPO3	PRG1_PRU0_GPO3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI3	1	I	0			7					
		PRG1_RGMII1_RD3	2	I	0			7					
		PRG1_PWM3_A2	3	IO	0			7					
		GPIO0_48	7	IO	pad			7					
		GPMC0_AD19	8	IO	0			7					

Table 6-1. Pin Attributes (ALV Package) (continued)

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
Y8	PRG1_PRU0_GPO4	PRG1_PRU0_GPO4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI4	1	I	0			7					
		PRG1_RGMII1_RX_CTL	2	I	0			7					
		PRG1_PWM2_B0	3	IO	1			7					
		GPIO0_49	7	IO	pad			7					
		GPMC0_AD20	8	IO	0			7					
V13	PRG1_PRU0_GPO5	PRG1_PRU0_GPO5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI5	1	I	0			7					
		PRG1_PWM3_B2	3	IO	1			7					
		RGMII1_RX_CTL	4	I	0			7					
		GPIO0_50	7	IO	pad			7					
		GPMC0_AD21	8	IO	0			7					
AA7	PRG1_PRU0_GPO6	PRG1_PRU0_GPO6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI6	1	I	0			7					
		PRG1_RGMII1_RXC	2	I	0			7					
		PRG1_PWM3_A1	3	IO	0			7					
		GPIO0_51	7	IO	pad			7					
		GPMC0_AD22	8	IO	0			7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
U13	PRG1_PRU0_GPO7	PRG1_PRU0_GPO7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI7	1	I	0			7					
		PRG1_IEP0_EDC_LATCH_IN1	2	I	0			7					
		PRG1_PWM3_B1	3	IO	1			7					
		CPTS0_HW2TSPUSH	4	I	0			7					
		CLKOUT0	5	O				7					
		TIMER_IO10	6	IO	0			7					
		GPI00_52	7	IO	pad			7					
GPMC0_AD23	8	IO	0			7							
W13	PRG1_PRU0_GPO8	PRG1_PRU0_GPO8	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI8	1	I	0			7					
		PRG1_PWM2_A1	3	IO	0			7					
		RGMII1_RXC	4	I	0			7					
		GPI00_53	7	IO	pad			7					
		GPMC0_AD24	8	IO	0			7					
U15	PRG1_PRU0_GPO9	PRG1_PRU0_GPO9	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI9	1	I	0			7					
		PRG1_UART0_CTSn	2	I	1			7					
		PRG1_PWM3_TZ_IN	3	I	0			7					
		RGMII1_TX_CTL	4	O				7					
		RMII1_RX_ER	5	I	0			7					
		PRG1_IEP0_EDIO_DATA_IN_OUT28	6	IO	0			7					
		GPI00_54	7	IO	pad			7					
GPMC0_AD25	8	IO	0			7							

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
U14	PRG1_PRU0_GPO10	PRG1_PRU0_GPO10	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI10	1	I	0			7					
		PRG1_UART0_RTSn	2	O				7					
		PRG1_PWM2_B1	3	IO	1			7					
		RGMII1_TXC	4	IO	0			7					
		RMII_REF_CLK	5	I	0			7					
		PRG1_IEP0_EDIO_DATA_IN_OUT29	6	IO	0			7					
		GPIO0_55	7	IO	pad			7					
		GPMC0_AD26	8	IO	0			7					
AA8	PRG1_PRU0_GPO11	PRG1_PRU0_GPO11	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI11	1	I	0			7					
		PRG1_RGMII1_TD0	2	O				7					
		PRG1_PWM3_TZ_OUT	3	O				7					
		GPIO0_56	7	IO	pad			7					
		GPMC0_AD27	8	IO	0			7					
U9	PRG1_PRU0_GPO12	PRG1_PRU0_GPO12	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI12	1	I	0			7					
		PRG1_RGMII1_TD1	2	O				7					
		PRG1_PWM0_A0	3	IO	0			7					
		GPIO0_57	7	IO	pad			7					
		GPMC0_AD28	8	IO	0			7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
W9	PRG1_PRU0_GPO13	PRG1_PRU0_GPO13	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI13	1	I	0			7					
		PRG1_RGMII1_TD2	2	O				7					
		PRG1_PWM0_B0	3	IO	1			7					
		GPIO0_58	7	IO	pad			7					
		GPMC0_AD29	8	IO	0			7					
AA9	PRG1_PRU0_GPO14	PRG1_PRU0_GPO14	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI14	1	I	0			7					
		PRG1_RGMII1_TD3	2	O				7					
		PRG1_PWM0_A1	3	IO	0			7					
		GPIO0_59	7	IO	pad			7					
		GPMC0_AD30	8	IO	0			7					
Y9	PRG1_PRU0_GPO15	PRG1_PRU0_GPO15	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI15	1	I	0			7					
		PRG1_RGMII1_TX_CTL	2	O				7					
		PRG1_PWM0_B1	3	IO	1			7					
		GPIO0_60	7	IO	pad			7					
		GPMC0_AD31	8	IO	0			7					
V9	PRG1_PRU0_GPO16	PRG1_PRU0_GPO16	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI16	1	I	0			7					
		PRG1_RGMII1_TXC	2	IO	0			7					
		PRG1_PWM0_A2	3	IO	0			7					
		GPIO0_61	7	IO	pad			7					
		GPMC0_BE2n	8	O				7					

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
U7	PRG1_PRU0_GPO17	PRG1_PRU0_GPO17	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI17	1	I	0			7					
		PRG1_IEP0_EDC_SYNC_OUT1	2	O				7					
		PRG1_PWM0_B2	3	IO	1			7					
		CPTS0_TS_SYNC	4	O				7					
		TIMER_IO7	6	IO	0			7					
		GPIO0_62	7	IO	pad			7					
		GPMC0_A0	8	OZ				7					
V7	PRG1_PRU0_GPO18	PRG1_PRU0_GPO18	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI18	1	I	0			7					
		PRG1_IEP0_EDC_LATCH_IN0	2	I	0			7					
		PRG1_PWM0_TZ_IN	3	I	0			7					
		CPTS0_HW1TSPUSH	4	I	0			7					
		TIMER_IO8	6	IO	0			7					
		GPIO0_63	7	IO	pad			7					
		GPMC0_A1	8	OZ				7					
W7	PRG1_PRU0_GPO19	PRG1_PRU0_GPO19	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU0_GPI19	1	I	0			7					
		PRG1_IEP0_EDC_SYNC_OUT0	2	O				7					
		PRG1_PWM0_TZ_OUT	3	O				7					
		CPTS0_TS_COMP	4	O				7					
		TIMER_IO9	6	IO	0			7					
		GPIO0_64	7	IO	pad			7					
		GPMC0_A2	8	OZ				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
W11	PRG1_PRU1_GPO0	PRG1_PRU1_GPO0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI0	1	I	0			7					
		PRG1_RGMII2_RD0	2	I	0			7					
		RGMII2_RD0	4	I	0			7					
		RMI2_RXD0	5	I	0			7					
		GPIOD_65	7	IO	pad			7					
		GPMC0_A3	8	OZ				7					
V11	PRG1_PRU1_GPO1	PRG1_PRU1_GPO1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI1	1	I	0			7					
		PRG1_RGMII2_RD1	2	I	0			7					
		RGMII2_RD1	4	I	0			7					
		RMI2_RXD1	5	I	0			7					
		GPIOD_66	7	IO	pad			7					
		GPMC0_A4	8	OZ				7					
AA12	PRG1_PRU1_GPO2	PRG1_PRU1_GPO2	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI2	1	I	0			7					
		PRG1_RGMII2_RD2	2	I	0			7					
		PRG1_PWM2_A2	3	IO	0			7					
		RGMII2_RD2	4	I	0			7					
		GPIOD_67	7	IO	pad			7					
		GPMC0_A5	8	OZ				7					

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
Y12	PRG1_PRU1_GPO3	PRG1_PRU1_GPO3	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI3	1	I	0			7					
		PRG1_RGMII2_RD3	2	I	0			7					
		RGMII2_RD3	4	I	0			7					
		GPIO0_68	7	IO	pad			7					
		GPMC0_A6	8	OZ				7					
W12	PRG1_PRU1_GPO4	PRG1_PRU1_GPO4	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI4	1	I	0			7					
		PRG1_RGMII2_RX_CTL	2	I	0			7					
		PRG1_PWM2_B2	3	IO	1			7					
		RGMII2_RX_CTL	4	I	0			7					
		RMII2_RX_ER	5	I	0			7					
		GPIO0_69	7	IO	pad			7					
		GPMC0_A7	8	OZ				7					
AA13	PRG1_PRU1_GPO5	PRG1_PRU1_GPO5	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI5	1	I	0			7					
		RGMII1_RD0	4	I	0			7					
		GPIO0_70	7	IO	pad			7					
		GPMC0_A8	8	OZ				7					
U11	PRG1_PRU1_GPO6	PRG1_PRU1_GPO6	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI6	1	I	0			7					
		PRG1_RGMII2_RXC	2	I	0			7					
		RGMII2_RXC	4	I	0			7					
		GPIO0_71	7	IO	pad			7					
		GPMC0_A9	8	OZ				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
V15	PRG1_PRU1_GPO7	PRG1_PRU1_GPO7	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI7	1	I	0			7					
		PRG1_IEP1_EDC_LATCH_IN1	2	I	0			7					
		RGMII1_TD0	4	O				7					
		RMII1_RXD0	5	I	0			7					
		SPI3_CS3	6	IO	1			7					
		GPI0_72	7	IO	pad			7					
		GPMC0_A10	8	OZ				7					
U12	PRG1_PRU1_GPO8	PRG1_PRU1_GPO8	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI8	1	I	0			7					
		PRG1_PWM2_TZ_OUT	3	O				7					
		RGMII1_RD1	4	I	0			7					
		GPI0_73	7	IO	pad			7					
		GPMC0_A11	8	OZ				7					
V14	PRG1_PRU1_GPO9	PRG1_PRU1_GPO9	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI9	1	I	0			7					
		PRG1_UART0_RXD	2	I	1			7					
		RGMII1_TD1	4	O				7					
		RMII1_RXD1	5	I	0			7					
		PRG1_IEP0_EDIO_DATA_IN_OUT30	6	IO	0			7					
		GPI0_74	7	IO	pad			7					
		GPMC0_A12	8	OZ				7					

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
W14	PRG1_PRU1_GPO10	PRG1_PRU1_GPO10	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI10	1	I	0			7					
		PRG1_UART0_TXD	2	O				7					
		PRG1_PWM2_TZ_IN	3	I	0			7					
		RGMII1_TD2	4	O				7					
		RMII1_TXD0	5	O				7					
		PRG1_IEP0_EDIO_DATA_IN_OUT31	6	IO	0			7					
		GPI0_75	7	IO	pad			7					
GPMC0_A13	8	OZ				7							
AA10	PRG1_PRU1_GPO11	PRG1_PRU1_GPO11	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI11	1	I	0			7					
		PRG1_RGMII2_TD0	2	O				7					
		RGMII2_TD0	4	O				7					
		RMII2_TXD0	5	O				7					
		GPI0_76	7	IO	pad			7					
		GPMC0_A14	8	OZ				7					
V10	PRG1_PRU1_GPO12	PRG1_PRU1_GPO12	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI12	1	I	0			7					
		PRG1_RGMII2_TD1	2	O				7					
		PRG1_PWM1_A0	3	IO	0			7					
		RGMII2_TD1	4	O				7					
		RMII2_TXD1	5	O				7					
		GPI0_77	7	IO	pad			7					
		GPMC0_A15	8	OZ				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
U10	PRG1_PRU1_GPO13	PRG1_PRU1_GPO13	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI13	1	I	0			7					
		PRG1_RGMII2_TD2	2	O				7					
		PRG1_PWM1_B0	3	IO	1			7					
		RGMII2_TD2	4	O				7					
		RMI2_CRS_DV	5	I	0			7					
		GPIO0_78	7	IO	pad			7					
		GPMC0_A16	8	OZ				7					
AA11	PRG1_PRU1_GPO14	PRG1_PRU1_GPO14	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI14	1	I	0			7					
		PRG1_RGMII2_TD3	2	O				7					
		PRG1_PWM1_A1	3	IO	0			7					
		RGMII2_TD3	4	O				7					
		GPIO0_79	7	IO	pad			7					
		GPMC0_A17	8	OZ				7					
		Y11	PRG1_PRU1_GPO15	PRG1_PRU1_GPO15	0	IO	0	Off / Off / Off					
PRG1_PRU1_GPI15	1			I	0			7					
PRG1_RGMII2_TX_CTL	2			O				7					
PRG1_PWM1_B1	3			IO	1			7					
RGMII2_TX_CTL	4			O				7					
RMI2_TX_EN	5			O				7					
GPIO0_80	7			IO	pad			7					
GPMC0_A18	8			OZ				7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
Y10	PRG1_PRU1_GPO16	PRG1_PRU1_GPO16	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI16	1	I	0			7					
		PRG1_RGMII2_TXC	2	IO	0			7					
		PRG1_PWM1_A2	3	IO	0			7					
		RGMII2_TXC	4	IO	0			7					
		GPIOD_81	7	IO	pad			7					
		GPMC0_A19	8	OZ				7					
AA14	PRG1_PRU1_GPO17	PRG1_PRU1_GPO17	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI17	1	I	0			7					
		PRG1_IEP1_EDC_SYNC_OUT1	2	O				7					
		PRG1_PWM1_B2	3	IO	1			7					
		RGMII1_TD3	4	O				7					
		RMII1_TXD1	5	O				7					
		GPIOD_19	7	IO	pad			7					
		GPMC0_BE3n	8	O				7					
		PRG1_ECAP0_SYNC_OUT	9	O				7					
Y13	PRG1_PRU1_GPO18	PRG1_PRU1_GPO18	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI18	1	I	0			7					
		PRG1_IEP1_EDC_LATCH_IN0	2	I	0			7					
		PRG1_PWM1_TZ_IN	3	I	0			7					
		RGMII1_RD2	4	I	0			7					
		RMII1_TX_EN	5	O				7					
		GPIOD_20	7	IO	pad			7					
		UART5_CTSn	8	I	1			7					
		PRG1_ECAP0_SYNC_IN	9	I	0			7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
V12	PRG1_PRU1_GPO19	PRG1_PRU1_GPO19	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD
		PRG1_PRU1_GPI19	1	I	0			7					
		PRG1_IEP1_EDC_SYNC_OUT0	2	O				7					
		PRG1_PWM1_TZ_OUT	3	O				7					
		RGMII1_RD3	4	I	0			7					
		RMII1_CRS_DV	5	I	0			7					
		SPI3_CS2	6	IO	1			7					
		GPI00_84	7	IO	pad			7					
		UART5_RTSn	8	O				7					
		PRG1_ECAP0_IN_APWM_OUT	9	IO	0			7					
F16	RESETSTATz	RESETSTATz	0	O		Off / Low / Off	Off / SS / Off	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
E18	RESET_REQz	RESET_REQz	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
T13	SERDES0_REXT	SERDES0_REXT		A					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	
W16	SERDES0_REFCLK0N	SERDES0_REFCLK0N		IO					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	
W17	SERDES0_REFCLK0P	SERDES0_REFCLK0P		IO					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	
Y15	SERDES0_RX0_N	SERDES0_RX0_N		I					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	
Y16	SERDES0_RX0_P	SERDES0_RX0_P		I					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES	

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE	
AA16	SERDES0_TX0_N	SERDES0_TX0_N		O					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES		
AA17	SERDES0_TX0_P	SERDES0_TX0_P		O					1.8 V	VDDA_1P8_SERDES0, VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C		SERDES		
D13	SPI0_CLK	SPI0_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	
		GPIO1_44	7	IO	pad									7
C14	SPI1_CLK	SPI1_CLK	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	
		EHRPWM6_SYNCI	3	I	0									7
		GPIO1_49	7	IO	pad									7
D12	SPI0_CS0	SPI0_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	
		GPIO1_42	7	IO	pad									7
C13	SPI0_CS1	SPI0_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	
		CPTS0_TS_COMP	1	O										7
		I2C2_SCL	2	IOD	1									7
		TIMER_IO10	3	IO	0									7
		PRG0_IEP0_EDIO_OUTVALID	4	O										7
		UART6_RXD	5	I	1									7
		ADC_EXT_TRIGGER0	6	I	0									7
		GPIO1_43	7	IO	pad									7
A13	SPI0_D0	SPI0_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	
		GPIO1_45	7	IO	pad									7
A14	SPI0_D1	SPI0_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	
		GPIO1_46	7	IO	pad									7

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
B14	SPI1_CS0	SPI1_CS0	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		EHRPWM6_A	3	IO	0			7					
		GPIO1_47	7	IO	pad			7					
D14	SPI1_CS1	SPI1_CS1	0	IO	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		CPTS0_TS_SYNC	1	O				7					
		I2C2_SDA	2	IOD	1			7					
		PRG1_IEP0_EDIO_OUTVALID	4	O				7					
		UART6_TXD	5	O				7					
		ADC_EXT_TRIGGER1	6	I	0			7					
		GPIO1_48	7	IO	pad			7					
		TIMER_IO11	8	IO	0			7					
B15	SPI1_D0	SPI1_D0	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		EHRPWM6_SYNC0	3	O				7					
		GPIO1_50	7	IO	pad			7					
A15	SPI1_D1	SPI1_D1	0	IO	0	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		EHRPWM6_B	3	IO	0			7					
		GPIO1_51	7	IO	pad			7					
B11	TCK	TCK	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
C11	TDI	TDI	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
A12	TDO	TDO	0	OZ		Off / Off / Up	Off / SS / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
C12	TMS	TMS	0	I		On / Off / Up	On / Off / Up	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD
D11	TRSTn	TRSTn	0	I		On / Off / Down	On / Off / Down	0	1.8 V/3.3 V	VDDSHV_MCU	Yes	LVCMOS	PU/PD

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
B16	UART0_CTSn	UART0_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI0_CS2	1	IO	1			7					
		ADC_EXT_TRIGGER0	2	I	0			7					
		UART2_RXD	3	I	1			7					
		TIMER_IO6	4	IO	0			7					
		SPI4_CLK	6	IO	0			7					
		GPIO1_54	7	IO	pad			7					
		EQEP0_S	8	IO	0			7					
CP_GEMAC_CPTS0_TS_SYNC	9	O		7									
A16	UART0_RTSn	UART0_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI0_CS3	1	IO	1			7					
		UART2_TXD	3	O				7					
		TIMER_IO7	4	IO	0			7					
		SPI4_D0	6	IO	0			7					
		GPIO1_55	7	IO	pad			7					
		EQEP0_I	8	IO	0			7					
D15	UART0_RXD	UART0_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_D0	2	IO	0			7					
		GPIO1_52	7	IO	pad			7					
		EQEP0_A	8	I	0			7					
C16	UART0_TXD	UART0_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_D1	2	IO	0			7					
		GPIO1_53	7	IO	pad			7					
		EQEP0_B	8	I	0			7					

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
D16	UART1_CTSn	UART1_CTSn	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI1_CS2	1	IO	1			7					
		ADC_EXT_TRIGGER1	2	I	0			7					
		PCIE0_CLKREQn	3	IO	0			7					
		UART3_RXD	4	I	1			7					
		CP_GEMAC_CPTS0_TS_SYNC	5	O				7					
		SPI4_D1	6	IO	0			7					
		GPIO1_58	7	IO	pad			7					
EQEP1_S	8	IO	0			7							
E16	UART1_RTSn	UART1_RTSn	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI1_CS3	1	IO	1			7					
		UART3_TXD	4	O				7					
		CP_GEMAC_CPTS0_HW2TSPUSH	5	I	0			7					
		SPI4_CS0	6	IO	1			7					
		GPIO1_59	7	IO	pad			7					
		EQEP1_I	8	IO	0			7					
E15	UART1_RXD	UART1_RXD	0	I	1	Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CS0	2	IO	1			7					
		CP_GEMAC_CPTS0_TS_COMP	5	O				7					
		GPIO1_56	7	IO	pad			7					
		EQEP1_A	8	I	0			7					

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
E14	UART1_TXD	UART1_TXD	0	O		Off / Off / Off	Off / Off / Off	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		SPI2_CLK	2	IO	0			7					
		CP_GEMAC_CPTS0_HW1TSPUSH	5	I	0			7					
		GPIO1_57	7	IO	pad			7					
		EQEP1_B	8	I	0			7					
AA20	USB0_DM	USB0_DM		IO					1.8 V/3.3 V	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0		USB2PHY	
AA19	USB0_DP	USB0_DP		IO					1.8 V/3.3 V	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0		USB2PHY	
E19	USB0_DRVVBUS	USB0_DRVVBUS	0	O		Off / Off / Down	Off / Off / Down	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD
		GPIO1_79	7	IO	pad			7					
U16	USB0_ID	USB0_ID		A					1.8 V/3.3 V	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0		USB2PHY	
U17	USB0_RCALIB	USB0_RCALIB		IO					1.8 V/3.3 V	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0		USB2PHY	
T14	USB0_VBUS	USB0_VBUS		A					1.8 V/3.3 V	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0		USB2PHY	
P12, P13	VDDA_0P85_SERDES0	VDDA_0P85_SERDES0		PWR									
P11	VDDA_0P85_SERDES0_C	VDDA_0P85_SERDES0_C		PWR									
T12	VDDA_0P85_USB0	VDDA_0P85_USB0		PWR									
R14	VDDA_1P8_SERDES0	VDDA_1P8_SERDES0		PWR									
R15	VDDA_1P8_USB0	VDDA_1P8_USB0		PWR									

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
H15	VDDA_3P3_SDIO	VDDA_3P3_SDIO		PWR									
R13	VDDA_3P3_USB0	VDDA_3P3_USB0		PWR									
J13	VDDA_ADC	VDDA_ADC		PWR									
K12	VDDA_MCU	VDDA_MCU		PWR									
N12	VDDA_PLL0	VDDA_PLL0		PWR									
H9	VDDA_PLL1	VDDA_PLL1		PWR									
J11	VDDA_PLL2	VDDA_PLL2		PWR									
G11	VDDA_TEMP0	VDDA_TEMP0		PWR									
L11	VDDA_TEMP1	VDDA_TEMP1		PWR									
L10, M13	VDDR_CORE	VDDR_CORE		PWR									
F11, G12, G14	VDDSHV0	VDDSHV0		PWR									
M7, N6, P7	VDDSHV1	VDDSHV1		PWR									
R10, R8, T9	VDDSHV2	VDDSHV2		PWR									
P14, P15	VDDSHV3	VDDSHV3		PWR									
M14, M15	VDDSHV4	VDDSHV4		PWR									
L14, L15	VDDSHV5	VDDSHV5		PWR									
F9, G10, G8	VDDSHV_MCU	VDDSHV_MCU		PWR									
F7, G6, H7, J6, K7, L6	VDDS_DDR	VDDS_DDR		PWR									
J8	VDDS_DDR_C	VDDS_DDR_C		PWR									
J15, K14	VDDS_MMC0	VDDS_MMC0		PWR									
H13	VDDS_OSC	VDDS_OSC		PWR									

**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
J10, J12, K11, K9, L12, L8, M11, M9, N10, N8, P9	VDD_CORE	VDD_CORE		PWR									
H14	VDD_DLL_MMC0	VDD_DLL_MMC0		PWR									
K13	VDD_MMC0	VDD_MMC0		PWR									
K16	VMON_1P8_MCU	VMON_1P8_MCU		PWR									
E12	VMON_1P8_SOC	VMON_1P8_SOC		PWR									
F13	VMON_3P3_MCU	VMON_3P3_MCU		PWR									
F14	VMON_3P3_SOC	VMON_3P3_SOC		PWR									
K10	VMON_VSYS	VMON_VSYS		PWR									
G15	VPP	VPP		PWR									

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
A1, A21, A5, A6, AA1, AA15, AA18, AA21, C10, C15, C3, D1, E11, E13, F10, F15, F8, G1, G16, G3, G7, G9, H11, H20, H21, H6, H8, J14, J16, J7, J9, K6, K8, L1, L16, L3, L7, L9, M10, M12, M6, M8, N11, N13, N15, N7, N9, P1, P10, P18, P6, P8, R12, R7, R9, T10, T11, T15, T16, T8, U3, V17, W10, W18,	VSS	VSS		PWR									

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**Table 6-1. Pin Attributes (ALV Package) (continued)**

BALL NUMBER	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	DSIS	BALL STATE DURING RESET RX/TX/PULL	BALL STATE AFTER RESET RX/TX/PULL	MUX MODE AFTER RESET	I/O VOLTAGE VALUE	POWER	HYS	BUFFER TYPE	PULL UP/DOWN TYPE
Y14, Y17, Y19													

## 6.3 Pin Attributes (ALX Package)

**Table 6-2. Pin Attributes (ALX Package)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/ DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
H21	ADC0_AIN0	ADC0_AIN0	0	A	1.8 V	ADC12B	VDDA_ADC0	Yes	-	PADCONFIG_172	0x000F42B0	-	-	0
		GPIO1_80	7	I										
F19	ADC0_AIN1	ADC0_AIN1	0	A	1.8 V	ADC12B	VDDA_ADC0	Yes	-	PADCONFIG_173	0x000F42B4	-	-	0
		GPIO1_81	7	I										
F21	ADC0_AIN2	ADC0_AIN2	0	A	1.8 V	ADC12B	VDDA_ADC0	Yes	-	PADCONFIG_174	0x000F42B8	-	-	0
		GPIO1_82	7	I										
F20	ADC0_AIN3	ADC0_AIN3	0	A	1.8 V	ADC12B	VDDA_ADC0	Yes	-	PADCONFIG_175	0x000F42BC	-	-	0
		GPIO1_83	7	I										
H20	ADC0_AIN4	ADC0_AIN4	0	A	1.8 V	ADC12B	VDDA_ADC0	Yes	-	PADCONFIG_176	0x000F42C0	-	-	0
		GPIO1_84	7	I										
E21	ADC0_AIN5	ADC0_AIN5	0	A	1.8 V	ADC12B	VDDA_ADC0	Yes	-	PADCONFIG_177	0x000F42C4	-	-	0
		GPIO1_85	7	I										
G20	ADC0_AIN6	ADC0_AIN6	0	A	1.8 V	ADC12B	VDDA_ADC0	Yes	-	PADCONFIG_178	0x000F42C8	-	-	0
		GPIO1_86	7	I										
E20	ADC0_AIN7	ADC0_AIN7	0	A	1.8 V	ADC12B	VDDA_ADC0	Yes	-	PADCONFIG_179	0x000F42CC	-	-	0
		GPIO1_87	7	I										
D12	CAP_VDDS0	CAP_VDDS0	-	CAP	-	-	-	-	-	-	-	-	-	-
N5	CAP_VDDS1	CAP_VDDS1	-	CAP	-	-	-	-	-	-	-	-	-	-
U9	CAP_VDDS2	CAP_VDDS2	-	CAP	-	-	-	-	-	-	-	-	-	-
R16	CAP_VDDS3	CAP_VDDS3	-	CAP	-	-	-	-	-	-	-	-	-	-
N18	CAP_VDDS4	CAP_VDDS4	-	CAP	-	-	-	-	-	-	-	-	-	-
M18	CAP_VDDS5	CAP_VDDS5	-	CAP	-	-	-	-	-	-	-	-	-	-
J17	CAP_VDDSHV_MMC1	CAP_VDDSHV_MMC1	-	CAP	-	-	-	-	-	-	-	-	-	-
D9	CAP_VDDS_MCU	CAP_VDDS_MCU	-	CAP	-	POR_POK	-	-	-	-	-	-	-	-

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
C5	EMU0	EMU0	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_31	0x0408407C	On / Off / Up	On / Off / Up	0
B3	EMU1	EMU1	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_32	0x04084080	On / Off / Up	On / Off / Up	0
		MCU_OBSCLK0	15	O										
A18	EXT_REFCLK1	EXT_REFCLK1	0	I	1.8 V/3.3 V	LVC MOS	VDDSHV0	Yes	PU/PD	PADCONFIG_157	0x000F4274	Off / Off / Off	Off / Off / Off	7
		SYNC1_OUT	1	O										
		SPI2_CS3	2	IO										
		CLKOUT0	5	O										
		GPIO1_69	7	IO										
R21	GPMC0_AD0	GPMC0_AD0	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV3	Yes	PU/PD	PADCONFIG_15	0x000F403C	On / Off / Off	On / Off / Off	7
		FSI_RX2_CLK	1	I										
		UART2_RXD	2	I										
		EHRPWM0_SYNCI	3	I										
		TRC_CLK	6	O										
		GPIO0_15	7	IO										
		BOOTMODE00	Bootstrap	I										
R20	GPMC0_AD1	GPMC0_AD1	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV3	Yes	PU/PD	PADCONFIG_16	0x000F4040	On / Off / Off	On / Off / Off	7
		FSI_RX2_D0	1	I										
		UART2_TXD	2	O										
		EHRPWM0_SYNCO	3	O										
		TRC_CTL	6	O										
		GPIO0_16	7	IO										
		PRG0_PWM2_TZ_OUT	9	O										
		BOOTMODE01	Bootstrap	I										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
T19	GPMC0_AD2	GPMC0_AD2	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_17	0x000F4044	On / Off / Off	On / Off / Off	7
		FSI_RX2_D1	1	I										
		UART2_RTSn	2	O										
		EHRPWM_TZn_IN0	3	I										
		TRC_DATA0	6	O										
		GPIO0_17	7	IO										
		PRG0_PWM2_TZ_IN	9	I										
		BOOTMODE02	Bootstrap	I										
V21	GPMC0_AD3	GPMC0_AD3	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_18	0x000F4048	On / Off / Off	On / Off / Off	7
		FSI_RX3_CLK	1	I										
		UART3_RXD	2	I										
		EHRPWM0_A	3	IO										
		TRC_DATA1	6	O										
		GPIO0_18	7	IO										
		PRG0_PWM2_A0	9	IO										
		BOOTMODE03	Bootstrap	I										
U21	GPMC0_AD4	GPMC0_AD4	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_19	0x000F404C	On / Off / Off	On / Off / Off	7
		FSI_RX3_D0	1	I										
		UART3_TXD	2	O										
		EHRPWM0_B	3	IO										
		TRC_DATA2	6	O										
		GPIO0_82	7	IO										
		PRG0_PWM2_B0	9	IO										
		BOOTMODE04	Bootstrap	I										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
T20	GPMC0_AD5	GPMC0_AD5	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_20	0x000F4050	On / Off / Off	On / Off / Off	7
		FSI_RX3_D1	1	I										
		UART3_RTSn	2	O										
		EHRPWM1_A	3	IO										
		TRC_DATA3	6	O										
		GPIO0_83	7	IO										
		PRG0_PWM2_A1	9	IO										
BOOTMODE05	Bootstrap	I												
T18	GPMC0_AD6	GPMC0_AD6	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_21	0x000F4054	On / Off / Off	On / Off / Off	7
		FSI_RX4_D0	1	I										
		UART4_RXD	2	I										
		EHRPWM1_B	3	IO										
		TRC_DATA4	6	O										
		GPIO0_21	7	IO										
		PRG0_PWM2_B1	9	IO										
BOOTMODE06	Bootstrap	I												
U19	GPMC0_AD7	GPMC0_AD7	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_22	0x000F4058	On / Off / Off	On / Off / Off	7
		FSI_RX4_D1	1	I										
		UART4_TXD	2	O										
		EHRPWM_TZn_IN1	3	I										
		EHRPWM8_A	4	IO										
		TRC_DATA5	6	O										
		GPIO0_22	7	IO										
PRG1_PWM2_A2	9	IO												
BOOTMODE07	Bootstrap	I												

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
U18	GPMC0_AD8	GPMC0_AD8	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_23	0x000F405C	On / Off / Off	On / Off / Off	7
		FSI_RX0_CLK	1	I										
		UART2_CTSn	2	I										
		EHRPWM2_A	3	IO										
		TRC_DATA6	6	O										
		GPIO0_23	7	IO										
		PRG0_PWM2_A2	9	IO										
		BOOTMODE08	Bootstrap	I										
U20	GPMC0_AD9	GPMC0_AD9	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_24	0x000F4060	On / Off / Off	On / Off / Off	7
		FSI_RX0_D0	1	I										
		UART3_CTSn	2	I										
		EHRPWM2_B	3	IO										
		TRC_DATA7	6	O										
		GPIO0_24	7	IO										
		PRG0_PWM2_B2	9	IO										
		BOOTMODE09	Bootstrap	I										
V20	GPMC0_AD10	GPMC0_AD10	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_25	0x000F4064	On / Off / Off	On / Off / Off	7
		FSI_RX0_D1	1	I										
		UART4_CTSn	2	I										
		EHRPWM_TZn_IN2	3	I										
		EHRPWM8_B	4	IO										
		TRC_DATA8	6	O										
		GPIO0_25	7	IO										
		PRG1_PWM2_B2	9	IO										
		BOOTMODE10	Bootstrap	I										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
W20	GPMC0_AD11	GPMC0_AD11	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_26	0x000F4068	On / Off / Off	On / Off / Off	7
		FSI_RX1_CLK	1	I										
		UART5_CTSn	2	I										
		EQEP1_A	3	I										
		TRC_DATA9	6	O										
		GPI00_26	7	IO										
		EHRPWM7_A	8	IO										
BOOTMODE11	Bootstrap	I												
Y20	GPMC0_AD12	GPMC0_AD12	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_27	0x000F406C	On / Off / Off	On / Off / Off	7
		FSI_RX1_D0	1	I										
		UART6_CTSn	2	I										
		EQEP1_B	3	I										
		TRC_DATA10	6	O										
		GPI00_27	7	IO										
		EHRPWM7_B	8	IO										
BOOTMODE12	Bootstrap	I												
Y19	GPMC0_AD13	GPMC0_AD13	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_28	0x000F4070	On / Off / Off	On / Off / Off	7
		FSI_RX1_D1	1	I										
		EHRPWM3_A	3	IO										
		TRC_DATA11	6	O										
		GPI00_28	7	IO										
		PRG0_PWM3_A0	9	IO										
		BOOTMODE13	Bootstrap	I										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
Y18	GPMC0_AD14	GPMC0_AD14	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_29	0x000F4074	On / Off / Off	On / Off / Off	7
		FSI_TX0_D0	1	O										
		UART6_RXD	2	I										
		EHRPWM3_B	3	IO										
		TRC_DATA12	6	O										
		GPIO0_29	7	IO										
		PRG0_PWM3_B0	9	IO										
		BOOTMODE14	Bootstrap	I										
AA19	GPMC0_AD15	GPMC0_AD15	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV3	Yes	PU/PD	PADCONFIG_30	0x000F4078	On / Off / Off	On / Off / Off	7
		FSI_TX0_D1	1	O										
		UART6_TXD	2	O										
		EHRPWM3_SYNCI	3	I										
		TRC_DATA13	6	O										
		GPIO0_30	7	IO										
		BOOTMODE15	Bootstrap	I										
		P21	GPMC0_BE1n	GPMC0_BE1n										
FSI_TX0_CLK	1			O										
EHRPWM5_A	3			IO										
TRC_DATA19	6			O										
GPIO0_36	7			IO										
PRG0_PWM3_A2	9			IO										
B16	I2C0_SCL			I2C0_SCL	0	IOD	1.8 V/3.3 V	I2C OD FS	VDDSHV0	Yes	-	PADCONFIG_152	0x000F4260	Off / Off / Off
		UART6_CTSn	4	I										
		GPIO1_64	7	IO										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
B15	I2C0_SDA	I2C0_SDA	0	IOD	1.8 V/3.3 V	I2C OD FS	VDDSHV0	Yes	-	PADCONFIG_153	0x000F4264	Off / Off / Off	On / SS / Off	0
		UART6_RTSn	4	O										
		GPIO1_65	7	IO										
A17	I2C1_SCL	I2C1_SCL	0	IOD	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_154	0x000F4268	Off / Off / Off	Off / Off / Off	7
		CPTS0_HW1TSPUSH	1	I										
		TIMER_IO0	2	IO										
		SPI2_CS1	3	IO										
		GPIO1_66	7	IO										
B18	I2C1_SDA	I2C1_SDA	0	IOD	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_155	0x000F426C	Off / Off / Off	Off / Off / Off	7
		CPTS0_HW2TSPUSH	1	I										
		TIMER_IO1	2	IO										
		SPI2_CS2	3	IO										
		GPIO1_67	7	IO										
A14	MCAN0_RX	MCAN0_RX	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_149	0x000F4254	Off / Off / Off	Off / Off / Off	7
		UART4_TXD	1	O										
		TIMER_IO3	2	IO										
		SYNC3_OUT	3	O										
		SPI4_CS2	6	IO										
		GPIO1_61	7	IO										
		EQEP2_S	8	IO										
		UART0_RIn	9	I										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
B13	MCAN0_TX	MCAN0_TX	0	O	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_148	0x000F4250	Off / Off / Off	Off / Off / Off	7
		UART4_RXD	1	I										
		TIMER_IO2	2	IO										
		SYNC2_OUT	3	O										
		SPI4_CS1	6	IO										
		GPIO1_60	7	IO										
		EQEP2_I	8	IO										
		UART0_DTRn	9	O										
A15	MCAN1_RX	MCAN1_RX	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_151	0x000F425C	Off / Off / Off	Off / Off / Off	7
		I2C3_SDA	1	IOD										
		ECAP2_IN_APWM_OUT	2	IO										
		OBSCCLK0	3	O										
		TIMER_IO5	4	IO										
		UART5_TXD	5	O										
		EHRPWM_SOCA	6	O										
		GPIO1_63	7	IO										
		EQEP2_B	8	I										
		UART0_DSRn	9	I										
		OBSCCLK0	15	O										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
B14	MCAN1_TX	MCAN1_TX	0	O	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_150	0x000F4258	Off / Off / Off	Off / Off / Off	7
		I2C3_SCL	1	IOD										
		ECAP1_IN_APWM_OUT	2	IO										
		SYCLKOUT0	3	O										
		TIMER_IO4	4	IO										
		UART5_RXD	5	I										
		EHRPWM_SOCA	6	O										
		GPIO1_62	7	IO										
		EQEP2_A	8	I										
UART0_DCDn	9	I												
D20	MCU_OSC0_XI	MCU_OSC0_XI	-	I	1.8 V	HFOSC	VDDS_OSC	-	-	-	-	-	-	-
C21	MCU_OSC0_XO	MCU_OSC0_XO	-	O	1.8 V	HFOSC	VDDS_OSC	-	-	-	-	-	-	-
C20	MCU_PORz	MCU_PORz	0	I	1.8 V	FS RESET	VDDS_OSC	Yes	-	MCU_PADCONFIG_23	0x0408405C	-	-	-
A6	MCU_RESETSTATz	MCU_RESETSTATz	0	O	1.8 V/3.3 V	LVCMOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_24	0x04084060	Off / Low / Off	Off / SS / Off	0
		MCU_GPIO0_22	7	IO										
A5	MCU_RESETz	MCU_RESETz	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_22	0x04084058	On / Off / Up	On / Off / Up	0
B20	MCU_SAFETY_ERRORn	MCU_SAFETY_ERRORn	0	IO	1.8 V	LVCMOS	VDDS_OSC	Yes	PU/PD	MCU_PADCONFIG_25	0x04084064	Off / Off / Down	On / SS / Down	0
D4	MCU_UART0_CTSn	MCU_UART0_CTSn	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_12	0x04084030	Off / Off / Off	Off / Off / Off	7
		MCU_TIMER_IO0	1	IO										
		MCU_SPI0_CS2	2	IO										
		MCU_GPIO0_1	7	IO										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
C2	MCU_UART0_RTSn	MCU_UART0_RTSn	0	O	1.8 V/3.3 V	LVC MOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_1 3	0x04084034	Off / Off / Off	Off / Off / Off	7
		MCU_TIMER_IO1	1	IO										
		MCU_SPI1_CS2	2	IO										
		MCU_GPIO0_0	7	IO										
D6	MCU_UART0_RXD	MCU_UART0_RXD	0	I	1.8 V/3.3 V	LVC MOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_1 0	0x04084028	Off / Off / Off	Off / Off / Off	7
		MCU_GPIO0_3	7	IO										
B2	MCU_UART0_TXD	MCU_UART0_TXD	0	O	1.8 V/3.3 V	LVC MOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_1 1	0x0408402C	Off / Off / Off	Off / Off / Off	7
		MCU_GPIO0_2	7	IO										
J20	MMC1_CLK	MMC1_CLK	0	IO	1.8 V/3.3 V	SDIO	VDDSHV5	Yes	PU/PD	PADCONFIG_163	0x000F428C	Off / Off / Off	Off / Off / Off	7
		UART2_CTSn	1	I										
		TIMER_IO4	2	IO										
		UART4_RXD	3	I										
		GPIO1_75	7	IO										
J21	MMC1_CMD	MMC1_CMD	0	IO	1.8 V/3.3 V	SDIO	VDDSHV5	Yes	PU/PD	PADCONFIG_165	0x000F4294	Off / Off / Off	Off / Off / Off	7
		UART2_RTSn	1	O										
		TIMER_IO5	2	IO										
		UART4_TXD	3	O										
		GPIO1_76	7	IO										
B17	MMC1_SDCD	MMC1_SDCD	0	I	1.8 V/3.3 V	LVC MOS	VDDSHV0	Yes	PU/PD	PADCONFIG_166	0x000F4298	Off / Off / Off	Off / Off / Off	7
		UART3_CTSn	1	I										
		TIMER_IO6	2	IO										
		UART5_RXD	3	I										
		GPIO1_77	7	IO										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
C16	MMC1_SDWP	MMC1_SDWP	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_167	0x000F429C	Off / Off / Off	Off / Off / Off	7
		UART3_RTSn	1	O										
		TIMER_IO7	2	IO										
		UART5_TXD	3	O										
		GPIO1_78	7	IO										
J18	MMC1_DAT0	MMC1_DAT0	0	IO	1.8 V/3.3 V	SDIO	VDDSHV5	Yes	PU/PD	PADCONFIG_162	0x000F4288	Off / Off / Off	Off / Off / Off	7
		CP_GEMAC_CPTS0_HW2TSPUSH	1	I										
		TIMER_IO3	2	IO										
		UART3_TXD	3	O										
		GPIO1_74	7	IO										
J19	MMC1_DAT1	MMC1_DAT1	0	IO	1.8 V/3.3 V	SDIO	VDDSHV5	Yes	PU/PD	PADCONFIG_161	0x000F4284	Off / Off / Off	Off / Off / Off	7
		CP_GEMAC_CPTS0_HW1TSPUSH	1	I										
		TIMER_IO2	2	IO										
		UART3_RXD	3	I										
		GPIO1_73	7	IO										
K20	MMC1_DAT2	MMC1_DAT2	0	IO	1.8 V/3.3 V	SDIO	VDDSHV5	Yes	PU/PD	PADCONFIG_160	0x000F4280	Off / Off / Off	Off / Off / Off	7
		CP_GEMAC_CPTS0_TS_SYNC	1	O										
		TIMER_IO1	2	IO										
		UART2_TXD	3	O										
		GPIO1_72	7	IO										
K18	MMC1_DAT3	MMC1_DAT3	0	IO	1.8 V/3.3 V	SDIO	VDDSHV5	Yes	PU/PD	PADCONFIG_159	0x000F427C	Off / Off / Off	Off / Off / Off	7
		CP_GEMAC_CPTS0_TS_COMP	1	O										
		TIMER_IO0	2	IO										
		UART2_RXD	3	I										
		GPIO1_71	7	IO										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
P20	OSPI0_CLK	OSPI0_CLK	0	O	1.8 V/3.3 V	LVCMOS	VDDSHV4	Yes	PU/PD	PADCONFIG_0	0x000F4000	Off / Off / Off	Off / Off / Off	7
		GPIO0_0	7	IO										
P17	OSPI0_DQS	OSPI0_DQS	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV4	Yes	PU/PD	PADCONFIG_2	0x000F4008	Off / Off / Off	Off / Off / Off	7
		GPIO0_2	7	IO										
M21	OSPI0_LBCLKO	OSPI0_LBCLKO	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV4	Yes	PU/PD	PADCONFIG_1	0x000F4004	Off / Off / Off	On / Off / Off	7
		GPIO0_1	7	IO										
L20	OSPI0_CSn0	OSPI0_CSn0	0	O	1.8 V/3.3 V	LVCMOS	VDDSHV4	Yes	PU/PD	PADCONFIG_11	0x000F402C	Off / Off / Off	Off / Off / Off	7
		GPIO0_11	7	IO										
M20	OSPI0_CSn1	OSPI0_CSn1	0	O	1.8 V/3.3 V	LVCMOS	VDDSHV4	Yes	PU/PD	PADCONFIG_12	0x000F4030	Off / Off / Off	Off / Off / Off	7
		GPIO0_12	7	IO										
L19	OSPI0_D0	OSPI0_D0	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV4	Yes	PU/PD	PADCONFIG_3	0x000F400C	Off / Off / Off	Off / Off / Off	7
		GPIO0_3	7	IO										
N20	OSPI0_D1	OSPI0_D1	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV4	Yes	PU/PD	PADCONFIG_4	0x000F4010	Off / Off / Off	Off / Off / Off	7
		GPIO0_4	7	IO										
L21	OSPI0_D2	OSPI0_D2	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV4	Yes	PU/PD	PADCONFIG_5	0x000F4014	Off / Off / Off	Off / Off / Off	7
		GPIO0_5	7	IO										
N19	OSPI0_D3	OSPI0_D3	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV4	Yes	PU/PD	PADCONFIG_6	0x000F4018	Off / Off / Off	Off / Off / Off	7
		GPIO0_6	7	IO										
D18	PORz_OUT	PORz_OUT	0	O	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_171	0x000F42AC	Off / Low / Off	Off / SS / Off	0
D2	PRG0_MDIO0_MDC	PRG0_MDIO0_MDC	0	O	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_129	0x000F4204	Off / Off / Off	Off / Off / Off	7
		GPIO1_41	7	IO										
		GPMC0_A13	9	OZ										
E4	PRG0_MDIO0_MDIO	PRG0_MDIO0_MDIO	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_128	0x000F4200	Off / Off / Off	Off / Off / Off	7
		GPIO1_40	7	IO										
		GPMC0_A12	9	OZ										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
J3	PRG0_PRU0_GPO0	PRG0_PRU0_GPO0	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_88	0x000F4160	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI0	1	I										
		PRG0_RGMII1_RD0	2	I										
		PRG0_PWM3_A0	3	IO										
		GPIO1_0	7	IO										
		UART2_CTSn	10	I										
J4	PRG0_PRU0_GPO1	PRG0_PRU0_GPO1	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_89	0x000F4164	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI1	1	I										
		PRG0_RGMII1_RD1	2	I										
		PRG0_PWM3_B0	3	IO										
		GPIO1_1	7	IO										
		UART2_TXD	10	O										
G1	PRG0_PRU0_GPO2	PRG0_PRU0_GPO2	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_90	0x000F4168	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI2	1	I										
		PRG0_RGMII1_RD2	2	I										
		PRG0_PWM2_A0	3	IO										
		GPIO1_2	7	IO										
		GPMC0_A0	9	OZ										
		UART2_RTSn	10	O										
H1	PRG0_PRU0_GPO3	PRG0_PRU0_GPO3	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_91	0x000F416C	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI3	1	I										
		PRG0_RGMII1_RD3	2	I										
		PRG0_PWM3_A2	3	IO										
		GPIO1_3	7	IO										
		UART3_CTSn	10	I										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
K2	PRG0_PRU0_GPO4	PRG0_PRU0_GPO4	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_92	0x000F4170	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI4	1	I										
		PRG0_RGMII1_RX_CTL	2	I										
		PRG0_PWM2_B0	3	IO										
		GPIO1_4	7	IO										
		GPMC0_A1	9	OZ										
		UART3_TXD	10	O										
F2	PRG0_PRU0_GPO5	PRG0_PRU0_GPO5	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_93	0x000F4174	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI5	1	I										
		PRG0_PWM3_B2	3	IO										
		GPIO1_5	7	IO										
		UART3_RTSn	10	O										
H2	PRG0_PRU0_GPO6	PRG0_PRU0_GPO6	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_94	0x000F4178	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI6	1	I										
		PRG0_RGMII1_RXC	2	I										
		PRG0_PWM3_A1	3	IO										
		GPIO1_6	7	IO										
		UART4_CTSn	10	I										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
E2	PRG0_PRU0_GPO7	PRG0_PRU0_GPO7	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_95	0x000F417C	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI7	1	I										
		PRG0_IEP0_EDC_LATCH_IN1	2	I										
		PRG0_PWM3_B1	3	IO										
		CPTS0_HW2TSPUSH	4	I										
		CP_GEMAC_CPTS0_HW2TSPUSH	5	I										
		TIMER_IO6	6	IO										
		GPIO1_7	7	IO										
UART4_TXD	10	O												
H5	PRG0_PRU0_GPO8	PRG0_PRU0_GPO8	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_96	0x000F4180	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI8	1	I										
		PRG0_PWM2_A1	3	IO										
		GPIO1_8	7	IO										
		GPMC0_A2	9	OZ										
		UART4_RTSn	10	O										
Y3	PRG0_PRU0_GPO9	PRG0_PRU0_GPO9	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_97	0x000F4184	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI9	1	I										
		PRG0_UART0_CTSn	2	I										
		PRG0_PWM3_TZ_IN	3	I										
		RGMI1_RX_CTL	4	I										
		RMII1_RX_ER	5	I										
		PRG0_IEP0_EDIO_DATA_IN_OUT28	6	IO										
		GPIO1_9	7	IO										
		UART2_RXD	10	I										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
U1	PRG0_PRU0_GPO10	PRG0_PRU0_GPO10	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_98	0x000F4188	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI10	1	I										
		PRG0_UART0_RTSn	2	O										
		PRG0_PWM2_B1	3	IO										
		RGMII1_RXC	4	I										
		RMII_REF_CLK	5	I										
		PRG0_IEP0_EDIO_DATA_IN_OUT29	6	IO										
		GPIO1_10	7	IO										
UART3_RXD	10	I												
L1	PRG0_PRU0_GPO11	PRG0_PRU0_GPO11	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_99	0x000F418C	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI11	1	I										
		PRG0_RGMII1_TD0	2	O										
		PRG0_PWM3_TZ_OUT	3	O										
		GPIO1_11	7	IO										
		UART4_RXD	10	I										
K1	PRG0_PRU0_GPO12	PRG0_PRU0_GPO12	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_100	0x000F4190	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI12	1	I										
		PRG0_RGMII1_TD1	2	O										
		PRG0_PWM0_A0	3	IO										
		GPIO1_12	7	IO										
		GPMC0_A14	9	OZ										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
N1	PRG0_PRU0_GPO13	PRG0_PRU0_GPO13	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_101	0x000F4194	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI13	1	I										
		PRG0_RGMII1_TD2	2	O										
		PRG0_PWM0_B0	3	IO										
		SPI3_D0	6	IO										
		GPIO1_13	7	IO										
		GPMC0_A15	9	OZ										
N2	PRG0_PRU0_GPO14	PRG0_PRU0_GPO14	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_102	0x000F4198	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI14	1	I										
		PRG0_RGMII1_TD3	2	O										
		PRG0_PWM0_A1	3	IO										
		SPI3_D1	6	IO										
		GPIO1_14	7	IO										
		GPMC0_A3	9	OZ										
N4	PRG0_PRU0_GPO15	PRG0_PRU0_GPO15	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_103	0x000F419C	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI15	1	I										
		PRG0_RGMII1_TX_CTL	2	O										
		PRG0_PWM0_B1	3	IO										
		SPI3_CS1	6	IO										
		GPIO1_15	7	IO										
		GPMC0_A16	9	OZ										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
N3	PRG0_PRU0_GPO16	PRG0_PRU0_GPO16	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_104	0x000F41A0	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI16	1	I										
		PRG0_RGMII1_TXC	2	IO										
		PRG0_PWM0_A2	3	IO										
		SPI3_CLK	6	IO										
		GPIO1_16	7	IO										
		GPMC0_A4	9	OZ										
E1	PRG0_PRU0_GPO17	PRG0_PRU0_GPO17	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_105	0x000F41A4	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI17	1	I										
		PRG0_IEP0_EDC_SYNC_OUT1	2	O										
		PRG0_PWM0_B2	3	IO										
		CPTS0_TS_SYNC	4	O										
		CP_GEMAC_CPTS0_TS_SYNC	5	O										
		SPI3_CS0	6	IO										
		GPIO1_17	7	IO										
		TIMER_IO11	8	IO										
		GPMC0_A17	9	OZ										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
K4	PRG0_PRU0_GPO18	PRG0_PRU0_GPO18	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_106	0x000F41A8	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI18	1	I										
		PRG0_IEP0_EDC_LATCH_IN0	2	I										
		PRG0_PWM0_TZ_IN	3	I										
		CPTS0_HW1TSPUSH	4	I										
		CP_GEMAC_CPTS0_HW1TSPUSH	5	I										
		EHRPWM8_A	6	IO										
		GPIO1_18	7	IO										
		UART4_CTSn	8	I										
		GPMC0_A5	9	OZ										
UART2_RXD	10	I												
G2	PRG0_PRU0_GPO19	PRG0_PRU0_GPO19	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_107	0x000F41AC	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU0_GPI19	1	I										
		PRG0_IEP0_EDC_SYNC_OUT0	2	O										
		PRG0_PWM0_TZ_OUT	3	O										
		CPTS0_TS_COMP	4	O										
		CP_GEMAC_CPTS0_TS_COMP	5	O										
		EHRPWM8_B	6	IO										
		GPIO1_19	7	IO										
		UART4_RTSn	8	O										
		GPMC0_A6	9	OZ										
UART3_RXD	10	I												

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
L5	PRG0_PRU1_GPO0	PRG0_PRU1_GPO0	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_108	0x000F41B0	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI0	1	I										
		PRG0_RGMII2_RD0	2	I										
		GPIO1_20	7	IO										
		EQEP0_A	8	I										
		UART5_CTSn	10	I										
J2	PRG0_PRU1_GPO1	PRG0_PRU1_GPO1	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_109	0x000F41B4	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI1	1	I										
		PRG0_RGMII2_RD1	2	I										
		GPIO1_21	7	IO										
		EQEP0_B	8	I										
		UART5_TXD	10	O										
M2	PRG0_PRU1_GPO2	PRG0_PRU1_GPO2	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_110	0x000F41B8	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI2	1	I										
		PRG0_RGMII2_RD2	2	I										
		PRG0_PWM2_A2	3	IO										
		GPIO1_22	7	IO										
		EQEP0_S	8	IO										
		UART5_RTSn	10	O										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
L2	PRG0_PRU1_GPO3	PRG0_PRU1_GPO3	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_111	0x000F41BC	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI3	1	I										
		PRG0_RGMII2_RD3	2	I										
		GPIO1_23	7	IO										
		EQEP1_A	8	I										
		GPMC0_A18	9	OZ										
		UART6_CTSn	10	I										
L3	PRG0_PRU1_GPO4	PRG0_PRU1_GPO4	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_112	0x000F41C0	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI4	1	I										
		PRG0_RGMII2_RX_CTL	2	I										
		PRG0_PWM2_B2	3	IO										
		GPIO1_24	7	IO										
		EQEP1_B	8	I										
		UART6_TXD	10	O										
E3	PRG0_PRU1_GPO5	PRG0_PRU1_GPO5	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_113	0x000F41C4	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI5	1	I										
		GPIO1_25	7	IO										
		EQEP1_S	8	IO										
		UART6_RTSn	10	O										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
F5	PRG0_PRU1_GPO6	PRG0_PRU1_GPO6	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_114	0x000F41C8	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI6	1	I										
		PRG0_RGMII2_RXC	2	I										
		GPIO1_26	7	IO										
		EQEP2_A	8	I										
		GPMC0_A19	9	OZ										
		UART4_CTSn	10	I										
T5	PRG0_PRU1_GPO7	PRG0_PRU1_GPO7	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_115	0x000F41CC	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI7	1	I										
		PRG0_IEP1_EDC_LATCH_IN1	2	I										
		RGMII1_RD0	4	I										
		RMII1_RXD0	5	I										
		GPIO1_27	7	IO										
		EQEP2_B	8	I										
		UART4_TXD	10	O										
F4	PRG0_PRU1_GPO8	PRG0_PRU1_GPO8	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_116	0x000F41D0	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI8	1	I										
		PRG0_PWM2_TZ_OUT	3	O										
		GPIO1_28	7	IO										
		EQEP2_S	8	IO										
		UART4_RTSn	10	O										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
R2	PRG0_PRU1_GPO9	PRG0_PRU1_GPO9	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_117	0x000F41D4	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI9	1	I										
		PRG0_UART0_RXD	2	I										
		RGMII1_RD1	4	I										
		RMII1_RXD1	5	I										
		PRG0_IEP0_EDIO_DATA_IN_OUT30	6	IO										
		GPIO1_29	7	IO										
		EQEP0_I	8	IO										
		UART5_RXD	10	I										
U2	PRG0_PRU1_GPO10	PRG0_PRU1_GPO10	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_118	0x000F41D8	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI10	1	I										
		PRG0_UART0_TXD	2	O										
		PRG0_PWM2_TZ_IN	3	I										
		RGMII1_RD2	4	I										
		RMII1_TXD0	5	O										
		PRG0_IEP0_EDIO_DATA_IN_OUT31	6	IO										
		GPIO1_30	7	IO										
		EQEP1_I	8	IO										
		UART6_RXD	10	I										
P1	PRG0_PRU1_GPO11	PRG0_PRU1_GPO11	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_119	0x000F41DC	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI11	1	I										
		PRG0_RGMII2_TD0	2	O										
		GPIO1_31	7	IO										
		EQEP2_I	8	IO										
		UART4_RXD	10	I										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
P2	PRG0_PRU1_GPO12	PRG0_PRU1_GPO12	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_120	0x000F41E0	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI12	1	I										
		PRG0_RGMII2_TD1	2	O										
		PRG0_PWM1_A0	3	IO										
		GPI01_32	7	IO										
		EQEP2_B	8	I										
		GPMC0_A7	9	OZ										
		UART4_TXD	10	O										
T4	PRG0_PRU1_GPO13	PRG0_PRU1_GPO13	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_121	0x000F41E4	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI13	1	I										
		PRG0_RGMII2_TD2	2	O										
		PRG0_PWM1_B0	3	IO										
		GPI01_33	7	IO										
		EQEP0_I	8	IO										
		GPMC0_A8	9	OZ										
		UART5_RXD	10	I										
R5	PRG0_PRU1_GPO14	PRG0_PRU1_GPO14	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_122	0x000F41E8	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI14	1	I										
		PRG0_RGMII2_TD3	2	O										
		PRG0_PWM1_A1	3	IO										
		GPI01_34	7	IO										
		EQEP1_I	8	IO										
		GPMC0_A9	9	OZ										
		UART6_RXD	10	I										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
M4	PRG0_PRU1_GPO15	PRG0_PRU1_GPO15	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_123	0x000F41EC	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI15	1	I										
		PRG0_RGMII2_TX_CTL	2	O										
		PRG0_PWM1_B1	3	IO										
		GPIO1_35	7	IO										
		GPMC0_A10	9	OZ										
		PRG0_ECAP0_IN_APWM_OUT	10	IO										
T3	PRG0_PRU1_GPO16	PRG0_PRU1_GPO16	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_124	0x000F41F0	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI16	1	I										
		PRG0_RGMII2_TXC	2	IO										
		PRG0_PWM1_A2	3	IO										
		GPIO1_36	7	IO										
		GPMC0_A11	9	OZ										
		PRG0_ECAP0_SYNC_OUT	10	O										
T1	PRG0_PRU1_GPO17	PRG0_PRU1_GPO17	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV1	Yes	PU/PD	PADCONFIG_125	0x000F41F4	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI17	1	I										
		PRG0_IEP1_EDC_SYNC_OUT1	2	O										
		PRG0_PWM1_B2	3	IO										
		RGMII1_RD3	4	I										
		RMII1_TXD1	5	O										
		GPIO1_37	7	IO										
		PRG0_ECAP0_SYNC_OUT	8	O										
		PRG0_ECAP0_SYNC_IN	10	I										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
D1	PRG0_PRU1_GPO18	PRG0_PRU1_GPO18	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_126	0x000F41F8	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI18	1	I										
		PRG0_IEP1_EDC_LATCH_IN0	2	I										
		PRG0_PWM1_TZ_IN	3	I										
		MDIO0_MDIO	4	IO										
		RMII1_TX_EN	5	O										
		EHRPWM7_A	6	IO										
		GPIO1_38	7	IO										
		PRG0_ECAP0_SYNC_IN	8	I										
F3	PRG0_PRU1_GPO19	PRG0_PRU1_GPO19	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV1	Yes	PU/PD	PADCONFIG_127	0x000F41FC	Off / Off / Off	Off / Off / Off	7
		PRG0_PRU1_GPI19	1	I										
		PRG0_IEP1_EDC_SYNC_OUT0	2	O										
		PRG0_PWM1_TZ_OUT	3	O										
		MDIO0_MDC	4	O										
		RMII1_CRSDV	5	I										
		EHRPWM7_B	6	IO										
		GPIO1_39	7	IO										
		PRG0_ECAP0_IN_APWM_OUT	8	IO										
W1	PRG1_MDIO0_MDC	PRG1_MDIO0_MDC	0	O	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_87	0x000F415C	Off / Off / Off	Off / Off / Off	7
		MDIO0_MDC	4	O										
		GPIO0_86	7	IO										
V2	PRG1_MDIO0_MDIO	PRG1_MDIO0_MDIO	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_86	0x000F4158	Off / Off / Off	Off / Off / Off	7
		MDIO0_MDIO	4	IO										
		GPIO0_85	7	IO										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
V4	PRG1_PRU0_GPO0	PRG1_PRU0_GPO0	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV2	Yes	PU/PD	PADCONFIG_46	0x000F40B8	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI0	1	I										
		PRG1_RGMII1_RD0	2	I										
		PRG1_PWM3_A0	3	IO										
		GPI00_45	7	IO										
		GPMC0_AD16	8	IO										
W5	PRG1_PRU0_GPO1	PRG1_PRU0_GPO1	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV2	Yes	PU/PD	PADCONFIG_47	0x000F40BC	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI1	1	I										
		PRG1_RGMII1_RD1	2	I										
		PRG1_PWM3_B0	3	IO										
		GPI00_46	7	IO										
		GPMC0_AD17	8	IO										
AA4	PRG1_PRU0_GPO2	PRG1_PRU0_GPO2	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV2	Yes	PU/PD	PADCONFIG_48	0x000F40C0	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI2	1	I										
		PRG1_RGMII1_RD2	2	I										
		PRG1_PWM2_A0	3	IO										
		GPI00_47	7	IO										
		GPMC0_AD18	8	IO										
Y5	PRG1_PRU0_GPO3	PRG1_PRU0_GPO3	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV2	Yes	PU/PD	PADCONFIG_49	0x000F40C4	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI3	1	I										
		PRG1_RGMII1_RD3	2	I										
		PRG1_PWM3_A2	3	IO										
		GPI00_48	7	IO										
		GPMC0_AD19	8	IO										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
AA5	PRG1_PRU0_GPO4	PRG1_PRU0_GPO4	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV2	Yes	PU/PD	PADCONFIG_50	0x000F40C8	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI4	1	I										
		PRG1_RGMII1_RX_CTL	2	I										
		PRG1_PWM2_B0	3	IO										
		GPIO0_49	7	IO										
		GPMC0_AD20	8	IO										
U14	PRG1_PRU0_GPO5	PRG1_PRU0_GPO5	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV2	Yes	PU/PD	PADCONFIG_51	0x000F40CC	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI5	1	I										
		PRG1_PWM3_B2	3	IO										
		RGMII1_RX_CTL	4	I										
		GPIO0_50	7	IO										
		GPMC0_AD21	8	IO										
Y2	PRG1_PRU0_GPO6	PRG1_PRU0_GPO6	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV2	Yes	PU/PD	PADCONFIG_52	0x000F40D0	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI6	1	I										
		PRG1_RGMII1_RXC	2	I										
		PRG1_PWM3_A1	3	IO										
		GPIO0_51	7	IO										
		GPMC0_AD22	8	IO										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
V13	PRG1_PRU0_GPO7	PRG1_PRU0_GPO7	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_53	0x000F40D4	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI7	1	I										
		PRG1_IEP0_EDC_LATCH_IN1	2	I										
		PRG1_PWM3_B1	3	IO										
		CPTS0_HW2TSPUSH	4	I										
		CLKOUT0	5	O										
		TIMER_IO10	6	IO										
		GPI00_52	7	IO										
GPMC0_AD23	8	IO												
Y13	PRG1_PRU0_GPO8	PRG1_PRU0_GPO8	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_54	0x000F40D8	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI8	1	I										
		PRG1_PWM2_A1	3	IO										
		RGMI1_RXC	4	I										
		GPI00_53	7	IO										
		GPMC0_AD24	8	IO										
W16	PRG1_PRU0_GPO9	PRG1_PRU0_GPO9	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_55	0x000F40DC	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI9	1	I										
		PRG1_UART0_CTSn	2	I										
		PRG1_PWM3_TZ_IN	3	I										
		RGMI1_TX_CTL	4	O										
		RMII1_RX_ER	5	I										
		PRG1_IEP0_EDIO_DATA_IN_OUT28	6	IO										
		GPI00_54	7	IO										
GPMC0_AD25	8	IO												

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
W13	PRG1_PRU0_GPO10	PRG1_PRU0_GPO10	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_56	0x000F40E0	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI10	1	I										
		PRG1_UART0_RTSn	2	O										
		PRG1_PWM2_B1	3	IO										
		RGMII1_TXC	4	IO										
		RMII_REF_CLK	5	I										
		PRG1_IEP0_EDIO_DATA_IN_OUT29	6	IO										
		GPI00_55	7	IO										
GPMC0_AD26	8	IO												
V5	PRG1_PRU0_GPO11	PRG1_PRU0_GPO11	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_57	0x000F40E4	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI11	1	I										
		PRG1_RGMII1_TD0	2	O										
		PRG1_PWM3_TZ_OUT	3	O										
		GPI00_56	7	IO										
		GPMC0_AD27	8	IO										
W2	PRG1_PRU0_GPO12	PRG1_PRU0_GPO12	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_58	0x000F40E8	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI12	1	I										
		PRG1_RGMII1_TD1	2	O										
		PRG1_PWM0_A0	3	IO										
		GPI00_57	7	IO										
		GPMC0_AD28	8	IO										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
V6	PRG1_PRU0_GPO13	PRG1_PRU0_GPO13	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV2	Yes	PU/PD	PADCONFIG_59	0x000F40EC	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI13	1	I										
		PRG1_RGMII1_TD2	2	O										
		PRG1_PWM0_B0	3	IO										
		GPI00_58	7	IO										
		GPMC0_AD29	8	IO										
AA7	PRG1_PRU0_GPO14	PRG1_PRU0_GPO14	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV2	Yes	PU/PD	PADCONFIG_60	0x000F40F0	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI14	1	I										
		PRG1_RGMII1_TD3	2	O										
		PRG1_PWM0_A1	3	IO										
		GPI00_59	7	IO										
		GPMC0_AD30	8	IO										
Y7	PRG1_PRU0_GPO15	PRG1_PRU0_GPO15	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV2	Yes	PU/PD	PADCONFIG_61	0x000F40F4	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI15	1	I										
		PRG1_RGMII1_TX_CTL	2	O										
		PRG1_PWM0_B1	3	IO										
		GPI00_60	7	IO										
		GPMC0_AD31	8	IO										
W6	PRG1_PRU0_GPO16	PRG1_PRU0_GPO16	0	IO	1.8 V/3.3 V	LVC MOS	VDDSHV2	Yes	PU/PD	PADCONFIG_62	0x000F40F8	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI16	1	I										
		PRG1_RGMII1_TXC	2	IO										
		PRG1_PWM0_A2	3	IO										
		GPI00_61	7	IO										
		GPMC0_BE2n	8	O										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
T2	PRG1_PRU0_GPO17	PRG1_PRU0_GPO17	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_63	0x000F40FC	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI17	1	I										
		PRG1_IEP0_EDC_SYNC_OUT1	2	O										
		PRG1_PWM0_B2	3	IO										
		CPTS0_TS_SYNC	4	O										
		TIMER_IO7	6	IO										
		GPIO0_62	7	IO										
		GPMC0_A0	8	OZ										
Y4	PRG1_PRU0_GPO18	PRG1_PRU0_GPO18	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_64	0x000F4100	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI18	1	I										
		PRG1_IEP0_EDC_LATCH_IN0	2	I										
		PRG1_PWM0_TZ_IN	3	I										
		CPTS0_HW1TSPUSH	4	I										
		TIMER_IO8	6	IO										
		GPIO0_63	7	IO										
		GPMC0_A1	8	OZ										
U3	PRG1_PRU0_GPO19	PRG1_PRU0_GPO19	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_65	0x000F4104	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU0_GPI19	1	I										
		PRG1_IEP0_EDC_SYNC_OUT0	2	O										
		PRG1_PWM0_TZ_OUT	3	O										
		CPTS0_TS_COMP	4	O										
		TIMER_IO9	6	IO										
		GPIO0_64	7	IO										
		GPMC0_A2	8	OZ										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
AA10	PRG1_PRU1_GPO0	PRG1_PRU1_GPO0	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_66	0x000F4108	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI0	1	I										
		PRG1_RGMII2_RD0	2	I										
		RGMII2_RD0	4	I										
		RMII2_RXD0	5	I										
		GPI00_65	7	IO										
		GPMC0_A3	8	OZ										
Y10	PRG1_PRU1_GPO1	PRG1_PRU1_GPO1	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_67	0x000F410C	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI1	1	I										
		PRG1_RGMII2_RD1	2	I										
		RGMII2_RD1	4	I										
		RMII2_RXD1	5	I										
		GPI00_66	7	IO										
		GPMC0_A4	8	OZ										
Y11	PRG1_PRU1_GPO2	PRG1_PRU1_GPO2	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_68	0x000F4110	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI2	1	I										
		PRG1_RGMII2_RD2	2	I										
		PRG1_PWM2_A2	3	IO										
		RGMII2_RD2	4	I										
		GPI00_67	7	IO										
		GPMC0_A5	8	OZ										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
V12	PRG1_PRU1_GPO3	PRG1_PRU1_GPO3	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_69	0x000F4114	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI3	1	I										
		PRG1_RGMII2_RD3	2	I										
		RGMII2_RD3	4	I										
		GPI00_68	7	IO										
		GPMC0_A6	8	OZ										
Y12	PRG1_PRU1_GPO4	PRG1_PRU1_GPO4	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_70	0x000F4118	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI4	1	I										
		PRG1_RGMII2_RX_CTL	2	I										
		PRG1_PWM2_B2	3	IO										
		RGMII2_RX_CTL	4	I										
		RMII2_RX_ER	5	I										
		GPI00_69	7	IO										
		GPMC0_A7	8	OZ										
AA11	PRG1_PRU1_GPO5	PRG1_PRU1_GPO5	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_71	0x000F411C	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI5	1	I										
		RGMII1_RD0	4	I										
		GPI00_70	7	IO										
		GPMC0_A8	8	OZ										
V10	PRG1_PRU1_GPO6	PRG1_PRU1_GPO6	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_72	0x000F4120	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI6	1	I										
		PRG1_RGMII2_RXC	2	I										
		RGMII2_RXC	4	I										
		GPI00_71	7	IO										
		GPMC0_A9	8	OZ										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
Y14	PRG1_PRU1_GPO7	PRG1_PRU1_GPO7	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_73	0x000F4124	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI7	1	I										
		PRG1_IEP1_EDC_LATCH_IN1	2	I										
		RGMI1_TD0	4	O										
		RMII1_RXD0	5	I										
		SPI3_CS3	6	IO										
		GPIO0_72	7	IO										
		GPMC0_A10	8	OZ										
W11	PRG1_PRU1_GPO8	PRG1_PRU1_GPO8	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_74	0x000F4128	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI8	1	I										
		PRG1_PWM2_TZ_OUT	3	O										
		RGMI1_RD1	4	I										
		GPIO0_73	7	IO										
		GPMC0_A11	8	OZ										
Y16	PRG1_PRU1_GPO9	PRG1_PRU1_GPO9	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_75	0x000F412C	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI9	1	I										
		PRG1_UART0_RXD	2	I										
		RGMI1_TD1	4	O										
		RMII1_RXD1	5	I										
		PRG1_IEP0_EDIO_DATA_IN_OUT30	6	IO										
		GPIO0_74	7	IO										
		GPMC0_A12	8	OZ										

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**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
U13	PRG1_PRU1_GPO10	PRG1_PRU1_GPO10	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_76	0x000F4130	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI10	1	I										
		PRG1_UART0_TXD	2	O										
		PRG1_PWM2_TZ_IN	3	I										
		RGMII1_TD2	4	O										
		RMII1_TXD0	5	O										
		PRG1_IEP0_EDIO_DATA_IN_OUT31	6	IO										
		GPI00_75	7	IO										
GPMC0_A13	8	OZ												
Y6	PRG1_PRU1_GPO11	PRG1_PRU1_GPO11	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_77	0x000F4134	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI11	1	I										
		PRG1_RGMII2_TD0	2	O										
		RGMII2_TD0	4	O										
		RMII2_TXD0	5	O										
		GPI00_76	7	IO										
		GPMC0_A14	8	OZ										
AA8	PRG1_PRU1_GPO12	PRG1_PRU1_GPO12	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_78	0x000F4138	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI12	1	I										
		PRG1_RGMII2_TD1	2	O										
		PRG1_PWM1_A0	3	IO										
		RGMII2_TD1	4	O										
		RMII2_TXD1	5	O										
		GPI00_77	7	IO										
		GPMC0_A15	8	OZ										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
Y9	PRG1_PRU1_GPO13	PRG1_PRU1_GPO13	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_79	0x000F413C	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI13	1	I										
		PRG1_RGMII2_TD2	2	O										
		PRG1_PWM1_B0	3	IO										
		RGMII2_TD2	4	O										
		RMII2_CRS_DV	5	I										
		GPI00_78	7	IO										
		GPMC0_A16	8	OZ										
W9	PRG1_PRU1_GPO14	PRG1_PRU1_GPO14	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_80	0x000F4140	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI14	1	I										
		PRG1_RGMII2_TD3	2	O										
		PRG1_PWM1_A1	3	IO										
		RGMII2_TD3	4	O										
		GPI00_79	7	IO										
		GPMC0_A17	8	OZ										
		V9	PRG1_PRU1_GPO15	PRG1_PRU1_GPO15										
PRG1_PRU1_GPI15	1			I										
PRG1_RGMII2_TX_CTL	2			O										
PRG1_PWM1_B1	3			IO										
RGMII2_TX_CTL	4			O										
RMII2_TX_EN	5			O										
GPI00_80	7			IO										
GPMC0_A18	8			OZ										

ADVANCE INFORMATION

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
Y8	PRG1_PRU1_GPO16	PRG1_PRU1_GPO16	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_82	0x000F4148	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI16	1	I										
		PRG1_RGMII2_TXC	2	IO										
		PRG1_PWM1_A2	3	IO										
		RGMII2_TXC	4	IO										
		GPIO0_81	7	IO										
		GPMC0_A19	8	OZ										
AA14	PRG1_PRU1_GPO17	PRG1_PRU1_GPO17	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_83	0x000F414C	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI17	1	I										
		PRG1_IEP1_EDC_SYNC_OUT1	2	O										
		PRG1_PWM1_B2	3	IO										
		RGMII1_TD3	4	O										
		RMII1_TXD1	5	O										
		GPIO0_19	7	IO										
		GPMC0_BE3n	8	O										
		PRG1_ECAP0_SYNC_OUT	9	O										
Y15	PRG1_PRU1_GPO18	PRG1_PRU1_GPO18	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_84	0x000F4150	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI18	1	I										
		PRG1_IEP1_EDC_LATCH_IN0	2	I										
		PRG1_PWM1_TZ_IN	3	I										
		RGMII1_RD2	4	I										
		RMII1_TX_EN	5	O										
		GPIO0_20	7	IO										
		UART5_CTSn	8	I										
		PRG1_ECAP0_SYNC_IN	9	I										

**ADVANCE INFORMATION**

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
AA13	PRG1_PRU1_GPO19	PRG1_PRU1_GPO19	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV2	Yes	PU/PD	PADCONFIG_85	0x000F4154	Off / Off / Off	Off / Off / Off	7
		PRG1_PRU1_GPI19	1	I										
		PRG1_IEP1_EDC_SYNC_OUT0	2	O										
		PRG1_PWM1_TZ_OUT	3	O										
		RGMII1_RD3	4	I										
		RMII1_CRS_DV	5	I										
		SPI3_CS2	6	IO										
		GPIO0_84	7	IO										
		UART5_RTSn	8	O										
PRG1_ECAP0_IN_APWM_OUT	9	IO												
E19	RESETSTATz	RESETSTATz	0	O	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_169	0x000F42A4	Off / Low / Off	Off / SS / Off	0
C17	RESET_REQz	RESET_REQz	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_168	0x000F42A0	On / Off / Up	On / Off / Up	0
H11, J13	RSVD	RSVD	-	A	RSVD	RSVD	RSVD	-	-	-	-	-	-	-
B8	SPI0_CLK	SPI0_CLK	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_132	0x000F4210	Off / Off / Off	Off / Off / Off	7
		GPIO1_44	7	IO										
B7	SPI0_CS1	SPI0_CS1	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_131	0x000F420C	Off / Off / Off	Off / Off / Off	7
		CPTS0_TS_COMP	1	O										
		I2C2_SCL	2	IOD										
		TIMER_IO10	3	IO										
		PRG0_IEP0_EDIO_OUTVALID	4	O										
		UART6_RXD	5	I										
		ADC_EXT_TRIGGER0	6	I										
GPIO1_43	7	IO												
A8	SPI0_D0	SPI0_D0	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_133	0x000F4214	Off / Off / Off	Off / Off / Off	7
		GPIO1_45	7	IO										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
C9	SPI0_D1	SPI0_D1	0	IO	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_134	0x000F4218	Off / Off / Off	Off / Off / Off	7
		GPIO1_46	7	IO										
C6	TCK	TCK	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_26	0x04084068	On / Off / Up	On / Off / Up	0
A3	TDI	TDI	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_28	0x04084070	On / Off / Up	On / Off / Up	0
B5	TDO	TDO	0	OZ	1.8 V/3.3 V	LVCMOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_29	0x04084074	Off / Off / Up	Off / SS / Up	0
B4	TMS	TMS	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_30	0x04084078	On / Off / Up	On / Off / Up	0
B6	TRSTn	TRSTn	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV_MCU	Yes	PU/PD	MCU_PADCONFIG_27	0x0408406C	On / Off / Down	On / Off / Down	0
B9	UART0_CTSn	UART0_CTSn	0	I	1.8 V/3.3 V	LVCMOS	VDDSHV0	Yes	PU/PD	PADCONFIG_142	0x000F4238	Off / Off / Off	Off / Off / Off	7
		SPI0_CS2	1	IO										
		ADC_EXT_TRIGGER0	2	I										
		UART2_RXD	3	I										
		TIMER_IO6	4	IO										
		SPI4_CLK	6	IO										
		GPIO1_54	7	IO										
		EQEP0_S	8	IO										
CP_GEMAC_CPTS0_TS_SYNC	9	O												

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
A9	UART0_RTSn	UART0_RTSn	0	O	1.8 V/3.3 V	LVC MOS	VDDSHV0	Yes	PU/PD	PADCONFIG_143	0x000F423C	Off / Off / Off	Off / Off / Off	7
		SPI0_CS3	1	IO										
		UART2_TXD	3	O										
		TIMER_IO7	4	IO										
		SPI4_D0	6	IO										
		GPIO1_55	7	IO										
		EQEP0_I	8	IO										
B10	UART0_RXD	UART0_RXD	0	I	1.8 V/3.3 V	LVC MOS	VDDSHV0	Yes	PU/PD	PADCONFIG_140	0x000F4230	Off / Off / Off	Off / Off / Off	7
		SPI2_D0	2	IO										
		GPIO1_52	7	IO										
		EQEP0_A	8	I										
B11	UART0_TXD	UART0_TXD	0	O	1.8 V/3.3 V	LVC MOS	VDDSHV0	Yes	PU/PD	PADCONFIG_141	0x000F4234	Off / Off / Off	Off / Off / Off	7
		SPI2_D1	2	IO										
		GPIO1_53	7	IO										
		EQEP0_B	8	I										
C11	UART1_CTSn	UART1_CTSn	0	I	1.8 V/3.3 V	LVC MOS	VDDSHV0	Yes	PU/PD	PADCONFIG_146	0x000F4248	Off / Off / Off	Off / Off / Off	7
		SPI1_CS2	1	IO										
		ADC_EXT_TRIGGER1	2	I										
		PCIE0_CLKREQn	3	IO										
		UART3_RXD	4	I										
		CP_GEMAC_CPTS0_TS_SYNC	5	O										
		SPI4_D1	6	IO										
		GPIO1_58	7	IO										
		EQEP1_S	8	IO										

ADVANCE INFORMATION



**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
A11	UART1_RTSn	UART1_RTSn	0	O	1.8 V/3.3 V	LVC MOS	VDDSHV0	Yes	PU/PD	PADCONFIG_147	0x000F424C	Off / Off / Off	Off / Off / Off	7
		SPI1_CS3	1	IO										
		UART3_TXD	4	O										
		CP_GEMAC_CPTS0_HW2TSPUSH	5	I										
		SPI4_CS0	6	IO										
		GPIO1_59	7	IO										
		EQEP1_I	8	IO										
B12	UART1_RXD	UART1_RXD	0	I	1.8 V/3.3 V	LVC MOS	VDDSHV0	Yes	PU/PD	PADCONFIG_144	0x000F4240	Off / Off / Off	Off / Off / Off	7
		SPI2_CS0	2	IO										
		CP_GEMAC_CPTS0_TS_COMP	5	O										
		GPIO1_56	7	IO										
		EQEP1_A	8	I										
A12	UART1_TXD	UART1_TXD	0	O	1.8 V/3.3 V	LVC MOS	VDDSHV0	Yes	PU/PD	PADCONFIG_145	0x000F4244	Off / Off / Off	Off / Off / Off	7
		SPI2_CLK	2	IO										
		CP_GEMAC_CPTS0_HW1TSPUSH	5	I										
		GPIO1_57	7	IO										
		EQEP1_B	8	I										
AA17	USB0_DM	USB0_DM	-	IO	1.8 V/3.3 V	USB2PHY	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0	-	-	-	-	-	-	-
AA16	USB0_DP	USB0_DP	-	IO	1.8 V/3.3 V	USB2PHY	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0	-	-	-	-	-	-	-
B19	USB0_DRVVBUS	USB0_DRVVBUS	0	O	1.8 V/3.3 V	LVC MOS	VDDSHV0	Yes	PU/PD	PADCONFIG_170	0x000F42A8	Off / Off / Down	Off / Off / Down	7
		GPIO1_79	7	IO										

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
Y17	USB0_ID	USB0_ID	-	A	1.8 V/3.3 V	USB2PHY	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0	-	-	-	-	-	-	-
W17	USB0_RCALIB	USB0_RCALIB	-	A	1.8 V/3.3 V	USB2PHY	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0	-	-	-	-	-	-	-
V18	USB0_VBUS	USB0_VBUS	-	A	1.8 V/3.3 V	USB2PHY	VDDA_3P3_USB0, VDDA_1P8_USB0, VDDA_0P85_USB0	-	-	-	-	-	-	-
V16	VDDA_0P85_USB0	VDDA_0P85_USB0	-	PWR	-	-	-	-	-	-	-	-	-	-
U15	VDDA_1P8_USB0	VDDA_1P8_USB0	-	PWR	-	-	-	-	-	-	-	-	-	-
K15	VDDA_3P3_SDIO	VDDA_3P3_SDIO	-	PWR	-	-	-	-	-	-	-	-	-	-
U16	VDDA_3P3_USB0	VDDA_3P3_USB0	-	PWR	-	-	-	-	-	-	-	-	-	-
G17, H17	VDDA_ADC	VDDA_ADC	-	PWR	-	-	-	-	-	-	-	-	-	-
H14	VDDA_MCU	VDDA_MCU	-	PWR	-	-	-	-	-	-	-	-	-	-
N12	VDDA_PLL0	VDDA_PLL0	-	PWR	-	-	-	-	-	-	-	-	-	-
G9	VDDA_PLL1	VDDA_PLL1	-	PWR	-	-	-	-	-	-	-	-	-	-
G12	VDDA_PLL2	VDDA_PLL2	-	PWR	-	-	-	-	-	-	-	-	-	-
G11	VDDA_TEMP0	VDDA_TEMP0	-	PWR	-	-	-	-	-	-	-	-	-	-
M11	VDDA_TEMP1	VDDA_TEMP1	-	PWR	-	-	-	-	-	-	-	-	-	-
G5, G6, J10, J12, P14, P8, R10	VDDR_CORE	VDDR_CORE	-	PWR	-	-	-	-	-	-	-	-	-	-
C13, D13, E14	VDDSHV0	VDDSHV0	-	PWR	-	-	-	-	-	-	-	-	-	-

ADVANCE INFORMATION

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
L6, M6, P5, P6	VDDSHV1	VDDSHV1	-	PWR	-	-	-	-	-	-	-	-	-	-
T11, T8, U11, U7, U8	VDDSHV2	VDDSHV2	-	PWR	-	-	-	-	-	-	-	-	-	-
R17, T17	VDDSHV3	VDDSHV3	-	PWR	-	-	-	-	-	-	-	-	-	-
N16, N17	VDDSHV4	VDDSHV4	-	PWR	-	-	-	-	-	-	-	-	-	-
L16, L17	VDDSHV5	VDDSHV5	-	PWR	-	-	-	-	-	-	-	-	-	-
E7, E8, E9	VDDSHV_MCU	VDDSHV_MCU	-	PWR	-	-	-	-	-	-	-	-	-	-
F18	VDDS_OSC	VDDS_OSC	-	PWR	-	-	-	-	-	-	-	-	-	-
F11, G10, H15, H8, J9, K11, K14, L13, L9, M14, M8, N10, N9, R12, R13, R9	VDD_CORE	VDD_CORE	-	PWR	-	-	-	-	-	-	-	-	-	-
F14	VMON_1P8_SOC	VMON_1P8_SOC	-	A	-	-	-	-	-	-	-	-	-	-
E15	VMON_3P3_SOC	VMON_3P3_SOC	-	A	-	-	-	-	-	-	-	-	-	-
G13	VMON_VSYS	VMON_VSYS	-	A	-	-	-	-	-	-	-	-	-	-
E16	VPP	VPP	-	PWR	-	-	-	-	-	-	-	-	-	-

**ADVANCE INFORMATION**

Table 6-2. Pin Attributes (ALX Package) (continued)

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
A1, A2, A20, A21, AA1, AA2, AA20, AA21, B1, B21, D10, D16, D17, E11, E13, E6, F17, F8, G16, H16, H6, H7, J11, J16, J5, J6, K16, K6, K7, K8, L10, L11, L12, M15, M16, M7, N11, N13, N6, P11, P15, P16, P7, R11, R6,	VSS	VSS	-	GND	-	-	-	-	-	-	-	-	-	-

ADVANCE INFORMATION

**Table 6-2. Pin Attributes (ALX Package) (continued)**

BALL #	BALL NAME	SIGNAL NAME	MUX MODE	TYPE	IO VOLTAGE VALUE	BUFFER TYPE	POWER	HYS	PULL UP/DOWN TYPE	PADCONFIG REGISTER	PADCONFIG ADDRESS	BALL STATE DURING RESET (RX/TX/PULL)	BALL STATE AFTER RESET (RX/TX/PULL)	MUX MODE AFTER RESET
T14, U6, Y1, Y21														

## 6.4 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

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### Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via PADCONFIG registers. Device subsystems may provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

---

2. **PIN TYPE:** Signal direction and type:

- I = Input
- O = Output
- IO = Input, Output, or simultaneously Input and Output
- IOD = Input, Output, or simultaneously Input and Output with open-drain output function
- IOZ = Input, Output, or simultaneously Input and Output with three-state output function
- OZ = Output with three-state output function
- A = Analog
- PWR = Power
- GND = Ground
- CAP = LDO Capacitor

3. **DESCRIPTION:** Description of the signal

4. **BALL:** Associated ball number

For more information on the I/O cell configurations, see the *Pad Configuration Registers* section in *Device Configuration* chapter of the device TRM.

### Note

The following peripheral instances and signals **are not supported** by the AM243x\_ALX device package. In some cases, the entire peripheral can not be used due to critical interface signal availability.

#### MAIN Domain

- **DDRSS0\***
- GPIO0\_[7:10]
- GPIO0\_[13:14]
- GPIO0\_[31:35]
- GPIO0\_[37:44]
- GPIO1\_[42]
- GPIO1\_[47:51]
- GPIO1\_[68,70]
- **I2C2\***
- **SPI1\***
- SYNC0
- CP\_GEMAC\_CPTS0\_RFT\_CLK
- ECAP0\_IN\_APWM\_OUT
- EHRPWM5\_B
- EHRPWM4\*
- EHRPWM6\*
- **SERDES0\***
- OSPI0\_D[4:7]
- OSPI0\_RESET\_OUT[0:1]
- OSPI0\_CSn[2:3]
- OSPI0\_ECC\_FAIL
- **GPMC0\***
- GPMC0\_FCLK\_MUX
- **MMC0\***
- **FSI\_TX1\***
- **FSI\_RX[4:5]\***
- PRG1\_IEP0\_EDIO\_OUTVALID
- CPTS0\_RFT\_CLK
- TRACE[14:23]
- EXTINTn

#### MCU Domain

- **MCU\_I2C[0:1]\***
- **MCU\_SPI[0:1]\***
- **MCU\_UART1\***
- MCU\_GPIO[4:21]
- MCU\_TIMER\_IO[2:3]
- MCU\_EXT\_REFCLK0
- MCU\_SYSCLKOUT0

**\*Entire peripheral instance is unsupported.**

## 6.4.1 ADC

### MAIN Domain Instances

#### 6.4.1.1 ADC0 Signal Descriptions

**Table 6-3. ADC0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
ADC0_AIN0	A	ADC Analog Input 0 / GPIO1_80 (Input Only)	G20	H21
ADC0_AIN1	A	ADC Analog Input 1 / GPIO1_81 (Input Only)	F20	F19
ADC0_AIN2	A	ADC Analog Input 2 / GPIO1_82 (Input Only)	E21	F21
ADC0_AIN3	A	ADC Analog Input 3 / GPIO1_83 (Input Only)	D20	F20
ADC0_AIN4	A	ADC Analog Input 4 / GPIO1_84 (Input Only)	G21	H20
ADC0_AIN5	A	ADC Analog Input 5 / GPIO1_85 (Input Only)	F21	E21
ADC0_AIN6	A	ADC Analog Input 6 / GPIO1_86 (Input Only)	F19	G20
ADC0_AIN7	A	ADC Analog Input 7 / GPIO1_87 (Input Only)	E20	E20
ADC_EXT_TRIGGER0	I	ADC Trigger Input	B16, C13	B7, B9
ADC_EXT_TRIGGER1	I	ADC Trigger Input	D14, D16	C11

## 6.4.2 DDRSS

### MAIN Domain Instances

#### 6.4.2.1 DDRSS0 Signal Descriptions

**Table 6-4. DDRSS0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
DDR0_ACT_n	O	DDRSS Activation Command	H2	
DDR0_ALERT_n	IO	DDRSS Alert	H1	
DDR0_CAS_n	O	DDRSS Column Address Strobe	J5	
DDR0_PAR	O	DDRSS Command and Address Parity	K5	
DDR0_RAS_n	O	DDRSS Row Address Strobe	F6	
DDR0_WE_n	O	DDRSS Write Enable	H4	
DDR0_A0	O	DDRSS Address Bus	D2	
DDR0_A1	O	DDRSS Address Bus	C5	
DDR0_A2	O	DDRSS Address Bus	E2	
DDR0_A3	O	DDRSS Address Bus	D4	
DDR0_A4	O	DDRSS Address Bus	D3	
DDR0_A5	O	DDRSS Address Bus	F2	
DDR0_A6	O	DDRSS Address Bus	J2	
DDR0_A7	O	DDRSS Address Bus	L5	
DDR0_A8	O	DDRSS Address Bus	J3	
DDR0_A9	O	DDRSS Address Bus	J4	
DDR0_A10	O	DDRSS Address Bus	K3	
DDR0_A11	O	DDRSS Address Bus	J1	



**Table 6-4. DDRSS0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
DDR0_A12	O	DDRSS Address Bus	M5	
DDR0_A13	O	DDRSS Address Bus	K4	
DDR0_BA0	O	DDRSS Bank Address	G4	
DDR0_BA1	O	DDRSS Bank Address	G5	
DDR0_BG0	O	DDRSS Bank Group	G2	
DDR0_BG1	O	DDRSS Bank Group	H3	
DDR0_CK0	O	DDRSS Clock	F1	
DDR0_CK0_n	O	DDRSS Negative Clock	E1	
DDR0_CKE0	O	DDRSS Clock Enable	F4	
DDR0_CKE1	O	DDRSS Clock Enable	F3	
DDR0_CS0_n	O	DDRSS Chip Select 0	E3	
DDR0_CS1_n	O	DDRSS Chip Select 1	E4	
DDR0_DM0	IO	DDRSS Data Mask	B2	
DDR0_DM1	IO	DDRSS Data Mask	M2	
DDR0_DQ0	IO	DDRSS Data	A3	
DDR0_DQ1	IO	DDRSS Data	A2	
DDR0_DQ2	IO	DDRSS Data	B5	
DDR0_DQ3	IO	DDRSS Data	A4	
DDR0_DQ4	IO	DDRSS Data	B3	
DDR0_DQ5	IO	DDRSS Data	C4	
DDR0_DQ6	IO	DDRSS Data	C2	
DDR0_DQ7	IO	DDRSS Data	B4	
DDR0_DQ8	IO	DDRSS Data	N5	
DDR0_DQ9	IO	DDRSS Data	L4	
DDR0_DQ10	IO	DDRSS Data	L2	
DDR0_DQ11	IO	DDRSS Data	M3	
DDR0_DQ12	IO	DDRSS Data	N4	
DDR0_DQ13	IO	DDRSS Data	N3	
DDR0_DQ14	IO	DDRSS Data	M4	
DDR0_DQ15	IO	DDRSS Data	N2	
DDR0_DQS0	IO	Data strobe 0 input/output for byte 0 of the 16-bit data bus. This signal is output to the DDRSS memory when writing and input when reading.	C1	
DDR0_DQS0_n	IO	Data strobe 0 invert	B1	
DDR0_DQS1	IO	Data strobe 1 input/output for byte 2 of the 16-bit data bus. This signal is output to the DDRSS memory when writing and input when reading.	N1	
DDR0_DQS1_n	IO	Data strobe 1 invert	M1	
DDR0_ODT0	O	DDRSS On-Die Termination for Chip Select 0	E5	

**Table 6-4. DDRSS0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
DDR0_ODT1	O	DDRSS On-Die Termination for Chip Select 1	F5	
DDR0_RESET0_n	O	DDRSS Reset	D5	

**6.4.3 GPIO****MAIN Domain Instances****6.4.3.1 GPIO0 Signal Descriptions****Table 6-5. GPIO0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
GPIO0_0	IO	General Purpose Input/Output	N20	P20
GPIO0_1	IO	General Purpose Input/Output	N21	M21
GPIO0_2	IO	General Purpose Input/Output	N19	P17
GPIO0_3	IO	General Purpose Input/Output	M19	L19
GPIO0_4	IO	General Purpose Input/Output	M18	N20
GPIO0_5	IO	General Purpose Input/Output	M20	L21
GPIO0_6	IO	General Purpose Input/Output	M21	N19
GPIO0_7	IO	General Purpose Input/Output	P21	
GPIO0_8	IO	General Purpose Input/Output	P20	
GPIO0_9	IO	General Purpose Input/Output	N18	
GPIO0_10	IO	General Purpose Input/Output	M17	
GPIO0_11	IO	General Purpose Input/Output	L19	L20
GPIO0_12	IO	General Purpose Input/Output	L18	M20
GPIO0_13	IO	General Purpose Input/Output	K17	
GPIO0_14	IO	General Purpose Input/Output	L17	
GPIO0_15	IO	General Purpose Input/Output	T20	R21
GPIO0_16	IO	General Purpose Input/Output	U21	R20
GPIO0_17	IO	General Purpose Input/Output	T18	T19
GPIO0_18	IO	General Purpose Input/Output	U20	V21
GPIO0_19	IO	General Purpose Input/Output	AA14	AA14
GPIO0_20	IO	General Purpose Input/Output	Y13	Y15
GPIO0_21	IO	General Purpose Input/Output	V20	T18
GPIO0_22	IO	General Purpose Input/Output	V21	U19
GPIO0_23	IO	General Purpose Input/Output	V19	U18
GPIO0_24	IO	General Purpose Input/Output	T17	U20
GPIO0_25	IO	General Purpose Input/Output	R16	V20
GPIO0_26	IO	General Purpose Input/Output	W20	W20
GPIO0_27	IO	General Purpose Input/Output	W21	Y20
GPIO0_28	IO	General Purpose Input/Output	V18	Y19

**Table 6-5. GPIO0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
GPIO0_29	IO	General Purpose Input/Output	Y21	Y18
GPIO0_30	IO	General Purpose Input/Output	Y20	AA19
GPIO0_31	IO	General Purpose Input/Output	R17	
GPIO0_32	IO	General Purpose Input/Output	P16	
GPIO0_33	IO	General Purpose Input/Output	R18	
GPIO0_34	IO	General Purpose Input/Output	T21	
GPIO0_35	IO	General Purpose Input/Output	P17	
GPIO0_36	IO	General Purpose Input/Output	T19	P21
GPIO0_37	IO	General Purpose Input/Output	W19	
GPIO0_38	IO	General Purpose Input/Output	Y18	
GPIO0_39	IO	General Purpose Input/Output	N16	
GPIO0_40	IO	General Purpose Input/Output	N17	
GPIO0_41	IO	General Purpose Input/Output	R19	
GPIO0_42	IO	General Purpose Input/Output	R20	
GPIO0_43	IO	General Purpose Input/Output	P19	
GPIO0_44	IO	General Purpose Input/Output	R21	
GPIO0_45	IO	General Purpose Input/Output	Y7	V4
GPIO0_46	IO	General Purpose Input/Output	U8	W5
GPIO0_47	IO	General Purpose Input/Output	W8	AA4
GPIO0_48	IO	General Purpose Input/Output	V8	Y5
GPIO0_49	IO	General Purpose Input/Output	Y8	AA5
GPIO0_50	IO	General Purpose Input/Output	V13	U14
GPIO0_51	IO	General Purpose Input/Output	AA7	Y2
GPIO0_52	IO	General Purpose Input/Output	U13	V13
GPIO0_53	IO	General Purpose Input/Output	W13	Y13
GPIO0_54	IO	General Purpose Input/Output	U15	W16
GPIO0_55	IO	General Purpose Input/Output	U14	W13
GPIO0_56	IO	General Purpose Input/Output	AA8	V5
GPIO0_57	IO	General Purpose Input/Output	U9	W2
GPIO0_58	IO	General Purpose Input/Output	W9	V6
GPIO0_59	IO	General Purpose Input/Output	AA9	AA7
GPIO0_60	IO	General Purpose Input/Output	Y9	Y7
GPIO0_61	IO	General Purpose Input/Output	V9	W6
GPIO0_62	IO	General Purpose Input/Output	U7	T2
GPIO0_63	IO	General Purpose Input/Output	V7	Y4
GPIO0_64	IO	General Purpose Input/Output	W7	U3
GPIO0_65	IO	General Purpose Input/Output	W11	AA10
GPIO0_66	IO	General Purpose Input/Output	V11	Y10

**Table 6-5. GPIO0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
GPIO0_67	IO	General Purpose Input/Output	AA12	Y11
GPIO0_68	IO	General Purpose Input/Output	Y12	V12
GPIO0_69	IO	General Purpose Input/Output	W12	Y12
GPIO0_70	IO	General Purpose Input/Output	AA13	AA11
GPIO0_71	IO	General Purpose Input/Output	U11	V10
GPIO0_72	IO	General Purpose Input/Output	V15	Y14
GPIO0_73	IO	General Purpose Input/Output	U12	W11
GPIO0_74	IO	General Purpose Input/Output	V14	Y16
GPIO0_75	IO	General Purpose Input/Output	W14	U13
GPIO0_76	IO	General Purpose Input/Output	AA10	Y6
GPIO0_77	IO	General Purpose Input/Output	V10	AA8
GPIO0_78	IO	General Purpose Input/Output	U10	Y9
GPIO0_79	IO	General Purpose Input/Output	AA11	W9
GPIO0_80	IO	General Purpose Input/Output	Y11	V9
GPIO0_81	IO	General Purpose Input/Output	Y10	Y8
GPIO0_82	IO	General Purpose Input/Output	U18	U21
GPIO0_83	IO	General Purpose Input/Output	U19	T20
GPIO0_84	IO	General Purpose Input/Output	V12	AA13
GPIO0_85	IO	General Purpose Input/Output	AA6	V2
GPIO0_86	IO	General Purpose Input/Output	Y6	W1

**6.4.3.2 GPIO1 Signal Descriptions****Table 6-6. GPIO1 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
GPIO1_0	IO	General Purpose Input/Output	Y1	J3
GPIO1_1	IO	General Purpose Input/Output	R4	J4
GPIO1_2	IO	General Purpose Input/Output	U2	G1
GPIO1_3	IO	General Purpose Input/Output	V2	H1
GPIO1_4	IO	General Purpose Input/Output	AA2	K2
GPIO1_5	IO	General Purpose Input/Output	R3	F2
GPIO1_6	IO	General Purpose Input/Output	T3	H2
GPIO1_7	IO	General Purpose Input/Output	T1	E2
GPIO1_8	IO	General Purpose Input/Output	T2	H5
GPIO1_9	IO	General Purpose Input/Output	W6	Y3
GPIO1_10	IO	General Purpose Input/Output	AA5	U1
GPIO1_11	IO	General Purpose Input/Output	Y3	L1
GPIO1_12	IO	General Purpose Input/Output	AA3	K1

**Table 6-6. GPIO1 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
GPIO1_13	IO	General Purpose Input/Output	R6	N1
GPIO1_14	IO	General Purpose Input/Output	V4	N2
GPIO1_15	IO	General Purpose Input/Output	T5	N4
GPIO1_16	IO	General Purpose Input/Output	U4	N3
GPIO1_17	IO	General Purpose Input/Output	U1	E1
GPIO1_18	IO	General Purpose Input/Output	V1	K4
GPIO1_19	IO	General Purpose Input/Output	W1	G2
GPIO1_20	IO	General Purpose Input/Output	Y2	L5
GPIO1_21	IO	General Purpose Input/Output	W2	J2
GPIO1_22	IO	General Purpose Input/Output	V3	M2
GPIO1_23	IO	General Purpose Input/Output	T4	L2
GPIO1_24	IO	General Purpose Input/Output	W3	L3
GPIO1_25	IO	General Purpose Input/Output	P4	E3
GPIO1_26	IO	General Purpose Input/Output	R5	F5
GPIO1_27	IO	General Purpose Input/Output	W5	T5
GPIO1_28	IO	General Purpose Input/Output	R1	F4
GPIO1_29	IO	General Purpose Input/Output	Y5	R2
GPIO1_30	IO	General Purpose Input/Output	V6	U2
GPIO1_31	IO	General Purpose Input/Output	W4	P1
GPIO1_32	IO	General Purpose Input/Output	Y4	P2
GPIO1_33	IO	General Purpose Input/Output	T6	T4
GPIO1_34	IO	General Purpose Input/Output	U6	R5
GPIO1_35	IO	General Purpose Input/Output	U5	M4
GPIO1_36	IO	General Purpose Input/Output	AA4	T3
GPIO1_37	IO	General Purpose Input/Output	V5	T1
GPIO1_38	IO	General Purpose Input/Output	P5	D1
GPIO1_39	IO	General Purpose Input/Output	R2	F3
GPIO1_40	IO	General Purpose Input/Output	P2	E4
GPIO1_41	IO	General Purpose Input/Output	P3	D2
GPIO1_42	IO	General Purpose Input/Output	D12	
GPIO1_43	IO	General Purpose Input/Output	C13	B7
GPIO1_44	IO	General Purpose Input/Output	D13	B8
GPIO1_45	IO	General Purpose Input/Output	A13	A8
GPIO1_46	IO	General Purpose Input/Output	A14	C9
GPIO1_47	IO	General Purpose Input/Output	B14	
GPIO1_48	IO	General Purpose Input/Output	D14	
GPIO1_49	IO	General Purpose Input/Output	C14	
GPIO1_50	IO	General Purpose Input/Output	B15	

**Table 6-6. GPIO1 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
GPIO1_51	IO	General Purpose Input/Output	A15	
GPIO1_52	IO	General Purpose Input/Output	D15	B10
GPIO1_53	IO	General Purpose Input/Output	C16	B11
GPIO1_54	IO	General Purpose Input/Output	B16	B9
GPIO1_55	IO	General Purpose Input/Output	A16	A9
GPIO1_56	IO	General Purpose Input/Output	E15	B12
GPIO1_57	IO	General Purpose Input/Output	E14	A12
GPIO1_58	IO	General Purpose Input/Output	D16	C11
GPIO1_59	IO	General Purpose Input/Output	E16	A11
GPIO1_60	IO	General Purpose Input/Output	A17	B13
GPIO1_61	IO	General Purpose Input/Output	B17	A14
GPIO1_62	IO	General Purpose Input/Output	C17	B14
GPIO1_63	IO	General Purpose Input/Output	D17	A15
GPIO1_64	IO	General Purpose Input/Output	A18	B16
GPIO1_65	IO	General Purpose Input/Output	B18	B15
GPIO1_66	IO	General Purpose Input/Output	C18	A17
GPIO1_67	IO	General Purpose Input/Output	B19	B18
GPIO1_68	IO	General Purpose Input/Output	D18	
GPIO1_69	IO	General Purpose Input/Output	A19	A18
GPIO1_70	IO	General Purpose Input/Output	C19	
GPIO1_71	IO	General Purpose Input/Output	K18	K18
GPIO1_72	IO	General Purpose Input/Output	K19	K20
GPIO1_73	IO	General Purpose Input/Output	L21	J19
GPIO1_74	IO	General Purpose Input/Output	K21	J18
GPIO1_75	IO	General Purpose Input/Output	L20	J20
GPIO1_76	IO	General Purpose Input/Output	J19	J21
GPIO1_77	IO	General Purpose Input/Output	D19	B17
GPIO1_78	IO	General Purpose Input/Output	C20	C16
GPIO1_79	IO	General Purpose Input/Output	E19	B19
GPIO1_80	I	General Purpose Input/Output	G20	H21
GPIO1_81	I	General Purpose Input/Output	F20	F19
GPIO1_82	I	General Purpose Input/Output	E21	F21
GPIO1_83	I	General Purpose Input/Output	D20	F20
GPIO1_84	I	General Purpose Input/Output	G21	H20
GPIO1_85	I	General Purpose Input/Output	F21	E21
GPIO1_86	I	General Purpose Input/Output	F19	G20
GPIO1_87	I	General Purpose Input/Output	E20	E20

## MCU Domain Instances

### 6.4.3.3 MCU\_GPIO0 Signal Descriptions

**Table 6-7. MCU\_GPIO0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_GPIO0_0	IO	General Purpose Input/Output	E8	C2
MCU_GPIO0_1	IO	General Purpose Input/Output	D8	D4
MCU_GPIO0_2	IO	General Purpose Input/Output	A8	B2
MCU_GPIO0_3	IO	General Purpose Input/Output	A9	D6
MCU_GPIO0_4	IO	General Purpose Input/Output	B6	
MCU_GPIO0_5	IO	General Purpose Input/Output	A7	
MCU_GPIO0_6	IO	General Purpose Input/Output	B7	
MCU_GPIO0_7	IO	General Purpose Input/Output	D7	
MCU_GPIO0_8	IO	General Purpose Input/Output	C7	
MCU_GPIO0_9	IO	General Purpose Input/Output	C8	
MCU_GPIO0_10	IO	General Purpose Input/Output	E7	
MCU_GPIO0_11	IO	General Purpose Input/Output	E6	
MCU_GPIO0_12	IO	General Purpose Input/Output	C6	
MCU_GPIO0_13		General Purpose Input/Output	D6	
MCU_GPIO0_14	IO	General Purpose Input/Output	C9	
MCU_GPIO0_15	IO	General Purpose Input/Output	D9	
MCU_GPIO0_16	IO	General Purpose Input/Output	B8	
MCU_GPIO0_17	IO	General Purpose Input/Output	B9	
MCU_GPIO0_18	IO	General Purpose Input/Output	E9	
MCU_GPIO0_19	IO	General Purpose Input/Output	A10	
MCU_GPIO0_20	IO	General Purpose Input/Output	A11	
MCU_GPIO0_21	IO	General Purpose Input/Output	B10	
MCU_GPIO0_22	IO	General Purpose Input/Output	B13	A6

**ADVANCE INFORMATION**

## 6.4.4 I2C

### MAIN Domain Instances

#### 6.4.4.1 I2C0 Signal Descriptions

**Table 6-8. I2C0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
I2C0_SCL	IOD	I2C Clock	A18	B16
I2C0_SDA	IOD	I2C Data	B18	B15

#### 6.4.4.2 I2C1 Signal Descriptions

Table 6-9. I2C1 Signal Descriptions

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
I2C1_SCL	IOD	I2C Clock	C18	A17
I2C1_SDA	IOD	I2C Data	B19	B18

#### 6.4.4.3 I2C2 Signal Descriptions

Table 6-10. I2C2 Signal Descriptions

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
I2C2_SCL	IOD	I2C Clock	C13, P19	B7
I2C2_SDA	IOD	I2C Data	D14, R21	

#### 6.4.4.4 I2C3 Signal Descriptions

Table 6-11. I2C3 Signal Descriptions

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
I2C3_SCL	IOD	I2C Clock	C17	B14
I2C3_SDA	IOD	I2C Data	D17	A15

### MCU Domain Instances

#### 6.4.4.5 MCU\_I2C0 Signal Descriptions

Table 6-12. MCU\_I2C0 Signal Descriptions

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_I2C0_SCL	IOD	I2C Clock	E9	
MCU_I2C0_SDA	IOD	I2C Data	A10	

#### 6.4.4.6 MCU\_I2C1 Signal Descriptions

Table 6-13. MCU\_I2C1 Signal Descriptions

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_I2C1_SCL	IOD	I2C Clock	A11	
MCU_I2C1_SDA	IOD	I2C Data	B10	

### 6.4.5 MCAN

#### MAIN Domain Instances

#### 6.4.5.1 MCAN0 Signal Descriptions

Table 6-14. MCAN0 Signal Descriptions

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCAN0_RX	I	MCAN Receive Data	B17	A14



**Table 6-14. MCAN0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCAN0_TX	O	MCAN Transmit Data	A17	B13

#### 6.4.5.2 MCAN1 Signal Descriptions

**Table 6-15. MCAN1 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCAN1_RX	I	MCAN Receive Data	D17	A15
MCAN1_TX	O	MCAN Transmit Data	C17	B14

#### 6.4.6 SPI (MCSPi)

##### MAIN Domain Instances

##### 6.4.6.1 MCSPI0 Signal Descriptions

**Table 6-16. MCSPI0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
SPI0_CLK	IO	SPI Clock	D13	B8
SPI0_CS0	IO	SPI Chip Select 0	D12	
SPI0_CS1	IO	SPI Chip Select 1	C13	B7
SPI0_CS2	IO	SPI Chip Select 2	B16	B9
SPI0_CS3	IO	SPI Chip Select 3	A16	A9
SPI0_D0	IO	SPI Data 0	A13	A8
SPI0_D1	IO	SPI Data 1	A14	C9

##### 6.4.6.2 MCSPI1 Signal Descriptions

**Table 6-17. MCSPI1 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
SPI1_CLK	IO	SPI Clock	C14	
SPI1_CS0	IO	SPI Chip Select 0	B14	
SPI1_CS1	IO	SPI Chip Select 1	D14	
SPI1_CS2	IO	SPI Chip Select 2	D16	C11
SPI1_CS3	IO	SPI Chip Select 3	E16	A11
SPI1_D0	IO	SPI Data 0	B15	
SPI1_D1	IO	SPI Data 1	A15	

##### 6.4.6.3 MCSPI2 Signal Descriptions

**Table 6-18. MCSPI2 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
SPI2_CLK	IO	SPI Clock	E14	A12

**Table 6-18. MCSPI2 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
SPI2_CS0	IO	SPI Chip Select 0	E15	B12
SPI2_CS1	IO	SPI Chip Select 1	C18	A17
SPI2_CS2	IO	SPI Chip Select 2	B19	B18
SPI2_CS3	IO	SPI Chip Select 3	A19	A18
SPI2_D0	IO	SPI Data 0	D15	B10
SPI2_D1	IO	SPI Data 1	C16	B11

**6.4.6.4 MCSPI3 Signal Descriptions****Table 6-19. MCSPI3 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
SPI3_CLK	IO	SPI Clock	U4	N3
SPI3_CS0	IO	SPI Chip Select 0	U1	E1
SPI3_CS1	IO	SPI Chip Select 1	T5	N4
SPI3_CS2	IO	SPI Chip Select 2	V12	AA13
SPI3_CS3	IO	SPI Chip Select 3	V15	Y14
SPI3_D0	IO	SPI Data 0	R6	N1
SPI3_D1	IO	SPI Data 1	V4	N2

**6.4.6.5 MCSPI4 Signal Descriptions****Table 6-20. MCSPI4 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
SPI4_CLK	IO	SPI Clock	B16	B9
SPI4_CS0	IO	SPI Chip Select 0	E16	A11
SPI4_CS1	IO	SPI Chip Select 1	A17	B13
SPI4_CS2	IO	SPI Chip Select 0	B17	A14
SPI4_CS3	IO	SPI Chip Select 2	D18	
SPI4_D0	IO	SPI Data 0	A16	A9
SPI4_D1	IO	SPI Data 1	D16	C11

**MCU Domain Instances****6.4.6.6 MCU\_MCSPI0 Signal Descriptions****Table 6-21. MCU\_MCSPI0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_SPI0_CLK	IO	SPI Clock	E6	
MCU_SPI0_CS0	IO	SPI Chip Select 0	D6	
MCU_SPI0_CS1	IO	SPI Chip Select 1	C6	

**Table 6-21. MCU\_MCSPi0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_SPI0_CS2	IO	SPI Chip Select 2	D8	D4
MCU_SPI0_CS3	IO	SPI Chip Select 3	B8	
MCU_SPI0_D0	IO	SPI Data 0	E7	
MCU_SPI0_D1	IO	SPI Data 1	B6	

#### 6.4.6.7 MCU\_MCSPi1 Signal Descriptions

**Table 6-22. MCU\_MCSPi1 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_SPI1_CLK	IO	SPI Clock	D7	
MCU_SPI1_CS0	IO	SPI Chip Select 0	A7	
MCU_SPI1_CS1	IO	SPI Chip Select 1	B7	
MCU_SPI1_CS2	IO	SPI Chip Select 2	E8	C2
MCU_SPI1_CS3	IO	SPI Chip Select 3	B9	
MCU_SPI1_D0	IO	SPI Data 0	C7	
MCU_SPI1_D1	IO	SPI Data 1	C8	

#### 6.4.7 UART

##### MAIN Domain Instances

##### 6.4.7.1 UART0 Signal Descriptions

**Table 6-23. UART0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
UART0_CTSn	I	UART Clear to Send (active low)	B16	B9
UART0_DCDn	I	UART Data Carrier Detect (active low)	C17	B14
UART0_DSRn	I	UART Data Set Ready (active low)	D17	A15
UART0_DTRn	O	UART Data Terminal Ready (active low)	A17	B13
UART0_RIn	I	UART Ring Indicator	B17	A14
UART0_RTSn	O	UART Request to Send (active low)	A16	A9
UART0_RXD	I	UART Receive Data	D15	B10
UART0_TXD	O	UART Transmit Data	C16	B11

##### 6.4.7.2 UART1 Signal Descriptions

**Table 6-24. UART1 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
UART1_CTSn	I	UART Clear to Send (active low)	D16	C11
UART1_RTSn	O	UART Request to Send (active low)	E16	A11
UART1_RXD	I	UART Receive Data	E15	B12

**Table 6-24. UART1 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
UART1_TXD	O	UART Transmit Data	E14	A12

**6.4.7.3 UART2 Signal Descriptions****Table 6-25. UART2 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
UART2_CTSn	I	UART Clear to Send (active low)	L20, V19, Y1	J20, J3, U18
UART2_RTSn	O	UART Request to Send (active low)	J19, T18, U2	G1, J21, T19
UART2_RXD	I	UART Receive Data	B16, K18, T20, V1, W6	B9, K18, K4, R21, Y3
UART2_TXD	O	UART Transmit Data	A16, K19, R4, U21	A9, J4, K20, R20

**6.4.7.4 UART3 Signal Descriptions****Table 6-26. UART3 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
UART3_CTSn	I	UART Clear to Send (active low)	D19, T17, V2	B17, H1, U20
UART3_RTSn	O	UART Request to Send (active low)	C20, R3, U19	C16, F2, T20
UART3_RXD	I	UART Receive Data	AA5, D16, L21, U20, W1	C11, G2, J19, U1, V21
UART3_TXD	O	UART Transmit Data	AA2, E16, K21, U18	A11, J18, K2, U21

**6.4.7.5 UART4 Signal Descriptions****Table 6-27. UART4 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
UART4_CTSn	I	UART Clear to Send (active low)	R16, R5, T3, V1	F5, H2, K4, V20
UART4_RTSn	O	UART Request to Send (active low)	R1, R17, T2, W1	F4, G2, H5
UART4_RXD	I	UART Receive Data	A17, L20, V20, W4, Y3	B13, J20, L1, P1, T18
UART4_TXD	O	UART Transmit Data	B17, J19, T1, V21, W5, Y4	A14, E2, J21, P2, T5, U19

**6.4.7.6 UART5 Signal Descriptions****Table 6-28. UART5 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
UART5_CTSn	I	UART Clear to Send (active low)	W20, Y13, Y2	L5, W20, Y15
UART5_RTSn	O	UART Request to Send (active low)	T21, V12, V3	AA13, M2
UART5_RXD	I	UART Receive Data	C17, D19, P16, T6, Y5	B14, B17, R2, T4

**Table 6-28. UART5 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
UART5_TXD	O	UART Transmit Data	C20, D17, R18, W2	A15, C16, J2

#### 6.4.7.7 UART6 Signal Descriptions

**Table 6-29. UART6 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
UART6_CTSn	I	UART Clear to Send (active low)	A18, T4, W21	B16, L2, Y20
UART6_RTSn	O	UART Request to Send (active low)	B18, P17, P4	B15, E3
UART6_RXD	I	UART Receive Data	C13, U6, V6, Y21	B7, R5, U2, Y18
UART6_TXD	O	UART Transmit Data	D14, W3, Y20	AA19, L3

#### MCU Domain Instances

#### 6.4.7.8 MCU\_UART0 Signal Descriptions

**Table 6-30. MCU\_UART0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_UART0_CTSn	I	UART Clear to Send (active low)	D8	D4
MCU_UART0_RTSn	O	UART Request to Send (active low)	E8	C2
MCU_UART0_RXD	I	UART Receive Data	A9	D6
MCU_UART0_TXD	O	UART Transmit Data	A8	B2

#### 6.4.7.9 MCU\_UART1 Signal Descriptions

**Table 6-31. MCU\_UART1 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_UART1_CTSn	I	UART Clear to Send (active low)	B8	
MCU_UART1_RTSn	O	UART Request to Send (active low)	B9	
MCU_UART1_RXD	I	UART Receive Data	C9	
MCU_UART1_TXD	O	UART Transmit Data	D9	

#### 6.4.8 MDIO

#### MAIN Domain Instances

#### 6.4.8.1 MDIO0 Signal Descriptions

**Table 6-32. MDIO0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MDIO0_MDC	O	MDIO Clock	R2, Y6	F3, W1
MDIO0_MDIO	IO	MDIO Data	AA6, P5	D1, V2

**6.4.9 CPSW****MAIN Domain Instances****6.4.9.1 CPSW3G0 Signal Descriptions****Table 6-33. CPSW3G0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
RGMII1_RXC	I	RGMII Receive Clock	AA5, W13	U1, Y13
RGMII1_RX_CTL	I	RGMII Receive Control	V13, W6	U14, Y3
RGMII1_TXC	IO	RGMII Transmit Clock	U14	W13
RGMII1_TX_CTL	O	RGMII Transmit Control	U15	W16
RGMII2_RXC	I	RGMII Receive Clock	U11	V10
RGMII2_RX_CTL	I	RGMII Receive Control	W12	Y12
RGMII2_TXC	IO	RGMII Transmit Clock	Y10	Y8
RGMII2_TX_CTL	O	RGMII Transmit Control	Y11	V9
RGMII1_RD0	I	RGMII Receive Data 0	AA13, W5	AA11, T5
RGMII1_RD1	I	RGMII Receive Data 1	U12, Y5	R2, W11
RGMII1_RD2	I	RGMII Receive Data 2	V6, Y13	U2, Y15
RGMII1_RD3	I	RGMII Receive Data 3	V12, V5	AA13, T1
RGMII1_TD0	O	RGMII Transmit Data 0	V15	Y14
RGMII1_TD1	O	RGMII Transmit Data 1	V14	Y16
RGMII1_TD2	O	RGMII Transmit Data 2	W14	U13
RGMII1_TD3	O	RGMII Transmit Data 3	AA14	AA14
RGMII2_RD0	I	RGMII Receive Data 0	W11	AA10
RGMII2_RD1	I	RGMII Receive Data 1	V11	Y10
RGMII2_RD2	I	RGMII Receive Data 2	AA12	Y11
RGMII2_RD3	I	RGMII Receive Data 3	Y12	V12
RGMII2_TD0	O	RGMII Transmit Data 0	AA10	Y6
RGMII2_TD1	O	RGMII Transmit Data 1	V10	AA8
RGMII2_TD2	O	RGMII Transmit Data 2	U10	Y9
RGMII2_TD3	O	RGMII Transmit Data 3	AA11	W9
RMII1_CRSDV	I	RMII Carrier Sense / Data Valid	R2, V12	AA13, F3
RMII1_RX_ER	I	RMII Receive Data Error	U15, W6	W16, Y3
RMII1_TX_EN	O	RMII Transmit Enable	P5, Y13	D1, Y15
RMII2_CRSDV	I	RMII Carrier Sense / Data Valid	U10	Y9
RMII2_RX_ER	I	RMII Receive Data Error	W12	Y12
RMII2_TX_EN	O	RMII Transmit Enable	Y11	V9
RMII1_RXD0	I	RMII Receive Data 0	V15, W5	T5, Y14
RMII1_RXD1	I	RMII Receive Data 1	V14, Y5	R2, Y16
RMII1_TXD0	O	RMII Transmit Data 0	V6, W14	U13, U2
RMII1_TXD1	O	RMII Transmit Data 1	AA14, V5	AA14, T1
RMII2_RXD0	I	RMII Receive Data 0	W11	AA10

**Table 6-33. CPSW3G0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
RMII2_RXD1	I	RMII Receive Data 1	V11	Y10
RMII2_TXD0	O	RMII Transmit Data 0	AA10	Y6
RMII2_TXD1	O	RMII Transmit Data 1	V10	AA8
RMII_REF_CLK	I	RMII Reference Clock	AA5, U14	U1, W13

## 6.4.10 ECAP

### MAIN Domain Instances

#### 6.4.10.1 ECAP0 Signal Descriptions

**Table 6-34. ECAP0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
ECAP0_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	D18	

#### 6.4.10.2 ECAP1 Signal Descriptions

**Table 6-35. ECAP1 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
ECAP1_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	C17	B14

#### 6.4.10.3 ECAP2 Signal Descriptions

**Table 6-36. ECAP2 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
ECAP2_IN_APWM_OUT	IO	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	D17	A15

## EQEP

### MAIN Domain Instances

#### 6.4.11.1 EQEP0 Signal Descriptions

**Table 6-37. EQEP0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EQEP0_A	I	EQEP Quadrature Input A	D15, N16, Y2	B10, L5
EQEP0_B	I	EQEP Quadrature Input B	C16, N17, W2	B11, J2
EQEP0_I	IO	EQEP Index	A16, R20, T6, Y5	A9, R2, T4
EQEP0_S	IO	EQEP Strobe	B16, R19, V3	B9, M2

### 6.4.11.2 EQEP1 Signal Descriptions

**Table 6-38. EQEP1 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EQEP1_A	I	EQEP Quadrature Input A	E15, T4, W20	B12, L2, W20
EQEP1_B	I	EQEP Quadrature Input B	E14, W21, W3	A12, L3, Y20
EQEP1_I	IO	EQEP Index	E16, R21, U6, V6	A11, R5, U2
EQEP1_S	IO	EQEP Strobe	D16, P19, P4	C11, E3

### 6.4.11.3 EQEP2 Signal Descriptions

**Table 6-39. EQEP2 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EQEP2_A	I	EQEP Quadrature Input A	C17, R5	B14, F5
EQEP2_B	I	EQEP Quadrature Input B	D17, W5, Y4	A15, P2, T5
EQEP2_I	IO	EQEP Index	A17, W4	B13, P1
EQEP2_S	IO	EQEP Strobe	B17, R1	A14, F4

## 6.4.11 EPWM

### MAIN Domain Instances

#### 6.4.11.1 EPWM Signal Descriptions

**Table 6-40. EPWM Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EHRPWM_SOCA	O	EHRPWM Start of Conversion A	C17	B14
EHRPWM_SOCB	O	EHRPWM Start of Conversion B	D17	A15
EHRPWM_TZn_IN0	I	EHRPWM Trip Zone Input 0 (active low)	T18	T19
EHRPWM_TZn_IN1	I	EHRPWM Trip Zone Input 1 (active low)	V21	U19
EHRPWM_TZn_IN2	I	EHRPWM Trip Zone Input 2 (active low)	R16, R20	V20
EHRPWM_TZn_IN3	I	EHRPWM Trip Zone Input 3 (active low)	P16	
EHRPWM_TZn_IN4	I	EHRPWM Trip Zone Input 4 (active low)	P17, P19	
EHRPWM_TZn_IN5	I	EHRPWM Trip Zone Input 5 (active low)	R21, Y18	

#### 6.4.11.2 EPWM0 Signal Descriptions

**Table 6-41. EPWM0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EHRPWM0_A	IO	EHRPWM Output A	U20	V21
EHRPWM0_B	IO	EHRPWM Output B	U18	U21
EHRPWM0_SYNCI	I	Sync Input to EHRPWM module from an external pin	T20	R21
EHRPWM0_SYNCO	O	Sync Output to EHRPWM module to an external pin	U21	R20
EHRPWM_TZn_IN0	I	EHRPWM Trip Zone Input 0 (active low)	T18	T19



### 6.4.11.3 EPWM1 Signal Descriptions

**Table 6-42. EPWM1 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EHRPWM1_A	IO	EHRPWM Output A	U19	T20
EHRPWM1_B	IO	EHRPWM Output B	V20	T18
EHRPWM_TZn_IN1	I	EHRPWM Trip Zone Input 1 (active low)	V21	U19

### 6.4.11.4 EPWM2 Signal Descriptions

**Table 6-43. EPWM2 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EHRPWM2_A	IO	EHRPWM Output A	V19	U18
EHRPWM2_B	IO	EHRPWM Output B	T17	U20
EHRPWM_TZn_IN2	I	EHRPWM Trip Zone Input 2 (active low)	R16, R20	V20

### 6.4.11.5 EPWM3 Signal Descriptions

**Table 6-44. EPWM3 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EHRPWM3_A	IO	EHRPWM Output A	V18	Y19
EHRPWM3_B	IO	EHRPWM Output B	Y21	Y18
EHRPWM3_SYNCI	I	Sync Input to EHRPWM module from an external pin	Y20	AA19
EHRPWM3_SYNCO	O	Sync Output to EHRPWM module to an external pin	R17	
EHRPWM_TZn_IN3	I	EHRPWM Trip Zone Input 3 (active low)	P16	

### 6.4.11.6 EPWM4 Signal Descriptions

**Table 6-45. EPWM4 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EHRPWM4_A	IO	EHRPWM Output A	R18	
EHRPWM4_B	IO	EHRPWM Output B	T21	
EHRPWM_TZn_IN4	I	EHRPWM Trip Zone Input 4 (active low)	P17, P19	

### 6.4.11.7 EPWM5 Signal Descriptions

**Table 6-46. EPWM5 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EHRPWM5_A	IO	EHRPWM Output A	T19	P21
EHRPWM5_B	IO	EHRPWM Output B	W19	
EHRPWM_TZn_IN5	I	EHRPWM Trip Zone Input 5 (active low)	R21, Y18	

### 6.4.11.8 EPWM6 Signal Descriptions

**Table 6-47. EPWM6 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EHRPWM6_A	IO	EHRPWM Output A	B14, N16	
EHRPWM6_B	IO	EHRPWM Output B	A15, N17	
EHRPWM6_SYNCI	I	Sync Input to EHRPWM module from an external pin	C14, R19	
EHRPWM6_SYNCO	O	Sync Output to EHRPWM module to an external pin	B15, R20	

### 6.4.11.9 EPWM7 Signal Descriptions

**Table 6-48. EPWM7 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EHRPWM7_A	IO	EHRPWM Output A	P17, P5, W20	D1, W20
EHRPWM7_B	IO	EHRPWM Output B	R2, W21, Y18	F3, Y20

### 6.4.11.10 EPWM8 Signal Descriptions

**Table 6-49. EPWM8 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EHRPWM8_A	IO	EHRPWM Output A	V1, V21	K4, U19
EHRPWM8_B	IO	EHRPWM Output B	R16, W1	G2, V20

## 6.4.12 SERDES

### MAIN Domain Instances

#### 6.4.12.1 SERDES0 Signal Descriptions

**Table 6-50. SERDES0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PCIE0_CLKREQn	IO	PCIE Clock Request Signal	D16	C11
SERDES0_REXT	A	External Calibration Resistor	T13	
SERDES0_REFCLK0N	IO	Serdes Reference Clock Input/Output (negative)	W16	
SERDES0_REFCLK0P	IO	Serdes Reference Clock Input/Output (positive)	W17	
SERDES0_RX0_N	I	SERDES Differential Receive Data (negative)	Y15	
SERDES0_RX0_P	I	SERDES Differential Receive Data (positive)	Y16	
SERDES0_TX0_N	O	SERDES Differential Transmit Data (negative)	AA16	
SERDES0_TX0_P	O	SERDES Differential Transmit Data (positive)	AA17	

## 6.4.13 USB

### MAIN Domain Instances

#### 6.4.13.1 USB0 Signal Descriptions

**Table 6-51. USB0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
USB0_DM	IO	USB 2.0 Differential Data (negative)	AA20	AA17
USB0_DP	IO	USB 2.0 Differential Data (positive)	AA19	AA16
USB0_DRVVBUS	O	USB VBUS control output (active high)	E19	B19
USB0_ID	A	USB 2.0 Dual-Role Device Role Select	U16	Y17
USB0_RCALIB	A	Pin to connect to calibration resistor	U17	W17
USB0_VBUS	A	USB Level-shifted VBUS Input	T14	V18

## 6.4.14 OSPI

### MAIN Domain Instances

#### 6.4.14.1 OSPI0 Signal Descriptions

**Table 6-52. OSPI0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
OSPI0_CLK	O	OSPI Clock	N20	P20
OSPI0_DQS	I	OSPI Data Strobe (DQS) or Loopback Clock Input	N19	P17
OSPI0_ECC_FAIL	I	OSPI ECC Status	L17	
OSPI0_LBCLKO	IO	OSPI Loopback Clock Output	N21	M21
OSPI0_CS <sub>n</sub> 0	O	OSPI Chip Select 0 (active low)	L19	L20
OSPI0_CS <sub>n</sub> 1	O	OSPI Chip Select 1 (active low)	L18	M20
OSPI0_CS <sub>n</sub> 2	O	OSPI Chip Select 2 (active low)	K17	
OSPI0_CS <sub>n</sub> 3	O	OSPI Chip Select 3 (active low)	L17	
OSPI0_D0	IO	OSPI Data 0	M19	L19
OSPI0_D1	IO	OSPI Data 1	M18	N20
OSPI0_D2	IO	OSPI Data 2	M20	L21
OSPI0_D3	IO	OSPI Data 3	M21	N19
OSPI0_D4	IO	OSPI Data 2	P21	
OSPI0_D5	IO	OSPI Data 2	P20	
OSPI0_D6	IO	OSPI Data 2	N18	
OSPI0_D7	IO	OSPI Data 2	M17	
OSPI0_RESET_OUT0	O	OSPI Reset	L17	
OSPI0_RESET_OUT1	O	OSPI Reset	K17	

## 6.4.15 GPMC

### MAIN Domain Instances

#### 6.4.15.1 GPMC0 Signal Descriptions

**Table 6-53. GPMC0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
GPMC0_ADVn_ALE	O	GPMC Address Valid (active low) or Address Latch Enable	P16	
GPMC0_CLK	O	GPMC clock	R17	
GPMC0_DIR	O	GPMC Data Bus Signal Direction Control	N17	
GPMC0_OEn_REn	O	GPMC Output Enable (active low) or Read Enable (active low)	R18	
GPMC0_WEn	O	GPMC Write Enable (active low)	T21	
GPMC0_WPn	O	GPMC Flash Write Protect (active low)	N16	
GPMC0_A0	OZ	GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories	U2, U7	G1, T2
GPMC0_A1	OZ	GPMC address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode	AA2, V7	K2, Y4
GPMC0_A2	OZ	GPMC address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode	T2, W7	H5, U3
GPMC0_A3	OZ	GPMC address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode	V4, W11	AA10, N2
GPMC0_A4	OZ	GPMC address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode	U4, V11	N3, Y10
GPMC0_A5	OZ	GPMC address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode	AA12, V1	K4, Y11
GPMC0_A6	OZ	GPMC address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode	W1, Y12	G2, V12
GPMC0_A7	OZ	GPMC address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode	W12, Y4	P2, Y12
GPMC0_A8	OZ	GPMC address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode	AA13, T6	AA11, T4
GPMC0_A9	OZ	GPMC address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode	U11, U6	R5, V10
GPMC0_A10	OZ	GPMC address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode	U5, V15	M4, Y14
GPMC0_A11	OZ	GPMC address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA4, U12	T3, W11
GPMC0_A12	OZ	GPMC address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	P2, V14	E4, Y16
GPMC0_A13	OZ	GPMC address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	P3, W14	D2, U13
GPMC0_A14	OZ	GPMC address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA10, AA3	K1, Y6

**Table 6-53. GPMC0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
GPMC0_A15	OZ	GPMC address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	R6, V10	AA8, N1
GPMC0_A16	OZ	GPMC address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	T5, U10	N4, Y9
GPMC0_A17	OZ	GPMC address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	AA11, U1	E1, W9
GPMC0_A18	OZ	GPMC address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	T4, Y11	L2, V9
GPMC0_A19	OZ	GPMC address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	R5, Y10	F5, Y8
GPMC0_A20	OZ	GPMC address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	R21	
GPMC0_A21	OZ	GPMC address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	Y18	
GPMC0_A22	OZ	GPMC address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	N16	
GPMC0_AD0	IO	GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode	T20	R21
GPMC0_AD1	IO	GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode	U21	R20
GPMC0_AD2	IO	GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	T18	T19
GPMC0_AD3	IO	GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode	U20	V21
GPMC0_AD4	IO	GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode	U18	U21
GPMC0_AD5	IO	GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode	U19	T20
GPMC0_AD6	IO	GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode	V20	T18
GPMC0_AD7	IO	GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode	V21	U19
GPMC0_AD8	IO	GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode	V19	U18

**Table 6-53. GPMC0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
GPMC0_AD9	IO	GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode	T17	U20
GPMC0_AD10	IO	GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode	R16	V20
GPMC0_AD11	IO	GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode	W20	W20
GPMC0_AD12	IO	GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode	W21	Y20
GPMC0_AD13	IO	GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode	V18	Y19
GPMC0_AD14	IO	GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode	Y21	Y18
GPMC0_AD15	IO	GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode	Y20	AA19
GPMC0_AD16	IO	GPMC Data 16 Input/Output in A/D non-multiplexed mode and additionally Address 17 Output in A/D multiplexed mode	Y7	V4
GPMC0_AD17	IO	GPMC Data 17 Input/Output in A/D non-multiplexed mode and additionally Address 18 Output in A/D multiplexed mode	U8	W5
GPMC0_AD18	IO	GPMC Data 18 Input/Output in A/D non-multiplexed mode and additionally Address 19 Output in A/D multiplexed mode	W8	AA4
GPMC0_AD19	IO	GPMC Data 19 Input/Output in A/D non-multiplexed mode and additionally Address 20 Output in A/D multiplexed mode	V8	Y5
GPMC0_AD20	IO	GPMC Data 20 Input/Output in A/D non-multiplexed mode and additionally Address 21 Output in A/D multiplexed mode	Y8	AA5
GPMC0_AD21	IO	GPMC Data 21 Input/Output in A/D non-multiplexed mode and additionally Address 22 Output in A/D multiplexed mode	V13	U14
GPMC0_AD22	IO	GPMC Data 22 Input/Output in A/D non-multiplexed mode and additionally Address 23 Output in A/D multiplexed mode	AA7	Y2
GPMC0_AD23	IO	GPMC Data 23 Input/Output in A/D non-multiplexed mode and additionally Address 24 Output in A/D multiplexed mode	U13	V13

**Table 6-53. GPMC0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
GPMC0_AD24	IO	GPMC Data 24 Input/Output in A/D non-multiplexed mode and additionally Address 25 Output in A/D multiplexed mode	W13	Y13
GPMC0_AD25	IO	GPMC Data 25 Input/Output in A/D non-multiplexed mode and additionally Address 26 Output in A/D multiplexed mode	U15	W16
GPMC0_AD26	IO	GPMC Data 26 Input/Output in A/D non-multiplexed mode and additionally Address 27 Output in A/D multiplexed mode	U14	W13
GPMC0_AD27	IO	GPMC Data 27 Input/Output in A/D non-multiplexed mode and additionally Address 28 Output in A/D multiplexed mode	AA8	V5
GPMC0_AD28	IO	GPMC Data 28 Input/Output in A/D non-multiplexed mode and additionally Address 29 Output in A/D multiplexed mode	U9	W2
GPMC0_AD29	IO	GPMC Data 29 Input/Output in A/D non-multiplexed mode and additionally Address 30 Output in A/D multiplexed mode	W9	V6
GPMC0_AD30	IO	GPMC Data 30 Input/Output in A/D non-multiplexed mode and additionally Address 31 Output in A/D multiplexed mode	AA9	AA7
GPMC0_AD31	IO	GPMC Data 31 Input/Output in A/D non-multiplexed mode and additionally Address 0 Output in A/D multiplexed mode	Y9	Y7
GPMC0_BE0n_CLE	O	GPMC Lower-Byte Enable (active low) or Command Latch Enable	P17	
GPMC0_BE1n	O	GPMC Upper-Byte Enable (active low)	T19	P21
GPMC0_BE2n	O	GPMC Upper-Byte Enable (active low)	V9	W6
GPMC0_BE3n	O	GPMC Upper-Byte Enable (active low)	AA14	AA14
GPMC0_CS0n	O	GPMC Chip Select 0 (active low)	R19	
GPMC0_CS1n	O	GPMC Chip Select 1 (active low)	R20	
GPMC0_CS2n	O	GPMC Chip Select 2 (active low)	P19	
GPMC0_CS3n	O	GPMC Chip Select 3 (active low)	R21	
GPMC0_WAIT0	I	GPMC External Indication of Wait	W19	
GPMC0_WAIT1	I	GPMC External Indication of Wait	Y18	

**ADVANCE INFORMATION**

#### 6.4.16 MMC

##### MAIN Domain Instances

##### 6.4.16.1 MMC0 Signal Descriptions

**Table 6-54. MMC0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MMC0_CALPAD	A	MMC/SD/SDIO Calibration Resistor	F18	

**Table 6-54. MMC0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MMC0_CLK	IO	MMC/SD/SDIO Clock	G18	
MMC0_CMD	IO	MMC/SD/SDIO Command	J21	
MMC0_DS	IO	MMC Data Strobe	G19	
MMC0_DAT0	IO	MMC/SD/SDIO Data	K20	
MMC0_DAT1	IO	MMC/SD/SDIO Data	J20	
MMC0_DAT2	IO	MMC/SD/SDIO Data	J18	
MMC0_DAT3	IO	MMC/SD/SDIO Data	J17	
MMC0_DAT4	IO	MMC/SD/SDIO Data	H17	
MMC0_DAT5	IO	MMC/SD/SDIO Data	H19	
MMC0_DAT6	IO	MMC/SD/SDIO Data	H18	
MMC0_DAT7	IO	MMC/SD/SDIO Data	G17	

**6.4.16.2 MMC1 Signal Descriptions****Table 6-55. MMC1 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MMC1_CLK	IO	MMC/SD/SDIO Clock	L20	J20
MMC1_CMD	IO	MMC/SD/SDIO Command	J19	J21
MMC1_SDCD	I	SD Card Detect	D19	B17
MMC1_SDWP	I	SD Write Protect	C20	C16
MMC1_DAT0	IO	MMC/SD/SDIO Data	K21	J18
MMC1_DAT1	IO	MMC/SD/SDIO Data	L21	J19
MMC1_DAT2	IO	MMC/SD/SDIO Data	K19	K20
MMC1_DAT3	IO	MMC/SD/SDIO Data	K18	K18

**6.4.17 FSITX****MAIN Domain Instances****6.4.17.1 FSI0 TX Signal Descriptions****Table 6-56. FSI0 TX Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
FSI_TX0_CLK	O	FSI Clock	T19	P21
FSI_TX0_D0	O	FSI Data	Y21	Y18
FSI_TX0_D1	O	FSI Data	Y20	AA19



### 6.4.17.2 FSI1 TX Signal Descriptions

**Table 6-57. FSI1 TX Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
FSI_TX1_CLK	O	FSI Clock	N16	
FSI_TX1_D0	O	FSI Data	P17	
FSI_TX1_D1	O	FSI Data	Y18	

### 6.4.18 FSIRX

#### MAIN Domain Instances

#### 6.4.18.1 FSI0 RX Signal Descriptions

**Table 6-58. FSI0 RX Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
FSI_RX0_CLK	I	FSI Clock	V19	U18
FSI_RX0_D0	I	FSI Data	T17	U20
FSI_RX0_D1	I	FSI Data	R16	V20

#### 6.4.18.2 FSI1 RX Signal Descriptions

**Table 6-59. FSI1 RX Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
FSI_RX1_CLK	I	FSI Clock	W20	W20
FSI_RX1_D0	I	FSI Data	W21	Y20
FSI_RX1_D1	I	FSI Data	V18	Y19

#### 6.4.18.3 FSI2 RX Signal Descriptions

**Table 6-60. FSI2 RX Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
FSI_RX2_CLK	I	FSI Clock	T20	R21
FSI_RX2_D0	I	FSI Data	U21	R20
FSI_RX2_D1	I	FSI Data	T18	T19

#### 6.4.18.4 FSI3 RX Signal Descriptions

**Table 6-61. FSI3 RX Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
FSI_RX3_CLK	I	FSI Clock	U20	V21
FSI_RX3_D0	I	FSI Data	U18	U21
FSI_RX3_D1	I	FSI Data	U19	T20

### 6.4.18.5 FSI4 RX Signal Descriptions

**Table 6-62. FSI4 RX Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
FSI_RX4_CLK	I	FSI Clock	R17	
FSI_RX4_D0	I	FSI Data	V20	T18
FSI_RX4_D1	I	FSI Data	V21	U19

### 6.4.18.6 FSI5 RX Signal Descriptions

**Table 6-63. FSI5 RX Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
FSI_RX5_CLK	I	FSI Clock	P16	
FSI_RX5_D0	I	FSI Data	R18	
FSI_RX5_D1	I	FSI Data	T21	

### 6.4.19 CPTS

#### MAIN Domain Instances

#### 6.4.19.1 CPTS0 Signal Descriptions

**Table 6-64. CPTS0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
CPTS0_RFT_CLK	I	CPTS Reference Clock	D18	
CPTS0_TS_COMP	O	CPTS Time Stamp Counter Compare	C13, W1, W7	B7, G2, U3
CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit	D14, U1, U7	E1, T2
CPTS0_HW1TSPUSH	I	CPTS Hardware Time Stamp Push 1	C18, V1, V7	A17, K4, Y4
CPTS0_HW2TSPUSH	I	CPTS Hardware Time Stamp Push 2	B19, T1, U13	B18, E2, V13

#### 6.4.19.2 CP GEMAC CPTS0 Signal Descriptions

**Table 6-65. CP GEMAC CPTS0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
CP_GEMAC_CPTS0_RFT_CLK	I	CPTS Reference Clock	D18	
CP_GEMAC_CPTS0_TS_COMP	O	CPTS Time Stamp Counter Compare	E15, K18, W1	B12, G2, K18
CP_GEMAC_CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit	B16, D16, K19, U1	B9, C11, E1, K20
CP_GEMAC_CPTS0_HW1TSPUSH	I	CPTS Hardware Time Stamp Push 1	E14, L21, V1	A12, J19, K4
CP_GEMAC_CPTS0_HW2TSPUSH	I	CPTS Hardware Time Stamp Push 2	E16, K21, T1	A11, E2, J18

## 6.4.20 ICSSG

### MAIN Domain Instances

#### 6.4.20.1 PRU\_ICSSG0 Signal Descriptions

**Table 6-66. PRU\_ICSSG0 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PRG0_ECAP0_IN_APWM_OUT	IO	PRU-ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	R2, U5	F3, M4
PRG0_ECAP0_SYNC_IN	I	PRU-ICSSG ECAP Sync Input	P5, V5	D1, T1
PRG0_ECAP0_SYNC_OUT	O	PRU-ICSSG ECAP Sync Output	AA4, V5	T1, T3
PRG0_IEP0_EDIO_OUTVALID	O	PRU_ICSSG Industrial Ethernet Digital I/O Outvalid	C13	B7
PRG0_IEP0_EDC_LATCH_IN0	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	V1	K4
PRG0_IEP0_EDC_LATCH_IN1	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	T1	E2
PRG0_IEP0_EDC_SYNC_OUT0	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	W1	G2
PRG0_IEP0_EDC_SYNC_OUT1	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	U1	E1
PRG0_IEP0_EDIO_DATA_IN_OUT28	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	W6	Y3
PRG0_IEP0_EDIO_DATA_IN_OUT29	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	AA5	U1
PRG0_IEP0_EDIO_DATA_IN_OUT30	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	Y5	R2
PRG0_IEP0_EDIO_DATA_IN_OUT31	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	V6	U2
PRG0_IEP1_EDC_LATCH_IN0	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	P5	D1
PRG0_IEP1_EDC_LATCH_IN1	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	W5	T5
PRG0_IEP1_EDC_SYNC_OUT0	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	R2	F3
PRG0_IEP1_EDC_SYNC_OUT1	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	V5	T1
PRG0_MDIO0_MDC	O	PRU-ICSSG MDIO Clock	P3	D2
PRG0_MDIO0_MDIO	IO	PRU-ICSSG MDIO Data	P2	E4
PRG0_PRU0_GPI0	I	PRU-ICSSG PRU Data Input	Y1	J3
PRG0_PRU0_GPI1	I	PRU-ICSSG PRU Data Input	R4	J4
PRG0_PRU0_GPI2	I	PRU-ICSSG PRU Data Input	U2	G1
PRG0_PRU0_GPI3	I	PRU-ICSSG PRU Data Input	V2	H1
PRG0_PRU0_GPI4	I	PRU-ICSSG PRU Data Input	AA2	K2
PRG0_PRU0_GPI5	I	PRU-ICSSG PRU Data Input	R3	F2

**Table 6-66. PRU\_ICSSG0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PRG0_PRU0_GPI6	I	PRU-ICSSG PRU Data Input	T3	H2
PRG0_PRU0_GPI7	I	PRU-ICSSG PRU Data Input	T1	E2
PRG0_PRU0_GPI8	I	PRU-ICSSG PRU Data Input	T2	H5
PRG0_PRU0_GPI9	I	PRU-ICSSG PRU Data Input	W6	Y3
PRG0_PRU0_GPI10	I	PRU-ICSSG PRU Data Input	AA5	U1
PRG0_PRU0_GPI11	I	PRU-ICSSG PRU Data Input	Y3	L1
PRG0_PRU0_GPI12	I	PRU-ICSSG PRU Data Input	AA3	K1
PRG0_PRU0_GPI13	I	PRU-ICSSG PRU Data Input	R6	N1
PRG0_PRU0_GPI14	I	PRU-ICSSG PRU Data Input	V4	N2
PRG0_PRU0_GPI15	I	PRU-ICSSG PRU Data Input	T5	N4
PRG0_PRU0_GPI16	I	PRU-ICSSG PRU Data Input	U4	N3
PRG0_PRU0_GPI17	I	PRU-ICSSG PRU Data Input	U1	E1
PRG0_PRU0_GPI18	I	PRU-ICSSG PRU Data Input	V1	K4
PRG0_PRU0_GPI19	I	PRU-ICSSG PRU Data Input	W1	G2
PRG0_PRU0_GPO0	IO	PRU-ICSSG PRU Data Output	Y1	J3
PRG0_PRU0_GPO1	IO	PRU-ICSSG PRU Data Output	R4	J4
PRG0_PRU0_GPO2	IO	PRU-ICSSG PRU Data Output	U2	G1
PRG0_PRU0_GPO3	IO	PRU-ICSSG PRU Data Output	V2	H1
PRG0_PRU0_GPO4	IO	PRU-ICSSG PRU Data Output	AA2	K2
PRG0_PRU0_GPO5	IO	PRU-ICSSG PRU Data Output	R3	F2
PRG0_PRU0_GPO6	IO	PRU-ICSSG PRU Data Output	T3	H2
PRG0_PRU0_GPO7	IO	PRU-ICSSG PRU Data Output	T1	E2
PRG0_PRU0_GPO8	IO	PRU-ICSSG PRU Data Output	T2	H5
PRG0_PRU0_GPO9	IO	PRU-ICSSG PRU Data Output	W6	Y3
PRG0_PRU0_GPO10	IO	PRU-ICSSG PRU Data Output	AA5	U1
PRG0_PRU0_GPO11	IO	PRU-ICSSG PRU Data Output	Y3	L1
PRG0_PRU0_GPO12	IO	PRU-ICSSG PRU Data Output	AA3	K1
PRG0_PRU0_GPO13	IO	PRU-ICSSG PRU Data Output	R6	N1
PRG0_PRU0_GPO14	IO	PRU-ICSSG PRU Data Output	V4	N2
PRG0_PRU0_GPO15	IO	PRU-ICSSG PRU Data Output	T5	N4
PRG0_PRU0_GPO16	IO	PRU-ICSSG PRU Data Output	U4	N3
PRG0_PRU0_GPO17	IO	PRU-ICSSG PRU Data Output	U1	E1
PRG0_PRU0_GPO18	IO	PRU-ICSSG PRU Data Output	V1	K4
PRG0_PRU0_GPO19	IO	PRU-ICSSG PRU Data Output	W1	G2
PRG0_PRU1_GPI0	I	PRU-ICSSG PRU Data Input	Y2	L5
PRG0_PRU1_GPI1	I	PRU-ICSSG PRU Data Input	W2	J2
PRG0_PRU1_GPI2	I	PRU-ICSSG PRU Data Input	V3	M2
PRG0_PRU1_GPI3	I	PRU-ICSSG PRU Data Input	T4	L2

**Table 6-66. PRU\_ICSSG0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PRG0_PRU1_GPI4	I	PRU-ICSSG PRU Data Input	W3	L3
PRG0_PRU1_GPI5	I	PRU-ICSSG PRU Data Input	P4	E3
PRG0_PRU1_GPI6	I	PRU-ICSSG PRU Data Input	R5	F5
PRG0_PRU1_GPI7	I	PRU-ICSSG PRU Data Input	W5	T5
PRG0_PRU1_GPI8	I	PRU-ICSSG PRU Data Input	R1	F4
PRG0_PRU1_GPI9	I	PRU-ICSSG PRU Data Input	Y5	R2
PRG0_PRU1_GPI10	I	PRU-ICSSG PRU Data Input	V6	U2
PRG0_PRU1_GPI11	I	PRU-ICSSG PRU Data Input	W4	P1
PRG0_PRU1_GPI12	I	PRU-ICSSG PRU Data Input	Y4	P2
PRG0_PRU1_GPI13	I	PRU-ICSSG PRU Data Input	T6	T4
PRG0_PRU1_GPI14	I	PRU-ICSSG PRU Data Input	U6	R5
PRG0_PRU1_GPI15	I	PRU-ICSSG PRU Data Input	U5	M4
PRG0_PRU1_GPI16	I	PRU-ICSSG PRU Data Input	AA4	T3
PRG0_PRU1_GPI17	I	PRU-ICSSG PRU Data Input	V5	T1
PRG0_PRU1_GPI18	I	PRU-ICSSG PRU Data Input	P5	D1
PRG0_PRU1_GPI19	I	PRU-ICSSG PRU Data Input	R2	F3
PRG0_PRU1_GPO0	IO	PRU-ICSSG PRU Data Output	Y2	L5
PRG0_PRU1_GPO1	IO	PRU-ICSSG PRU Data Output	W2	J2
PRG0_PRU1_GPO2	IO	PRU-ICSSG PRU Data Output	V3	M2
PRG0_PRU1_GPO3	IO	PRU-ICSSG PRU Data Output	T4	L2
PRG0_PRU1_GPO4	IO	PRU-ICSSG PRU Data Output	W3	L3
PRG0_PRU1_GPO5	IO	PRU-ICSSG PRU Data Output	P4	E3
PRG0_PRU1_GPO6	IO	PRU-ICSSG PRU Data Output	R5	F5
PRG0_PRU1_GPO7	IO	PRU-ICSSG PRU Data Output	W5	T5
PRG0_PRU1_GPO8	IO	PRU-ICSSG PRU Data Output	R1	F4
PRG0_PRU1_GPO9	IO	PRU-ICSSG PRU Data Output	Y5	R2
PRG0_PRU1_GPO10	IO	PRU-ICSSG PRU Data Output	V6	U2
PRG0_PRU1_GPO11	IO	PRU-ICSSG PRU Data Output	W4	P1
PRG0_PRU1_GPO12	IO	PRU-ICSSG PRU Data Output	Y4	P2
PRG0_PRU1_GPO13	IO	PRU-ICSSG PRU Data Output	T6	T4
PRG0_PRU1_GPO14	IO	PRU-ICSSG PRU Data Output	U6	R5
PRG0_PRU1_GPO15	IO	PRU-ICSSG PRU Data Output	U5	M4
PRG0_PRU1_GPO16	IO	PRU-ICSSG PRU Data Output	AA4	T3
PRG0_PRU1_GPO17	IO	PRU-ICSSG PRU Data Output	V5	T1
PRG0_PRU1_GPO18	IO	PRU-ICSSG PRU Data Output	P5	D1
PRG0_PRU1_GPO19	IO	PRU-ICSSG PRU Data Output	R2	F3
PRG0_PWM0_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	V1	K4
PRG0_PWM0_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	W1	G2

**Table 6-66. PRU\_ICSSG0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PRG0_PWM1_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	P5	D1
PRG0_PWM1_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	R2	F3
PRG0_PWM2_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	T18, V6	T19, U2
PRG0_PWM2_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	R1, U21	F4, R20
PRG0_PWM3_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	P16, W6	Y3
PRG0_PWM3_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	R17, Y3	L1
PRG0_PWM0_A0	IO	PRU_ICSSG PWM Output A	AA3	K1
PRG0_PWM0_A1	IO	PRU_ICSSG PWM Output A	V4	N2
PRG0_PWM0_A2	IO	PRU_ICSSG PWM Output A	U4	N3
PRG0_PWM0_B0	IO	PRU_ICSSG PWM Output B	R6	N1
PRG0_PWM0_B1	IO	PRU_ICSSG PWM Output B	T5	N4
PRG0_PWM0_B2	IO	PRU_ICSSG PWM Output B	U1	E1
PRG0_PWM1_A0	IO	PRU_ICSSG PWM Output A	Y4	P2
PRG0_PWM1_A1	IO	PRU_ICSSG PWM Output A	U6	R5
PRG0_PWM1_A2	IO	PRU_ICSSG PWM Output A	AA4	T3
PRG0_PWM1_B0	IO	PRU_ICSSG PWM Output B	T6	T4
PRG0_PWM1_B1	IO	PRU_ICSSG PWM Output B	U5	M4
PRG0_PWM1_B2	IO	PRU_ICSSG PWM Output B	V5	T1
PRG0_PWM2_A0	IO	PRU_ICSSG PWM Output A	U2, U20	G1, V21
PRG0_PWM2_A1	IO	PRU_ICSSG PWM Output A	T2, U19	H5, T20
PRG0_PWM2_A2	IO	PRU_ICSSG PWM Output A	V19, V3	M2, U18
PRG0_PWM2_B0	IO	PRU_ICSSG PWM Output B	AA2, U18	K2, U21
PRG0_PWM2_B1	IO	PRU_ICSSG PWM Output B	AA5, V20	T18, U1
PRG0_PWM2_B2	IO	PRU_ICSSG PWM Output B	T17, W3	L3, U20
PRG0_PWM3_A0	IO	PRU_ICSSG PWM Output A	V18, Y1	J3, Y19
PRG0_PWM3_A1	IO	PRU_ICSSG PWM Output A	R18, T3	H2
PRG0_PWM3_A2	IO	PRU_ICSSG PWM Output A	T19, V2	H1, P21
PRG0_PWM3_B0	IO	PRU_ICSSG PWM Output B	R4, Y21	J4, Y18
PRG0_PWM3_B1	IO	PRU_ICSSG PWM Output B	T1, T21	E2
PRG0_PWM3_B2	IO	PRU_ICSSG PWM Output B	R3, W19	F2
PRG0_RGMII1_RXC	I	PRU_ICSSG RGMII Receive Clock	T3	H2
PRG0_RGMII1_RX_CTL	I	PRU_ICSSG RGMII Receive Control	AA2	K2
PRG0_RGMII1_TXC	IO	PRU_ICSSG RGMII Transmit Clock	U4	N3
PRG0_RGMII1_TX_CTL	O	PRU_ICSSG RGMII Transmit Control	T5	N4
PRG0_RGMII2_RXC	I	PRU_ICSSG RGMII Receive Clock	R5	F5
PRG0_RGMII2_RX_CTL	I	PRU_ICSSG RGMII Receive Control	W3	L3
PRG0_RGMII2_TXC	IO	PRU_ICSSG RGMII Transmit Clock	AA4	T3
PRG0_RGMII2_TX_CTL	O	PRU_ICSSG RGMII Transmit Control	U5	M4

**Table 6-66. PRU\_ICSSG0 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PRG0_RGMII1_RD0	I	PRU_ICSSG RGMII Receive Data	Y1	J3
PRG0_RGMII1_RD1	I	PRU_ICSSG RGMII Receive Data	R4	J4
PRG0_RGMII1_RD2	I	PRU_ICSSG RGMII Receive Data	U2	G1
PRG0_RGMII1_RD3	I	PRU_ICSSG RGMII Receive Data	V2	H1
PRG0_RGMII1_TD0	O	PRU_ICSSG RGMII Transmit Data	Y3	L1
PRG0_RGMII1_TD1	O	PRU_ICSSG RGMII Transmit Data	AA3	K1
PRG0_RGMII1_TD2	O	PRU_ICSSG RGMII Transmit Data	R6	N1
PRG0_RGMII1_TD3	O	PRU_ICSSG RGMII Transmit Data	V4	N2
PRG0_RGMII2_RD0	I	PRU_ICSSG RGMII Receive Data	Y2	L5
PRG0_RGMII2_RD1	I	PRU_ICSSG RGMII Receive Data	W2	J2
PRG0_RGMII2_RD2	I	PRU_ICSSG RGMII Receive Data	V3	M2
PRG0_RGMII2_RD3	I	PRU_ICSSG RGMII Receive Data	T4	L2
PRG0_RGMII2_TD0	O	PRU_ICSSG RGMII Transmit Data	W4	P1
PRG0_RGMII2_TD1	O	PRU_ICSSG RGMII Transmit Data	Y4	P2
PRG0_RGMII2_TD2	O	PRU_ICSSG RGMII Transmit Data	T6	T4
PRG0_RGMII2_TD3	O	PRU_ICSSG RGMII Transmit Data	U6	R5
PRG0_UART0_CTSn	I	PRU-ICSSG UART Clear to Send (active low)	W6	Y3
PRG0_UART0_RTSn	O	PRU-ICSSG UART Request to Send (active low)	AA5	U1
PRG0_UART0_RXD	I	PRU-ICSSG UART Receive Data	Y5	R2
PRG0_UART0_TXD	O	PRU-ICSSG UART Transmit Data	V6	U2

**6.4.20.2 PRU\_ICSSG1 Signal Descriptions**

**Table 6-67. PRU\_ICSSG1 Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PRG1_ECAP0_IN_APWM_OUT	IO	PRU-ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output	V12	AA13
PRG1_ECAP0_SYNC_IN	I	PRU-ICSSG ECAP Sync Input	Y13	Y15
PRG1_ECAP0_SYNC_OUT	O	PRU-ICSSG ECAP Sync Output	AA14	AA14
PRG1_IEP0_EDIO_OUTVALID	O	PRU_ICSSG Industrial Ethernet Digital I/O Outvalid	D14	
PRG1_IEP0_EDC_LATCH_IN0	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	V7	Y4
PRG1_IEP0_EDC_LATCH_IN1	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	U13	V13
PRG1_IEP0_EDC_SYNC_OUT0	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	W7	U3
PRG1_IEP0_EDC_SYNC_OUT1	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	U7	T2

**Table 6-67. PRU\_ICSSG1 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PRG1_IEP0_EDIO_DATA_IN_OUT28	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	U15	W16
PRG1_IEP0_EDIO_DATA_IN_OUT29	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	U14	W13
PRG1_IEP0_EDIO_DATA_IN_OUT30	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	V14	Y16
PRG1_IEP0_EDIO_DATA_IN_OUT31	IO	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/Output	W14	U13
PRG1_IEP1_EDC_LATCH_IN0	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	Y13	Y15
PRG1_IEP1_EDC_LATCH_IN1	I	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	V15	Y14
PRG1_IEP1_EDC_SYNC_OUT0	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	V12	AA13
PRG1_IEP1_EDC_SYNC_OUT1	O	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	AA14	AA14
PRG1_MDIO0_MDC	O	PRU-ICSSG MDIO Clock	Y6	W1
PRG1_MDIO0_MDIO	IO	PRU-ICSSG MDIO Data	AA6	V2
PRG1_PRU0_GPI0	I	PRU-ICSSG PRU Data Input	Y7	V4
PRG1_PRU0_GPI1	I	PRU-ICSSG PRU Data Input	U8	W5
PRG1_PRU0_GPI2	I	PRU-ICSSG PRU Data Input	W8	AA4
PRG1_PRU0_GPI3	I	PRU-ICSSG PRU Data Input	V8	Y5
PRG1_PRU0_GPI4	I	PRU-ICSSG PRU Data Input	Y8	AA5
PRG1_PRU0_GPI5	I	PRU-ICSSG PRU Data Input	V13	U14
PRG1_PRU0_GPI6	I	PRU-ICSSG PRU Data Input	AA7	Y2
PRG1_PRU0_GPI7	I	PRU-ICSSG PRU Data Input	U13	V13
PRG1_PRU0_GPI8	I	PRU-ICSSG PRU Data Input	W13	Y13
PRG1_PRU0_GPI9	I	PRU-ICSSG PRU Data Input	U15	W16
PRG1_PRU0_GPI10	I	PRU-ICSSG PRU Data Input	U14	W13
PRG1_PRU0_GPI11	I	PRU-ICSSG PRU Data Input	AA8	V5
PRG1_PRU0_GPI12	I	PRU-ICSSG PRU Data Input	U9	W2
PRG1_PRU0_GPI13	I	PRU-ICSSG PRU Data Input	W9	V6
PRG1_PRU0_GPI14	I	PRU-ICSSG PRU Data Input	AA9	AA7
PRG1_PRU0_GPI15	I	PRU-ICSSG PRU Data Input	Y9	Y7
PRG1_PRU0_GPI16	I	PRU-ICSSG PRU Data Input	V9	W6
PRG1_PRU0_GPI17	I	PRU-ICSSG PRU Data Input	U7	T2
PRG1_PRU0_GPI18	I	PRU-ICSSG PRU Data Input	V7	Y4
PRG1_PRU0_GPI19	I	PRU-ICSSG PRU Data Input	W7	U3
PRG1_PRU0_GPO0	IO	PRU-ICSSG PRU Data Output	Y7	V4
PRG1_PRU0_GPO1	IO	PRU-ICSSG PRU Data Output	U8	W5



**Table 6-67. PRU\_ICSSG1 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PRG1_PRU0_GPO2	IO	PRU-ICSSG PRU Data Output	W8	AA4
PRG1_PRU0_GPO3	IO	PRU-ICSSG PRU Data Output	V8	Y5
PRG1_PRU0_GPO4	IO	PRU-ICSSG PRU Data Output	Y8	AA5
PRG1_PRU0_GPO5	IO	PRU-ICSSG PRU Data Output	V13	U14
PRG1_PRU0_GPO6	IO	PRU-ICSSG PRU Data Output	AA7	Y2
PRG1_PRU0_GPO7	IO	PRU-ICSSG PRU Data Output	U13	V13
PRG1_PRU0_GPO8	IO	PRU-ICSSG PRU Data Output	W13	Y13
PRG1_PRU0_GPO9	IO	PRU-ICSSG PRU Data Output	U15	W16
PRG1_PRU0_GPO10	IO	PRU-ICSSG PRU Data Output	U14	W13
PRG1_PRU0_GPO11	IO	PRU-ICSSG PRU Data Output	AA8	V5
PRG1_PRU0_GPO12	IO	PRU-ICSSG PRU Data Output	U9	W2
PRG1_PRU0_GPO13	IO	PRU-ICSSG PRU Data Output	W9	V6
PRG1_PRU0_GPO14	IO	PRU-ICSSG PRU Data Output	AA9	AA7
PRG1_PRU0_GPO15	IO	PRU-ICSSG PRU Data Output	Y9	Y7
PRG1_PRU0_GPO16	IO	PRU-ICSSG PRU Data Output	V9	W6
PRG1_PRU0_GPO17	IO	PRU-ICSSG PRU Data Output	U7	T2
PRG1_PRU0_GPO18	IO	PRU-ICSSG PRU Data Output	V7	Y4
PRG1_PRU0_GPO19	IO	PRU-ICSSG PRU Data Output	W7	U3
PRG1_PRU1_GPI0	I	PRU-ICSSG PRU Data Input	W11	AA10
PRG1_PRU1_GPI1	I	PRU-ICSSG PRU Data Input	V11	Y10
PRG1_PRU1_GPI2	I	PRU-ICSSG PRU Data Input	AA12	Y11
PRG1_PRU1_GPI3	I	PRU-ICSSG PRU Data Input	Y12	V12
PRG1_PRU1_GPI4	I	PRU-ICSSG PRU Data Input	W12	Y12
PRG1_PRU1_GPI5	I	PRU-ICSSG PRU Data Input	AA13	AA11
PRG1_PRU1_GPI6	I	PRU-ICSSG PRU Data Input	U11	V10
PRG1_PRU1_GPI7	I	PRU-ICSSG PRU Data Input	V15	Y14
PRG1_PRU1_GPI8	I	PRU-ICSSG PRU Data Input	U12	W11
PRG1_PRU1_GPI9	I	PRU-ICSSG PRU Data Input	V14	Y16
PRG1_PRU1_GPI10	I	PRU-ICSSG PRU Data Input	W14	U13
PRG1_PRU1_GPI11	I	PRU-ICSSG PRU Data Input	AA10	Y6
PRG1_PRU1_GPI12	I	PRU-ICSSG PRU Data Input	V10	AA8
PRG1_PRU1_GPI13	I	PRU-ICSSG PRU Data Input	U10	Y9
PRG1_PRU1_GPI14	I	PRU-ICSSG PRU Data Input	AA11	W9
PRG1_PRU1_GPI15	I	PRU-ICSSG PRU Data Input	Y11	V9
PRG1_PRU1_GPI16	I	PRU-ICSSG PRU Data Input	Y10	Y8
PRG1_PRU1_GPI17	I	PRU-ICSSG PRU Data Input	AA14	AA14
PRG1_PRU1_GPI18	I	PRU-ICSSG PRU Data Input	Y13	Y15
PRG1_PRU1_GPI19	I	PRU-ICSSG PRU Data Input	V12	AA13

**ADVANCE INFORMATION**

Table 6-67. PRU\_ICSSG1 Signal Descriptions (continued)

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PRG1_PRU1_GPO0	IO	PRU-ICSSG PRU Data Output	W11	AA10
PRG1_PRU1_GPO1	IO	PRU-ICSSG PRU Data Output	V11	Y10
PRG1_PRU1_GPO2	IO	PRU-ICSSG PRU Data Output	AA12	Y11
PRG1_PRU1_GPO3	IO	PRU-ICSSG PRU Data Output	Y12	V12
PRG1_PRU1_GPO4	IO	PRU-ICSSG PRU Data Output	W12	Y12
PRG1_PRU1_GPO5	IO	PRU-ICSSG PRU Data Output	AA13	AA11
PRG1_PRU1_GPO6	IO	PRU-ICSSG PRU Data Output	U11	V10
PRG1_PRU1_GPO7	IO	PRU-ICSSG PRU Data Output	V15	Y14
PRG1_PRU1_GPO8	IO	PRU-ICSSG PRU Data Output	U12	W11
PRG1_PRU1_GPO9	IO	PRU-ICSSG PRU Data Output	V14	Y16
PRG1_PRU1_GPO10	IO	PRU-ICSSG PRU Data Output	W14	U13
PRG1_PRU1_GPO11	IO	PRU-ICSSG PRU Data Output	AA10	Y6
PRG1_PRU1_GPO12	IO	PRU-ICSSG PRU Data Output	V10	AA8
PRG1_PRU1_GPO13	IO	PRU-ICSSG PRU Data Output	U10	Y9
PRG1_PRU1_GPO14	IO	PRU-ICSSG PRU Data Output	AA11	W9
PRG1_PRU1_GPO15	IO	PRU-ICSSG PRU Data Output	Y11	V9
PRG1_PRU1_GPO16	IO	PRU-ICSSG PRU Data Output	Y10	Y8
PRG1_PRU1_GPO17	IO	PRU-ICSSG PRU Data Output	AA14	AA14
PRG1_PRU1_GPO18	IO	PRU-ICSSG PRU Data Output	Y13	Y15
PRG1_PRU1_GPO19	IO	PRU-ICSSG PRU Data Output	V12	AA13
PRG1_PWM0_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	V7	Y4
PRG1_PWM0_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	W7	U3
PRG1_PWM1_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	Y13	Y15
PRG1_PWM1_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	V12	AA13
PRG1_PWM2_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	P19, W14	U13
PRG1_PWM2_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	R20, U12	W11
PRG1_PWM3_TZ_IN	I	PRU_ICSSG PWM Trip Zone Input	U15	W16
PRG1_PWM3_TZ_OUT	O	PRU_ICSSG PWM Trip Zone Output	AA8	V5
PRG1_PWM0_A0	IO	PRU_ICSSG PWM Output A	U9	W2
PRG1_PWM0_A1	IO	PRU_ICSSG PWM Output A	AA9	AA7
PRG1_PWM0_A2	IO	PRU_ICSSG PWM Output A	V9	W6
PRG1_PWM0_B0	IO	PRU_ICSSG PWM Output B	W9	V6
PRG1_PWM0_B1	IO	PRU_ICSSG PWM Output B	Y9	Y7
PRG1_PWM0_B2	IO	PRU_ICSSG PWM Output B	U7	T2
PRG1_PWM1_A0	IO	PRU_ICSSG PWM Output A	V10	AA8
PRG1_PWM1_A1	IO	PRU_ICSSG PWM Output A	AA11	W9
PRG1_PWM1_A2	IO	PRU_ICSSG PWM Output A	Y10	Y8
PRG1_PWM1_B0	IO	PRU_ICSSG PWM Output B	U10	Y9

**Table 6-67. PRU\_ICSSG1 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PRG1_PWM1_B1	IO	PRU_ICSSG PWM Output B	Y11	V9
PRG1_PWM1_B2	IO	PRU_ICSSG PWM Output B	AA14	AA14
PRG1_PWM2_A0	IO	PRU_ICSSG PWM Output A	N16, W8	AA4
PRG1_PWM2_A1	IO	PRU_ICSSG PWM Output A	P17, W13	Y13
PRG1_PWM2_A2	IO	PRU_ICSSG PWM Output A	AA12, V21	U19, Y11
PRG1_PWM2_B0	IO	PRU_ICSSG PWM Output B	N17, Y8	AA5
PRG1_PWM2_B1	IO	PRU_ICSSG PWM Output B	U14, Y18	W13
PRG1_PWM2_B2	IO	PRU_ICSSG PWM Output B	R16, W12	V20, Y12
PRG1_PWM3_A0	IO	PRU_ICSSG PWM Output A	Y7	V4
PRG1_PWM3_A1	IO	PRU_ICSSG PWM Output A	AA7	Y2
PRG1_PWM3_A2	IO	PRU_ICSSG PWM Output A	V8	Y5
PRG1_PWM3_B0	IO	PRU_ICSSG PWM Output B	U8	W5
PRG1_PWM3_B1	IO	PRU_ICSSG PWM Output B	U13	V13
PRG1_PWM3_B2	IO	PRU_ICSSG PWM Output B	V13	U14
PRG1_RGMII1_RXC	I	PRU_ICSSG RGMII Receive Clock	AA7	Y2
PRG1_RGMII1_RX_CTL	I	PRU_ICSSG RGMII Receive Control	Y8	AA5
PRG1_RGMII1_TXC	IO	PRU_ICSSG RGMII Transmit Clock	V9	W6
PRG1_RGMII1_TX_CTL	O	PRU_ICSSG RGMII Transmit Control	Y9	Y7
PRG1_RGMII2_RXC	I	PRU_ICSSG RGMII Receive Clock	U11	V10
PRG1_RGMII2_RX_CTL	I	PRU_ICSSG RGMII Receive Control	W12	Y12
PRG1_RGMII2_TXC	IO	PRU_ICSSG RGMII Transmit Clock	Y10	Y8
PRG1_RGMII2_TX_CTL	O	PRU_ICSSG RGMII Transmit Control	Y11	V9
PRG1_RGMII1_RD0	I	PRU_ICSSG RGMII Receive Data	Y7	V4
PRG1_RGMII1_RD1	I	PRU_ICSSG RGMII Receive Data	U8	W5
PRG1_RGMII1_RD2	I	PRU_ICSSG RGMII Receive Data	W8	AA4
PRG1_RGMII1_RD3	I	PRU_ICSSG RGMII Receive Data	V8	Y5
PRG1_RGMII1_TD0	O	PRU_ICSSG RGMII Transmit Data	AA8	V5
PRG1_RGMII1_TD1	O	PRU_ICSSG RGMII Transmit Data	U9	W2
PRG1_RGMII1_TD2	O	PRU_ICSSG RGMII Transmit Data	W9	V6
PRG1_RGMII1_TD3	O	PRU_ICSSG RGMII Transmit Data	AA9	AA7
PRG1_RGMII2_RD0	I	PRU_ICSSG RGMII Receive Data	W11	AA10
PRG1_RGMII2_RD1	I	PRU_ICSSG RGMII Receive Data	V11	Y10
PRG1_RGMII2_RD2	I	PRU_ICSSG RGMII Receive Data	AA12	Y11
PRG1_RGMII2_RD3	I	PRU_ICSSG RGMII Receive Data	Y12	V12
PRG1_RGMII2_TD0	O	PRU_ICSSG RGMII Transmit Data	AA10	Y6
PRG1_RGMII2_TD1	O	PRU_ICSSG RGMII Transmit Data	V10	AA8
PRG1_RGMII2_TD2	O	PRU_ICSSG RGMII Transmit Data	U10	Y9
PRG1_RGMII2_TD3	O	PRU_ICSSG RGMII Transmit Data	AA11	W9

**Table 6-67. PRU\_ICSSG1 Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
PRG1_UART0_CTSn	I	PRU-ICSSG UART Clear to Send (active low)	U15	W16
PRG1_UART0_RTSn	O	PRU-ICSSG UART Request to Send (active low)	U14	W13
PRG1_UART0_RXD	I	PRU-ICSSG UART Receive Data	V14	Y16
PRG1_UART0_TXD	O	PRU-ICSSG UART Transmit Data	W14	U13

**6.4.21 DMTIMER****MAIN Domain Instances****6.4.21.1 DMTIMER Signal Descriptions****Table 6-68. DMTIMER Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	C18, K18	A17, K18
TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	B19, K19	B18, K20
TIMER_IO2	IO	Timer Inputs and Outputs (not tied to single timer instance)	A17, L21	B13, J19
TIMER_IO3	IO	Timer Inputs and Outputs (not tied to single timer instance)	B17, K21	A14, J18
TIMER_IO4	IO	Timer Inputs and Outputs (not tied to single timer instance)	C17, L20	B14, J20
TIMER_IO5	IO	Timer Inputs and Outputs (not tied to single timer instance)	D17, J19	A15, J21
TIMER_IO6	IO	Timer Inputs and Outputs (not tied to single timer instance)	B16, D19, T1	B17, B9, E2
TIMER_IO7	IO	Timer Inputs and Outputs (not tied to single timer instance)	A16, C20, U7	A9, C16, T2
TIMER_IO8	IO	Timer Inputs and Outputs (not tied to single timer instance)	P19, V7	Y4
TIMER_IO9	IO	Timer Inputs and Outputs (not tied to single timer instance)	R21, W7	U3
TIMER_IO10	IO	Timer Inputs and Outputs (not tied to single timer instance)	C13, U13	B7, V13
TIMER_IO11	IO	Timer Inputs and Outputs (not tied to single timer instance)	D14, U1	E1

## MCU Domain Instances

### 6.4.21.2 MCU\_DMTIMER Signal Descriptions

**Table 6-69. MCU\_DMTIMER Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_TIMER_IO0	IO	Timer Inputs and Outputs (not tied to single timer instance)	D8	D4
MCU_TIMER_IO1	IO	Timer Inputs and Outputs (not tied to single timer instance)	E8	C2
MCU_TIMER_IO2	IO	Timer Inputs and Outputs (not tied to single timer instance)	B8	
MCU_TIMER_IO3	IO	Timer Inputs and Outputs (not tied to single timer instance)	B9	

## 6.4.22 TRACE

### MAIN Domain Instances

#### 6.4.22.1 Trace Signal Descriptions

**Table 6-70. Trace Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
TRC_CLK	O	Trace Clock	T20	R21
TRC_CTL	O	Trace Control	U21	R20
TRC_DATA0	O	Trace Data 0	T18	T19
TRC_DATA1	O	Trace Data 1	U20	V21
TRC_DATA2	O	Trace Data 2	U18	U21
TRC_DATA3	O	Trace Data 3	U19	T20
TRC_DATA4	O	Trace Data 4	V20	T18
TRC_DATA5	O	Trace Data 5	V21	U19
TRC_DATA6	O	Trace Data 6	V19	U18
TRC_DATA7	O	Trace Data 7	T17	U20
TRC_DATA8	O	Trace Data 8	R16	V20
TRC_DATA9	O	Trace Data 9	W20	W20
TRC_DATA10	O	Trace Data 10	W21	Y20
TRC_DATA11	O	Trace Data 11	V18	Y19
TRC_DATA12	O	Trace Data 12	Y21	Y18
TRC_DATA13	O	Trace Data 13	Y20	AA19
TRC_DATA14	O	Trace Data 14	R17	
TRC_DATA15	O	Trace Data 15	P16	
TRC_DATA16	O	Trace Data 16	R18	
TRC_DATA17	O	Trace Data 17	T21	
TRC_DATA18	O	Trace Data 18	P17	
TRC_DATA19	O	Trace Data 19	T19	P21

**Table 6-70. Trace Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
TRC_DATA20	O	Trace Data 20	W19	
TRC_DATA21	O	Trace Data 21	Y18	
TRC_DATA22	O	Trace Data 22	N16	
TRC_DATA23	O	Trace Data 23	R19	

**6.4.23 JTAG****MAIN Domain Instances****6.4.23.1 JTAG Signal Descriptions****Table 6-71. JTAG Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
EMU0	IO	Emulation Control 0	D10	C5
EMU1	IO	Emulation Control 1	E10	B3
TCK	I	JTAG Test Clock Input	B11	C6
TDI	I	JTAG Test Data Input	C11	A3
TDO	OZ	JTAG Test Data Output	A12	B5
TMS	I	JTAG Test Mode Select Input	C12	B4
TRSTn	I	JTAG Reset	D11	B6

**6.4.24 SYSBOOT****MAIN Domain Instances****6.4.24.1 Sysboot Signal Descriptions****Table 6-72. Sysboot Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
BOOTMODE00	I	Bootmode pin 0	T20	R21
BOOTMODE01	I	Bootmode pin 1	U21	R20
BOOTMODE02	I	Bootmode pin 2	T18	T19
BOOTMODE03	I	Bootmode pin 3	U20	V21
BOOTMODE04	I	Bootmode pin 4	U18	U21
BOOTMODE05	I	Bootmode pin 5	U19	T20
BOOTMODE06	I	Bootmode pin 6	V20	T18
BOOTMODE07	I	Bootmode pin 7	V21	U19
BOOTMODE08	I	Bootmode pin 8	V19	U18
BOOTMODE09	I	Bootmode pin 9	T17	U20
BOOTMODE10	I	Bootmode pin 10	R16	V20
BOOTMODE11	I	Bootmode pin 11	W20	W20
BOOTMODE12	I	Bootmode pin 12	W21	Y20
BOOTMODE13	I	Bootmode pin 13	V18	Y19

**Table 6-72. Sysboot Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
BOOTMODE14	I	Bootmode pin 14	Y21	Y18
BOOTMODE15	I	Bootmode pin 15	Y20	AA19

## 6.4.25 SYSTEM

### MAIN Domain Instances

#### 6.4.25.1 System Signal Descriptions

**Table 6-73. System Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
CLKOUT0	O	RMII Clock Output (50 MHz). This pin is used for clock source to the external PHY and must be routed back to the RMII_REF_CLK pin for proper device operation.	A19, U13	A18, V13
EXTINTn	I	External Interrupt	C19	
EXT_REFCLK1	I	External clock input to Main Domain, routed to Timer clock muxes as one of the selectable input clock sources for Timer/WDT modules, or as reference clock to MAIN_PLL2 (PER1 PLL)	A19	A18
GPMC0_FCLK_MUX	O	GPMC functional clock output selected through a mux logic	R17	
OBSCLK0	O	Observation clock output for test and debug purposes only	D17	A15
PORz_OUT	O	Main Domain POR status output	E17	D18
RESETSTATz	O	Main Domain warm reset status output	F16	E19
RESET_REQz	I	Main Domain external warm reset request input	E18	C17
SYNC0_OUT	O	CPTS Time Stamp Generator Bit 0	D18	
SYNC1_OUT	O	CPTS Time Stamp Generator Bit 1	A19	A18
SYNC2_OUT	O	CPTS Time Stamp Generator Bit 2	A17	B13
SYNC3_OUT	O	CPTS Time Stamp Generator Bit 3	B17	A14
SYSCCLKOUT0	O	SYSCCLK0 output from Main PLL controller (divided by 6) for test and debug purposes only	C17	B14

### MCU Domain Instances

#### 6.4.25.2 MCU System Signal Descriptions

**Table 6-74. MCU System Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_EXT_REFCLK0	I	External system clock input	B7	
MCU_OBSCLK0	O	Observation clock output for test and debug purposes only	C6, E10	B3
MCU_PORz	I	MCU Domain cold reset	B21	C20
MCU_RESETSTATz	O	MCU Domain warm reset status output	B13	A6

**Table 6-74. MCU System Signal Descriptions (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_RESETz	I	MCU Domain warm reset	B12	A5
MCU_SAFETY_ERRORn	IO	Error signal output from MCU Domain ESM	A20	B20
MCU_SYSCLKOUT0	O	MCU Domain system clock output for test and debug purposes only	C6	

**6.4.26 CLOCK****MCU Domain Instances****6.4.26.1 MCU Clock Signal Descriptions****Table 6-75. MCU Clock Signal Descriptions**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
MCU_OSC0_XI	I	High frequency oscillator input	C21	D20
MCU_OSC0_XO	O	High frequency oscillator output	B20	C21

**6.4.27 VMON****6.4.27.1 VMON Signal Description****Table 6-76. VMON Signal Description**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
VMON_1P8_MCU	A	Voltage monitor input for 1.8 V MCU power supply	K16	
VMON_1P8_SOC	A	Voltage monitor input for 1.8 V SoC power supply	E12	F14
VMON_3P3_MCU	A	Voltage monitor input for 3.3 V MCU power supply	F13	
VMON_3P3_SOC	A	Voltage monitor input for 3.3 V SoC power supply	F14	E15
VMON_VSYS	A	Voltage monitor input, fixed 0.45 V (+/-3%) threshold. Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply.	K10	G13

**6.4.28 Power Supply****6.4.28.1 Power Supply Signal Description****Table 6-77. Power Supply Signal Description**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
CAP_VDDS0	CAP	External capacitor connection for IO group 0	H12	D12
CAP_VDDS1	CAP	External capacitor connection for IO group 1	T7	N5
CAP_VDDS2	CAP	External capacitor connection for IO group 2	R11	U9
CAP_VDDS3	CAP	External capacitor connection for IO group 3	N14	R16
CAP_VDDS4	CAP	External capacitor connection for IO group 4	M16	N18
CAP_VDDS5	CAP	External capacitor connection for IO group 5	L13	M18
CAP_VDDSHV_MMC1	CAP	External capacitor connection for MMC1	K15	J17
CAP_VDDS_MCU	CAP	External capacitor connection for IO MCU	H10	D9



**Table 6-77. Power Supply Signal Description (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
VDDA_0P85_SERDES0	PWR	SERDES0 0.85 V analog supply	P12, P13	
VDDA_0P85_SERDES0_C	PWR	SERDES0 clock 0.85 V analog supply	P11	
VDDA_0P85_USB0	PWR	USB0 0.85 V analog supply	T12	V16
VDDA_1P8_SERDES0	PWR	SERDES0 1.8 V analog supply	R14	
VDDA_1P8_USB0	PWR	USB0 1.8 V analog supply	R15	U15
VDDA_3P3_SDIO	PWR	SDIO 3.3 V analog supply	H15	K15
VDDA_3P3_USB0	PWR	USB0 3.3 V analog supply	R13	U16
VDDA_ADC	PWR	ADC0 analog supply	J13	G17, H17
VDDA_MCU	PWR	POR and MCU PLL analog supply	K12	H14
VDDA_PLL0	PWR	Main, PER1, and R5F PLL analog supply	N12	N12
VDDA_PLL1	PWR	ARM and DDR PLL analog supply	H9	G9
VDDA_PLL2	PWR	PER0 PLL analog supply	J11	G12
VDDA_TEMP0	PWR	TEMP0 analog supply	G11	G11
VDDA_TEMP1	PWR	TEMP1 analog supply	L11	M11
VDDR_CORE	PWR	RAM supply	L10, M13	G5, G6, J10, J12, P14, P8, R10
VDDSHV0	PWR	IO supply for IO group 0	F11, G12, G14	C13, D13, E14
VDDSHV1	PWR	IO supply for IO group 1	M7, N6, P7	L6, M6, P5, P6
VDDSHV2	PWR	IO supply for IO group 2	R10, R8, T9	T11, T8, U11, U7, U8
VDDSHV3	PWR	IO supply for IO group 3	P14, P15	R17, T17
VDDSHV4	PWR	IO supply for IO group 4	M14, M15	N16, N17
VDDSHV5	PWR	IO supply for IO group 5	L14, L15	L16, L17
VDDSHV_MCU	PWR	IO supply for IO MCU	F9, G10, G8	E7, E8, E9
VDDS_DDR	PWR	DDR PHY IO supply	F7, G6, H7, J6, K7, L6	
VDDS_DDR_C	PWR	DDR clock IO supply	J8	
VDDS_MMC0	PWR	MMC0 PHY IO supply	J15, K14	
VDDS_OSC	PWR	MCU_OSC0 supply	H13	F18
VDD_CORE	PWR	Core supply	J10, J12, K11, K9, L12, L8, M11, M9, N10, N8, P9	F11, G10, H15, H8, J9, K11, K14, L13, L9, M14, M8, N10, N9, R12, R13, R9
VDD_DLL_MMC0	PWR	MMC0 PLL analog supply	H14	
VDD_MMC0	PWR	MMC0 PHY core supply	K13	
VPP	PWR	eFuse ROM programming supply	G15	E16

**Table 6-77. Power Supply Signal Description (continued)**

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION	ALV	ALX
VSS	GND	Ground	A1, A21, A5, A6, AA1, AA15, AA18, AA21, C10, C15, C3, D1, E11, E13, F10, F15, F8, G1, G16, G3, G7, G9, H11, H20, H21, H6, H8, J14, J16, J7, J9, K6, K8, L1, L16, L3, L7, L9, M10, M12, M6, M8, N11, N13, N15, N7, N9, P1, P10, P18, P6, P8, R12, R7, R9, T10, T11, T15, T16, T8, U3, V17, W10, W18, Y14, Y17, Y19	A1, A2, A20, A21, AA1, AA2, AA20, AA21, B1, B21, D10, D16, D17, E11, E13, E6, F17, F8, G16, H16, H6, H7, J11, J16, J5, J6, K16, K6, K7, K8, L10, L11, L12, M15, M16, M7, N11, N13, N6, P11, P15, P16, P7, R11, R6, T14, U6, Y1, Y21

ADVANCE INFORMATION



**Table 6-78. Pin Multiplexing (continued)**

(ALX) BALL #	(ALV) BALL #	PADCONFIG REGISTER	PADCONFIG ADDRESS	MUX MODE SETTINGS [Bootstrap:0]													
				0	1	2	3	4	5	6	7	8	9	10	15	Bootstrap	
Y20	W21	PADCONFIG_27	0x000F406C	GPMC0_AD12	FSI_RX1_D0	UART6_CTS n	EQEP1_B				TRC_DATA1 0	GPIO0_27	EHRPWM7_ B				BOOTMODE 12
Y19	V18	PADCONFIG_28	0x000F4070	GPMC0_AD13	FSI_RX1_D1		EHRPWM3_ A				TRC_DATA11	GPIO0_28		PRG0_PWM 3_A0			BOOTMODE 13
Y18	Y21	PADCONFIG_29	0x000F4074	GPMC0_AD14	FSI_TX0_D0	UART6_RXD	EHRPWM3_ B				TRC_DATA1 2	GPIO0_29		PRG0_PWM 3_B0			BOOTMODE 14
AA19	Y20	PADCONFIG_30	0x000F4078	GPMC0_AD15	FSI_TX0_D1	UART6_TXD	EHRPWM3_ SYNCl				TRC_DATA1 3	GPIO0_30					BOOTMODE 15
	R17	PADCONFIG_31	0x000F407C	GPMC0_CLK	FSI_RX4_CL K	UART4_RTS n	EHRPWM3_ SYNCO	GPMC0_FCL K_MUX			TRC_DATA1 4	GPIO0_31		PRG0_PWM 3_TZ_OUT			
	P16	PADCONFIG_33	0x000F4084	GPMC0_ADV n_ALE	FSI_RX5_CL K	UART5_RXD	EHRPWM_T Zn_IN3				TRC_DATA1 5	GPIO0_32		PRG0_PWM 3_TZ_IN			
	R18	PADCONFIG_34	0x000F4088	GPMC0_OEn_ REn	FSI_RX5_D0	UART5_TXD	EHRPWM4_ A				TRC_DATA1 6	GPIO0_33		PRG0_PWM 3_A1			
	T21	PADCONFIG_35	0x000F408C	GPMC0_WEn	FSI_RX5_D1	UART5_RTS n	EHRPWM4_ B				TRC_DATA1 7	GPIO0_34		PRG0_PWM 3_B1			
	P17	PADCONFIG_36	0x000F4090	GPMC0_BE0n_ CLE	FSI_TX1_D0	UART6_RTS n	EHRPWM_T Zn_IN4		EHRPWM7_ A		TRC_DATA1 8	GPIO0_35		PRG1_PWM 2_A1			
	P21	PADCONFIG_37	0x000F4094	GPMC0_BE1n	FSI_TX0_CL K		EHRPWM5_ A				TRC_DATA1 9	GPIO0_36		PRG0_PWM 3_A2			
	W19	PADCONFIG_38	0x000F4098	GPMC0_WAIT 0			EHRPWM5_ B				TRC_DATA2 0	GPIO0_37		PRG0_PWM 3_B2			
	Y18	PADCONFIG_39	0x000F409C	GPMC0_WAIT 1	FSI_TX1_D1		EHRPWM_T Zn_IN5	GPMC0_A21	EHRPWM7_ B		TRC_DATA2 1	GPIO0_38		PRG1_PWM 2_B1			
	N16	PADCONFIG_40	0x000F40A0	GPMC0_WPn	FSI_TX1_CL K		EQEP0_A	GPMC0_A22			TRC_DATA2 2	GPIO0_39	EHRPWM6_ A	PRG1_PWM 2_A0			
	N17	PADCONFIG_41	0x000F40A4	GPMC0_DIR			EQEP0_B					GPIO0_40	EHRPWM6_ B	PRG1_PWM 2_B0			
	R19	PADCONFIG_42	0x000F40A8	GPMC0_CSn0			EQEP0_S				TRC_DATA2 3	GPIO0_41	EHRPWM6_ SYNCl				
	R20	PADCONFIG_43	0x000F40AC	GPMC0_CSn1			EQEP0_I		EHRPWM_T Zn_IN2			GPIO0_42	EHRPWM6_ SYNCO	PRG1_PWM 2_TZ_OUT			
	P19	PADCONFIG_44	0x000F40B0	GPMC0_CSn2	I2C2_SCL	TIMER_IO8	EQEP1_S		EHRPWM_T Zn_IN4			GPIO0_43		PRG1_PWM 2_TZ_IN			
	R21	PADCONFIG_45	0x000F40B4	GPMC0_CSn3	I2C2_SDA	TIMER_IO9	EQEP1_I	GPMC0_A20	EHRPWM_T Zn_IN5			GPIO0_44					
V4	Y7	PADCONFIG_46	0x000F40B8	PRG1_PRU0_ GPO0	PRG1_PRU0_ GPI0	PRG1_RGMII 1_RD0	PRG1_PWM 3_A0					GPIO0_45	GPMC0_AD1 6				
W5	U8	PADCONFIG_47	0x000F40BC	PRG1_PRU0_ GPO1	PRG1_PRU0_ GPI1	PRG1_RGMII 1_RD1	PRG1_PWM 3_B0					GPIO0_46	GPMC0_AD1 7				
AA4	W8	PADCONFIG_48	0x000F40C0	PRG1_PRU0_ GPO2	PRG1_PRU0_ GPI2	PRG1_RGMII 1_RD2	PRG1_PWM 2_A0					GPIO0_47	GPMC0_AD1 8				
Y5	V8	PADCONFIG_49	0x000F40C4	PRG1_PRU0_ GPO3	PRG1_PRU0_ GPI3	PRG1_RGMII 1_RD3	PRG1_PWM 3_A2					GPIO0_48	GPMC0_AD1 9				
AA5	Y8	PADCONFIG_50	0x000F40C8	PRG1_PRU0_ GPO4	PRG1_PRU0_ GPI4	PRG1_RGMII 1_RX_CTL	PRG1_PWM 2_B0					GPIO0_49	GPMC0_AD2 0				

**Table 6-78. Pin Multiplexing (continued)**

(ALX) BALL #	(ALV) BALL #	PADCONFIG REGISTER	PADCONFIG ADDRESS	MUX MODE SETTINGS [Bootstrap:0]												Bootstrap	
				0	1	2	3	4	5	6	7	8	9	10	15		
U14	V13	PADCONFIG_51	0x000F40CC	PRG1_PRU0_GPO5	PRG1_PRU0_GPI5		PRG1_PWM_3_B2	RGMI11_RX_CTL				GPIO0_50	GPMC0_AD2_1				
Y2	AA7	PADCONFIG_52	0x000F40D0	PRG1_PRU0_GPO6	PRG1_PRU0_GPI6	PRG1_RGMII1_RXC	PRG1_PWM_3_A1					GPIO0_51	GPMC0_AD2_2				
V13	U13	PADCONFIG_53	0x000F40D4	PRG1_PRU0_GPO7	PRG1_PRU0_GPI7	PRG1_IEP0_EDC_LATCH_IN1	PRG1_PWM_3_B1	CPTS0_HW2_TSPUSH	CLKOUT0	TIMER_IO10		GPIO0_52	GPMC0_AD2_3				
Y13	W13	PADCONFIG_54	0x000F40D8	PRG1_PRU0_GPO8	PRG1_PRU0_GPI8		PRG1_PWM_2_A1	RGMI11_RXC				GPIO0_53	GPMC0_AD2_4				
W16	U15	PADCONFIG_55	0x000F40DC	PRG1_PRU0_GPO9	PRG1_PRU0_GPI9	PRG1_UART0_CTSn	PRG1_PWM_3_TZ_IN	RGMI11_TX_CTL	RMII1_RX_ER	PRG1_IEP0_EDIO_DATA_IN_OUT28		GPIO0_54	GPMC0_AD2_5				
W13	U14	PADCONFIG_56	0x000F40E0	PRG1_PRU0_GPO10	PRG1_PRU0_GPI10	PRG1_UART0_RTSn	PRG1_PWM_2_B1	RGMI11_TXC	RMII_REF_CLK	PRG1_IEP0_EDIO_DATA_IN_OUT29		GPIO0_55	GPMC0_AD2_6				
V5	AA8	PADCONFIG_57	0x000F40E4	PRG1_PRU0_GPO11	PRG1_PRU0_GPI11	PRG1_RGMII1_TD0	PRG1_PWM_3_TZ_OUT					GPIO0_56	GPMC0_AD2_7				
W2	U9	PADCONFIG_58	0x000F40E8	PRG1_PRU0_GPO12	PRG1_PRU0_GPI12	PRG1_RGMII1_TD1	PRG1_PWM_0_A0					GPIO0_57	GPMC0_AD2_8				
V6	W9	PADCONFIG_59	0x000F40EC	PRG1_PRU0_GPO13	PRG1_PRU0_GPI13	PRG1_RGMII1_TD2	PRG1_PWM_0_B0					GPIO0_58	GPMC0_AD2_9				
AA7	AA9	PADCONFIG_60	0x000F40F0	PRG1_PRU0_GPO14	PRG1_PRU0_GPI14	PRG1_RGMII1_TD3	PRG1_PWM_0_A1					GPIO0_59	GPMC0_AD3_0				
Y7	Y9	PADCONFIG_61	0x000F40F4	PRG1_PRU0_GPO15	PRG1_PRU0_GPI15	PRG1_RGMII1_TX_CTL	PRG1_PWM_0_B1					GPIO0_60	GPMC0_AD3_1				
W6	V9	PADCONFIG_62	0x000F40F8	PRG1_PRU0_GPO16	PRG1_PRU0_GPI16	PRG1_RGMII1_TXC	PRG1_PWM_0_A2					GPIO0_61	GPMC0_BE2_n				
T2	U7	PADCONFIG_63	0x000F40FC	PRG1_PRU0_GPO17	PRG1_PRU0_GPI17	PRG1_IEP0_EDC_SYNC_OUT1	PRG1_PWM_0_B2	CPTS0_TS_SYNC		TIMER_IO7		GPIO0_62	GPMC0_A0				
Y4	V7	PADCONFIG_64	0x000F4100	PRG1_PRU0_GPO18	PRG1_PRU0_GPI18	PRG1_IEP0_EDC_LATCH_IN0	PRG1_PWM_0_TZ_IN	CPTS0_HW1_TSPUSH		TIMER_IO8		GPIO0_63	GPMC0_A1				
U3	W7	PADCONFIG_65	0x000F4104	PRG1_PRU0_GPO19	PRG1_PRU0_GPI19	PRG1_IEP0_EDC_SYNC_OUT0	PRG1_PWM_0_TZ_OUT	CPTS0_TS_COMP		TIMER_IO9		GPIO0_64	GPMC0_A2				
AA10	W11	PADCONFIG_66	0x000F4108	PRG1_PRU1_GPO0	PRG1_PRU1_GPI0	PRG1_RGMII2_RD0		RGMI2_RD0	RMII2_RXD0			GPIO0_65	GPMC0_A3				
Y10	V11	PADCONFIG_67	0x000F410C	PRG1_PRU1_GPO1	PRG1_PRU1_GPI1	PRG1_RGMII2_RD1		RGMI2_RD1	RMII2_RXD1			GPIO0_66	GPMC0_A4				
Y11	AA12	PADCONFIG_68	0x000F4110	PRG1_PRU1_GPO2	PRG1_PRU1_GPI2	PRG1_RGMII2_RD2	PRG1_PWM_2_A2	RGMI2_RD2				GPIO0_67	GPMC0_A5				
V12	Y12	PADCONFIG_69	0x000F4114	PRG1_PRU1_GPO3	PRG1_PRU1_GPI3	PRG1_RGMII2_RD3		RGMI2_RD3				GPIO0_68	GPMC0_A6				
Y12	W12	PADCONFIG_70	0x000F4118	PRG1_PRU1_GPO4	PRG1_PRU1_GPI4	PRG1_RGMII2_RX_CTL	PRG1_PWM_2_B2	RGMI2_RX_CTL	RMII2_RX_ER			GPIO0_69	GPMC0_A7				
AA11	AA13	PADCONFIG_71	0x000F411C	PRG1_PRU1_GPO5	PRG1_PRU1_GPI5			RGMI11_RD0				GPIO0_70	GPMC0_A8				

**ADVANCE INFORMATION**

**Table 6-78. Pin Multiplexing (continued)**

(ALX) BALL #	(ALV) BALL #	PADCONFIG REGISTER	PADCONFIG ADDRESS	MUX MODE SETTINGS [Bootstrap:0]												
				0	1	2	3	4	5	6	7	8	9	10	15	Bootstrap
V10	U11	PADCONFIG_72	0x000F4120	PRG1_PRU1_ GPO6	PRG1_PRU1_ GPI6	PRG1_RGMII_2_RXC		RGMII2_RXC				GPIO0_71	GPMC0_A9			
Y14	V15	PADCONFIG_73	0x000F4124	PRG1_PRU1_ GPO7	PRG1_PRU1_ GPI7	PRG1_IEP1_ EDC_LATCH_ IN1		RGMII1_TD0	RMII1_RXD0	SPI3_CS3		GPIO0_72	GPMC0_A10			
W11	U12	PADCONFIG_74	0x000F4128	PRG1_PRU1_ GPO8	PRG1_PRU1_ GPI8		PRG1_PWM_2_TZ_OUT	RGMII1_RD1				GPIO0_73	GPMC0_A11			
Y16	V14	PADCONFIG_75	0x000F412C	PRG1_PRU1_ GPO9	PRG1_PRU1_ GPI9	PRG1_UART_0_RXD		RGMII1_TD1	RMII1_RXD1	PRG1_IEP0_ EDIO_DATA_ IN_OUT30		GPIO0_74	GPMC0_A12			
U13	W14	PADCONFIG_76	0x000F4130	PRG1_PRU1_ GPO10	PRG1_PRU1_ GPI10	PRG1_UART_0_TXD	PRG1_PWM_2_TZ_IN	RGMII1_TD2	RMII1_TXD0	PRG1_IEP0_ EDIO_DATA_ IN_OUT31		GPIO0_75	GPMC0_A13			
Y6	AA10	PADCONFIG_77	0x000F4134	PRG1_PRU1_ GPO11	PRG1_PRU1_ GPI11	PRG1_RGMII_2_TD0		RGMII2_TD0	RMII2_TXD0			GPIO0_76	GPMC0_A14			
AA8	V10	PADCONFIG_78	0x000F4138	PRG1_PRU1_ GPO12	PRG1_PRU1_ GPI12	PRG1_RGMII_2_TD1	PRG1_PWM_1_A0	RGMII2_TD1	RMII2_TXD1			GPIO0_77	GPMC0_A15			
Y9	U10	PADCONFIG_79	0x000F413C	PRG1_PRU1_ GPO13	PRG1_PRU1_ GPI13	PRG1_RGMII_2_TD2	PRG1_PWM_1_B0	RGMII2_TD2	RMII2_CRS_ DV			GPIO0_78	GPMC0_A16			
W9	AA11	PADCONFIG_80	0x000F4140	PRG1_PRU1_ GPO14	PRG1_PRU1_ GPI14	PRG1_RGMII_2_TD3	PRG1_PWM_1_A1	RGMII2_TD3				GPIO0_79	GPMC0_A17			
V9	Y11	PADCONFIG_81	0x000F4144	PRG1_PRU1_ GPO15	PRG1_PRU1_ GPI15	PRG1_RGMII_2_TX_CTL	PRG1_PWM_1_B1	RGMII2_TX_ CTL	RMII2_TX_E N			GPIO0_80	GPMC0_A18			
Y8	Y10	PADCONFIG_82	0x000F4148	PRG1_PRU1_ GPO16	PRG1_PRU1_ GPI16	PRG1_RGMII_2_TXC	PRG1_PWM_1_A2	RGMII2_TXC				GPIO0_81	GPMC0_A19			
AA14	AA14	PADCONFIG_83	0x000F414C	PRG1_PRU1_ GPO17	PRG1_PRU1_ GPI17	PRG1_IEP1_ EDC_SYNC_ OUT1	PRG1_PWM_1_B2	RGMII1_TD3	RMII1_TXD1			GPIO0_19	GPMC0_BE3 n	PRG1_ECAP_0_SYNC_ OUT		
Y15	Y13	PADCONFIG_84	0x000F4150	PRG1_PRU1_ GPO18	PRG1_PRU1_ GPI18	PRG1_IEP1_ EDC_LATCH_ IN0	PRG1_PWM_1_TZ_IN	RGMII1_RD2	RMII1_TX_E N			GPIO0_20	UART5_CTS n	PRG1_ECAP_0_SYNC_ IN		
AA13	V12	PADCONFIG_85	0x000F4154	PRG1_PRU1_ GPO19	PRG1_PRU1_ GPI19	PRG1_IEP1_ EDC_SYNC_ OUT0	PRG1_PWM_1_TZ_OUT	RGMII1_RD3	RMII1_CRS_ DV	SPI3_CS2		GPIO0_84	UART5_RTS n	PRG1_ECAP_0_IN_ APWM_ OUT		
V2	AA6	PADCONFIG_86	0x000F4158	PRG1_MDIO0_ MDIO				MDIO0_MDI_ O				GPIO0_85				
W1	Y6	PADCONFIG_87	0x000F415C	PRG1_MDIO0_ MDC				MDIO0_MDC				GPIO0_86				
J3	Y1	PADCONFIG_88	0x000F4160	PRG0_PRU0_ GPO0	PRG0_PRU0_ GPI0	PRG0_RGMII_1_RD0	PRG0_PWM_3_A0					GPIO1_0			UART2_CTS n	
J4	R4	PADCONFIG_89	0x000F4164	PRG0_PRU0_ GPO1	PRG0_PRU0_ GPI1	PRG0_RGMII_1_RD1	PRG0_PWM_3_B0					GPIO1_1			UART2_TXD	
G1	U2	PADCONFIG_90	0x000F4168	PRG0_PRU0_ GPO2	PRG0_PRU0_ GPI2	PRG0_RGMII_1_RD2	PRG0_PWM_2_A0					GPIO1_2		GPMC0_A0	UART2_RTS n	
H1	V2	PADCONFIG_91	0x000F416C	PRG0_PRU0_ GPO3	PRG0_PRU0_ GPI3	PRG0_RGMII_1_RD3	PRG0_PWM_3_A2					GPIO1_3			UART3_CTS n	
K2	AA2	PADCONFIG_92	0x000F4170	PRG0_PRU0_ GPO4	PRG0_PRU0_ GPI4	PRG0_RGMII_1_RX_CTL	PRG0_PWM_2_B0					GPIO1_4		GPMC0_A1	UART3_TXD	

**Table 6-78. Pin Multiplexing (continued)**

(ALX) BALL #	(ALV) BALL #	PADCONFIG REGISTER	PADCONFIG ADDRESS	MUX MODE SETTINGS [Bootstrap:0]												
				0	1	2	3	4	5	6	7	8	9	10	15	Bootstrap
F2	R3	PADCONFIG_93	0x000F4174	PRG0_PRU0_ GPO5	PRG0_PRU0_ _GPI5		PRG0_PWM 3_B2					GPIO1_5			UART3_RTS n	
H2	T3	PADCONFIG_94	0x000F4178	PRG0_PRU0_ GPO6	PRG0_PRU0_ _GPI6	PRG0_RGMII 1_RXC	PRG0_PWM 3_A1					GPIO1_6			UART4_CTS n	
E2	T1	PADCONFIG_95	0x000F417C	PRG0_PRU0_ GPO7	PRG0_PRU0_ _GPI7	PRG0_IEP0_ EDC_LATCH _IN1	PRG0_PWM 3_B1	CPTS0_HW2 TSPUSH	CP_GEMAC_ CPTS0_HW2 TSPUSH	TIMER_IO6		GPIO1_7			UART4_TXD	
H5	T2	PADCONFIG_96	0x000F4180	PRG0_PRU0_ GPO8	PRG0_PRU0_ _GPI8		PRG0_PWM 2_A1					GPIO1_8	GPMC0_A2		UART4_RTS n	
Y3	W6	PADCONFIG_97	0x000F4184	PRG0_PRU0_ GPO9	PRG0_PRU0_ _GPI9	PRG0_UART 0_CTSn	PRG0_PWM 3_TZ_IN	RGMII1_RX_ CTL	RMII1_RX_E R	PRG0_IEP0_ EDIO_DATA_ IN_OUT28		GPIO1_9			UART2_RXD	
U1	AA5	PADCONFIG_98	0x000F4188	PRG0_PRU0_ GPO10	PRG0_PRU0_ _GPI10	PRG0_UART 0_RTSn	PRG0_PWM 2_B1	RGMII1_RXC	RMII_REF_C LK	PRG0_IEP0_ EDIO_DATA_ IN_OUT29		GPIO1_10			UART3_RXD	
L1	Y3	PADCONFIG_99	0x000F418C	PRG0_PRU0_ GPO11	PRG0_PRU0_ _GPI11	PRG0_RGMII 1_TD0	PRG0_PWM 3_TZ_OUT					GPIO1_11			UART4_RXD	
K1	AA3	PADCONFIG_100	0x000F4190	PRG0_PRU0_ GPO12	PRG0_PRU0_ _GPI12	PRG0_RGMII 1_TD1	PRG0_PWM 0_A0					GPIO1_12	GPMC0_A14			
N1	R6	PADCONFIG_101	0x000F4194	PRG0_PRU0_ GPO13	PRG0_PRU0_ _GPI13	PRG0_RGMII 1_TD2	PRG0_PWM 0_B0			SPI3_D0		GPIO1_13	GPMC0_A15			
N2	V4	PADCONFIG_102	0x000F4198	PRG0_PRU0_ GPO14	PRG0_PRU0_ _GPI14	PRG0_RGMII 1_TD3	PRG0_PWM 0_A1			SPI3_D1		GPIO1_14	GPMC0_A3			
N4	T5	PADCONFIG_103	0x000F419C	PRG0_PRU0_ GPO15	PRG0_PRU0_ _GPI15	PRG0_RGMII 1_TX_CTL	PRG0_PWM 0_B1			SPI3_CS1		GPIO1_15	GPMC0_A16			
N3	U4	PADCONFIG_104	0x000F41A0	PRG0_PRU0_ GPO16	PRG0_PRU0_ _GPI16	PRG0_RGMII 1_TXC	PRG0_PWM 0_A2			SPI3_CLK		GPIO1_16	GPMC0_A4			
E1	U1	PADCONFIG_105	0x000F41A4	PRG0_PRU0_ GPO17	PRG0_PRU0_ _GPI17	PRG0_IEP0_ EDC_SYNC_ OUT1	PRG0_PWM 0_B2	CPTS0_TS_ SYNC	CP_GEMAC_ CPTS0_TS_ SYNC	SPI3_CS0		GPIO1_17	TIMER_IO11	GPMC0_A17		
K4	V1	PADCONFIG_106	0x000F41A8	PRG0_PRU0_ GPO18	PRG0_PRU0_ _GPI18	PRG0_IEP0_ EDC_LATCH _IN0	PRG0_PWM 0_TZ_IN	CPTS0_HW1 TSPUSH	CP_GEMAC_ CPTS0_HW1 TSPUSH	EHRPWM8_ A		GPIO1_18	UART4_CTS n	GPMC0_A5	UART2_RXD	
G2	W1	PADCONFIG_107	0x000F41AC	PRG0_PRU0_ GPO19	PRG0_PRU0_ _GPI19	PRG0_IEP0_ EDC_SYNC_ OUT0	PRG0_PWM 0_TZ_OUT	CPTS0_TS_ COMP	CP_GEMAC_ CPTS0_TS_ COMP	EHRPWM8_ B		GPIO1_19	UART4_RTS n	GPMC0_A6	UART3_RXD	
L5	Y2	PADCONFIG_108	0x000F41B0	PRG0_PRU1_ GPO0	PRG0_PRU1_ _GPI0	PRG0_RGMII 2_RD0						GPIO1_20	EQEP0_A		UART5_CTS n	
J2	W2	PADCONFIG_109	0x000F41B4	PRG0_PRU1_ GPO1	PRG0_PRU1_ _GPI1	PRG0_RGMII 2_RD1						GPIO1_21	EQEP0_B		UART5_TXD	
M2	V3	PADCONFIG_110	0x000F41B8	PRG0_PRU1_ GPO2	PRG0_PRU1_ _GPI2	PRG0_RGMII 2_RD2	PRG0_PWM 2_A2					GPIO1_22	EQEP0_S		UART5_RTS n	
L2	T4	PADCONFIG_111	0x000F41BC	PRG0_PRU1_ GPO3	PRG0_PRU1_ _GPI3	PRG0_RGMII 2_RD3						GPIO1_23	EQEP1_A	GPMC0_A18	UART6_CTS n	
L3	W3	PADCONFIG_112	0x000F41C0	PRG0_PRU1_ GPO4	PRG0_PRU1_ _GPI4	PRG0_RGMII 2_RX_CTL	PRG0_PWM 2_B2					GPIO1_24	EQEP1_B		UART6_TXD	
E3	P4	PADCONFIG_113	0x000F41C4	PRG0_PRU1_ GPO5	PRG0_PRU1_ _GPI5							GPIO1_25	EQEP1_S		UART6_RTS n	

**Table 6-78. Pin Multiplexing (continued)**

(ALX) BALL #	(ALV) BALL #	PADCONFIG REGISTER	PADCONFIG ADDRESS	MUX MODE SETTINGS [Bootstrap:0]													
				0	1	2	3	4	5	6	7	8	9	10	15	Bootstrap	
F5	R5	PADCONFIG_114	0x000F41C8	PRG0_PRU1_GPO6	PRG0_PRU1_GPI6	PRG0_RGMII2_RXC						GPIO1_26	EQEP2_A	GPMC0_A19	UART4_CTSn		
T5	W5	PADCONFIG_115	0x000F41CC	PRG0_PRU1_GPO7	PRG0_PRU1_GPI7	PRG0_IEP1_EDC_LATCH_IN1		RGMI11_RD0	RMII1_RXD0			GPIO1_27	EQEP2_B			UART4_TXD	
F4	R1	PADCONFIG_116	0x000F41D0	PRG0_PRU1_GPO8	PRG0_PRU1_GPI8		PRG0_PWM2_TZ_OUT					GPIO1_28	EQEP2_S			UART4_RTSn	
R2	Y5	PADCONFIG_117	0x000F41D4	PRG0_PRU1_GPO9	PRG0_PRU1_GPI9	PRG0_UART0_RXD		RGMI11_RD1	RMII1_RXD1	PRG0_IEP0_EDIO_DATA_IN_OUT30		GPIO1_29	EQEP0_I			UART5_RXD	
U2	V6	PADCONFIG_118	0x000F41D8	PRG0_PRU1_GPO10	PRG0_PRU1_GPI10	PRG0_UART0_TXD	PRG0_PWM2_TZ_IN	RGMI11_RD2	RMII1_TXD0	PRG0_IEP0_EDIO_DATA_IN_OUT31		GPIO1_30	EQEP1_I			UART6_RXD	
P1	W4	PADCONFIG_119	0x000F41DC	PRG0_PRU1_GPO11	PRG0_PRU1_GPI11	PRG0_RGMII2_TD0						GPIO1_31	EQEP2_I			UART4_RXD	
P2	Y4	PADCONFIG_120	0x000F41E0	PRG0_PRU1_GPO12	PRG0_PRU1_GPI12	PRG0_RGMII2_TD1	PRG0_PWM1_A0					GPIO1_32	EQEP2_B	GPMC0_A7		UART4_TXD	
T4	T6	PADCONFIG_121	0x000F41E4	PRG0_PRU1_GPO13	PRG0_PRU1_GPI13	PRG0_RGMII2_TD2	PRG0_PWM1_B0					GPIO1_33	EQEP0_I	GPMC0_A8		UART5_RXD	
R5	U6	PADCONFIG_122	0x000F41E8	PRG0_PRU1_GPO14	PRG0_PRU1_GPI14	PRG0_RGMII2_TD3	PRG0_PWM1_A1					GPIO1_34	EQEP1_I	GPMC0_A9		UART6_RXD	
M4	U5	PADCONFIG_123	0x000F41EC	PRG0_PRU1_GPO15	PRG0_PRU1_GPI15	PRG0_RGMII2_TX_CTL	PRG0_PWM1_B1					GPIO1_35		GPMC0_A10	PRG0_ECAP0_IN_APWM_OUT		
T3	AA4	PADCONFIG_124	0x000F41F0	PRG0_PRU1_GPO16	PRG0_PRU1_GPI16	PRG0_RGMII2_TXC	PRG0_PWM1_A2					GPIO1_36		GPMC0_A11	PRG0_ECAP0_SYNC_OUT		
T1	V5	PADCONFIG_125	0x000F41F4	PRG0_PRU1_GPO17	PRG0_PRU1_GPI17	PRG0_IEP1_EDC_SYNC_OUT1	PRG0_PWM1_B2	RGMI11_RD3	RMII1_TXD1			GPIO1_37	PRG0_ECAP0_SYNC_OUT			PRG0_ECAP0_SYNC_IN	
D1	P5	PADCONFIG_126	0x000F41F8	PRG0_PRU1_GPO18	PRG0_PRU1_GPI18	PRG0_IEP1_EDC_LATCH_IN0	PRG0_PWM1_TZ_IN	MDIO0_MDI_O	RMII1_TX_EN	EHRPWM7_A		GPIO1_38	PRG0_ECAP0_SYNC_IN				
F3	R2	PADCONFIG_127	0x000F41FC	PRG0_PRU1_GPO19	PRG0_PRU1_GPI19	PRG0_IEP1_EDC_SYNC_OUT0	PRG0_PWM1_TZ_OUT	MDIO0_MDC	RMII1_CRS_DV	EHRPWM7_B		GPIO1_39	PRG0_ECAP0_IN_APWM_OUT				
E4	P2	PADCONFIG_128	0x000F4200	PRG0_MDIO0_MDIO								GPIO1_40		GPMC0_A12			
D2	P3	PADCONFIG_129	0x000F4204	PRG0_MDIO0_MDC								GPIO1_41		GPMC0_A13			
	D12	PADCONFIG_130	0x000F4208	SPI0_CS0								GPIO1_42					
B7	C13	PADCONFIG_131	0x000F420C	SPI0_CS1	CPTS0_TS_COMP	I2C2_SCL	TIMER_IO10	PRG0_IEP0_EDIO_OUTV_ALID	UART6_RXD	ADC_EXT_T_RIGGER0		GPIO1_43					
B8	D13	PADCONFIG_132	0x000F4210	SPI0_CLK								GPIO1_44					
A8	A13	PADCONFIG_133	0x000F4214	SPI0_D0								GPIO1_45					
C9	A14	PADCONFIG_134	0x000F4218	SPI0_D1								GPIO1_46					



**Table 6-78. Pin Multiplexing (continued)**

(ALX) BALL #	(ALV) BALL #	PADCONFIG REGISTER	PADCONFIG ADDRESS	MUX MODE SETTINGS [Bootstrap:0]												
				0	1	2	3	4	5	6	7	8	9	10	15	Bootstrap
	B14	PADCONFIG_135	0x000F421C	SPI1_CS0			EHRPWM6_A					GPIO1_47				
	D14	PADCONFIG_136	0x000F4220	SPI1_CS1	CPTS0_TS_SYNC	I2C2_SDA		PRG1_IEP0_EDIO_OUTV_ALID	UART6_TXD	ADC_EXT_T_RIGGER1		GPIO1_48	TIMER_IO11			
	C14	PADCONFIG_137	0x000F4224	SPI1_CLK			EHRPWM6_SYNCI					GPIO1_49				
	B15	PADCONFIG_138	0x000F4228	SPI1_D0			EHRPWM6_SYNCO					GPIO1_50				
	A15	PADCONFIG_139	0x000F422C	SPI1_D1			EHRPWM6_B					GPIO1_51				
B10	D15	PADCONFIG_140	0x000F4230	UART0_RXD		SPI2_D0						GPIO1_52	EQEP0_A			
B11	C16	PADCONFIG_141	0x000F4234	UART0_TXD		SPI2_D1						GPIO1_53	EQEP0_B			
B9	B16	PADCONFIG_142	0x000F4238	UART0_CTSn	SPI0_CS2	ADC_EXT_T_RIGGER0	UART2_RXD	TIMER_IO6			SPI4_CLK	GPIO1_54	EQEP0_S	CP_GEMAC_CPTS0_TS_SYNC		
A9	A16	PADCONFIG_143	0x000F423C	UART0_RTSn	SPI0_CS3		UART2_TXD	TIMER_IO7			SPI4_D0	GPIO1_55	EQEP0_I			
B12	E15	PADCONFIG_144	0x000F4240	UART1_RXD		SPI2_CS0				CP_GEMAC_CPTS0_TS_COMP		GPIO1_56	EQEP1_A			
A12	E14	PADCONFIG_145	0x000F4244	UART1_TXD		SPI2_CLK				CP_GEMAC_CPTS0_HW1_TSPUSH		GPIO1_57	EQEP1_B			
C11	D16	PADCONFIG_146	0x000F4248	UART1_CTSn	SPI1_CS2	ADC_EXT_T_RIGGER1	PCIE0_CLKR EQn	UART3_RXD	CP_GEMAC_CPTS0_TS_SYNC	SPI4_D1	GPIO1_58	EQEP1_S				
A11	E16	PADCONFIG_147	0x000F424C	UART1_RTSn	SPI1_CS3			UART3_TXD	CP_GEMAC_CPTS0_HW2_TSPUSH	SPI4_CS0	GPIO1_59	EQEP1_I				
B13	A17	PADCONFIG_148	0x000F4250	MCAN0_TX	UART4_RXD	TIMER_IO2	SYNC2_OUT				SPI4_CS1	GPIO1_60	EQEP2_I	UART0_DTRn		
A14	B17	PADCONFIG_149	0x000F4254	MCAN0_RX	UART4_TXD	TIMER_IO3	SYNC3_OUT				SPI4_CS2	GPIO1_61	EQEP2_S	UART0_RIn		
B14	C17	PADCONFIG_150	0x000F4258	MCAN1_TX	I2C3_SCL	ECAP1_IN_A_PWM_OUT	SYSCLKOUT_0	TIMER_IO4	UART5_RXD	EHRPWM_S_OCA	GPIO1_62	EQEP2_A	UART0_DCDn			
A15	D17	PADCONFIG_151	0x000F425C	MCAN1_RX	I2C3_SDA	ECAP2_IN_A_PWM_OUT	OBSCLK0	TIMER_IO5	UART5_TXD	EHRPWM_S_OCB	GPIO1_63	EQEP2_B	UART0_DSRn		OBSCLK0	
B16	A18	PADCONFIG_152	0x000F4260	I2C0_SCL				UART6_CTSn				GPIO1_64				
B15	B18	PADCONFIG_153	0x000F4264	I2C0_SDA				UART6_RTSn				GPIO1_65				
A17	C18	PADCONFIG_154	0x000F4268	I2C1_SCL	CPTS0_HW1_TSPUSH	TIMER_IO0	SPI2_CS1					GPIO1_66				
B18	B19	PADCONFIG_155	0x000F426C	I2C1_SDA	CPTS0_HW2_TSPUSH	TIMER_IO1	SPI2_CS2					GPIO1_67				
	D18	PADCONFIG_156	0x000F4270	ECAP0_IN_A_PWM_OUT	SYNC0_OUT	CPTS0_RFT_CLK				CP_GEMAC_CPTS0_RFT_CLK	SPI4_CS3	GPIO1_68				

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**Table 6-78. Pin Multiplexing (continued)**

(ALX) BALL #	(ALV) BALL #	PADCONFIG REGISTER	PADCONFIG ADDRESS	MUX MODE SETTINGS [Bootstrap:0]												
				0	1	2	3	4	5	6	7	8	9	10	15	Bootstrap
A18	A19	PADCONFIG_157	0x000F4274	EXT_REFCLK 1	SYNC1_OUT	SPI2_CS3				CLKOUT0		GPIO1_69				
	C19	PADCONFIG_158	0x000F4278	EXTINTn								GPIO1_70				
K18	K18	PADCONFIG_159	0x000F427C	MMC1_DAT3	CP_GEMAC_ CPTS0_TS_ COMP	TIMER_IO0	UART2_RXD					GPIO1_71				
K20	K19	PADCONFIG_160	0x000F4280	MMC1_DAT2	CP_GEMAC_ CPTS0_TS_ SYNC	TIMER_IO1	UART2_TXD					GPIO1_72				
J19	L21	PADCONFIG_161	0x000F4284	MMC1_DAT1	CP_GEMAC_ CPTS0_HW1 TSPUSH	TIMER_IO2	UART3_RXD					GPIO1_73				
J18	K21	PADCONFIG_162	0x000F4288	MMC1_DAT0	CP_GEMAC_ CPTS0_HW2 TSPUSH	TIMER_IO3	UART3_TXD					GPIO1_74				
J20	L20	PADCONFIG_163	0x000F428C	MMC1_CLK	UART2_CTS n	TIMER_IO4	UART4_RXD					GPIO1_75				
J21	J19	PADCONFIG_165	0x000F4294	MMC1_CMD	UART2_RTS n	TIMER_IO5	UART4_TXD					GPIO1_76				
B17	D19	PADCONFIG_166	0x000F4298	MMC1_SDCD	UART3_CTS n	TIMER_IO6	UART5_RXD					GPIO1_77				
C16	C20	PADCONFIG_167	0x000F429C	MMC1_SDWP	UART3_RTS n	TIMER_IO7	UART5_TXD					GPIO1_78				
C17	E18	PADCONFIG_168	0x000F42A0	RESET_REQz												
E19	F16	PADCONFIG_169	0x000F42A4	RESETSTATz												
B19	E19	PADCONFIG_170	0x000F42A8	USB0_DRVVB US								GPIO1_79				
D18	E17	PADCONFIG_171	0x000F42AC	PORz_OUT												
H21	G20	PADCONFIG_172	0x000F42B0	ADC0_AIN0								GPIO1_80				
F19	F20	PADCONFIG_173	0x000F42B4	ADC0_AIN1								GPIO1_81				
F21	E21	PADCONFIG_174	0x000F42B8	ADC0_AIN2								GPIO1_82				
F20	D20	PADCONFIG_175	0x000F42BC	ADC0_AIN3								GPIO1_83				
H20	G21	PADCONFIG_176	0x000F42C0	ADC0_AIN4								GPIO1_84				
E21	F21	PADCONFIG_177	0x000F42C4	ADC0_AIN5								GPIO1_85				
G20	F19	PADCONFIG_178	0x000F42C8	ADC0_AIN6								GPIO1_86				
E20	E20	PADCONFIG_179	0x000F42CC	ADC0_AIN7								GPIO1_87				
	D6	MCU_PADCONFIG _0	0x04084000	MCU_SPI0_C S0								MCU_GPI O0_13				
	C6	MCU_PADCONFIG _1	0x04084004	MCU_SPI0_C S1	MCU_OBSC LK0	MCU_SYSCL KOUT0						MCU_GPI O0_12				
	E6	MCU_PADCONFIG _2	0x04084008	MCU_SPI0_C LK								MCU_GPI O0_11				
	E7	MCU_PADCONFIG _3	0x0408400C	MCU_SPI0_D 0								MCU_GPI O0_10				

**Table 6-78. Pin Multiplexing (continued)**

(ALX) BALL #	(ALV) BALL #	PADCONFIG REGISTER	PADCONFIG ADDRESS	MUX MODE SETTINGS [Bootstrap:0]													
				0	1	2	3	4	5	6	7	8	9	10	15	Bootstrap	
	B6	MCU_PADCONFIG _4	0x04084010	MCU_SPIO_D 1								MCU_GPI O0_4					
	A7	MCU_PADCONFIG _5	0x04084014	MCU_SPI1_C S0								MCU_GPI O0_5					
	B7	MCU_PADCONFIG _6	0x04084018	MCU_SPI1_C S1	MCU_EXT_R EFCLK0							MCU_GPI O0_6					
	D7	MCU_PADCONFIG _7	0x0408401C	MCU_SPI1_C LK								MCU_GPI O0_7					
	C7	MCU_PADCONFIG _8	0x04084020	MCU_SPIO_D 0								MCU_GPI O0_8					
	C8	MCU_PADCONFIG _9	0x04084024	MCU_SPI1_D 1								MCU_GPI O1*					
D6	A9	MCU_PADCONFIG _10	0x04084028	MCU_UART0_ RXD								MCU_GPI O0_3					
B2	A8	MCU_PADCONFIG _11	0x0408402C	MCU_UART0_ TXD								MCU_GPI O0_2					
D4	D8	MCU_PADCONFIG _12	0x04084030	MCU_UART0_ CTSn	MCU_TIMER _IO0	MCU_SPIO_ CS2						MCU_GPI O0_1					
C2	E8	MCU_PADCONFIG _13	0x04084034	MCU_UART0_ RTSn	MCU_TIMER _IO1	MCU_SPI1_ CS2						MCU_GPI O0_0					
	C9	MCU_PADCONFIG _14	0x04084038	MCU_UART1_ RXD								MCU_GPI O0_14					
	D9	MCU_PADCONFIG _15	0x0408403C	MCU_UART1_ TXD								MCU_GPI O0_15					
	B8	MCU_PADCONFIG _16	0x04084040	MCU_UART1_ CTSn	MCU_TIMER _IO2	MCU_SPIO_ CS3						MCU_GPI O0_16					
	B9	MCU_PADCONFIG _17	0x04084044	MCU_UART1_ RTSn	MCU_TIMER _IO3	MCU_SPI1_ CS3						MCU_GPI O0_17					
	E9	MCU_PADCONFIG _18	0x04084048	MCU_I2C0_S CL								MCU_GPI O0_18					
	A10	MCU_PADCONFIG _19	0x0408404C	MCU_I2C0_S DA								MCU_GPI O0_19					
	A11	MCU_PADCONFIG _20	0x04084050	MCU_I2C1_S CL								MCU_GPI O0_20					
	B10	MCU_PADCONFIG _21	0x04084054	MCU_I2C1_S DA								MCU_GPI O0_21					
A5	B12	MCU_PADCONFIG _22	0x04084058	MCU_RESETz													
C20	B21	MCU_PADCONFIG _23	0x0408405C	MCU_PORz													
A6	B13	MCU_PADCONFIG _24	0x04084060	MCU_RESET STATz								MCU_GPI O0_22					
B20	A20	MCU_PADCONFIG _25	0x04084064	MCU_SAFETY _ERRORn													
C6	B11	MCU_PADCONFIG _26	0x04084068	TCK													

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**Table 6-78. Pin Multiplexing (continued)**

(ALX) BALL #	(ALV) BALL #	PADCONFIG REGISTER	PADCONFIG ADDRESS	MUX MODE SETTINGS [Bootstrap:0]													
				0	1	2	3	4	5	6	7	8	9	10	15	Bootstrap	
B6	D11	MCU_PADCONFIG _27	0x0408406C	TRSTn													
A3	C11	MCU_PADCONFIG _28	0x04084070	TDI													
B5	A12	MCU_PADCONFIG _29	0x04084074	TDO													
B4	C12	MCU_PADCONFIG _30	0x04084078	TMS													
C5	D10	MCU_PADCONFIG _31	0x0408407C	EMU0													
B3	E10	MCU_PADCONFIG _32	0x04084080	EMU1													MCU_OB SCLK0

**ADVANCE INFORMATION**

## 6.6 Connections for Unused Pins

This section describes the Unused/Reserved balls connection requirements for the mechanical packages supported.

**Table 6-79. Reserved Balls Specific Connection Requirements (ALV)**

PKG	BALL NUMBER	CONNECTION REQUIREMENTS
ALV	D21, F12, F17, G13, H16, K1, K2, V16, W15	These balls must be left unconnected.

**Table 6-80. Unused Balls Specific Connection Requirements (ALV)**

BALL NUMBER (ALV)	BALL NAME	CONNECTION REQUIREMENTS
TBD	TBD	Each of these balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level if unused.
TBD	TBD	Each of these balls must be connected to the corresponding power supply through a separate external pull resistor to ensure these balls are held to a valid logic high level, if unused. <sup>(1)</sup>
J13 G20 F20 E21, D20 G21 F21 F19 E20	VDDA_ADC ADC0_AIN0 ADC0_AIN1 ADC0_AIN2 ADC0_AIN3 ADC0_AIN4 ADC0_AIN5 ADC0_AIN6 ADC0_AIN7	If the entire ADC is not used, each of these balls must be connected directly to VSS.
G20 F20 E21, D20 G21 F21 F19 E20	ADC0_AIN0 ADC0_AIN1 ADC0_AIN2 ADC0_AIN3 ADC0_AIN4 ADC0_AIN5 ADC0_AIN6 ADC0_AIN7	Any unused AIN ball must be pulled to VSS through a resistor or connected directly to VSS when VDDA_ADC is connected to a power source.
F7 G6 H7 J6, K7 L6 J8	VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR VDDS_DDR_C	If DDRSS is not used, each of these balls must be connected directly to VSS.

**Table 6-80. Unused Balls Specific Connection Requirements (ALV) (continued)**

BALL NUMBER (ALV)	BALL NAME	CONNECTION REQUIREMENTS
H2 H1 J5 K5 F6 H4 D2 C5 E2 D4 D3 F2 J2 L5 J3 J4 K3 J1 M5 K4 G4 G5 G2 H3 H5 F1 E1 F4 F3 E3 E4 B2 M2 A3 A2 B5 A4 B3 C4 C2 B4 N5 L4 L2 M3 N4 N3 M4 N2 C1 B1 N1 M1 E5 F5 D5	DDR0_ACT_n DDR0_ALERT_n DDR0_CAS_n DDR0_PAR DDR0_RAS_n DDR0_WE_n DDR0_A0 DDR0_A1 DDR0_A2 DDR0_A3 DDR0_A4 DDR0_A5 DDR0_A6 DDR0_A7 DDR0_A8 DDR0_A9 DDR0_A10 DDR0_A11 DDR0_A12 DDR0_A13 DDR0_BA0 DDR0_BA1 DDR0_BG0 DDR0_BG1 DDR0_CAL0 DDR0_CK0 DDR0_CK0_n DDR0_CKE0 DDR0_CKE1 DDR0_CS0_n DDR0_CS1_n DDR0_DM0 DDR0_DM1 DDR0_DQ0 DDR0_DQ1 DDR0_DQ2 DDR0_DQ3 DDR0_DQ4 DDR0_DQ5 DDR0_DQ6 DDR0_DQ7 DDR0_DQ8 DDR0_DQ9 DDR0_DQ10 DDR0_DQ11 DDR0_DQ12 DDR0_DQ13 DDR0_DQ14 DDR0_DQ15 DDR0_DQS0 DDR0_DQS0_n DDR0_DQS1 DDR0_DQS1_n DDR0_ODT0 DDR0_ODT1 DDR0_RESET0_n	<p>Leave unconnected.</p> <p>Note: The DDR0 pins in this list can only be left unconnected when VDDS_DDR and VDDS_DDR_C are connected to VSS. The DDR0 pins must be connected as defined in the <a href="#">AM64x/AM243x DDR Board Design and Layout Guidelines</a>, when VDDS_DDR and VDDS_DDR_C are connected to a power source.</p>
K13 H14	VDD_MMC0 VDD_DLL_MMC0	If MMC0 is not used, each of these balls must be connected to the same power source as VDD_CORE.
J15 K14	VDDS_MMC0 VDDS_MMC0	If MMC0 is not used, each of these balls must be connected to any 1.8V power source that does not violate device power supply sequencing requirements.

**ADVANCE INFORMATION**

**Table 6-80. Unused Balls Specific Connection Requirements (ALV) (continued)**

BALL NUMBER (ALV)	BALL NAME	CONNECTION REQUIREMENTS
F18 G18 J21 G19 K20 J20 J18 J17 H17 H19 H18 G17	MMC0_CALPAD MMC0_CLK MMC0_CMD MMC0_DS MMC0_DAT0 MMC0_DAT1 MMC0_DAT2 MMC0_DAT3 MMC0_DAT4 MMC0_DAT5 MMC0_DAT6 MMC0_DAT7	If MMC0 is not used, each of these balls must be left unconnected.
P12 P13 P11 R14	VDDA_0P85_SERDES0 VDDA_0P85_SERDES0 VDDA_0P85_SERDES0_C VDDA_1P8_SERDES0	If SERDES0 is not used, each of these balls must be connected directly to VSS.
T13 W16 W17 Y15 Y16 AA16 AA17	SERDES0_REXT SERDES0_REFCLK0N SERDES0_REFCLK0P SERDES0_RX0_N SERDES0_RX0_P SERDES0_TX0_N SERDES0_TX0_P	Leave unconnected. Note: The SERDES0_REXT pin can only be left unconnected when VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C, and VDDA_1P8_SERDES0 are connected to VSS. The SERDES0_REXT pin must be connected to VSS through the appropriate external resistor when VDDA_0P85_SERDES0, VDDA_0P85_SERDES0_C, and VDDA_1P8_SERDES0 are connected to a power source.
T12 R15 R13	VDDA_0P85_USB0 VDDA_1P8_USB0 VDDA_3P3_USB0	If USB0 is not used, each of these balls must be connected directly to VSS.
AA20 AA19 U16 U17 T14	USB0_DM USB0_DP USB0_ID USB0_RCALIB USB0_VBUS	Leave unconnected. Note: The USB0_RCALIB pin can only be left unconnected when VDDA_0P85_USB0, VDDA_1P8_USB0, and VDDA_3P3_USB0 are connected to VSS. The USB0_RCALIB pin must be connected to VSS through the appropriate external resistor when VDDA_0P85_USB0, VDDA_1P8_USB0, and VDDA_3P3_USB0 are connected to a power source.

**Table 6-81. Reserved Balls Specific Connection Requirements (ALX)**

PKG	BALL NUMBER	CONNECTION REQUIREMENTS
ALX	H11, J13	These balls must be left unconnected.

**Table 6-82. Unused Balls Specific Connection Requirements (ALX)**

BALL NUMBER (ALX)	BALL NAME	CONNECTION REQUIREMENTS
TBD	TBD	Each of these balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level if unused.
TBD	TBD	Each of these balls must be connected to the corresponding power supply through a separate external pull resistor to ensure these balls are held to a valid logic high level, if unused. <sup>(1)</sup>
J13 H21 F19 F21, F20 H20 E21 G20 E20	VDDA_ADC ADC0_AIN0 ADC0_AIN1 ADC0_AIN2 ADC0_AIN3 ADC0_AIN4 ADC0_AIN5 ADC0_AIN6 ADC0_AIN7	If the entire ADC is not used, each of these balls must be connected directly to VSS.

**Table 6-82. Unused Balls Specific Connection Requirements (ALX) (continued)**

BALL NUMBER (ALX)	BALL NAME	CONNECTION REQUIREMENTS
H21 F19 F21, F20 H20 E21 G20 E20	ADC0_AIN0 ADC0_AIN1 ADC0_AIN2 ADC0_AIN3 ADC0_AIN4 ADC0_AIN5 ADC0_AIN6 ADC0_AIN7	Any unused AIN ball must be pulled to VSS through a resistor or connected directly to VSS when VDDA_ADC is connected to a power source.
V16 U15 U16	VDDA_0P85_USB0 VDDA_1P8_USB0 VDDA_3P3_USB0	If USB0 is not used, each of these balls must be connected directly to VSS.
AA17 AA16 Y17 W17 V18	USB0_DM USB0_DP USB0_ID USB0_RCALIB USB0_VBUS	Leave unconnected. Note: The USB0_RCALIB pin can only be left unconnected when VDDA_0P85_USB0, VDDA_1P8_USB0, and VDDA_3P3_USB0 are connected to VSS. The USB0_RCALIB pin must be connected to VSS through the appropriate external resistor when VDDA_0P85_USB0, VDDA_1P8_USB0, and VDDA_3P3_USB0 are connected to a power source.

- (1) To determine which power supply is associated with any IO refer to the *Pin Attributes* tables.

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#### Note

All power balls must be supplied with the voltages specified in [Section 7.4, Recommended Operating Conditions](#), unless otherwise specified in [Section 6.4, Signal Descriptions](#).

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#### Note

All other unused signal balls **with** a Pad Configuration register can be left unconnected with their multiplexing mode set to GPIO input and internal pulldown resistor enabled.

Unused balls are defined as those which only connect to a PCB solder pad. This is the only use case where internal pull resistors are allowed as the only source/sink to hold a valid logic level.

Any balls connected to a via, test point, or PCB trace are considered used and must not depend on the internal pull resistor to hold a valid logic level.

Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This may be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors may be required to hold a valid logic level on balls with external connections.

If balls are allowed to float between valid logic levels, the input buffer may enter a high-current state which could damage the IO cell.

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#### Note

All other unused signal balls **without** a Pad Configuration register should be left unconnected.

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## 7 Specifications

### 7.1 Absolute Maximum Ratings

**Table 7-1. Absolute Maximum Ratings**

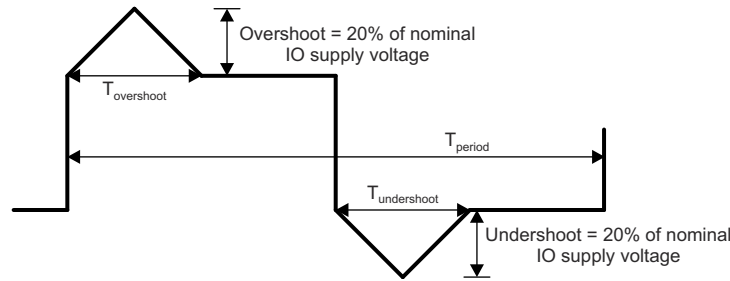
PARAMETER		MIN	MAX	Unit
VDD_CORE	Core supply	-0.3	1.05	V
VDDR_CORE	RAM supply	-0.3	1.05	V
VDD_MMC0	MMC0 PHY core supply	-0.3	1.05	V
VDD_DLL_MMC0	MMC0 PLL analog supply	-0.3	1.05	V
VDDA_0P85_SERDES0	SERDES0 0.85 V analog supply	-0.3	1.05	V
VDDA_0P85_SERDES0_C	SERDES0 clock 0.85 V analog supply	-0.3	1.05	V
VDDA_0P85_USB0	USB0 0.85 V analog supply	-0.3	1.05	V
VDDS_DDR	DDR PHY IO supply	-0.3	TBD	V
VDDS_DDR_C	DDR clock IO supply	-0.3	TBD	V
VDDS_MMC0	MMC0 PHY IO supply	-0.3	2.2	V
VDDS_OSC	MCU_OSC0 supply	-0.3	2.2	V
VDDA_MCU	POR and MCU PLL analog supply	-0.3	2.2	V
VDDA_ADC0	ADC0 analog supply	-0.3	2.2	V
VDDA_PLL0	Main, PER1, and R5F PLL analog supply	-0.3	2.2	V
VDDA_PLL1	ARM and DDR PLL analog supply	-0.3	2.2	V
VDDA_PLL2	PER0 PLL analog supply	-0.3	2.2	V
VDDA_1P8_SERDES0	SERDES0 1.8 V analog supply	-0.3	2.2	V
VDDA_1P8_USB0	USB0 1.8 V analog supply	-0.3	2.2	V
VDDA_TEMP0	TEMP0 analog supply	-0.3	2.2	V
VDDA_TEMP1	TEMP1 analog supply	-0.3	2.2	V
VPP	eFuse ROM programming supply	-0.3	TBD	V
VDDSHV_MCU	IO supply for IO MCU	-0.3	3.8	V
VDDSHV0	IO supply for IO group 0	-0.3	3.8	V
VDDSHV1	IO supply for IO group 1	-0.3	3.8	V
VDDSHV2	IO supply for IO group 2	-0.3	3.8	V
VDDSHV3	IO supply for IO group 3	-0.3	3.8	V
VDDSHV4	IO supply for IO group 4	-0.3	3.8	V
VDDSHV5	IO supply for IO group 5	-0.3	3.8	V
VDDA_3P3_USB0	USB0 3.3 V analog supply	-0.3	3.8	V
VDDA_3P3_SDIO	SDIO 3.3 V analog supply	-0.3	TBD	V
Steady-state max voltage at all fail-safe IO pins	MCU_I2C0_SCL, MCU_I2C0_SDA, I2C0_SCL, I2C0_SDA, EXTINTn, MCU_PORz	-0.3	TBD	V
	VMON_1P8_MCU, VMON_1P8_SOC	-0.3	2.2	V
	VMON_3P3_MCU, VMON_3P3_SOC	-0.3	3.8	V
	VMON_VSYS <sup>(2)</sup>	-0.3	2.2	V
Steady-state max voltage at all other IO pins <sup>(1)</sup>	USB0_VBUS <sup>(4)</sup>	-0.3	3.6	V
	All other IO pins	-0.3	IO Supply Voltage + 0.3	V
Transient overshoot and undershoot at IO pin	20% of IO supply voltage for up to 20% of the signal period (see <a href="#">Figure 7-1, IO Transient Voltage Ranges</a> )		$0.2 \times VDD^{(3)}$	V
Latch-up performance		TBD	TBD	mA

**Table 7-1. Absolute Maximum Ratings (continued)**

PARAMETER		MIN	MAX	Unit
T <sub>STG</sub>	Storage temperature	-55	+150	°C

- (1) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
- (2) The VMON\_VSYS pin provides a way to monitor the system power supply. For more information, see [Section 9.3.5, System Power Supply Monitor Design Guidelines](#).
- (3) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
- (4) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see [Section 9.3.4, USB Design Guidelines](#).

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The MCU\_I2C0\_SCL, MCU\_I2C0\_SDA, I2C0\_SCL, I2C0\_SDA, EXTINTn, VMON\_1P8\_MCU, VMON\_1P8\_SOC, VMON\_3P3\_MCU, VMON\_3P3\_SOC, and MCU\_PORz are the only fail-safe IO terminals. All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in [Section 7.1](#).



A.  $T_{overshoot} + T_{undershoot} < 20\% \text{ of } T_{period}$

**Figure 7-1. IO Transient Voltage Ranges**

ADVANCE INFORMATION

## 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	TBD	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	TBD	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Power-On Hours (POH)

Temperature Range	JUNCTION TEMP (T <sub>j</sub> )	LIFETIME (POH) <sup>(1) (2) (3)</sup>
Commercial Junction Temperature Range	0°C to 90°C	TBD
Extended Junction Temperature Range	-40°C to 105°C	TBD

- (1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
- (2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
- (3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.

## 7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN <sup>(3)</sup>	NOM	MAX <sup>(3)</sup>	UNIT
VDD_CORE	Core supply	0.85 V Operation	0.81	0.85	0.895	V
VDDR_CORE	RAM supply		0.81	0.85	0.895	V
VDD_MMC0	MMC0 PHY core supply		0.81	0.85	0.895	V
VDD_DLL_MMC0	MMC0 PLL analog supply		0.81	0.85	0.895	V
VDDA_0P85_SERDES0	SERDES0 0.85 V analog supply		0.81	0.85	0.895	V
VDDA_0P85_SERDES0_C	SERDES0 clock 0.85 V analog supply		0.81	0.85	0.895	V
VDDA_0P85_USB0	USB0 0.85 V analog supply		0.81	0.85	0.895	V
VDDS_DDR	DDR PHY IO supply	1.1 V Operation	1.06	1.1	1.17	V
		1.2 V Operation	1.14	1.2	1.26	V
VDDS_DDR_C	DDR clock IO supply	1.1 V Operation	1.06	1.1	1.17	V
		1.2 V Operation	1.14	1.2	1.26	V
VDDS_MMC0	MMC0 PHY IO supply		1.71	1.8	1.89	V
VDDS_OSC	MCU_OSC0 supply		1.71	1.8	1.89	V
VDDA_MCU	POR and MCU PLL analog supply		1.71	1.8	1.89	V
VDDA_ADC0	ADC0 analog supply		1.71	1.8	1.89	V
VDDA_PLL0	Main, PER and R5F PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL1	ARM and DDR PLL analog supply		1.71	1.8	1.89	V
VDDA_PLL2	PER0 PLL analog supply		1.71	1.8	1.89	V
VDDA_1P8_SERDES0	SERDES0 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_1P8_USB0	USB0 1.8 V analog supply		1.71	1.8	1.89	V
VDDA_TEMP0	TEMP0 analog supply		1.71	1.8	1.89	V
VDDA_TEMP1	TEMP1 analog supply		1.71	1.8	1.89	V
VPP	eFuse ROM programming supply		1.71	1.8	1.89	V
VMON_1P8_MCU	Voltage monitor for 1.8 V MCU power supply		1.71	1.8	1.89	V
VMON_1P8_SOC	Voltage monitor for 1.8 V SoC power supply		1.71	1.8	1.89	V
VDDA_3P3_USB0	USB0 3.3 V analog supply		3.135	3.3	3.465	V
VDDA_3P3_SDIO	SDIO 3.3 V analog supply		3.135	3.3	3.465	V
VMON_3P3_MCU	Voltage monitor for 3.3 V MCU power supply		3.135	3.3	3.465	V
VMON_3P3_SOC	Voltage monitor for 3.3 V SoC power supply		3.135	3.3	3.465	V
VMON_VSYS	Voltage monitor pin		0	see <sup>(1)</sup>	1	V
USB0_VBUS	USB Level-shifted VBUS Input		0	see <sup>(2)</sup>	3.465	V
VDDSHV_MCU	Dual-voltage IO supply	1.8 V Operation	1.71	1.8	1.89	V
		3.3 V Operation	3.135	3.3	3.465	V
VDDSHV0	Dual-voltage IO supply	1.8 V Operation	1.71	1.8	1.89	V
		3.3 V Operation	3.135	3.3	3.465	V
VDDSHV1	Dual-voltage IO supply	1.8 V Operation	1.71	1.8	1.89	V
		3.3 V Operation	3.135	3.3	3.465	V
VDDSHV2	Dual-voltage IO supply	1.8 V Operation	1.71	1.8	1.89	V
		3.3 V Operation	3.135	3.3	3.465	V
VDDSHV3	Dual-voltage IO supply	1.8 V Operation	1.71	1.8	1.89	V
		3.3 V Operation	3.135	3.3	3.465	V
VDDSHV4	Dual-voltage IO supply	1.8 V Operation	1.71	1.8	1.89	V
		3.3 V Operation	3.135	3.3	3.465	V

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION	MIN <sup>(3)</sup>	NOM	MAX <sup>(3)</sup>	UNIT	
VDDSHV5	Dual-voltage IO supply	1.8 V Operation	1.71	1.8	1.89	V
		3.3 V Operation	3.135	3.3	3.465	V
T <sub>J</sub>	Operating junction temperature range	Extended	-40		105	°C
		Commercial	0		90	

- (1) The VMON\_VSYS pin provides a way to monitor the system power supply. For more information, see [Section 9.3.5, System Power Supply Monitor Design Guidelines](#).
- (2) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see [Section 9.3.4, USB Design Guidelines](#).
- (3) The voltage at the device ball must never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, and so forth.

## 7.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks and device core clocks.

### Note

The OPP voltage and frequency values may change following the silicon characterization result.

Table 7-2 describes the maximum supported frequency per speed grade for the device.

**Table 7-2. Speed Grade Maximum Frequency**

DEVICE <sup>(1)</sup>	MAXIMUM FREQUENCY (MHz)							
	SPEED GRADE	R5FSS	M4FSS	INFRA (CBASS)	ICSSG	DMSC-L	DDR4	LPDDR4
AM243x...ALV	S	800	400	250	333	250	800 (DDR-1600) <sup>(2)</sup>	800 (LPDDR-1600) <sup>(2)</sup>
AM243x...ALV	K	400	400	250	TBD	250	800 (DDR-1600) <sup>(2)</sup>	800 (LPDDR-1600) <sup>(2)</sup>
AM243x...ALX	S	800	400	250	333	250	N/A	N/A
AM243x...ALX	K	400	400	250	TBD	250	N/A	N/A

(1) N/A in this table stands for Not Applicable.

(2) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation.

## 7.6 Power Consumption Summary

For information on the device power consumption contact your TI Representative.

## 7.7 Electrical Characteristics

### Note

The interfaces or signals described in the following Electrical Characteristics tables correspond to the interfaces or signals available when the associated PADCONFIG register is configured for multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a combined PHY and GPIO topology. In this case, different DC electrical characteristics are specified for the different multiplexing modes (Functions).

### 7.7.1 Fail-Safe Reset (FS RESET) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IL</sub>	Input Low Voltage				0.3 × V <sub>DDS_OSC</sub>	V
V <sub>ILSS</sub>	Input Low Voltage Steady State				TBD	V
V <sub>IH</sub>	Input High Voltage		0.7 × V <sub>DDS_OSC</sub>			V
V <sub>IHSS</sub>	Input High Voltage Steady State		TBD			V
V <sub>HYS</sub>	Input Hysteresis Voltage		200			mV
I <sub>IN</sub>	Input Leakage Current.	V <sub>I</sub> = 1.8 V or V <sub>I</sub> = 0 V			±10	μA
SR <sub>I</sub>	Input Slew Rate		TBD	TBD	TBD	V/s

### 7.7.2 I2C Open-Drain, and Fail-Safe (I2C OD FS) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>1.8 V MODE</b>						
V <sub>IL</sub>	Input Low Voltage				0.3 × VDD <sup>(1)</sup>	V
V <sub>ILSS</sub>	Input Low Voltage Steady State				0.3 × VDD <sup>(1)</sup>	V
V <sub>IH</sub>	Input High Voltage		0.7 × VDD <sup>(1)</sup>			V
V <sub>IHSS</sub>	Input High Voltage Steady State		0.7 × VDD <sup>(1)</sup>			V
V <sub>HYS</sub>	Input Hysteresis Voltage		0.1 × VDD <sup>(1)</sup>		TBD	mV
I <sub>IN</sub>	Input Leakage Current.	V <sub>I</sub> = 1.8 V or V <sub>I</sub> = 0 V		±10	±10	μA
V <sub>OL</sub>	Output Low Voltage				0.2 × VDD <sup>(1)</sup>	V
I <sub>OL</sub>	Low Level Output Current	V <sub>OL(MAX)</sub>	20			mA
SR <sub>I</sub>	Input Slew Rate		TBD	TBD	TBD	V/s
<b>3.3 V MODE<sup>(2)</sup></b>						
V <sub>IL</sub>	Input Low Voltage				0.3 × VDD <sup>(1)</sup>	V
V <sub>ILSS</sub>	Input Low Voltage Steady State				0.25 × VDD <sup>(1)</sup>	V
V <sub>IH</sub>	Input High Voltage		0.7 × VDD <sup>(1)</sup>			V
V <sub>IHSS</sub>	Input High Voltage Steady State		0.7 × VDD <sup>(1)</sup>			V
V <sub>HYS</sub>	Input Hysteresis Voltage		0.05 × VDD <sup>(1)</sup>		TBD	mV
I <sub>IN</sub>	Input Leakage Current.	V <sub>I</sub> = 3.3 V or V <sub>I</sub> = 0 V		±10	±10	μA
V <sub>OL</sub>	Output Low Voltage				0.4	V

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OL}$	Low Level Output Current	$V_{OL(MAX)}$	20			mA
$SR_I$	Input Slew Rate		TBD	TBD	$8E + 7$	V/s

- (1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see POWER column of the *Pin Attributes* table.
- (2) I2C HS-mode is not supported when operating the IO in 3.3 V mode.

### 7.7.3 High-Frequency Oscillator (HFOSC) Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL}$	Input Low Voltage				$0.35 \times V_{DD5\_OSC}$	V
$V_{IH}$	Input High Voltage		$0.65 \times V_{DD5\_OSC}$			V
$V_{HYS}$	Input Hysteresis Voltage		49			mV
$I_{IN}$	Input Leakage Current.	$V_I = 1.8\text{ V}$ or $V_I = 0.0\text{ V}$			$\pm TBD$	$\mu A$

### 7.7.4 eMMCPHY Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL}$	Input Low Voltage				$0.35 \times V_{DD5\_MMC0}$	V
$V_{ILSS}$	Input Low Voltage Steady State				0.20	V
$V_{IH}$	Input High Voltage		$0.65 \times V_{DD5\_MMC0}$			V
$V_{IHSS}$	Input High Voltage Steady State		1.4			V
$I_{IN}$	Input Leakage Current.	$V_I = 1.8\text{ V}$ or $0\text{ V}$			$\pm 10$	$\mu A$
$R_{PU}$	Pull-up Resistor		15	20	25	k $\Omega$
$R_{PD}$	Pull-down Resistor		15	20	25	k $\Omega$
$V_{OL}$	Output Low Voltage	$I_{OL} = 2\text{ mA}$			0.30	V
$V_{OH}$	Output High Voltage	$I_{OH} = -2\text{ mA}$	$V_{DD5\_MMC0} - 0.30$			V
$SR_I$	Input Slew Rate		$5E + 8$			V/s

### 7.7.5 SDIO Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>1.8 V MODE</b>						
$V_{IL}$	Input Low Voltage				0.58	V
$V_{ILSS}$	Input Low Voltage Steady State				0.58	V
$V_{IH}$	Input High Voltage		1.27			V
$V_{IHSS}$	Input High Voltage Steady State		1.7			V
$V_{HYS}$	Input Hysteresis Voltage		150			mV
$I_{IN}$	Input Leakage Current.	$V_I = 1.8\text{ V}$ or $V_I = 0\text{ V}$			$\pm 10$	$\mu A$
$R_{PU}$	Pull-up Resistor		40	50	60	k $\Omega$
$R_{PD}$	Pull-down Resistor		40	50	60	k $\Omega$

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OL</sub>	Output Low Voltage				0.45	V
V <sub>OH</sub>	Output High Voltage		V <sub>DDSHV5</sub> - 0.45			V
I <sub>OL</sub>	Low Level Output Current	V <sub>OL(MAX)</sub>	4			mA
I <sub>OH</sub>	High Level Output Current	V <sub>OH(MIN)</sub>	4			mA
SR <sub>I</sub>	Input Slew Rate		TBD			V/s
<b>3.3 V MODE</b>						
V <sub>IL</sub>	Input Low Voltage				0.25 × V <sub>DDSHV5</sub>	V
V <sub>ILSS</sub>	Input Low Voltage Steady State				0.15 × V <sub>DDSHV5</sub>	V
V <sub>IH</sub>	Input High Voltage		0.625 × V <sub>DDSHV5</sub>			V
V <sub>IHSS</sub>	Input High Voltage Steady State		0.625 × V <sub>DDSHV5</sub>			V
V <sub>HYS</sub>	Input Hysteresis Voltage		150			mV
I <sub>IN</sub>	Input Leakage Current.	V <sub>I</sub> = 3.3 V or V <sub>I</sub> = 0 V			±10	μA
R <sub>PU</sub>	Pull-up Resistor		40	50	60	kΩ
R <sub>PD</sub>	Pull-down Resistor		40	50	60	kΩ
V <sub>OL</sub>	Output Low Voltage				0.125 × V <sub>DDSHV5</sub>	V
V <sub>OH</sub>	Output High Voltage		0.75 × V <sub>DDSHV5</sub>			V
I <sub>OL</sub>	Low Level Output Current	V <sub>OL(MAX)</sub>	6			mA
I <sub>OH</sub>	High Level Output Current	V <sub>OH(MIN)</sub>	10			mA
SR <sub>I</sub>	Input Slew Rate		TBD	TBD	TBD	V/s



## 7.7.6 ADC12B Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>ADC_AIN[7:0]</sub>	Full-scale Input Range		VSS	VDDA_ADC0		V
DNL	Differential Non-Linearity		-1	0.5	2	LSB
INL	Integral Non-Linearity			±1	±3	LSB
LSB <sub>GAIN-ERROR</sub>	Gain Error			±2		LSB
LSB <sub>OFFSET-ERROR</sub>	Offset Error			±2		LSB
C <sub>IN</sub>	Input Sampling Capacitance			5.5		pF
SNR	Signal-to-Noise Ratio	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		70		dB
THD	Total Harmonic Distortion	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		75		dB
SFDR	Spurious Free Dynamic Range	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		80		dB
SNR <sub>(PLUS)</sub>	Signal-to-Noise Plus Distortion	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		69		dB
R <sub>ADC_AIN[0:7]</sub>	Input Impedance of ADC0_AIN[7:0]	f = input frequency		$[1/((65.97 \times 10^{-12}) \times f)]$		Ω
I <sub>IN</sub>	Input Leakage	ADC0_AIN[7:0] = VSS			4	μA
		ADC0_AIN[7:0] = VDDA_ADC0			10	μA
<b>Sampling Dynamics</b>						
F <sub>SMPL_CLK</sub>	SMPL_CLK Frequency			60		MHz
t <sub>C</sub>	Conversion Time			13		ADC0 SMPL_CLK Cycles
t <sub>ACQ</sub>	Acquisition time		2		257	ADC0 SMPL_CLK Cycles
T <sub>R</sub>	Sampling Rate	ADC0 SMPL_CLK = 60 MHz			4	MSPS
CCISO	Channel to Channel Isolation			100		dB
<b>General Purpose Input Mode <sup>(1)</sup></b>						
V <sub>IL</sub>	Input Low Voltage				0.35 × VDDA_ADC0	V
V <sub>ILSS</sub>	Input Low Voltage Steady State				0.35 × VDDA_ADC0	V
V <sub>IH</sub>	Input High Voltage		0.65 × VDDA_ADC0			V
V <sub>IHSS</sub>	Input High Voltage Steady State		0.65 × VDDA_ADC0			V
V <sub>HYS</sub>	Input Hysteresis Voltage		200			mV

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_I$	Input Leakage Current	ADC0_AIN[7:0] = VDDA_ADC0 or ADC0_AIN[7:0] = VSS			2	$\mu\text{A}$

- (1) ADC0 can be configured to operate in General Purpose Input mode, where all ADC0\_AIN[7:0] inputs are globally enabled to operate as digital inputs via the ADC0\_CTRL register (gpi\_mode\_en = 1).

### 7.7.7 LVC MOS Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>1.8-V MODE</b>						
$V_{IL}$	Input Low Voltage				$0.35 \times VDD^{(1)}$	V
$V_{ILSS}$	Input Low Voltage Steady State				$0.3 \times VDD^{(1)}$	V
$V_{IH}$	Input High Voltage		$0.65 \times VDD^{(1)}$			V
$V_{IHS}$	Input High Voltage Steady State		$0.85 \times VDD^{(1)}$			V
$V_{HYS}$	Input Hysteresis Voltage		150			mV
$I_{IN}$	Input Leakage Current.	$V_I = 1.8\text{ V}$ or $V_I = 0.0\text{ V}$			$\pm 10$	$\mu\text{A}$
$R_{PU}$	Pull-up Resistor		15	22	30	k $\Omega$
$R_{PD}$	Pull-down Resistor		15	22	30	k $\Omega$
$V_{OL}$	Output Low Voltage				0.45	V
$V_{OH}$	Output High Voltage		$0.45 \times VDD^{(1)}$			V
$I_{OL}$	Low Level Output Current	$V_{OL(MAX)}$	3			mA
$I_{OH}$	High Level Output Current	$V_{OH(MIN)}$	3			mA
$SR_I$	Input Slew Rate		TBD	TBD	TBD	V/s
<b>3.3-V MODE</b>						
$V_{IL}$	Input Low Voltage				0.8	V
$V_{ILSS}$	Input Low Voltage Steady State				0.6	V
$V_{IH}$	Input High Voltage		2.0			V
$V_{IHS}$	Input High Voltage Steady State		2.0			V
$V_{HYS}$	Input Hysteresis Voltage		150			mV
$I_{IN}$	Input Leakage Current.	$V_I = 3.3\text{ V}$ or $V_I = 0.0\text{ V}$			$\pm 10$	$\mu\text{A}$
$R_{PD}$	Pull-down Resistor		15	22	30	k $\Omega$
$R_{PD}$	Pull-down Resistor		15	22	30	k $\Omega$
$V_{OL}$	Output Low Voltage				0.4	V
$V_{OH}$	Output High Voltage		2.4			V
$I_{OL}$	Low Level Output Current	$V_{OL(MAX)}$	5			mA
$I_{OH}$	High Level Output Current	$V_{OH(MIN)}$	9			mA
$SR_I$	Input Slew Rate		TBD	TBD	TBD	V/s

- (1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see the POWER column of the *Pin Attributes* table.

### 7.7.8 USB2PHY Electrical Characteristics

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**Note**

USB0 interface is compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

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### 7.7.9 DDR Electrical Characteristics

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**Note**

The DDR interface is compatible with DDR4 and LPDDR4 devices

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## 7.8 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses..

### 7.8.1 Recommended Operating Conditions for OTP eFuse Programming

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VDD_CORE	Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)	See <i>Recommended Operating Conditions</i>			V
VPP	Supply voltage range for the eFuse ROM domain during normal operation without hardware support to program eFuse ROM	NC <sup>(2)</sup>			V
	Supply voltage range for the eFuse ROM domain during normal operation with hardware support to program eFuse ROM	0			V
	Supply voltage range for the eFuse ROM domain during OTP programming <sup>(1)</sup>	1.71	1.8	1.89	V
I <sub>(VPP)</sub>	VPP current	TBD			mA
SR <sub>(VPP)</sub>	VPP Slew Rate	6E + 4			V/s
Tj	Temperature (ambient)	0	25	85	°C

(1) Supply voltage range includes DC errors and peak-to-peak noise. TI power management solutions [TLV70718](#) from the TLV707x family is a example device that meets the supply voltage range needed for VPP.

(2) NC stands for No Connect.

### 7.8.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.
- The VPP power supply must be ramped up after the proper device power-up sequence (for more details, see [Section 7.10.2, Power Supply Sequencing](#)).

### 7.8.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP terminal according to the specification in [Section 7.8.1](#).
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP terminal.

### 7.8.4 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

## 7.9 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the  $T_J$  value identified in *Recommended Operating Conditions*.

### 7.9.1 Thermal Resistance Characteristics

**Table 7-3. ALV Package Thermal Resistance Characteristics**

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

NO.	PARAMETER	DESCRIPTION	°C/W <sup>(1) (3)</sup>	AIR FLOW (m/s) <sup>(2)</sup>	°C/W <sup>(1) (3)</sup>	AIR FLOW (m/s) <sup>(2)</sup>
			ALV Package		ALX Package	
T1	$R\theta_{JC}$	Junction-to-case	0.98	N/A	TBD	N/A
T2	$R\theta_{JB}$	Junction-to-board	3.87	N/A	TBD	N/A
T3	$R\theta_{JA}$	Junction-to-free air	12.8	0	TBD	0
T4	$R\theta_{JA}$	Junction-to-moving air	TBD	1	TBD	1
T5			TBD	2	TBD	2
T6			TBD	3	TBD	3
T7	$\Psi_{JT}$	Junction-to-package top	0.53	0	TBD	0
T8			TBD	1	TBD	1
T9			TBD	2	TBD	2
T10	$\Psi_{JB}$	Junction-to-board	TBD	3	TBD	3
T11			3.74	0	TBD	0
T12			TBD	1	TBD	1
T13			TBD	2	TBD	2
T14			TBD	3	TBD	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [ $R\theta_{JC}$ ] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second.

(3) °C/W = degrees Celsius per watt.

## 7.10 Timing and Switching Characteristics

### Note

The Timing Requirements and Switching Characteristics values may change following the silicon characterization result.

### Note

The default SLEWRATE settings in each pad configuration register must be used to ensure timings, unless specific instructions are given otherwise.

### 7.10.1 Timing Parameters and Information

The timing parameter symbols used in *Timing and Switching Characteristics* sections are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in [Table 7-4](#):

**Table 7-4. Timing Parameters Subscripts**

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

## 7.10.2 Power Supply Sequencing

This section describes power supply sequencing required to ensure proper device operation. The power supply names described in this section comprise a superset of a family of compatible devices. Some members of this family will not include a subset of these power supplies and their associated device modules.

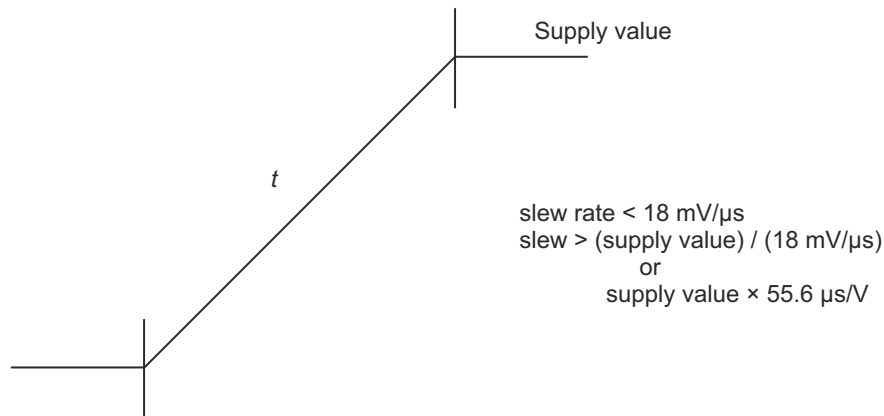
### Note

All power sequence timing shown is preliminary and under evaluation. Updates will be provided as details become known during validation testing.

### 7.10.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 18 mV/μs. For instance, as shown in Figure 7-2, TI recommends having the supply ramp slew for a 1.8-V supply of more than 100 μs.

Figure 7-2 describes the Power Supply Slew Rate Requirement in the device.

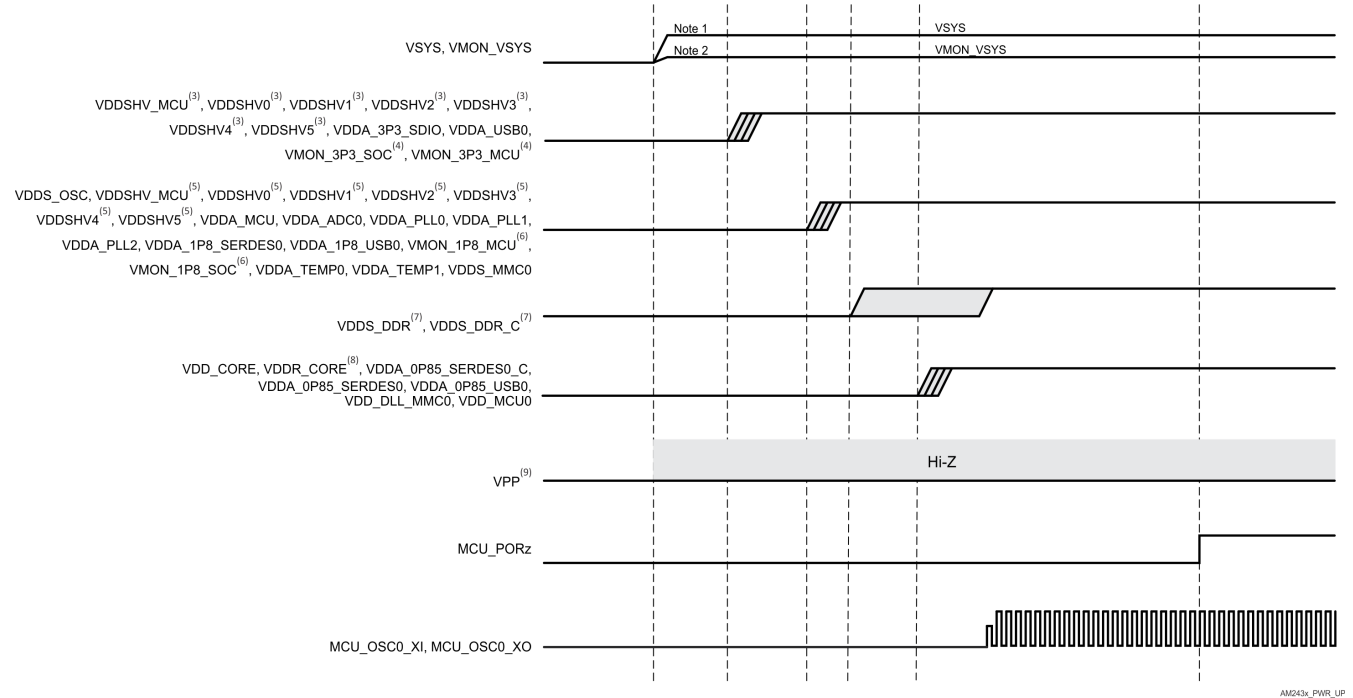


SPRT740\_ELCH\_06

Figure 7-2. Power Supply Slew and Slew Rate

### 7.10.2.2 Power-Up Sequencing

The Figure 7-3 diagram describes the device power-up sequencing.


**Figure 7-3. Power-Up Sequencing**

1. VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.
2. VMON\_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see [Section 9.3.5, System Power Supply Monitor Design Guidelines](#).
3. VDDSHV\_MCU and VDDSHV<sub>x</sub> [x=0-5] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. When any of the VDDSHV\_MCU or VDDSHV<sub>x</sub> [x=0-5] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.
4. The VMON\_3P3\_MCU and VMON\_3P3\_SOC inputs are used to monitor supply voltage and shall be connected to the respective 3.3V supply source.
5. VDDSHV\_MCU and VDDSHV<sub>x</sub> [x=0-5] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. When any of the VDDSHV\_MCU or VDDSHV<sub>x</sub> [x=0-5] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.
6. The VMON\_1P8\_MCU and VMON\_1P8\_SOC inputs are used to monitor supply voltage and shall be connected to the respective 1.8V supply source.
7. VDDS\_DDR and VDDS\_DDR\_C are expected to be powered by the same source such that they ramp together.
8. VDD\_CORE and VDDR\_CORE are expected to be powered by the same source such that they ramp together.
9. VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.

### 7.10.2.3 Power-Down Sequencing

Figure 7-4 describes the device power-down sequencing.



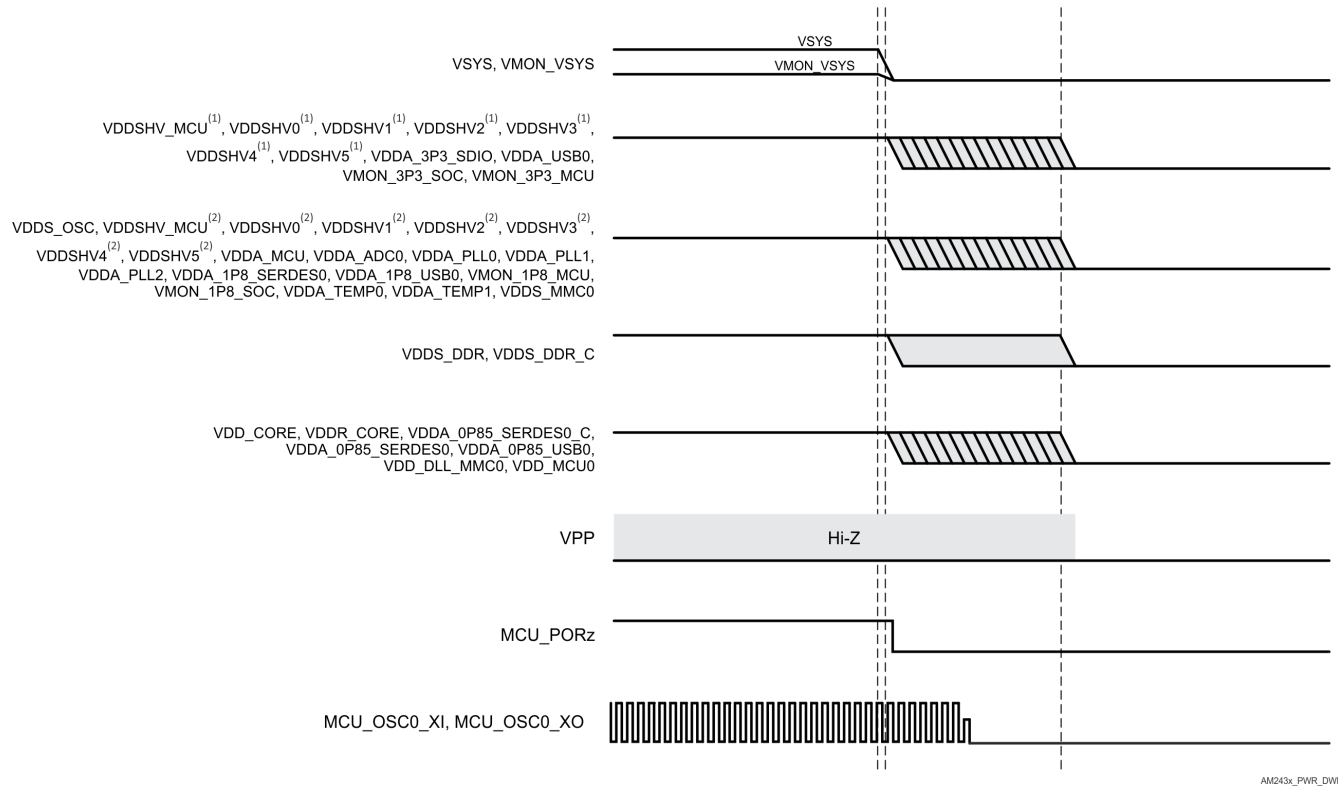


Figure 7-4. Power-Down Sequencing

1. VDDSHV\_MCU and VDDSHVx [x=0-5] when operating at 3.3V.
2. VDDSHV\_MCU and VDDSHVx [x=0-5] when operating at 1.8V.

### 7.10.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 7-5. System Timing Conditions

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>I</sub>	Input slew rate	0.5	2	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	3	30	pF

#### 7.10.3.1 Reset Timing

Tables and figures provided in this section define timing requirements and switching characteristics for reset related signals.

Table 7-6. MCU\_PORz Timing Requirements

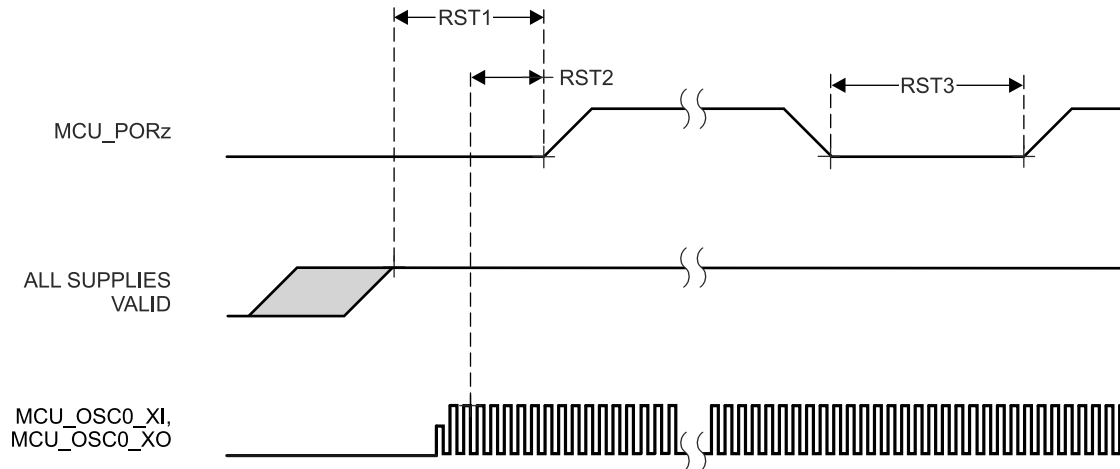
see Figure 7-5

NO.		MIN	MAX	UNIT
RST1	Hold time, MCU_PORz active (low) at Power-up after supplies valid (using external crystal)	9500000		ns
RST2	t <sub>h</sub> (SUPPLIES_VALID - MCU_PORz) Hold time, MCU_PORz active (low) at Power-up after supplies valid and external clock stable (using external LVCMOS oscillator)	1200		ns

**Table 7-6. MCU\_PORz Timing Requirements (continued)**

see Figure 7-5

NO.			MIN	MAX	UNIT
RST3	$t_w(\text{MCU\_PORzL})$	Pulse Width minimum, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)	1200		ns



**Figure 7-5. MCU\_PORz Timing Requirements**

**Table 7-7. MCU\_RESETSTATz, and RESETSTATz Switching Characteristics**

see Figure 7-6

NO.	PARAMETER	MIN	MAX	UNIT
RST4	$t_d(\text{MCU\_PORzL-MCU\_RESETSTATzL})$	0		ns
RST5	$t_d(\text{MCU\_PORzH-MCU\_RESETSTATzH})$	$6120 \cdot S^{(1)}$		ns
RST6	$t_d(\text{MCU\_PORzL-RESETSTATzL})$	0		ns
RST7	$t_d(\text{MCU\_PORzH-RESETSTATzH})$	$9195 \cdot S^{(1)}$		ns
RST8	$t_w(\text{MCU\_RESETSTATzL})$	$4040 \cdot S^{(1)}$		ns
RST9	$t_w(\text{RESETSTATzL})$	301200		ns

(1) S = MCU\_OSC0\_XI/XO clock period

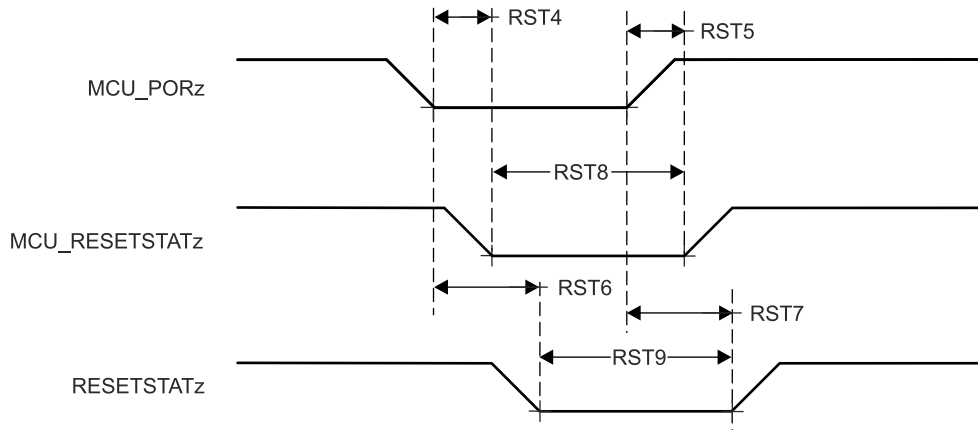


Figure 7-6. MCU\_RESETSTATz, and RESETSTATz Switching Characteristics

Table 7-8. MCU\_RESETz Timing Requirements

see Figure 7-7

NO.	PARAMETER	MIN	MAX	UNIT
RST10	$t_w(\text{MCU\_RESETzL})^{(1)}$	Pulse Width minimum, MCU_RESETz active (low)	1200	ns

(1) This timing parameter is valid only after all supplies are valid and MCU\_PORz has been asserted for the specified time.

Table 7-9. MCU\_RESETSTATz, and RESETSTATz Switching Characteristics

see Figure 7-7

NO.	PARAMETER	MIN	MAX	UNIT
RST11	$t_d(\text{MCU\_RESETzL-MCU\_RESETSTATzL})$	Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)	0	ns
RST12	$t_d(\text{MCU\_RESETzH-MCU\_RESETSTATzH})$	Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high)	$966 * S^{(1)}$	ns
RST13	$t_d(\text{MCU\_RESETzL-RESETSTATzL})$	Delay time, MCU_RESETz active (low) to RESETSTATz active (low)	0	ns
RST14	$t_d(\text{MCU\_RESETzH-RESETSTATzH})$	Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)	$4040 * S^{(1)}$	ns

(1) S = MCU\_OSC0\_XI/XO clock period

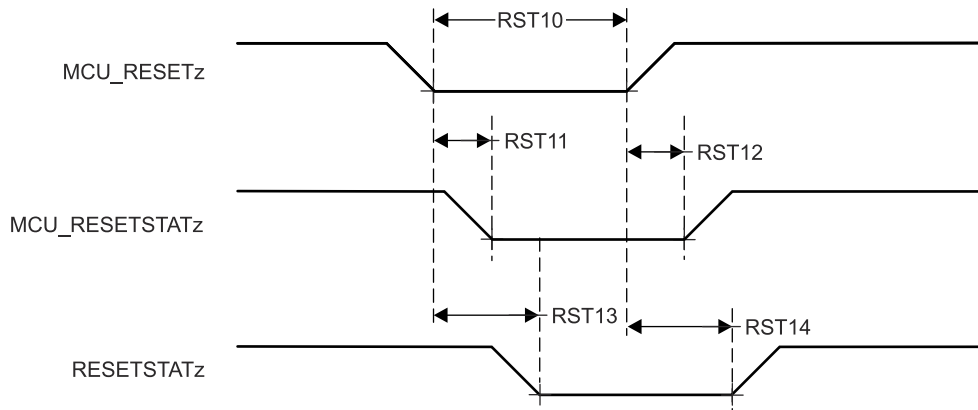


Figure 7-7. MCU\_RESETz, MCU\_RESETSTATz, and RESETSTATz Timing Requirements and Switching Characteristics

**Table 7-10. RESET\_REQz Timing Requirements**

see Figure 7-8

NO.	PARAMETER	MIN	MAX	UNIT
RST15	$t_{w(RESSET\_REQzL)}$ <sup>(1)</sup>	Pulse Width minimum, RESET_REQz active (low)	1200	ns

(1) This timing parameter is valid only after all supplies are valid and MCU\_PORz has been asserted for the specified time.

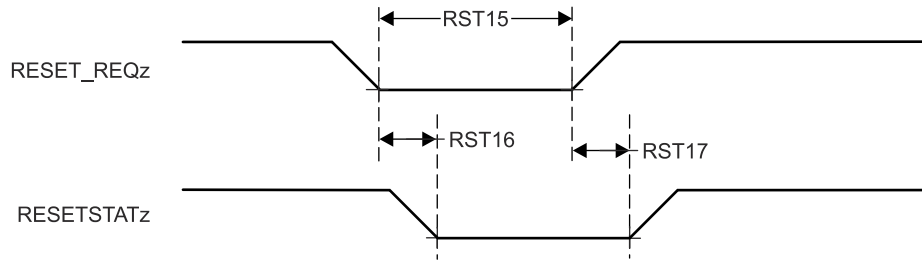
**Table 7-11. RESETSTATz Switching Characteristics**

see Figure 7-8

NO.	PARAMETER	MIN	MAX	UNIT
RST16	$t_{d(RESSET\_REQzL-RESETSTATzL)}$	Delay time, RESET_REQz active (low) to RESETSTATz active (low)	T <sup>(1)</sup>	ns
RST17	$t_{d(RESSET\_REQzH-RESETSTATzH)}$	Delay time, RESET_REQz inactive (high) to RESETSTATz inactive (high)	W <sup>(2)</sup>	ns

(1) T = Reset Isolation Time (Software Dependent)

(2) W = Max [300 μs (Typical) from RESETz\_REQz inactive (high), Reset Isolation Time + 300 μs (TYP) from RESET\_REQz active (low)]



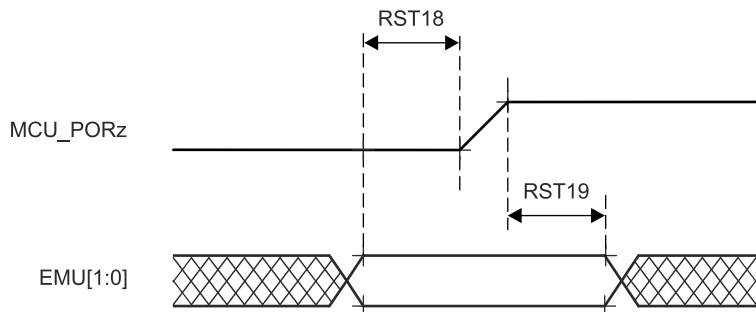
**Figure 7-8. RESET\_REQz and RESETSTATz Timing Requirements and Switching Characteristics**

**Table 7-12. EMUx Timing Requirements**

see Figure 7-9

NO.	PARAMETER	MIN	MAX	UNIT
RST18	$t_{su(EMUx-MCU\_PORz)}$	Setup time, EMU[1:0] before MCU_PORz inactive (high)	3*S <sup>(1)</sup>	ns
RST19	$t_{h(MCU\_PORz - EMUx)}$	Hold time, EMU[1:0] after MCU_PORz inactive (high)	10	ns

(1) S = MCU\_OSC0\_XI/XO clock period



**Figure 7-9. EMUx Timing Requirements**

**Table 7-13. BOOTMODE Timing Requirements**

see Figure 7-10

NO.	PARAMETER	MIN	MAX	UNIT
RST23	$t_{su(BOOTMODE-PORz\_OUT)}$	Setup time, BOOTMODE[15:00] before PORz_OUT high (External MCU PORz event or Software SW_MAIN_PORz)	3*S <sup>(1)</sup>	ns

**Table 7-13. BOOTMODE Timing Requirements (continued)**

see [Figure 7-10](#)

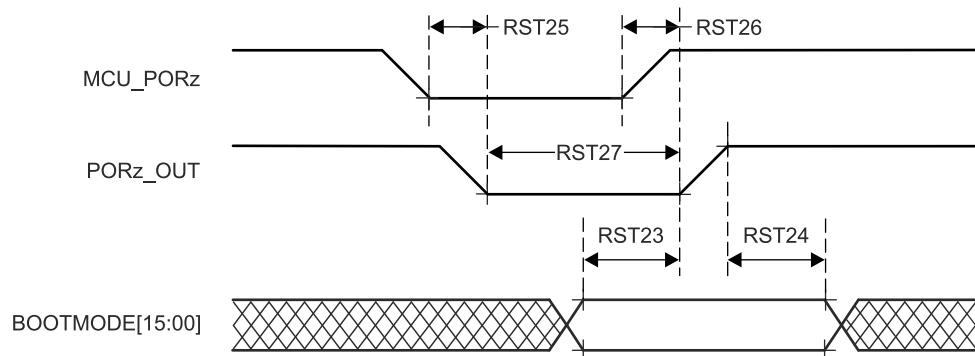
NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RST24	$t_{n(PORz\_OUT - BOOTMODE)}$	Hold time, BOOTMODE[15:00] after PORz_OUT high (External MCU PORz event, Software SW_MAIN_PORz)	0		ns

(1) S = MCU\_OSC0\_XI/XO clock period

**Table 7-14. PORz\_OUT Switching Characteristics**

see [Figure 7-10](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RST25	$t_{d(MCU\_PORzL-PORz\_OUT)}$	Delay time, MCU_PORz active (low) to PORz_OUT active (low)	0		ns
RST26	$t_{d(MCU\_PORzH-PORz\_OUT)}$	Delay time, MCU_PORz inactive (high) to PORz_OUT inactive (high)	0		ns
RST27	$t_{w(PORz\_OUTL)}$	Pulse Width Minimum PORz_OUT low (MCU_PORz, SW_MAIN_PORz)	1200		ns



**Figure 7-10. BOOTMODE Timing Requirements and PORz\_OUT Switching Characteristics**

### 7.10.3.2 Safety Signal Timing

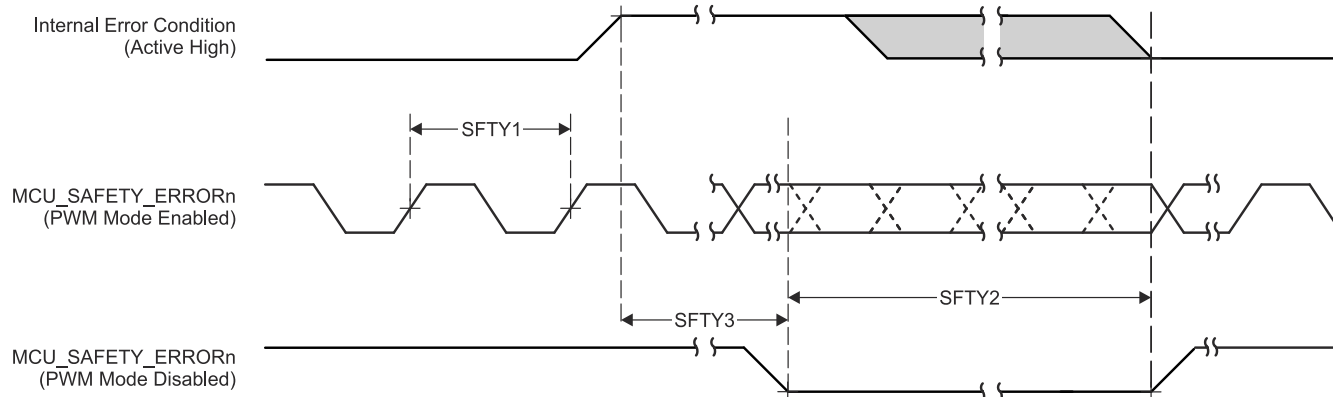
Tables and figures provided in this section define switching characteristics for MCU\_SAFETY\_ERRORn.

**Table 7-15. MCU\_SAFETY\_ERRORn Switching Characteristics**

see [Figure 7-11](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SFTY1	$t_{c(MCU\_SAFETY\_ERRORn)}$	Cycle time minimum, MCU_SAFETY_ERRORn (PWM mode enabled)	$(P*H)+(P*L)^{(1) (3) (4)}$		ns
SFTY2	$t_{w(MCU\_SAFETY\_ERRORn)}$	Pulse width minimum, MCU_SAFETY_ERRORn active (PWM mode disabled) <sup>(5)</sup>	$P*R^{(1) (2)}$		ns
SFTY3	$t_{d(ERROR\_CONDITION-MCU\_SAFETY\_ERRORnL)}$	Delay time, ERROR CONDITION to MCU_SAFETY_ERRORn active <sup>(5)</sup>	$50*P^{(1)}$		ns

- (1) P = ESM functional clock
- (2) R = Error Pin Counter Pre-Load Register count value
- (3) H = Error Pin PWM High Pre-Load Register count value
- (4) L = Error Pin PWM Low Pre-Load Register count value
- (5) When PWM mode is enabled, MCU\_SAFETY\_ERRORn stops toggling after RST22 and will maintain its value (either high or low) until the error is cleared. When PWM mode is disabled, MCU\_SAFETY\_ERRORn is active low.


**Figure 7-11. MCU\_SAFETY\_ERRORn Timing Requirements and Switching Characteristics**

### 7.10.3.3 Clock Timing

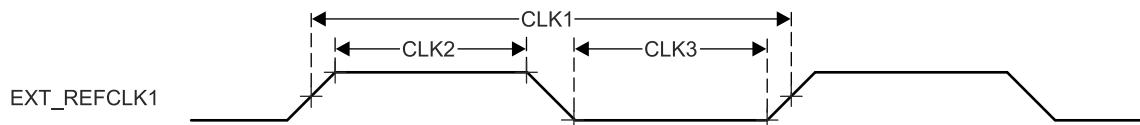
Tables and figures provided in this section define timing requirements and switching characteristics for clock signals.

**Table 7-16. Clock Timng Requiements**

see [Figure 7-12](#)

NO.			MIN	MAX	UNIT
CLK1	$t_{c(EXT\_REFCLK1)}$	Cycle time minimum, EXT_REFCLK1	10		ns
CLK2	$t_{w(EXT\_REFCLK1H)}$	Pulse Duration minimum, EXT_REFCLK1 high	$E*0.45^{(1)}$	$E*0.55^{(1)}$	ns
CLK3	$t_{w(EXT\_REFCLK1L)}$	Pulse Duration minimum, EXT_REFCLK1 low	$E*0.45^{(1)}$	$E*0.55^{(1)}$	ns

(1) E = EXT\_REFCLK1 cycle time


**Figure 7-12. Clock Timing Requirements**
**Table 7-17. Clock Switching Characteristics**

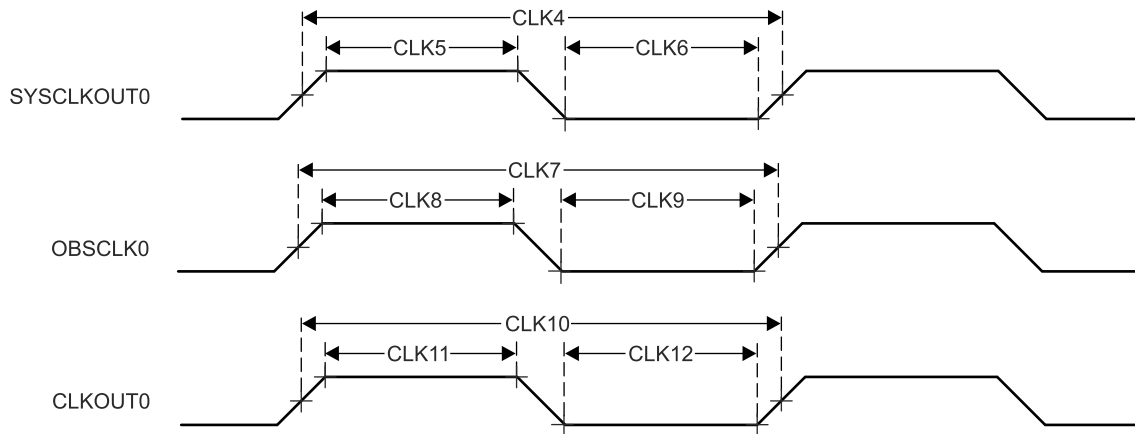
see [Figure 7-13](#)

NO.	PARAMETER		MIN	MAX	UNIT
CLK4	$t_{c(SYSCCLKOUT0)}$	Cycle time minimum, SYSCCLKOUT0	8		ns
CLK5	$t_{w(SYSCCLKOUT0H)}$	Pulse Duration minimum, SYSCCLKOUT0 high	$A*0.4^{(1)}$	$A*0.6^{(1)}$	ns
CLK6	$t_{w(SYSCCLKOUT0L)}$	Pulse Duration minimum, SYSCCLKOUT0 low	$A*0.4^{(1)}$	$A*0.6^{(1)}$	ns
CLK7	$t_{c(OBSCLK0)}$	Cycle time minimum, OBSCLK0	5		ns
CLK8	$t_{w(OBSCLK0H)}$	Pulse Duration minimum, OBSCLK0 high	$B*0.45^{(2)}$	$B*0.55^{(2)}$	ns
CLK9	$t_{w(OBSCLK0L)}$	Pulse Duration minimum, OBSCLK0 low	$B*0.45^{(2)}$	$B*0.55^{(2)}$	ns
CLK10	$t_{c(CLKOUT0)}$	Cycle time minimum, CLKOUT0	20		ns
CLK11	$t_{w(CLKOUT0H)}$	Pulse Duration minimum, CLKOUT0 high	$C*0.4^{(3)}$	$C*0.6^{(3)}$	ns
CLK12	$t_{w(CLKOUT0L)}$	Pulse Duration minimum, CLKOUT0 low	$C*0.4^{(3)}$	$C*0.6^{(3)}$	ns

(1) A = SYSCCLKOUT0 cycle time

(2) B = OBSCLK0 cycle time

(3) C = CLKOUT0 cycle time



**Figure 7-13. Clock Switching Characteristics**

## 7.10.4 Clock Specifications

### 7.10.4.1 Input Clocks / Oscillators

Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- MCU\_OSC0\_XI/MCU\_OSC0\_XO — External main crystal interface pins connected to the internal high-frequency oscillator (MCU\_HFOSC0), which is the default clock source for internal reference clock MCU\_HFOSC0\_CLKOUT.
- General purpose clock inputs
  - MCU\_EXT\_REFCLK0 — Optional external system clock input for MCU domain.
  - EXT\_REFCLK1 — Optional external system clock input for MAIN domain.
  - SERDES0\_REFCLK0P/N — Optional SERDES0 reference clock input for PCIe.
- External CPTS reference clock inputs
  - CP\_GEMAC\_CPTS0\_RFT\_CLK — CPTS reference clock input.
  - CPTS\_RFT\_CLK — CPTS reference clock input.

Figure 7-14 shows the external input clock sources and the output clocks to peripherals.

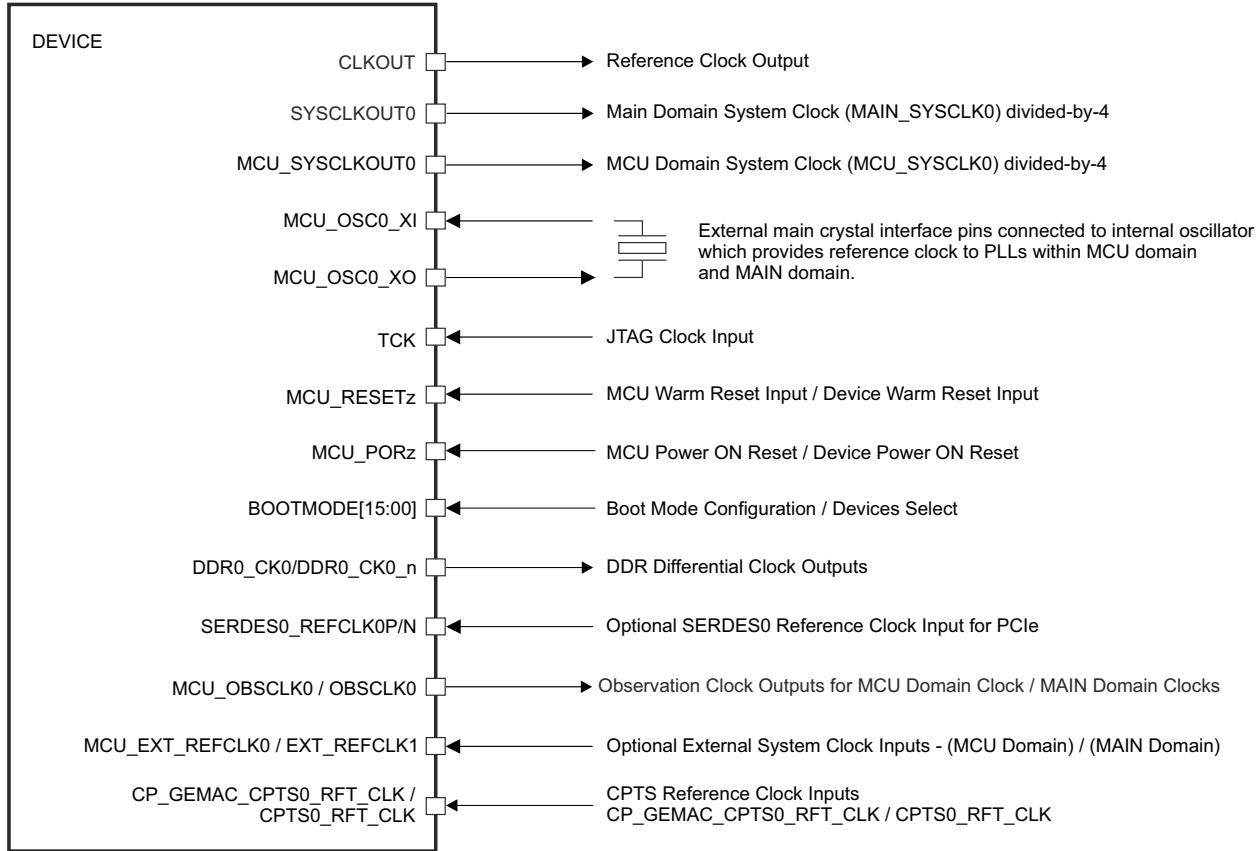


Figure 7-14. Input Clocks Interface

For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

#### 7.10.4.1.1 MCU\_OSC0 Internal Oscillator Clock Source

Figure 7-15 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit should be placed as close as possible to the MCU\_OSC0\_XI and MCU\_OSC0\_XO pins.

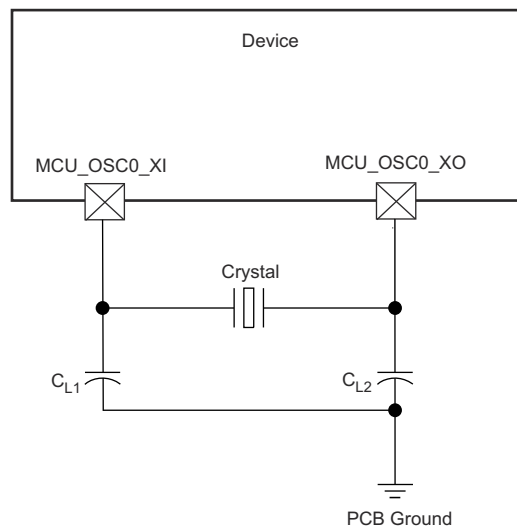


Figure 7-15. MCU\_OSC0 Crystal Implementation



The crystal must be in the fundamental mode of operation and parallel resonant. Table 7-18 summarizes the required electrical constraints.

**Table 7-18. MCU\_OSC0 Crystal Circuit Requirements**

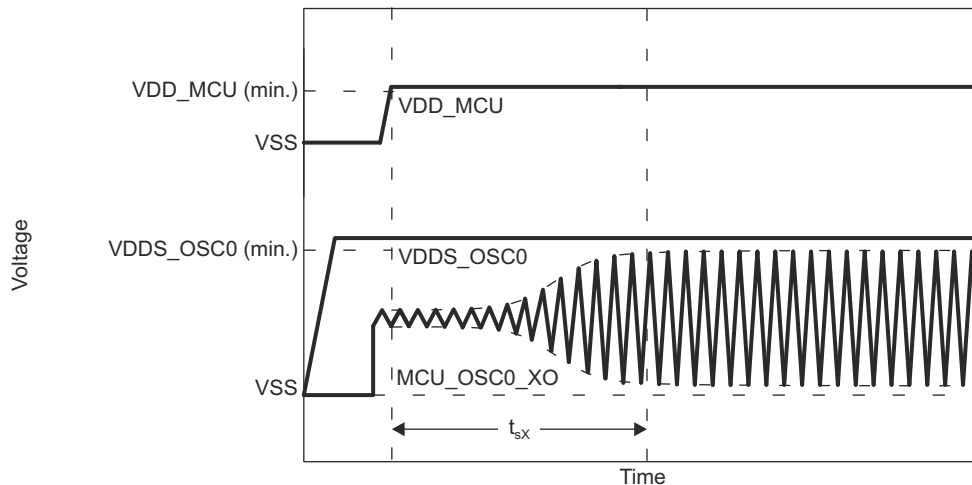
PARAMETER		MIN	TYP	MAX	UNIT
F <sub>xtal</sub>	Crystal Parallel Resonance Frequency	25			MHz
F <sub>xtal</sub>	Crystal Frequency Stability and Tolerance	Ethernet RGMII and RMII not used		±100	ppm
		Ethernet RGMII and RMII using derived clock		±50	
C <sub>L1+PCBXI</sub>	Capacitance of C <sub>L1</sub> + C <sub>PCBXI</sub>	12		24	pF
C <sub>L2+PCBXO</sub>	Capacitance of C <sub>L2</sub> + C <sub>PCBXO</sub>	12		24	pF
C <sub>L</sub>	Crystal Load Capacitance	6		12	pF
C <sub>shunt</sub>	Crystal Circuit Shunt Capacitance	ESR <sub>xtal</sub> = 30 Ω	25 MHz	7	pF
		ESR <sub>xtal</sub> = 40 Ω	25 MHz	5	pF
		ESR <sub>xtal</sub> = 50 Ω	25 MHz	5	pF
ESR <sub>xtal</sub>	Crystal Effective Series Resistance			100	Ω

When selecting a crystal, the system design must consider temperature and aging characteristics of the crystal based on worst case environment and expected life expectancy of the system.

Table 7-19 details the switching characteristics of the oscillator.

**Table 7-19. MCU\_OSC0 Switching Characteristics - Crystal Mode**

PARAMETER		MIN	TYP	MAX	UNIT
C <sub>XI</sub>	XI Capacitance			1.44	pF
C <sub>XO</sub>	XO Capacitance			1.52	pF
C <sub>XIXO</sub>	XI to XO Mutual Capacitance			0.01	pF
t <sub>s</sub>	Start-up Time		4		ms

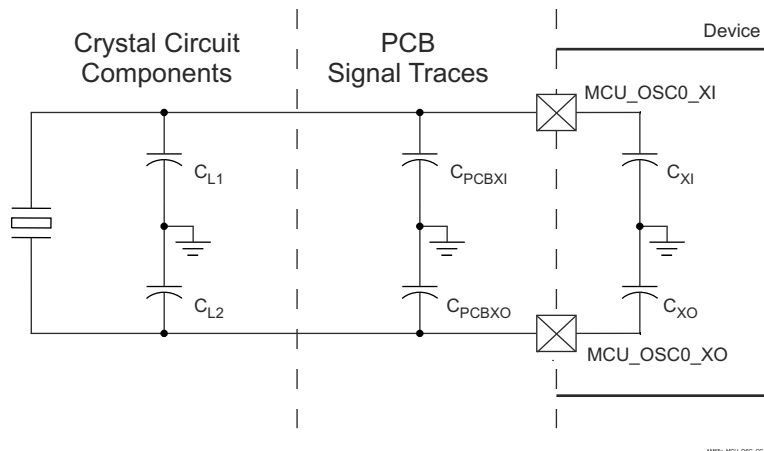


**Figure 7-16. MCU\_OSC0 Start-up Time**

#### 7.10.4.1.1.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C<sub>L</sub>, of this circuit is a combination of discrete capacitors C<sub>L1</sub>, C<sub>L2</sub>, and several parasitic contributions. PCB signal traces which connect crystal circuit components to MCU\_OSC0\_XI and MCU\_OSC0\_XO have parasitic capacitance to ground, C<sub>PCBXI</sub> and C<sub>PCBXO</sub>, where the

PCB designer should be able to extract parasitic capacitance for each signal trace. The MCU\_OSC0 circuits and device package have combined parasitic capacitance to ground,  $C_{PCBXI}$  and  $C_{PCBXO}$ , where these parasitic capacitance values are defined in [Table 7-19](#).



**Figure 7-17. Load Capacitance**

Load capacitors,  $C_{L1}$  and  $C_{L2}$  in [Figure 7-15](#), should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of  $C_{L1}$  and  $C_{L2}$ , multiply the capacitive load value  $C_L$  by 2. Using this result, subtract the combined values of  $C_{PCBXI} + C_{XI}$  to determine the value of  $C_{L1}$  and the combined values of  $C_{PCBXO} + C_{XO}$  to determine the value of  $C_{L2}$ . For example, if  $C_L = 10$  pF,  $C_{PCBXI} = 2.9$  pF,  $C_{XI} = 0.5$  pF,  $C_{PCBXO} = 3.7$  pF,  $C_{XO} = 0.5$  pF, the value of  $C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 \times 10 \text{ pF}) - 2.9 \text{ pF} - 0.5 \text{ pF}] = 16.6$  pF and  $C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10 \text{ pF}) - 3.7 \text{ pF} - 0.5 \text{ pF}] = 15.8$  pF

#### 7.10.4.1.1.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for MCU\_OSC0 operating conditions defined in [Table 7-18](#). Shunt capacitance,  $C_{shunt}$ , of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to MCU\_OSC0 have mutual parasitic capacitance to each other,  $C_{PCBXIXO}$ , where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance,  $C_{XIXO}$ , where this mutual parasitic capacitance value is defined in [Table 7-19](#).

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

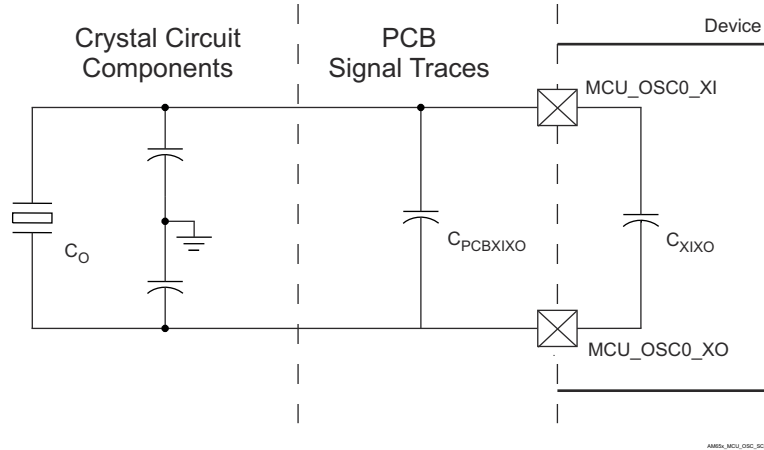


Figure 7-18. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied.  $C_O$  in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$$C_{\text{shunt}} \geq C_O + C_{\text{PCBXIXO}} + C_{\text{XIXO}}$$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30  $\Omega$ ,  $C_{\text{PCBXIXO}} = 0.04$  pF,  $C_{\text{XIXO}} = 0.01$  pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

#### 7.10.4.1.2 MCU\_OSC0 LVCMOS Digital Clock Source

Figure 7-19 shows the recommended oscillator connections when MCU\_OSC0\_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

#### Note

A DC steady-state condition is not allowed on MCU\_OSC0\_XI when the oscillator is powered up. This is not allowed because MCU\_OSC0\_XI is internally AC coupled to a comparator that may enter a unknown state when DC is applied to the input. Therefore, application software should power down MCU\_OSC0 any time MCU\_OSC0\_XI is not toggling between logic states.

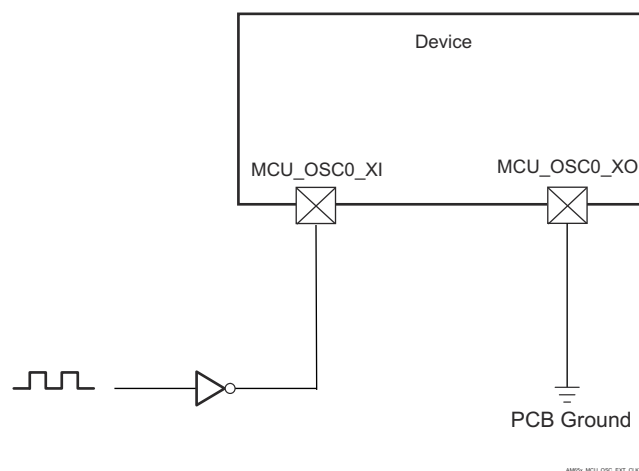


Figure 7-19. 1.8-V LVCMOS-Compatible Clock Input

### 7.10.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU\_SYCLKOUT0**
  - MCU\_SYCLKOUT0 is the MCU Domain system clock (MCU\_SYCLK0) divided-by-4. This clock output is provided for test and debug purposes only.
- **MCU\_OBSCLK0**
  - Observation clock output for test and debug purposes only.
- **SYCLKOUT0**
  - SYCLKOUT0 is the Main domain system clock (MAIN\_SYCLK0) divided-by-4. This clock output is provided for test and debug purposes only.
- **CLKOUT0**
  - CLKOUT0 is the Ethernet Subsystem clock (MAIN\_PLL0\_HSDIV4\_CLKOUT) divided-by-5 or divided-by-10. This clock output was provided to source to the external PHY. When configured to operate as the RMIIClock source (50 MHz), it must also be routed back to the RMIICLK pin for proper device operation.
- **OBSCCLK0**
  - Observation clock output for test and debug purposes only.
- **GPMC\_FCLK\_MUX**
  - GPMC\_FCLK\_MUX is the GPMC0 functional clock (GPMC\_FCLK). This clock is provided as an alternative GPMC interface clock when attached devices require a continuous running clock.

For more information, see *Clock Outputs* section in *Clocking* chapter and *GPMC Clock Configuration* section in *Peripherals* chapter in the device TRM.

### 7.10.4.3 PLLs

Power is supplied to the Phase-Locked Loop circuits (PLLs) by internal regulators that derive their power from off-chip power-sources.

There is one PLL in the MCU domain:

- MCU0\_PLL

There are six PLLs in the MAIN domain:

- ARM0\_PLL
- MAIN\_PLL
- PER0\_PLL
- PER1\_PLL
- DDR PLL
- R5F PLL

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#### Note

For more information, see:

- *Device Configuration / Clocking / PLLs* section in the device TRM.
  - *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU\_ICSSG)* section in the device TRM.
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#### Note

The input reference clock (MCU\_OSC0\_XI / MCU\_OSC0\_XO) is specified and the lock time is ensured by the PLL controller, as documented in the *Device Configuration* chapter in the device TRM.

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## 7.10.5 Peripherals

### 7.10.5.1 CPSW3G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

#### 7.10.5.1.1 CPSW3G MDIO Timing

Table 7-20, Table 7-21, Table 7-22, and Figure 7-20 present timing conditions, requirements, and switching characteristics for CPSW3G MDIO.

**Table 7-20. CPSW3G MDIO Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>i</sub>	Input slew rate	0.9	3.6	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	10	470	pF

**Table 7-21. CPSW3G MDIO Timing Requirements**

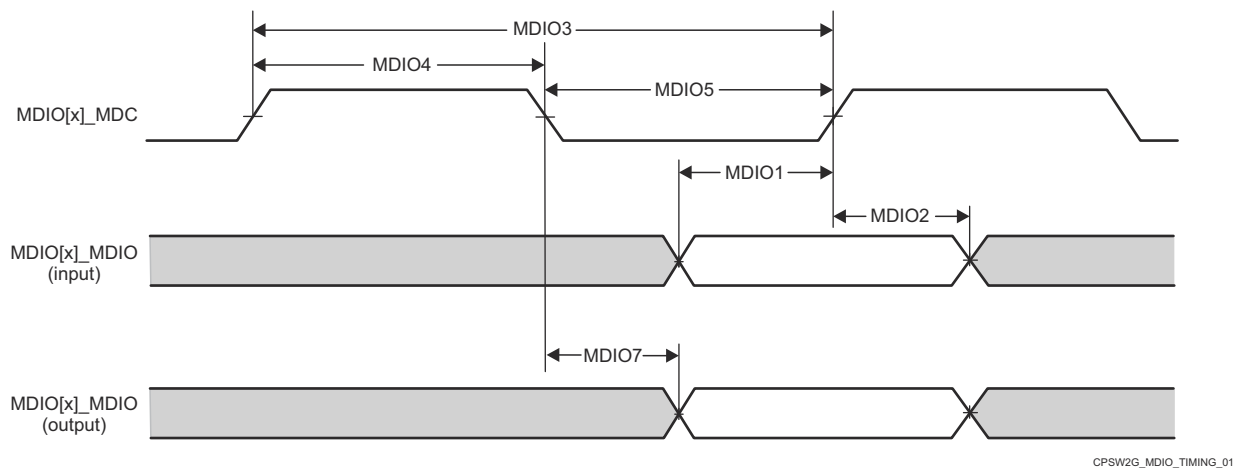
see Figure 7-20

NO.	PARAMETER	MIN	MAX	UNIT
MDIO1	t <sub>su</sub> (MDIO_MDC)	90		ns
MDIO2	t <sub>h</sub> (MDC_MDIO)	0		ns

**Table 7-22. CPWS3G MDIO Switching Characteristics**

see Figure 7-20

NO.	PARAMETER	MIN	MAX	UNIT
MDIO3	t <sub>c</sub> (MDC)	400		ns
MDIO4	t <sub>w</sub> (MDCH)	160		ns
MDIO5	t <sub>w</sub> (MDCL)	160		ns
MDIO7	t <sub>d</sub> (MDC_MDIO)	-150	150	ns



**Figure 7-20. CPSW3G MDIO Timing Requirements and Switching Characteristics**

#### 7.10.5.1.2 CPSW3G RMII Timing

Table 7-23, Table 7-24, Figure 7-21, Table 7-25, Figure 7-22 Table 7-26, and Figure 7-23 present timing conditions, requirements, and switching characteristics for CPSW3G RMII.

**Table 7-23. CPSW3G RMIITiming Conditions**

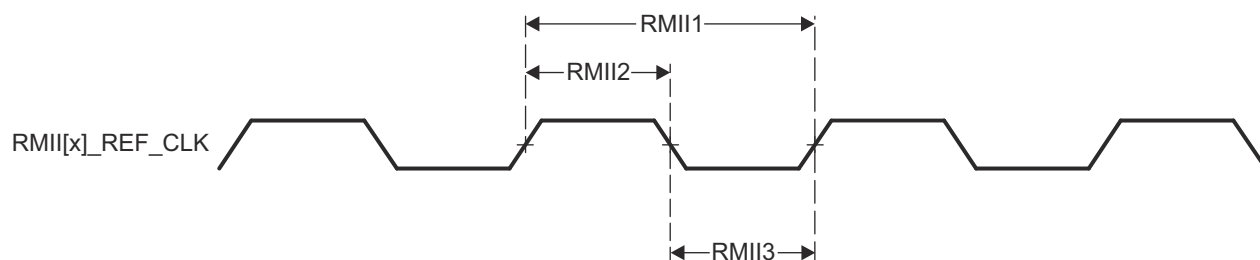
PARAMETER		MIN	MAX	UNIT	
<b>INPUT CONDITIONS</b>					
SR <sub>i</sub>	Input slew rate	VDDSHV <sub>x</sub> <sup>(1)</sup> = 1.8V	0.18	0.54	V/ns
		VDDSHV <sub>x</sub> <sup>(1)</sup> = 3.3V	0.4	1.2	V/ns
<b>OUTPUT CONDITIONS</b>					
C <sub>L</sub>	Output load capacitance	3	25	pF	

(1) x = 0 - 5, where x indicates the respective IO power rail. Refer to the *Pin Attributes* section, for more information on IO power rail assignments.

**Table 7-24. RMII[x]\_REF\_CLK Timing Requirements – RMII Mode**

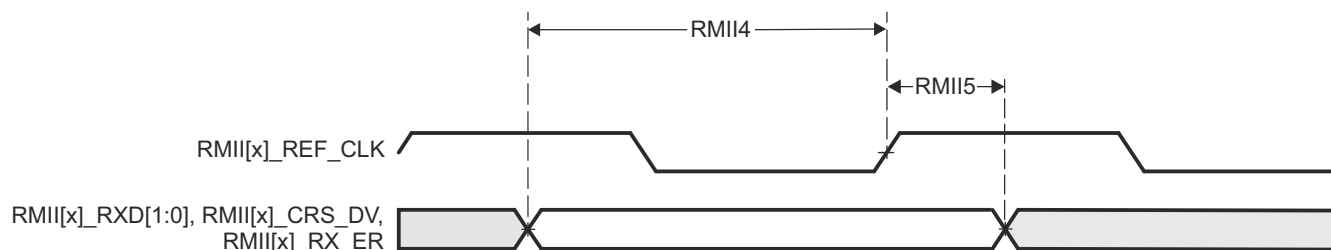
 see [Figure 7-21](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	t <sub>c</sub> (REF_CLK)	Cycle time, RMII[x]_REF_CLK	19.999	20.001	ns
RMII2	t <sub>w</sub> (REF_CLKH)	Pulse Duration, RMII[x]_REF_CLK High	7	13	ns
RMII3	t <sub>w</sub> (REF_CLKL)	Pulse Duration, RMII[x]_REF_CLK Low	7	13	ns


**Figure 7-21. CPSW3G RMII[x]\_REF\_CLK Timing Requirements – RMII Mode**
**Table 7-25. RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, and RMII[x]\_RX\_ER Timing Requirements – RMII Mode**

 see [Figure 7-22](#)

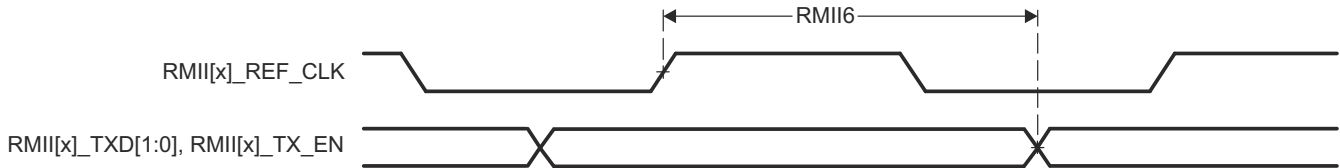
NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII4	t <sub>su</sub> (RXD-REF_CLK)	Setup time, RMII[x]_RXD[1:0] valid before RMII[x]_REF_CLK	4		ns
	t <sub>su</sub> (CRS_DV-REF_CLK)	Setup time, RMII[x]_CRS_DV valid before RMII[x]_REF_CLK	4		ns
	t <sub>su</sub> (RX_ER-REF_CLK)	Setup time, RMII[x]_RX_ER valid before RMII[x]_REF_CLK	4		ns
RMII5	t <sub>h</sub> (REF_CLK-RXD)	Hold time RMII[x]_RXD[1:0] valid after RMII[x]_REF_CLK	2		ns
	t <sub>h</sub> (REF_CLK-CRS_DV)	Hold time, RMII[x]_CRS_DV valid after RMII[x]_REF_CLK	2		ns
	t <sub>h</sub> (REF_CLK-RX_ER)	Hold time, RMII[x]_RX_ER valid after RMII[x]_REF_CLK	2		ns


**Figure 7-22. CPSW3G RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, RMII[x]\_RX\_ER Timing Requirements – RMII Mode**

**Table 7-26. RMII[x]\_TXD[1:0], and RMII[x]\_TX\_EN Switching Characteristics – RMII Mode**

see [Figure 7-23](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII6	$t_{d(REF\_CLK-TXD)}$	Delay time, RMII[x]_REF_CLK High to RMII[x]_TXD[1:0] valid	2	10	ns
	$t_{d(REF\_CLK-TX\_EN)}$	Delay time, RMII[x]_REF_CLK to RMII[x]_TX_EN valid	2	10	ns



**Figure 7-23. RMII[x]\_TXD[1:0], and RMII[x]\_TX\_EN Switching Characteristics – RMII Mode**

### 7.10.5.1.3 CPSW3G RGMII Timing

[Table 7-27](#), [Table 7-28](#), [Table 7-29](#), [Figure 7-24](#), [Table 7-30](#), [Table 7-31](#), and [Figure 7-25](#) present timing conditions, requirements, and switching characteristics for CPSW3G RGMII.

**Table 7-27. CPSW3G RGMII Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
$SR_i$	Input slew rate	2.64	5	V/ns
<b>OUTPUT CONDITIONS</b>				
$C_L$	Output load capacitance	2	20	pF
<b>PCB CONNECTIVITY REQUIREMENTS</b>				
$t_{d(\text{Trace Mismatch Delay})}$	Propagation delay mismatch across all traces	RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL	50	ps
		RGMII[x]_TXC, RGMII[x]_TD[3:0], RGMII[x]_TX_CTL	50	ps

**Table 7-28. RGMII[x]\_RXC Timing Requirements – RGMII Mode**

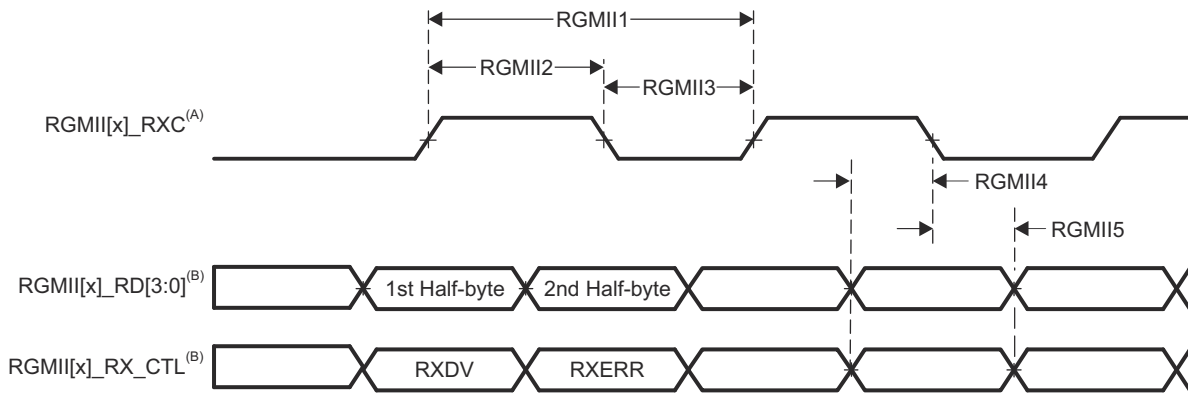
see [Figure 7-24](#)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, RGMII[x]_RXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII2	$t_{w(RXCH)}$	Pulse duration, RGMII[x]_RXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII3	$t_{w(RXCL)}$	Pulse duration, RGMII[x]_RXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

**Table 7-29. RGMII[x]\_RD[3:0], and RGMII[x]\_RX\_CTL Timing Requirements – RGMII Mode**

see Figure 7-24

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII4	$t_{su}(RD-RXC)$	Setup time, RGMII[x]_RD[3:0] valid before RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{su}(RX\_CTL-RXC)$	Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
RGMII5	$t_h(RXC-RD)$	Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_h(RXC-RX\_CTL)$	Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns



- A. RGMII[x]\_RXC must be externally delayed relative to the data and control pins.
- B. Data and control information is received using both edges of the clocks. RGMII[x]\_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]\_RXC and data bits 7-4 on the falling edge of RGMII[x]\_RXC. Similarly, RGMII[x]\_RX\_CTL carries RXDV on rising edge of RGMII[x]\_RXC and RXERR on falling edge of RGMII[x]\_RXC.

**Figure 7-24. CPSW3G RGMII[x]\_RXC, RGMII[x]\_RD[3:0], RGMII[x]\_RX\_CTL Timing Requirements - RGMII Mode**

**Table 7-30. RGMII[x]\_TXC Switching Characteristics – RGMII Mode**

see Figure 7-25

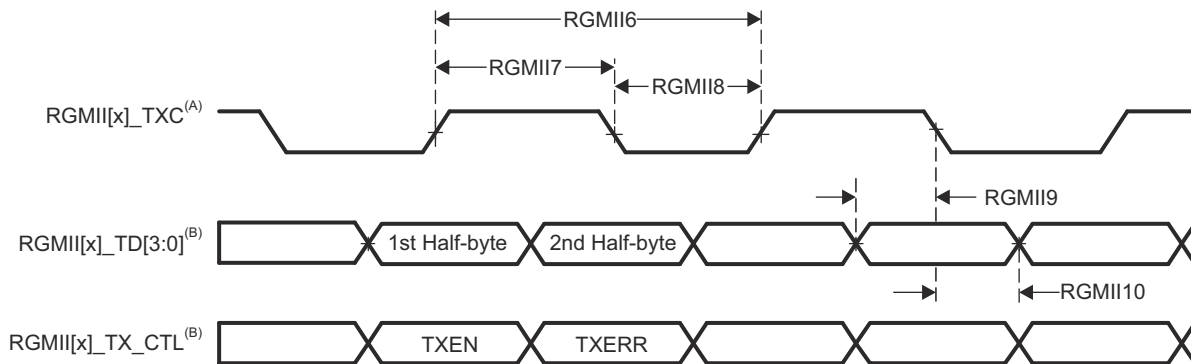
NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII6	$t_c(TXC)$	Cycle time, RGMII[x]_TXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII7	$t_w(TXCH)$	Pulse duration, RGMII[x]_TXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII8	$t_w(TXCL)$	Pulse duration, RGMII[x]_TXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns



**Table 7-31. RGMII[x]\_TD[3:0] and RGMII[x]\_TX\_CTL Switching Characteristics – RGMII Mode**

see [Figure 7-25](#)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII9	$t_{osu}(TD\_TXC)$	Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{osu}(TX\_CTL\_TXC)$	Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
RGMII10	$t_{oh}(TXC\_TD)$	Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{oh}(TXC\_TX\_CTL)$	Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns



- A. TXC is delayed internally before being driven to the RGMII[x]\_TXC pin. This internal delay is always enabled.  
 B. Data and control information is received using both edges of the clocks. RGMII[x]\_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]\_TXC and data bits 7-4 on the falling edge of RGMII[x]\_TXC. Similarly, RGMII[x]\_TX\_CTL carries TXEN on rising edge of RGMII[x]\_TXC and TXERR on falling edge of RGMII[x]\_TXC.

**Figure 7-25. CPSW3G RGMII[x]\_TXC, RGMII[x]\_TD[3:0], and RGMII[x]\_TX\_CTL Switching Characteristics - RGMII Mode**

### 7.10.5.2 DDRSS

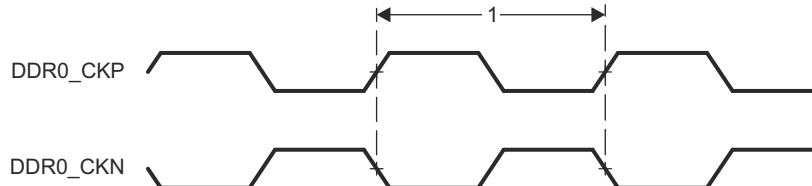
For more details about features and additional description information on the device (LP)DDR4 Memory Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

[Table 7-32](#) and [Figure 7-26](#) present switching characteristics for DDRSS.

**Table 7-32. DDRSS Switching Characteristics**

see [Figure 7-26](#)

NO.	PARAMETER	DESCRIPTION	DDR TYPE	MIN	MAX	UNIT
1	$t_c(DDR\_CKP/DDR\_CKN)$	Cycle time, DDR_CKP and DDR_CKN	LPDDR4	1.25	20	ns
			DDR4	1.25	1.6	ns



**Figure 7-26. DDRSS Switching Characteristics**

For more information, see *DDR Subsystem (DDRSS)* section in *Memory Controllers* chapter in the device TRM.

**7.10.5.3 ECAP**

Table 7-33, Table 7-34, Figure 7-27, Table 7-35, and Figure 7-28 present timing conditions, requirements, and switching characteristics for ECAP.

**Table 7-33. ECAP Timing Conditions**

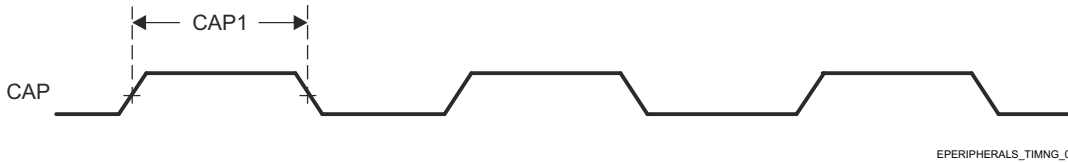
PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>i</sub>	Input slew rate	1	4	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	2	7	pF

**Table 7-34. ECAP Timing Requirements**

see Figure 7-27

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP1	t <sub>w</sub> (CAP)	Pulse duration, CAP (asynchronous)	2 + 2P <sup>(1)</sup>		ns

(1) P = sysclk period in ns.



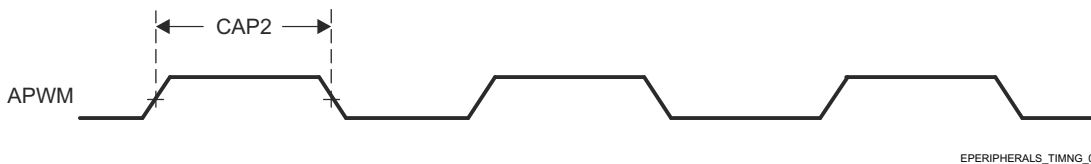
**Figure 7-27. ECAP Timings Requirements**

**Table 7-35. ECAP Switching Characteristics**

see Figure 7-28

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP2	t <sub>w</sub> (APWM)	Pulse duration, APWMx high/low	-2 + 2P <sup>(1)</sup>		ns

(1) P = sysclk period in ns.



**Figure 7-28. ECAP Switching Characteristics**

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

**7.10.5.4 EPWM**

Table 7-36, Table 7-37, Figure 7-29, Table 7-38, Figure 7-30, Figure 7-31, and Figure 7-32 present timing conditions, requirements, and switching characteristics for EPWM.

**Table 7-36. EPWM Timing Conditions**

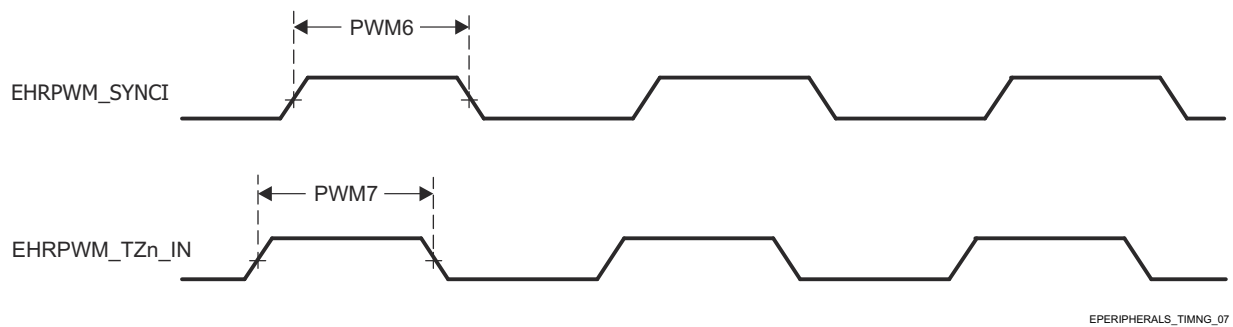
PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>I</sub>	Input slew rate	1	4	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	2	7	pF

**Table 7-37. EPWM Timing Requirements**

see [Figure 7-29](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM6	t <sub>w</sub> (SYNCIN)	Pulse duration, EHRPWM_SYNCIN	2 + 2P <sup>(1)</sup>		ns
PWM7	t <sub>w</sub> (TZ)	Pulse duration, EHRPWM_TZn_IN low	2 + 3P <sup>(1)</sup>		ns

(1) P = sysclk period in ns.



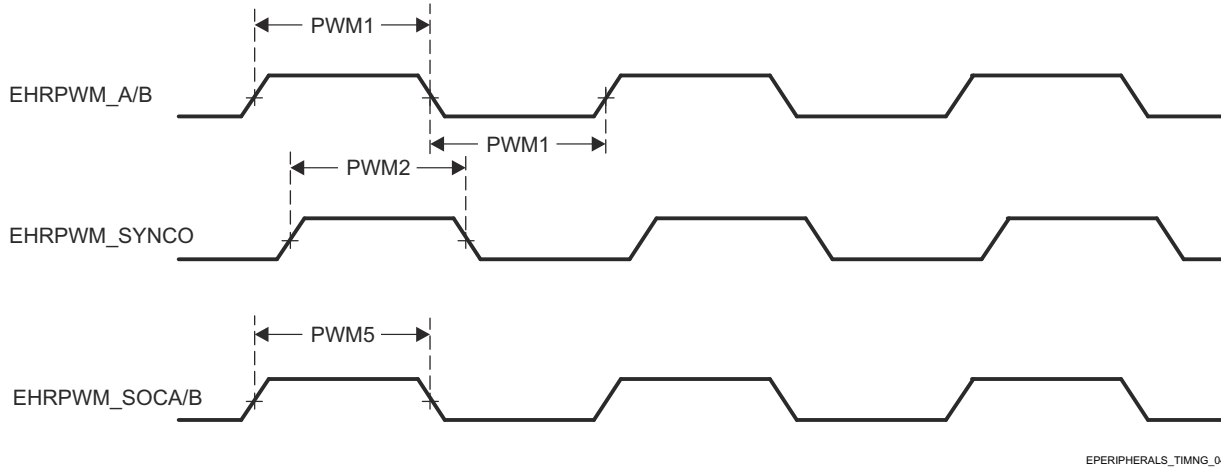
**Figure 7-29. EPWM Timing Requirements**

**Table 7-38. EPWM Switching Characteristics**

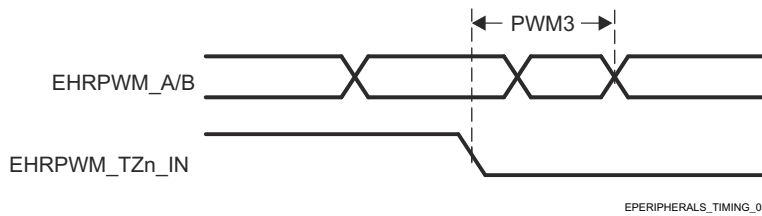
see [Figure 7-30](#), [Figure 7-31](#), and [Figure 7-32](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM1	t <sub>w</sub> (PWM)	Pulse duration, EHRPWM_A/B high/low	P - 3 <sup>(1)</sup>		ns
PWM2	t <sub>w</sub> (SYNCOU)	Pulse duration, EHRPWM_SYNCO	P - 3 <sup>(1)</sup>		ns
PWM3	t <sub>d</sub> (TZ-PWM)	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B forced high/low		11	ns
PWM4	t <sub>d</sub> (TZ-PWMZ)	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B Hi-Z		11	ns
PWM5	t <sub>w</sub> (SOC)	Pulse duration, EHRPWM_SOCA/B output	P - 3 <sup>(1)</sup>		ns

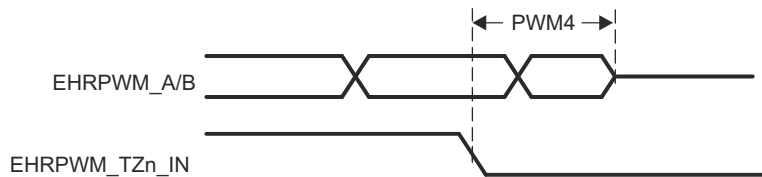
(1) P = sysclk period in ns.



**Figure 7-30. EHRPWM Switching Characteristics**



**Figure 7-31. EHRPWM\_TZn\_IN to EHRPWM\_A/B Forced Switching Characteristics**



**Figure 7-32. EHRPWM\_TZn\_IN to EHRPWM\_A/B Hi-Z Switching Characteristics**

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

**7.10.5.5 EQEP**

Table 7-39, Table 7-40, Figure 7-33, and Table 7-41 present timing conditions, requirements, and switching characteristics for EQEP.

**Table 7-39. EQEP Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>i</sub>	Input slew rate	1	4	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	2	7	pF

**Table 7-40. EQEP Timing Requirements**

see Figure 7-33

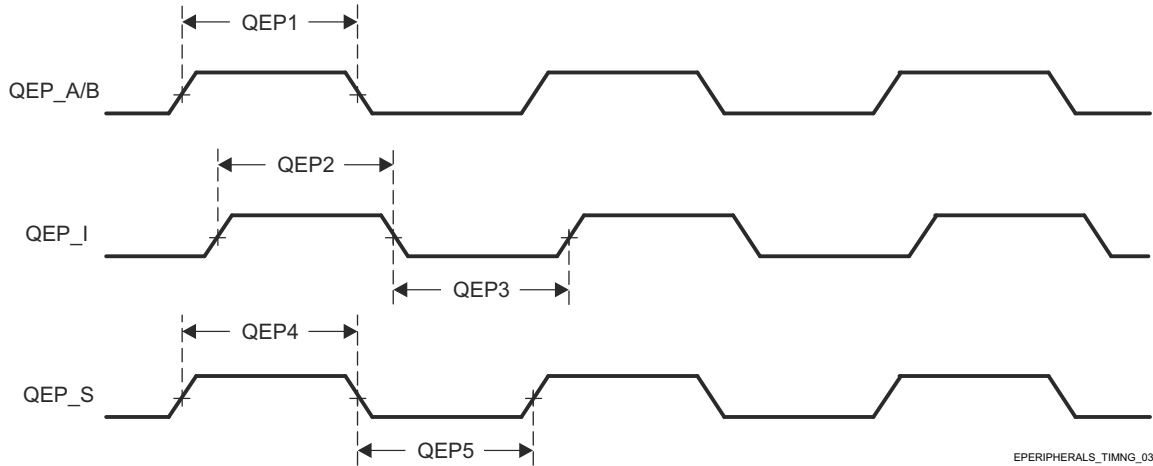
NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP1	t <sub>w(QEP)</sub>	Pulse duration, QEP_A/B	2 + 2P <sup>(1)</sup>		ns
QEP2	t <sub>w(QEPIH)</sub>	Pulse duration, QEP_I high	2 + 2P <sup>(1)</sup>		ns

**Table 7-40. EQEP Timing Requirements (continued)**

see [Figure 7-33](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP3	$t_{w(QEPIL)}$	Pulse duration, QEP_I low	$2 + 2P^{(1)}$		ns
QEP4	$t_{w(QEP SH)}$	Pulse duration, QEP_S high	$2 + 2P^{(1)}$		ns
QEP5	$t_{w(QEP SL)}$	Pulse duration, QEP_S low	$2 + 2P^{(1)}$		ns

(1) P = sysclk period in ns



**Figure 7-33. EQEP Timing Requirements**

**Table 7-41. EQEP Switching Characteristics**

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP6	$t_d(QEP-CNTR)$	Delay time, external clock to counter increment		24	ns

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

### 7.10.5.6 FSI

[Table 7-42](#), [Table 7-43](#), [Figure 7-34](#), [Table 7-44](#), [Figure 7-35](#), [Table 7-45](#), and [Figure 7-36](#) present timing conditions, requirements, and switching characteristics for FSI.

**Table 7-42. FSI Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>i</sub>	Input slew rate	0.8	4	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	1	7	pF

**Table 7-43. FSI Timing Requirements**

see [Figure 7-34](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FSIR1	$t_c(RX\_CLK)$	Cycle time, FSI_RXn_CLK	20		ns
FSIR2	$t_w(RX\_CLK)$	Pulse width, FSI_RXn_CLK low or FSI_RXn_CLK high	$0.5P - 1^{(1)}$	$0.5P + 1^{(1)}$	ns
FSIR3	$t_{su}(RX\_D-RX\_CLK)$	Setup time, FSI_RXn_D[1:0] valid before FSI_RXn_CLK	3		ns
FSIR4	$t_h(RX\_CLK-RX\_D)$	Hold time, FSI_RXn_D[1:0] valid after FSI_RXn_CLK	2.5		ns

(1) P = FSI\_RXn\_CLK period in ns.

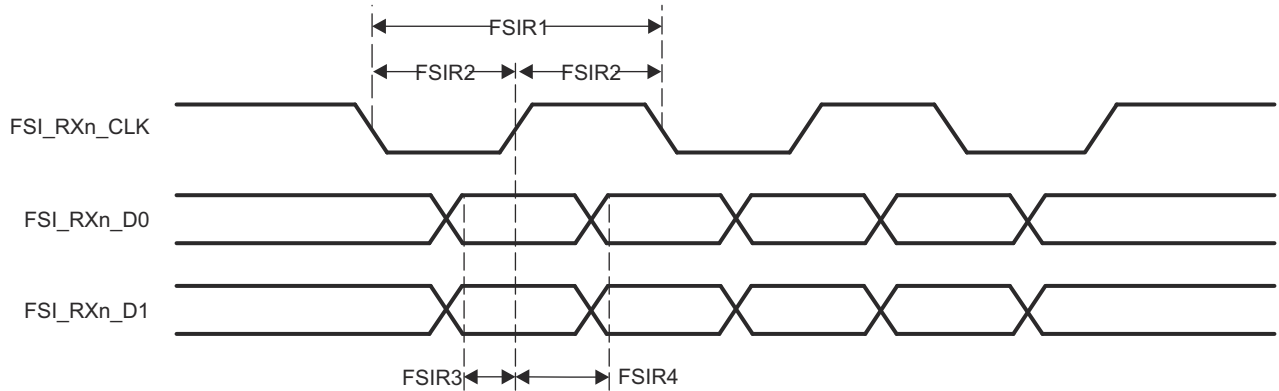


Figure 7-34. FSI Timing Requirements

Table 7-44. FSI Switching Characteristics - FSI Mode

see Figure 7-35

NO.	PARAMETER		MODE	MIN	MAX	UNIT
FSIT1	$t_{c(TX\_CLK)}$	Cycle time, FSI_TXn_CLK	FSI Mode	20		ns
FSIT2	$t_{w(TX\_CLK)}$	Pulse width, FSI_TXn_CLK low or FSI_TXn_CLK high	FSI Mode	$0.5P + 1^{(1)}$	$0.5P - 1^{(1)}$	ns
FSIT3	$t_{d(TX\_CLK-TX\_D)}$	Delay time, FSI_TXn_D[1:0] valid after FSI_TXn_CLK high or FSI_TXn_CLK low	FSI Mode	$0.25P - 2^{(1)}$	$0.25P + 2.5^{(1)}$	ns

(1) P = FSI\_TXn\_CLK period in ns.

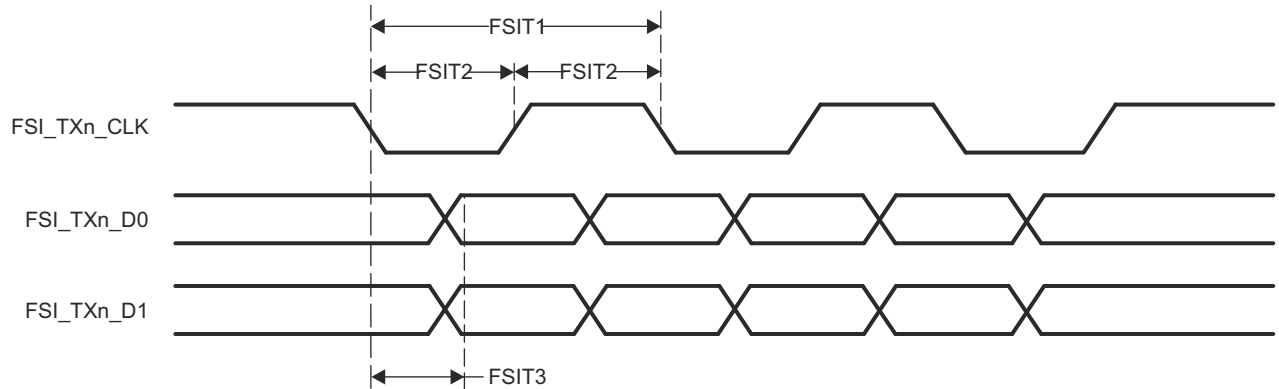


Figure 7-35. FSI Switching Characteristics - FSI Mode

Table 7-45. FSI Switching Characteristics - SPI Mode

see Figure 7-36

NO.	PARAMETER		MODE	MIN	MAX	UNIT
FSIT4	$t_{c(TX\_CLK)}$	Cycle time, FSI_TXn_CLK	SPI Mode	20		ns
FSIT5	$t_{w(TX\_CLK)}$	Pulse width, FSI_TXn_CLK low or FSI_TXn_CLK high	SPI Mode	$0.5P + 1^{(1)}$	$0.5P - 1^{(1)}$	ns
FSIT6	$t_{d(TX\_CLKH-TX\_D0)}$	Delay time, FSI_TXn_CLK high to FSI_TXn_D0 valid	SPI Mode		3	ns
FSIT7	$t_{d(TX\_D1-TX\_CLK)}$	Delay time, FSI_TXn_D1 low to FSI_TXn_CLK high	SPI Mode	$P - 3^{(1)}$		ns
FSIT8	$t_{d(TX\_CLK-TX\_D1)}$	Delay time, FSI_TXn_CLK low to FSI_TXn_D1 high	SPI Mode	$P - 2^{(1)}$		ns

(1) P = FSI\_TXn\_CLK period in ns.

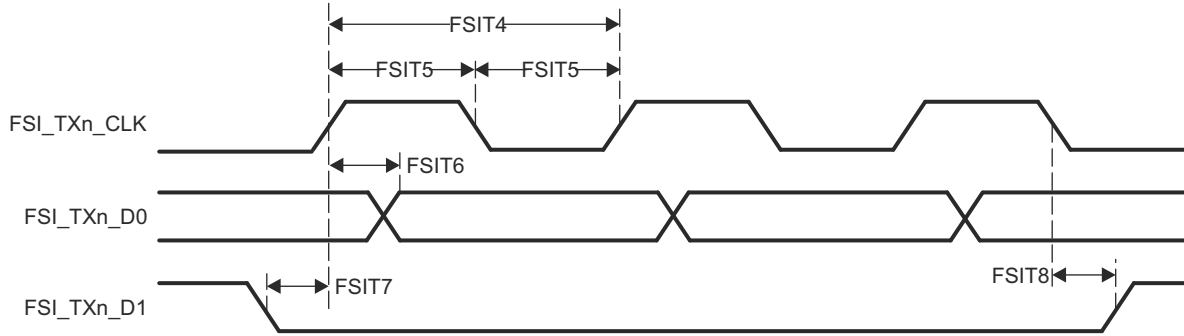


Figure 7-36. FSI Switching Characteristics - SPI Mode

For more information, see *Fast Serial Interface* section in *Peripherals* chapter in the device TRM.

### 7.10.5.7 GPIO

Table 7-46, Table 7-47, and Table 7-48 present timing conditions, requirements, and switching characteristics for GPIO.

For more details about features and additional description information on the device GPIO, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

#### Note

The device has multiple GPIO modules. GPIO<sub>n</sub>\_x is generic name used to describe a GPIO signal, where n represents the specific GPIO module and x represents one of the input/output signals associated with the module.

Table 7-46. GPIO Timing Conditions

PARAMETER		BUFFER TYPE	MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>					
SR <sub>i</sub>	Input slew rate	LVC MOS	0.75	6.6	V/ns
		I2C OD FS	TBD	TBD	V/ns
<b>OUTPUT CONDITIONS</b>					
C <sub>L</sub>	Output load capacitance	LVC MOS	3	10	pF
		I2C OD FS	3	100	pF

Table 7-47. GPIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
GPIO1	t <sub>w</sub> (GPIO_IN)	Pulse width, GPIO <sub>n</sub> _x	LVC MOS	2P + 2.6 <sup>(1)</sup>		ns
			I2C OD FS	2P + 2.6 <sup>(1)</sup>		ns

(1) P = functional clock period in ns.

Table 7-48. GPIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
GPIO2	t <sub>w</sub> (GPIO_OUT)	Pulse width, GPIO <sub>n</sub> _x	LVC MOS	-3.6 + 0.975P <sup>(1)</sup>		ns
			I2C OD FS	160		ns

(1) P = functional clock period in ns.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

### 7.10.5.8 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Table 7-49 presents timing conditions for GPMC.

**Table 7-49. GPMC Timing Conditions**

PARAMETER		MIN	MAX	UNIT	
<b>INPUT CONDITIONS</b>					
SR <sub>I</sub>	Input slew rate	1.65	4	V/ns	
<b>OUTPUT CONDITIONS</b>					
C <sub>L</sub>	Output load capacitance	5	20	pF	
<b>PCB CONNECTIVITY REQUIREMENTS</b>					
t <sub>d</sub> (Trace Delay)	Propagation delay of each trace	133 MHz Synchronous Mode	140	360	ps
		All other modes	140	720	ps
t <sub>d</sub> (Trace Mismatch Delay)	Propagation delay mismatch across all traces		200	ps	

For more information, see *General-Purpose Memory Controller (GPMC)* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.8.1 GPMC and NOR Flash — Synchronous Mode

Table 7-50 and Table 7-51 present timing requirements and switching characteristics for GPMC and NOR Flash - Synchronous Mode.

**Table 7-50. GPMC and NOR Flash Timing Requirements — Synchronous Mode**

see Figure 7-37, Figure 7-38, and Figure 7-41

NO.	PARAMETER	DESCRIPTION	MODE <sup>(4)</sup>	MIN	MAX	MIN	MAX	UNIT
				GPMC_FCLK = 100 MHz <sup>(1)</sup>		GPMC_FCLK = 133 MHz <sup>(1)</sup>		
F12	t <sub>su</sub> (dV-clkH)	Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.81		1.11		ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.06		3.50		ns
F13	t <sub>h</sub> (clkH-dV)	Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.28		2.28		ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.28		2.28		ns
F21	t <sub>su</sub> (waitV-clkH)	Setup time, input wait GPMC_WAIT[jj] <sup>(2) (3)</sup> valid before output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.81		1.11		ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	1.06		3.50		ns
F22	t <sub>h</sub> (clkH-waitV)	Hold time, input wait GPMC_WAIT[jj] <sup>(2) (3)</sup> valid after output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.28		2.28		ns
			not_div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	2.8		2.28		ns

(1) GPMC\_FCLK select



- gpmc\_fclk\_sel[1:0] = 2b01 to select the 100MHz GPMC\_FCLK
  - gpmc\_fclk\_sel[1:0] = 2b00 to select the 133MHz GPMC\_FCLK
- (2) In GPMC\_WAIT[j], j is equal to 0 or 1.
- (3) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see *General-Purpose Memory Controller (GPMC)* section in the device TRM.
- (4) For div\_by\_1\_mode:
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
    - GPMC\_CLK frequency = GPMC\_FCLK frequency

For not\_div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 1h to 3h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency / (2 to 4)

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 01 = PER1\_PLL\_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

**Table 7-51. GPMC and NOR Flash Switching Characteristics – Synchronous Mode**

see [Figure 7-37](#), [Figure 7-38](#), [Figure 7-39](#), [Figure 7-40](#), and [Figure 7-41](#)

NO. (2)	PARAMETER	DESCRIPTION	MODE <sup>(17)</sup>	MIN	MAX	MIN	MAX	UNIT
				100 MHz		133 MHz		
F0	1 / tc(clk)	Period, output clock GPMC_CLK <sup>(15)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	10.00		7.52		ns
F1	t <sub>w</sub> (clkH)	Typical pulse duration, output clock GPMC_CLK high	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475P - 0.3 <sup>(14)</sup>		0.475P - 0.3 <sup>(14)</sup>		ns
F1	t <sub>w</sub> (clkL)	Typical pulse duration, output clock GPMC_CLK low	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	0.475P - 0.3 <sup>(14)</sup>		0.475P - 0.3 <sup>(14)</sup>		ns
	t <sub>dc</sub> (clk)	Duty cycle error, output clock GPMC_CLK	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	-500.00	500.00	-500.00	500.00	ps
	t <sub>J</sub> (clk)	Jitter standard deviation, output clock GPMC_CLK <sup>(16)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		33.33		33.33	ps
	t <sub>R</sub> (clk)	Rise time, output clock GPMC_CLK	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.0		2.0	ns
	t <sub>F</sub> (clk)	Fall time, output clock GPMC_CLK	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.0		2.0	ns
	t <sub>R</sub> (do)	Rise time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.0		2.0	ns
	t <sub>F</sub> (do)	Fall time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.0		2.0	ns
F2	t <sub>d</sub> (clkH-csnV)	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CS <sub>n</sub> [j] transition <sup>(13)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	F - 2.2 <sup>(5)</sup>	F + 3.75	F - 2.2 <sup>(5)</sup>	F + 3.75	ns

**Table 7-51. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (continued)**

see Figure 7-37, Figure 7-38, Figure 7-39, Figure 7-40, and Figure 7-41

NO. (2)	PARAMETER	DESCRIPTION	MODE <sup>(17)</sup>	MIN	MAX	MIN	MAX	UNIT
				100 MHz		133 MHz		
F3	$t_{d(\text{clkH-CSn}[j]V)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CS <sub>n</sub> [j] invalid <sup>(13)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	E - 2.2 (4)	E + 1.31	E - 2.2 (4)	E + 4.5	ns
F4	$t_{d(aV\text{-clk})}$	Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2.3 (2)	B + 4.5	B - 2.3 (2)	B + 4.5	ns
F5	$t_{d(\text{clkH-aIV})}$	Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	-2.3	4.5	-2.3	4.5	ns
F6	$t_{d(\text{be}[x]nV\text{-clk})}$	Delay time, output lower byte enable and command latch enable GPMC_BE0 <sub>n</sub> _CLE, output upper byte enable GPMC_BE1 <sub>n</sub> valid to output clock GPMC_CLK first edge	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2.3 (2)	B + 1.9	B - 2.3 (2)	B + 1.9	ns
F7	$t_{d(\text{clkH-be}[x]nIV)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0 <sub>n</sub> _CLE, output upper byte enable GPMC_BE1 <sub>n</sub> invalid <sup>(10)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3 (3)	D + 1.9	D - 2.3 (3)	D + 1.9	ns
F7	$t_{d(\text{clkL-be}[x]nIV)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0 <sub>n</sub> _CLE, GPMC_BE1 <sub>n</sub> invalid <sup>(11)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3 (3)	D + 1.9	D - 2.3 (3)	D + 1.9	ns
F7	$t_{d(\text{clkL-be}[x]nIV)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0 <sub>n</sub> _CLE, GPMC_BE1 <sub>n</sub> invalid <sup>(12)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2.3 (3)	D + 1.9	D - 2.3 (3)	D + 1.9	ns
F8	$t_{d(\text{clkH-advn})}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADV <sub>n</sub> _ALE transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	G - 2.3 (6)	G + 4.5	G - 2.3 (6)	G + 4.5	ns
F9	$t_{d(\text{clkH-advnIV})}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADV <sub>n</sub> _ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	D - 2.3 (3)	D + 4.5	D - 2.3 (3)	D + 4.5	ns
F10	$t_{d(\text{clkH-oen})}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	-2.3H (7)	H + 3.5	H - 2.3 (7)	H + 3.5	ns
F11	$t_{d(\text{clkH-oenIV})}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	E - 2.3 (7)	E + 3.5	E - 2.3 (7)	E + 3.5	ns
F14	$t_{d(\text{clkH-wen})}$	Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1; no extra_delay	I - 2.3 (8)	I + 4.5	I - 2.3 (8)	I + 4.5	ns
F15	$t_{d(\text{clkH-do})}$	Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition <sup>(10)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9)	J + 2.7	J - 2.3 (9)	J + 2.7	ns
F15	$t_{d(\text{clkL-do})}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition <sup>(11)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9)	J + 2.7	J - 2.3 (9)	J + 2.7	ns
F15	$t_{d(\text{clkL-do})}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition <sup>(12)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9)	J + 2.7	J - 2.3 (9)	J + 2.7	ns

**Table 7-51. GPMC and NOR Flash Switching Characteristics – Synchronous Mode (continued)**

see [Figure 7-37](#), [Figure 7-38](#), [Figure 7-39](#), [Figure 7-40](#), and [Figure 7-41](#)

NO. (2)	PARAMETER	DESCRIPTION	MODE <sup>(17)</sup>	MIN	MAX	MIN	MAX	UNIT
				100 MHz		133 MHz		
F17	$t_{d(\text{clkH-be}[x]n)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition <sup>(10)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9)	J + 1.9	J - 2.3 (9)	J + 1.9	ns
F17	$t_{d(\text{clkL-be}[x]n)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(11)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9)	J + 1.9	J - 2.3 (9)	J + 1.9	ns
F17	$t_{d(\text{clkL-be}[x]n)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(12)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.3 (9)	J + 1.9	J - 2.3 (9)	J + 1.9	ns
F18	$t_{w(\text{csnV})}$	Pulse duration, output chip select GPMC_CS[n][i] <sup>(13)</sup> low	Read	A		A		ns
			Write	A		A		ns
F19	$t_{w(\text{be}[x]nV)}$	Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low	Read	C		C		ns
			Write	C		C		ns
F20	$t_{w(\text{advnV})}$	Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low	Read	K		K		ns
			Write	K		K		ns

- (1) For single read:  $A = (\text{CSRDoffTime} - \text{CSOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
 For burst read:  $A = (\text{CSRDoffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
 For burst write:  $A = (\text{CSWrOffTime} - \text{CSOnTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
 With n being the page burst access number.
- (2)  $B = \text{ClkActivationTime} \times \text{GPMC\_FCLK}^{(14)}$
- (3) For single read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
 For burst read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
 For burst write:  $D = (\text{WrCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$
- (4) For single read:  $E = (\text{CSRDoffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
 For burst read:  $E = (\text{CSRDoffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
 For burst write:  $E = (\text{CSWrOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$
- (5) For csn falling edge (CS activated):
- Case GPMCFCLKDIVIDER = 0:
    - $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$
  - Case GPMCFCLKDIVIDER = 1:
    - $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
    - $F = (1 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  otherwise
  - Case GPMCFCLKDIVIDER = 2:
    - $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if ((CSOnTime - ClkActivationTime) is a multiple of 3)
    - $F = (1 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
    - $F = (2 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)
- (6) For ADV falling edge (ADV activated):
- Case GPMCFCLKDIVIDER = 0:
    - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$
  - Case GPMCFCLKDIVIDER = 1:
    - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
    - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  otherwise
  - Case GPMCFCLKDIVIDER = 2:
    - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
    - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
    - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

- Case GPMCFCLKDIVIDER = 0:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$
- Case GPMCFCLKDIVIDER = 1:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GPMCFCLKDIVIDER = 0:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$
- Case GPMCFCLKDIVIDER = 1:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(7) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GPMCFCLKDIVIDER = 0:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$
- Case GPMCFCLKDIVIDER = 1:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $H = (2 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$
- Case GPMCFCLKDIVIDER = 1:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $H = (2 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For WE falling edge (WE activated):

- Case GPMCFCLKDIVIDER = 0:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$
- Case GPMCFCLKDIVIDER = 1:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if ((WEOnTime - ClkActivationTime) is a multiple of 3)

- $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if  $((\text{WEOnTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)
- $I = (2 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if  $((\text{WEOnTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

For WE rising edge (WE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$
- Case GPMCFCLKDIVIDER = 1:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if  $(\text{ClkActivationTime}$  and  $\text{WEOffTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{WEOffTime}$  are even)
  - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(14)}$  if  $((\text{WEOffTime} - \text{ClkActivationTime})$  is a multiple of 3)
  - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if  $((\text{WEOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)
  - $I = (2 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(14)}$  if  $((\text{WEOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

(9)  $J = \text{GPMC\_FCLK}^{(14)}$

(10) First transfer only for CLK DIV 1 mode.

(11) Half cycle; for all data after initial transfer for CLK DIV 1 mode.

(12) Half cycle of GPMC\_CLKOUT; for all data for modes other than CLK DIV 1 mode. GPMC\_CLKOUT divide down from GPMC\_FCLK.

(13) In GPMC\_CS*n*[*j*], *i* is equal to 0, 1, 2 or 3. In GPMC\_WAIT[*j*], *j* is equal to 0 or 1.

(14)  $P = \text{GPMC\_CLK}$  period in ns

(15) Related to the GPMC\_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC\_CONFIG1\_*i* configuration register bit field GPMCFCLKDIVIDER.

(16) The jitter probability density can be approximated by a Gaussian function.

(17) For `div_by_1_mode`:

- GPMC\_CONFIG1\_*i* register: GPMCFCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

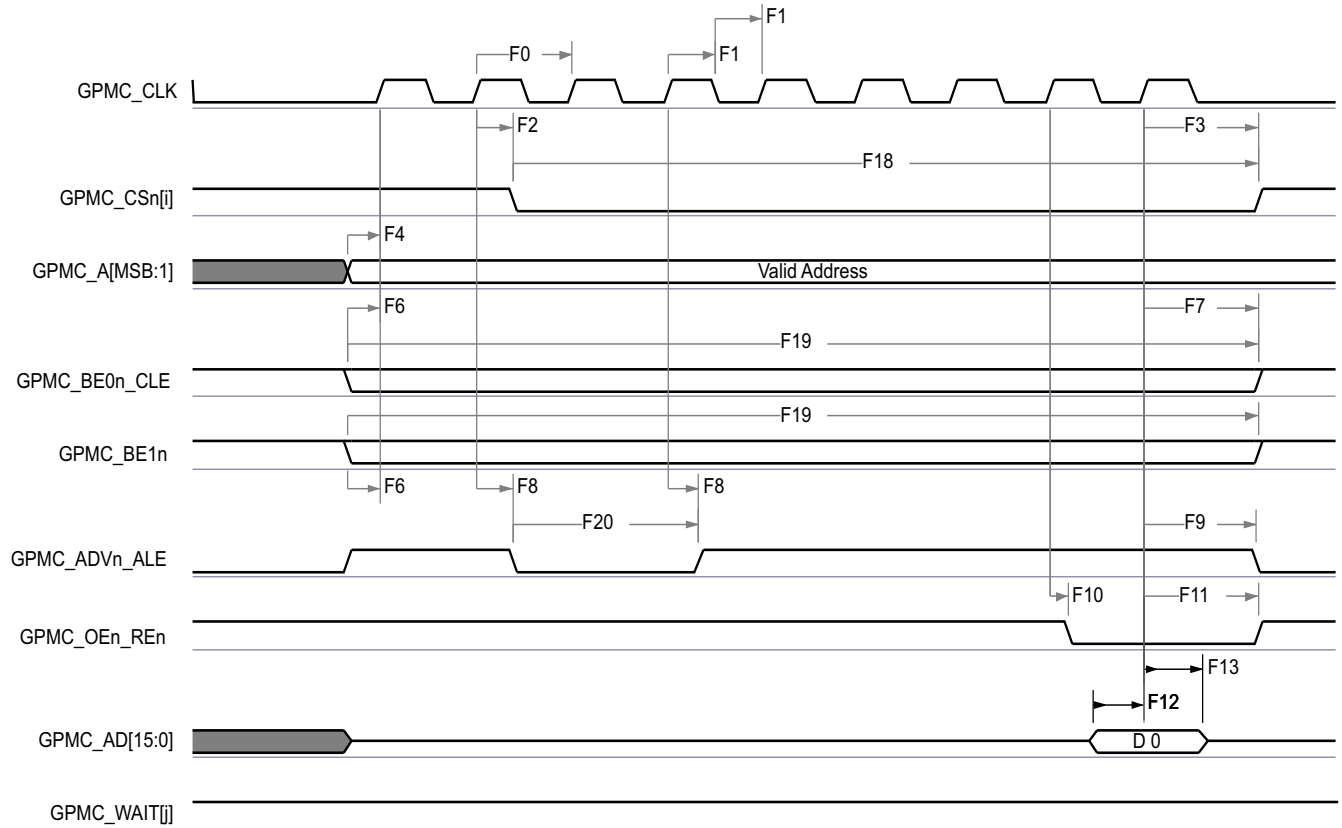
- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 01 = PER1\_PLL\_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_*i* Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

For no extra\_delay:

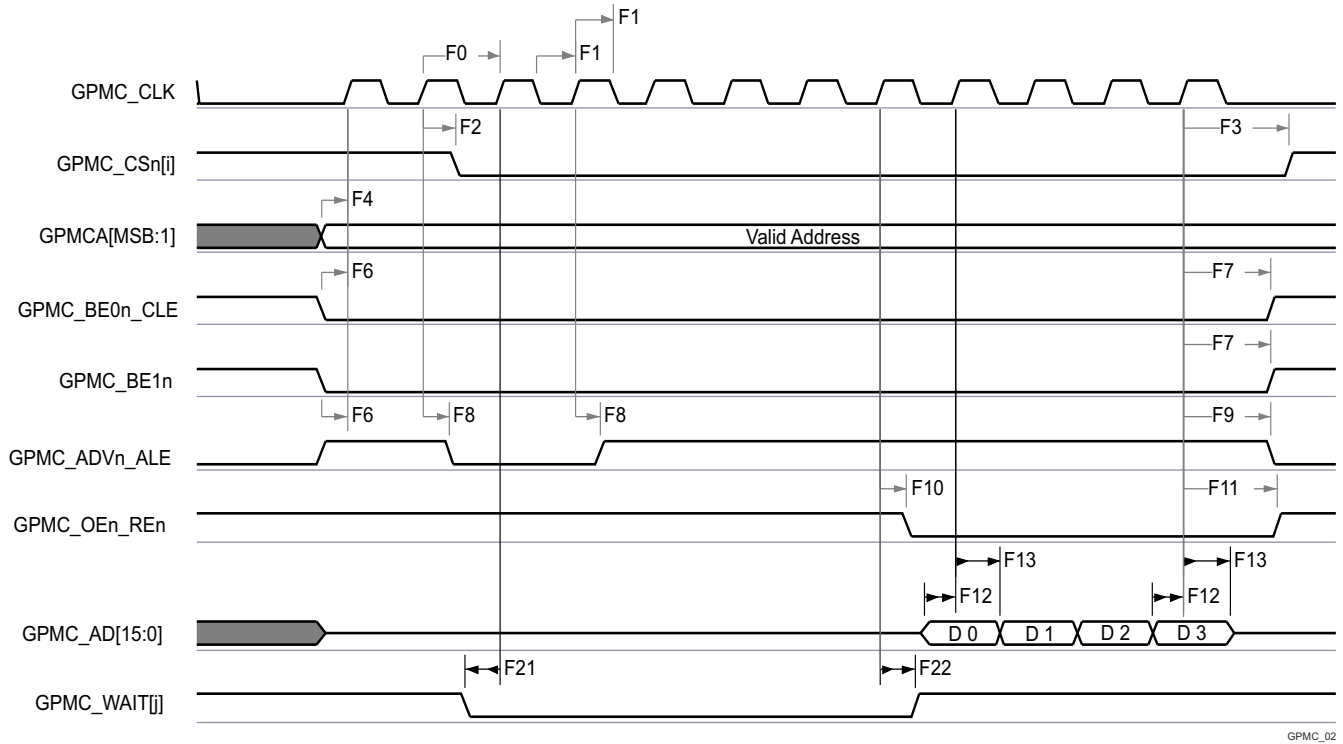
- GPMC\_CONFIG2\_*i* Register: CSEXTRADELAY = 0h = CS*n* Timing control signal is not delayed
- GPMC\_CONFIG4\_*i* Register: WEEXTRADELAY = 0h = nWE timing control signal is not delayed
- GPMC\_CONFIG4\_*i* Register: OEEXTRADELAY = 0h = nOE timing control signal is not delayed
- GPMC\_CONFIG3\_*i* Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed



GPMC\_01

- A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.
- B. In GPMC\_WAIT[j], j is equal to 0 or 1.

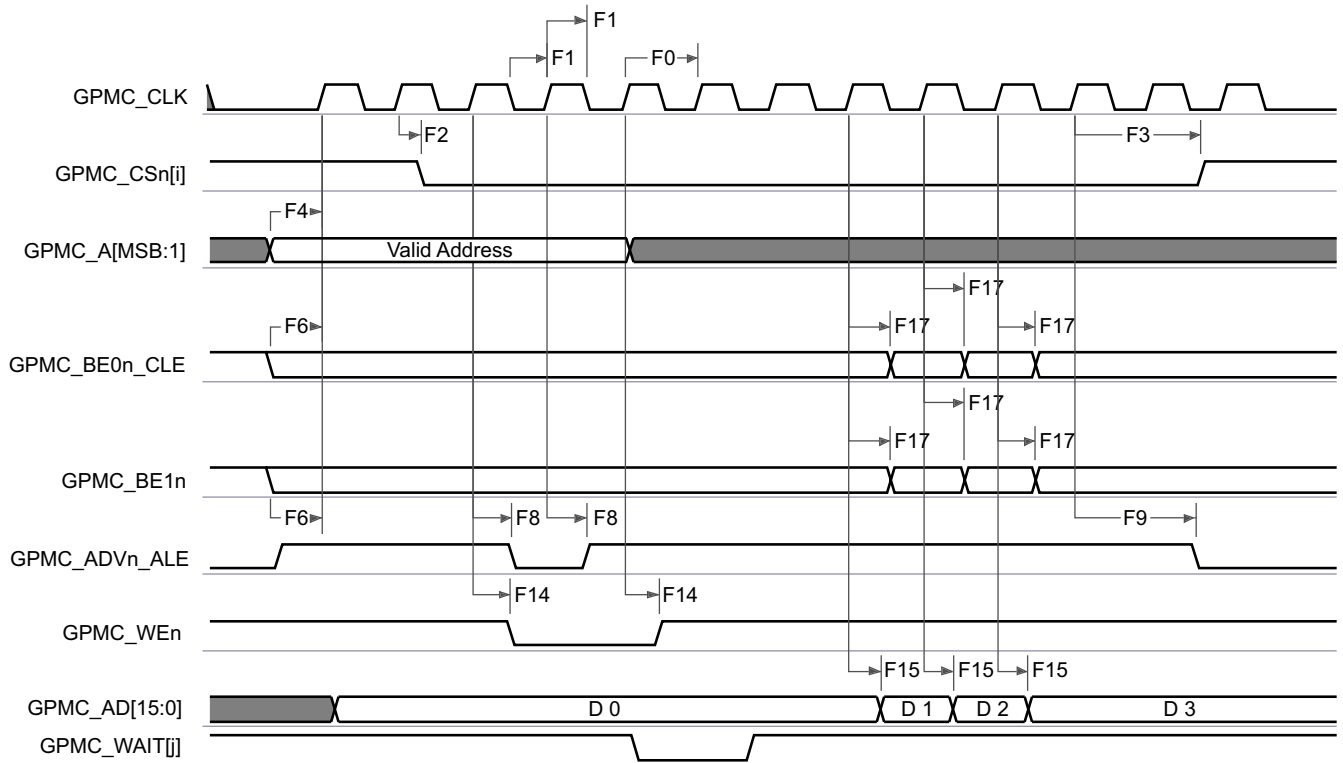
**Figure 7-37. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)**



GPMC\_02

- A. In GPMC\_CS*n*[i], i is equal to 0, 1, 2 or 3.
- B. In GPMC\_WAIT[i], j is equal to 0 or 1.

**Figure 7-38. GPMC and NOR Flash — Synchronous Burst Read — 4x16-bit (GPMCFCLKDIVIDER = 0)**

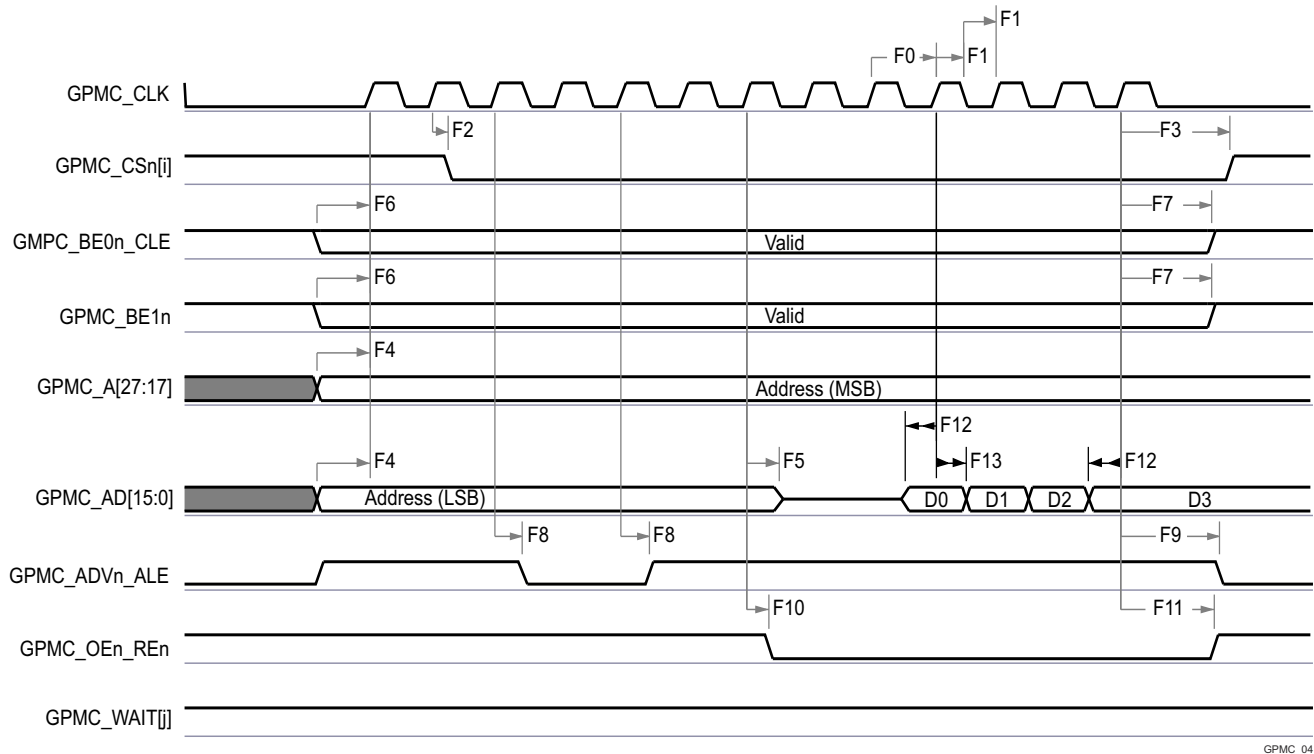


GPMC\_03

- A. In GPMC\_CS*n*[i], i is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 7-39. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)**



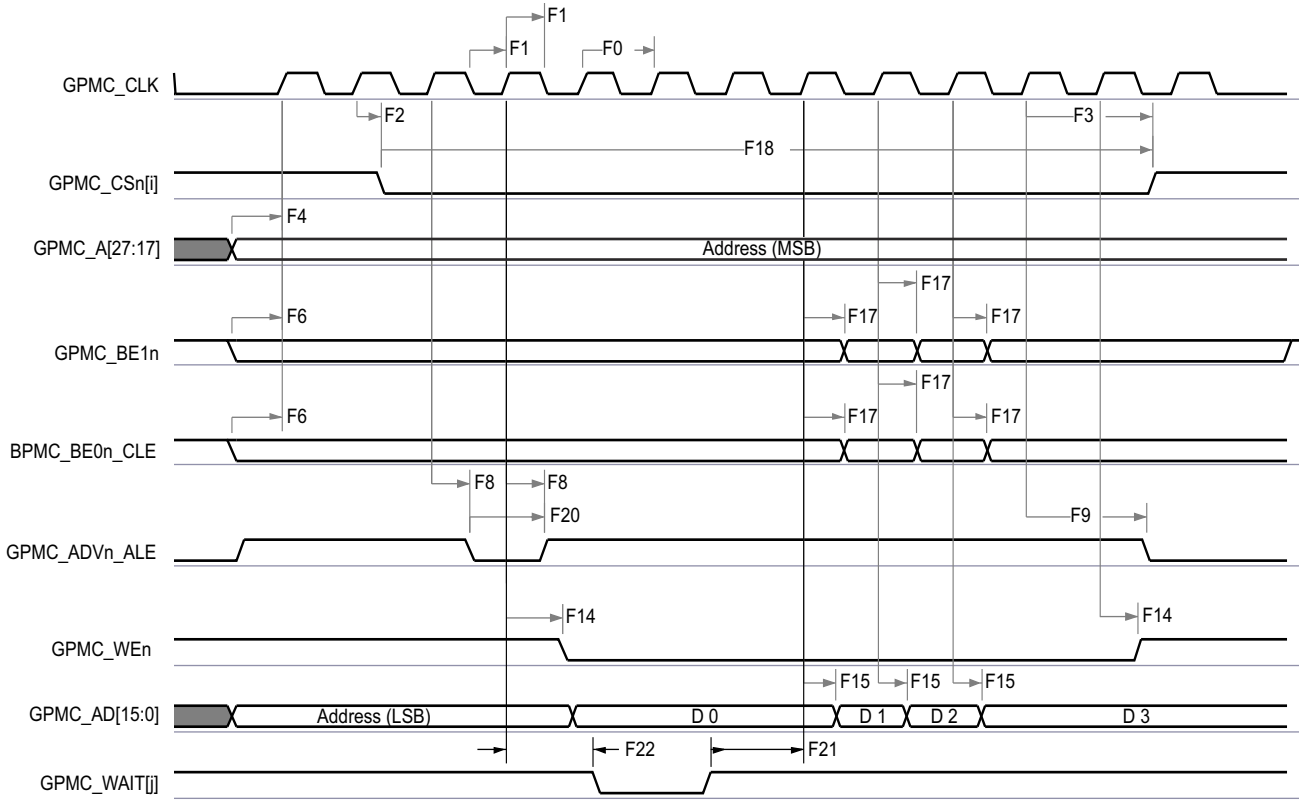
GPMC\_04

- A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.
- B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 7-40. GPMC and Multiplexed NOR Flash — Synchronous Burst Read**

ADVANCE INFORMATION





GPMC\_05

- A. In GPMC\_CS[n][i], i is equal to 0, 1, 2 or 3.
- B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 7-41. GPMC and Multiplexed NOR Flash — Synchronous Burst Write**

**7.10.5.8.2 GPMC and NOR Flash — Asynchronous Mode**

Table 7-52 and Table 7-53 present timing requirements and switching characteristics for GPMC and NOR Flash — Asynchronous Mode.

**Table 7-52. GPMC and NOR Flash Timing Requirements – Asynchronous Mode**

see Figure 7-42, Figure 7-43, Figure 7-44, and Figure 7-46

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
FA5 <sup>(1)</sup>	t <sub>acc(d)</sub>	Data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H <sup>(4)</sup>	ns
FA2 <sub>0</sub> <sup>(2)</sup>	t <sub>acc1-pgmode(d)</sub>	Page mode successive data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		P <sup>(3)</sup>	ns
FA2 <sub>1</sub> <sup>(1)</sup>	t <sub>acc2-pgmode(d)</sub>	Page mode first data access time	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H <sup>(4)</sup>	ns

- (1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
- (2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
- (3) P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC\_FCLK<sup>(5)</sup>
- (4) H = AccessTime × (TimeParaGranularity + 1) × GPMC\_FCLK<sup>(5)</sup>
- (5) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

**Table 7-53. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode**

see Figure 7-42, Figure 7-43, Figure 7-44, Figure 7-45, Figure 7-46, and Figure 7-47

NO.	PARAMETER	DESCRIPTION	MODE <sup>(15)</sup>	MIN	MAX	UNIT
				133 MHz		
	$t_{R(d)}$	Rise time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.0	ns
	$t_{F(d)}$	Fall time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.0	ns
FA0	$t_{w(be x)nV}$	Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time	Read Write	N <sup>(12)</sup> N <sup>(12)</sup>		ns
FA1	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CS[n] <sup>(13)</sup> low	Read Write	A <sup>(1)</sup> A <sup>(1)</sup>		ns
FA3	$t_{d(csnV-advnV)}$	Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADVn_ALE invalid	Read Write	B - 2.1 <sup>(2)</sup> B + 2.1 <sup>(2)</sup>		ns
FA4	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output enable GPMC_OEn_REn invalid (Single read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2.1 <sup>(3)</sup> C + 2.1 <sup>(3)</sup>		ns
FA9	$t_{d(aV-csnV)}$	Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CS[n] <sup>(13)</sup> valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.1 <sup>(9)</sup> J + 2.1 <sup>(9)</sup>		ns
FA10	$t_{d(be x)nV-csnV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CS[n] <sup>(13)</sup> valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.1 <sup>(9)</sup> J + 2.1 <sup>(9)</sup>		ns
FA12	$t_{d(csnV-advnV)}$	Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADVn_ALE valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	K - 2.1 <sup>(10)</sup> K + 2.1 <sup>(10)</sup>		ns
FA13	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L - 2.1 <sup>(11)</sup> L + 2.1 <sup>(11)</sup>		ns
FA16	$t_{w(aV)}$	Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G <sup>(7)</sup>		ns
FA18	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output enable GPMC_OEn_REn invalid (Burst read)	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I - 2.1 <sup>(8)</sup> I + 2.1 <sup>(8)</sup>		ns
FA20	$t_{w(aV)}$	Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D <sup>(4)</sup>		ns
FA25	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E - 2.1 <sup>(5)</sup> E + 2.1 <sup>(5)</sup>		ns
FA27	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CS[n] <sup>(13)</sup> valid to output write enable GPMC_WEn invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2.1 <sup>(6)</sup> F + 2.1 <sup>(6)</sup>		ns
FA28	$t_{d(wenV-dV)}$	Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.1	ns
FA29	$t_{d(dV-csnV)}$	Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CS[n] <sup>(13)</sup> valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	J - 2.1 <sup>(9)</sup> J + 2.1 <sup>(9)</sup>		ns

**Table 7-53. GPMC and NOR Flash Switching Characteristics – Asynchronous Mode (continued)**

see [Figure 7-42](#), [Figure 7-43](#), [Figure 7-44](#), [Figure 7-45](#), [Figure 7-46](#), and [Figure 7-47](#)

NO.	PARAMETER	DESCRIPTION	MODE <sup>(15)</sup>	MIN	MAX	UNIT
				133 MHz		
FA37	t <sub>d(oenV-alV)</sub>	Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.1	ns

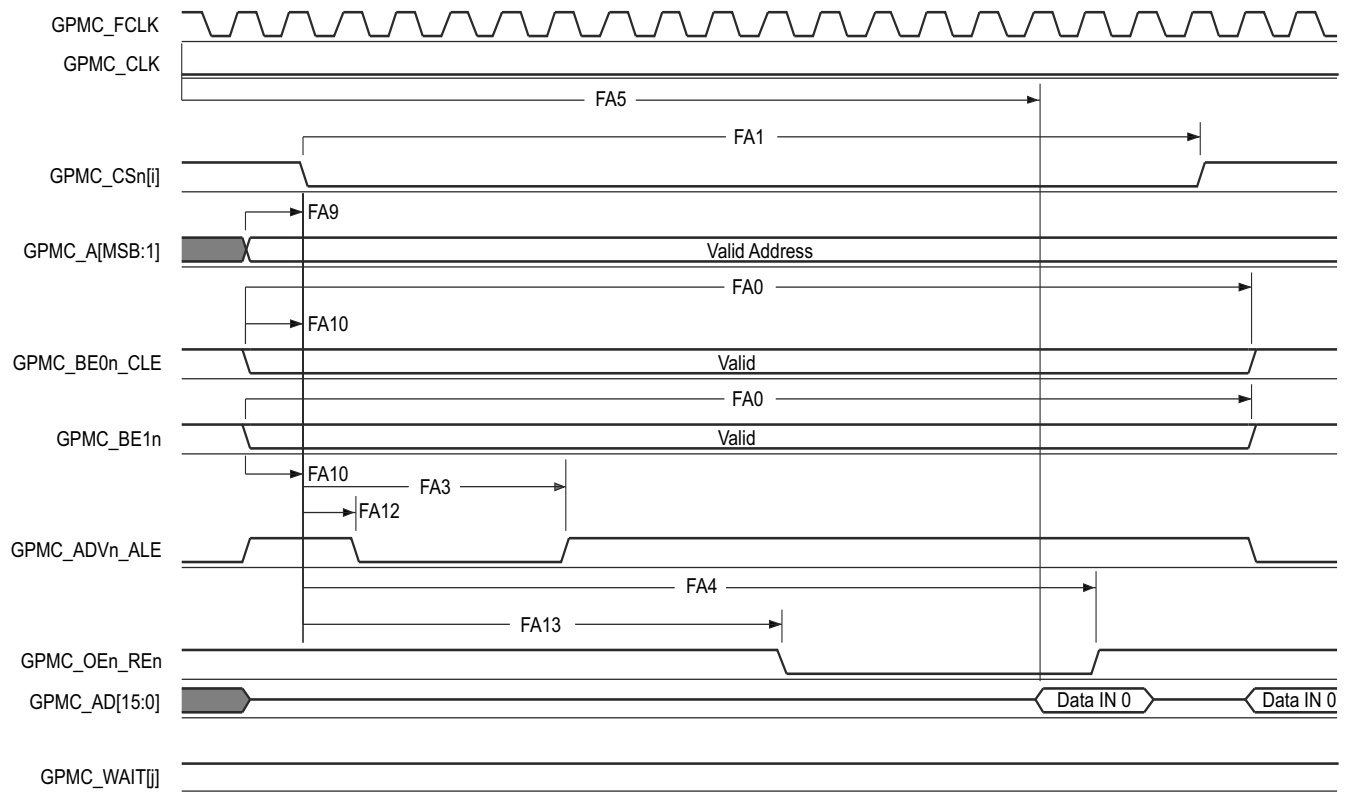
- (1) For single read:  $A = (CSRdOffTime - CSONTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For single write:  $A = (CSWrOffTime - CSONTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst read:  $A = (CSRdOffTime - CSONTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst write:  $A = (CSWrOffTime - CSONTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
with n being the page burst access number
- (2) For reading:  $B = ((ADVrdOffTime - CSONTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
For writing:  $B = ((ADVwrOffTime - CSONTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (3)  $C = ((OEOffTime - CSONTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (4)  $D = PageBurstAccessTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$
- (5)  $E = ((WEOnTime - CSONTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (6)  $F = ((WEOffTime - CSONTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (7)  $G = Cycle2CycleDelay \times GPMC\_FCLK^{(14)}$
- (8)  $I = ((OEOffTime + (n - 1) \times PageBurstAccessTime - CSONTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (9)  $J = (CSONTime \times (TimeParaGranularity + 1) + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK^{(14)}$
- (10)  $K = ((ADVOnTime - CSONTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (11)  $L = ((OEOnTime - CSONTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (12) For single read:  $N = RdCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For single write:  $N = WrCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst read:  $N = (RdCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst write:  $N = (WrCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$
- (13) In GPMC\_CS*n*[i], i is equal to 0, 1, 2 or 3.
- (14) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (15) For div\_by\_1\_mode:
  - GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
    - GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHS DIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

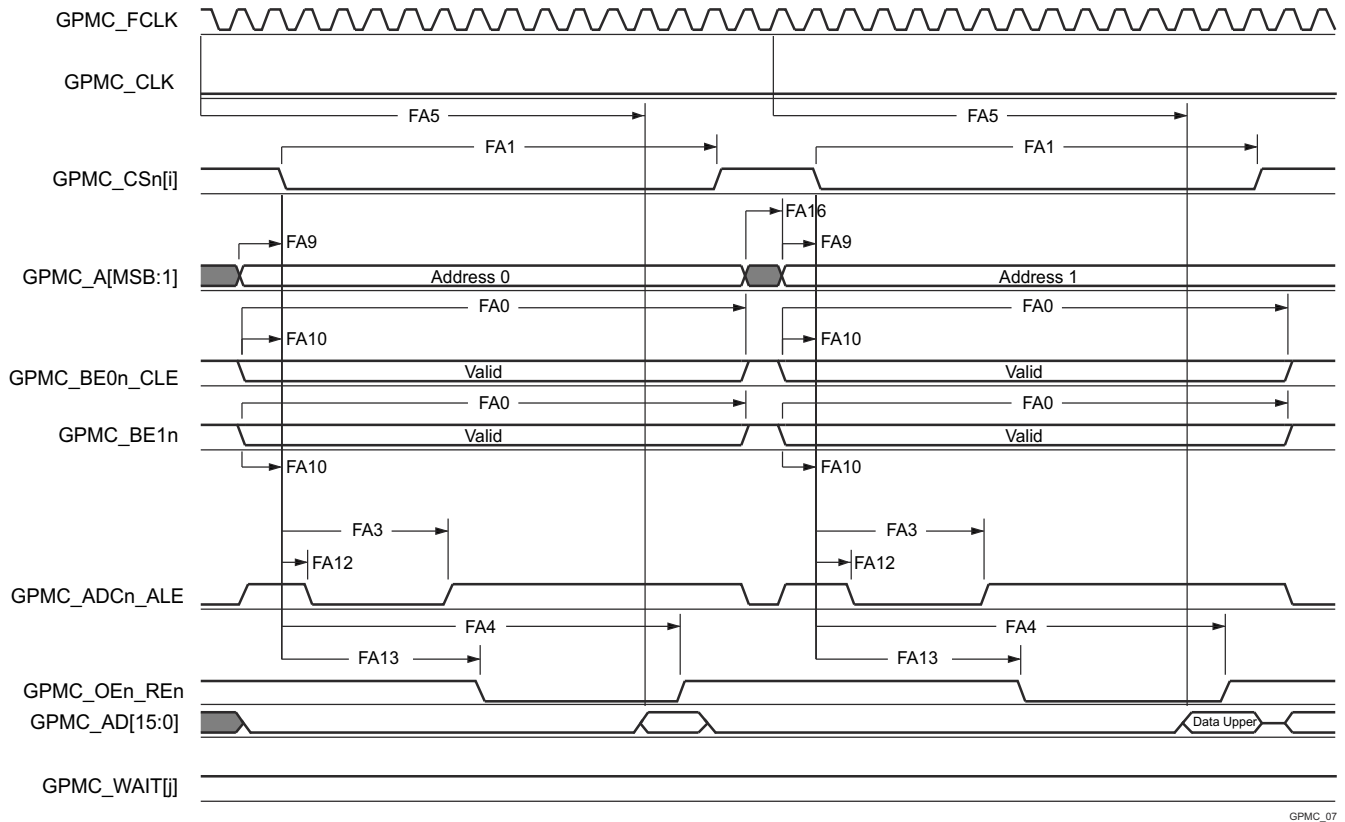
- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRd/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



GPMC\_06

- A. In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], *j* is equal to 0 or 1.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

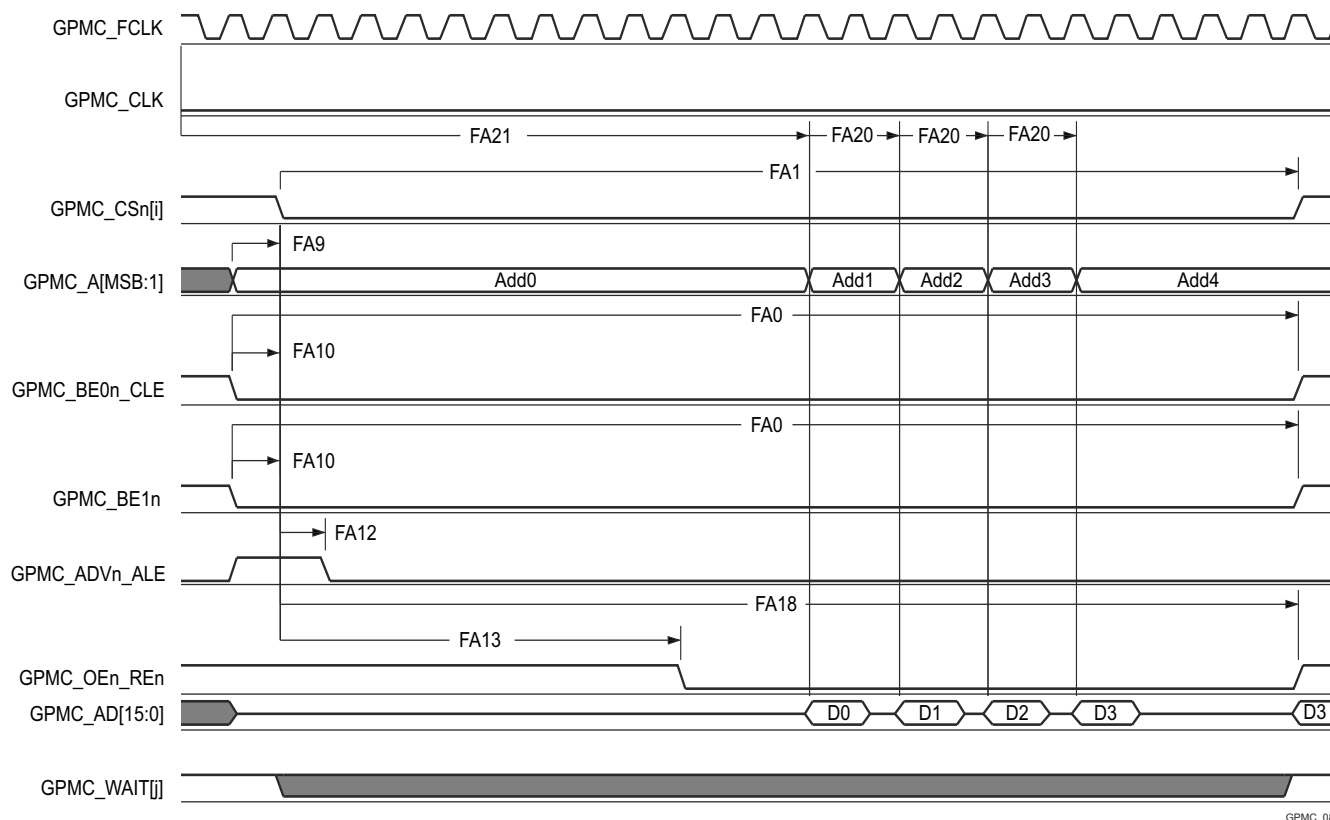
**Figure 7-42. GPMC and NOR Flash — Asynchronous Read — Single Word**



GPMC\_07

- A. In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], *j* is equal to 0 or 1.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

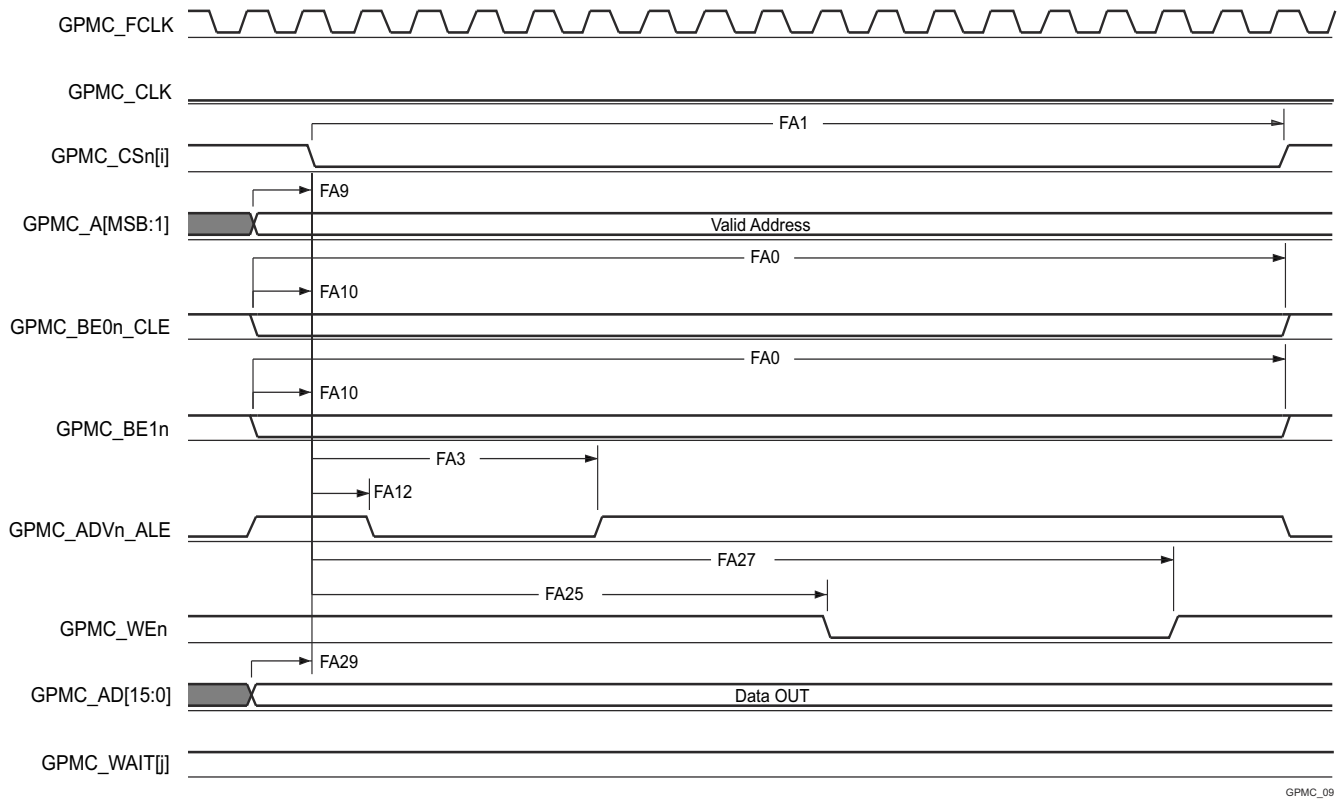
**Figure 7-43. GPMC and NOR Flash — Asynchronous Read — 32-Bit**



GPMC\_08

- A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
- C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
- D. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

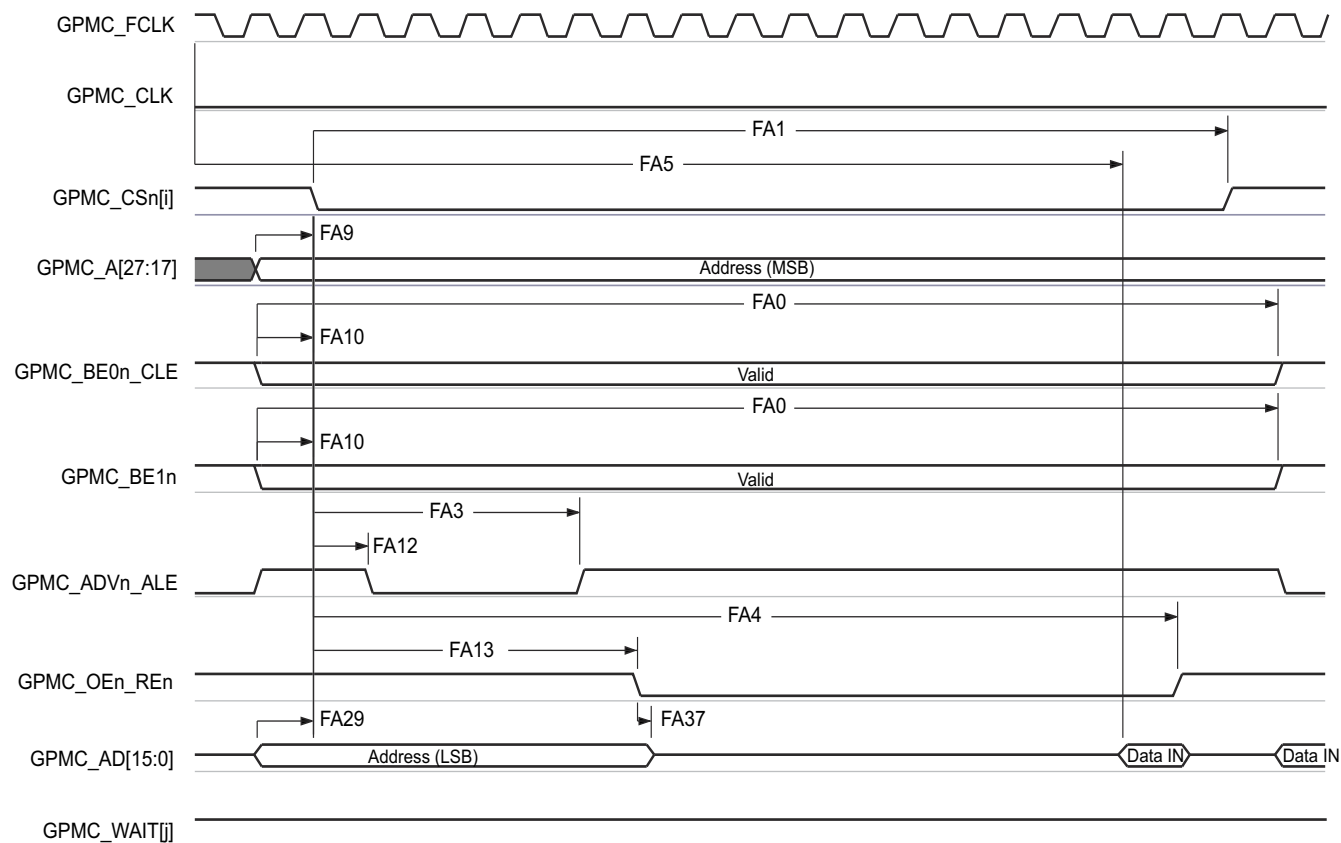
**Figure 7-44. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16–Bit**



GPMC\_09

A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 7-45. GPMC and NOR Flash — Asynchronous Write — Single Word**

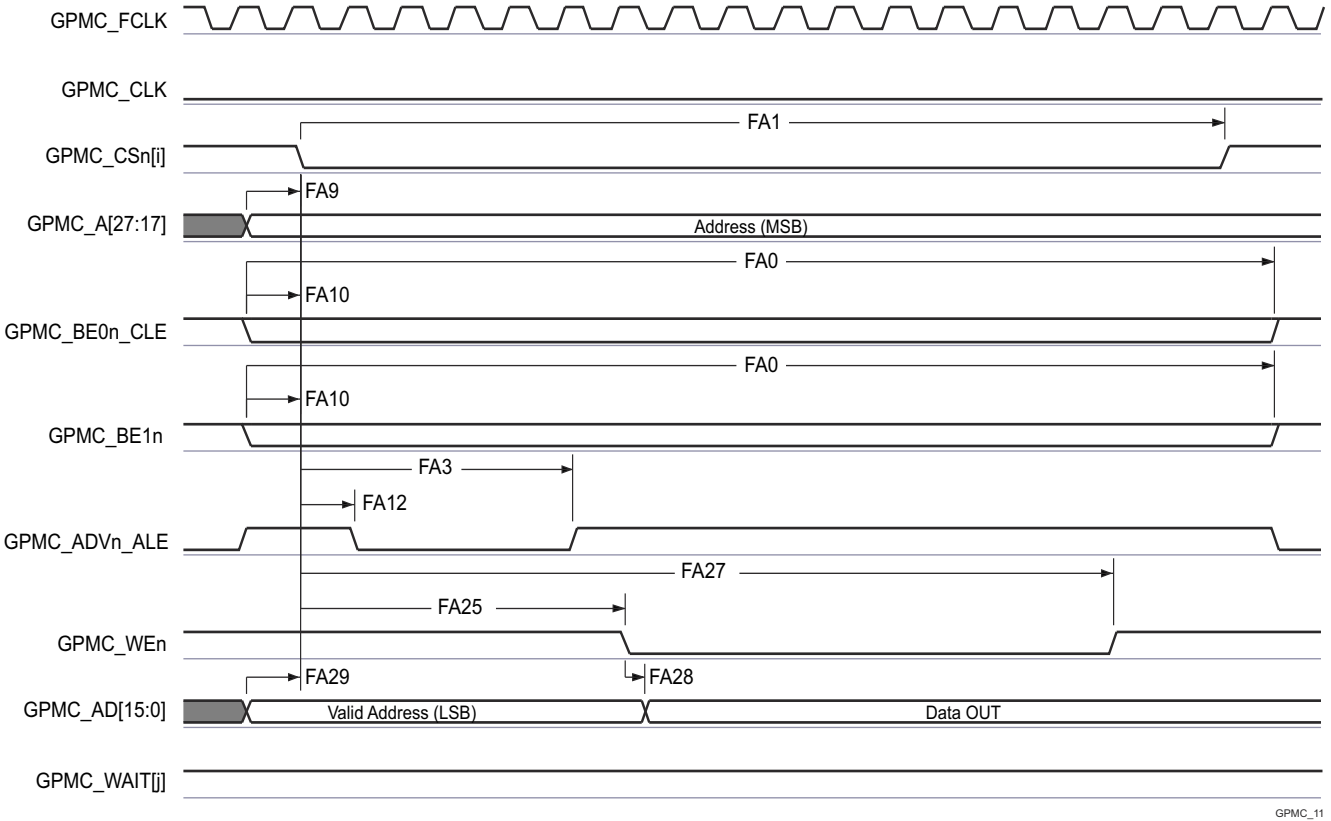


GPMC\_10

- A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

**Figure 7-46. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word**





GPMC\_11

A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 7-47. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word**

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**7.10.5.8.3 GPMC and NAND Flash — Asynchronous Mode**

Table 7-54 and Table 7-55 present timing requirements and switching characteristics for GPMC and NAND Flash — Asynchronous Mode.

**Table 7-54. GPMC and NAND Flash Timing Requirements – Asynchronous Mode**

see Figure 7-50

NO.	PARAMETER	DESCRIPTION	MODE <sup>(4)</sup>	MIN	MAX	UNIT
				133 MHz		
GNF12 <sup>(1)</sup>	$t_{acc(d)}$	Access time, input data GPMC_AD[15:0] <sup>(3)</sup>	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		J <sup>(2)</sup>	ns

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2)  $J = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(3)}$

(3) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

(4) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHS DIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

**Table 7-55. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode**

see Figure 7-48, Figure 7-49, Figure 7-50 and Figure 7-51

NO.	PARAMETER	DESCRIPTION	MODE <sup>(4)</sup>	MIN	MAX	UNIT
	$t_{R(d)}$	Rise time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.0	ns
	$t_{F(d)}$	Fall time, output data GPMC_AD[15:0]	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		2.0	ns
GNF0	$t_{w(wenV)}$	Pulse duration, output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	A	TBD	ns
GNF1	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CS <i>n</i> [ <i>j</i> ] <sup>(2)</sup> valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	B - 2	B + 2	ns
GNF2	$t_{w(cleH-wenV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2	C + 2	ns
GNF3	$t_{w(wenV-dV)}$	Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	D - 2	D + 2	ns
GNF4	$t_{w(wenIV-dIV)}$	Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	E - 2	E + 2	ns
GNF5	$t_{w(wenIV-cleIV)}$	Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2	F + 2	ns

**Table 7-55. GPMC and NAND Flash Switching Characteristics – Asynchronous Mode (continued)**

see [Figure 7-48](#), [Figure 7-49](#), [Figure 7-50](#) and [Figure 7-51](#)

NO.	PARAMETER		MODE <sup>(4)</sup>	MIN	MAX	UNIT
GNF6	$t_{w(wenIV-CSn[i]V)}$	Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CS <i>n</i> [ <i>i</i> ] <sup>(2)</sup> invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	G - 2	G + 2	ns
GNF7	$t_{w(aleH-wenV)}$	Delay time, output address valid and address latch enable GPMC_ADV <i>n</i> _ALE high to output write enable GPMC_WEn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	C - 2	C + 2	ns
GNF8	$t_{w(wenIV-aleIV)}$	Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADV <i>n</i> _ALE invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	F - 2	F + 2	ns
GNF9	$t_{c(wen)}$	Cycle time, write	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		H	ns
GNF10	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CS <i>n</i> [ <i>i</i> ] <sup>(2)</sup> valid to output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	I - 2	I + 2	ns
GNF13	$t_{w(oenV)}$	Pulse duration, output enable GPMC_OEn_REn valid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1		K	ns
GNF14	$t_{c(oen)}$	Cycle time, read	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	L		ns
GNF15	$t_{w(oenIV-CSn[i]V)}$	Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CS <i>n</i> [ <i>i</i> ] <sup>(2)</sup> invalid	div_by_1_mode; GPMC_FCLK_MUX; TIMEPARAGRANULARITY_X1	M - 2	M + 2	ns

(1)  $A = (WEOffTime - WEOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(3)}$

(2) In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3.

(3) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

(4) For div\_by\_1\_mode:

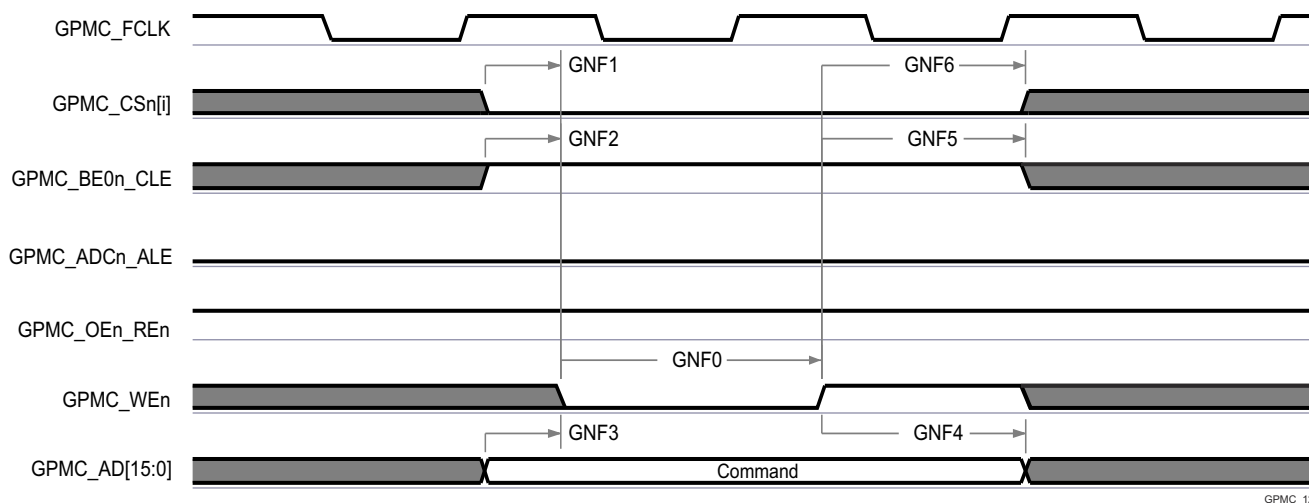
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHSIDIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

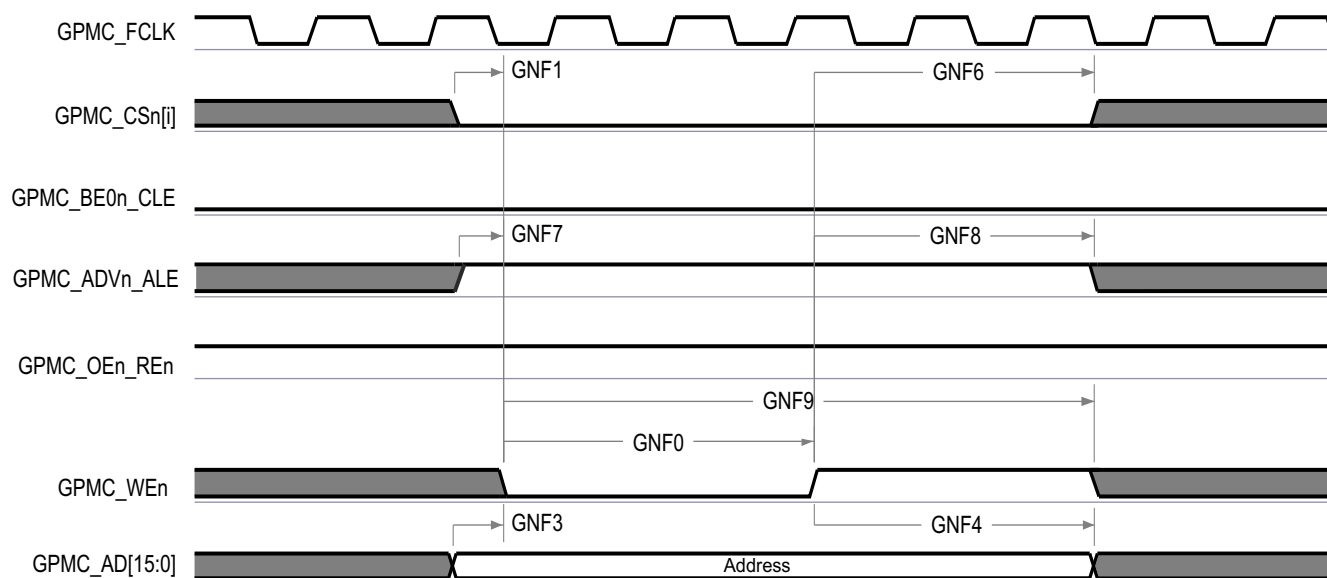
- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



GPMC\_12

A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.

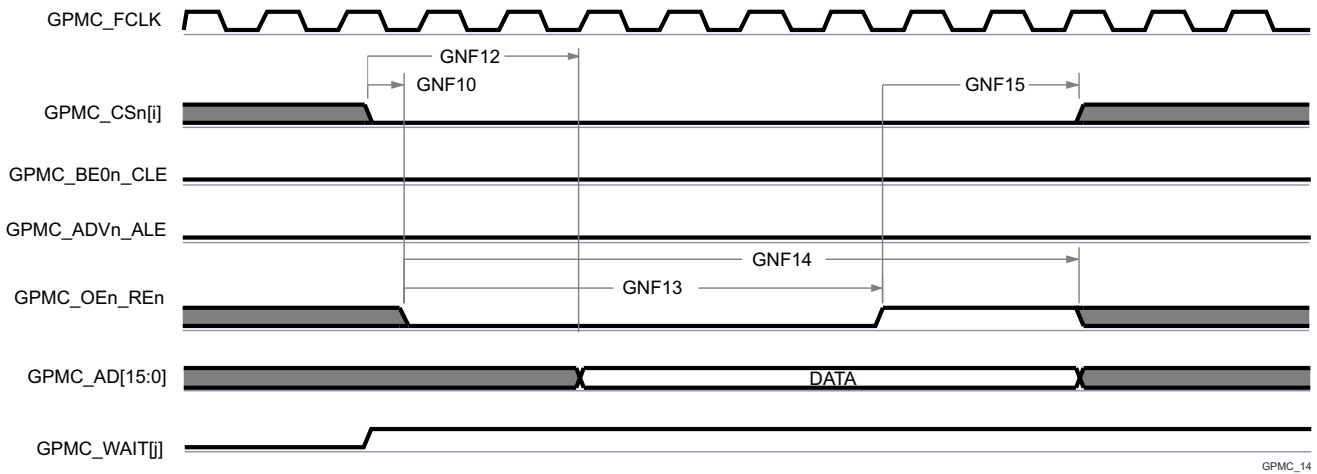
Figure 7-48. GPMC and NAND Flash — Command Latch Cycle



GPMC\_13

A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.

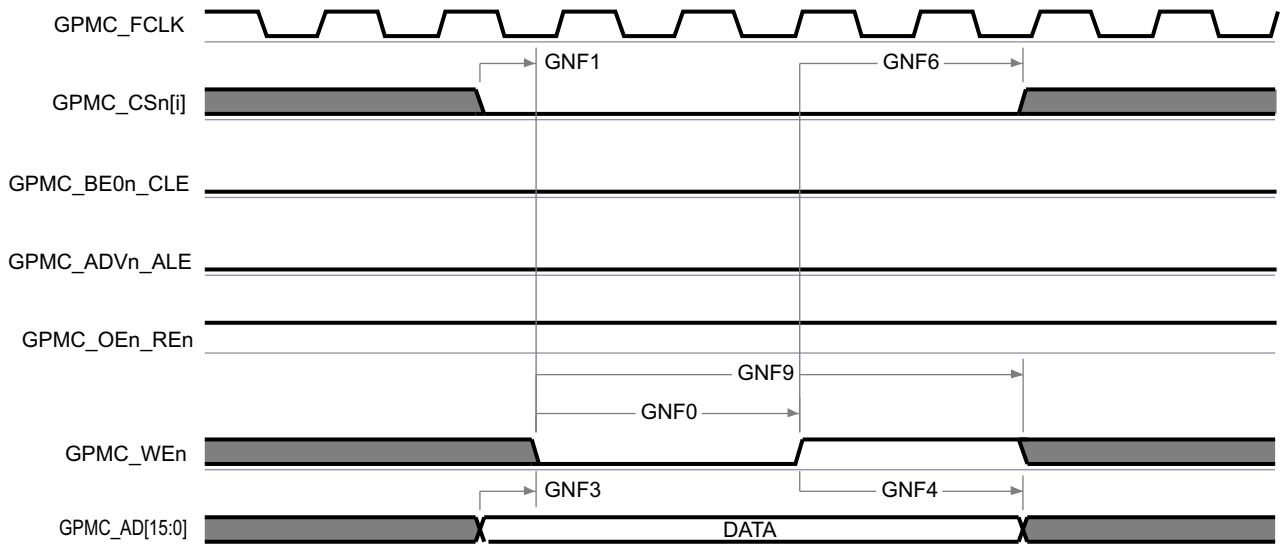
Figure 7-49. GPMC and NAND Flash — Address Latch Cycle



GPMC\_14

- A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
- B. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.
- C. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.

Figure 7-50. GPMC and NAND Flash — Data Read Cycle



GPMC\_15

- A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 7-51. GPMC and NAND Flash — Data Write Cycle

### 7.10.5.9 I2C

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Section 7.10.5.9.1, Table 7-56 and Figure 7-52 assume testing over the recommended operating conditions and electrical characteristic conditions.

#### 7.10.5.9.1 Timing Requirements for I2C Input Timings

NO. (1) (6)	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
I1	$t_{c(SCL)}$	Cycle time, SCL	Standard	10000		ns
			Fast	2500		ns

NO. (1) (6)	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
12	$t_{su}(SCLH-SDAL)$	Setup time, SCL high before SDA low (for a repeated START condition)	Standard	4700		ns
			Fast	600		ns
13	$t_h(SDAL-SCLL)$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	Standard	4000		ns
			Fast	900		ns
14	$t_w(SCLL)$	Pulse duration, SCL low	Standard	4700		ns
			Fast	1300		ns
15	$t_w(SCLH)$	Pulse duration, SCL high	Standard	4000		ns
			Fast	600		ns
16	$t_{su}(SDAV-SCLH)$	Setup time, SDA valid before SCL high	Standard	250		ns
			Fast	100 <sup>(2)</sup>		ns
17	$t_h(SCLL-SDAV)$	Hold time, SDA valid after SCL low	Standard	0 <sup>(3)</sup>	3450 <sup>(4)</sup>	ns
			Fast	0 <sup>(3)</sup>	900 <sup>(4)</sup>	ns
18	$t_w(SDAH)$	Pulse duration, SDA high between STOP and START conditions	Standard	4700		ns
			Fast	1300		ns
19	$t_r(SDA)$	Rise time, SDA	Standard		1000	ns
			Fast	$20^*(V_{dd}/5.5V)^{(5)(7)}$	300 <sup>(3)(7)</sup>	ns
110	$t_r(SCL)$	Rise time, SCL	Standard		1000	ns
			Fast	$20^*(V_{dd}/5.5V)^{(5)(7)}$	300 <sup>(3)(7)</sup>	ns
111	$t_f(SDA)$	Fall time, SDA	Standard		300	ns
			Fast	$20^*(V_{dd}/5.5V)^{(5)(7)}$	300 <sup>(3)(7)</sup>	ns
112	$t_f(SCL)$	Fall time, SCL	Standard		300	ns
			Fast	$20^*(V_{dd}/5.5V)$	300	ns
113	$t_{su}(SCLH-SDAH)$	Setup time, SCL high before SDA high (for STOP condition)	Standard	4000		ns
			Fast	600		ns
114	$t_w(SP)$	Pulse duration, spike (must be suppressed)	Standard			ns
			Fast	0	50	ns
115	$t_{skew}$	Skew	Standard		3	ns
			Fast		3	ns
116	$C_b$	Capacitive load for each bus line	Standard		400	pF
			Fast		400	pF

- (1) The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
- (2) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement  $t_{su}(SDA-SCLH) \geq 250$  ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line  $t_{rmax} + t_{su}(SDA-SCLH) = 1000 + 250 = 1250$  ns (according to the Standard-mode I2C-Bus Specification) before the SCL line is released.
- (3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the  $V_{IHmin}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (4) The maximum  $t_h(SDA-SCLL)$  has only to be met if the device does not stretch the low period [ $t_w(SCLL)$ ] of the SCL signal.
- (5)  $C_b$  = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed
- (6) Software must properly configure the I2C module registers to achieve the timings shown in this table. See the device TRM for details.
- (7) These timings apply only to I2C0 and MCU\_I2C0. I2C[3:1] and MCU\_I2C1 use standard LVCMOS buffers to emulate open-drain buffers and their rise/fall times should be referenced in the device IBIS model.

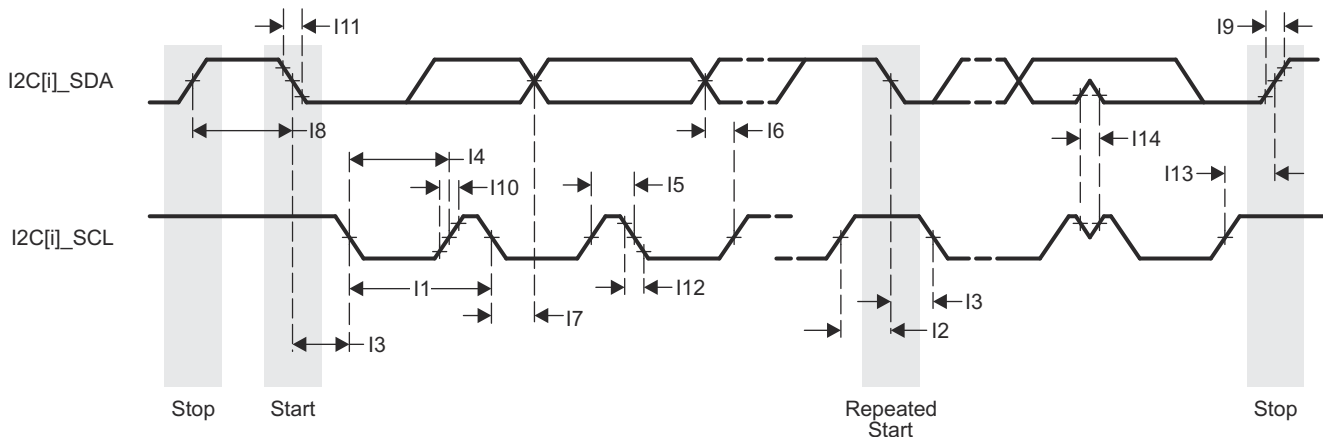
**Table 7-56. Timing Requirements for I2C HS-Mode**

NO.	PARAMETER	DESCRIPTION	CAPACITANCE	MIN	MAX	UNIT
11	$t_c(SCL)$	Cycle time, SCL	100 pF Max	294		ns
			400 pF Max	588		ns

Table 7-56. Timing Requirements for I2C HS-Mode (continued)

NO.	PARAMETER	DESCRIPTION	CAPACITANCE	MIN	MAX	UNIT
I2	$t_{su}(SCLH-SDAL)$	Setup time, SCL high before SDA low (for a repeated START condition)	100 pF Max	160		ns
			400 pF Max	160		ns
I3	$t_h(SDAL-SCLL)$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	100 pF Max	160		ns
			400 pF Max	160		ns
I4	$t_w(SCLL)$	Pulse duration, SCL low	100 pF Max	160		ns
			400 pF Max	320		ns
I5	$t_w(SCLH)$	Pulse duration, SCL high	100 pF Max	60		ns
			400 pF Max	120		ns
I6	$t_{su}(SDAV-SCLH)$	Setup time, SDA valid before SCL high	100 pF Max	10		ns
			400 pF Max	10		ns
I7	$t_h(SCLL-SDAV)$	Hold time, SDA valid after SCL low	100 pF Max	0	70	ns
			400 pF Max	0	150	ns
I13	$t_w(SDAH)$	Setup time, SCL high before SDA high (for STOP condition)	100 pF Max	160		ns
			400 pF Max	160 <sup>(2)</sup>		ns
I14	$t_r(SDA)$	Pulse duration, spike (must be suppressed)	100 pF Max	0	10 <sup>(2)</sup>	ns
			400 pF Max			ns
I15	$t_{skew}$	Skew				ns
I16	$C_b^{(1)}$	Capacitive Load for SDA and SCL Lines	100 pF Max		100	pF
			400 pF Max		400	pF

- (1) For bus line loads  $C_b$  between 100 pF and 400 pF the timing parameters must be linearly interpolated.  
 (2) A device must internally provide a Data hold time to bridge the undefined part between  $V_{IH}$  and  $V_{IL}$  of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.



- A.  $i = 0$  to 1 for MCU domain  
 $i = 0$  to 3 for MAIN domain

Figure 7-52. I2C Receive Timing

### 7.10.5.10 MCAN

Table 7-57 and Table 7-58 presents timing conditions and switching characteristics for MCAN.

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

**Note**

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

**Table 7-57. MCAN Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>I</sub>	Input slew rate	2	15	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	5	20	pF

**Table 7-58. MCAN Switching Characteristics**

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MCAN1	t <sub>d(MCAN_TX)</sub>	Delay time, transmit shift register to MCANn_TX		10	ns
MCAN2	t <sub>d(MCAN_RX)</sub>	Delay time, MCANn_RX to receive shift register		10	ns

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

**7.10.5.11 MCSPI**

For more details about features and additional description information on the device Serial Port Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

[Table 7-59](#) presents timing conditions for MCSPI.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

**Table 7-59. MCSPI Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>I</sub>	Input slew rate	2	8.5	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	6	12	pF

**7.10.5.11.1 MCSPI — Master Mode**

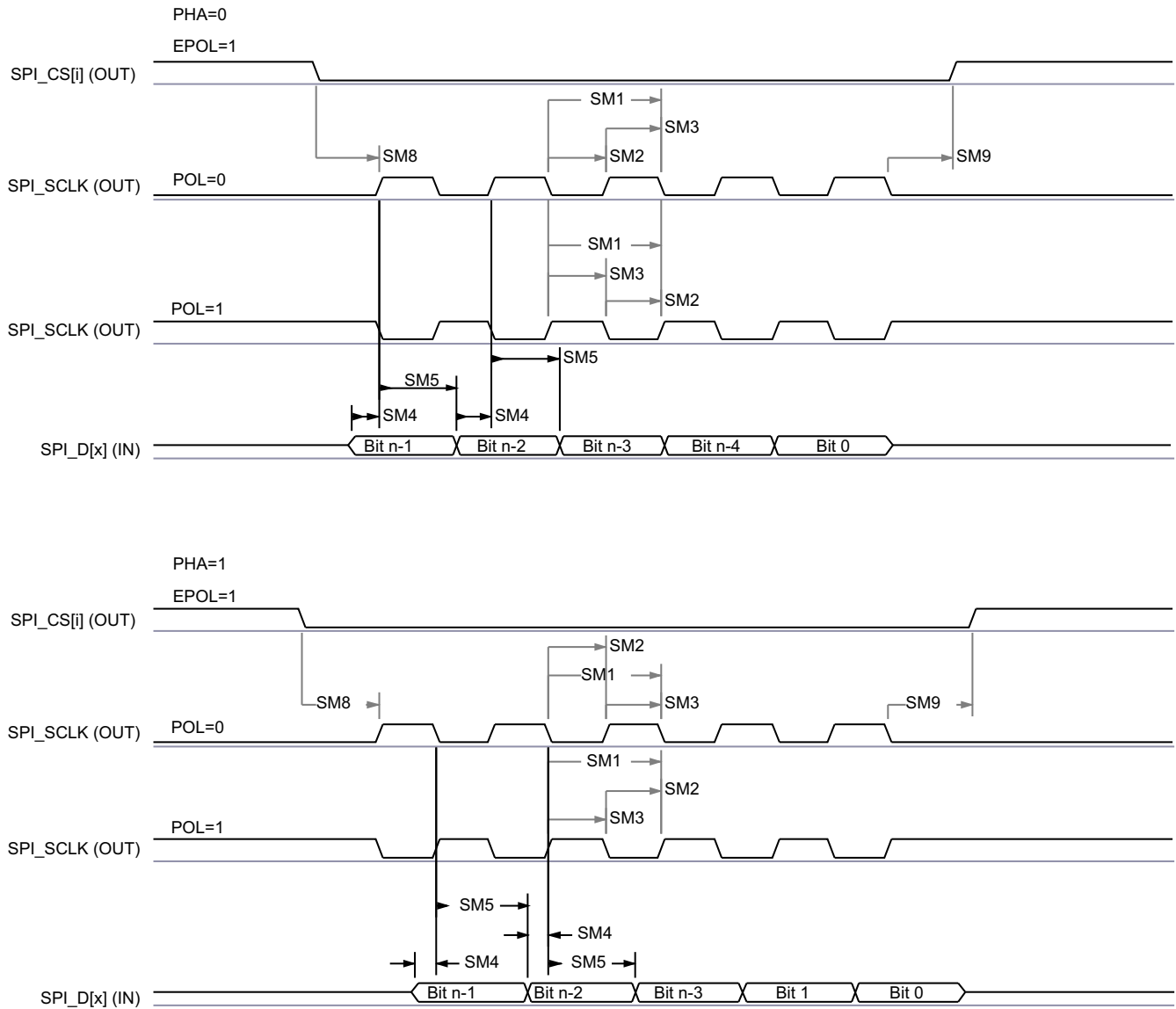
[Table 7-60](#), [Figure 7-53](#), [Table 7-61](#), and [Figure 7-54](#) present timing requirements and switching characteristics for SPI – Master Mode.

**Table 7-60. MCSPI Timing Requirements – Master Mode**

see [Figure 7-53](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SM4	t <sub>su(MISO-SPICLK)</sub>	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	2.8		ns
SM5	t <sub>h(SPICLK-MISO)</sub>	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	3		ns





SPRSP08\_TIMING\_MCSPI\_02

Figure 7-53. SPI Master Mode Receive Timing

Table 7-61. MCSPI Switching Characteristics - Master Mode

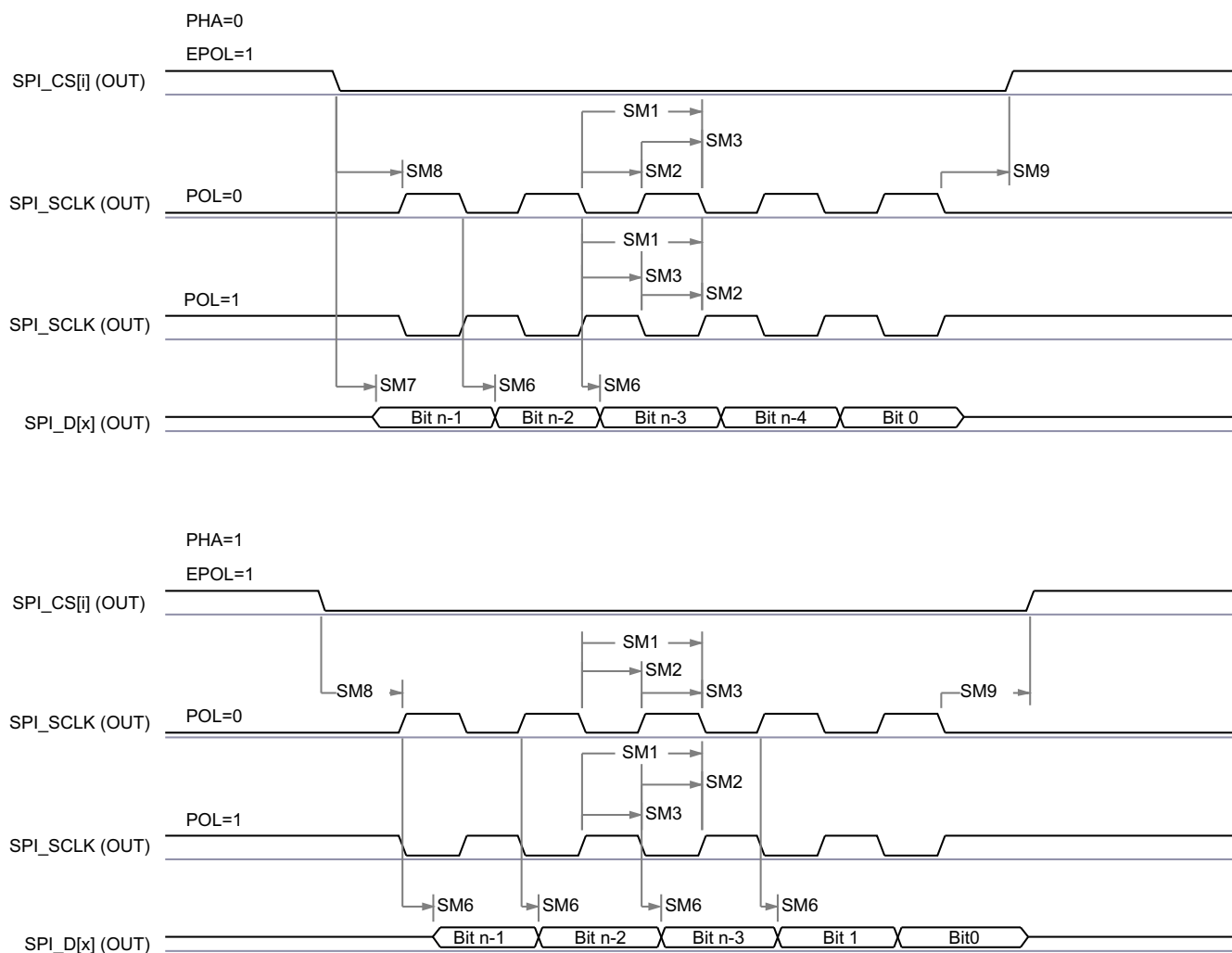
see Figure 7-54

NO.	PARAMETER		MIN	MAX	UNIT
SM1	$t_c(\text{SPICLK})$	Cycle time, SPIn_CLK	20		ns
SM2	$t_w(\text{SPICLK}_L)$	Pulse duration, SPIn_CLK low	$0.5P - 1^{(1)}$		ns
SM3	$t_w(\text{SPICLK}_H)$	Pulse duration, SPIn_CLK high	$0.5P - 1^{(1)}$		ns
SM6	$t_d(\text{SPICLK-SIMO})$	Delay time, SPIn_CLK active edge to SPIn_D[x]	-3	2.5	ns
SM7	$t_d(\text{CS-SIMO})$	Delay time, SPIn_CS <sub>i</sub> active edge to SPIn_D[x]	5		ns
SM8	$t_d(\text{CS-SPICLK})$	Delay time, SPIn_CS <sub>i</sub> active to SPIn_CLK first edge	PHA = 0	B - 4 <sup>(3)</sup>	ns
			PHA = 1	A - 4 <sup>(2)</sup>	ns
SM9	$t_d(\text{SPICLK-CS})$	Delay time, SPIn_CLK last edge to SPIn_CS <sub>i</sub> inactive	PHA = 0	A - 4 <sup>(2)</sup>	ns
			PHA = 1	B - 4 <sup>(3)</sup>	ns

(1) P = SPI\_CLK period in ns.

(2) When P = 20.8 ns, A = (TCS + 1) \* TSPICLKREF, where TCS is a bit field of the SPI\_CH(i)CONF register. When P > 20.8 ns, A = (TCS + 0.5) \* Fratio \* TSPICLKREF, where TCS is a bit field of the SPI\_CH(i)CONF register.

(3)  $B = (TCS + .5) * TSPICLKREF$ , where TCS is a bit field of the SPI\_CH(i)CONF register and Fratio = Even  $\geq 2$ .



SPRSP08\_TIMING\_McSPI\_01

**Figure 7-54. SPI Master Mode Transmit Timing**

### 7.10.5.11.2 MCSPI — Slave Mode

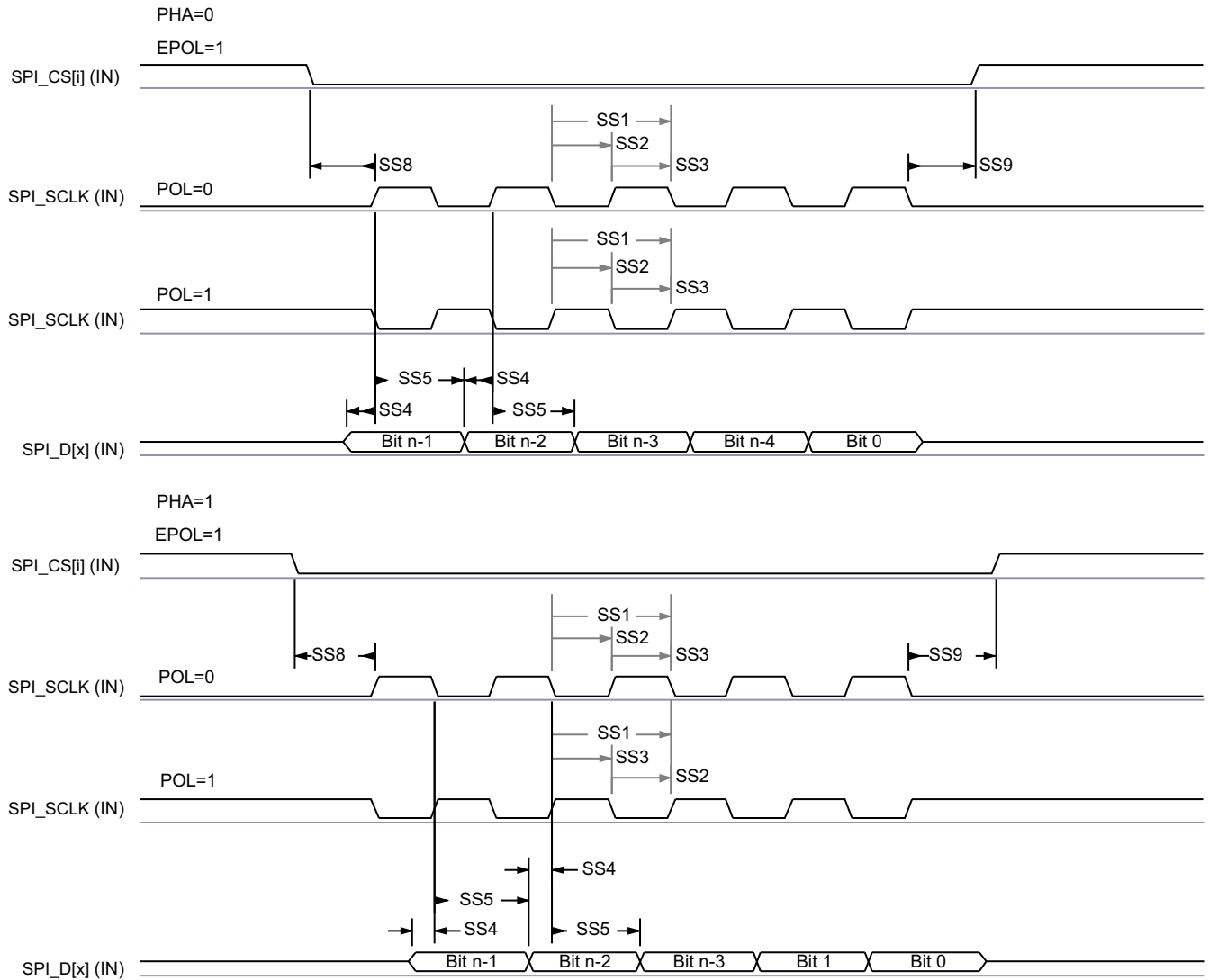
Table 7-62, Figure 7-55, Table 7-63, and Figure 7-56 present timing requirements and switching characteristics for SPI – Slave Mode.

**Table 7-62. MCSPI Timing Requirements – Slave Mode**

see Figure 7-55

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS1	$t_c(\text{SPICLK})$	Cycle time, SPIn_CLK	20		ns
SS2	$t_w(\text{SPICLK}_L)$	Pulse duration, SPIn_CLK low	$0.45P^{(1)}$		ns
SS3	$t_w(\text{SPICLK}_H)$	Pulse duration, SPIn_CLK high	$0.45P^{(1)}$		ns
SS4	$t_{su}(\text{SIMO-SPICLK})$	Setup time, SPIn_D[x] valid before SPIn_CLK active edge	5		ns
SS5	$t_h(\text{SPICLK-SIMO})$	Hold time, SPIn_D[x] valid after SPIn_CLK active edge	5		ns
SS8	$t_{su}(\text{CS-SPICLK})$	Setup time, SPIn_CSi valid before SPIn_CLK first edge	5		ns
SS9	$t_h(\text{SPICLK-CS})$	Hold time, SPIn_CSi valid after SPIn_CLK last edge	5		ns

(1)  $P = \text{SPIn\_CLK period in ns.}$



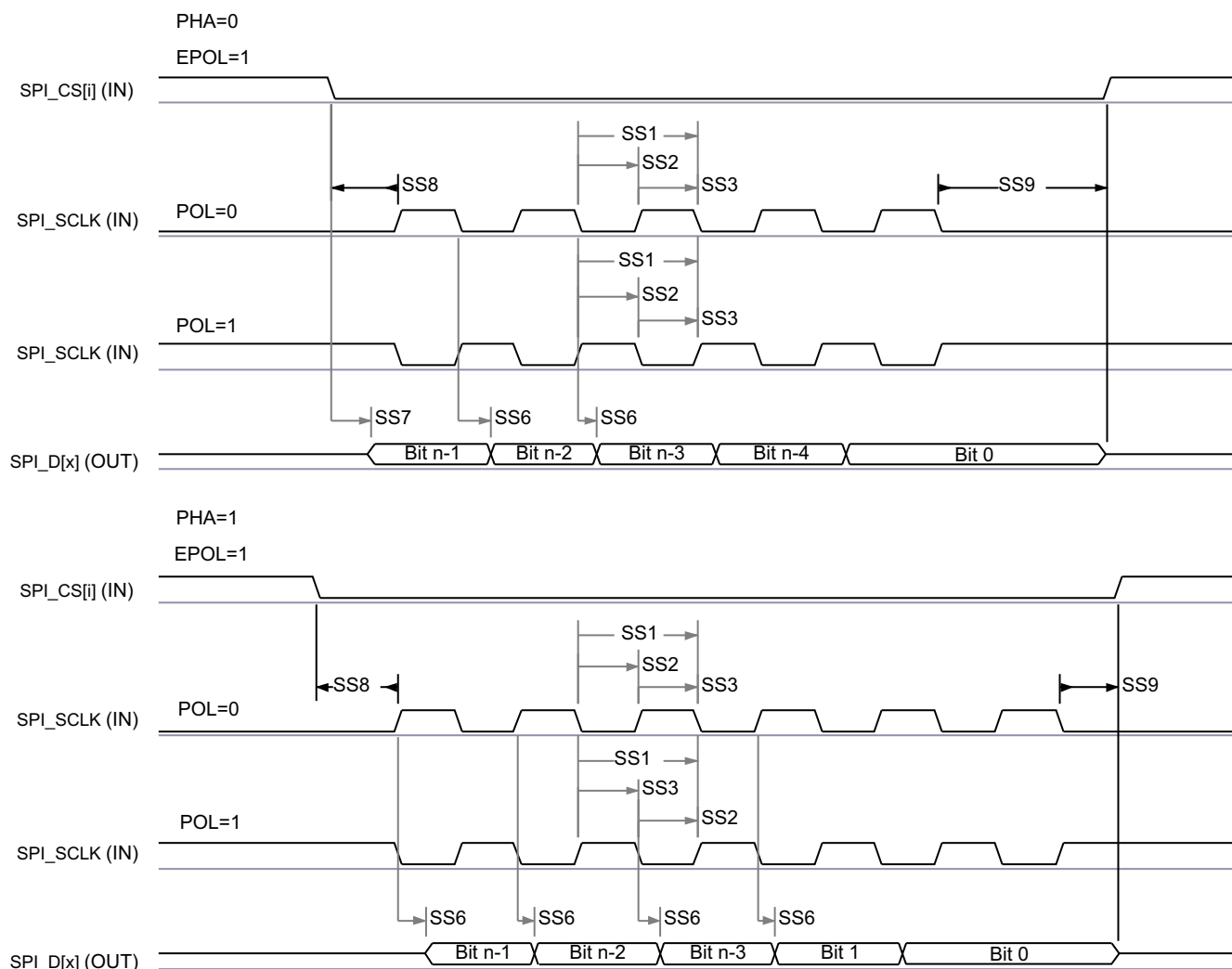
SPRSP08\_TIMING\_McSPI\_04

Figure 7-55. SPI Slave Mode Receive Timing

Table 7-63. MCSPI Switching Characteristics – Slave Mode

see Figure 7-56

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS6	$t_{d(SPICLK-SOMI)}$	Delay time, SPIn_CLK active edge to SPIn_D[x]	2	17.12	ns
SS7	$t_{sk(CS-SOMI)}$	Delay time, SPIn_CSi active edge to SPIn_D[x]	20.95		ns



SPRSP08\_TIMING\_McSPI\_03

Figure 7-56. SPI Slave Mode Transmit Timing

#### 7.10.5.12 MMCSD

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC), Secure Digital (SD), and Secure Digital IO (SDIO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSD interfaces, see the corresponding MMC0 and MMC1 subsections within *Signal Descriptions* and *Detailed Description* sections.

#### Note

Some operating modes require software configuration of the MMC DLL delay settings, as shown in [Table 7-64](#) and [Table 7-73](#).

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

### 7.10.5.12.1 MMC0 - eMMC Interface

MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and it supports the following eMMC applications:

- Legacy speed
- High speed SDR
- High speed DDR
- HS200

Table 7-64 presents the required DLL software configuration settings for MMC0 timing modes.

**Table 7-64. MMC0 DLL Delay Mapping for All Timing Modes**

REGISTER NAME		MMCS0_SS_PHY_CTRL_4_REG					MMCS0_SS_PHY_CTRL_5_REG		
BIT FIELD		[31:24]	[20]	[15:12]	[8]	[4:0]	[17:16]	[10:8]	[2:0]
BIT FIELD NAME		STRBSEL	OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	SELDLYTXCLK SELDLYRXCLK	FRQSEL	CLKBUFSEL
MODE	DESCRIPTION	STROBE DELAY	OUTPUT DELAY ENABLE	OUTPUT DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DLL DELAY CHAIN SELECT	DLL REF FREQUENCY	DELAY BUFFER DURATION
Legacy SDR	8-bit PHY operating 1.8 V, 25 MHz	0x0	0x0	NA	0x1	0x10	0x1	0x0	0x7
High Speed SDR	8-bit PHY operating 1.8 V, 50 MHz	0x0	0x0	NA	0x1	0xA	0x1	0x0	0x7
High Speed DDR	8-bit PHY operating 1.8 V, 50 MHz	0x0	0x1	0x6	0x1	0x3	0x0	0x4	0x7
HS200	8-bit PHY operating 1.8 V, 200 MHz	0x0	0x1	0x7	0x1	Tuning	0x0	0x0	0x7

Table 7-65 presents timing conditions for MMC0.

**Table 7-65. MMC0 Timing Conditions**

PARAMETER		MIN	MAX	UNIT	
<b>INPUT CONDITIONS</b>					
SR <sub>i</sub>	Input slew rate	Legacy SDR	0.14	1.44	V/ns
		High Speed SDR	0.3	0.9	V/ns
		High Speed DDR (CMD)	0.3	0.9	V/ns
		High Speed DDR (DAT[7:0])	0.45	0.9	V/ns
<b>OUTPUT CONDITIONS</b>					
C <sub>L</sub>	Output load capacitance	Legacy SDR	1	12	pF
		High Speed SDR	1	12	pF
		High Speed DDR	1	12	pF
		HS200	1	6	pF
<b>PCB CONNECTIVITY REQUIREMENTS</b>					
t <sub>d</sub> (Trace Delay)	Propagation delay of each trace	All modes	126	756	ps
t <sub>d</sub> (Trace Mismatch Delay)	Propagation delay mismatch across all traces	Legacy SDR, High Speed SDR		100	ps
		High Speed DDR, HS200		8	ps

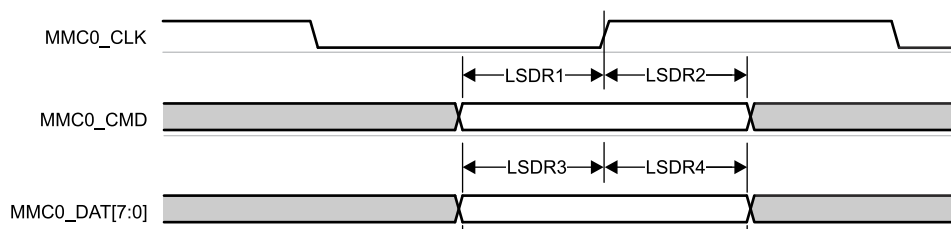
**7.10.5.12.1.1 Legacy SDR Mode**

Table 7-66, Figure 7-57, Table 7-67, and Figure 7-58 present timing requirements and switching characteristics for MMC0 – Legacy SDR Mode.

**Table 7-66. MMC0 Timing Requirements – Legacy SDR Mode**

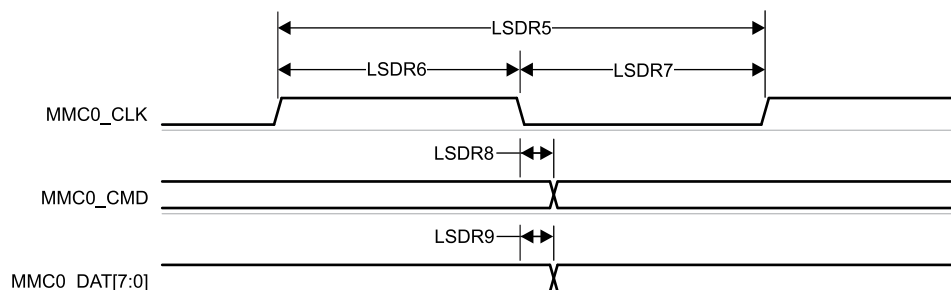
see Figure 7-57

NO.			MIN	MAX	UNIT
LSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	9.69		ns
LSDR2	$t_h(clkH-cmdV)$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	27.97		ns
LSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	9.69		ns
LSDR4	$t_h(clkH-dV)$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	27.97		ns


**Figure 7-57. MMC0 – Legacy SDR – Receive Mode**
**Table 7-67. MMC0 Switching Characteristics – Legacy SDR Mode**

see Figure 7-58

NO.	PARAMETER	MIN	MAX	UNIT
	$f_{op(clk)}$		25	MHz
LSDR5	$t_c(clk)$	40		ns
LSDR6	$t_w(clkH)$	18.7		ns
LSDR7	$t_w(clkL)$	18.7		ns
LSDR8	$t_d(clkL-cmdV)$	-16.1	16.1	ns
LSDR9	$t_d(clkL-dV)$	-16.1	16.1	ns


**Figure 7-58. MMC0 – Legacy SDR – Transmit Mode**

7.10.5.12.1.2 High Speed SDR Mode

Table 7-68, Figure 7-59, Table 7-69, and Figure 7-60 present timing requirements and switching characteristics for MMC0 – High Speed SDR Mode.

Table 7-68. MMC0 Timing Requirements – High Speed SDR Mode

see Figure 7-59

NO.			MIN	MAX	UNIT
HSSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2.99		ns
HSSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	2.67		ns
HSSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	2.99		ns
HSSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	2.67		ns

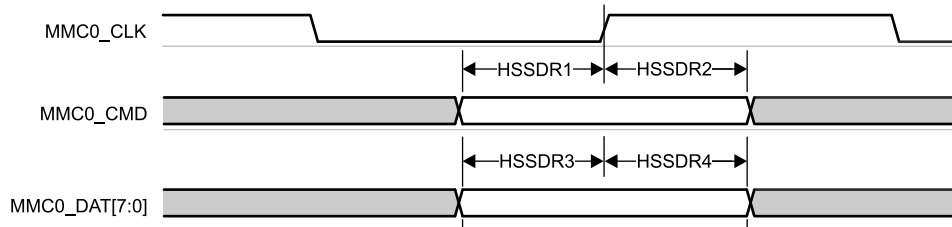


Figure 7-59. MMC0 – High Speed SDR Mode – Receive Mode

Table 7-69. MMC0 Switching Characteristics – High Speed SDR Mode

see Figure 7-60

NO.	PARAMETER	MIN	MAX	UNIT
	$f_{op(clk)}$		50	MHz
HSSDR5	$t_{c(clk)}$	20		ns
HSSDR6	$t_{w(clkH)}$	9.2		ns
HSSDR7	$t_{w(clkL)}$	9.2		ns
HSSDR8	$t_{d(clkL-cmdV)}$	-6.35	6.35	ns
HSSDR9	$t_{d(clkL-dV)}$	-6.35	6.35	ns

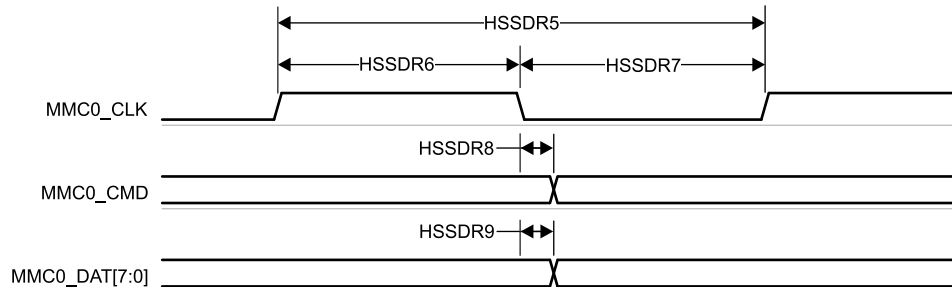


Figure 7-60. MMC0 – High Speed SDR Mode – Transmit Mode

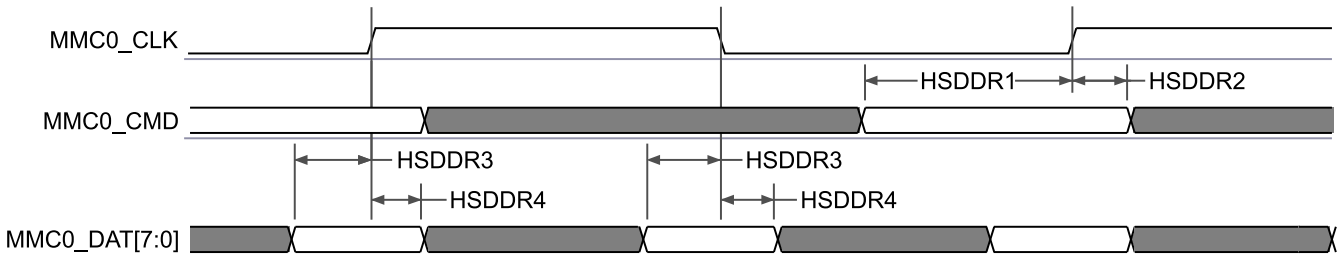
**7.10.5.12.1.3 High Speed DDR Mode**

Table 7-70, Figure 7-61, Table 7-71, and Figure 7-62 present timing requirements and switching characteristics for MMC0 – High Speed DDR Mode.

**Table 7-70. MMC0 Timing Requirements – High Speed DDR Mode**

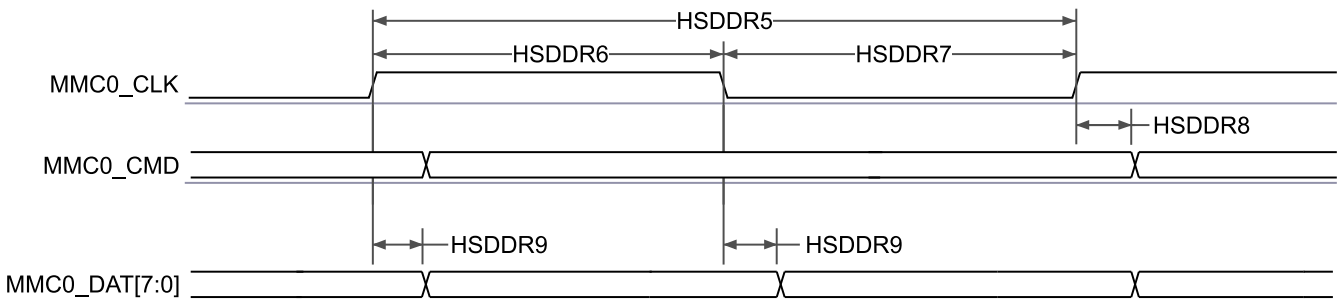
see Figure 7-61

NO.			MIN	MAX	UNIT
HSDDR1	$t_{su(cmdV-clk)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	3.88		ns
HSDDR2	$t_{h(clk-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	2.67		ns
HSDDR3	$t_{su(dV-clk)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK transition	0.83		ns
HSDDR4	$t_{h(clk-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK transition	1.76		ns


**Figure 7-61. MMC0 – High Speed DDR Mode – Receive Mode**
**Table 7-71. MMC0 Switching Characteristics – High Speed DDR Mode**

see Figure 7-62

NO.	PARAMETER	MIN	MAX	UNIT
	$f_{op(clk)}$		50	MHz
HSDDR5	$t_{c(clk)}$	20		ns
HSDDR6	$t_{w(clkH)}$	9.2		ns
HSDDR7	$t_{w(clkL)}$	9.2		ns
HSDDR8	$t_{d(clk-cmdV)}$	3.31	16.19	ns
HSDDR9	$t_{d(clk-dV)}$	2.81	6.94	ns


**Figure 7-62. MMC0 – High Speed DDR Mode – Transmit Mode**



7.10.5.12.1.4 HS200 Mode

Table 7-72 and Figure 7-63 present switching characteristics for MMC0 – HS200 Mode.

Table 7-72. MMC0 Switching Characteristics – HS200 Mode

see Figure 7-63

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op}(clk)$	Operating frequency, MMC0_CLK		200	MHz
HS2005	$t_c(clk)$	Cycle time, MMC0_CLK	5		ns
HS2006	$t_w(clkH)$	Pulse duration, MMC0_CLK high	2.08		ns
HS2007	$t_w(clkL)$	Pulse duration, MMC0_CLK low	2.08		ns
HS2008	$t_d(clkL-cmdV)$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	0.99	3.28	ns
HS2009	$t_d(clkL-dV)$	Delay time, MMC0_CLK rising edge to MMC0_DAT[7:0] transition	0.99	3.28	ns

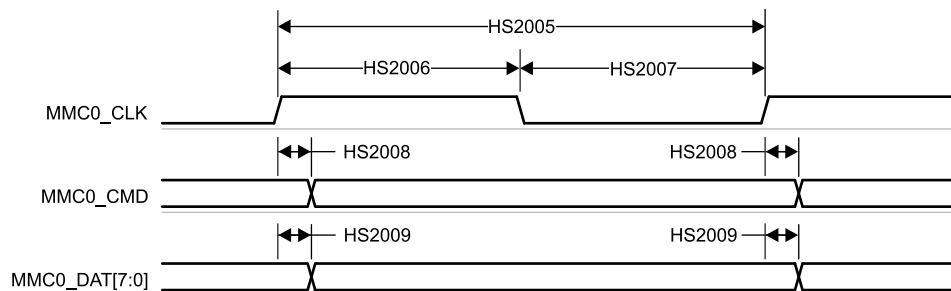


Figure 7-63. MMC0 – HS200 Mode – Transmit Mode

7.10.5.12.2 MMC1 - SD/SDIO Interface

MMC1 interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and it supports the following SD Card applications:

- Default speed
- High speed
- UHS-I SDR12
- UHS-I SDR25
- UHS-I SDR50
- UHS-I SDR104
- UHS-I DDR50

Table 7-73 presents the required DLL software configuration settings for MMC1 timing modes.

Table 7-73. MMC1 DLL Delay Mapping for All Timing Modes

REGISTER NAME		MMCSD1_SS_PHY_CTRL_4_REG				MMCSD1_SS_PHY_CTRL_5_REG
BIT FIELD		[20]	[15:12]	[8]	[4:0]	[2:0]
BIT FIELD NAME		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL
MODE	DESCRIPTION	DELAY ENABLE	DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DELAY BUFFER DURATION
Default Speed	4-bit PHY operating 3.3 V, 25 MHz	0x0	0x0	0x1	0x0	0x7
High Speed	4-bit PHY operating 3.3 V, 50 MHz	0x0	0x0	0x1	0x0	0x7
UHS-I SDR12	4-bit PHY operating 1.8 V, 25 MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR25	4-bit PHY operating 1.8 V, 50 MHz	0x1	0xF	0x1	0x0	0x7
UHS-I SDR50	4-bit PHY operating 1.8 V, 100 MHz	0x1	0xC	0x1	Tuning	0x7

**Table 7-73. MMC1 DLL Delay Mapping for All Timing Modes (continued)**

REGISTER NAME		MMCSD1_SS_PHY_CTRL_4_REG				MMCSD1_SS_PHY_CTRL_5_REG
BIT FIELD		[20]	[15:12]	[8]	[4:0]	[2:0]
BIT FIELD NAME		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL
MODE	DESCRIPTION	DELAY ENABLE	DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DELAY BUFFER DURATION
UHS-I DR50	4-bit PHY operating 1.8 V, 50 MHz	0x1	0x9	0x1	Tuning	0x7
UHS-I SDR104	4-bit PHY operating 1.8, V 200 MHz	0x1	0x6	0x1	Tuning	0x7

Table 7-74 presents timing conditions for MMC1.

**Table 7-74. MMC1 Timing Conditions**

PARAMETER		MIN	MAX	UNIT	
<b>Input Conditions</b>					
SR <sub>i</sub>	Input slew rate	Default Speed, High Speed	0.69	2.06	V/ns
		UHS-I SDR12, UHS-I SDR25	0.34	1.34	V/ns
		UHS-I DDR50	1	2	V/ns
<b>Output Conditions</b>					
C <sub>L</sub>	Output load capacitance	UHS-I DDR50	3	10	pF
		All other modes	1	10	pF
<b>PCB Connectivity Requirements</b>					
t <sub>d</sub> (Trace Delay)	Propagation delay of each trace	UHS-I DDR50	240	1134	ps
		All other modes	126	1386	ps
t <sub>d</sub> (Trace Mismatch Delay)	Propagation delay mismatch across all traces	UHS-I DDR50, UHS-I SDR104		20	ps
		All other modes		100	ps

7.10.5.12.2.1 Default Speed Mode

Table 7-75, Figure 7-64, Table 7-76, and Figure 7-65 present timing requirements and switching characteristics for MMC1 – Default Speed Mode.

Table 7-75. Timing Requirements for MMC1 – Default Speed Mode

see Figure 7-64

NO.			MIN	MAX	UNIT
DS1	$t_{su}(cmdV-clkH)$	Setup time, MMC1_CMD valid before MMCi_CLK rising edge	2.55		ns
DS2	$t_h(clkH-cmdV)$	Hold time, MMC1_CMD valid after MMC1_CLK rising edge	19.67		ns
DS3	$t_{su}(dV-clkH)$	Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge	2.55		ns
DS4	$t_h(clkH-dV)$	Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge	19.67		ns

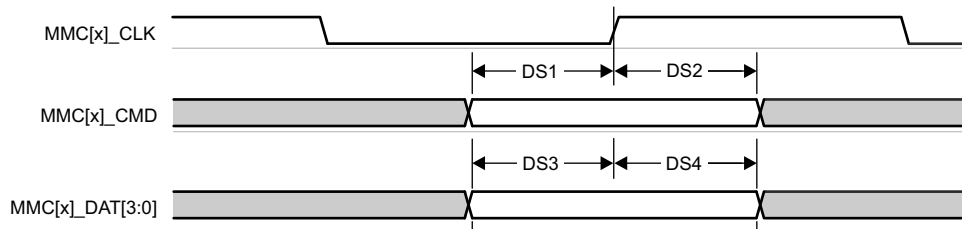


Figure 7-64. MMC1 – Default Speed – Receive Mode

Table 7-76. Switching Characteristics for MMC1 – Default Speed Mode

see Figure 7-65

NO.	PARAMETER	MIN	MAX	UNIT
	$f_{op}(clk)$		25	MHz
DS5	$t_c(clk)$	40		ns
DS6	$t_w(clkH)$	18.7		ns
DS7	$t_w(clkL)$	18.7		ns
DS8	$t_d(clkL-cmdV)$	- 14.1	14.1	ns
DS9	$t_d(clkL-dV)$	- 14.1	14.1	ns

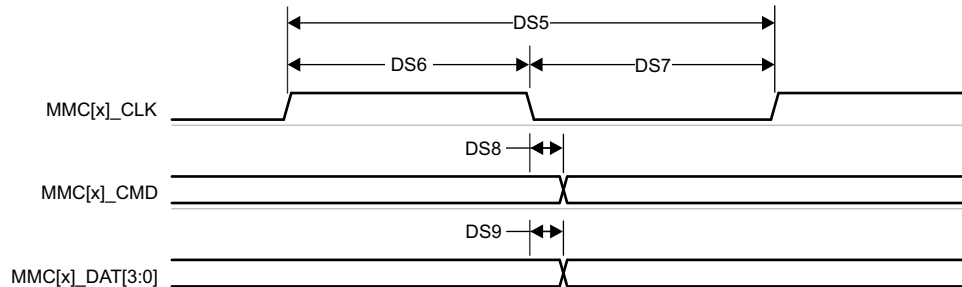


Figure 7-65. MMC1 – Default Speed – Transmit Mode

7.10.5.12.2.2 High Speed Mode

Table 7-77, Figure 7-66, Table 7-78, and Figure 7-67 present timing requirements and switching characteristics for MMC1 – High Speed Mode.

Table 7-77. Timing Requirements for MMC1 – High Speed Mode

see Figure 7-66

NO.			MIN	MAX	UNIT
HS1	$t_{su(cmdV-clkH)}$	Setup time, MMC1_CMD valid before MMC1_CLK rising edge	2.55		ns
HS2	$t_h(clkH-cmdV)$	Hold time, MMC1_CMD valid after MMC1_CLK rising edge	2.67		ns
HS3	$t_{su(dV-clkH)}$	Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge	2.55		ns
HS4	$t_h(clkH-dV)$	Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge	2.67		ns

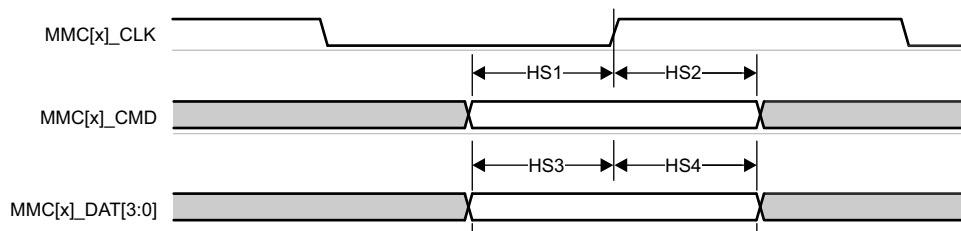


Figure 7-66. MMC1 – High Speed – Receive Mode

Table 7-78. Switching Characteristics for MMC1 – High Speed Mode

see Figure 7-67

NO.	PARAMETER	MIN	MAX	UNIT
	$f_{op(clk)}$		50	MHz
HS5	$t_c(clk)$	20		ns
HS6	$t_w(clkH)$	9.2		ns
HS7	$t_w(clkL)$	9.2		ns
HS8	$t_d(clkL-cmdV)$	-7.35	3.35	ns
HS9	$t_d(clkL-dV)$	-7.35	3.35	ns

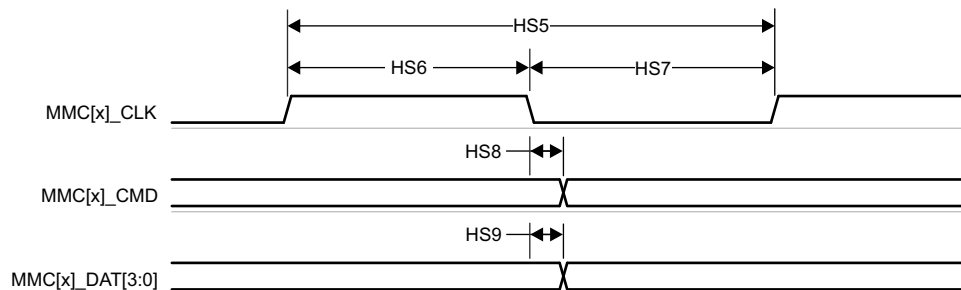


Figure 7-67. MMC1 – High Speed – Transmit Mode

7.10.5.12.2.3 UHS-I SDR12 Mode

Table 7-79, Figure 7-68, Table 7-80, and Figure 7-69 present timing requirements and switching characteristics for MMC1 – UHS-I SDR12 Mode.

Table 7-79. Timing Requirements for MMC1 – UHS-I SDR12 Mode

see Figure 7-68

NO.			MIN	MAX	UNIT
SDR121	$t_{su(cmdV-clkH)}$	Setup time, MMC1_CMD valid before MMC1_CLK rising edge	21.65		ns
SDR122	$t_{h(clkH-cmdV)}$	Hold time, MMC1_CMD valid after MMC1_CLK rising edge	1.67		ns
SDR123	$t_{su(dV-clkH)}$	Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge	21.65		ns
SDR124	$t_{h(clkH-dV)}$	Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge	1.67		ns

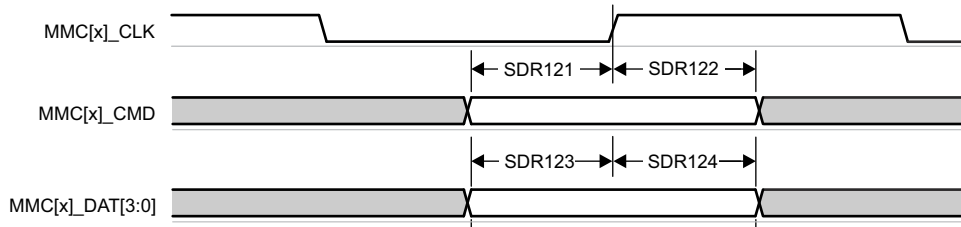


Figure 7-68. MMC1 – UHS-I SDR12 – Receive Mode

Table 7-80. Switching Characteristics for MMC1 – UHS-I SDR12 Mode

see Figure 7-69

NO.	PARAMETER	MIN	MAX	UNIT
	$f_{op(clk)}$		25	MHz
SDR125	$t_{c(clk)}$	40		ns
SDR126	$t_{w(clkH)}$	18.7		ns
SDR127	$t_{w(clkL)}$	18.7		ns
SDR128	$t_{d(clkL-cmdV)}$	-13.6	13.6	ns
SDR129	$t_{d(clkL-dV)}$	-13.6	13.6	ns

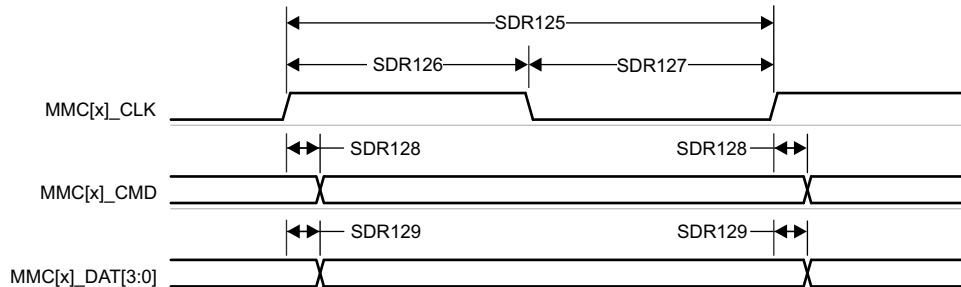


Figure 7-69. MMC1 – UHS-I SDR12 – Transmit Mode

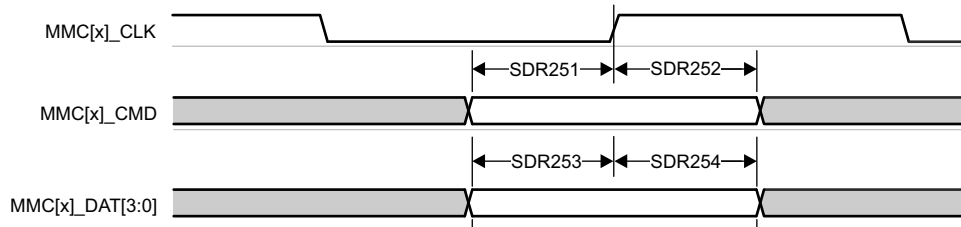
7.10.5.12.2.4 UHS-I SDR25 Mode

Table 7-81, Figure 7-70, Table 7-82, and Figure 7-71 present timing requirements and switching characteristics for MMC1 – UHS-I SDR25 Mode.

**Table 7-81. Timing Requirements for MMC1 – UHS-I SDR25 Mode**

see Figure 7-70

NO.			MIN	MAX	UNIT
SDR251	$t_{su(cmdV-clkH)}$	Setup time, MMC1_CMD valid before MMC1_CLK rising edge	2.15		ns
SDR252	$t_{h(clkH-cmdV)}$	Hold time, MMC1_CMD valid after MMC1_CLK rising edge	1.67		ns
SDR253	$t_{su(dV-clkH)}$	Setup time, MMC1_DAT[3:0] valid before MMC1_CLK rising edge	2.15		ns
SDR254	$t_{h(clkH-dV)}$	Hold time, MMC1_DAT[3:0] valid after MMC1_CLK rising edge	1.67		ns

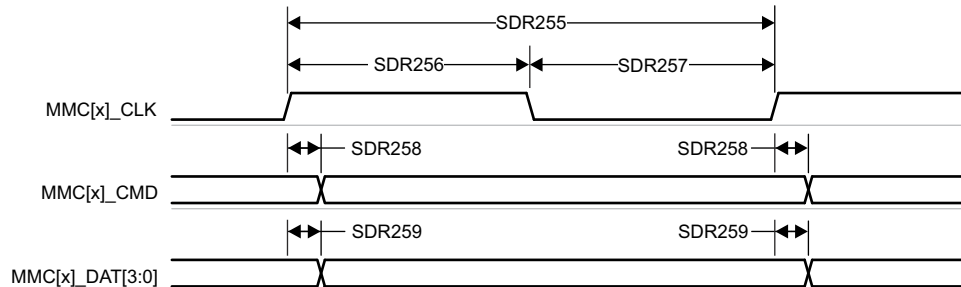


**Figure 7-70. MMC1 – UHS-I SDR25 – Receive Mode**

**Table 7-82. Switching Characteristics for MMC1 – UHS-I SDR25 Mode**

see Figure 7-71

NO.	PARAMETER	MIN	MAX	UNIT
	$f_{op(clk)}$		50	MHz
SDR255	$t_{c(clk)}$	20		ns
SDR256	$t_{w(clkH)}$	9.2		ns
SDR257	$t_{w(clkL)}$	9.2		ns
SDR258	$t_{d(clkL-cmdV)}$	-7.1	3.1	ns
SDR259	$t_{d(clkL-dV)}$	-7.1	3.1	ns



**Figure 7-71. MMC1 – UHS-I SDR25 – Transmit Mode**

ADVANCE INFORMATION

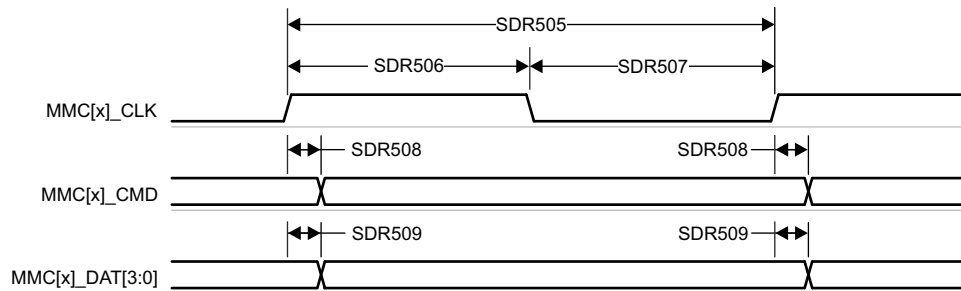
7.10.5.12.2.5 UHS-I SDR50 Mode

Table 7-83, and Figure 7-72 presents switching characteristics for MMC1 – UHS-I SDR50 Mode.

**Table 7-83. Switching Characteristics for MMC1 – UHS-I SDR50 Mode**

see Figure 7-72

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op}(clk)$	Operating frequency, MMC1_CLK		100	MHz
SDR505	$t_{c}(clk)$	Cycle time, MMC1_CLK	10		ns
SDR506	$t_{w}(clkH)$	Pulse duration, MMC1_CLK high	4.45		ns
SDR507	$t_{w}(clkL)$	Pulse duration, MMC1_CLK low	4.45		ns
SDR508	$t_{d}(clkL-cmdV)$	Delay time, MMC1_CLK rising edge to MMC1_CMD transition	1.2	6.35	ns
SDR509	$t_{d}(clkL-dV)$	Delay time, MMC1_CLK rising edge to MMC1_DAT[3:0] transition	1.2	6.35	ns



**Figure 7-72. MMC1 – UHS-I SDR50 – Transmit Mode**

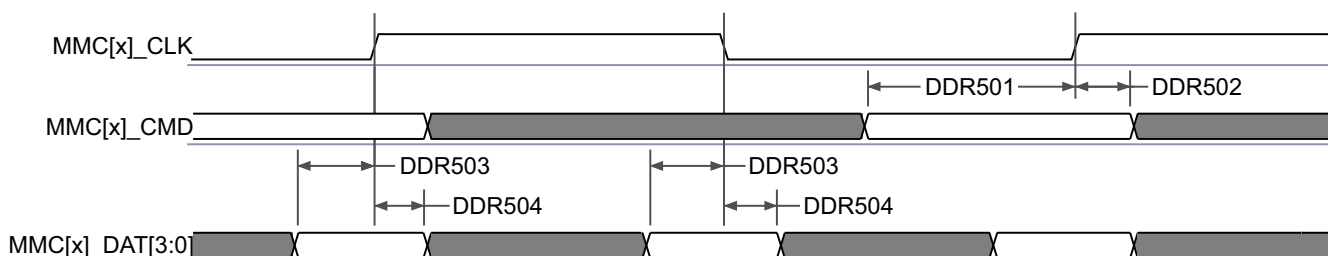
**7.10.5.12.2.6 UHS-I DDR50 Mode**

Table 7-84, Figure 7-73, Table 7-85, and Figure 7-74 present timing requirements and switching characteristics for MMC1 – UHS-I DDR50 Mode.

**Table 7-84. Timing Requirements for MMC1 – UHS-I DDR50 Mode**

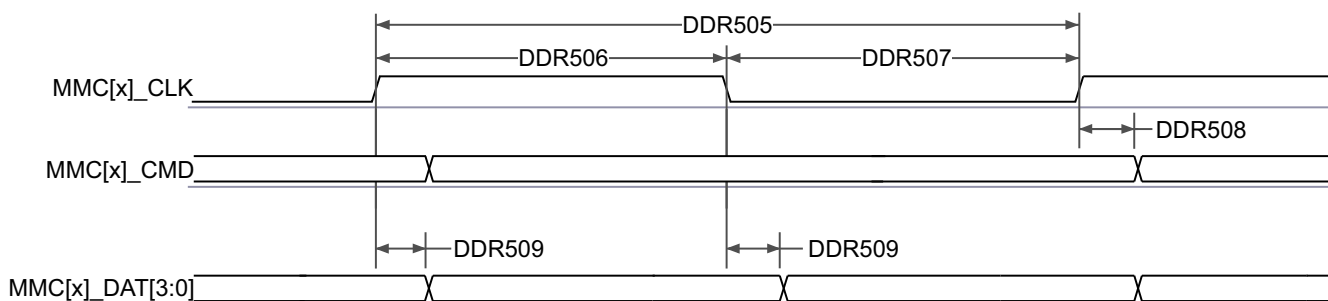
see Figure 7-73

NO.			MIN	MAX	UNIT
DDR501	$t_{su(cmdV-clk)}$	Setup time, MMC1_CMD valid before MMC1_CLK rising edge	2.99		ns
DDR502	$t_h(clk-cmdV)$	Hold time, MMC1_CMD valid after MMC1_CLK rising edge	1.91		ns
DDR503	$t_{su(dV-clk)}$	Setup time, MMC1_DAT[3:0] valid before MMC1_CLK transition	-0.06		ns
DDR504	$t_h(clk-dV)$	Hold time, MMC1_DAT[3:0] valid after MMC1_CLK transition	1.91		ns


**Figure 7-73. MMC1 – UHS-I DDR50 – Receive Mode**
**Table 7-85. Switching Characteristics for MMC1 – UHS-I DDR50 Mode**

see Figure 7-74

NO.	PARAMETER	MIN	MAX	UNIT
	$f_{op(clk)}$		50	MHz
DDR505	$t_{c(clk)}$	20		ns
DDR506	$t_w(clkH)$	9.2		ns
DDR507	$t_w(clkL)$	9.2		ns
DDR508	$t_d(clk-cmdV)$	1.2	13.1	ns
DDR509	$t_d(clk-dV)$	1.2	6.35	ns


**Figure 7-74. MMC1 – UHS-I DDR50 – Transmit Mode**



7.10.5.12.2.7 UHS-I SDR104 Mode

Table 7-86, and Figure 7-75 present switching characteristics for MMC1 – UHS-I SDR104 Mode.

Table 7-86. Switching Characteristics for MMC1 – UHS-I SDR104 Mode

see Figure 7-75

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op}(clk)$	Operating frequency, MMC1_CLK		200	MHz
SDR1045	$t_{c}(clk)$	Cycle time, MMC1_CLK	5		ns
SDR1046	$t_{w}(clkH)$	Pulse duration, MMC1_CLK high	2.08		ns
SDR1047	$t_{w}(clkL)$	Pulse duration, MMC1_CLK low	2.08		ns
SDR1048	$t_{d}(clkL-cmdV)$	Delay time, MMC1_CLK rising edge to MMC1_CMD transition	1.12	3.16	ns
SDR1049	$t_{d}(clkL-dV)$	Delay time, MMC1_CLK rising edge to MMC1_DAT[3:0] transition	1.12	3.16	ns

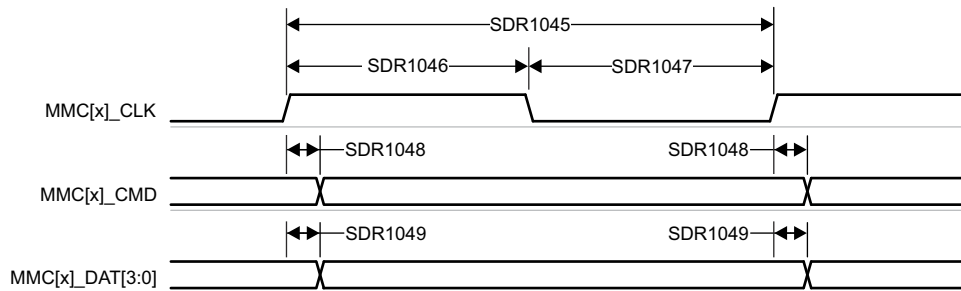


Figure 7-75. MMC1 – UHS-I SDR104 – Transmit Mode

7.10.5.13 CPTS

Table 7-87, Table 7-88, Figure 7-76, Table 7-89, and Figure 7-77 present timing conditions, requirements, and switching characteristics for CPTS.

Table 7-87. CPTS Timing Conditions

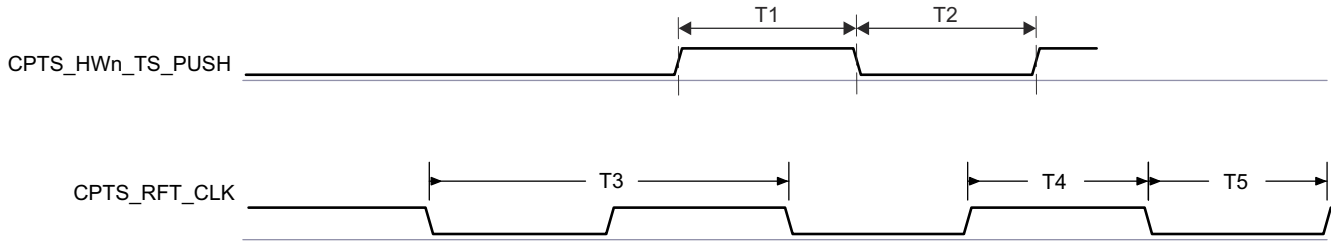
PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
$SR_i$	Input slew rate	0.5	5	V/ns
<b>OUTPUT CONDITIONS</b>				
$C_L$	Output load capacitance	2	10	pF

Table 7-88. CPTS Timing Requirements

see Figure 7-76

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T1	$t_{w}(HWTSPUSHH)$	Pulse duration, CPTS_HWn_TS_PUSH high	$2 + 12P^{(1)}$		ns
T2	$t_{w}(HWTSPUSHL)$	Pulse duration, CPTS_HWn_TS_PUSH low	$2 + 12P^{(1)}$		ns
T3	$t_{c}(RFT\_CLK)$	Cycle time, CPTS_RFT_CLK	5	8	ns
T4	$t_{w}(RFT\_CLKH)$	Pulse duration, CPTS_RFT_CLK high	$0.45 \times t_{c}(RFT\_CLK)$		ns
T5	$t_{w}(RFT\_CLKL)$	Pulse duration, CPTS_RFT_CLK low	$0.45 \times t_{c}(RFT\_CLK)$		ns

(1) P = functional clock period in ns.



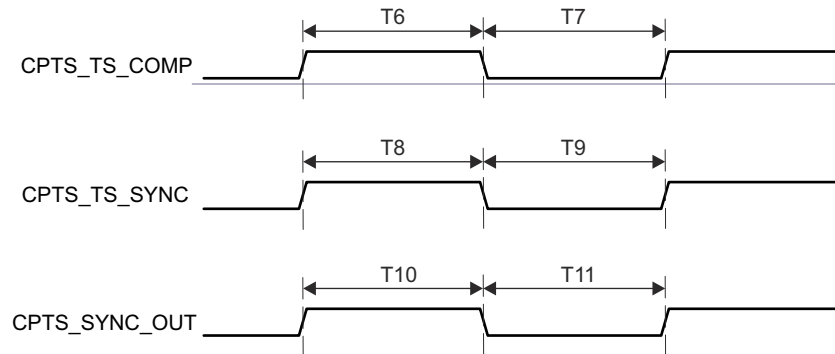
**Figure 7-76. CPTS Timing Requirements**

**Table 7-89. CPTS Switching Characteristics**

see [Figure 7-77](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T6	$t_w(TS\_COMPH)$	Pulse duration, CPTS_TS_COMP high	-2+36P <sup>(1)</sup>		ns
T7	$t_w(TS\_COMPL)$	Pulse duration, CPTS_TS_COMP low	-2+36P <sup>(1)</sup>		ns
T10	$t_w(TS\_SYNCH)$	Pulse duration, CPTS_TS_SYNC high	-2+36P <sup>(1)</sup>		ns
T11	$t_w(TS\_SYNCL)$	Pulse duration, CPTS_TS_SYNC low	-2+36P <sup>(1)</sup>		ns
T14	$t_w(SYNC\_OUTH)$	Pulse duration, CPTS_TS_SYNC sourcing CPTS_SYNCn_OUT high	-2+36P <sup>(1)</sup>		ns
T15	$t_w(SYNC\_OUTL)$	Pulse duration, CPTS_TS_SYNC sourcing CPTS_SYNCn_OUT low	-2+36P <sup>(1)</sup>		ns
T16	$t_w(SYNC\_OUTH)$	Pulse duration, GENF sourcing CPTS_SYNCn_OUT high	-2+5P <sup>(1)</sup>		ns
T17	$t_w(SYNC\_OUTL)$	Pulse duration, GENF sourcing CPTS_SYNCn_OUT low	-2+5P <sup>(1)</sup>		ns

(1) P = functional clock period in ns.



**Figure 7-77. CPTS Switching Characteristics**

For more information, see *Navigator Subsystem (NAVSS)* section in *Data Movement Architecture (DMA)* chapter in the device TRM.

**7.10.5.14 OSPI**

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

[Table 7-90](#) presents timing conditions for OSPI.

**Table 7-90. OSPI Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>i</sub>	Input slew rate	1	6	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	3	10	pF

**Table 7-90. OSPI Timing Conditions (continued)**

PARAMETER		MIN	MAX	UNIT
<b>PCB CONNECTIVITY REQUIREMENTS</b>				
$t_d$ (Trace Delay)	Propagation delay of each trace		450	ps
$t_d$ (Trace Mismatch Delay)	Propagation delay mismatch across all traces		60	ps

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

#### 7.10.5.14.1 OSPI With Data Training

##### 7.10.5.14.1.1 OSPI Switching Characteristics – Data Training

Table 7-91 presents switching characteristics for OSPI with Data Training.

**Table 7-91. OSPI Switching Characteristics – Data Training**

PARAMETER		MODE	MIN	MAX	UNIT
$t_c$ (CLK)	Cycle time, CLK	1.8V, SDR	6.02		ns
		3.3V, SDR	7.52		ns
		1.8V, DDR	6.02		ns
		3.3V, DDR	7.52		ns

#### 7.10.5.14.2 OSPI Without Data Training

##### Note

The I/O Timings provided in this section are only applicable when data training is not implemented. Additionally, the I/O Timings are valid only for some OSPI usage modes when the corresponding DLL Delays are configured as described in Table 7-92.

**Table 7-92. OSPI DLL Delay Mapping for Timing Modes**

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
1.8V, OSPI0 DDR TX	PHY_CONFIG_TX_DLL_DELAY_FLD	0x45
3.3V, OSPI0 DDR TX	PHY_CONFIG_TX_DLL_DELAY_FLD	0x46
1.8V, OSPI0 DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x14
3.3V, OSPI0 DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x3A
All other modes	PHY_CONFIG_TX_DLL_DELAY_FLD, PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

#### 7.10.5.14.2.1 OSPI SDR Timing

Table 7-93, Figure 7-78, Figure 7-79, Table 7-94, and Figure 7-80 present timing requirements and switching characteristics for OSPI SDR Mode.

**Table 7-93. OSPI Timing Requirements – SDR Mode**

see Figure 7-78 and Figure 7-79

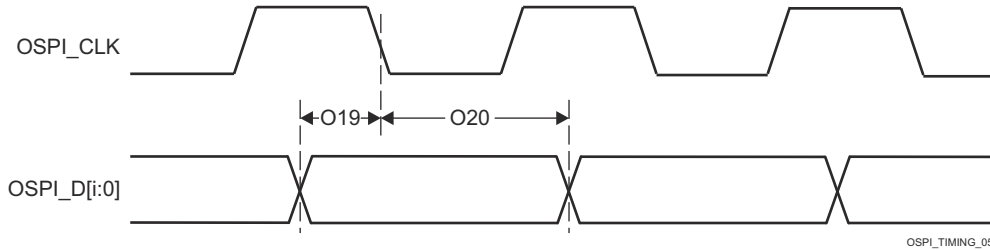
NO. (1)			MODE	MIN	MAX	UNIT
O19	$t_{su}$ (D-CLK)	Setup time, D[i:0] valid before active CLK edge	1.8V, No Loopback	-2.19		ns
			3.3V, No Loopback	-1.71		ns
O20	$t_h$ (CLK-D)	Hold time, D[i:0] valid after active CLK edge	1.8V, No Loopback	7.62		ns
			3.3V, No Loopback	8.1		ns
O21	$t_{su}$ (D-LBCLK)	Setup time, D[i:0] valid before active LBCLK input (DQS) edge	1.8V, External Board Loopback	-3.1		ns
			3.3V, External Board Loopback	-3.47		ns

**Table 7-93. OSPI Timing Requirements – SDR Mode (continued)**

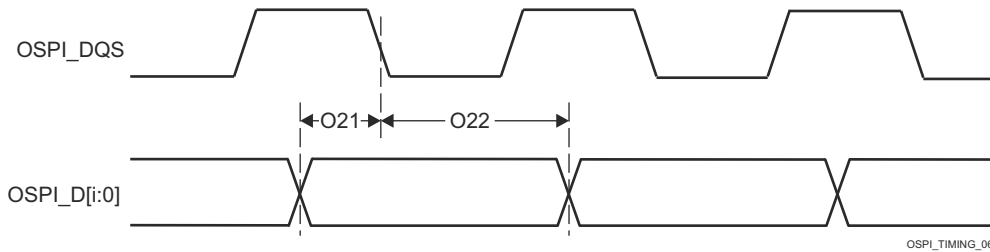
see [Figure 7-78](#) and [Figure 7-79](#)

NO. (1)		MODE	MIN	MAX	UNIT
O22	$t_{h(LBCLK-D)}$	1.8V, External Board Loopback	3.31		ns
		3.3V, External Board Loopback	4.33		ns

(1) i in [i:0] = 7 for OSPI0



**Figure 7-78. OSPI Timing Requirements – SDR, No Loopback Clock and Internal Pad Loopback Clock**



**Figure 7-79. OSPI Timing Requirements – SDR, External Loopback Clock**

**Table 7-94. OSPI Switching Characteristics – SDR Mode**

see [Figure 7-80](#)

NO.(1)	PARAMETER	MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	1.8V	7		ns
		3.3V	6.03		ns
O8	$t_{w(CLKL)}$		0.475P - 0.3 (2)		ns
O9	$t_{w(CLKH)}$		0.475P - 0.3 (2)		ns
O10	$t_{d(CLK-CSn)}$		- 0.475P - 0.975(N)(R) - 1 (2) (3) (4)	- 0.475P - 0.975(N)(R) + 1 (2) (3) (4)	ns
O11	$t_{d(CLK-CSn)}$		0.475P + 0.975(N)(R) - 1 (2) (3) (4)	0.475P + 0.975(N)(R) + 1 (2) (3) (4)	ns
O12	$t_{d(CLK-D)}$	1.8V	-1.16	1.25	ns
		3.3V	-1.33	1.51	ns

(1) i in [i:0] = 7 for OSPI0

(2) P = CLK cycle time = SCLK period in ns

(3) N = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]

(4) R = reflck cycle time in ns

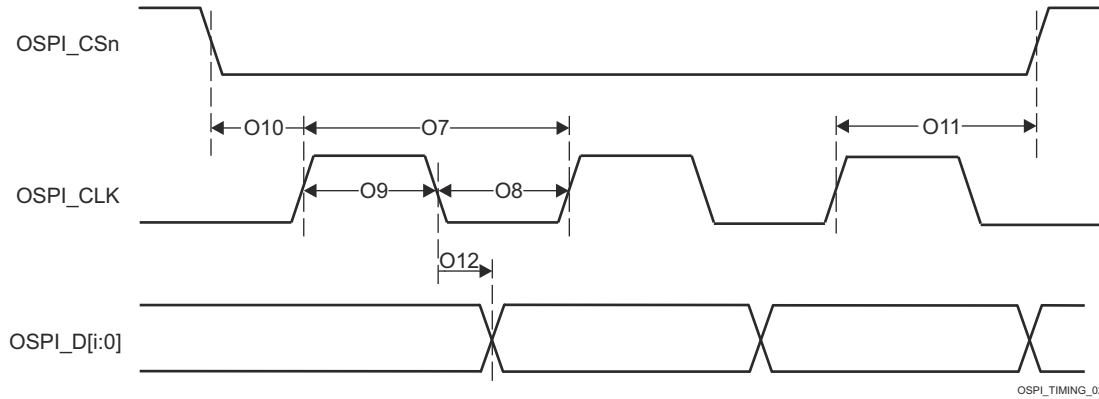


Figure 7-80. OSPI Switching Characteristics – SDR

7.10.5.14.2.2 OSPI DDR Timing

Table 7-95, Figure 7-81, Figure 7-82, Table 7-96, and Figure 7-83 present timing requirements and switching characteristics for OSPI DDR Mode.

Table 7-95. OSPI Timing Requirements – DDR Mode

see Figure 7-81 and Figure 7-82

NO. (1)		MODE	MIN	MAX	UNIT
O13	$t_{su(D-CLK)}$	Setup time, D[i:0] valid before active CLK edge	1.8V, No Loopback or Internal Pad Loopback	5.23	ns
			3.3V, No Loopback or Internal Pad Loopback	5.44	ns
O14	$t_{h(CLK-D)}$	Hold time, D[i:0] valid after active CLK edge	1.8V, No Loopback or Internal Pad Loopback	1.34	ns
			3.3V, No Loopback or Internal Pad Loopback	1.44	ns
O15	$t_{su(D-LBCLK)}$	Setup time, D[i:0] valid before active LBCLK (DQS) edge	1.8V, External Board Loopback	TBD	ns
			3.3V, External Board Loopback	TBD	ns
O16	$t_{h(LBCLK-D)}$	Hold time, D[i:0] valid after active LBCLK (DQS) edge	1.8V, External Board Loopback	TBD (2)	ns
			3.3V, External Board Loopback	TBD (2)	ns
O17	$t_{su(D-DQS)}$	Setup time, D[i:0] valid before active DQS edge	1.8V, DQS	-0.46	ns
			3.3V, DQS	-0.66	ns
O18	$t_{h(DQS-D)}$	Hold time, D[i:0] valid after active DQS edge	1.8V, DQS	3.59	ns
			3.3V, DQS	7.92	ns

(1) i in [i:0] = 7 for OSPI0

(2) This Hold time requirement is larger than the Hold time provided by a typical flash device. Therefore, the trace length between the SoC and flash device must be sufficiently long enough to ensure that the Hold time is met at the SoC. The length of the SoC's external loopback clock (OSPI\_LBCLKO to OSPI\_DQS) may need to be shortened to compensate.

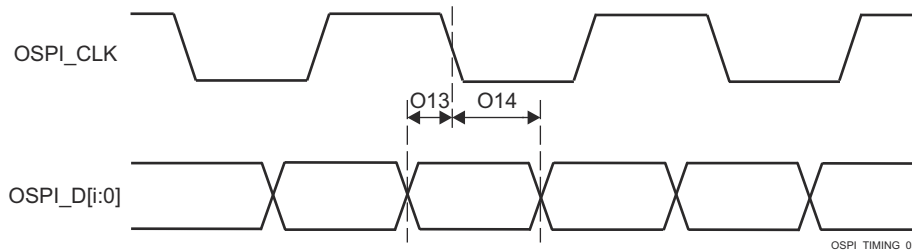
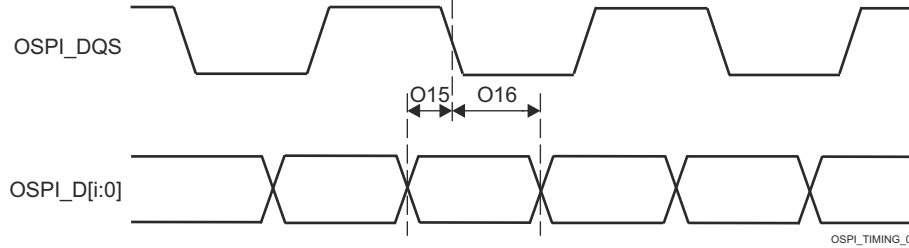


Figure 7-81. OSPI Timing Requirements – DDR, No Loopback Clock and Internal Pad Loopback Clock



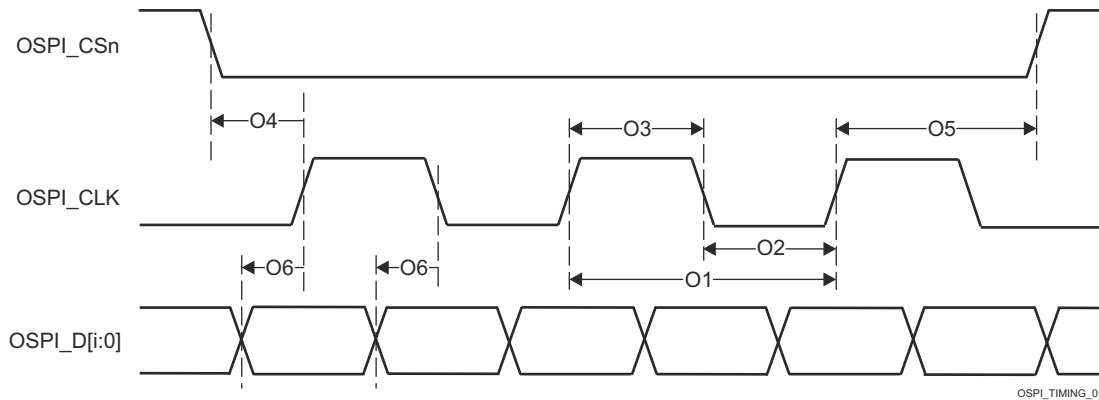
**Figure 7-82. OSPI Timing Requirements – DDR, External Loopback Clock and DQS**

**Table 7-96. OSPI Switching Characteristics – DDR Mode**

see Figure 7-83

NO. <sup>(1)</sup>	PARAMETER	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, CLK	19		ns
O2	$t_{w(CLKL)}$	Pulse duration, CLK low	0.475P - 0.3 (2)		ns
O3	$t_{w(CLKH)}$	Pulse duration, CLK high	0.475P - 0.3 (2)		ns
O4	$t_{d(CLK-CSn)}$	Delay time, CLK rising edge to CSn active edge	-0.475P - 0.975(N)(R) - 7 (2) (3) (4)	-0.475P - 0.975(N)(R) (2) (3) (4)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, CLK rising edge to CSn inactive edge	0.475P + 0.975(N)(R) (2) (3) (4)	0.475P + 0.975(N)(R) (2) (3) (4)	ns
O6	$t_{d(CLK-D)}$	1.8V	-7.71	-1.56	ns
		3.3V	-7.71	-1.56	ns

- (1) i in [i:0] = 7 for OSPI0
- (2) P = CLK cycle time = SCLK period in ns
- (3) N = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD]
- (4) R = refclk cycle time in ns



**Figure 7-83. OSPI Switching Characteristics – DDR**

**7.10.5.15 PCIe**

The PCI-Express Subsystem is compliant with the PCIe® Base Specification, Revision 4.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Peripheral Component Interconnect Express, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

ADVANCE INFORMATION

### 7.10.5.16 PRU\_ICSSG

The device has integrated two identical Programmable Real-Time Unit Subsystem and Industrial Communication Subsystems - Gigabit (PRU\_ICSSG), PRU\_ICSSG0 and PRU\_ICSSG1. The programmable nature of the PRU cores, along with their access to pins, events and all device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores in the device.

For more details about features and additional description information on the device PRU\_ICSSG, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

#### Note

The PRU\_ICSSG0 and PRU\_ICSSG1 support an internal wrapper multiplexing that expands the device top-level multiplexing.

#### 7.10.5.16.1 PRU\_ICSSG Programmable Real-Time Unit (PRU)

#### Note

The PRU\_ICSSG PRU signals have different functionality depending on the mode of operation. The signal naming in this section matches the naming used in the *PRU Module Interface* section in the device TRM.

Table 7-97. PRU\_ICSSG PRU Timing Conditions

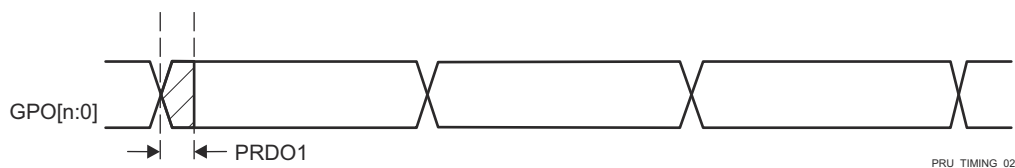
PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>i</sub>	Input slew rate	1	3	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	2	30	pF

#### 7.10.5.16.1.1 PRU\_ICSSG PRU Direct Output Mode Timing

Table 7-98. PRU\_ICSSG PRU Switching Characteristics – Direct Output Mode

see Figure 7-84

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRDO1	t <sub>sk(GPO-GPO)</sub>	Skew, GPO to GPO		3	ns



A. n in GPO[n:0] = 19.

Figure 7-84. PRU\_ICSSG PRU Direct Output Timing

#### 7.10.5.16.1.2 PRU\_ICSSG PRU Parallel Capture Mode Timing

Table 7-99. PRU\_ICSSG PRU Timing Requirements – Parallel Capture Mode

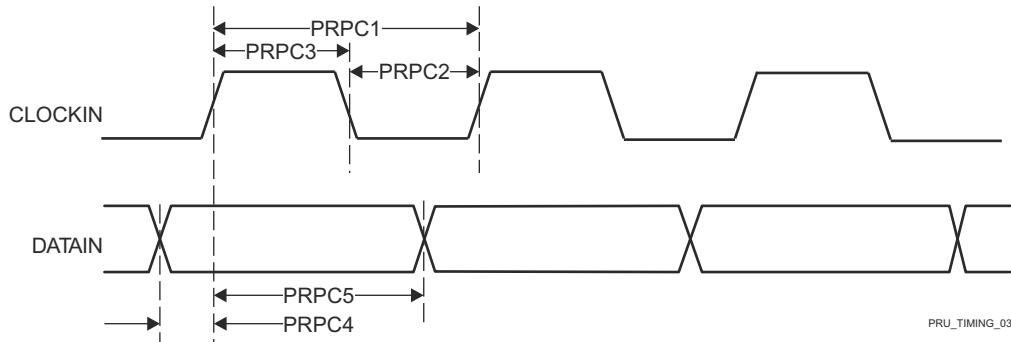
see Figure 7-85 and Figure 7-86

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPC1	t <sub>c(CLOCK)</sub>	Cycle time, CLOCKIN	20		ns
PRPC2	t <sub>w(CLOCKL)</sub>	Pulse duration, CLOCKIN low	10		ns
PRPC3	t <sub>w(CLOCKH)</sub>	Pulse duration, CLOCKIN high	10		ns
PRPC4	t <sub>su(DATAIN-CLOCK)</sub>	Setup time, DATAIN valid before CLOCKIN active edge	4		ns

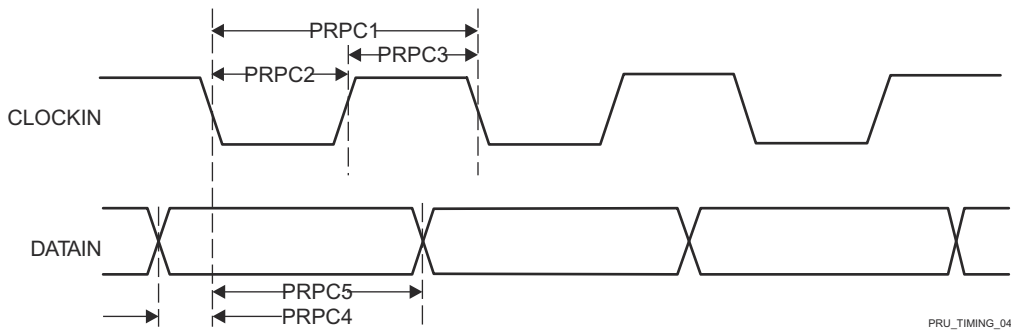
**Table 7-99. PRU\_ICSSG PRU Timing Requirements – Parallel Capture Mode (continued)**

see [Figure 7-85](#) and [Figure 7-86](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPC5	$t_{h(\text{CLOCK-DATAIN})}$	Hold time, DATAIN valid after CLOCKIN active edge	0		ns



**Figure 7-85. PRU\_ICSSG PRU Parallel Capture Timing Requirements – Rising Edge Mode**



**Figure 7-86. PRU\_ICSSG PRU Parallel Capture Timing Requirements – Falling Edge Mode**

ADVANCE INFORMATION

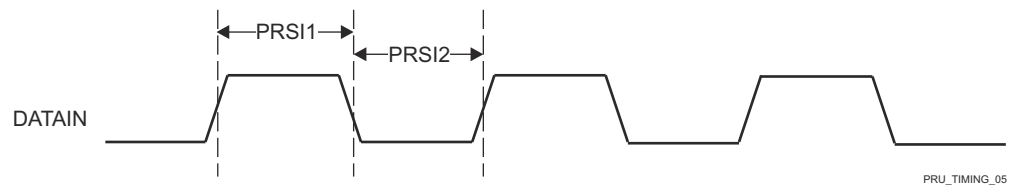
7.10.5.16.1.3 PRU\_ICSSG PRU Shift Mode Timing

**Table 7-100. PRU\_ICSSG PRU Timing Requirements – Shift In Mode**

see [Figure 7-87](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRS11	$t_{w(\text{DATAINH})}$	Pulse duration, DATAIN high	$2+2*P^{(1)}$		ns
PRS12	$t_{w(\text{DATAINL})}$	Pulse duration, DATAIN low	$2+2*P^{(1)}$		ns

(1) P = Internal shift in clock period, defined by PRUn\_GPI\_DIV0 and PRUn\_GPI\_DIV1 bit fields in the ICSSG\_GPCFGn\_REG register. PRUn represents the respective PRU0 or PRU1 instance.



**Figure 7-87. PRU\_ICSSG PRU Shift In Timing**

**Table 7-101. PRU\_ICSSG PRU Switching Characteristics – Shift Out Mode**

see [Figure 7-88](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSO1	$t_{c(\text{CLOCKOUT})}$	Cycle time, CLOCKOUT	10		ns

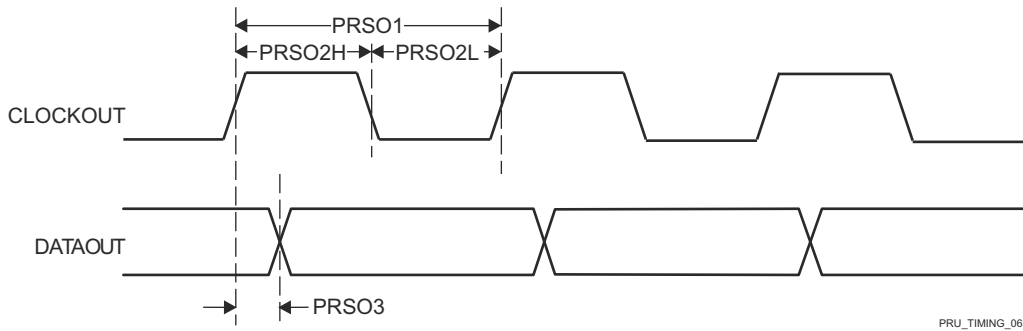


**Table 7-101. PRU\_ICSSG PRU Switching Characteristics – Shift Out Mode (continued)**

see Figure 7-88

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSO2L	$t_{w(\text{CLOCKOUTL})}$	Pulse duration, CLOCKOUT low	-0.3 + $0.475 * P * Z^{(1)(2)}$		ns
PRSO2H	$t_{w(\text{CLOCKOUTH})}$	Pulse duration, CLOCKOUT high	-0.3 + $0.475 * P * Y^{(1)(3)}$		ns
PRSO3	$t_{d(\text{CLOCKOUT-DATAOUT})}$	Delay time, CLOCKOUT to DATAOUT valid	-1	4	ns

- (1) P = Software programmable shift out clock period, defined by PRUn\_GPO\_DIV0 and PRUn\_GPO\_DIV1 bit fields in the ICSSG\_GPCFGn\_REG register, where PRUn represents the respective PRU0 or PRU1 instance.
- (2) The Z parameter is defined as follows, where PRUn represents the respective PRU0 or PRU1 instance.
  - a. If PRUn\_GPI\_DIV0 and PRUn\_GPI\_DIV1 are INTEGERS -or- if PRUn\_GPI\_DIV0 is a NON-INTEGGER and PRUn\_GPI\_DIV1 is an EVEN INTEGER then, Z equals (PRUn\_GPI\_DIV0 \* PRUn\_GPI\_DIV1).
  - b. If PRUn\_GPI\_DIV0 is a NON-INTEGGER and PRUn\_GPI\_DIV1 is an ODD INTEGER then, Z equals (PRUn\_GPI\_DIV0 \* PRUn\_GPI\_DIV1 + 0.5).
  - c. If PRUn\_GPI\_DIV0 is a NON-INTEGGER and PRUn\_GPI\_DIV1 is an ODD INTEGER then, Z equals (PRUn\_GPI\_DIV0 \* PRUn\_GPI\_DIV1 + 0.5).
  - d. If PRUn\_GPI\_DIV0 is an INTEGER and PRUn\_GPI\_DIV1 is a NON-INTEGGER then, Z equals (PRUn\_GPI\_DIV0 \* PRUn\_GPI\_DIV1 + 0.5 \* PRUn\_GPI\_DIV0). If PRUn\_GPI\_DIV0 and PRUn\_GPI\_DIV1 are NON-INTEGERS then, Z equals (PRUn\_GPI\_DIV0 \* PRUn\_GPI\_DIV1 + 0.25 \* PRUn\_GPI\_DIV0).
- (3) The Y parameter is defined as follows, where PRUn represents the respective PRU0 or PRU1 instance.
  - a. If PRUn\_GPI\_DIV0 and PRUn\_GPI\_DIV1 are INTEGERS -or- if PRUn\_GPI\_DIV0 is a NON-INTEGGER and PRUn\_GPI\_DIV1 is an EVEN INTEGER then, Y equals (PRUn\_GPI\_DIV0 \* PRUn\_GPI\_DIV1). If PRUn\_GPI\_DIV0 is a NON-INTEGGER and PRUn\_GPI\_DIV1 is an ODD INTEGER then, Y equals (PRUn\_GPI\_DIV0 \* PRUn\_GPI\_DIV1 - 0.5).
  - b. If PRUn\_GPI\_DIV0 is an INTEGER and PRUn\_GPI\_DIV1 is a NON-INTEGGER then, Y equals (PRUn\_GPI\_DIV0 \* PRUn\_GPI\_DIV1 - 0.5 \* PRUn\_GPI\_DIV0).
  - c. If PRUn\_GPI\_DIV0 and PRUn\_GPI\_DIV1 are NON-INTEGERS then, Y1 equals (PRUn\_GPI\_DIV0 \* PRUn\_GPI\_DIV1 - 0.25 \* PRUn\_GPI\_DIV0) and Y2 equals (PRUn\_GPI\_DIV0 \* PRUn\_GPI\_DIV1 + 0.25 \* PRUn\_GPI\_DIV0), where Y1 is the first high pulse and Y2 is the second high pulse.



**Figure 7-88. PRU\_ICSSG PRU Shift Out Timing**

**7.10.5.16.1.4 PRU\_ICSSG PRU Sigma Delta and Peripheral Interface**

**Table 7-102. PRU\_ICSSG PRU Sigma Delta and Peripheral Interface Timing Conditions**

PARAMETER	MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>			
SR <sub>i</sub> Input slew rate	1	3	V/ns
<b>OUTPUT CONDITIONS</b>			
C <sub>L</sub> Output load capacitance	2	18	pF

7.10.5.16.1.4.1 PRU\_ICSSG PRU Sigma Delta and Peripheral Interface Timing

Table 7-103. PRU\_ICSSG PRU Timing Requirements – Sigma Delta Mode

see Figure 7-89 and Figure 7-90

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSD1	$t_{c(SD\_CLK)}$	Cycle time, SDx_CLK	40		ns
PRSD2L	$t_{w(SD\_CLKL)}$	Pulse duration, SDx_CLK low	20		ns
PRSD2H	$t_{w(SD\_CLKH)}$	Pulse duration, SDx_CLK high	20		ns
PRSD3	$t_{su(SD\_D-SD\_CLK)}$	Setup time, SDx_D valid before SDx_CLK active edge	10		ns
PRSD4	$t_{h(SD\_CLK-SD\_D)}$	Hold time, SDx_D valid before SDx_CLK active edge	5		ns

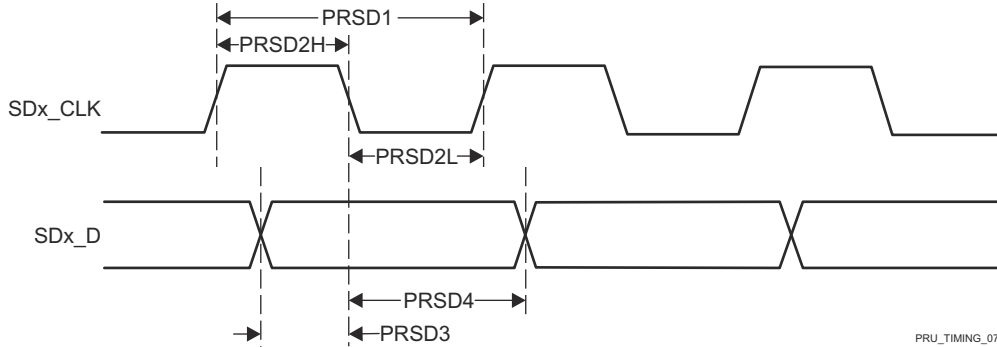


Figure 7-89. PRU\_ICSSG PRU SD\_CLK Falling Active Edge

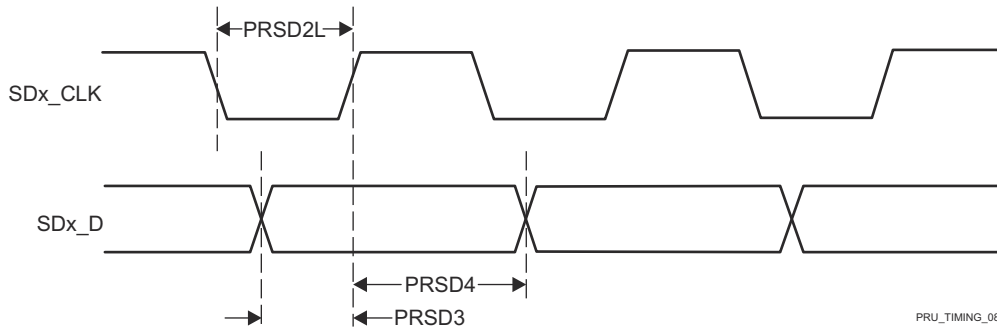


Figure 7-90. PRU\_ICSSG PRU SD\_CLK Rising Active Edge

Table 7-104. PRU\_ICSSG PRU Timing Requirements – Peripheral Interface Mode

see Figure 7-91

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF1	$t_{w(PIF\_DATA\_INH)}$	Pulse duration, PIF_DATA_IN high	$2 + 0.475 \cdot (4 \cdot P)^{(1)}$		ns
PRPIF2	$t_{w(PIF\_DATA\_INL)}$	Pulse duration, PIF_DATA_IN low	$2 + 0.475 \cdot (4 \cdot P)^{(1)}$		ns

(1) P = 1x (or TX) clock period in ns, defined by PRUn\_ED\_TX\_DIV\_FACTOR and PRUn\_ED\_TX\_DIV\_FACTOR\_FRAC in the ICSSG\_PRUn\_ED\_TX\_CFG\_REG register. PRUn represents the respective PRU0 or PRU1 instance.

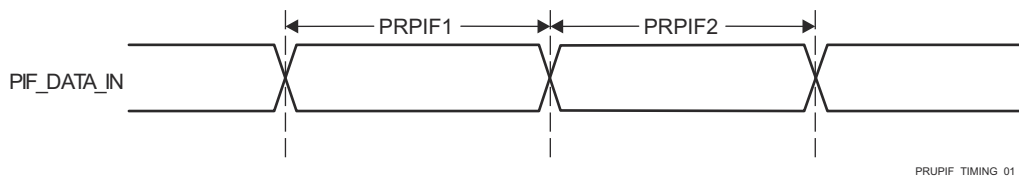


Figure 7-91. PRU\_ICSSG PRU Peripheral Interface Timing Requirements

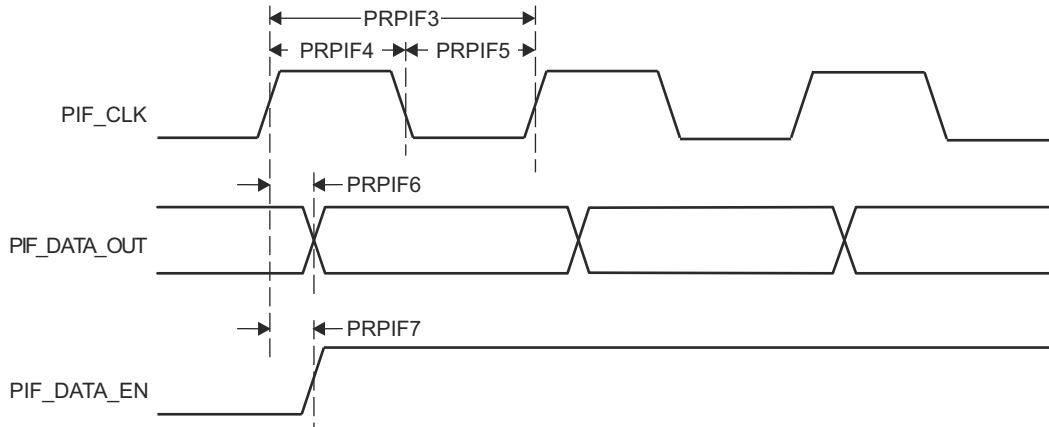
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**Table 7-105. PRU\_ICSSG PRU Switching Characteristics – Peripheral Interface Mode**

see [Figure 7-92](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF3	$t_c(\text{PIF\_CLK})$	Cycle time, PIF_CLK	30		ns
PRPIF4	$t_w(\text{PIF\_CLKH})$	Pulse duration, PIF_CLK high	$0.475 \cdot P^{(1)}$		ns
PRPIF5	$t_w(\text{PIF\_CLKL})$	Pulse duration, PIF_CLK low	$0.475 \cdot P^{(1)}$		ns
PRPIF6	$t_d(\text{PIF\_CLK-PIF\_DATA\_OUT})$	Delay time, PIF_CLK fall to PIF_DATA_OUT	-5	5	ns
PRPIF7	$t_d(\text{PIF\_CLK-PIF\_DATA\_EN})$	Delay time, PIF_CLK fall to PIF_DATA_EN	-5	5	ns

(1)  $P = 1x$  (or TX) clock period in ns, defined by PRUn\_ED\_TX\_DIV\_FACTOR and PRUn\_ED\_TX\_DIV\_FACTOR\_FRAC in the ICSSG\_PRUn\_ED\_TX\_CFG\_REG register. PRUn represents the respective PRU0 or PRU1 instance.



**Figure 7-92. PRU\_ICSSG PRU Peripheral Interface Switching Characteristics**

#### 7.10.5.16.2 PRU\_ICSSG Pulse Width Modulation (PWM)

**Table 7-106. PRU\_ICSSG PWM Timing Conditions**

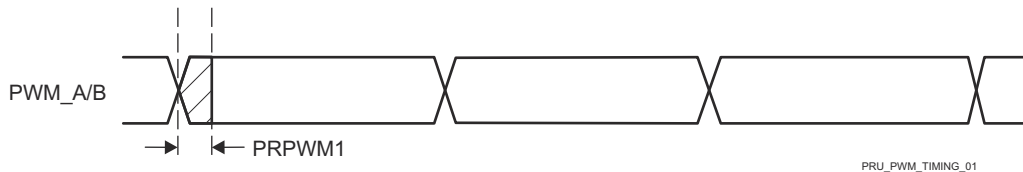
PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
$SR_i$	Input slew rate	1	4	V/ns
<b>OUTPUT CONDITIONS</b>				
$C_L$	Output load capacitance	2	7	pF

#### 7.10.5.16.2.1 PRU\_ICSSG PWM Timing

**Table 7-107. PRU\_ICSSG PWM Switching Characteristics**

see [Figure 7-93](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPWM1	$t_{sk}(\text{PWM\_A-PWM\_B})$	Skew, PWM_A to PWM_B		5	ns



**Figure 7-93. PRU\_ICSSG PWM Timing**

7.10.5.16.3 PRU\_ICSSG Industrial Ethernet Peripheral (IEP)

Table 7-108. PRU\_ICSSG IEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>I</sub>	Input slew rate	1	3	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	2	7	pF

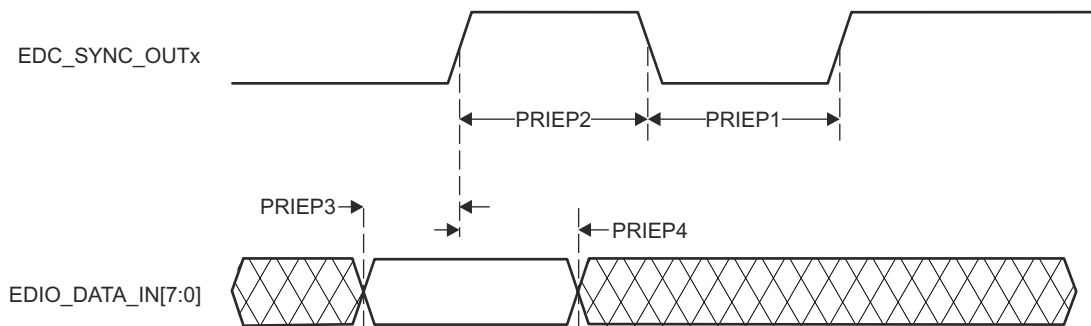
7.10.5.16.3.1 PRU\_ICSSG IEP Timing

Table 7-109. PRU\_ICSSG IEP Timing Requirements – Input Validated with SYNC

see Figure 7-94

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRIEP1	t <sub>w</sub> (EDC_SYNC_OUTxL)	Pulse duration, EDC_SYNC_OUTx low	-2+20*P <sup>(1)</sup>		ns
PRIEP2	t <sub>w</sub> (EDC_SYNC_OUTxH)	Pulse duration, EDC_SYNC_OUTx high	-2+20*P <sup>(1)</sup>		ns
PRIEP3	t <sub>su</sub> (EDIO_DATA_IN-EDC_SYNC_OUTx)	Setup time, EDIO_DATA_IN valid before EDC_SYNC_OUTx active edge	20		ns
PRIEP4	t <sub>h</sub> (EDC_SYNC_OUTx-EDIO_DATA_IN)	Hold time, EDIO_DATA_IN valid after EDC_SYNC_OUTx active edge	20		ns

(1) P = PRU\_ICSSG IEP clock source period in ns.



PRU\_IEP\_TIMING\_01

Figure 7-94. PRU\_ICSSG IEP SYNC Timing Requirements

Table 7-110. PRU\_ICSSG IEP Timing Requirements – Digital IOs

see Figure 7-95

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
IEPIO1	t <sub>w</sub> (EDIO_OUTVALIDL)	Pulse duration, EDIO_OUTVALID low	-2+14*P <sup>(1)</sup>		ns
IEPIO2	t <sub>w</sub> (EDIO_OUTVALIDH)	Pulse duration, EDIO_OUTVALID high	-2+32*P <sup>(1)</sup>		ns
IEPIO3	t <sub>d</sub> (EDIO_OUTVALID-EDIO_DATA_OUT)	Delay time, EDIO_OUTVALID to EDIO_DATA_OUT	0	18*P <sup>(1)</sup>	ns
IEPIO4	t <sub>sk</sub> (EDIO_DATA_OUT)	EDIO_DATA_OUT skew	5		ns

(1) P = PRU\_ICSSG IEP clock source period in ns.



PRU\_EDIO\_DATA\_OUT\_TIMING\_00

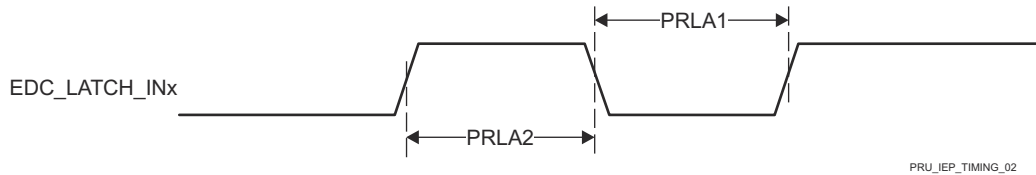
Figure 7-95. PRU\_ICSSG IEP Digital IOs Timing Requirements

**Table 7-111. PRU\_ICSSG IEP Timing Requirements – LATCH\_INx**

see [Figure 7-96](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRLA1	$t_{w(EDC\_LATCH\_INxL)}$	Pulse duration, EDC_LATCH_INx low	$2+3*P^{(1)}$		ns
PRLA2	$t_{w(EDC\_LATCH\_INxH)}$	Pulse duration, EDC_LATCH_INx high	$2+3*P^{(1)}$		ns

(1) P = PRU\_ICSSG IEP clock source period in ns.



**Figure 7-96. PRU\_ICSSG IEP LATCH\_INx Timing Requirements**

#### 7.10.5.16.4 PRU\_ICSSG Universal Asynchronous Receiver Transmitter (UART)

**Table 7-112. PRU\_ICSSG UART Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
$SR_i$	Input slew rate	0.01	0.33	V/ns
<b>OUTPUT CONDITIONS</b>				
$C_L$	Output load capacitance	1	30	pF

##### 7.10.5.16.4.1 PRU\_ICSSG UART Timing

**Table 7-113. PRU\_ICSSG UART Timing Requirements**

see [Figure 7-97](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRUR1H	$t_{w(RXH)}$	Pulse duration, receive start, stop, data bit high	$U^{(1)}$		ns
PRUR1L	$t_{w(RXL)}$	Pulse duration, receive start, stop, data bit low	$-2+U^{(1)}$		ns

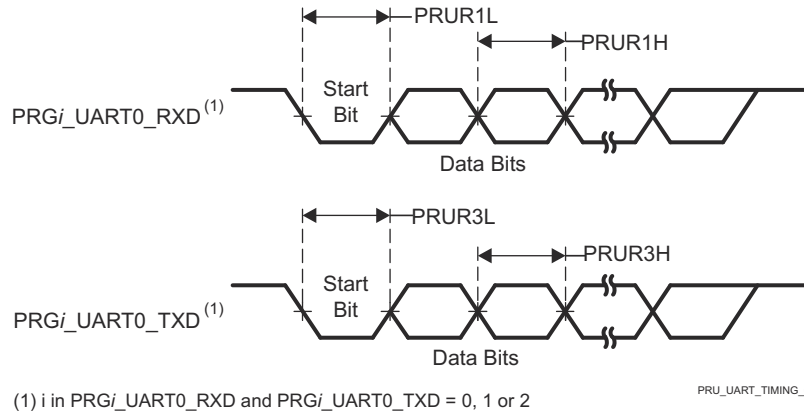
(1) U = UART baud time in ns = 1/programmed baud rate.

**Table 7-114. PRU\_ICSSG UART Switching Characteristics**

see [Figure 7-97](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	f(baud)	Programmed baud rate		12	Mbps
PRUR3H	$t_{w(TXH)}$	Pulse duration, transmit start, stop, data bit high	$U^{(1)}$		ns
PRUR3L	$t_{w(TXL)}$	Pulse duration, transmit start, stop, data bit low	$-2+U^{(1)}$		ns

(1) U = UART baud time in ns = 1/programmed baud rate.



**Figure 7-97. PRU\_ICSSG UART Timing Requirements and Switching Characteristics**

7.10.5.16.5 PRU\_ICSSG Enhanced Capture Peripheral (ECAP)

**Table 7-115. PRU\_ICSSG ECAP Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>i</sub>	Input slew rate	1	3	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	2	7	pF

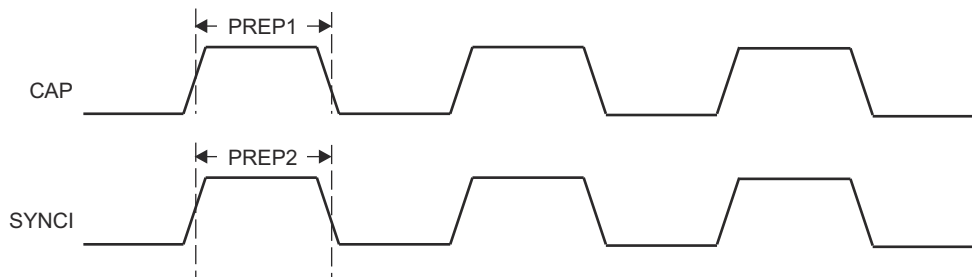
7.10.5.16.5.1 PRU\_ICSSG ECAP Timing

**Table 7-116. PRU\_ICSSG ECAP Timing Requirements**

see [Figure 7-98](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP1	t <sub>w</sub> (CAP)	Pulse Duration, CAP (asynchronous)	2+2*P <sup>(1)</sup>		ns
PREP2	t <sub>w</sub> (SYNCI)	Pulse Duration, SYNCI (asynchronous)	2+2*P <sup>(1)</sup>		ns

(1) P = CORE\_CLK period in ns.



**Figure 7-98. PRU\_ICSSG ECAP Timing**

**Table 7-117. PRU\_ICSSG ECAP Switching Characteristics**

see [Figure 7-99](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP3	t <sub>w</sub> (APWM)	Pulse Duration, APWM high/low	2*P <sup>(1)</sup>		ns
PREP4	t <sub>w</sub> (SYNCO)	Pulse Duration, SYNCO (asynchronous)	P <sup>(1)</sup>		ns

(1) P = CORE\_CLK period in ns.

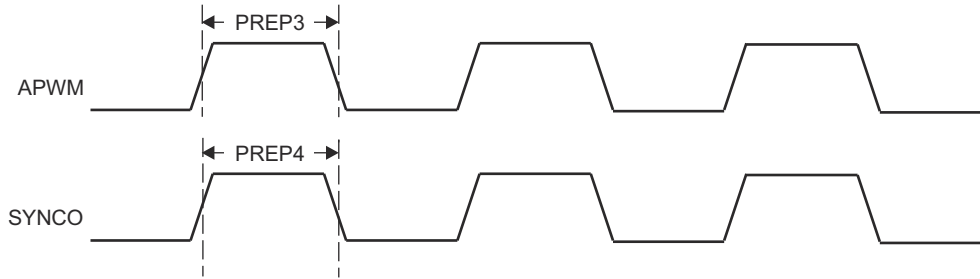


Figure 7-99. PRU\_ICSSG ECAP Switching Characteristics

#### 7.10.5.16.6 PRU\_ICSSG RGMII, MII\_RT, and Switch

For more information, see *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU\_ICSSG)* section in *Processors and Accelerators* chapter in the device TRM.

##### 7.10.5.16.6.1 PRU\_ICSSG MDIO Timing

Table 7-118, Table 7-119, Table 7-120, and Figure 7-100 present timing conditions, requirements, and switching characteristics for PRU\_ICSSG MDIO.

Table 7-118. PRU\_ICSSG MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>i</sub>	Input slew rate	0.9	3.6	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	10	470	pF

Table 7-119. PRU\_ICSSG MDIO Timing Requirements

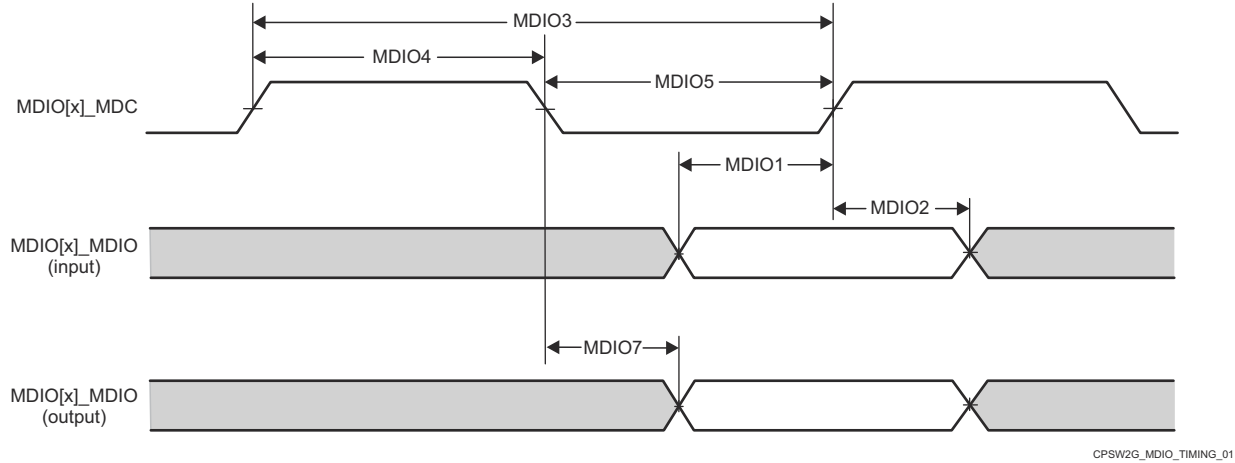
see Figure 7-100

NO.	PARAMETER		MIN	MAX	UNIT
MDIO1	t <sub>su</sub> (MDIO_MDC)	Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high	90		ns
MDIO2	t <sub>h</sub> (MDC_MDIO)	Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high	0		ns

Table 7-120. PRU\_ICSSG MDIO Switching Characteristics

see Figure 7-100

NO.	PARAMETER		MIN	MAX	UNIT
MDIO3	t <sub>c</sub> (MDC)	Cycle time, MDIO[x]_MDC	400		ns
MDIO4	t <sub>w</sub> (MDCH)	Pulse Duration, MDIO[x]_MDC high	160		ns
MDIO5	t <sub>w</sub> (MDCL)	Pulse Duration, MDIO[x]_MDC low	160		ns
MDIO7	t <sub>d</sub> (MDC_MDIO)	Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid	-150	150	ns



**Figure 7-100. PRU\_ICSSG MDIO Timing Requirements and Switching Characteristics**

**7.10.5.16.6.2 PRU\_ICSSG MII Timing**

**Note**

In order to ensure the MII\_G\_RT I/O timing values published in the device data sheet, the PRU\_ICSSG ICSSGn\_CORE\_CLK (where n = 0 to 1) core clock must be configured for 200 MHz, 225 MHz, or 250 MHz and the TX\_CLK\_DELAYn (where n = 0 or 1) bit field in the ICSSG\_TXCFG0/1 register must be set to 0h (default value).

Table 7-121, Table 7-122, Figure 7-101, Table 7-123, Figure 7-102, Table 7-124, Figure 7-103, Table 7-125, and Figure 7-104 present timing conditions, requirements, and switching characteristics for PRU\_ICSSG MII.

**Table 7-121. PRU\_ICSSG MII Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>i</sub>	Input slew rate	0.9	3.6	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	2	20	pF

**Table 7-122. PRU\_ICSSG MII Timing Requirements – MII[x]\_RX\_CLK**

see [Figure 7-101](#)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIR1	t <sub>c</sub> (RX_CLK)	Cycle time, MII[x]_RX_CLK	10 Mbps	399.96	400.04	ns
			100 Mbps	39.996	40.004	ns
PMIR2	t <sub>w</sub> (RX_CLKH)	Pulse Duration, MII[x]_RX_CLK High	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
PMIR3	t <sub>w</sub> (RX_CLKL)	Pulse Duration, MII[x]_RX_CLK Low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns



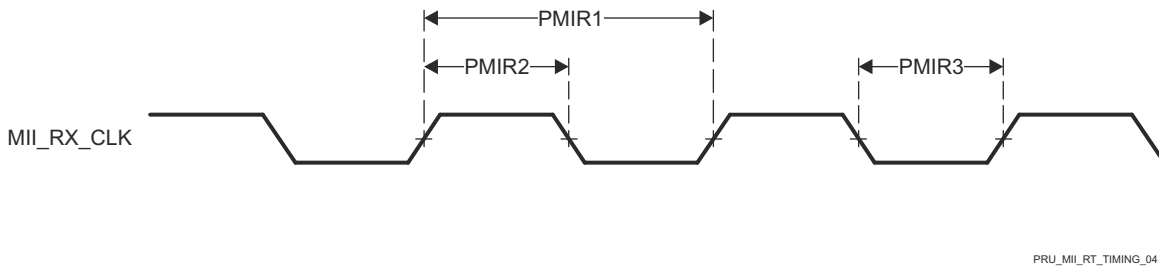


Figure 7-101. PRU\_ICSSG MII[x]\_RX\_CLK Timing

Table 7-123. PRU\_ICSSG MII Timing Requirements – MII[x]\_RXD[3:0], MII[x]\_RX\_DV, and MII[x]\_RX\_ER  
see Figure 7-102

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT	
PMIR4	$t_{su}(RXD-RX\_CLK)$	Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK	10 Mbps	8		ns	
	$t_{su}(RX\_DV-RX\_CLK)$	Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK		8		ns	
	$t_{su}(RX\_ER-RX\_CLK)$	Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK		8		ns	
	PMIR5	$t_{su}(RXD-RX\_CLK)$	Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK	100 Mbps	8		ns
		$t_{su}(RX\_DV-RX\_CLK)$	Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK		8		ns
		$t_{su}(RX\_ER-RX\_CLK)$	Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK		8		ns
PMIR5	$t_h(RX\_CLK-RXD)$	Hold time, MII[x]_RXD[3:0] valid after MII[x]_RX_CLK	10 Mbps	8		ns	
	$t_h(RX\_CLK-RX\_DV)$	Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK		8		ns	
	$t_h(RX\_CLK-RX\_ER)$	Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK		8		ns	
	PMIR5	$t_h(RX\_CLK-RXD)$	Hold time, MII[x]_RXD[3:0] valid after MII[x]_RX_CLK	100 Mbps	8		ns
		$t_h(RX\_CLK-RX\_DV)$	Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK		8		ns
		$t_h(RX\_CLK-RX\_ER)$	Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK		8		ns

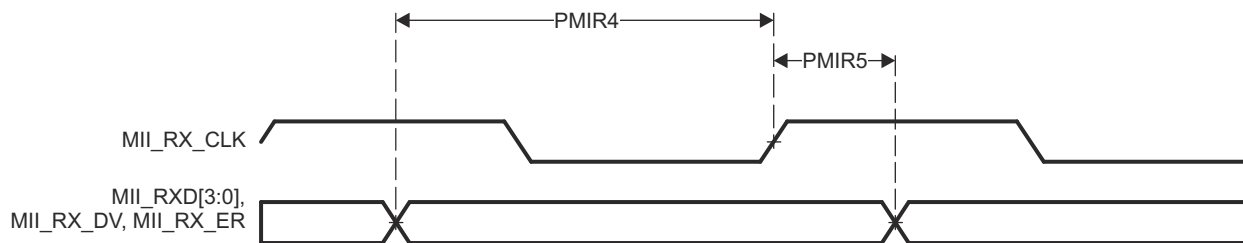


Figure 7-102. PRU\_ICSSG MII[x]\_RXD[3:0], MII[x]\_RX\_DV, and MII[x]\_RX\_ER Timing

Table 7-124. PRU\_ICSSG MII Timing Requirements – MII[x]\_TX\_CLK

see Figure 7-103

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIT1	$t_c(TX\_CLK)$	Cycle time, MII[x]_TX_CLK	10 Mbps	399.96	400.04	ns
			100 Mbps	39.996	40.004	ns
PMIT2	$t_w(TX\_CLKH)$	Pulse Duration, MII[x]_TX_CLK High	10 Mbps	140	260	ns
			100 Mbps	14	26	ns
PMIT3	$t_w(TX\_CLKL)$	Pulse Duration, MII[x]_TX_CLK Low	10 Mbps	140	260	ns
			100 Mbps	14	26	ns

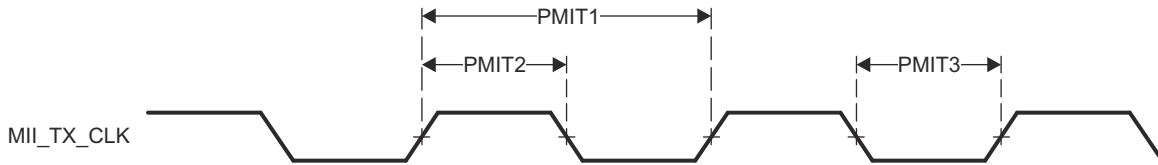


Figure 7-103. PRU\_ICSSG MII[x]\_TX\_CLK Timing

Table 7-125. PRU\_ICSSG MII Switching Characteristics – MII[x]\_TXD[3:0] and MII[x]\_TX\_EN

see Figure 7-104

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIT4	$t_{d(TX\_CLK-TXD)}$	Delay time, MII[x]_TX_CLK High to MII[x]_TXD[3:0] valid	10 Mbps	0	25	ns
	$t_{d(TX\_CLK-TX\_EN)}$	Delay time, MII[x]_TX_CLK to MII[x]_TX_EN valid		0	25	ns
	$t_{d(TX\_CLK-TXD)}$	Delay time, MII[x]_TX_CLK High to MII[x]_TXD[3:0] valid	100 Mbps	0	25	ns
	$t_{d(TX\_CLK-TX\_EN)}$	Delay time, MII[x]_TX_CLK to MII[x]_TX_EN valid		0	25	ns

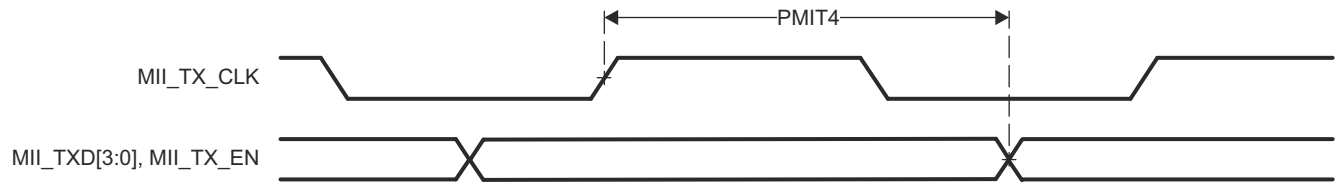


Figure 7-104. PRU\_ICSSG MII[x]\_TXD[3:0], MII[x]\_TX\_EN Timing

7.10.5.16.6.3 PRU\_ICSSG RGMII Timing

Table 7-126, Table 7-127, Table 7-128, Figure 7-105, Table 7-129, Table 7-130, and Figure 7-106 present timing conditions, requirements, and switching characteristics for PRU\_ICSSG RGMII.

Table 7-126. PRU\_ICSSG RGMII Timing Conditions

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>i</sub>	Input slew rate	2.65	5	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	2	20	pF

Table 7-127. PRU\_ICSSG RGMII Timing Requirements – RGMII[x]\_RXC

see Figure 7-105

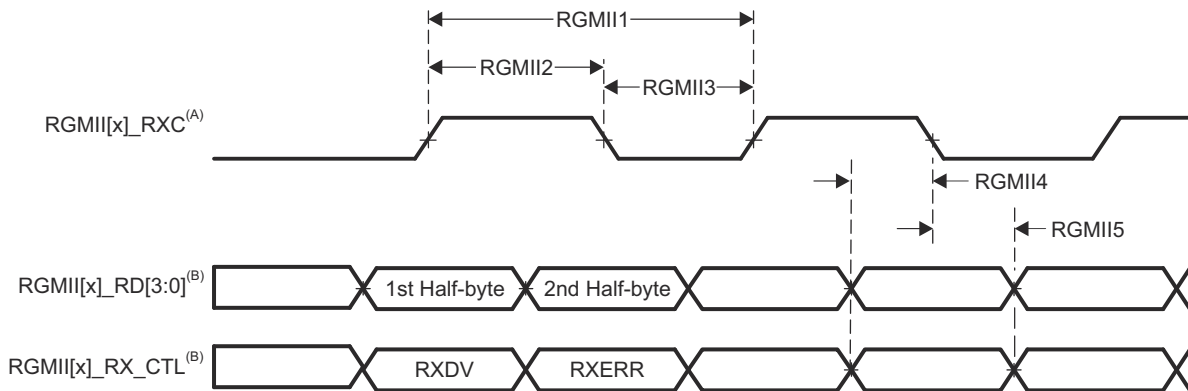
NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, RGMII[x]_RXC	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
RGMII2	$t_{w(RXCH)}$	Pulse duration, RGMII[x]_RXC high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
RGMII3	$t_{w(RXCL)}$	Pulse duration, RGMII[x]_RXC low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns

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**Table 7-128. PRU\_ICSSG RGMII Timing Requirements – RGMII[x]\_RD[3:0] and RGMII[x]\_RX\_CTL**

see [Figure 7-105](#)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII4	$t_{su}(RD-RXC)$	Setup time, RGMII[x]_RD[3:0] valid before RXC high/low	10 Mbps	1		ns
			100 Mbps	1		ns
			1000 Mbps	1		ns
	$t_{su}(RX\_CTL-RXC)$	Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC high/low	10 Mbps	1		ns
			100 Mbps	1		ns
			1000 Mbps	1		ns
RGMII5	$t_h(RXC-RD)$	Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC high/low	10 Mbps	1		ns
			100 Mbps	1		ns
			1000 Mbps	1		ns
	$t_h(RXC-RX\_CTL)$	Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC high/low	10 Mbps	1		ns
			100 Mbps	1		ns
			1000 Mbps	1		ns



- A. RGMII[x]\_RXC must be externally delayed relative to the data and control pins.
- B. Data and control information is received using both edges of the clocks. RGMII[x]\_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]\_RXC and data bits 7-4 on the falling edge of RGMII[x]\_RXC. Similarly, RGMII[x]\_RX\_CTL carries RXDV on rising edge of RGMII[x]\_RXC and RXERR on falling edge of RGMII[x]\_RXC.

**Figure 7-105. PRU\_ICSSG RGMII[x]\_RXC, RGMII[x]\_RD[3:0], RGMII[x]\_RX\_CTL Timing Requirements - RGMII Mode**

**Table 7-129. PRU\_ICSSG RGMII Switching Characteristics – RGMII[x]\_TXC**

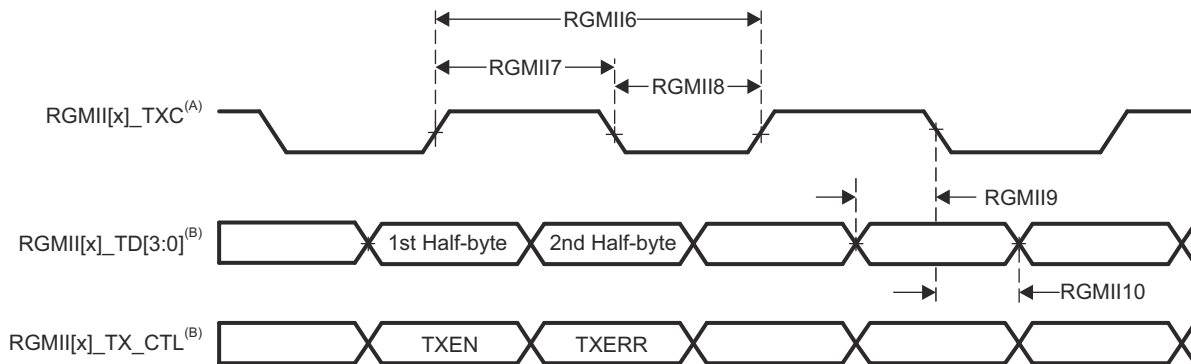
see [Figure 7-106](#)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII6	$t_c(TXC)$	Cycle time, RGMII[x]_TXC	10 Mbps	360	440	ns
			100 Mbps	36	44	ns
			1000 Mbps	7.2	8.8	ns
RGMII7	$t_w(TXCH)$	Pulse duration, RGMII[x]_TXC high	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns
RGMII8	$t_w(TXCL)$	Pulse duration, RGMII[x]_TXC low	10 Mbps	160	240	ns
			100 Mbps	16	24	ns
			1000 Mbps	3.6	4.4	ns

**Table 7-130. PRU\_ICSSG RGMII Switching Characteristics – RGMII[x]\_TD[3:0] and RGMII[x]\_TX\_CTL**

see Figure 7-106

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(TD-TXC)}$	Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low	10 Mbps	1.2		ns
			100 Mbps	1.2		ns
			1000 Mbps	1.2		ns
	$t_{osu(TX_CTL-TXC)}$	Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low	10 Mbps	1.2		ns
			100 Mbps	1.2		ns
			1000 Mbps	1.2		ns
RGMII10	$t_{oh(TXC-TD)}$	Output setup time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low	10 Mbps	1.2		ns
			100 Mbps	1.2		ns
			1000 Mbps	1.2		ns
	$t_{oh(TXC-TX_CTL)}$	Output setup time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low	10 Mbps	1.2		ns
			100 Mbps	1.2		ns
			1000 Mbps	1.2		ns



- A. TxC is delayed internally before being driven to the RGMII[x]\_TxC pin. This internal delay is always enabled.
- B. Data and control information is received using both edges of the clocks. RGMII[x]\_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]\_TxC and data bits 7-4 on the falling edge of RGMII[x]\_TxC. Similarly, RGMII[x]\_TX\_CTL carries TXEN on rising edge of RGMII[x]\_TxC and TXERR on falling edge of RGMII[x]\_TxC.

**Figure 7-106. PRU\_ICSSG RGMII[x]\_TxC, RGMII[x]\_TD[3:0], and RGMII[x]\_TX\_CTL Switching Characteristics - RGMII Mode**

**7.10.5.17 Timers**

For more details about features and additional description information on the device Timers, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

**Table 7-131. Timer Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
SR <sub>i</sub>	Input slew rate	0.5	5	V/ns
<b>OUTPUT CONDITIONS</b>				
C <sub>L</sub>	Output load capacitance	2	10	pF

**Table 7-132. Timer Input Timing Requirements**

see Figure 7-107

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T1	$t_{w(TINPH)}$	Pulse duration, high	CAPTURE	$2 + 4P^{(1)}$		ns

**Table 7-132. Timer Input Timing Requirements (continued)**

see [Figure 7-107](#)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T2	$t_{w(TINPL)}$	Pulse duration, low	CAPTURE	$2 + 4P^{(1)}$		ns

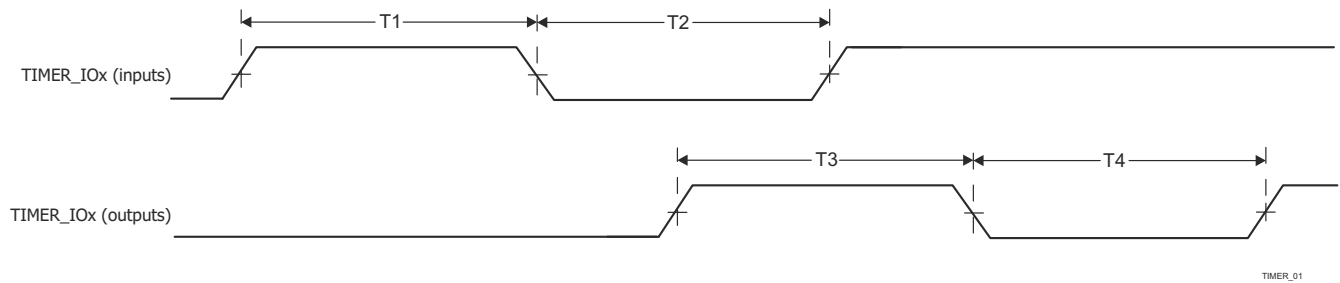
(1) P = functional clock period in ns.

**Table 7-133. Timer Output Switching Characteristics**

see [Figure 7-107](#)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T3	$t_{w(TOUTH)}$	Pulse duration, high	PWM	$-2 + 4P^{(1)}$		ns
T4	$t_{w(TOURL)}$	Pulse duration, low	PWM	$-2 + 4P^{(1)}$		ns

(1) P = functional clock period in ns.



**Figure 7-107. Timer Timing Requirements and Switching Characteristics**

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

### 7.10.5.18 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

**Table 7-134. UART Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
$SR_I$	Input slew rate	0.5	5	V/ns
<b>OUTPUT CONDITIONS</b>				
$C_L$	Output load capacitance	1	30	pF

**Table 7-135. UART Timing Requirements**

see [Figure 7-108](#)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
4	$t_{w(RX)}$	Pulse width, receive data bit, high or low	$0.95U^{(1)}$	$1.05U^{(1)}$	ns
5	$t_{w(CTS)}$	Pulse width, receive start bit, high or low	$0.95U^{(1)}$		ns

(1) U = UART baud time in ns = 1/programmed baud rate.

**Table 7-136. UART Switching Characteristics**

see [Figure 7-108](#)

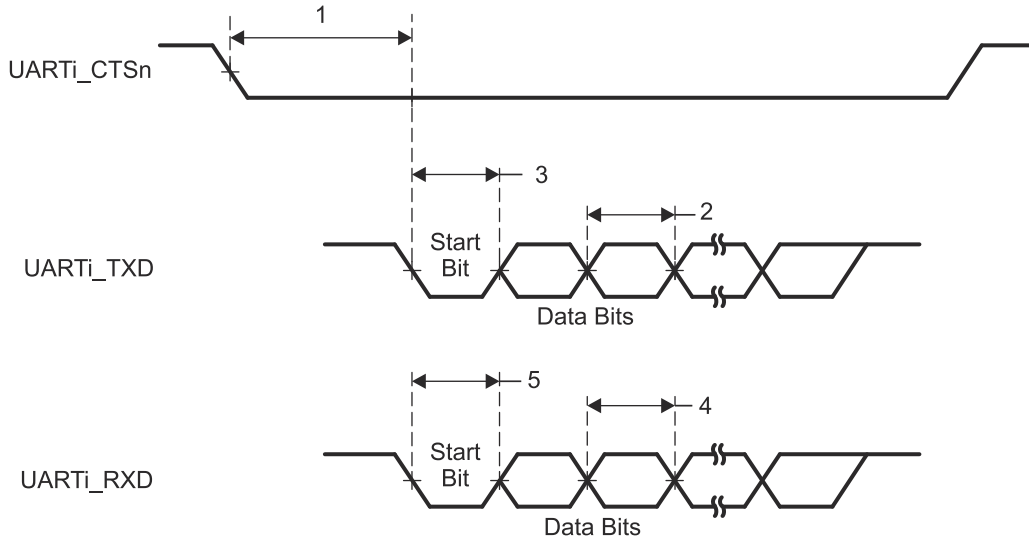
NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
	$f_{(baud)}$	Programmable baud rate	15 pF		TDB	Mbps
			30 pF		0.115	Mbps
1	$t_{d(CTS-TX)}$	Delay time, CTS bit to transmit data		30		ns
2	$t_{w(TX)}$	Pulse width, transmit data bit, high or low		$U - 2.2^{(1)}$	$U + 2.2^{(1)}$	ns

**Table 7-136. UART Switching Characteristics (continued)**

see [Figure 7-108](#)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
3	$t_{w(RTS)}$	Pulse width, transmit start bit, high or low		U - 2.2 <sup>(1)</sup>		ns

(1) U = UART baud time in ns = 1/programmed baud rate.



**Figure 7-108. UART Timing Requirements and Switching Characteristics**

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

**7.10.5.19 USB**

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

The USB 3.1 GEN1 subsystem is compliant with the Universal Serial Bus (USB) 3.1 Specification, revision 1.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

**7.10.6 Emulation and Debug**

For more details about features and additional description information on the device Trace and JTAG interfaces, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

**7.10.6.1 Trace**

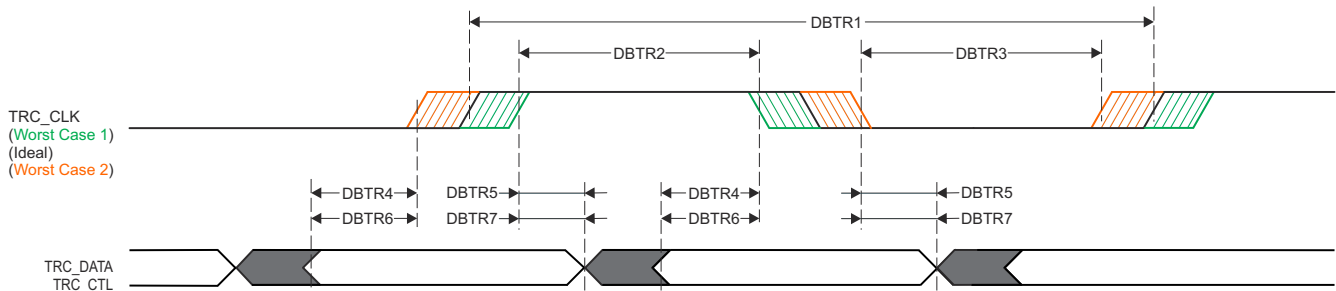
**Table 7-137. Trace Timing Conditions**

PARAMETER		MIN	MAX	UNIT
<b>OUTPUT CONDITIONS</b>				
$C_L$	Output load capacitance	2	5	pF
<b>PCB CONNECTIVITY REQUIREMENTS</b>				
$t_d(\text{Trace Mismatch})$	Propagation delay mismatch across all traces	VDDSHV3 = 1.8V	200	ps
		VDDSHV3 = 3.3V	100	ps

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Table 7-138. Trace Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
<b>1.8V Mode</b>					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	6.50		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	2.50		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	2.50		ns
DBTR4	$t_{osu(TRC\_DATAV-TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	0.81		ns
DBTR5	$t_{oh(TRC\_CLK-TRC\_DATA)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	0.81		ns
DBTR6	$t_{osu(TRC\_CTLV-TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	0.81		ns
DBTR7	$t_{oh(TRC\_CLK-TRC\_CTL)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	0.81		ns
<b>3.3V Mode</b>					
DBTR1	$t_{c(TRC\_CLK)}$	Cycle time, TRC_CLK	8.67		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	3.58		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	3.58		ns
DBTR4	$t_{osu(TRC\_DATAV-TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	1.08		ns
DBTR5	$t_{oh(TRC\_CLK-TRC\_DATA)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	1.08		ns
DBTR6	$t_{osu(TRC\_CTLV-TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	1.08		ns
DBTR7	$t_{oh(TRC\_CLK-TRC\_CTL)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	1.08		ns



SPRSP08\_Debug\_01

Figure 7-109. Trace Switching Characteristics

7.10.6.2 JTAG

Table 7-139. JTAG Timing Conditions

PARAMETER		MIN	MAX	UNIT
<b>INPUT CONDITIONS</b>				
$SR_i$	Input slew rate	0.5	2.0	V/ns
<b>OUTPUT CONDITIONS</b>				
$C_L$	Output load capacitance	5	15	pF

Table 7-140. JTAG Timing Requirements

see Figure 7-110

NO.	PARAMETER		MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time minimum, TCK	45.5		ns
J2	$t_{w(TCKH)}$	Pulse width minimum, TCK high	18.2		ns
J3	$t_{w(TCKL)}$	Pulse width minimum, TCK low	18.2		ns
J4	$t_{su(TDI-TCK)}$	Input setup time minimum, TDI valid to TCK high	4		ns
	$t_{su(TMS-TCK)}$	Input setup time minimum, TMS valid to TCK high	4		ns

**Table 7-140. JTAG Timing Requirements (continued)**

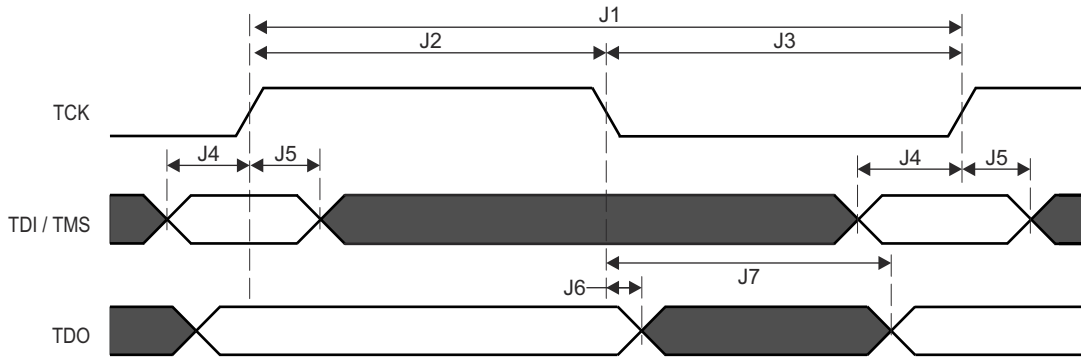
see [Figure 7-110](#)

NO.		MIN	MAX	UNIT
J5	$t_{h(TCK-TDI)}$	Input hold time minimum, TDI valid from TCK high		ns
	$t_{h(TCK-TMS)}$	Input hold time minimum, TMS valid from TCK high		ns

**Table 7-141. JTAG Switching Characteristics**

see [Figure 7-110](#)

NO.	PARAMETER		MIN	MAX	UNIT
J6	$t_{d(TCKL-TDOI)}$	Delay time minimum, TCK low to TDO invalid	0		ns
J7	$t_{d(TCKL-TDOV)}$	Delay time maximum, TCK low to TDO valid		14	ns



**Figure 7-110. JTAG Timing Requirements and Switching Characteristics**

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## 8 Detailed Description

### 8.1 Overview

AM243x is an extension of the Sitara's industrial-grade family of heterogeneous Arm processors. AM243x is built for industrial applications, such as motor drives and programmable logic controllers (PLCs), which require a unique combination of real-time processing and communications with applications processing. AM243x combines two instances of Sitara's gigabit TSN-enabled PRU-ICSSG, up to four Cortex-R5F MCUs and a Cortex-M4F MCU.

AM243x is architected to provide real-time performance through the high-performance R5Fs, Tightly-Coupled Memory banks, configurable SRAM partitioning, and low-latency paths to and from peripherals for rapid data movement in and out of the SoC. This deterministic architecture allows for AM243x to handle the tight control loops found in servo drives, while the peripherals like FSI, GPMC, PWMs, sigma delta decimation filters, and absolute encoder interfaces help enable a number of different architectures found in these systems.

The PRU-ICSSG in AM243x provides the flexible industrial communications capability necessary to run gigabit TSN, EtherCAT, PROFINET, EtherNet/IP, and various other protocols. In addition, the PRU-ICSSG also enables additional interfaces in the SoC including sigma delta decimation filters and absolute encoder interfaces.

Functional safety features can be enabled through the integrated Cortex-M4F along with its dedicated peripherals which can all be isolated from the rest of the SoC. AM243x also supports secure boot.

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#### Note

For more information on features, subsystems, and architecture of superset device System on Chip (SoC), see the device TRM.

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## 8.2 Processor Subsystems

### 8.2.1 Arm Cortex-R5F Subsystem (R5FSS)

The R5FSSSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for dual/single-core operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC.

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#### Note

The Cortex®-R5F processor is a Cortex-R5 processor that includes the optional Floating Point Unit (FPU) extension.

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For more information, see *Dual-R5F Subsystem (R5FSS)* section in *Processors and Accelerators* chapter in the device TRM.

### 8.2.2 Arm Cortex-M4F (M4FSS)

The M4FSS module on the AM243x device provides a safety channel (secondary channel - working in conjunction with an external microcontroller)- or- a general purpose MCU.

The M4FSS module supports the following features:

- Cortex M4F With MPU
- ARMv7-M architecture
- Support for Nested Vectored Interrupt Controller (NVIC) with 64 inputs
- Ability to executed code from internal or external memories
- 192 KB of SRAM (I-Code)
- 64 KB of SRAM (D-Code)
- External access to internal memories if allowed
- Debug Support Including:
  - DAP based Debug to the CPU Core
  - Full Debug Features of CPU Core are enabled
  - Standard ITM trace
  - CTM Cross Trigger
  - ETM Trace Support
- Fault Detection and Correction
  - SECEDED ECC protection on I-CODE
  - SECEDED ECC protection on D-CODE
  - Fault Error Interrupt Output

For more information, see *Arm Cortex M4F Subsystem (M4FSS)* section in *Processors and Accelerators* chapter in the device TRM.

## 8.3 Accelerators and Coprocessors

### 8.3.1 Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU\_ICSSG)

The PRU\_ICSSG module supports the following main features:

- 3x PRUs
  - General-Purpose PRU (PRU)
  - Real-Time PRU(RTU\_PRU)
  - Transmit PRU (TX\_PRU)
- 2x Ethernet MII\_G\_RT configurable connection to PRUs
  - Up to 2x RGMII ports
  - Up to 2x MII ports
  - RX Classifier
- 2x Industrial Ethernet Peripheral (IEP) to manage and generate industrial Ethernet functions
- 2x Industrial Ethernet 64-bit timers, each with 10 capture and 16 compare events, along with slow and fast compensation.
- 1x MDIO
- 1x UART, with a dedicated 192-MHz clock input
- Supports up to 4 sets of 3-phased motor control, with 12 primary and 12 complimentary programmable PWM outputs.
- Supports up to 9 safety events with optional external trip I/O per PWM set with hardware glitch filter.
- 1x Enhanced Capture Module (ECAP)
- 1x Interrupt Controller (INTC)
  - 160 input events supported – 96 external, 64 internal
- Flexible power management support
- Integrated switched central resource with programmable priority
- All memories support ECC

For more information, see *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU\_ICSSG)* section in *Processors and Accelerators* chapter in the device TRM.

## 8.4 Other Subsystems

### 8.4.1 PDMA Controller

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers accessed via a standard non-coherent bus fabric. The PDMA module is intended to be located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured Transfer Request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer UDMA-P destination channel which then performs the movement of the data into memory. Likewise, a remote UDMA-P source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (UDMA-P + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

There are five PDMA modules in the device.

For more information, see *PDMA Controller* section in *DMA Controllers* chapter in the device TRM.

## 8.4.2 Peripherals

### 8.4.2.1 ADC

The analog-to-digital converter (ADC) module is an eight-channel general purpose analog-to-digital converter, which supports 12-bit conversion samples from an analog front end (AFE).

There is one ADC module in the device.

For more information, see *Analog-to-Digital Converter (ADC)* section in *Peripherals* chapter in the device TRM.

### 8.4.2.2 DCC

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programmed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

The device has seven instances of DCC modules.

For more information, see *Dual Clock Comparator (DCC)* section in *Peripherals* chapter in the device TRM.

### 8.4.2.3 Dual Data Rate (DDR) External Memory Interface (DDRSS)

Integrated in MAIN domain: one instance of DDR Subsystem (DDRSS) is used as an interface to external RAM devices which can be utilized for storing program or data. DDRSS provides the following main features:

- Support of DDR4 / LPDDR4 memory types
- 16-bit memory bus interface with in-line ECC
- Up to 2 GB memory address range
- System bus interface: little endian only with 128-bit data width
- Configuration bus Interface: little endian only with 32-bit data width
- Support of dual rank configuration
- Support of automatic idle power saving mode when no or low activity is detected
- Class of Service (CoS) - three latency classes supported
- Prioritized refresh scheduling
- Statistical counters for performance management

For more information, see *DDR Subsystem (DDRSS)* section in *Peripherals* chapter in the device TRM.

### 8.4.2.4 ECAP

This section describes the Enhanced Capture (ECAP) module for the device.

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

### 8.4.2.5 EPWM

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In the further description the letter x within a signal or module name is used to indicate a generic EPWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the EPWM\_x instance. Thus, EPWM1A and EPWM1B belong to EPWM1, EPWM2A and EPWM2B belong to EPWM2, and so forth.

Additionally, the EPWM integration allows this synchronization scheme to be extended to the capture peripheral modules (ECAP). The number of modules is device-dependent and based on target application needs. Modules can also operate stand-alone.

The device has six instances of EPWM modules.

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

#### **8.4.2.6 ELM**

The Error Location Module (ELM) is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

The General-Purpose Memory Controller (GPMC) probes data read from an external NAND flash and uses this to compute checksum-like information, called syndrome polynomials, on a per-block basis. Each syndrome polynomial gives a status of the read operations for a full block, including 512 bytes of data, parity bits, and an optional spare-area data field, with a maximum block size of 1023 bytes. Computation is based on a Bose-Chaudhuri-Hocquenghem (BCH) algorithm. The ELM extracts error addresses from these syndrome polynomials.

For more information, see *Error Location Module (ELM)* section in *Peripherals* chapter in the device TRM.

#### **8.4.2.7 ESM**

The Error Signaling Module (ESM) aggregates safety-related events and/or errors from throughout the device into one location. It can signal both low and high priority interrupts to a processor to deal with a safety event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore an external controller is able to reset the device or keep the system in safe, known state.

For more information, see *Error Signaling Module (ESM)* section in *Peripherals* chapter in the device TRM.

#### **8.4.2.8 GPIO**

The general-purpose input/output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

#### **8.4.2.9 EQEP**

The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 degrees out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vice versa.

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel may be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 KHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

#### 8.4.2.10 GPMC

The GPMC module supports the following features:

- Data path to external memory device can be 32, 16 or 8 bits wide
- Support for the following memory types:
  - Asynchronous or synchronous 8-bit memory or device (non-burst device)
  - Asynchronous or synchronous 16-bit memory or device
  - Asynchronous or synchronous 32-bit memory or device
  - 16-bit non-multiplexed NOR Flash device
  - 16-bit address and 32-bit address and data multiplexed NOR Flash device
  - 8-bit and 16-bit NAND flash device
  - 16-bit and 32bit pSRAM device
- Supports Error Code detection using BCH code (t=4, 8 or 16) or Hamming code for 8-bit or 16-bit NAND-flash, organized with page size of 512 Byte, 1Kbytes, or more. • Supports 1 GByte maximum addressing capability, which can be divided into 8 independent chip-select with programmable bank size and base address on 16 MByte, 32 MByte, 64 MByte, or 128 MByte boundary.
- Fully-pipelined operation for optimal memory bandwidth usage
- Supports external device clock frequency of /1, /2, /3, and /4 divide of interface clock
- Supports programmable auto-clock gating when there is no access
- Supports Mdlereq/SidleAck protocol
- Supports the following interface protocols when communicating with external memory or external devices:
  - Asynchronous read/write access
  - Asynchronous read page access (4-8-16 Word16), 4-8-16 Word32
  - Synchronous read/write access
  - Synchronous read burst access without wrap capability (4-8-16-32 Word16, 4-8-16 Word32)
  - Synchronous read burst access with wrap capability (4-8-16-32 Word16, 4-8-16 Word32)
- Address and data multiplexed access
- Each chip-select has independent and programmable control signal timing parameters for Setup and Hold time. Parameters are set according to the memory device timing parameters, with one interface clock cycle timing granularity.
- Flexible internal access time control (wait state) and flexible handshake mode using external WAIT pin
- Supports bus keeping
- Supports bus turn around
- Pre-fetch and write posting engine associated with system DMA, to get full performance from NAND device, and with minimum impact on NOR/SRAM concurrent access monitoring (up to 4 WAIT pins)

For more information, see *General-Purpose Memory Controller (GPMC)* section in *Peripherals* chapter in the device TRM.

#### 8.4.2.11 I2C

The Inter-IC Bus (I2C) interface is implemented using the mshsi2c module. This peripheral implements the multi-master I2C bus, which allows serial transfer of 8-bit data to and from other I2C master and slave devices, through a two-wire interface.

The I2C module supports the following main features:

- Compliant with Philips I2C specification version 2.1



- Supports standard mode (up to 100K bits/s), fast mode (up to 400K bits/s), and high-speed mode (up to 3.4Mb/s).
- Multi-master transmitter and slave receiver mode
- Multi-master receiver and slave transmitter mode
- Combined master transmit/receive and receive/transmit modes
- 7-bit and 10-bit device addressing modes
- Built-in FIFO for buffered read or write
  - Parameterizable size of 8 to 64 bytes
- Programmable multi-slave channel (responds to 4 separate addresses)
- Programmable clock generation
- Support for asynchronous wake-up
- One interrupt line

For more information, see *Inter-Integrated Circuit (I2C) Interface* section in *Peripherals* chapter in the device TRM.

#### **8.4.2.12 MCAN**

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a high level of security. CAN has high immunity to electrical interference and the ability to self-diagnose and repair data errors. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

The device supports 2 MCAN modules

For more information, see *Modular Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

#### **8.4.2.13 MCRC Controller**

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a pre-determined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system. Channel 1 can also be put into data trace mode, where MCRC controller compresses each data being read through CPU read data bus.

For more information, see *MCRC Controller* section in *Interprocessor Communication* chapter in the device TRM.

#### **8.4.2.14 MCSPI**

The MCSPI module is a multichannel transmit/receive, master/slave synchronous serial bus.

There are total of seven MCSPI modules in the device.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

#### **8.4.2.15 MMCSDB**

There are two Multi-Media Card/Secure Digital (MMCSDB) modules inside the device - MMCSDB0 and MMCSDB1. Each MMCSDB module includes one MMCSDB Host Controller, where MMCSDB0 is associated with MMC0 and MMCSDB1 is associated with MMC1.

The MMCSDB Host Controller supports:

- One controller with 8-bit wide data bus
- One controller with 4-bit wide data bus

- Support of eMMC5.1 Host Specification (JESD84-B51)
- Support of SD Host Controller Standard Specification - SDIO 3.00
- Integrated DMA controller supporting SD Advanced DMA - ADMA2 and ADMA3
- eMMC Electrical Standard 5.1 (JESD84-B51)
- Multi-Media card features:
  - Backward compatible with earlier eMMC standards
  - Legacy MMC SDR: 1.8 V, 8/4/1-bit bus width, 0-25 MHz, 25/12.5/3.125 MB/s
  - High Speed SDR: 1.8 V, 8/4/1-bit bus width, 0-50 MHz, 50/25/6.25 MB/s
  - High Speed DDR: 1.8 V, 8/4-bit bus width, 0-50 MHz, 100/50 MB/s
  - HS200 SDR: 1.8 V, 0-200 MHz, 8/4-bit bus width, 200/100 MB/s
- SD card support: SDIO, SDR12, SDR25, SDR50, DDR50
- System bus interface: CBA 4.0 VBUSM master port with 64-bit data width and 64-bit address, little endian only
- Configuration bus interface: CBA 4.0 VBUSM with 32-bit data width, 32-bit aligned accesses only, linear incrementing addressing mode, little endian only

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

#### 8.4.2.16 OSPI

The Octal Serial Peripheral Interface (OSPI) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices. This module has a memory mapped register interface, which provides a direct memory interface for accessing data from external flash devices, simplifying software requirements.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signalling its completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device master at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

#### 8.4.2.17 Peripheral Component Interconnect Express (PCIe)

The PCIe subsystem supports the following main features:

- Dual mode – root port (RP) or end point (EP) modes. Selectable through bootstrap pins.
- 1-lane configuration with up to 5.0GT/lane.
- 62.5/125 MHz operation on PIPE interface for Gen1/Gen2 respectively
- Constant 32-bit PIPE width for Gen1/Gen2 modes
- Maximum outbound payload size of 128 bytes
- Maximum inbound payload size of 128 bytes
- Maximum remote read request size of 4K bytes
- Maximum number of nonposted outstanding transactions: 8 on each VBUSM interface.
- Four virtual channels (4VC)
- Resizable BAR capability
- SRIS support
- Power Management
  - L1 Power Management Substate support
  - D1 support
  - L1 Power Shutoff support
- Legacy, MSI, and MSI-X interrupt support
- 32 outbound address translation regions
- Precision time measurement (PTM)



For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

#### 8.4.2.18 Serializer/Deserializer (SerDes)

Integrated in the MAIN domain is one instance of high-speed differential interface implemented with Serializer/Deserializer (SERDES) Multi-protocol Multi-link modules with the following main blocks:

- Single-lane PHY with common module for peripheral and Tx clocking handling
- Physical coding sub-block for data translation from/to the parallel interface, as well as data encoding/decoding and symbol alignment
- MUX module for device interface multiplexing into a single SERDES lane (Tx and Rx)
- A wrapper for sending control and reporting status signals from the SerDes and muxes

For more information, see *Serializer/Deserializer (SerDes)* section in *Peripherals* chapter in the device TRM.

#### 8.4.2.19 RTI

This section describes the Real Time Interrupt (RTI) modules with Windowed Watchdog Timer (WWDT) functionality for the device.

For more information, see *Real Time Interrupt (RTI) Module* section in *Peripherals* chapter in the device TRM.

#### 8.4.2.20 DMTIMER

The DMTIMER module supports the following main features:

- Interrupts generated on overflow, compare and capture
- Free running 32-bit upward counter
- Supported modes:
  - Compare and capture modes
  - Auto-reload mode
  - Start-stop mode
- Programmable divider clock source (2<sup>n</sup> with n=[0:8])
- Dedicated input trigger for capture mode, and dedicated output trigger/PWM (pulse width modulation) signal
- On the fly read/write register (while counting)
- Generate 1-ms tick with 32768-Hz functional clock

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

#### 8.4.2.21 UART

The UART module supports the following main features:

- 16C750 compatibility
- Baud rate from 300 bps up to 3.6864 Mbps (subject to functional clock frequency)
- Auto-baud between 1200 bps and 115.2 Kbps
- Software/hardware flow control
  - Programmable Xon/Xoff characters
  - Programmable Auto-RTS and Auto CTS
- Programmable serial interface characteristics
  - 5, 6, 7, or 8-bit characters
  - Even, odd, mark (always 1), space (always 0), or no parity (non-parity bit frame) bit generation and detection
  - 1-, 1.5-, or 2-stop bit generation
- Optional multi-drop transmission
- Configurable time-guard feature
- False start bit detection
- Line break generation and detection
- Modem control functions on UART0 (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully prioritized interrupt system controls
- Internal test and loopback capabilities
- RS-485 External transceiver auto flow control support

For more information, see *Universal Synchronous/Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

#### **8.4.2.22 Universal Serial Bus Subsystem(USBSS)**

The Universal Serial Bus Subsystem (USBSS) module supports the following main features:

USB interface:

- Compliant with USB 3.1 Gen1 specification
- Compliant with xHCI 1.1 specification
- Limited USB 2.0 on-the-go support
- SuperSpeed Gen1 (5 Gbps), high speed (480 Mbps), and full (12Mbps) Device
- SuperSpeed Gen1 (5 Gbps), high speed (480 Mbps), full (12Mbps), and low speed (1.5 Mbps) Host
- Shared USB3.1/USB2.0 port

Dual mode operation:

- OTG 2.0 host negotiation protocol (HNP) support
- OTG 2.0 session request support (SRP) support

Host mode:

- 64 slots supported
- Up to 96 periodic endpoints supported simultaneously
- 256 primary streams supported
- MSI support
- Root hub functionality

For more information, see *Universal Serial Bus (USB) Subsystem* section in *Peripherals* chapter in the device TRM.

## 9 Applications, Implementation, and Layout

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 9.1 Power Supply Mapping

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#### Note

NOTE TO USERS:

The content of this section is UNDER DEVELOPMENT!

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## 9.2 Device Connection and Layout Fundamentals

### 9.2.1 Power Supply Decoupling and Bulk Capacitors

#### 9.2.1.1 Power Distribution Network Implementation Guidance

The [Sitara Processor Power Distribution Networks: Implementation and Analysis](#) provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI supports *only* designs that follow the board design guidelines contained in the application report.

### 9.2.2 External Oscillator

For more information about External Oscillators, see the *Clock Specifications* section.

### 9.2.3 JTAG and EMU

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the [XDS Target Connection Guide](#).

For more recommendations on EMU routing, see [Emulation and Trace Headers Technical Reference Manual](#)

### 9.2.4 Unused Pins

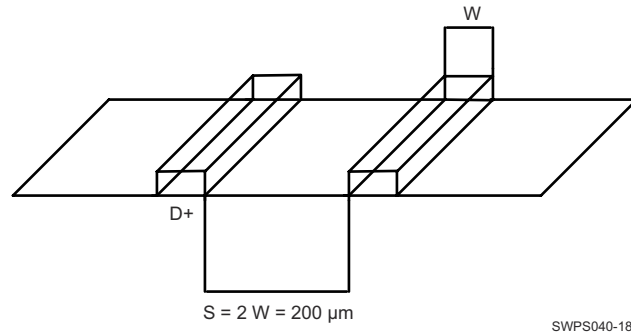
For more information about Unused Pins, see the *Connections for Unused Pins* section.

## 9.3 Peripheral- and Interface-Specific Design Information

### 9.3.1 General Routing Guidelines

The following paragraphs detail the routing guidelines that must be observed when routing the various functional LVCMOS interfaces.

- Line spacing:
  - For a line width equal to  $W$ , the spacing between two lines must be  $2W$ , at least. This minimizes the crosstalk between switching signals between the different lines. On the PCB, this is not achievable everywhere (for example, when breaking signals out from the device package), but it is recommended to follow this rule as much as possible. When violating this guideline, minimize the length of the traces running parallel to each other (see [Figure 9-1](#)).



**Figure 9-1. Ground Guard Illustration**

- Length matching (unless otherwise specified):
  - For bus or traces at frequencies less than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 25 mm.
  - For bus or traces at frequencies greater than 10 MHz, the trace length matching (maximum length difference between the longest and the shortest lines) must be less than 2.5 mm.
- Characteristic impedance
  - Unless otherwise specified, the characteristic impedance for single-ended interfaces is recommended to be between 35-Ω and 65-Ω.
- Multiple peripheral support
  - For interfaces where multiple peripherals have to be supported in the star topology, the length of each branch has to be balanced. Before closing the PCB design, it is highly recommended to verify signal integrity based on simulations including actual PCB extraction.

### 9.3.2 DDR Board Design and Layout Guidelines

The goal of the [AM64x DDR Board Design and Layout Guidelines](#) is to make the DDR system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using DDR4 or LPDDR4 memories that follow the guidelines in this document.

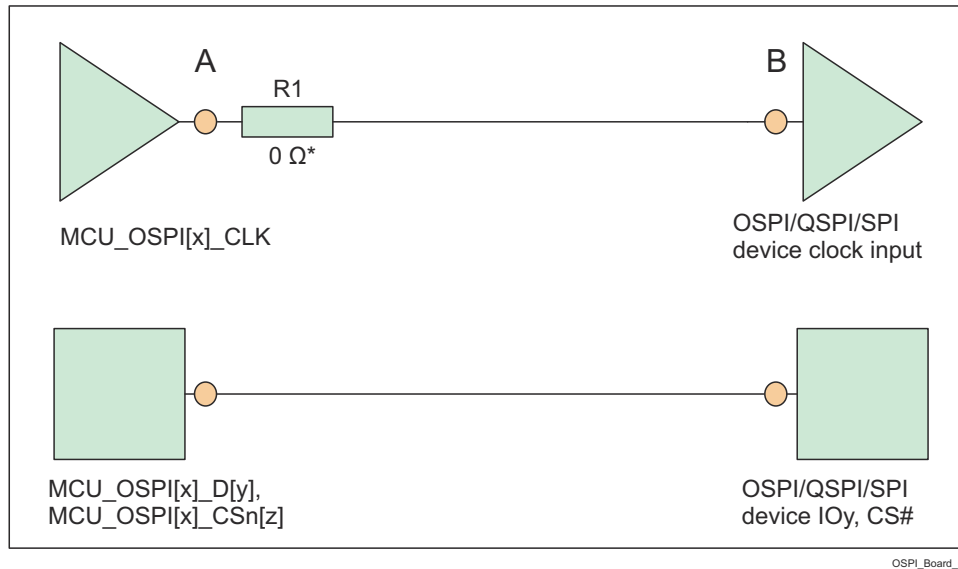
### 9.3.3 OSPI and QSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the OSPI and QSPI interfaces.

#### 9.3.3.1 No Loopback and Internal Pad Loopback

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The signal propagation delay from the MCU\_OSPI[x]\_CLK signal to the flash device must be < 450 ps (~7cm as stripline or ~8cm as microstrip)
- 50 Ω PCB routing is recommended along with series terminations, as shown in [OSPI Interface High Level Schematic](#)
- Propagation delays and matching:
  - A to B < 450 ps

- Matching skew: < 60 ps



\* 0 Ω resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK pin, is placeholder for fine tuning, if needed.

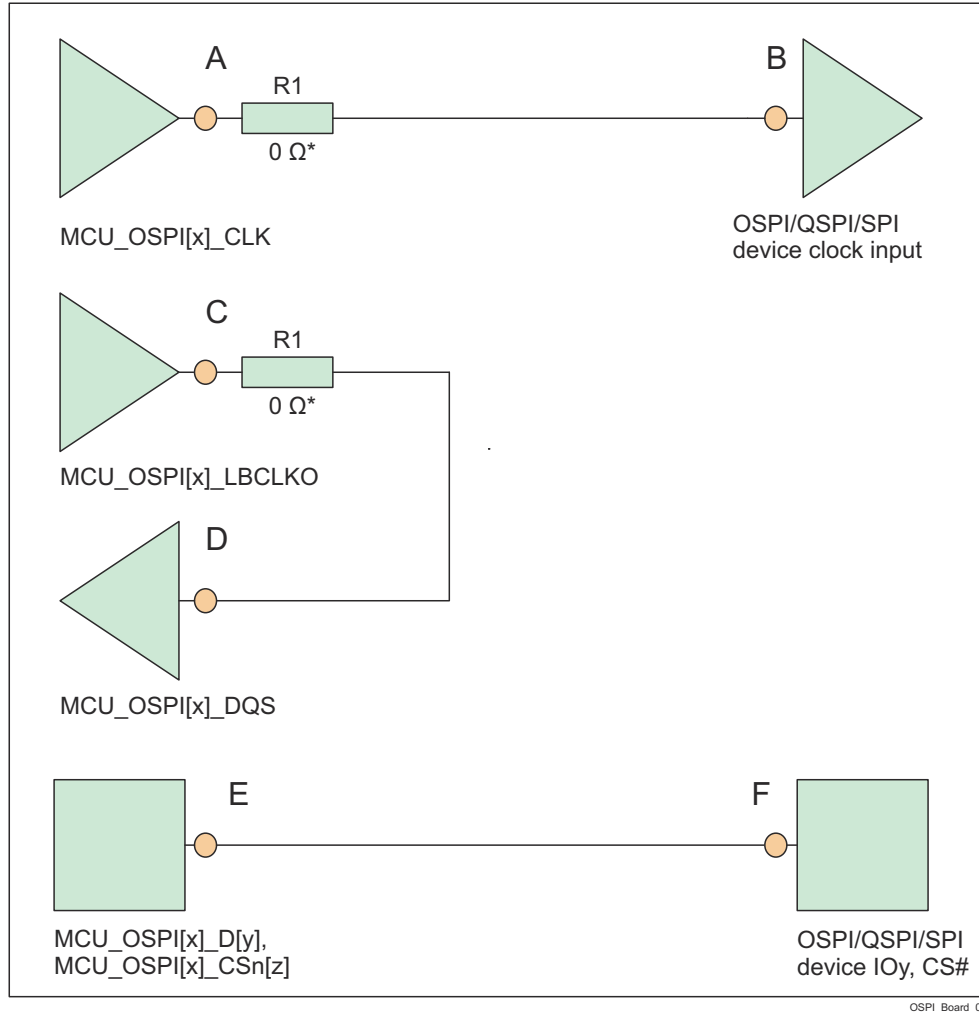
**Figure 9-2. OSPI Interface High Level Schematic**

### 9.3.3.2 External Board Loopback

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The MCU\_OSPI[x]\_LBCLKO output signal must be looped back into the MCU\_OSPI[x]\_DQS input
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to half of the signal propagation delay from the MCU\_OSPI[x]\_LBCLKO pin to the MCU\_OSPI[x]\_DQS pin ((C to D)/2). See the note below.
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) must be approximately equal to the signal propagation delay of the control and data signals between the flash device and the SoC device (E to F, or F to E)
- 50 Ω PCB routing is recommended along with series terminations, as shown in [OSPI Interface High Level Schematic](#)
- Propagation delays and matching:
  - $A \text{ to } B = E \text{ to } F = (C \text{ to } D) / 2$
  - Matching skew: < 60 ps

#### Note

The OSPI Board Loopback Hold time requirement (described in [Section 7.10.5.14, OSPI](#)) is larger than the Hold time provided by a typical flash device. Therefore, the length of MCU\_OSPI[x]\_LBCLKO pin to the MCU\_OSPI[x]\_DQS pin (C to D) can be shortened to compensate.

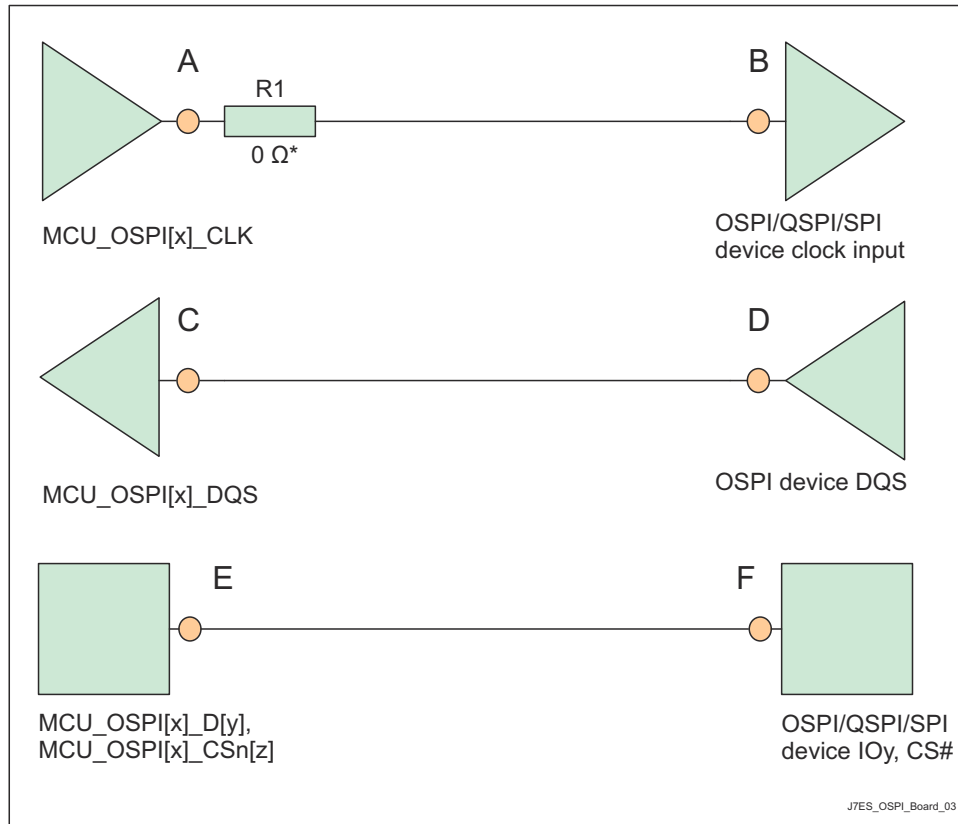


\* 0  $\Omega$  resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK and MCU\_OSPI[x]\_LBCLKO pins, is a placeholder for fine tuning, if needed.

**Figure 9-3. OSPI Interface High Level Schematic**

### 9.3.3.3 DQS (only available in Octal Flash devices)

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The DQS pin of the flash devices must be connected to MCU\_OSPI[x]\_DQS signal
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to the signal propagation delay from the MCU\_OSPI[x]\_DQS pin to the DQS output pin (C to D)
- 50  $\Omega$  PCB routing is recommended along with series terminations, as shown in [OSPI Interface High Level Schematic](#)
- Propagation delays and matching:
  - A to B = C to D
  - Matching skew: < 60 ps



\* 0 Ω resistor (R1), located as close as possible to the `MCU_OSPI[x]_CLK` pin, is a placeholder for fine tuning, if needed.

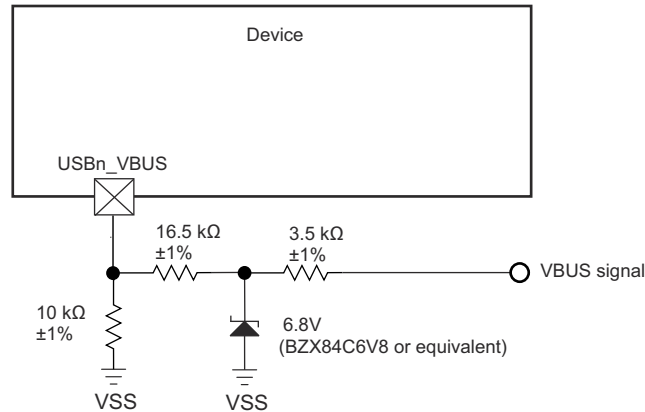
**Figure 9-4. OSPI Interface High Level Schematic**

### 9.3.4 USB VBUS Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30 V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the [Figure 9-5](#)), which limits the voltage applied to the actual device pin (`USB0_VBUS`). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of zener diode at 5 V should be less than 100 nA.





J7ES\_USB\_VBUS\_01

A. USBn\_VBUS, where n = 0.

**Figure 9-5. USB VBUS Detect Voltage Divider / Clamp Circuit**

The USB0\_VBUS pin can be considered to be fail-safe because the external circuit in Figure 9-5 limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

### 9.3.5 System Power Supply Monitor Design Guidelines

The VMON\_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system. This supply is monitored by comparing the output of an external voltage divider circuit sourced by this supply with an internal voltage reference, with a power fail event being triggered when the voltage applied to VMON\_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit.

When designing the resistor divider circuit it is important to understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON\_VSYS input threshold which has a nominal value of 0.45 V, with a variation of  $\pm 3\%$ . Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON\_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON\_VSYS input leakage current may be in the range of 10 nA to 2.5  $\mu$ A when applying 0.45 V.

#### Note

The resistor voltage divider shall be designed such that its output voltage never exceeds the maximum value defined in the *Recommended Operating Conditions* section, during normal operating conditions.

Figure 9-6 presents an example, where the system power supply is nominally 5 V and the maximum trigger threshold is 5 V - 10%, or 4.5 V.

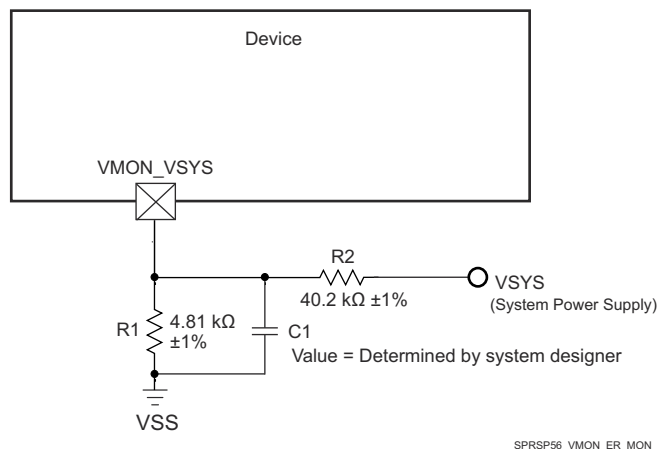
For this example, it is important to understand which variables effect the maximum trigger threshold when selecting resistor values. It is obvious a device which has a VMON\_VSYS input threshold of 0.45 V + 3% needs to be considered when trying to design a voltage divider that doesn't trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but how these contributions effect the maximum trigger point may not be obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON\_VSYS pin is 2.5  $\mu$ A. When implementing a resistor divider where R1 = 4.81 K $\Omega$  and R2 = 40.2 K $\Omega$ , the result is a maximum trigger threshold of 4.523 V.

Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of 0.45 V - 3% when the value of R1 is 1% high and the value of R2 is 1% low, and the input leakage current is 10 nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.008 V.

This example demonstrates a system power supply voltage trip point that ranges from 4.008 V to 4.523 V. Approximately 250 mV of this range is introduced by VMON\_VSYS input threshold accuracy of  $\pm 3\%$ , approximately 150 mV of this range is introduced by resistor tolerance of  $\pm 1\%$ , and approximately 100 mV of this range is introduced by loading error when VMON\_VSYS input leakage current is 2.5  $\mu\text{A}$ .

The resistor values selected in this example produces approximately 100  $\mu\text{A}$  of bias current through the resistor divider when the system supply is 4.5 V. The 100 mV of loading error mentioned above could be reduced to about 10 mV by increasing the bias current through the resistor divider to approximately 1 mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer should also consider implementing a noise filter on the voltage divider output since VMON\_VSYS has minimum hysteresis and a high-bandwidth response to transients. This could be done by installing a capacitor across R1 as shown in Figure 9-6. However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.



**Figure 9-6. System Supply Monitor Voltage Divider Circuit**

VMON\_1P8\_MCU and VMON\_1P8\_SOC pins provide a way to monitor external 1.8 V power supplies. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

VMON\_3P3\_MCU and VMON\_3P3\_SOC pins provide a way to monitor external 3.3 V power supplies. An internal resistor divider with software control is implemented inside the SoC for each of these pins. Software can program each internal resistor divider to create appropriate under voltage and over voltage interrupts.

### 9.3.6 High Speed Differential Signal Routing Guidance

The [High Speed Interface Layout Guidelines](#) provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application report.

### 9.3.7 Thermal Solution Guidance

The [Thermal Design Guide for DSP and ARM Application Processors](#) provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

## 10 Device and Documentation Support

### 10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, AM2434\_ALV, AM2432\_ALV, AM2431\_ALV). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM243x devices in the ALV package type, see the Package Option Addendum of this document, the TI website ([ti.com](http://ti.com)), or contact your TI sales representative.

### 10.1.1 Standard Package Symbolization

#### Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

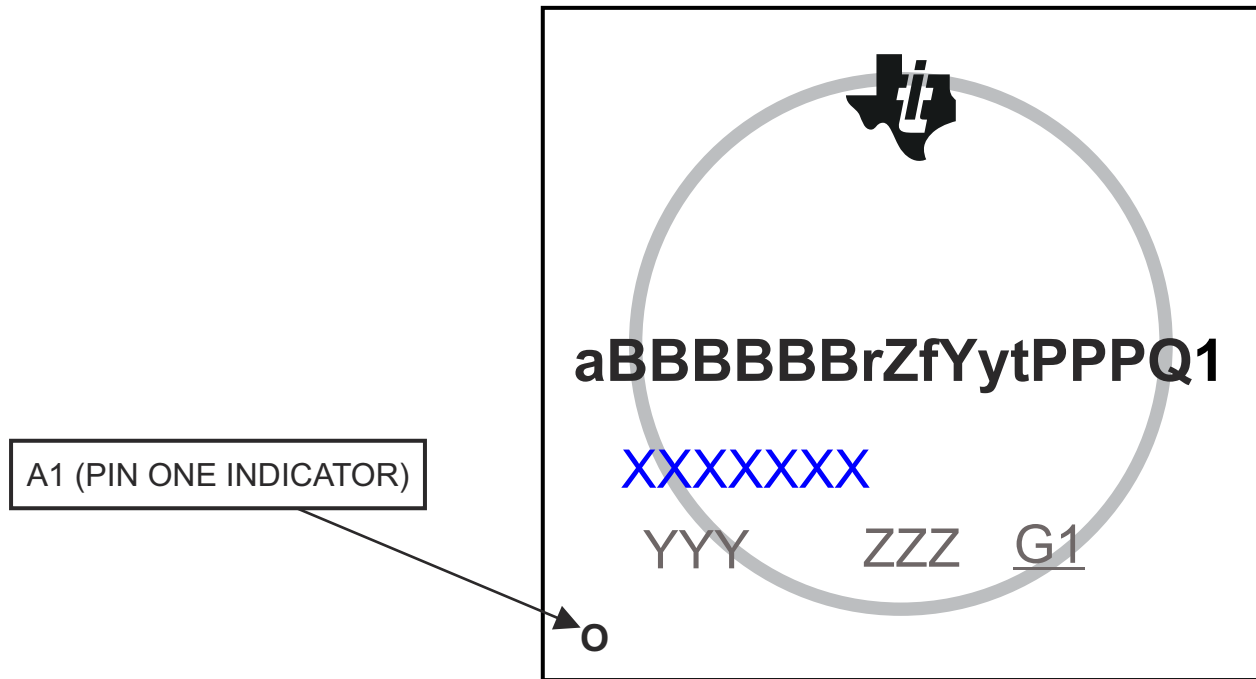


Figure 10-1. Printed Device Reference

### 10.1.2 Device Naming Convention

Table 10-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
a <sup>(1)</sup>	Device evolution stage	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK	Production
BBBBBB	Base production part number	AM2434	See Table 5-1 , Device Comparison
		AM2432	
		AM2431	
r	Device revision	A	SR 1.0
Z	Device Speed Grades	S	See Table 7-2, Speed Grade Maximum Frequency
f	Features (see Table 5-1)	C	No Additional Features Enabled
		D	ICSS Enabled
		E	ICSS + EtherCAT HW Accelerator + CAN-FD Enabled
		F	ICSS + EtherCAT HW Accelerator + CAN-FD + Pre-integrated Stacks Enabled
Y	Functional Safety	G	Non-Functional Safety
		F <sup>(2)</sup>	Functional Safety

**Table 10-1. Nomenclature Description (continued)**

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
y	Security	G	Non-Secure
		Other	Secure
t <sup>(3)</sup>	Temperature	A	-40°C to 105°C - Extended Industrial (see <a href="#">Recommended Operating Conditions</a> )
PPP	Package Designator	ALV	ALV FCBGA-N441 (17.2 mm × 17.2 mm) Package
		ALX	ALX FC/CSP-N293 (11.0 mm × 11.0 mm) Package
XXXXXXX			Lot Trace Code (LTC)
YYY			Production Code; For TI use only
ZZZ			Production Code; For TI use only
O			Pin one designator
G1			ECAT—Green package designator

- To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices. Prototype devices are shipped against the following disclaimer:  
“This product is still in development and is intended for internal evaluation purposes.”  
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.
- Functional Safety features are not supported by ALX package.
- Applies to device max junction temperature.

**Note**

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

## 10.2 Tools and Software

The following products support development for AM243x platforms:

### Development Tools

**Code Composer Studio™ Integrated Development Environment** Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

**SysConfig-PinMux Tool** The SysConfig-PinMux Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool will generate output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements.

**Power Estimation Tool (PET)** Power Estimation Tool (PET) provides users the ability to gain insight in to the power consumption of select TI processors. The tool includes the ability for the user to choose multiple application scenarios and understand the power consumption as well as how advanced power saving techniques can be applied to further reduce overall power consumption.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at [ti.com](http://ti.com). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

## 10.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral is listed below.

The following documents describe the AM243x family of devices.

### Technical Reference Manual

[AM64x/AM243x Processors Silicon Revision 1.0 Technical Reference Manual](#) Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM243x family of devices.

### Errata

[AM64x/AM243x Processors Silicon Revision 1.0 Silicon Errata](#) Describes the known exceptions to the functional specifications for the device.

**Tip:** Search TI.com using literature numbers.

## 10.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 10.5 Trademarks

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PCI-Express® are registered trademarks of PCI-SIG.

EtherCAT® is a registered trademark of Beckhoff Automation GmbH.

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## 10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

### 11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XAM2431ASFGGAALV	ACTIVE	FCBGA	ALV	441	84	TBD	Call TI	Call TI	-40 to 105		<a href="#">Samples</a>
XAM2431ASFGGAALX	ACTIVE	FC/CSP	ALX	293	96	TBD	Call TI	Call TI	-40 to 105		<a href="#">Samples</a>
XAM2432ASFGGAALV	ACTIVE	FCBGA	ALV	441	84	TBD	Call TI	Call TI	-40 to 105		<a href="#">Samples</a>
XAM2432ASFGGAALX	ACTIVE	FC/CSP	ALX	293	96	TBD	Call TI	Call TI	-40 to 105		<a href="#">Samples</a>
XAM2434ASFGGAALV	ACTIVE	FCBGA	ALV	441	1	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 105	(SFGGAALV, XAM2434 A) 709	<a href="#">Samples</a>
XAM2434ASFGGAALX	ACTIVE	FC/CSP	ALX	293	1	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 105	XAM2434A SFGGAALX 709	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

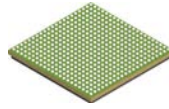


<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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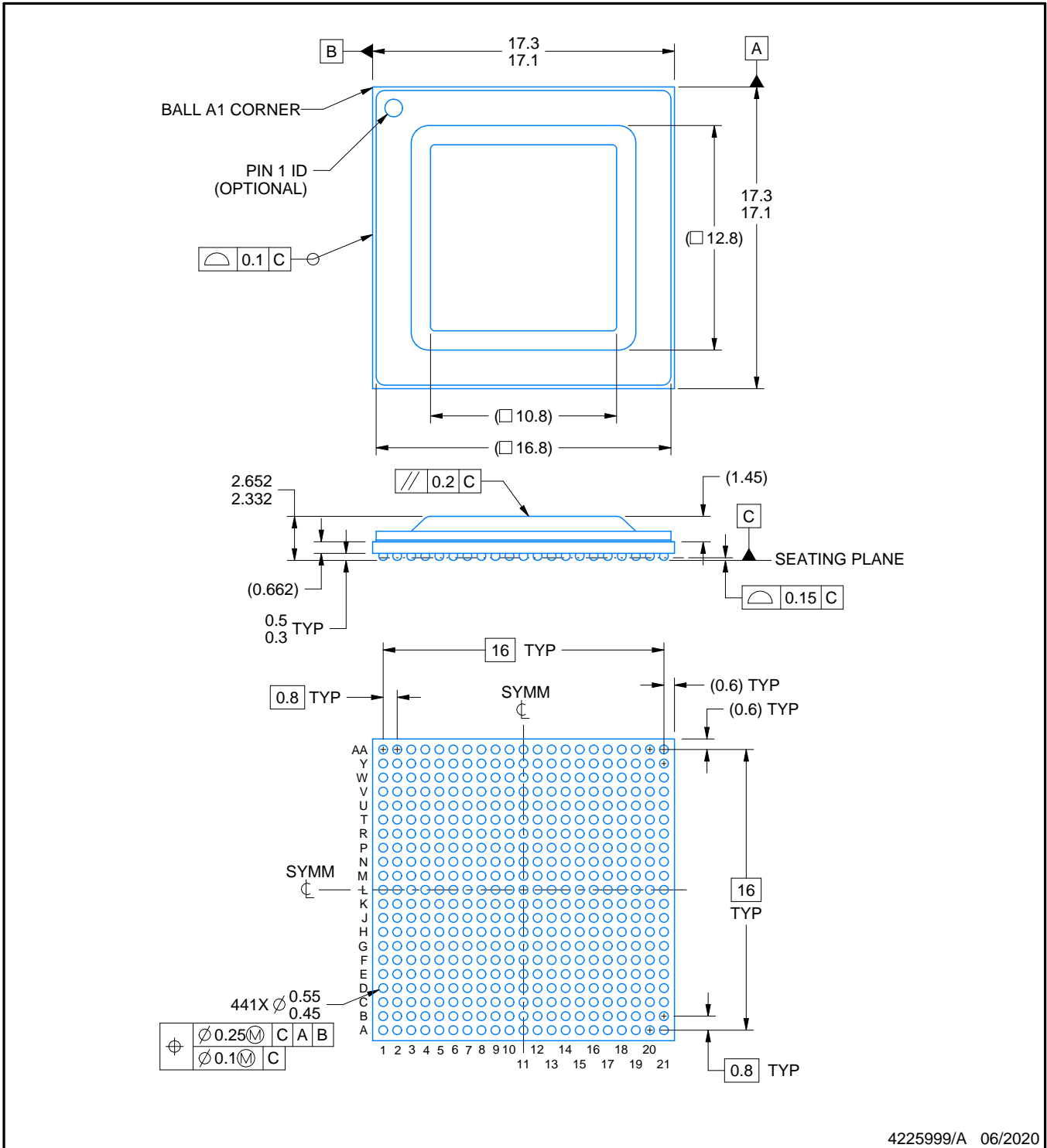
# ALV0441A



# PACKAGE OUTLINE

FCBGA - 2.657 mm max height

BALL GRID ARRAY



4225999/A 06/2020

**NOTES:**

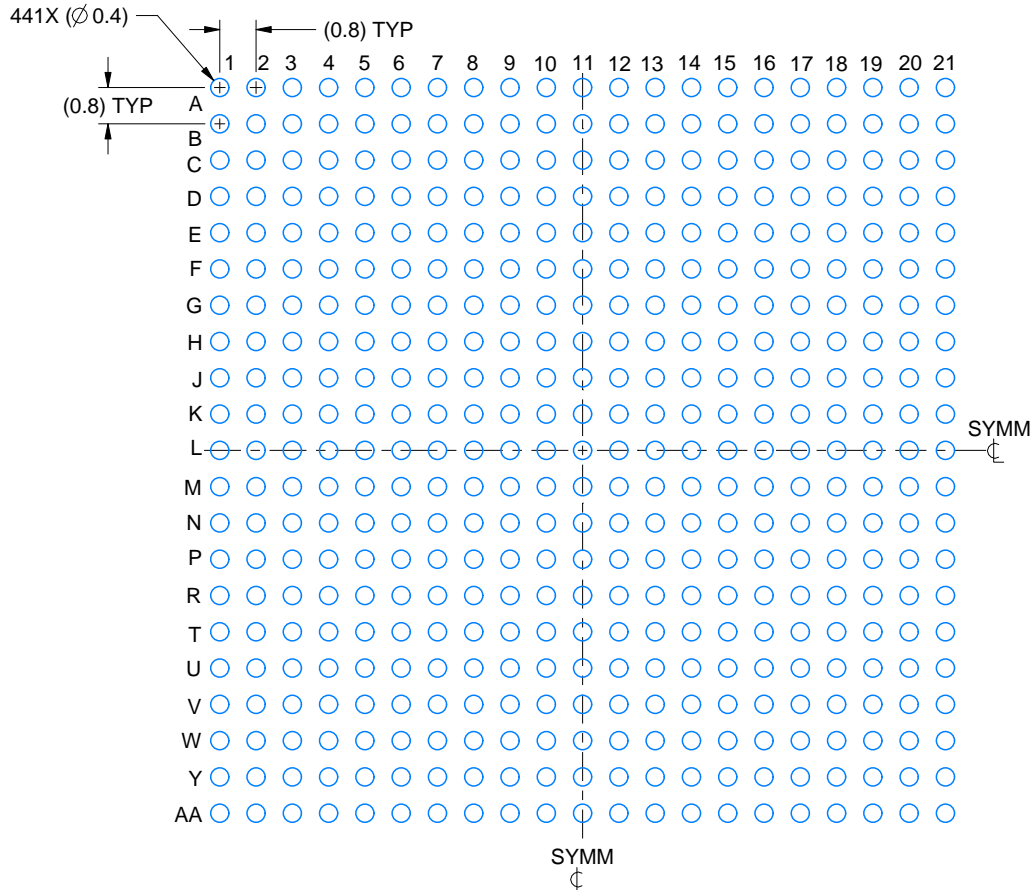
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

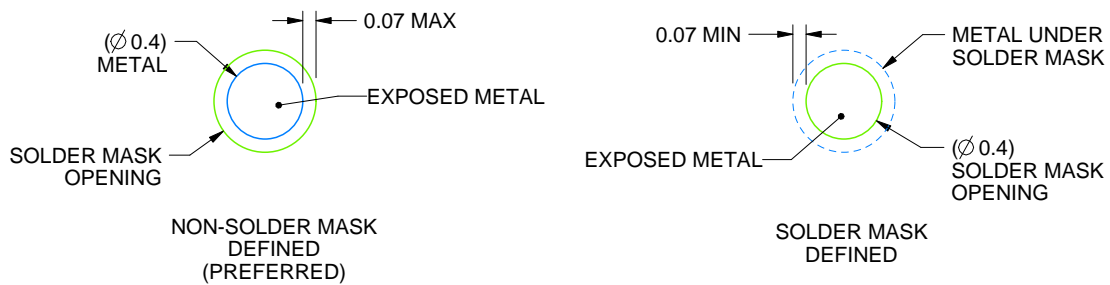
ALV0441A

FCBGA - 2.657 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

4225999/A 06/2020

NOTES: (continued)

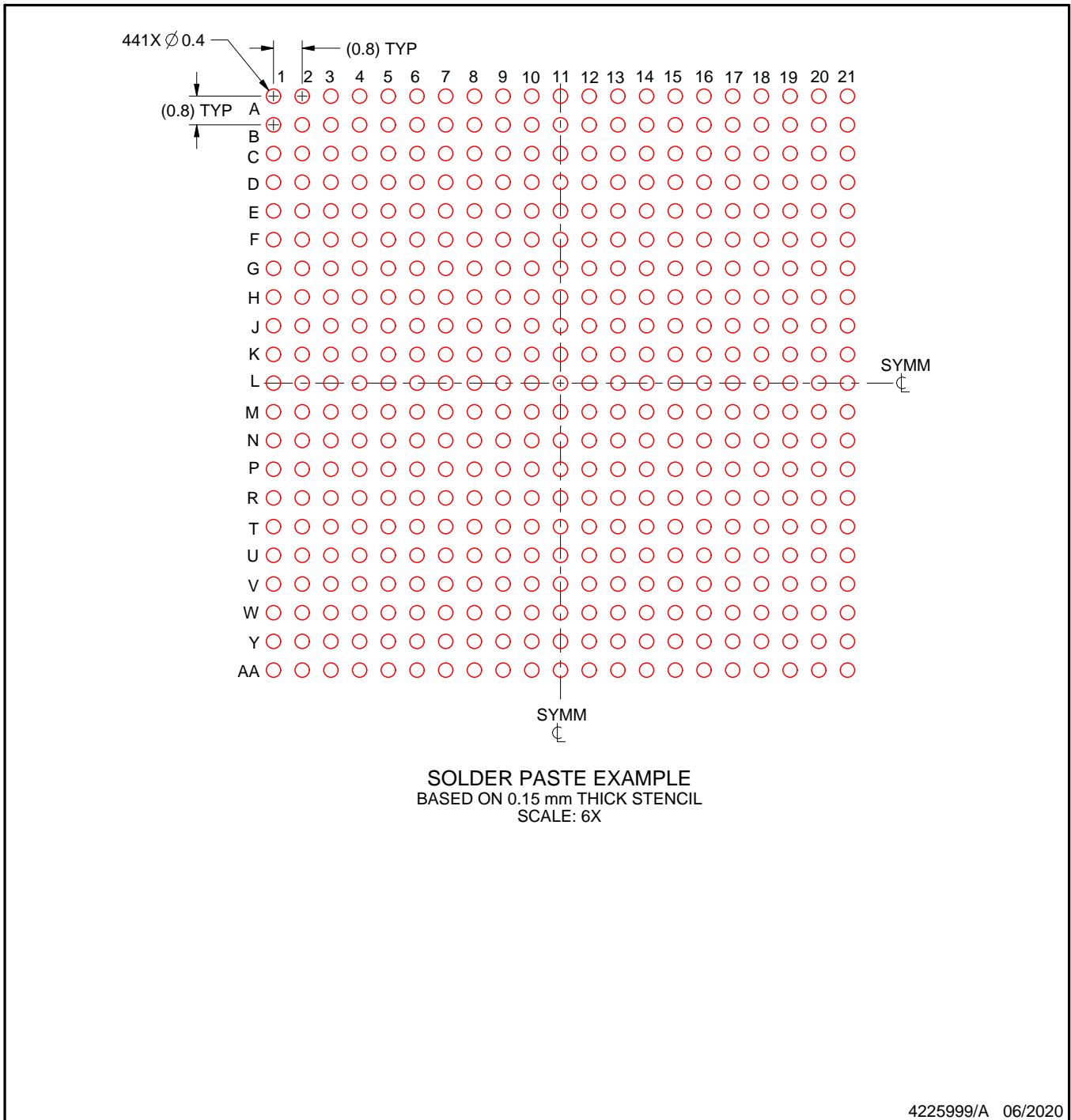
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

ALV0441A

FCBGA - 2.657 mm max height

BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

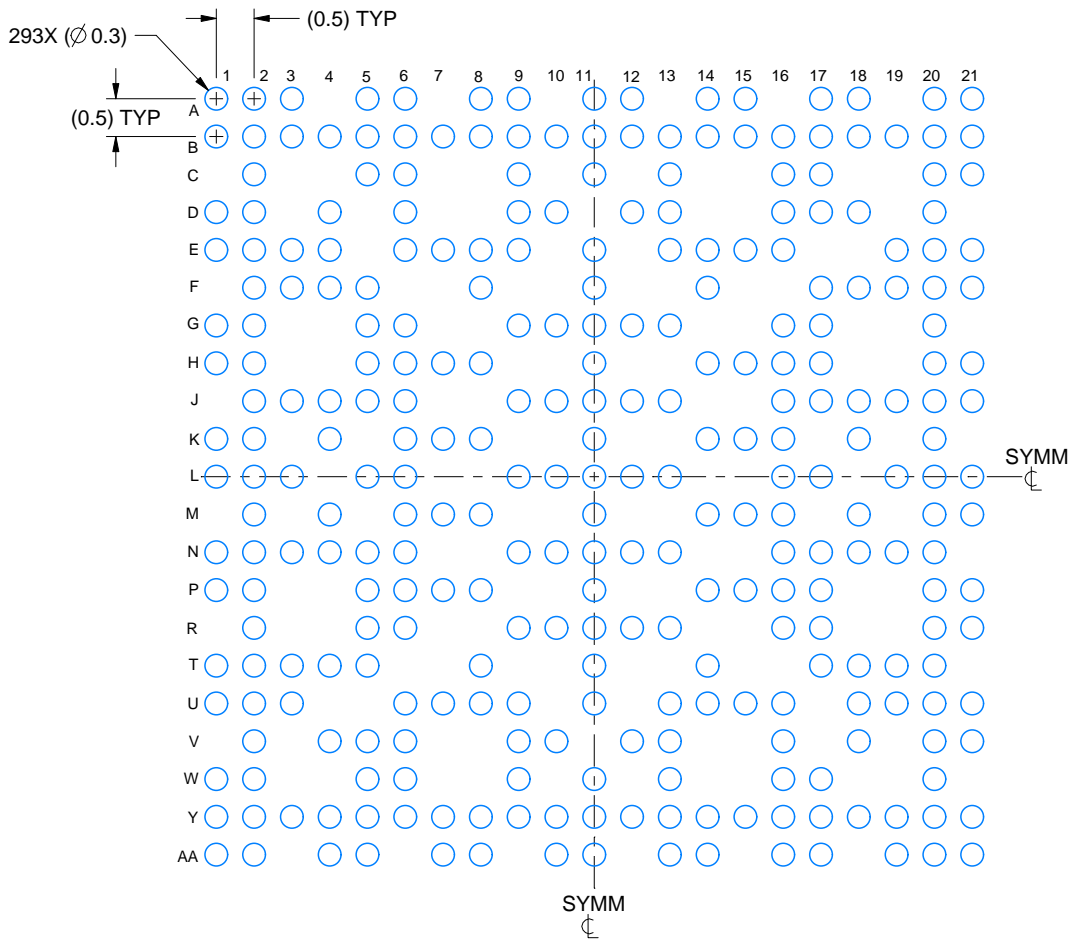


# EXAMPLE BOARD LAYOUT

ALX0293A

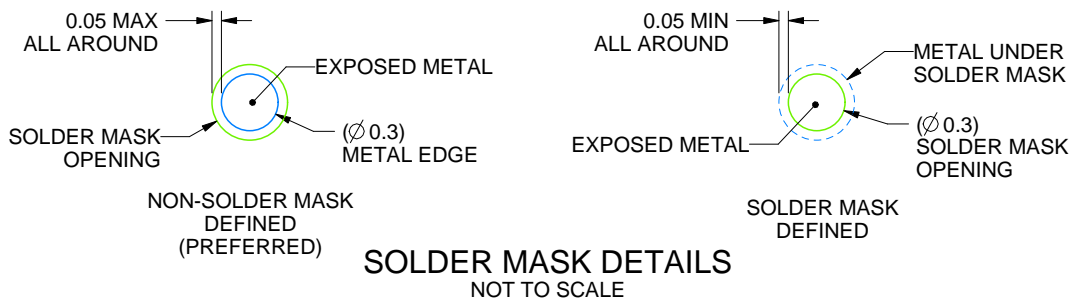
FCBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN  
SCALE: 10X



4226368/A 10/2020

NOTES: (continued)

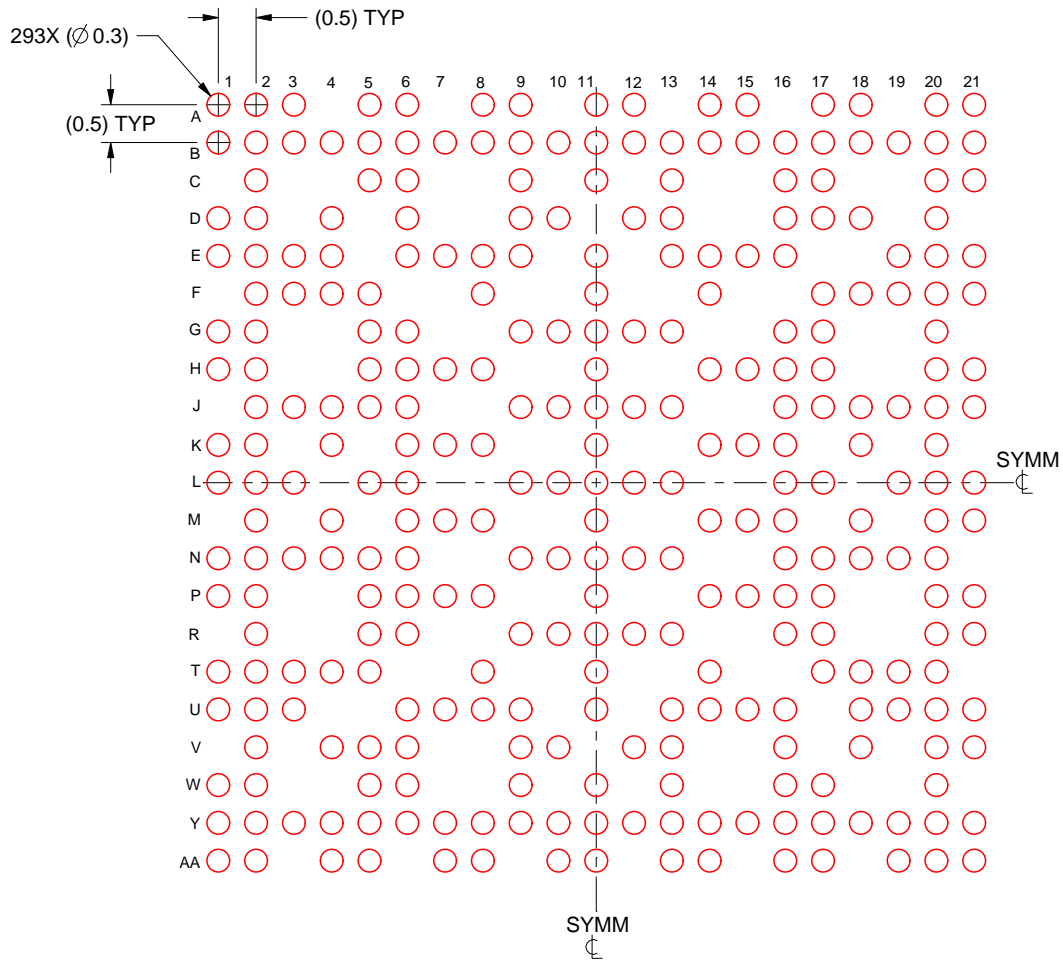
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

# EXAMPLE STENCIL DESIGN

ALX0293A

FCBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4226368/A 10/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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