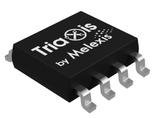
MLX90421 Triaxis® Position Sensor IC

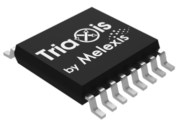
Datasheet

Features and Benefits

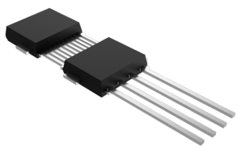
- Triaxis® Hall Technology
- On Chip Signal Processing for Robust Absolute Position Sensing
- ASIL READY BY MELEXIS ISO26262 ASIL-B Safety Element out of Context
- AEC-Q100 Qualified (Grade 0)
- Programmable Measurement Range
- Programmable Linear Transfer Characteristic with up to 17 points
- Ratiometric analog or PWM Output
- Single Die - SOIC-8 Package RoHS Compliant
- Dual Die (Full Redundant) - TSSOP-16 Package RoHS Compliant
- PCB-less DMP-4 and SMP-3 RoHS Compliant
- PCB-less dual die SMP-4 RoHS Compliant



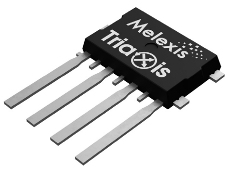
SOIC-8



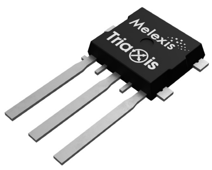
TSSOP-16



DMP-4



SMP-4



SMP-3

Application Examples

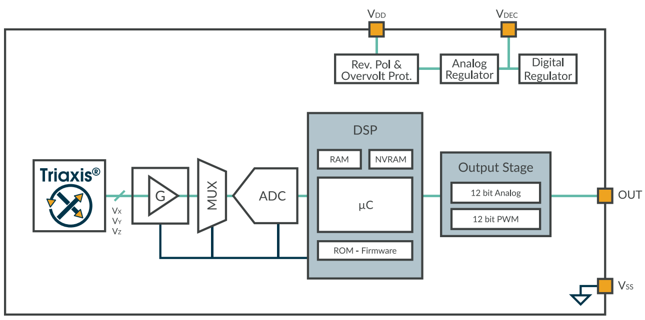
- Absolute Rotary Position Sensor
- Pedal Position Sensor
- Throttle Position Sensor
- Ride Height Position Sensor
- Transmission Position Sensor
- Absolute Linear Position Sensor
- Steering Wheel Position Sensor
- Float-Level Sensor
- Non-Contacting Potentiometer

Description

The MLX90421 is a monolithic magnetic position sensor IC. It consists of a Triaxis® Hall magnetic front end, an analog to digital signal conditioner, a DSP for advanced signal processing and a programmable output stage driver.

The MLX90421 is sensitive to the three components of the magnetic flux density applied to the ICs (i.e. Bx, By and Bz). Programming the sensor determines which axes are used to calculate a rotation or linear position. This allows the MLX90421, with the correct magnetic design, to calculate the absolute position of any moving magnet (e.g. rotary position from 0 to 360 Degrees, see Figure 2). It enables the design of non-contacting position sensors that are frequently required for both automotive and industrial applications.

The MLX90421 provides ratiometric analog or pulse width modulated (PWM) outputs. Programming the sensor, after assembly into the application, increases the accuracy of the system thanks to the multi-point programmable linearization function.



MLX90421

Ordering Information

Product	Temp.	Package	Option Code	Packing Form	Definition
MLX90421	G	DC	ADC-000	RE	Angular Rotary Analog/PWM version
MLX90421	G	GO	ADC-000	RE	Angular Rotary Analog/PWM version
MLX90421	G	VS	ADC-000	RE/RX	Angular Rotary Analog/PWM version
MLX90421	G	VS	ADC-003	RE/RX	Angular Rotary Analog/PWM version
MLX90421	G	VS	ADC-008	RE/RX	Angular Rotary Analog/PWM version
MLX90421	G	VE	ADC-000	RE/RX	Angular Rotary Analog/PWM version
MLX90421	G	VD	ADC-000	RE/RX	Angular Rotary Analog/PWM version

Table 1 - Ordering Codes

Temperature Code:	G : from -40°C to 160°C
Package Code:	DC : SOIC-8 package (see 18.1) GO : TSSOP-16 package (full redundancy dual die, see 18.2) VS : DMP-4 package (PCB-less dual mold, see 18.3) VE : SMP-3 package (PCB-less single mold, see 18.4) VD : SMP-4 package (PCB-less single mold dual die, see 18.5)
Option Code - Chip revision	**AAA-123 : Chip Revision** ▪ ADC: MLX90421 production version
Option Code - Application	AAA-123 : **1-Application - Magnetic configuration** ▪ 0: Angular Rotary / Linear Position
Option Code	AAA-123 : **2-Option** ▪ 0: Standard
Option Code - Trim & Form	AAA-123 : **3-DMP-4 Trim & Form configuration** ▪ 0: Standard straight leads. See section 18.3.1 ▪ 3: Trim and Form STD2 2.54. See section 18.3.2 ▪ 8: Trim and Form STD4 2.54. See section 18.3.3
Packing Form:	-RE : Tape & Reel ▪ VS: 2500 pcs/reel ▪ DC: 3000 pcs/reel ▪ GO: 4500 pcs/reel ▪ VE: 2500 pcs/reel ▪ VD: 2500 pcs/reel -RX : Tape & Reel, similar to RE with parts face-down (VS, VE, VD package only)
Ordering Example:	MLX90421GDC-ADC-000-RE For an analog version in SOIC-8 package, delivered in Reel of 3000pcs.

Table 2 - Ordering Codes Information

Contents

1. Functional Diagram and Application Modes

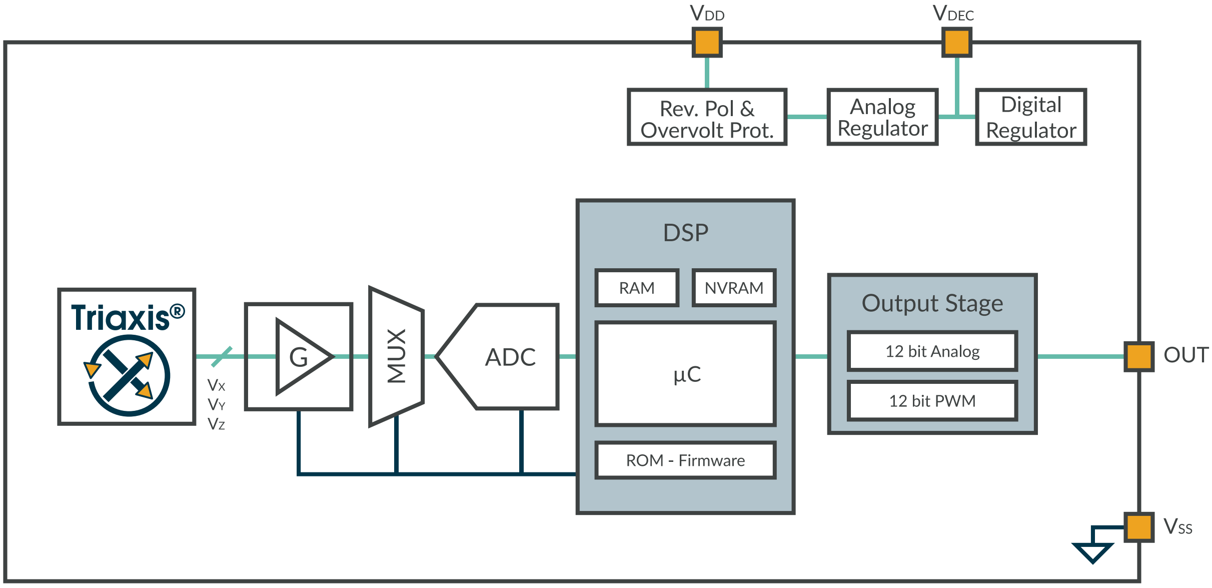


Figure 1 - MLX90421 Block diagram

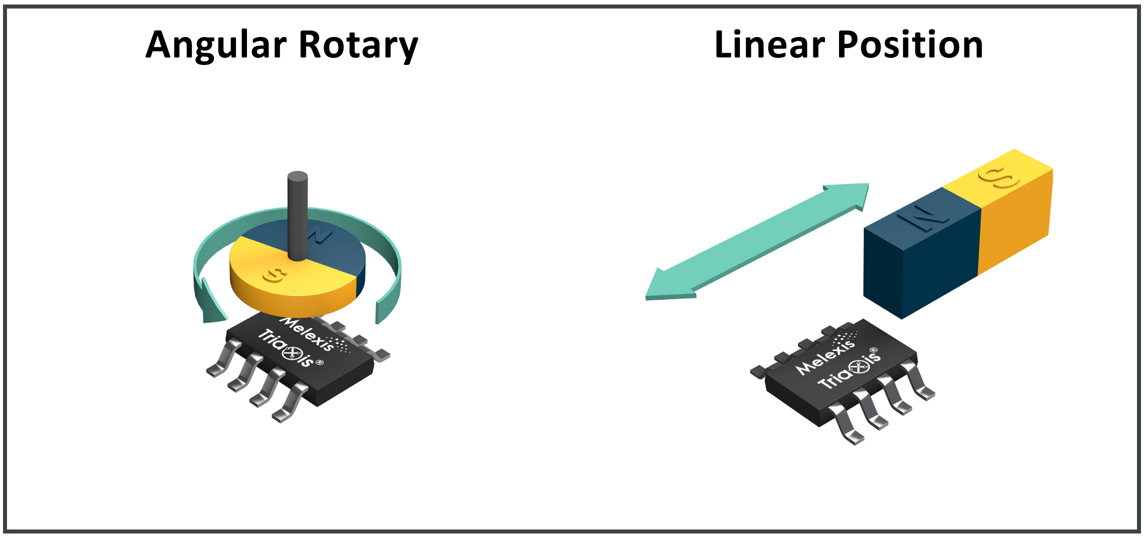


Figure 2 - Application Modes

2. Glossary of Terms

Name	Description
ADC	Analog-to-Digital Converter
AoU	Assumption of Use
AWD	Absolute Watchdog
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
%DC	Duty Cycle of the output signal i.e. T_{ON} /(T_{ON} + T_{OFF})
DMP	Dual Mold Package
DP	Discontinuity Point
DCT	Diagnostic Cycle Time
DSP	Digital Signal Processing
ECC	Error Correcting Code
EMC	Electro-Magnetic Compatibility
EoL	End of Line
FIR	Finite Impulse Response
Gauss (G)	Alternative unit for the magnetic flux density (10G = 1mT)
HW	Hardware
IMC	Integrated Magnetic Concentrator
INL / DNL	Integral Non-Linearity / Differential Non-Linearity
IWD	Intelligent Watchdog
LSB/MSB	Least Significant Bit / Most Significant Bit
N.C.	Not Connected
NVRAM	Non Volatile RAM
PCB	Printed Circuit Board
POR	Power On Reset
PSF	Product Specific Functions
PWL	Piecewise Linear
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
SEooC	Safety Element out of Context
SMP	Single-Mold Package
TC	Temperature Coefficient (in ppm/°C)
Tesla (T)	SI derived unit for the magnetic flux density (Vs/m2)

Table 3 - Glossary of Terms

3. Pin Definitions and Descriptions

3.1. Pin Definition for SOIC-8

Pin #	Name	Description
1	V_{DD}	Supply
2	$Test_1$	For Melexis factory test
3	$Test_2$	For Melexis factory test
4	N.C.	Not connected
5	OUT	Output
6	N.C.	Not connected
7	V_{DEC}	Decoupling pin
8	V_{SS}	Ground

Table 4 - SOIC-8 Pins definition and description

Test pins are internally grounded when in application mode. For optimal EMC behavior always connect the Test and N.C. pins to the ground of the PCB.

3.2. Pin Definition for TSSOP-16

Pin #	Name	Description
1	V_{DEC1}	Decoupling pin die1
2	V_{SS1}	Ground die1
3	V_{DD1}	Supply die1
4	$Test_{11}$	For Melexis factory test, die1
5	$Test_{22}$	For Melexis factory test, die2
6	OUT_2	Output die2
7	N.C.	Not connected
8	N.C.	Not connected
9	V_{DEC2}	Decoupling pin die2
10	V_{SS2}	Ground die2
11	V_{DD2}	Supply die2
12	$Test_{12}$	For Melexis factory test, die2
13	$Test_{21}$	For Melexis factory test, die1
14	N.C.	Not connected
15	OUT_1	Output die1
16	N.C.	Not connected

Table 5 - TSSOP-16 Pins definition and description

Test pins are internally grounded when in application mode. For optimal EMC behavior, always connect the Test and N.C. pins to the ground of the PCB.

3.3. Pin Definition for DMP-4

DMP-4 package offers a pin-to-pin compatibility with the previous generation of Triaxis® products.

Pin #	Name	Description
1	V_{SS}	Ground
2	V_{DD}	Supply
3	OUT	Output
4	V_{SS}	Ground

Table 6 - DMP-4 Pins definition and description

3.4. Pin Definition for SMP-3

SMP-3 package offers advanced components integration in a single mold compact form.

Pin #	Name	Description
1	V_{DD}	Supply
2	OUT	Output
3	V_{SS}	Ground

Table 7 - SMP-3 Pins definition and description

3.5. Pin Definition for SMP-4

SMP-4 package offers a redundant dual-die package with advanced components integration in a single mold compact form.

Pin #	Name	Description
1	OUT_1	Output 1
2	V_{SS}	Ground
3	V_{DD}	Supply
4	OUT_2	Output 2

Table 8 - SMP-4 Pins definition and description

4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{DD}		28 37	V	< 48h; T_J < 175°C < 60s ; $T_{AMB} \leq 35$°C
Reverse Voltage Protection	$V_{DD\text{-}rev}$	-14 -18		V	< 48h < 1h
Positive Output Voltage	V_{OUT}		28 34	V	< 48h < 1h
Reverse Output Voltage	$V_{OUT\text{-}rev}$	-14 -18		V	< 48h < 1h
Internal Voltage	V_{DEC}		3.6	V	< 1h
	$V_{DEC\text{-}rev}$	-0.3		V	< 1h
Positive $Test_1$ pin Voltage	V_{Test1}		6	V	< 1h
Reverse $Test_1$ pin Voltage	$V_{Test1\text{-}rev}$	-3		V	< 1h
Positive $Test_2$ pin Voltage	V_{test2}		3.6	V	< 1h
Reverse $Test_2$ pin Voltage	$V_{test2\text{-}rev}$	-0.3		V	< 1h
Operating Temperature	T_{AMB}	-40	+160	°C	
Junction Temperature	T_J		+175 +190	°C °C	See [1] < 100h
Storage Temperature	T_{ST}	-55	+170	°C	
Magnetic Flux Density	B_{max}	-1	1	T	

Table 9 - Absolute maximum ratings

Exceeding any of the absolute maximum ratings may cause permanent damage.
Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

5. Isolation Specification

The specified isolation resistance is only valid for the TSSOP-16 package (code GO).

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Isolation Resistance	R_{isol}	4	-	-	MΩ	Between dies, measured between V_{SS1} and V_{SS2} with +/-20V bias

Table 10 - Isolation specification

[1] *Find package thermal dissipation values in section 18.4*

6. General Electrical Specifications

General electrical specifications are valid for temperature range [-40, 160] °C and supply voltage range [4.5, 5.5] V unless otherwise noted.

Electrical Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply Voltage	V_{DD}	4.5	5	5.5	V	
Supply Current[2]	I_{DD}	7.5	8.5	10.0	mA	
Start-up Level (rising)	$V_{DDstartH}$	3.85	4.00	4.15	V	
Start-up Hysteresis	$V_{DDstartHyst}$		100		mV	
PTC Entry Level (rising)	V_{PROV0}	5.85	6.05	6.25	V	Supply overvoltage detection
PTC Entry Level Hysteresis	$V_{PROV0Hyst}$	100	175	250	mV	
Under voltage detection	V_{DDUVL}	3.75	3.90	4.05	V	Supply voltage low threshold
Under voltage detection hysteresis	$V_{DDUVHyst}$		100		mV	
Regulated Voltage	V_{DEC}	3.2	3.3	3.4	V	Internal analog voltage
External Pull-up Voltage	V_{ext}			18 V_{DD}	V	Output Pull-up voltage in open-drain NMOS mode or analog mode Output Pull-up voltage in Push-Pull mode

Table 11 - Supply System Electrical Specifications

Electrical Parameter	Symbol	Min	Typ	Max	Unit	Condition
Output Short Circuit Current Limit	$I_{OUTshort}$	10		35	mA	
Output Load	R_L	5	10		kΩ	Analog output
		5		100	kΩ	Digital output with Push-Pull PWM pull-up to V_{DD}, PWM pull-down to V_{SS}
		1.5 5 1.5		25 18 25	kΩ	Digital output with open-drain PMOS, pull-down to V_{SS} NMOS, pull-up to V_{ext} ≤ 18V NMOS, pull-up to V_{ext} = V_{DD}

[2] *For the dual die version, the supply current is multiplied by 2.*

Electrical Parameter	Symbol	Min	Typ	Max	Unit	Condition
Analog output Saturation Level	V_{satA_lo}		0.5[3] 3.3[3]	1.2[4] 7.4[4]	$\%V_{DD}$	Pull-up load $R_L \geq 10$ kΩ to $V_{ext} \leq V_{DD}$ Pull-up load $R_L \geq 5$ kΩ to $V_{ext} \leq 18$V
	V_{satA_hi}	97.0[4] 95.0[4]	99.0[3] 98.0[3]		$\%V_{DD}$	Pull-down load $R_L \geq 10$ kΩ to V_{SS} Pull-down load $R_L \geq 5$ kΩ to V_{SS}
Digital output with push-pull level	V_{satD_lopp}			1.2[4]	$\%V_{DD}$	Pull-up load $R_L \geq 10$ kΩ to $V_{ext} \leq V_{DD}$
	V_{satD_hipp}	97.0[4] 95.0[4]			$\%V_{DD}$	Pull-down load $R_L \geq 10$ kΩ to V_{SS} Pull-down load $R_L \geq 5$ kΩ to V_{SS}
Digital output with open-drain level	$V_{satLoOd}$	0		10	$\%V_{ext}$	Pull-up $V_{ext} \leq 18$V, $I_L \leq 3.4$mA
	$V_{satHiOd}$	90		100	$\%V_{DD}$	Pull-down V_{SS}, $I_L \leq 3.4$mA
Digital open-drain output leakage [5]	$I_{leakpuOd}$			100	µA	$V_{ext} > V_{DD}$, with a pull-up resistor
				20	µA	$V_{ext} = V_{DD}$, with a pull-up resistor
				20	µA	with a pull-down resistor to V_{SS}
Digital output Ron	R_{on}	27	50	130	Ω	
Passive Diagnostic Output Level (Broken-Wire Detection) [6]	$BV_{SS}PD$		1.2 0.5	4.0 1.6	$\%V_{DD}$	Broken V_{SS} & Pull-down load $R_L \leq 25$ kΩ to V_{SS} Pull-down load $R_L \leq 10$ kΩ to V_{SS}
	$BV_{SS}PU$	99.5	100		$\%V_{DD}$	Broken Vss & Pull-up load $R_L \geq 1$ kΩ to V_{DD}
	$BV_{DD}PD$		0	0.5	$\%V_{DD}$	Broken V_{DD} & Pull-down load $R_L \geq 1$ kΩ to V_{SS}
	$BV_{DD}PU$	92.5 97.0	98.7 99.5		$\%V_{DD}$	Broken V_{DD} & Pull-up load $R_L \leq 25$ kΩ to V_{DD} Pull-up load $R_L \leq 10$ kΩ to V_{DD}

Table 12 - Output Electrical specifications

[3] *at 35 °C and 5V supply voltage*

[4] *at 160 °C and ≥4.5V supply voltage*

[5] *The digital output level is determined by the external voltage and pull-up or pull-down resistor.*

[6] *Valid for dual-die configurations as well where the two dies have the same supply and ground level, while the output of one die is connected with PU and the output of the other one is connected with PD.*

7. Timing Specification

Timing specifications are valid for temperature range [-40, 160] °C and supply voltage range [4.5, 5.5] V unless otherwise noted.

7.1. General Timing Specifications

Parameter	Symbol	Min.	Typ	Max.	Unit	Condition
Main Clock Frequency	F_{CK}	22.8 -5	24	25.2 5	MHz $\%F_{ck}$	Including thermal and lifetime drift
Main Clock initial tolerances	$\Delta F_{CK,0}$	-1		1	$\%F_{ck}$	T=35°C, trimmed
Main Clock Frequency Thermal Drift	$\Delta F_{CK,T}$	-3.5		3.5	$\%F_{ck}$	Relative to clock frequency at 35°C. Ageing effect not included
1MHz Clock Frequency	F_{1M}	0.95 -5	1	1.05 5	MHz $\%F_{1M}$	Including thermal and lifetime drift
Intelligent Watchdog Timeout	T_{IWD}			20	ms	F_{CK} = 24MHz, IWD reporting time
Absolute Watchdog Timeout	T_{AWD}			20	ms	F_{1M} = 1MHz, AWD reporting time
Analog Diagnostics DCT	DCT_{ANA}			10.4	ms	Continuous Acquisition mode (7.2), applicable to analog and PWM.
Digital Diagnostics DCT	DCT_{DIG}			15.6	ms	
Fail Safe state duration[7]	T_{FSS}	5		33	ms	For digital single-event faults

Table 13 - General Timing Specifications

[7] *Fully programmable. Time between reset due to digital fault to first valid data transmission. Min. value defined by OUT_DIAG_HIZ_TIME (see Table 24 in chapter 12 for details).*

7.2. Continuous Acquisition Mode

In this mode, the sensor continuously acquires an angle at a fixed rate and updates its output when the information is ready. The acquisition rate is defined by the angle measurement period $T_{angleMeas}$. The PWM output frequency is asynchronous with regards to the angle measurement sequence and controlled by the T_FRAME parameter.

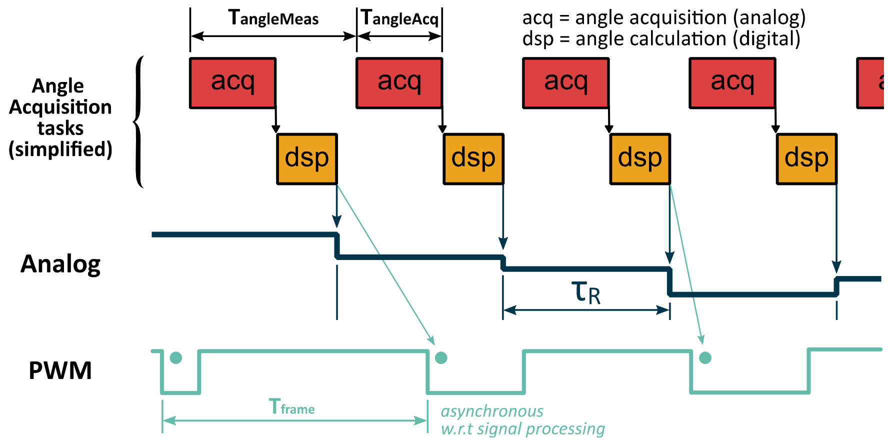


Figure 3 - Continuous Acquisition Timing Mode[8]

Parameter	Symbol	Min.	Typ	Max.	Unit	Condition
Angle acquisition time	$T_{angleAcq}$		192		µs	Default factory settings
Internal Angle Measurement Period	$T_{angleMeas}$		448		µs	Default factory settings

Table 14 - Continuous Acquisition Timing Mode

7.3. Timing Definitions

7.3.1. Startup Time

In analog mode, the start-up time τ_{SU} is defined by the duration between rising of the supply voltage and the output being set to the voltage level of the measured angle. During the start-up phase, the sensor output remains in a high impedance state. The output driver is enabled only when the sensor is able to transmit a valid angle.

In PWM mode, the start-up phase consists of three phases of durations $T_{stup[1:3]}$. The first phase ends when the sensor output leaves high impedance state and starts to drive a voltage. The end of the second phase T_{stup2} is reached when an angle is ready to be transmitted and indicated by the first synchronization edge of the PWM signal. The start-up phase is considered complete after T_{stup3} when the first angle has been transmitted, which happens one PWM period after T_{stup2}.

[8] *τ_R is defined in Table 15.*

These definitions are illustrated in the following figure (Figure 4) where τ_{init} represents the sensor internal initialization sequence.

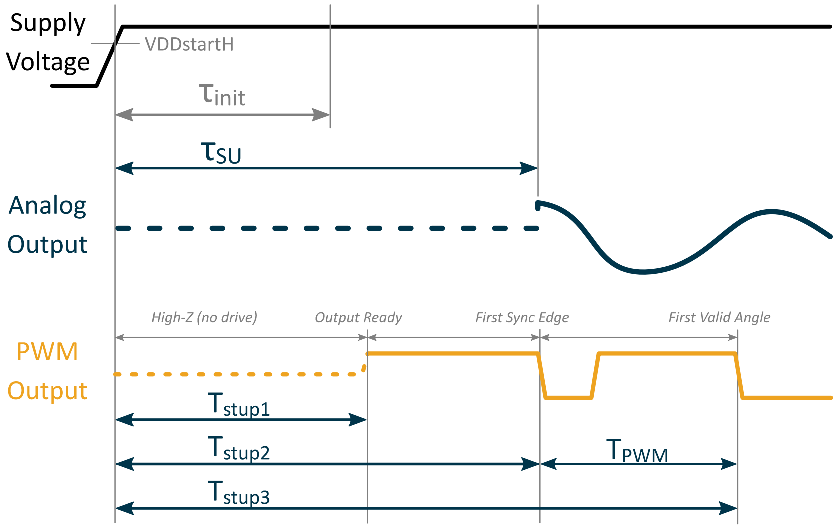


Figure 4 - Startup Time Definition

7.3.2. Latency (average)

Latency is the average lag between the movement of the detected object (magnet) and the response of the sensor output. This value is representative of the time constant of the MLX90421 for regulation calculations.

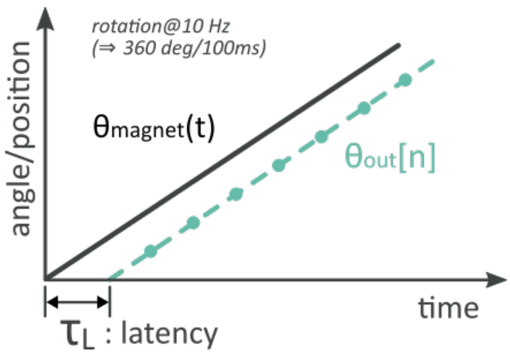


Figure 5 - Definition of Latency

7.3.3. Step Response (worst-case)

The Step Response τ_S is defined as the maximal delay between a change of position of the magnet and the 100% settling time of the sensor output, with full angle accuracy with regards to filtering. This worst-case is happening when the movement of the magnet occurs just after a measurement sequence has begun. The Step Response therefore consists of the sum of:

- $\delta_{mag,measSeq}$, the delay between a magnetic change and the start of the next measurement sequence
- $T_{angleMeas}$, the measurement sequence duration
- $\delta_{measSeq,trans}$, the delay between the end of the measurement sequence and the beginning of the transmission of the angle information
- T_{trans}, the duration of the transmission of the angle information, which depends on the protocol

For the worst-case, $\delta_{mag,measSeq} = T_{angleMeas}$. This gives:

$$\tau_S = 2T_{angleMeas} + \delta_{measSeq,frameStart} + T_{trans}$$

In analog output mode, the angle information is immediately available and the transmission delay is negligible. The last two terms of the above equation can be nulled. When using a PWM output protocol, the last two terms of the equation are, in the worst-case condition, both equal to a PWM frame duration T_{PWM}. The Figure 6 shows a practical case of a step response for both an analog and PWM output. This figure also defines the analog refresh period τ_R that is given in the table of the next section.

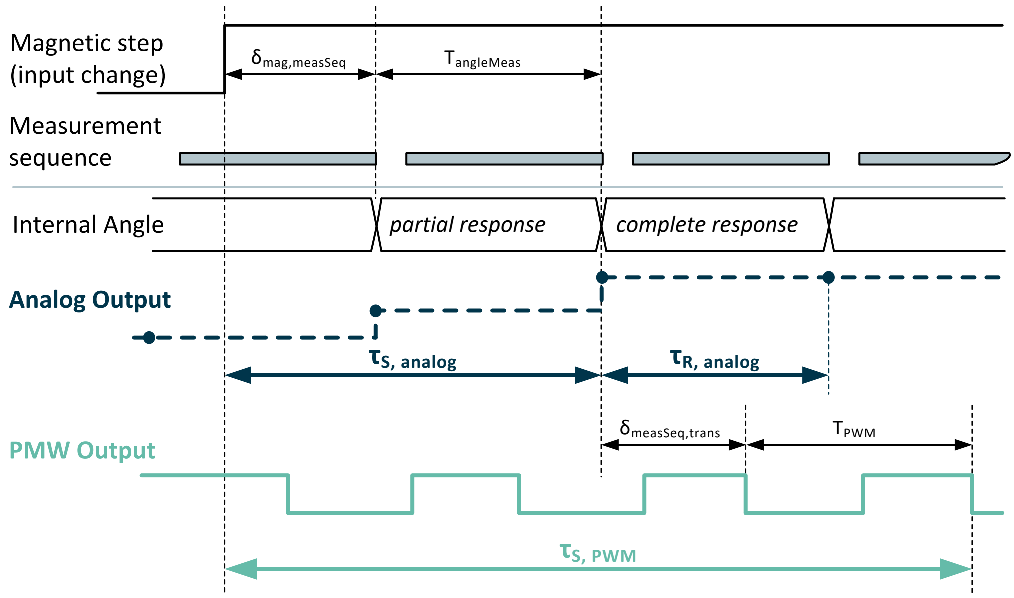


Figure 6 - Step Response Definition

7.4. Analog output timing specifications

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Output refresh period	τ_R		448	470	µs	Default factory setting
Latency	τ_L		228	240	µs	
Step response	τ_S		763 1211 2107	811 1282 2223	µs	Filter 0, Filter 1, Filter 2 (see 13.4 Filtering)
Start-up time	τ_{SU}		4.1	5.0	ms	
Safe startup Time	$T_{SafeStup}$			31	ms	Default factory setting OUT_DIAG_HIZ_TIME set to 15
Slew-rate	S_R			120 200	V/ms	C_{out} = 100nF C_{out} = 10nF

Table 15 - Analog Output Timing Specifications

7.5. PWM output timing specifications

For the parameters in below table, maximum timings correspond to minimal frequencies and vice versa.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
PWM Frequency	F_{PWM}	100		2000	Hz	
PWM Frequency Initial Tolerances	$\Delta F_{PWM,0}$	-1		1	$\%F_{PWM}$	T=35°C, can be trimmed at EOL
PWM Frequency Thermal Drift	$\Delta F_{PWM,T}$	-3.5		3.5	$\%F_{PWM}$	
PWM Frequency Drift	ΔF_{PWM}	-5		5	$\%F_{PWM}$	Over temperature and lifetime
PWM startup Time[9]	T_{stup1}		4.1		ms	Default factory setting Up to output ready
	T_{stup2}		5.2		ms	Default factory setting Up to first sync. Edge $T_{stup1} + T_{PWM}$
	T_{stup3}		6.3		ms	Default factory setting Up to first data received $T_{stup2} + T_{PWM}$
PWM Safe startup time				31	ms	Default factory setting up to first sync. Edge

Table 16 - PWM timing specifications

[9] Typical value specified according to the typical PWM frequency. Max. value can be obtained by scaling with the PWM frequency drift accordingly.

8. Magnetic Field Specifications

Magnetic field specifications are valid for temperature range [-40, 160] °C unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Number of magnetic poles	N_P		2			
Magnetic Flux Density in X-Y plane	B_x, B_y[10]			70	mT	$\sqrt{B_X^2 + B_Y^2}$
Magnetic Flux Density in Z	B_z			126	mT	in absolute value
Useful Magnetic Flux Density Norm	B_{Norm}	10[11]	20		mT	$\sqrt{B_X^2 + B_Y^2}$ (X-Y mode) $\sqrt{B_X^2 + \left(\frac{1}{G_{IMC}} B_Z\right)^2}$ (X-Z mode) $\sqrt{B_Y^2 + \left(\frac{1}{G_{IMC}} B_Z\right)^2}$ (Y-Z mode) see 13.3 for sensing mode description.
IMC gain[12]	G_{IMC}		1.19			
Magnet Temperature Coefficient	TC_m	-2400		0	$\frac{ppm}{°C}$	
Field Too Low Threshold	B_{TH_LOW}	2	4	30	mT	Typ. is recommended value to be set by user (see 13.5.4)
Field Too High Threshold[13]	B_{TH_HIGH}	70	126	126	mT	Typ. is recommended value to be set by user (see 13.5.4)

Table 17 - Magnetic specifications for Standard application

The magnetic performances are listed in chapter 9. The Figure 7 defined under which conditions nominal or limited performances apply.

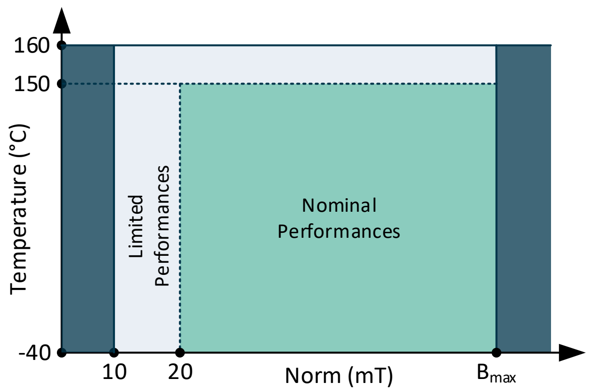


Figure 7 - Useful magnetic signal definition

[10] The condition must be fulfilled for all combinations of B_x and B_y.

[11] Only valid under the conditions of Figure 7. Outside of the "Limited Performances" zone, the performances are further degraded due to a reduction of the signal-to-noise ratio and signal-to-offset ratio.

[12] The IMC has a better performance for concentrating in-plane (X-Y) field components, resulting in a better overall magnetic sensitivity. A correction factor, called IMC gain has to be applied to the z field component to account for this difference.

[13] Due to the saturation effect of the IMC, the FieldTooHigh monitor detects only defects in the sensor

9. Accuracy Specifications

Accuracy specifications are valid for temperature range [-40, 160] °C and supply voltage range [4.5, 5.5] V unless otherwise noted.

9.1. Definitions

9.1.1. Intrinsic Linearity Error

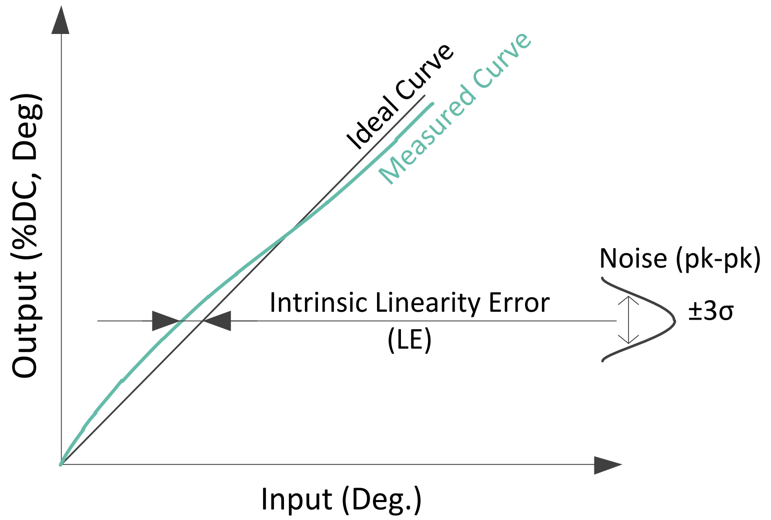


Figure 8 - Sensor accuracy definition

The illustration of Figure 8 depicts the intrinsic linearity error in new parts. The Intrinsic Linearity Error refers to the error sources of the IC (offset, sensitivity mismatch, orthogonality error) taking into account an ideal magnetic field. Once associated to a practical magnetic construction and its respective mechanical and magnetic tolerances, the output linearity error increases. The linearity error can be improved with the multi-point end-user calibration (see 13.2). As a consequence, this error is not the critical factor in application when it is calibrated away.

9.1.2. Total Angle Drift

After calibration, the output angle of the sensor might still change due to temperature change and aging. This error is defined as the total drift $\partial\theta_{TT}$:

$$\partial\theta_{TT} = \max\{\theta(\theta_{IN}, T, t) - \theta(\theta_{IN}, T_{RT}, t_0)\}$$

where θ_{IN} is the input angle, T is the temperature, T_{RT} is the room temperature, and t is the elapsed lifetime after calibration. t_0 represents the start of the sensor operating life. Note that the total drift $\partial\theta_{TT}$ is always defined with respect to the angle at room temperature. In this datasheet, T_{RT} is typically defined at 35°C unless stated otherwise. The total drift is valid for all angles along the full mechanical stroke.

9.2. Performances

9.2.1. Nominal Performances

Valid before EoL calibration and for all applications under nominal performances conditions described in chapter 6 and chapter 8.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
XY - Intrinsic Linearity Error	L_{E_XY}	-1		1	Deg.	
XZ - Intrinsic Linearity Error	L_{E_XZ}	-2.5		2.5	Deg.	
YZ - Intrinsic Linearity Error	L_{E_YZ}	-2.5		2.5	Deg.	
Noise [14]			0.1 0.15 0.1	0.2 0.35 0.2	Deg.	Filter = 0, $B_{Norm} \geq 40mT$ Filter = 0, $B_{Norm} \geq 20mT$ Filter = 2, $B_{Norm} \geq 20mT$
XY - Total Drift [15]	$\partial\theta_{TT\_XY}$	-0.6		0.6	Deg.	
XZ - Total Drift [15]	$\partial\theta_{TT\_XZ}$	-0.8		0.8	Deg.	Relative to 35°C
YZ - Total Drift [15]	$\partial\theta_{TT\_YZ}$	-0.8		0.8	Deg.	
Hysteresis				0.1	Deg.	$B_{Norm} \geq 20mT$

Table 18 - Nominal Magnetic Performances

9.2.2. Limited Performances

Valid before EoL calibration and for all applications under limited performances conditions described in chapter 6 and chapter 8.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
XY - Intrinsic Linearity Error	L_{E_XY}	-1		1	Deg.	
XZ - Intrinsic Linearity Error	L_{E_XZ}	-2.5		2.5	Deg.	
YZ - Intrinsic Linearity Error	L_{E_YZ}	-2.5		2.5	Deg.	
Noise [14]			0.15 0.3 0.55 0.15	0.25 0.45 0.8 0.25	Deg.	Filter = 0, $B_{Norm} \geq 40mT$ Filter = 0, $B_{Norm} \geq 20mT$ Filter = 0, $B_{Norm} \geq 10mT$ Filter = 2, $B_{Norm} \geq 20mT$
XY - Total Drift [15]	$\partial\theta_{TT\_XY}$	-0.8		0.8	Deg.	
XZ - Total Drift [15]	$\partial\theta_{TT\_XZ}$	-1.0		1.0	Deg.	Relative to 35°C
YZ - Total Drift [15]	$\partial\theta_{TT\_YZ}$	-1.0		1.0	Deg.	
Hysteresis				0.2	Deg.	$B_{Norm} \geq 10mT$

Table 19 - Limited Magnetic Performances

14 ±3σ

15 Verification done on new and aged devices in an ideal magnetic field. An additional application-specific error arises from the non-ideal magnet and mechanical tolerance drift.

10. Memory Specifications

Parameter	Symbol	Value	Unit	Note
ROM	ROM_{size}	16	kB	1 bit parity check per 32bits word (single error detection)
RAM	RAM_{size}	512	B	1 bit parity check per 16bits word (single error detection)
NVRAM	$NVRAM_{size}$	128	B	6 bits ECC per word 16b (single error correction, double error detection)

Table 20 - Memory Specifications

11. Output Protocol Description

11.1. Analog Output Description

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Thermal analog output Drift				0.2	%VDD	
Analog Output Resolution	R_{DAC}		12		bit	12bit DAC (theoretical)
		-4		+4	LSB12	INL (before EoL calibration), output between 3-97%VDD
		-1.5		1.5	LSB12	DNL
Ratiometric Error		-0.05 -0.1		0.05 0.1	%VDD	$4.5V \leq V_{DD} \leq 5.5V$ $V_{DDUVL} \leq V_{DD} \leq V_{PROV0}$

Table 21 - Analog Output Accuracy

11.2. PWM Output Description

11.2.1. Definition

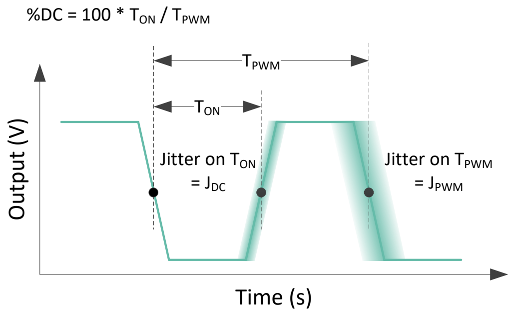


Figure 9 - PWM Signal definition

Parameter	Symbol	Test Conditions
PWM period	T_{PWM}	Trigger level = 50% V_{DD}
Rise time, Fall time	t_{rise}, t_{fall}	Between 10% and 90% of V_{DD}
Jitter	J_{DC} J_{PWM}	±3σ for 1000 successive acquisitions with clamped output
Duty Cycle	%DC	100 * T_{ON} / T_{PWM}

Table 22 - PWM Signal definition

11.2.2. PWM performances

Parameter	Symbol	Min	Typ	Max	Unit	Condition
PWM period	T_{PWM}	0.5		10	ms	Configurable through the T_FRAME parameter
PWM Output Resolution	R_{PWM}		0.024		%DC/LSB12	
PWM %DC Jitter	J_{DC}			0.03	%DC	C_{OUT} = 10nF, R_L = 10kΩ Push-pull, 2KHz
PWM Period Jitter	J_{PWM}			500	ns	2KHz, PWM_LOW_SR=0
PWM %DC thermal drift			0.02	0.05	%DC	C_{OUT} = 10nF, R_L = 10kΩ Push-pull, 2KHz
Rise/Fall Time PWM	T_{rise_fall}	2.5	5.0	7.5	µs	Fast slope[16], Cout ≤ 15nF[17][18] Push-pull or open-drain
	T_{rise_fall}	3.7	8	12	µs	Slow slope[16], Cout ≤ 22nF Push-pull or open-drain

Table 23 - PWM Signal Specifications

[16] *The fast and slow slope configuration can be controlled through the PWM_LOW_SR parameter (see Table 24 in chapter 12)*

[17] *The 10nF output capacitor included in the DMP, SMP-3 and SMP-4 packages need to be taken into account in the 15nF limit.*

[18] *If the total load current at the output is high enough to trigger the current limit protection, then the slopes will be determined by the maximum output current drive of around 15mA (typical value).*

12. End-User Programmable Items

Parameter	PSF value	Description	Default Value	# bits
		GENERAL CONFIGURATION		
USER_ID[0:5]	113 .. 118	Reserve for end-user to program information to keep traceability, unless the patch area is used	-	8
WARM_TRIGGER_LONG	106	Add delay for PTC entry level	0	1
MUPET_ADDRESS	110	PTC address for which the slave will communicate	0/1	2
		SENSOR FRONT-END		
GAINMIN	2	Virtual Gain min	0	6
GAINMAX	3	Virtual Gain max	48	7
GAINSATURATION	4	Gain saturation enable	0	1
SENSING_MODE	16	0: X-Y Angular Rotary 1: Y-Z Angular Rotary / Y Linear Position 2: X-Z Angular Rotary / X Linear Position 3: Do not use	0	2
		FILTERING		
FILTER	11	FIR filter bandwidth selection 0: no filter (default) 1: FIR11 2: FIR1111 3: Do not use	0	2
		LINEAR TRANSFER CHARACTERISTIC		
4POINTS	10	Enable 4 points PWL linearization	0	1
CLAMPHIGH	18	High clamping value of angle output data	50%	12
CLAMPLOW	13	Low clamping value of angle output data	50%	12
CW	14	Magnet rotation direction	0	1
DP	9	DSP discontinuity point	0	13
LNRS0	21	4-pts - Slope coefficient before reference point A	-	16
LNRAX LNRBX LNRCX LNRDX	25 37 50 64	4-pts - X Coordinate for reference points A,B,C,D	-	16
LNRAY LNRBY LNRCY LNRDY	29 42 55 69	4-pts - Y Coordinate for reference points A,B,C,D	-	16

Parameter	PSF value	Description	Default Value	# bits
LNRAS LNRBS LNRCS LNRDS	33 46 60 71	4-pts - Slope coefficient for reference points A,B,C,D	-	16
LNRY0 LNRY1 LNRY2 LNRY3 LNRY4 LNRY5 LNRY6 LNRY7 LNRY8 LNRY9 LNRY10 LNRY11 LNRY12 LNRY13 LNRY14 LNRY15 LNRY16	24 27 32 36 40 45 49 53 59 63 67 70 74 79 84 88 92	17-pts / 16 segments - Y coordinate point [0:16]	10% 15% 20% 25% 30% 35% 40% 45% 50% 55% 60% 65% 70% 75% 80% 85% 90%	12
OUTSLOPE_COLD	94	Slope coefficient at cold of the programmable temperature-dependent offset	0	8
OUTSLOPE_HOT	95	Slope coefficient at hot of the programmable temperature-dependent offset	0	8
USEROPTION_SCALING	15	Enable output scaling 2x after linearization	0	1
WORK_RANGE	111	Working Range 17 points	0	4
WORK_RANGE_GAIN	6	Post DSP Gain Stage	16	8
		DIAGNOSTICS		
COLD_SAFE_STARTUP_EN	56	Normal (0) or safe start-up (1) after power-on reset	0	1
DIAG_EN	44	Diagnostics global enable. **Do not modify!**	1	1
DIAG_FIELDTOOHIGHTHRES	77	Field strength limit over which a fault is reported	14	4
DIAG_FIELDTOOLOWTHRES	76	Field strength limit under which a fault is reported	0	4
DIAGDEBOUNCE_STEPDOWN	30	Diagnostic debouncing step-down time used for recovery time setting	1	2
DIAGDEBOUNCE_STEPUP	31	Diagnostic debouncing step-up time used for hold time setting	1	2
DIAGDEBOUNCE_THRESH	43	Diagnostic debouncing threshold	1	3
MEMLOCK	58	Enable NVRAM write protection	0	2

Parameter	PSF value	Description	Default Value	# bits
OUT_DIAG_HIZ_TIME	103	Recovery time when a transient digital failure is detected. Timeout = (5 + OUT_DIAG_HIZ_TIME) * 1ms	15	5
PWM_DC_FAULT_BAND	99	PWM Upper or Lower band for analog fault reporting	0	1
PWM_DC_FAULT_VAL	98	PWM Duty Cycle in case of analog fault	0	3
PWM_DC_FIELDTOOLOW_BAND	81	PWM Upper or Lower band for analog fault reporting in case of Field Strength Too Low	-	1
PWM_DC_FIELDTOOLOW_VAL	82	PWM Duty Cycle in case of Field Strength Too Low	-	3
ROUT_LOW	104	Select output impedance for PTC communication	1	1
OUTPUT CONFIGURATION				
ABE_OUT_MODE	105	HW backend output-amplifier mode selection: 0: Analog output (12-bit DAC) 1: Digital output with open-drain-NMOS 2: Digital output with open-drain-PMOS 3: Digital output with Push-Pull	0	2
PROTOCOL	107	Selection of the measurement timing mode and the corresponding output protocol: 0: continuous synchronous angle acquisition, analog output 1: continuous asynchronous angle acquisition, PWM output	0	1
T_FRAME	97	Output PWM period PWM period = 4us * T_FRAME	266	12
PWM_LOW_SR	112	Enables slow PWM slopes	0	1
PWM_POL	101	Invert the PWM polarity	0	1

Table 24 - MLX90421 End-User Programmable Items Table

Performances described in this document are only achieved by adequate programming of the device. To ensure desired functionality, Melexis recommends to follow its programming guide and to contact its technical or application service.

13. Description of End-User Programmable Items

13.1. Output modes and protocols

The MLX90421 offers an analog output mode and a digital output mode using the PWM protocol.

13.1.1. Output Modes

The parameter ABE_OUT_MODE defines the output stage mode (outside of fail-safe state) in application.

ABE_OUT_MODE	Description	Comments
0	Analog output (12-bit DAC)	Default
1	Digital output with open-drain NMOS	Requires a pull-up resistor on output.
2	Digital output with open-drain PMOS	Requires a pull-down resistor on output.
3	Digital output with push-pull	

Table 25 - Output mode selection

13.1.2. Protocol

The parameter PROTOCOL defined the measurement timings mode and the corresponding output protocol.

PROTOCOL	Description
0	Continuous synchronous angle acquisition, analog output (DAC)
1	Continuous asynchronous angle acquisition, PWM

Table 26 - Protocol selection

13.1.3. PWM Protocol

If a digital output mode is selected, the output signal is a Pulse Width Modulation (PWM) digital signal.

The PWM polarity is selected by the PWM_POL parameter:

- PWM_POL = 0 for a low level at 100%
- PWM_POL = 1 for a high level at 100%

The PWM frequency is selected in the range [100, 2000] Hz by the T_FRAME parameter (12bits), defining the period time in the range [0.5, 10] ms. Minimum allowed value for T_FRAME is therefore 125 (0x7d).

$$T_{PWM} = \frac{4}{10^6} \times T\_FRAME$$

The PWM slope is configurable through the parameter PWM_LOW_SR. When set to 0, fast PWM slopes are selected. Conversely, when set to 1, slow PWM slopes are selected to reduce conducted EMC emissions on the output.

PWM timings specifications in the scope of the MLX90422 can be found in section 7.5 while PWM signal characteristics such the rise time, fall times, jitter, can be found in section 11.2.

13.2. Output Transfer Characteristic

There are 2 different possibilities to define the transfer function (LNR) as specified in Table 27.

- With 4 arbitrary points (defined by X and Y coordinates) and 5 slopes
- With 17 equidistant points for which only the Y coordinates are defined

Output Transfer Characteristic	4POINTS
4 Arbitrary Points	1
17 Equidistant Points	0

Table 27 - Output Transfer Characteristic Selection Table

13.2.1. Clockwise Parameter

The CW parameter defines the magnet rotation direction.

Rotation Direction	CW
Clockwise	1
Counter Clockwise	0

Table 28 - Magnet Rotation Selection Table

Counter clockwise is the defined by

- the 1-4-5-8 pin order direction for the SOIC-8 package
- the 1-8-9-16 pin order direction for the TSSOP-16 package
- the 1-2-3-4 pin order direction for the DMP-4 package
- the 1-2-3 pin order direction for the SMP-3 package
- the 1-2-3-4 pin order direction for the SMP-4 package

Clockwise if defined by the reverse pin order. Refer to the package drawings in chapter 18.

13.2.2. Discontinuity Point (or Zero Degree Point)

The Discontinuity Point defines the 0° point on the circle. The discontinuity point places the origin at any location of the trigonometric circle. The DP is used as reference for all the angular measurements.

$$\text{New Angle} = \text{Angle} - DP$$

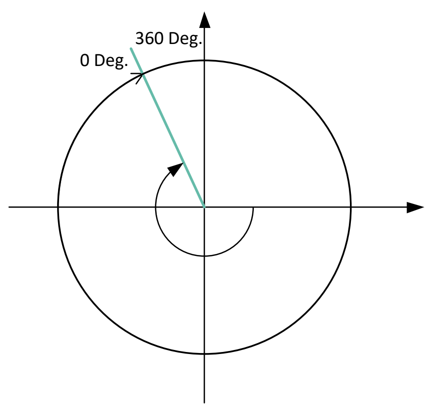


Figure 10 - Discontinuity Point Positioning

13.2.3. 4-Pts LNR Parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital angle and the output signal.

The shape of the MLX90421 four points transfer function from the digital angle value to the digital output is described in the following figure (Figure 11). Seven segments can be programmed but the clamping levels are necessarily flat.

Two to six calibration points are available, reducing the overall non-linearity of the IC by almost an order of magnitude each time. Three or more calibration point will be preferred by customers looking for excellent non-linearity figures. Two-point calibrations will be preferred by customers looking for a cheaper calibration set-up and shorter calibration time.

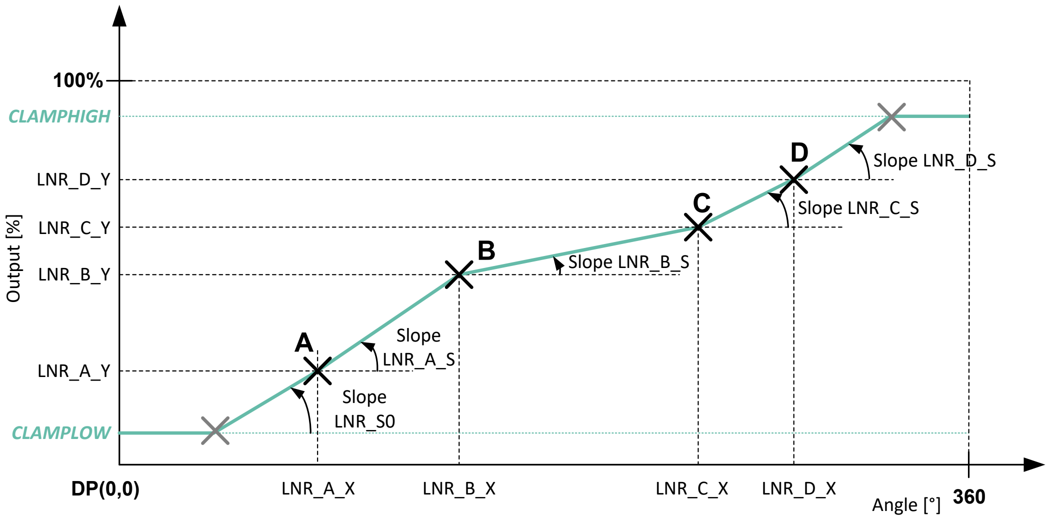


Figure 11 - 4pts Linearization Parameters Description

13.2.4. 17-Pts LNR Parameters

The LNR parameters, together with the clamping values, fully define the relation (the transfer function) between the digital angle and the output signal.

The shape of the MLX90421 seventeen points transfer function from the digital angle value to the output voltage is described in the Figure 12. In the 17-Pts mode, the output transfer characteristic is Piecewise Linear (PWL).

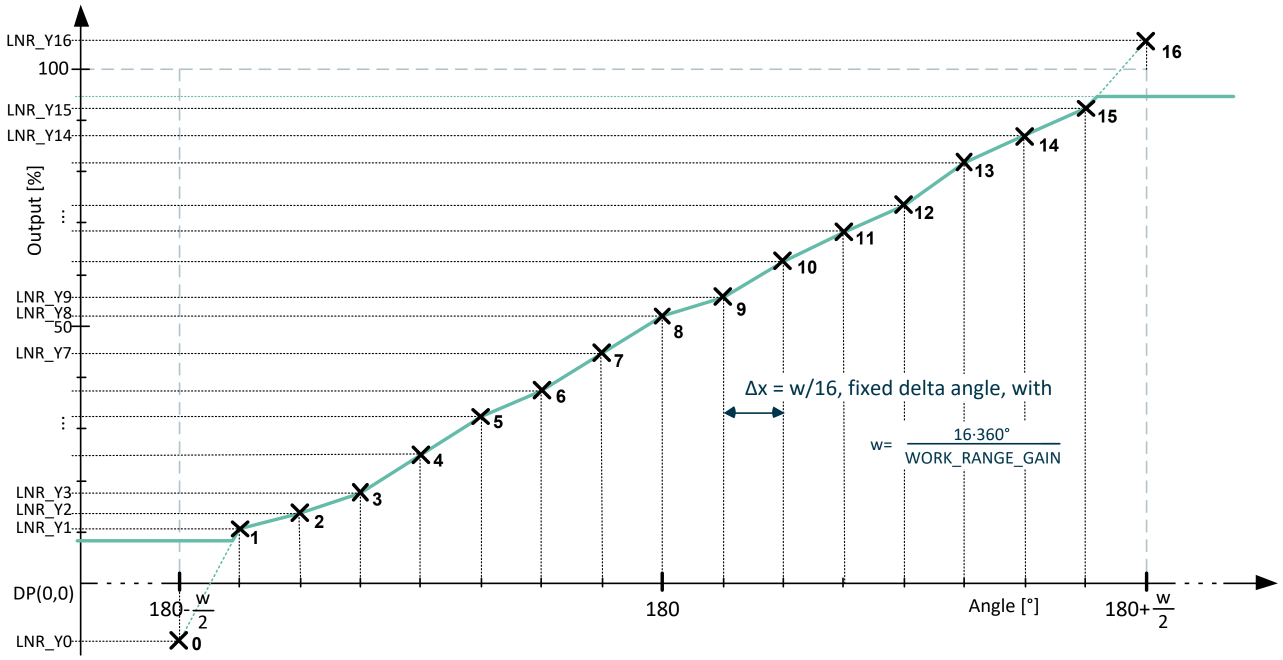


Figure 12 - 17pts Linearization Parameters Description

All the Y-coordinates can be programmed from -50% up to +150% to allow clamping in the middle of one segment (like on the figure), but the output value is limited to CLAMPLOW and CLAMPHIGH values.

Between two consecutive points, the output characteristic is interpolated.

13.2.5. WORK_RANGE Parameter for Angle Range Selection

The parameter WORK_RANGE determines the input range on which the 16 segments are uniformly spread. This parameter is provided for compatibility with former versions of Melexis Triaxis sensors.

For full featured working range selection, see section 13.2.6. For WORK_RANGE parameter, following table applies.

WORK_RANGE	Range	Δx 17pts	WORK_RANGE	Range	Δx 17pts
0	360.0°	22.5°	8	180.0°	11.3°
1	320.0°	20.0°	9	144.0°	9.0°
2	288.0°	18.0°	10	120.0°	7.5°
3	261.8°	16.4°	11	102.9°	6.4°
4	240.0°	15.0°	12	90.0°	5.6°
5	221.5°	13.8°	13	80.0°	5.0°
6	205.7°	12.9°	14	72.0°	4.5°
7	192.0°	12.0°	15	65.5°	4.1°

Table 29 - Work range for 360° periodicity

Outside of the selected range, the output will remain at clamping levels.

13.2.6. WORK_RANGE_GAIN Parameter for Angle Range Selection

Alternatively, the range for the angle can be selected using the WORK_RANGE_GAIN parameter, which applies a fixed gain to the transfer characteristics. WORK_RANGE_GAIN is coded on 8 bits where the 4 MSB defines the integer part and the 4 LSB the fractional part (in power of twos). Therefore, the following equation applies to define the angle range *w*:

$$w = \frac{16 * 360}{WORK\_RANGE\_GAIN}$$

Both minimal and maximal angles are then defined by:

$$\theta_{min} = \frac{360 - w}{2} \; ; \; \theta_{max} = \frac{360 + w}{2}$$

where θ_{min} corresponds to the angle yielding 0% output and θ_{max} the angle giving a 100% output.

Using WORK_RANGE_GAIN parameter, the anchor point is kept at *180* and the range is symmetrically set around this value. It creates a zoom-in of the angle around this point.

Following tables give some values as example:

GAIN	Factor	Range (w)	θmin	θmax	Δx 17pts
0x10	1	360°	0°	360°	22.5°
0x20	2	180°	90°	270°	11.3°
0x40	4	90°	135°	225°	5.6°
0xFF	15.94	22.6°	168.7°	191.3°	1.41°

Table 30 - Working range defined by WORK_RANGE_GAIN parameter

Outside of the working range, the output will remain at clamping levels.

13.2.7. Clamping Parameters

The clamping levels are two independent values to limit the output voltage range in normal operation. The CLAMPLOW parameter adjusts the minimum output level. The CLAMPHIGH parameter sets the maximum output level. Both parameters have 12 bits of adjustment and are available for all four LNR modes. The values are encoded in fractional code, from 0% to 100%

13.3. Sensor Front-End

Parameter	Value
SENSING_MODE	[0:2]
GAINMIN	[0:47]
GAINMAX	[0:47]
GAINSATURATION	[0:1]

Table 31 - Sensing Mode and Front End Configuration

The SENSING_MODE parameter defines which sensing mode and fields are used to calculate the angle. The different possibilities are described in the tables below. This 2-bit value selects the first (B1) and second (B2) field components according to the Table 32 content.

SENSING_MODE	B1	B2	Motion
0	X	Y	X-Y Angular Rotary
1	Y	Z	Y-Z Angular Rotary / Y Linear Position
2	X	Z	X-Z Angular Rotary / X Linear Position

Table 32 - Sensing Mode Description

GAINMIN and GAINMAX define the thresholds on the virtual gain code outside which the fault “GAIN out of Spec.” is reported.

If GAINSATURATION is set, then the virtual gain code is saturated at GAINMIN and GAINMAX, and no Diagnostic fault is set since the saturations applies before the diagnostic is checked.

13.4. Filtering

The MLX90421 features 2 low-pass FIR filter modes controlled with FILTER = 1…2. FILTER = 0 corresponds to no filtering. The transfer function is described by:

$$y_n = \frac{1}{\sum_{i=0}^{j} a_i} \sum_{i=0}^{j} a_i x_{n-i}$$

This filter characteristic is given in the Table 33.

FILTER	0	1	2
Type	Disable	Finite Impulse Response (FIR)	
Coefficients a_i	1	11	1111
Title	No filter	ExtraLight	Light
DSP cycles (j= nb of taps)	1	2	4
Efficiency RMS (dB)	0	3.0	6.0

Table 33 - FIR Filter Characteristics

13.5. Programmable Diagnostics Settings

13.5.1. Diagnostics Global Enable

DIAG_EN should be kept to its default value (1) to retain all functional safety abilities of the MLX90421. This feature shall not be disabled.

13.5.2. Diagnostic Debouncer

A debouncing algorithm is available for analog diagnostic reporting. Enabling this debouncer will increase the FHTI of the device. Therefore, Melexis recommends keeping the debouncing of analog faults off by not modifying below described values. The factory default settings mentioned in chapter 12 should be used.

Parameter	Description
DIAGDEBOUNCE_STEPDOWN	Decrement values for debouncer counter. The counter is decremented once per evaluation cycle when no analog fault is detected.
DIAGDEBOUNCE_STEPUP	Increment value for debouncer counter. The counter is incremented once per evaluation cycle when an analog fault is detected.
DIAGDEBOUNCE_THRESH	Threshold for debouncer counter to enter diagnostic mode. When set to 0, debouncing is off and analog faults are reported immediately after detection.

Table 34 - Diagnostic debouncing parameters

Once an analog monitor detects an error, it takes control of the debouncing counter. This counter will be incremented by DIAGDEBOUNCE_STEPUP value each time this specific monitor is evaluated and the error is still present. When the debouncing counter reaches the value defined by DIAGDEBOUNCE_THRESH, an error is reported on the error channel, and the debouncing counter stays clamped to this DEBOUNCE_THRESH value (see section 13.5.5 for PWM error reporting). Once the error disappears, each time its monitor is evaluated, the debouncing counter is decremented by DIAGDEBOUNCE_STEPDOWN value. When the debouncing counter reaches zero, the error disappears from the reporting channel and the debouncing counter is released. To implement proper reporting times, one should refer to the FHTI, see chapter 14.3. The reporting and recovery time are defined in the table below (valid for DIAGDEBOUNCE_THRESH > 0).

Parameter	Min	Max
Reporting Time	$DCT \cdot \left(\left\lceil \frac{THRESH}{STEPUP} \right\rceil - 1\right)$	$DCT \cdot \left(\left\lceil \frac{THRESH}{STEPUP} \right\rceil\right)$
Recovery Time	$DCT \cdot \left(\left\lceil \frac{THRESH}{STEPDOWN} \right\rceil\right)$	$DCT \cdot \left(\left\lceil \frac{THRESH}{STEPDOWN} \right\rceil + 1\right)$
	$\left\lceil \frac{x}{y} \right\rceil$	is the ceiling function of x divided by y

Table 35 - Diagnostic Reporting and Recovery times

13.5.3. Over/Under Temperature Diagnostic

DIAG_TEMP_THR_HIGH defines the threshold for over temperature detection and is compared to the linearized value of the temperature sensor T_{LIN}. DIAG_TEMP_THR_LOW defines the threshold for under temperature detection and is compared to the linearized value of the temperature sensor T_{LIN}.

One can get the physical temperature of the die using following formula

$$T_{PHY}[°C] = \frac{T_{LIN}}{8} - 73.15$$

DIAG_TEMP_THR_LOW/HIGH are encoded on 8-bit unsigned values with the following relationship towards T_{Lin}

$$DIAG\_TEMP\_THR\_(LOW/HIGH) = \frac{T_{LIN}}{16}$$

In the MLX90421, the parameter DIAG_TEMP_THR_LOW and DIAG_TEMP_THR_HIGH are fixed to 8 (-57°C) and 136 (199°C) respectively.

The following table summarizes the characteristics of the linearized temperature sensor and the encoding of the temperature monitor thresholds.

Parameter	Symbol	Min	Typ	Max	Unit	Condition
T_{LIN} resolution	Res_{TLIN}	-	0.125	-	°C	12-bit range
T_{LIN} refresh rate	$F_{S,TLIN}$	-	200	-	Hz	
T_{LIN} linearity error	T_{LinErr}	-10	-	10	°C	from -40 to 160°C
High temperature threshold	DIAG_TEMP_THR_LOW	-	8	-	LSB12	Fixed value, corresponds to -57°C
Low temperature threshold	DIAG_TEMP_THR_HIGH	-	136	-	LSB12	Fixed value, corresponds to 199°C
High/low temperature threshold resolution	Res_{Tthr}	-	2	-	°C	12-bit range

Table 36 - Linearized Temperature Sensor characteristics

13.5.4. Field Strength and Field Monitoring Diagnostics

Field Strength is compensated over the circuit operating temperature range and represents a reliable image of the field intensity generated by the magnet.

13.5.5. Analog mode diagnostic reporting

When in analog mode, a digital fault is reported by configuring the OUT pin in high-impedance. Conversely, an analog fault is reported by pulling the OUT pin to the V_{satD_Iopp} low level (refer to Table 12).

This behavior is only valid for the factory default settings. Other reporting behaviors and further information on the safe-states are available in the safety manual of the MLX90421.

13.5.6. PWM mode diagnostic reporting

When in PWM mode, a digital fault is reported by configuring the OUT pin in high-impedance.

When reporting an analog fault, the parameter PWM_DC_FAULT_BAND and PWM_DC_FAULT_VAL can be used to specify the 12-bits output level. The parameter PWM_DC_FAULT_BAND is used to define the BAND within which the output level is set.

PWM_DC_FAULT_BAND	Description
0	The Low band [0:CLAMPLOW] is selected
1	The High band [CLAMPHIGH:4095] is selected

Table 37 - Output level band selection in case of an analog fault

The parameter PWM_DC_FAULT_VAL selects a value in the specified band

$$\text{Low band output level} = PWM\_DC\_FAULT\_VAL \cdot \left(\frac{CLAMPLOW}{8}\right)$$

$$\text{High band output level} = 4095 - PWM\_DC\_FAULT\_VAL \cdot \left(\frac{CLAMPHIGH}{8}\right)$$

Correspondingly, the parameters PWM_DC_FIELDTOOLOW_BAND and PWM_DC_FIELDTOOLOW_VAL can be used to specify the 12-bits output level in case of a field strength too low event.

This reporting behavior is only valid for the factory default settings, with the exception of the aforementioned parameters in this section. Other reporting behaviors and further information on the safe-states are available in the safety manual of the MLX90421.

14. Functional Safety

14.1. Safety Manual

The safety manual, available upon request, contains the necessary information to integrate the MLX90421 component in a safety related item, as a Safety Element Out-of-Context (SEooC).

In particular, it includes:

- The description of the Product Development lifecycle tailored for the Safety Element.
- An extract of the Technical Safety concept.
- The description of Assumptions-of-Use (AoU) of the element with respect to its intended use, including:
    - assumptions on the device safe state;
    - assumptions on fault tolerant time interval and multiple-point faults detection interval;
    - assumptions on the context, including its external interfaces;
- The description of safety analysis results (at the device level, to be used for the system integration), HW architectural metrics and description of dependent failures initiators.
- The description and the result of the functional safety assessment process; list of confirmation measures and description of the independency level.

14.2. Safety Mechanisms

The MLX90421 provides numerous self-diagnostic features (safety mechanisms). Those features increase the robustness of the IC functionality either by preventing the IC from providing an erroneous output signal or by reporting the failure.

Legend
● High coverage
○ Medium coverage
ANA: Analog hardware failure reporting mode, described in the safety manual
High-Z: A special failure reporting mode where the output is set in high-impedance mode (no HW fail-safe mode/timeout, no SW safe startup)
DIG: Digital hardware failure reporting mode, described in the safety manual
At Startup: A HW fault present at time zero is detected before the first frame is transmitted.
DIAG_EN: This safety mechanism can be disabled by setting DIAG_EN = 0 (see chapter 13.5.1). This option should not be used in application mode!

Table 38 - Self Diagnostic Legend

Category and safety mechanism name	Front-end	ADC	DSP	Back-end	Support. Func.	Module & Package	Reporting mode	At startup	DIAG EN
Signal-conditioning (AFE, External Sensor) Diagnostic	●	●				●			
Magnetic Signal Conditioning Voltage Test Pattern	●	○	○				ANA	NO	●
Magnetic Signal Conditioning Rough Offset Clipping check	●		○				ANA	NO	●
Magnetic Signal Conditioning Gain Monitor	●		○			●	ANA	YES	●
Magnetic Signal Conditioning Gain Clamping	●		○			●	ANA	YES	●
Mag. Sig. Cond. Failure control by the chopping technique	●						n/a	YES	
A/D Converter Test Pattern		●					ANA	NO	●
ADC Conversion errors & Overflow Errors		●					ANA	YES	●
ADC Common Mode monitor		●					ANA	YES	
Flux Monitor (Rotary mode)	●	○				●	ANA	NO	●

Category and safety mechanism name	Front-end	ADC	DSP	Back-end	Support. Func.	Module & Package	Reporting mode	At startup	DIAG EN
Digital-circuit Diagnostic		○	●		○				
RAM Parity, 1 bit per 16 bits word, ISO D.2.5.2			●				DIG	YES	●
ROM Parity, 1 bit per 32 bits word, ISO D.2.5.2			●				DIG	YES	●
NVRAM 16 bits signature (run-time) ISO D.2.4.3, by means of SW CRC-CCITT16			●				DIG	NO	●
NVRAM Double Error Detection ECC ISO D.2.4.1			●				DIG	YES	
Logical Monitoring of program sequence ISO D.2.9.3 via Watchdog "IWD" (CPU clock) ISO D.2.9.2			●		○		DIG	NO	●
Watchdog "AWD" (separate clock) ISO D2.9.1			●		○		DIG	YES	
CPU Errors "Invalid Address", "Wrong opcode"			●		○		DIG	YES	
ADC Interface Checksum		●					DIG	NO	●
DSP Test Pattern (atan2)			●		○		DIG	NO	●
Critical ports monitoring			●				DIG	NO	●
ADC data adder test - range check		○					DIG	YES	●
DSP Overflow	○	○	●				ANA	n/a	●

Category and safety mechanism name	Front-end	ADC	DSP	Back-end	Support. Func.	Module & Package	Reporting mode	At startup	DIAG EN
System-level diagnostic					●	●			
Supply Voltage Monitors (all supply domains) except VS_OV & POR					●	●	ANA	YES	●
External Supply Overvoltage Monitor VS_OV					●	●	High-Z	YES	
Digital Supply under-voltage monitor (Power-on reset)					●	●	DIG	YES	
Overheating monitor	○	○	○	○	○	●	ANA	YES	●
Warning/Reporting Mechanisms									
HW Error Controller			●	●	●		DIG	YES	
HW Fail-safe mode with timeout			●	●	●		DIG	YES	
Analog-type Error management	●	●			●		ANA	NO	●
Safe start-up mode			●		●		DIG	n/a	
Mechanisms executed at start-up only									
RAM March-C HW Test at start-up			●		●		DIG	YES	

Table 39 - MLX90421 List of Self Diagnostics with Characteristics

14.3. Fault Handling Time Interval

The Fault handling Time Interval (FHTI) is the time interval between the start of the first frame with invalid position value without notice, and the end of the last frame preceding a fail-safe state of the IC.

The following table provides the worst-case FHTI for both an analog fault and a digital fault in MLX90421.

Case	FHTI	Comment
Analog Fault	$DCT_{ANA} + 2\ \tau_R$	Refer to section 7.1 for the DCT_{ANA} value and to section 7.4 for the τ_R value.
Digital Fault	DCT_{DIG}	Refer to section 7.1 for the DCT_{DIG} value.

Table 40 – Worst-case FHTI

The FHTI values provided here are valid only for the default factory settings. A full list of timings is available in the safety manual of the MLX90421, including cycle times, execution times and reporting times for every implemented safety mechanism.

15. Recommended Application Diagrams

15.1. Wiring with the MLX90421 in SOIC-8 Package

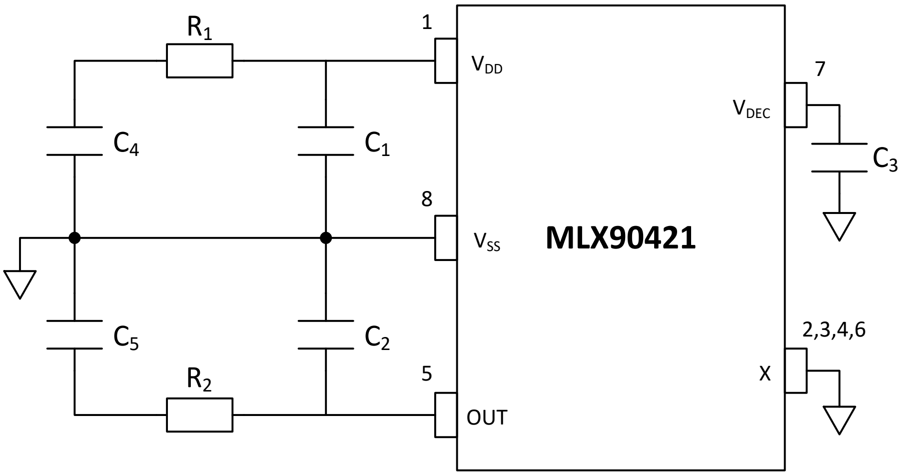


Figure 13 - Recommended wiring for the MLX90421 in SOIC-8 package

Component	Min	Typ.	Max	Remark
C_1	-	220 nF	-	
$C_2(C_L)$	10 nF 4.7 nF	10 nF 4.7 nF	100 nF 22 nF	Analog output PWM output
C_3	-	100 nF	220 nF	
C_4	-	-	1 nF	Optional, for improved EMC robustness
C_5	-	-	1 nF	
R_1	-	-	10 Ω	
R_2	-	-	-	

Table 41 - Recommended Values for the MLX90421 in SOIC-8 Package

For best EMC performance, C_1, C_2 and C_3 with typical values need to be placed as close as possible to the IC. To further improve EMC robustness, a 1nF capacitor can be placed close to the connector (C_4, C_5) and a 10 Ohm resistor added in series with the supply line (R_1).

15.2. Wiring with the MLX90421 in TSSOP-16 Package

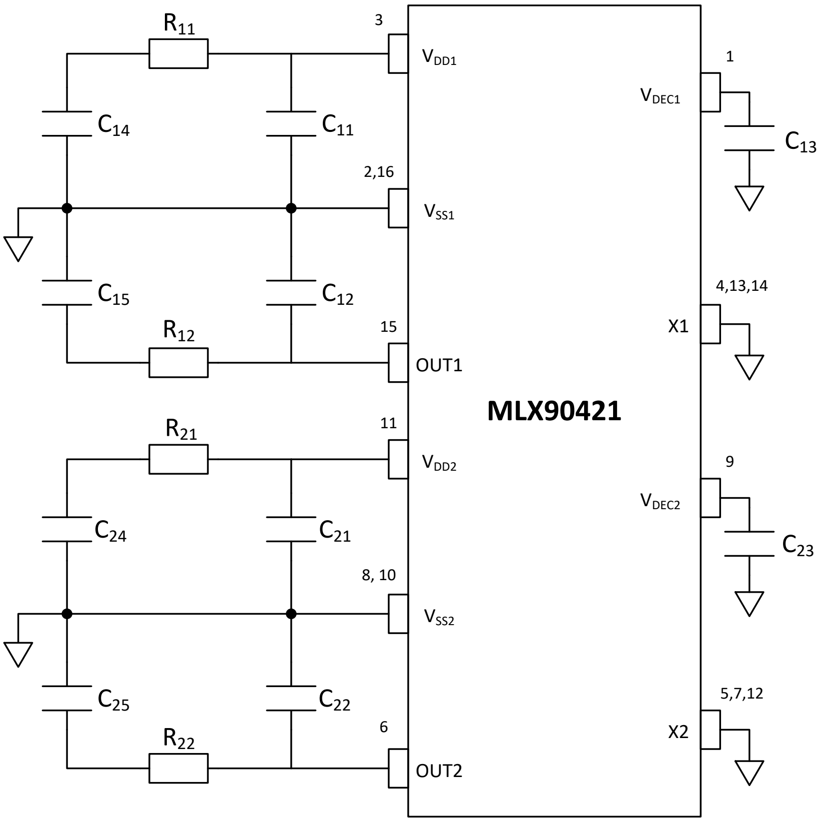


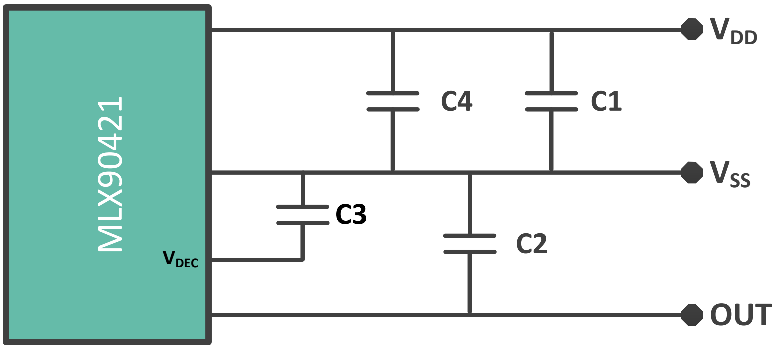
Figure 14 - Recommended wiring for the MLX90421 in TSSOP-16 package (dual die)

Component	Min	Typ.	Max	Remark
C_{x1}	-	220 nF	-	
$C_{x2}(C_L)$	10 nF 4.7 nF	10 nF 4.7 nF	100 nF 22 nF	Analog output PWM output
C_{x3}	-	100 nF	220 nF	
C_{x4}	-	-	1 nF	Optional, for improved EMC robustness
C_{x5}	-	-	1 nF	
R_{x1}	-	-	10 Ω	
R_{x2}	-	-	-	

Table 42 - Recommended Values for the MLX90421 in TSSOP-16 Package

For best EMC performance, C_{x1}, C_{x2} and C_{x3} with typical values need to be placed as close as possible to the IC. To further improve EMC robustness, a 1nF capacitor can be placed close to the connector (C_{x4}, C_{x5}) and a 10 Ohm resistor added in series with the supply line (R_{x1}).

15.3. Wiring with the MLX90421 in DMP-4 Package (built-in capacitors)



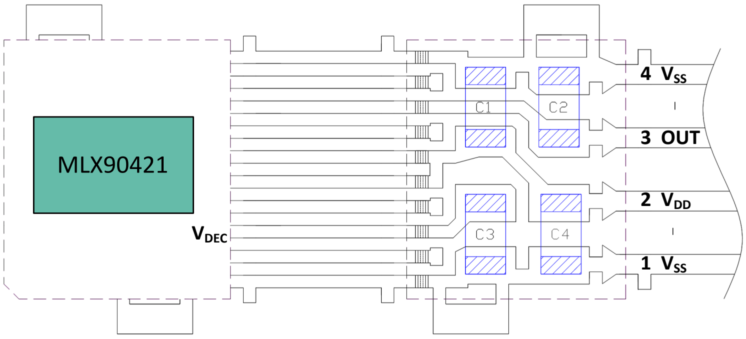


Figure 15 - Internal wiring of the MLX90421 in DMP-4

Component	Value	Remark
C1	220 nF	Supply capacitor
C2	10 nF	Output capacitor
C3	100 nF	Decoupling capacitor
C4	-	Not mounted

Table 43 - DMP-4 capacitors configuration

15.4. Wiring with the MLX90421 in SMP-3 Package (built-in capacitors)

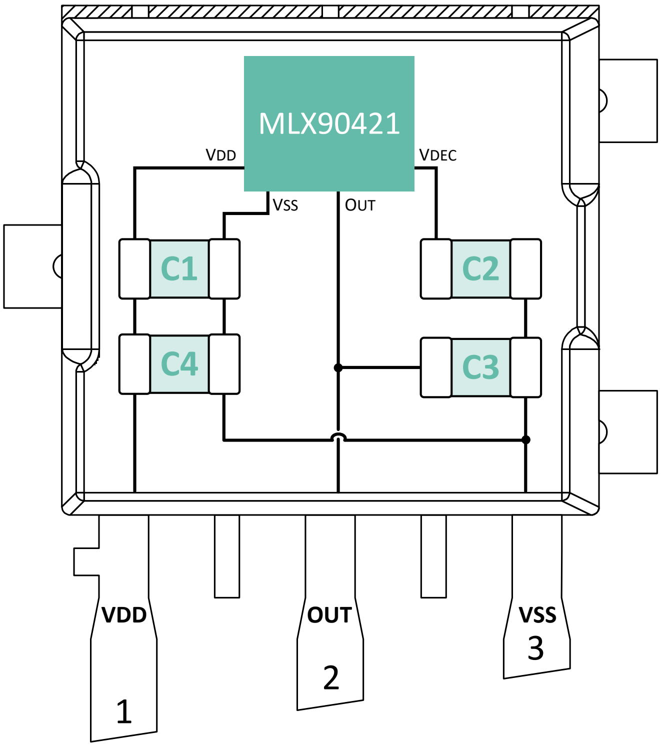


Figure 16 - Internal wiring of the MLX90421 in SMP-3

Component	Value	Remark
C1	220nF	Supply capacitor
C2	100nF	Decoupling capacitor
C3	10nF	Output capacitor
C4	-	Not mounted

Table 44 - SMP-3 capacitors configuration

15.5. Wiring with the MLX90421 in SMP-4 Package (built-in capacitors)

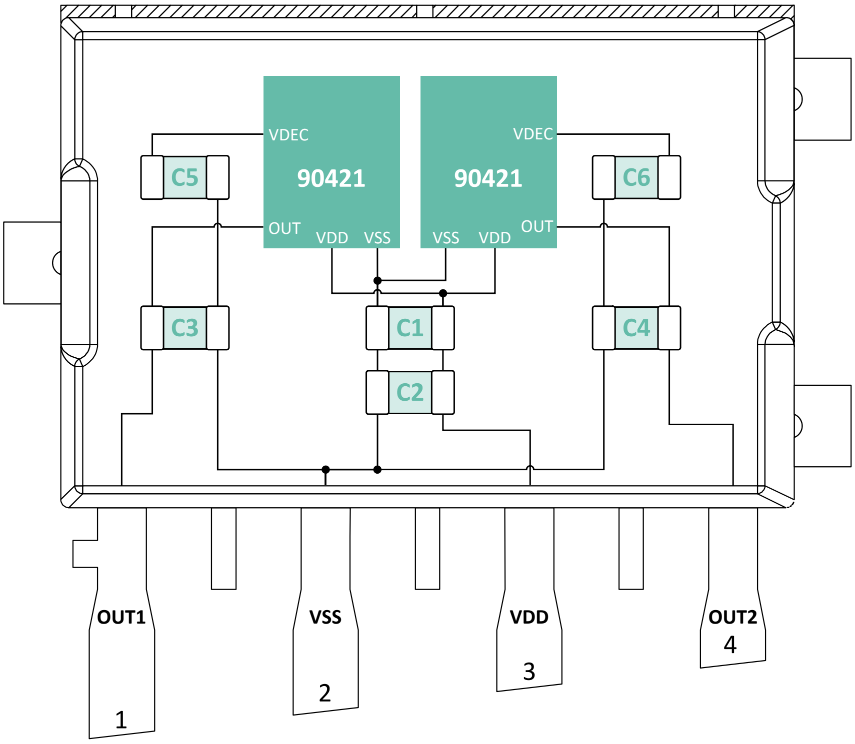


Figure 17 - Internal wiring of the MLX90421 in SMP-4

Component	Value	Remark
C1 C2	220nF	Supply capacitor
C3 C4	10nF	Output capacitor
C5 C6	100nF	Decoupling capacitor

Table 45 - SMP-4 capacitors configuration

16. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to standards in place in Semiconductor industry.

For further details about test method references and for compliance verification of selected soldering method for product integration, Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/en/quality-environment/soldering)

For all soldering technologies deviating from the one mentioned in above document (regarding peak temperature, temperature gradient, temperature profile, etc.), additional classification and qualification tests have to be agreed upon with Melexis.

For package technology embedding trim and form post-delivery capability, Melexis recommends consulting the dedicated trim & form recommendation application note : “Lead Trimming and Forming Recommendations” (http://www.melexis.com/en/documents/documentation/application-notes/lead-trimming-and-forming-recommendations).

Melexis is contributing to global environmental conservation by promoting lead free solutions. For more information on qualifications of RoHS compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/en/quality-environment.

17. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).

Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

18. Package Information

18.1. SOIC-8 - Package Information

18.1.1. SOIC-8 - Package Dimensions

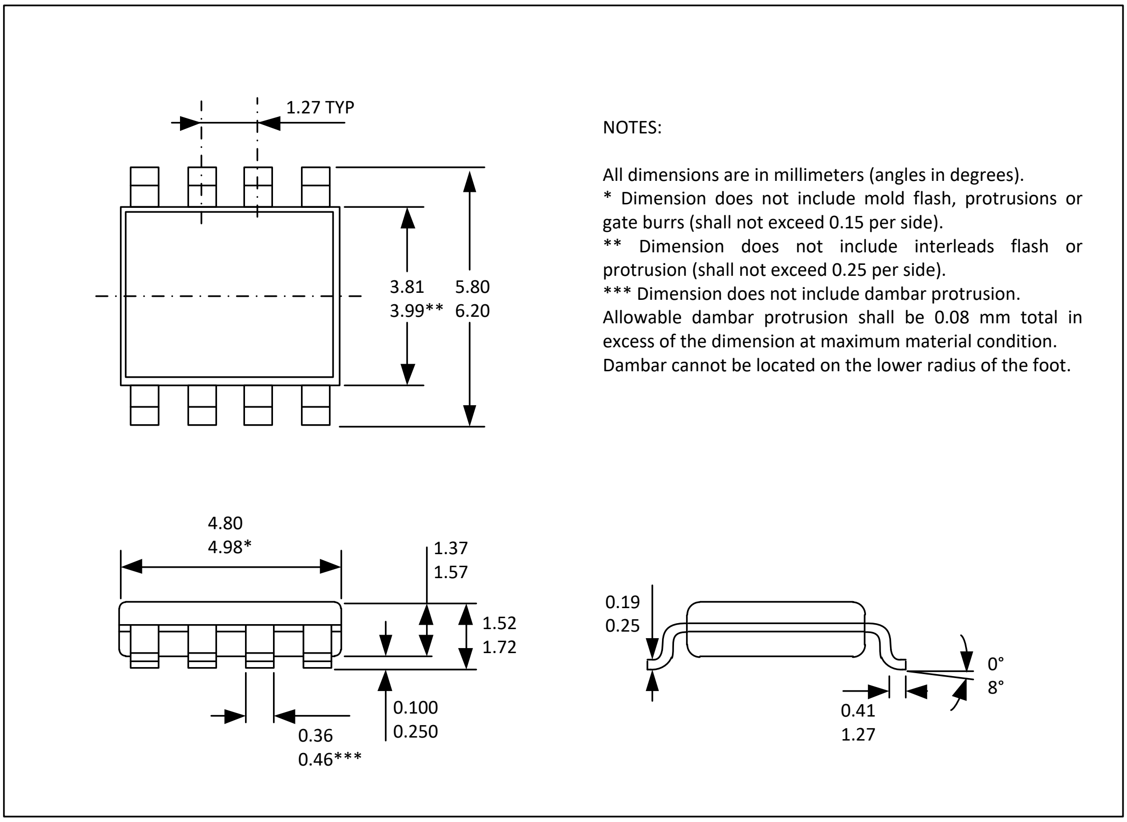


Figure 18 - SOIC-8 Package Outline Drawing

18.1.2. SOIC-8 - Pinout and Marking

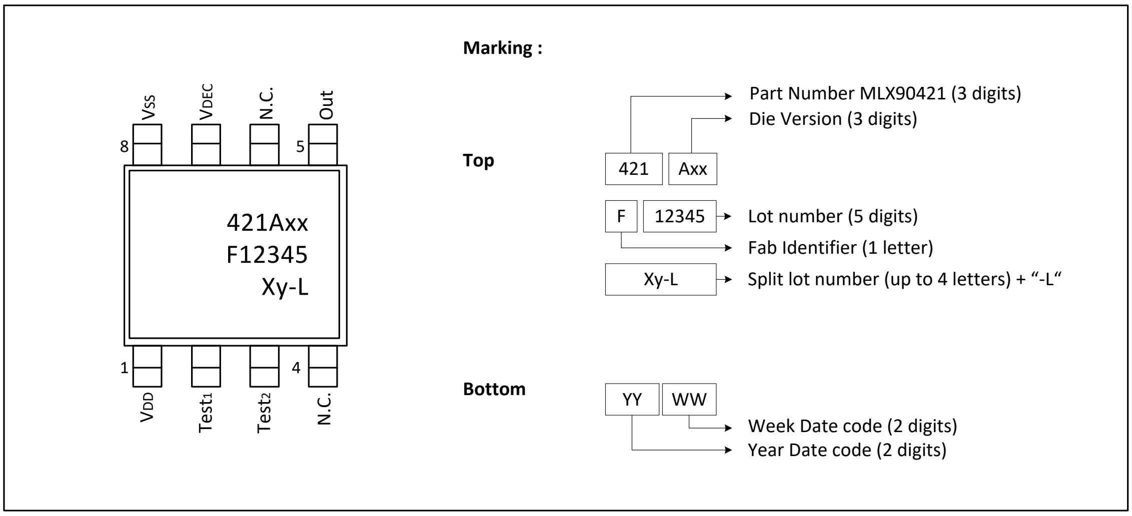


Figure 19 - SOIC-8 Pinout and Marking

18.1.3. SOIC-8 - Sensitive Spot Positioning

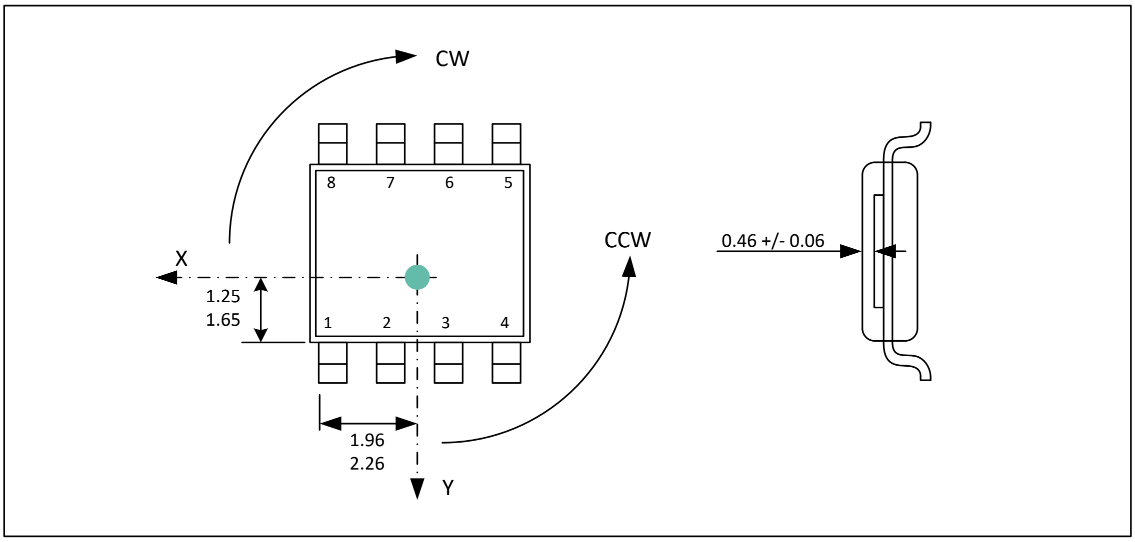


Figure 20 - SOIC-8 Sensitive Spot Position

18.1.4. SOIC-8 - Angle Detection

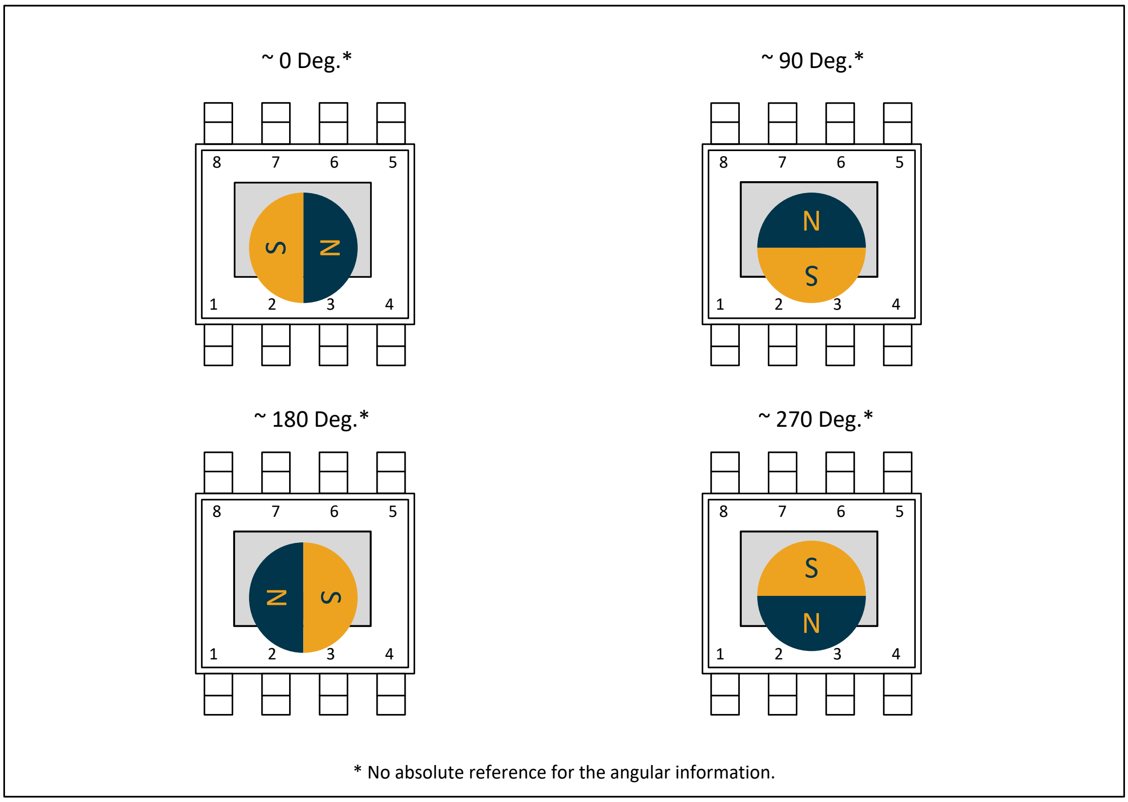
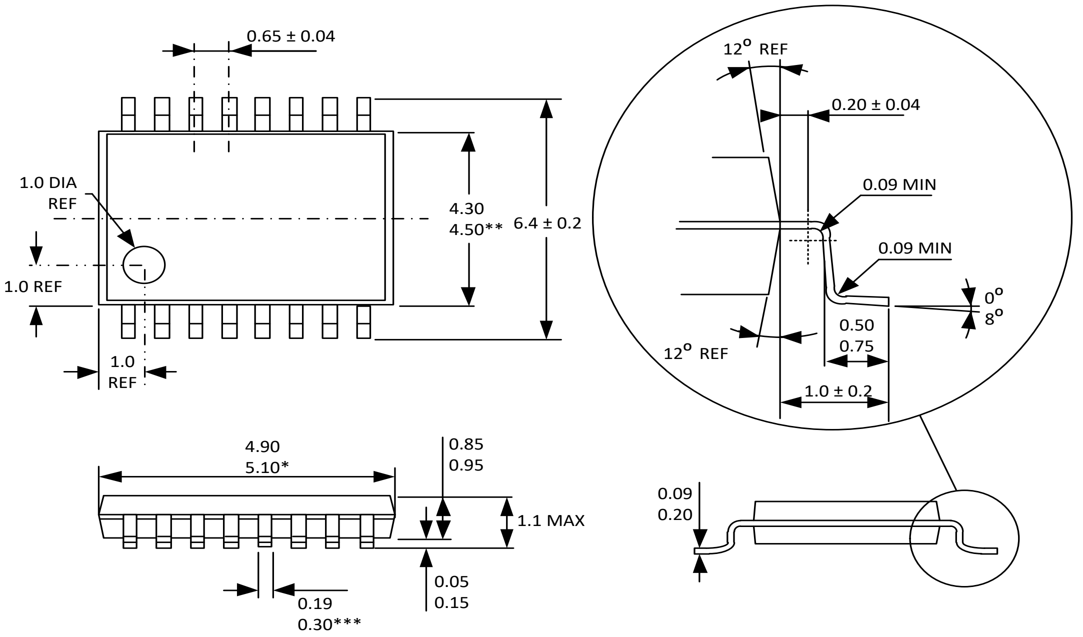


Figure 21 - SOIC-8 Angle Detection

The MLX90421 is an absolute angular position sensor but the linearity error (See section 9) does not include the error linked to the absolute reference 0 Deg. This reference can be fixed in the application through the discontinuity point.

18.2. TSSOP-16 - Package Information

18.2.1. TSSOP-16 - Package Dimensions



NOTES:

All dimensions are in millimeters (angles in degrees).
* Dimension does not include mold flash, protrusions or gate burrs (shall not exceed 0.15 per side).
** Dimension does not include interleads flash or protrusion (shall not exceed 0.25 per side).
*** Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot.
REF: Reference dimensions as stated in packaging supplier POD, based on JEDEC.

Figure 22 - TSSOP-16 Package Outline Drawing

18.2.2. TSSOP-16 - Pinout and Marking

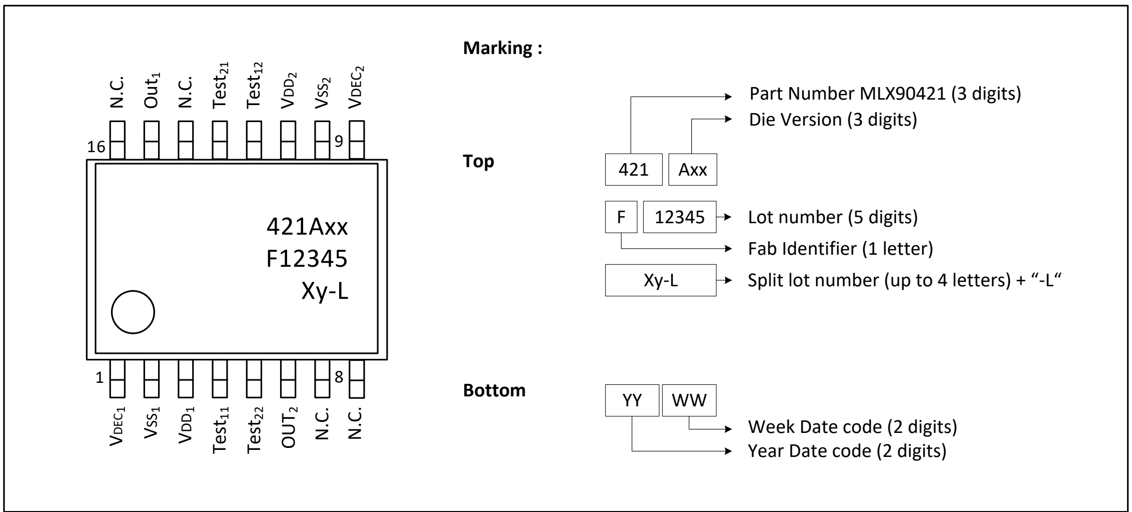


Figure 23 - TSSOP-16 Pinout and Marking

18.2.3. TSSOP-16 - Sensitive Spot Positioning

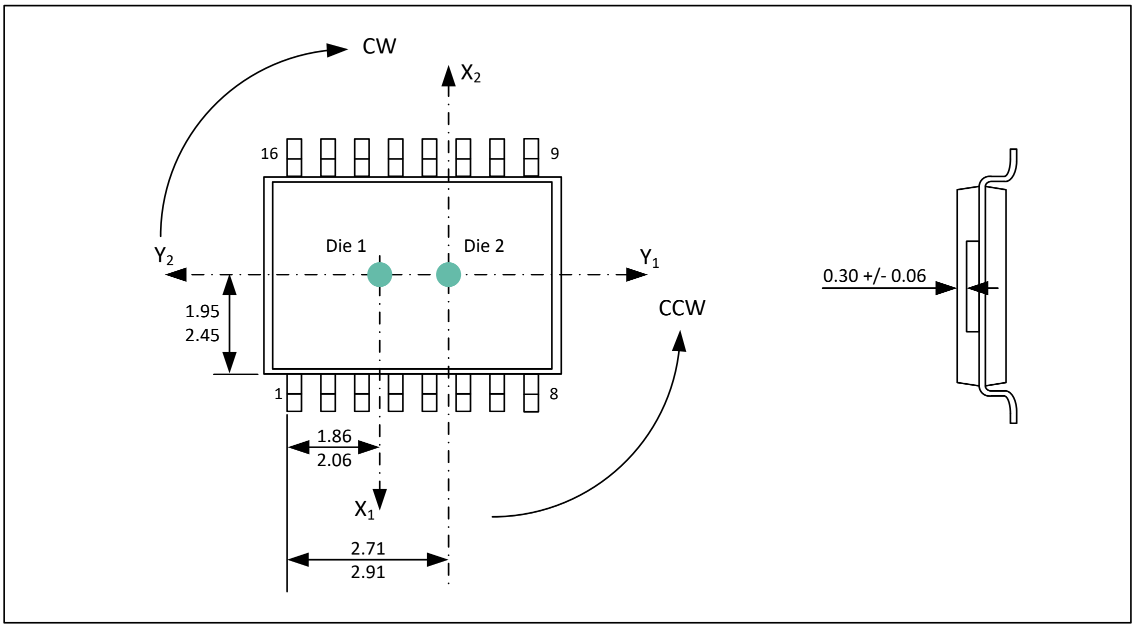


Figure 24 - TSSOP-16 Sensitive Spot Position

18.2.4. TSSOP-16 - Angle Detection

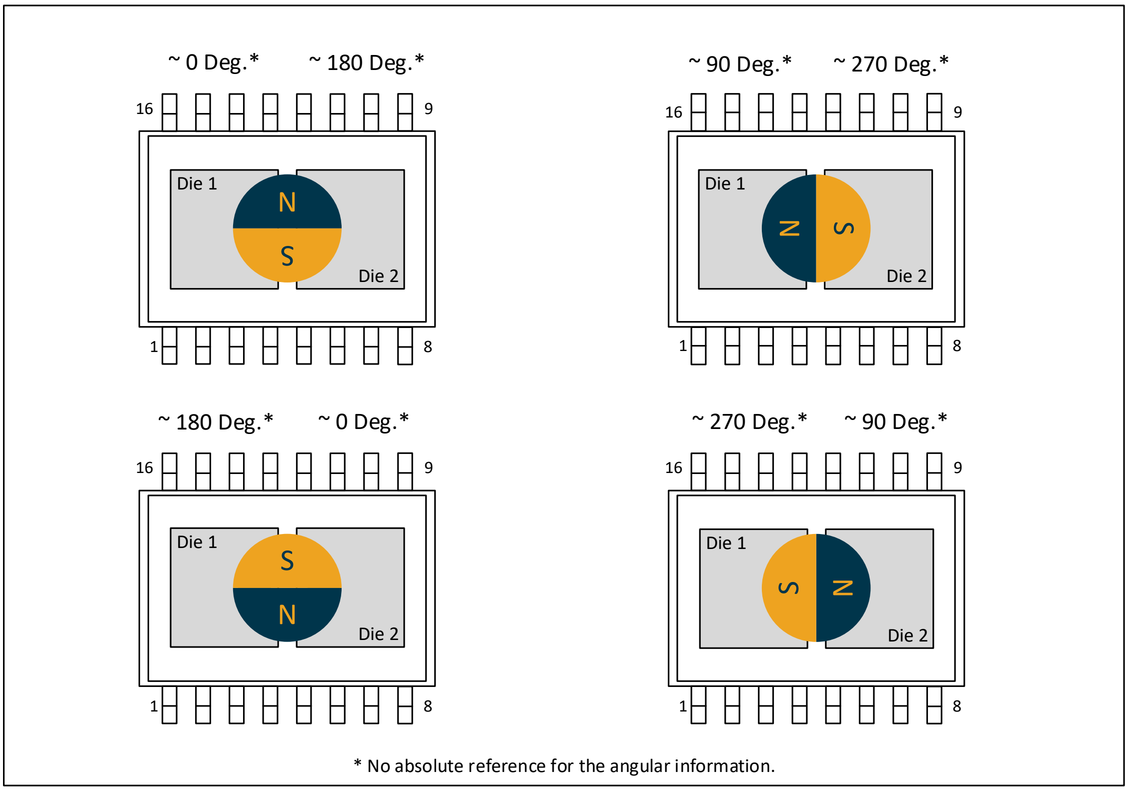


Figure 25 - TSSOP-16 Angle Detection

The MLX90421 is an absolute angular position sensor but the linearity error (See section 9) does not include the error linked to the absolute reference 0 Deg. This reference can be fixed in the application through the discontinuity point.

18.3. DMP-4 - Package Information

18.3.1. DMP-4 - Package Outline Dimensions (POD) - Straight Leads

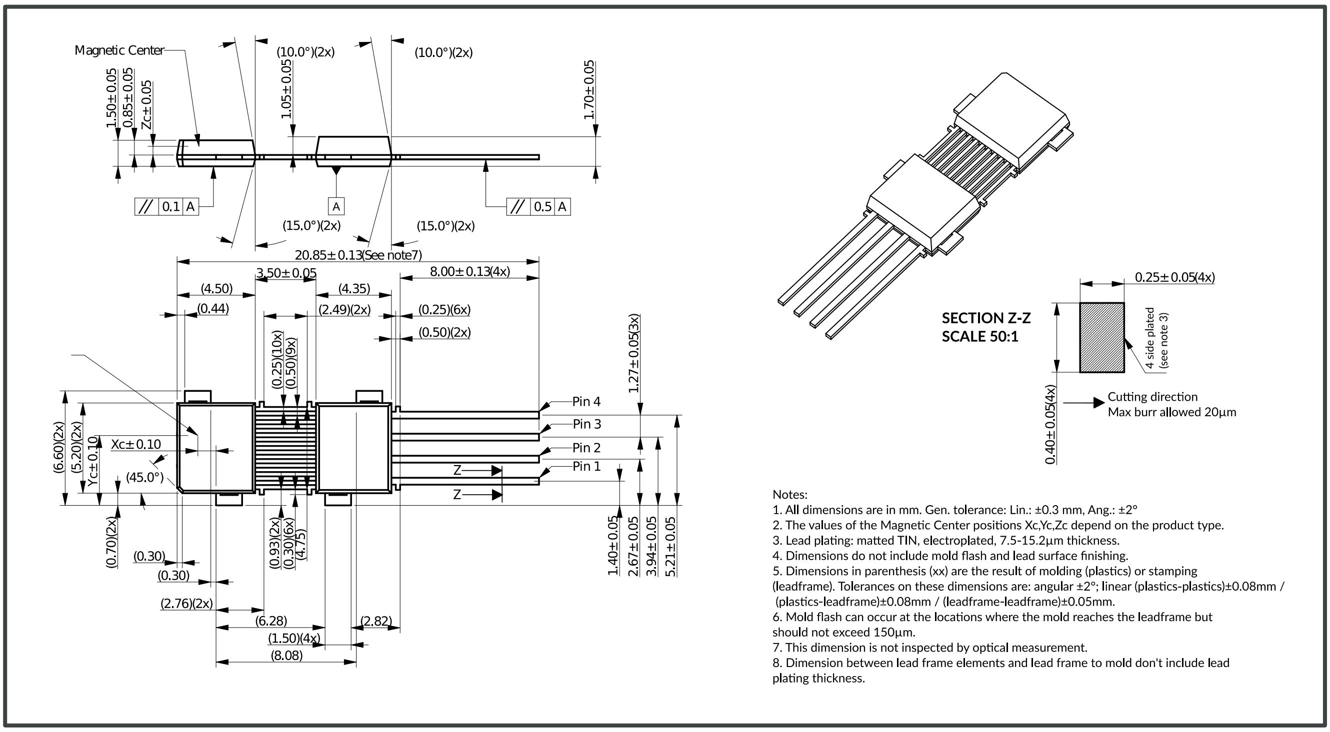


Figure 26 - DMP-4 Straight Leads Package Outline Drawing

18.3.2. DMP-4 - Package Outline Dimensions (POD) - STD2 2.54

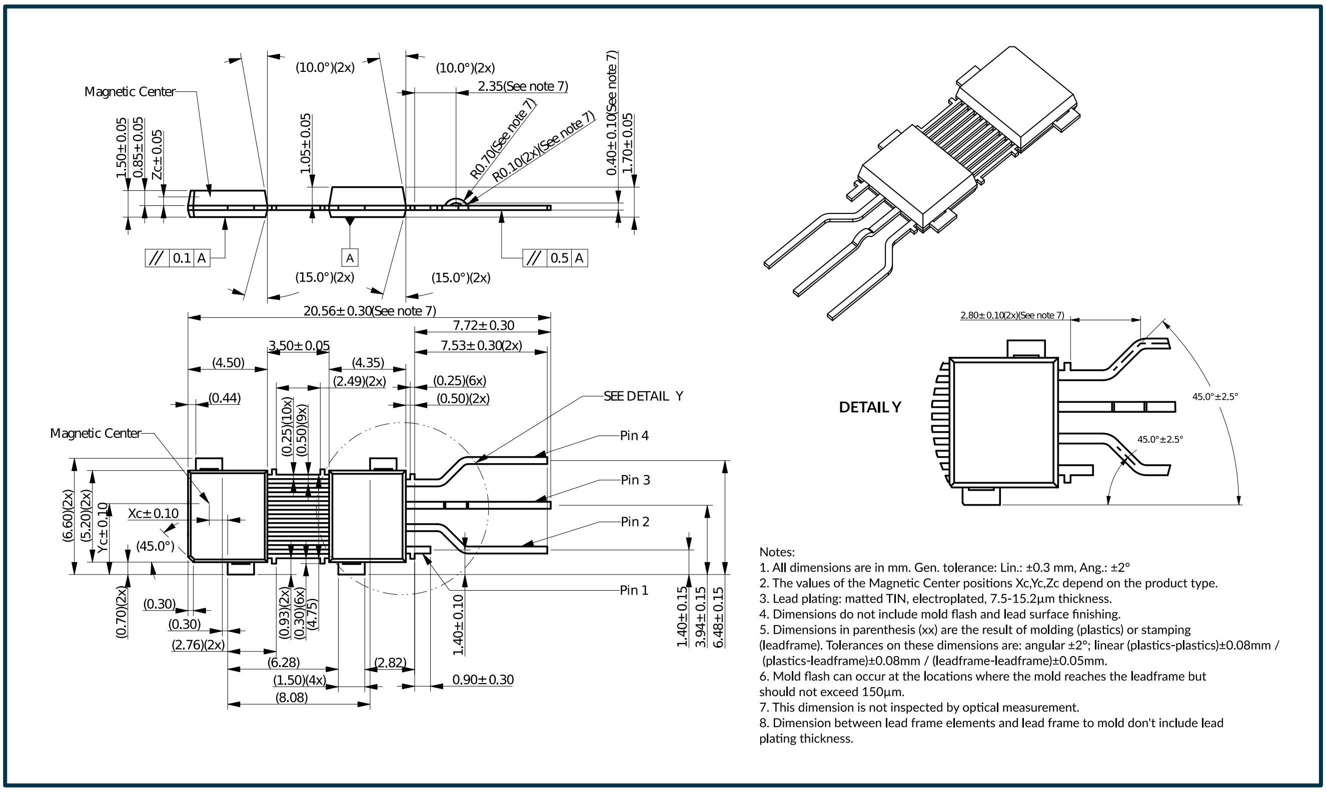


Figure 27 - DMP-4 STD2 2.54 Package Outline Drawing

18.3.3. DMP-4 - Package Outline Dimensions (POD) - STD4 2.54

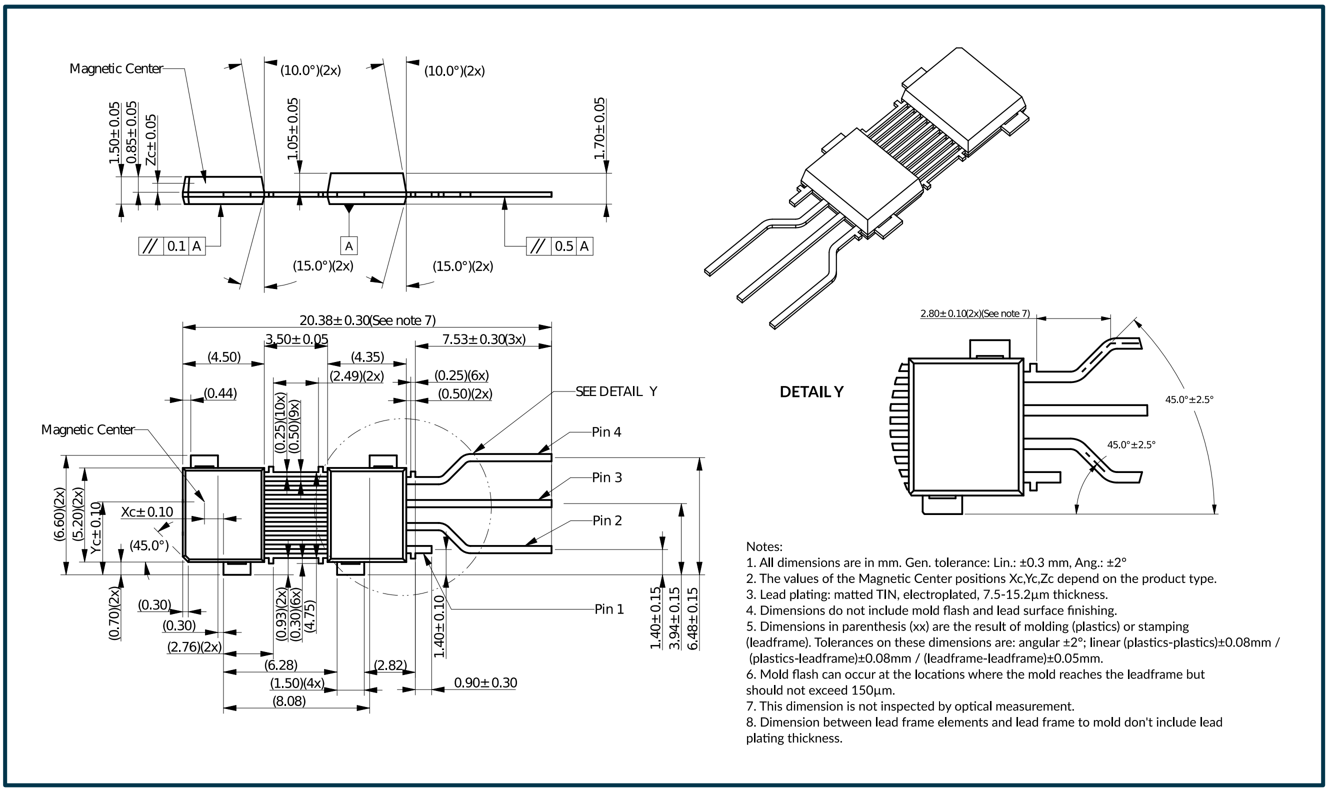


Figure 28 - DMP-4 STD4 2.54 Package Outline Drawing

18.3.4. DMP-4 - Marking

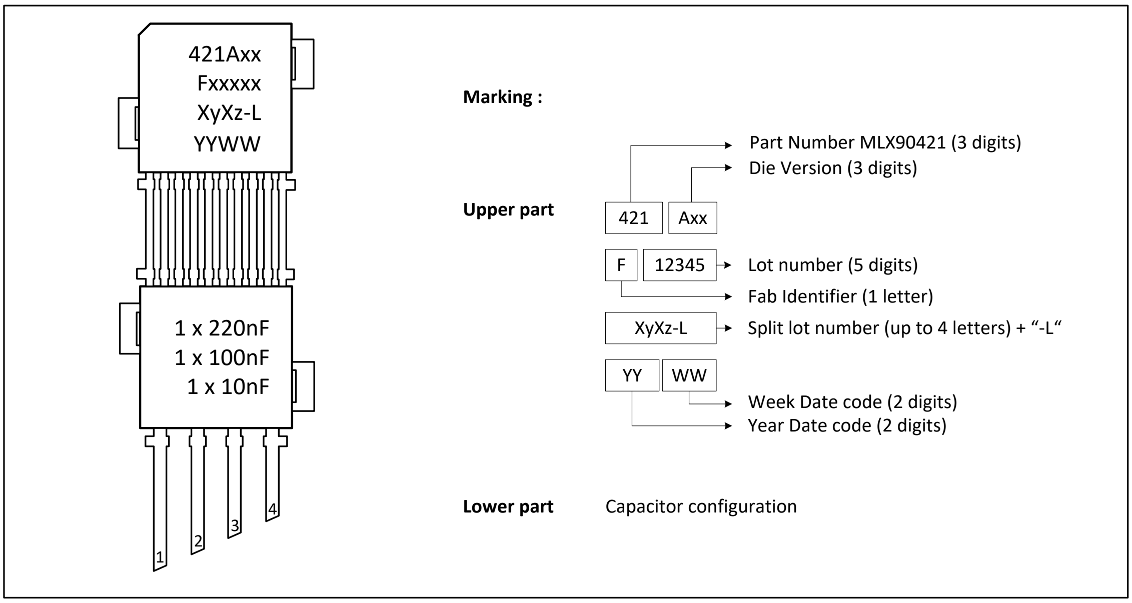


Figure 29 - DMP-4 Marking

18.3.5. DMP-4 - Sensitive Spot Positioning

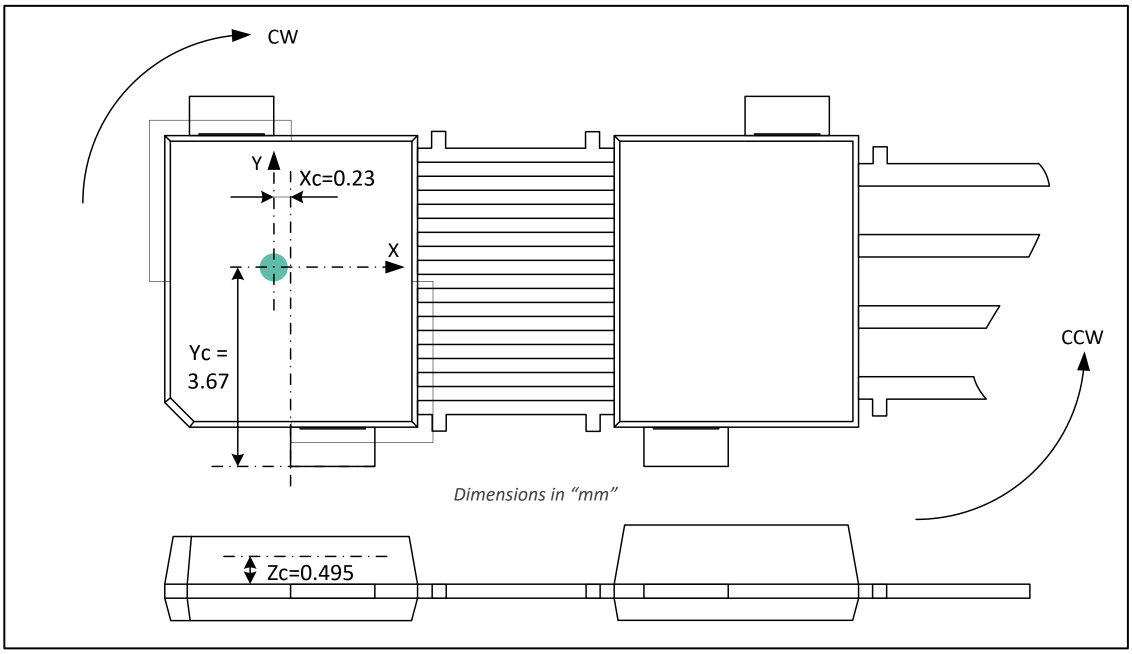


Figure 30 - DMP-4 Sensitive Spot Position

18.3.6. DMP-4 - Angle Detection

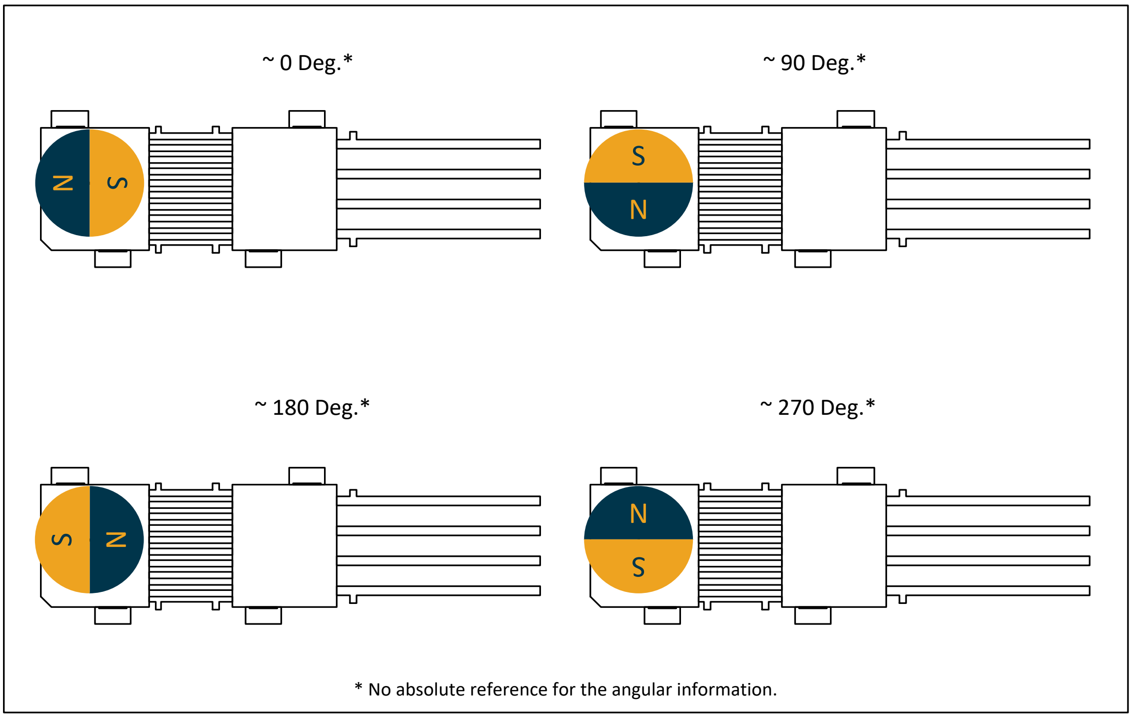
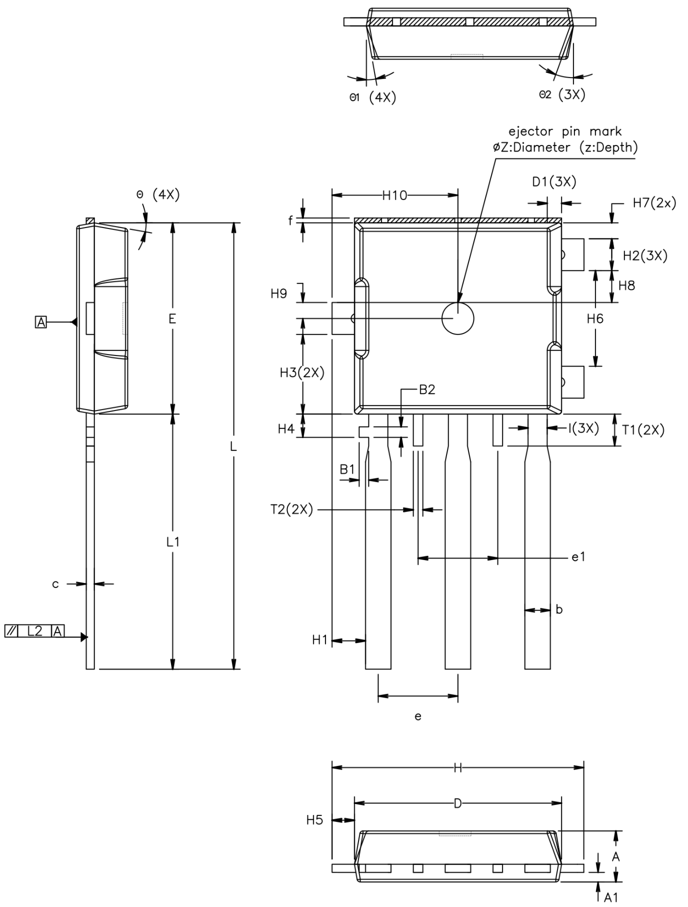


Figure 31 - DMP-4 Angle Detection

The MLX90421 is an absolute angular position sensor but the linearity error (See section 9) does not include the error linked to the absolute reference 0 Deg. This reference can be fixed in the application through the discontinuity point.

18.4. SMP-3 - Package Information

18.4.1. SMP-3 - Package Outline Dimension (POD)



Dimension	MIN.	NOM.	MAX.	Dimension	MIN.	NOM.	MAX.
A	1.550	1.600	1.650	L	13.800	14.000	14.200
A1	0.235	0.300	0.365	L1	7.870	8.000	8.130
B1	0.235	0.300	0.365	L2	-0.325	0.000	0.325
B2		0.33 REF		I	0.525	0.600	0.675
c	0.179	0.254	0.329	b	0.725	0.800	0.875
D	6.420	6.500	6.580	e1	2.400	2.500	2.600
D1		0.450 REF		e	2.400	2.500	2.600
E	5.920	6.000	6.080	θ	8°	10°	12°
f	0.000	- - -	0.152	θ1	8°	10°	12°
H	7.75	7.900	8.050	θ2	18°	20°	22°
H1	0.850	1.050	1.250	øZ	0.900	1.000	1.100
H2	0.925	1.000	1.075	z	0.000	- - -	0.152
H3	2.405	2.500	2.595	T1	0.870	1.000	1.130
H4	0.635	0.730	0.825	T2	0.225	0.300	0.375
H5	0.605	0.700	0.795				
H6	2.925	3.000	3.075				
H7		0.500 REF					
H8	0.925	1.000	1.075				
H9	0.350	0.500	0.650				
H10	3.800	3.950	4.100				

NOTES:

1. DIMENSIONS ARE IN MILLIMETER.
2. PACKAGE WIDTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15MM PER END. PACKAGE LENGTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
3. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. PACKAGE WIDTH AND LENGTH ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH.
4. ALL DIMENSIONS BETWEEN LEADFRAME ELEMENTS OR LEADFRAME AND PACKAGE SHALL EXCLUDE TIN PLATING THICKNESS.
5. PLATING SPECS: MATTED TIN, ELECTROPLATED, 7.6~15.2 MICRO METER THICKNESS
6. ALL "EARS" ARE SHORTED TO GND.

Figure 32 - SMP-3 Package Outline Drawing

18.4.2. SMP-3 - Marking

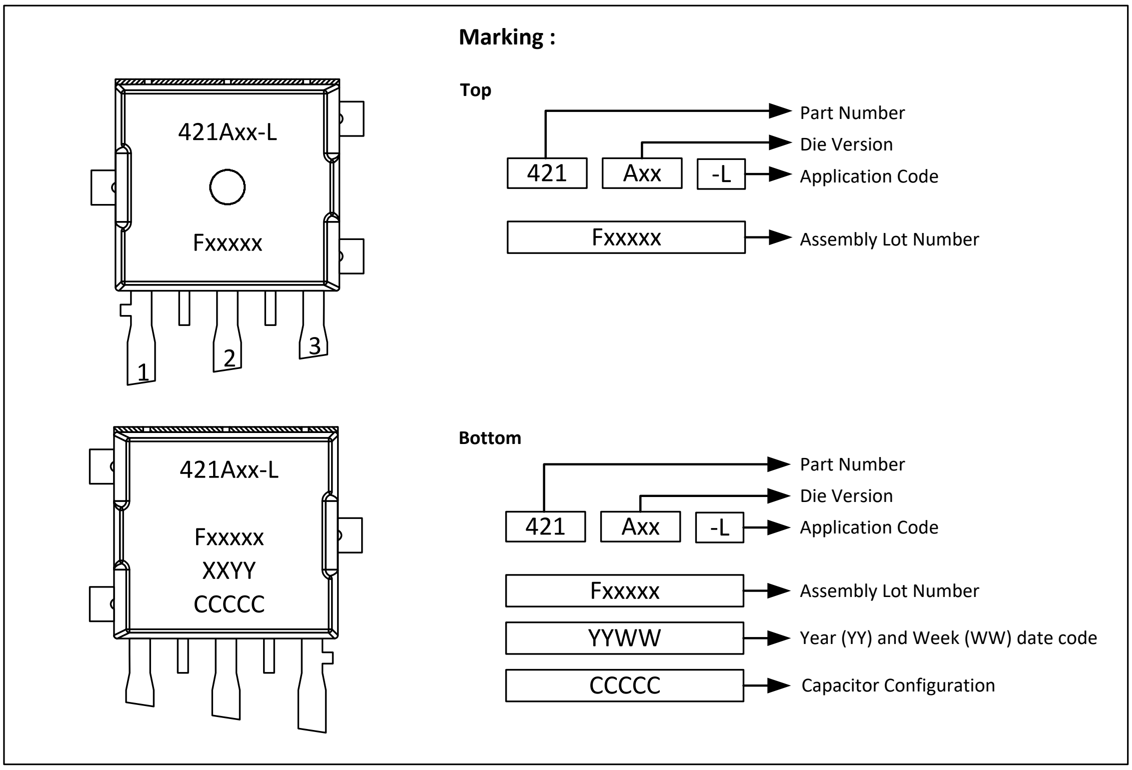


Figure 33 - SMP-3 Marking

18.4.3. SMP-3 - Sensitive Spot Positioning

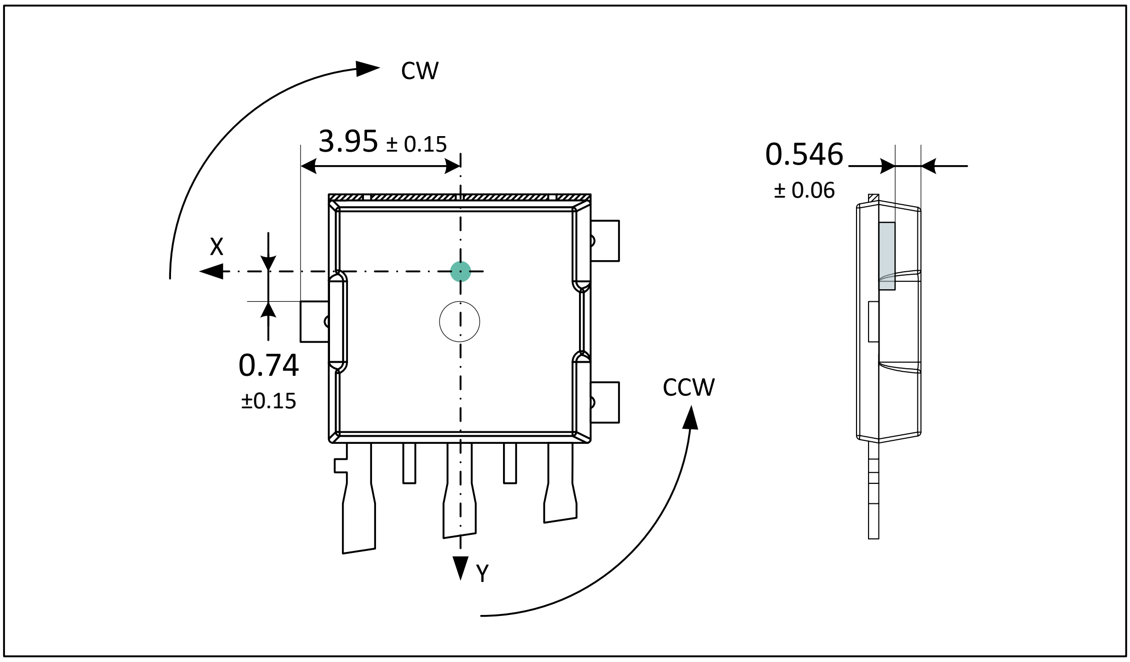


Figure 34 - SMP-3 Sensitive Spot Position

18.4.4. SMP-3 - Angle Detection

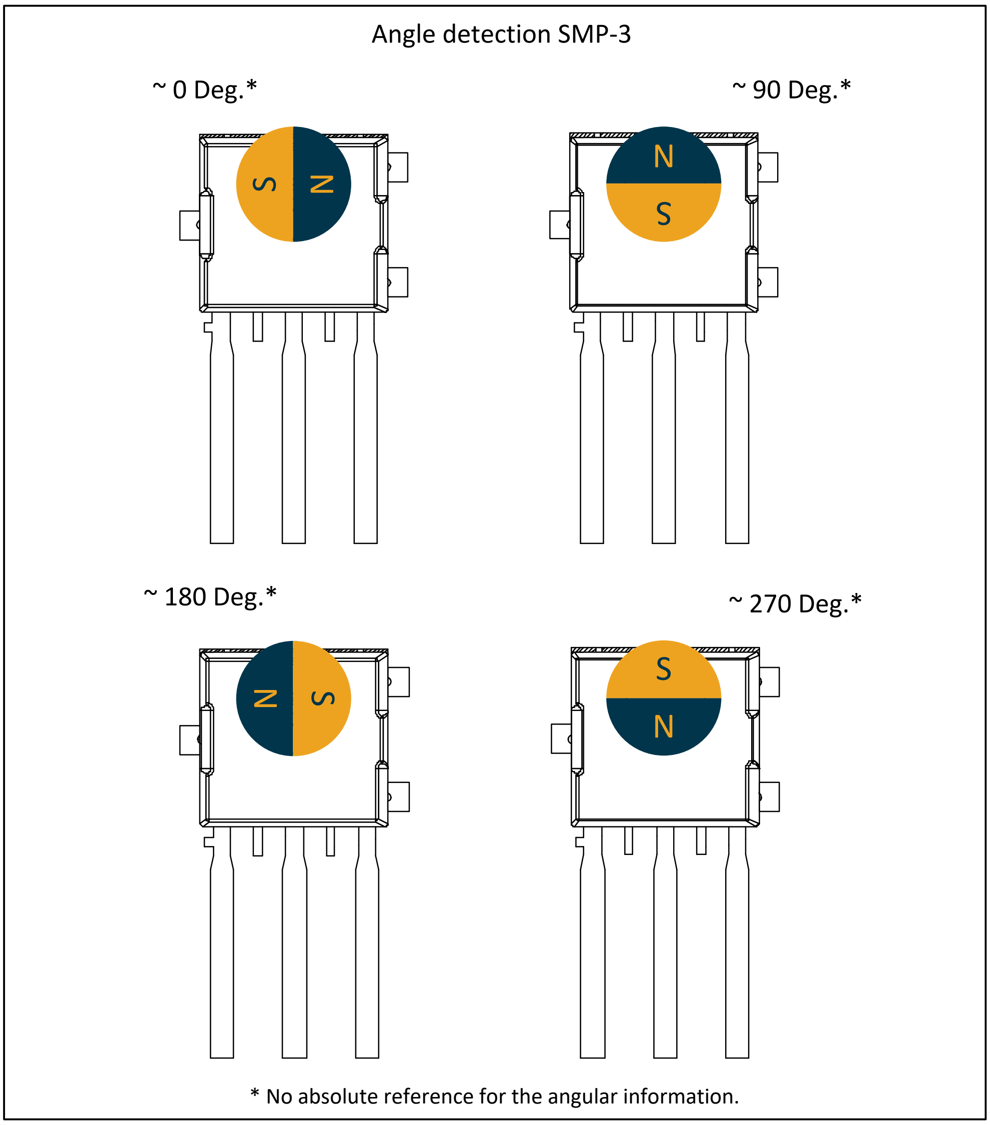
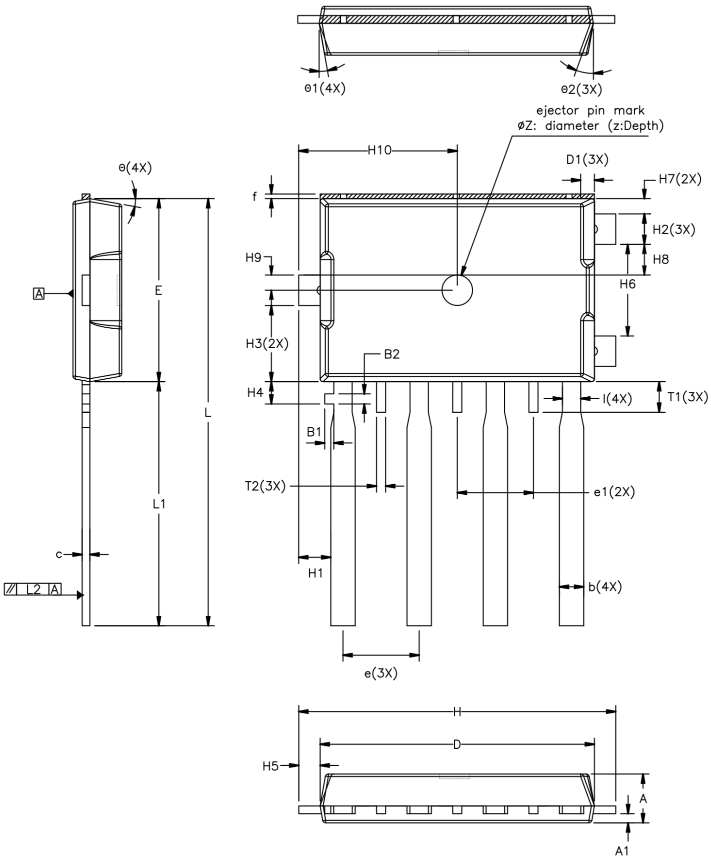


Figure 35 - SMP-3 Angle Detection

18.5. SMP-4 - Package Information

18.5.1. SMP-4 - Package Outline Dimension (POD)



Dimension	MIN.	NOM.	MAX.
A	1.550	1.600	1.650
A1	0.235	0.300	0.365
B1	0.235	0.300	0.365
B2		0.33 REF	
c	0.179	0.254	0.329
D	8.920	9.000	9.080
D1		0.450 REF	
E	5.920	6.000	6.080
f	0.000	- - -	0.152
H	10.250	10.400	10.550
H1	0.850	1.050	1.250
H2	0.925	1.000	1.075
H3	2.405	2.500	2.595
H4	0.635	0.730	0.825
H5	0.605	0.700	0.795
H6	2.925	3.000	3.075
H7		0.500 REF	
H8	0.925	1.000	1.075
H9	0.350	0.500	0.650
H10	5.050	5.200	5.350

Dimension	MIN.	NOM.	MAX.
L	13.800	14.000	14.200
L1	7.870	8.000	8.130
L2	-0.325	0.000	0.325
I	0.525	0.600	0.675
b	0.725	0.800	0.875
e1	2.400	2.500	2.600
e	2.400	2.500	2.600
θ	8°	10°	12°
θ1	8°	10°	12°
θ2	18°	20°	22°
øZ	0.900	1.000	1.100
z	0.000	- - -	0.152
T1	0.870	1.000	1.130
T2	0.225	0.300	0.375

NOTES:

1. DIMENSIONS ARE IN MILLIMETER.
2. PACKAGE WIDTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15MM PER END. PACKAGE LENGTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
3. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. PACKAGE WIDTH AND LENGTH ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH.
4. ALL DIMENSIONS BETWEEN LEADFRAME ELEMENTS OR LEADFRAME AND PACKAGE SHALL EXCLUDE TIN PLATING THICKNESS.
5. PLATING SPECS: MATTED TIN, ELECTROPLATED, 7.6~15.2 MICRO METER THICKNESS
6. ALL "EARS" ARE SHORTED TO GND.

Figure 36 - SMP-4 Package Outline Drawing

18.5.2. SMP-4 - Marking

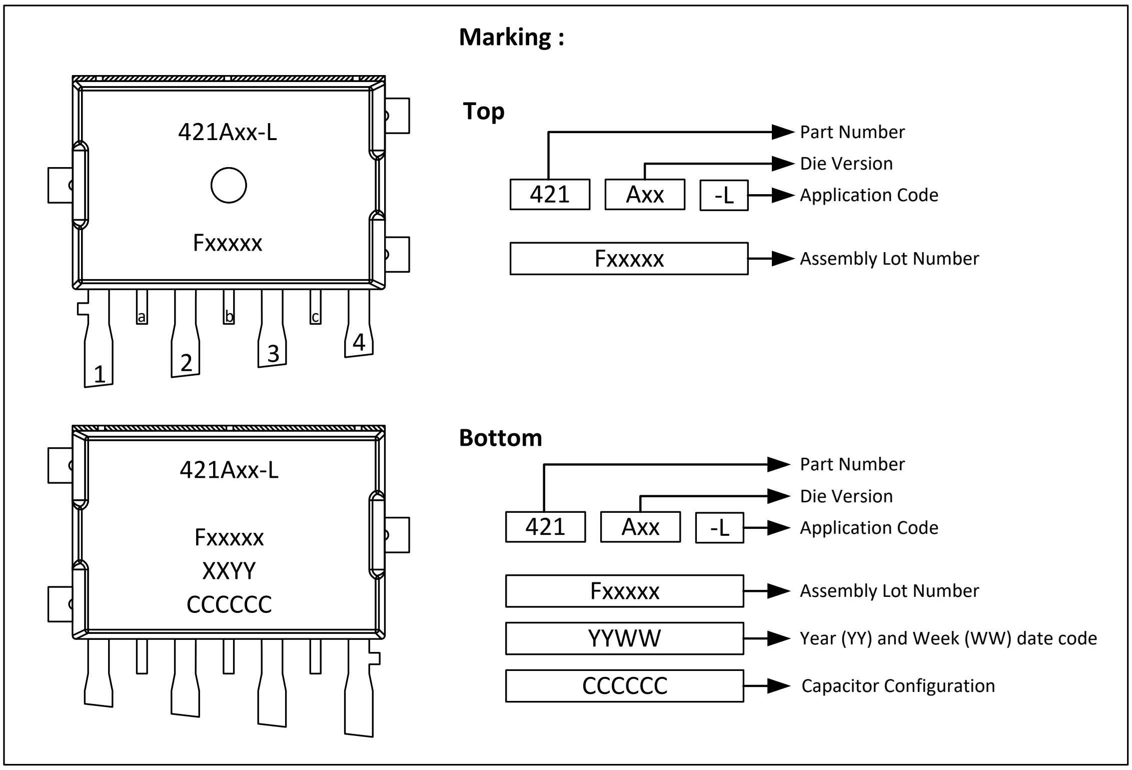


Figure 37 - SMP-4 Marking

18.5.3. SMP-4 - Sensitive Spot Positioning

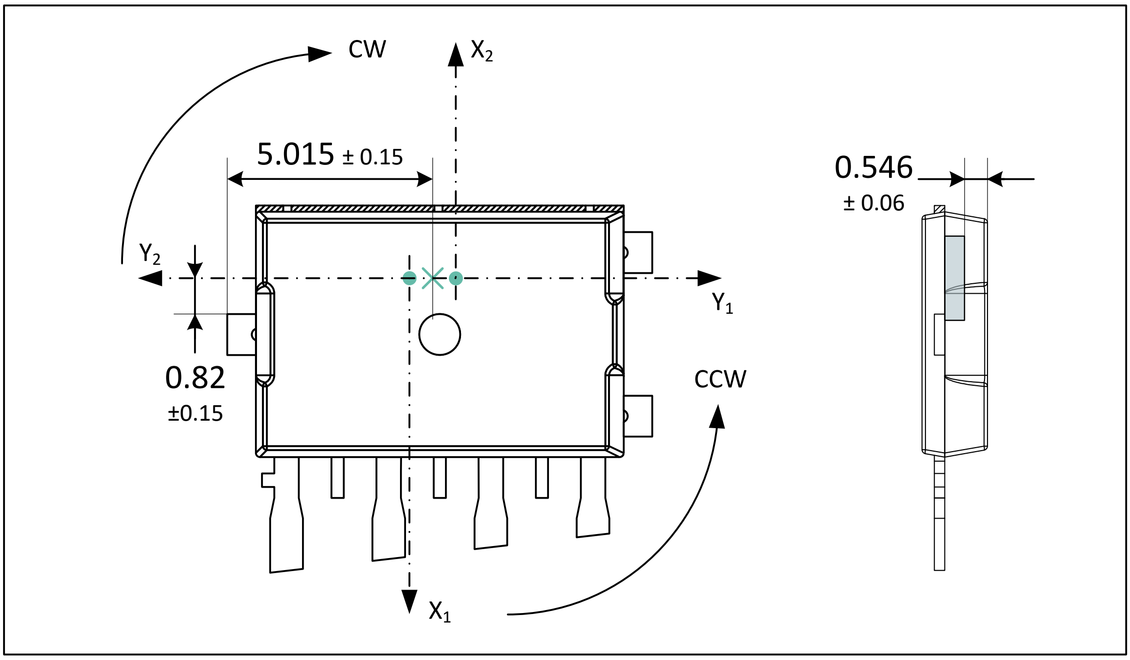


Figure 38 - SMP-4 Sensitive Spot Position

18.5.4. SMP-4 - Angle Detection

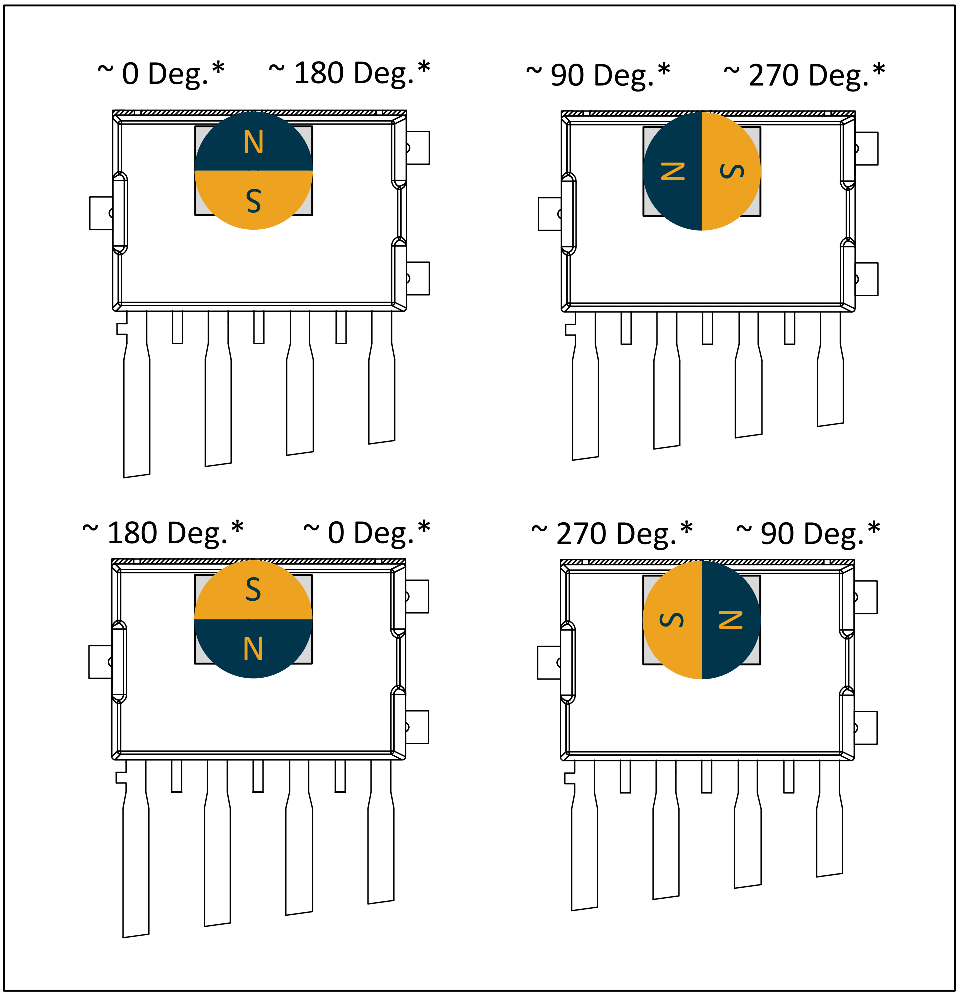


Figure 39 - SMP-4 angle detection

18.6. Packages Thermal Performances

The table below describes the thermal behavior of available packages following JEDEC EIA/JESD 51.X standard.

Package	Junction to case - θjc	Junction to ambient - θja (JEDEC 1s2p board)	Junction to ambient - θja (JEDEC 1s0p board)
SOIC-8	38.8 K/W	112 K/W	153 K/W
TSSOP-16	27.6 K/W	99.1 K/W	137 K/W
DMP-4	32.2 K/W	88.7 K/W(19)	-
SMP-3	34.4 K/W	-	206 K/W(19)
SMP-4	20.82 K/W	-	139.9 K/W(19)

Table 46 - Standard Packages Thermal Performances

[19] *PCB-less solution have been evaluated in a typical application case. Values for these packages are given as informative.*

19. Contact

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20. Disclaimer

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