

## MAX16137

# 1% Accuracy Single-Window Voltage Monitor with BIST

### General Description

The MAX16137 is a low-voltage,  $\pm 1\%$  accurate supervisory circuit that monitors a single system supply voltage for undervoltage and overvoltage faults within a factory-set threshold window. When the monitored supply voltage drops below the undervoltage threshold or goes above the overvoltage threshold, the reset output asserts low. The reset output deasserts after the reset timeout period when the supply voltage returns to within the undervoltage and overvoltage threshold window. The reset output is active-low available in either the push-pull or open-drain options.

The MAX16137 offers factory-trimmed nominal input voltage options from 0.5V to 5V in approximately 20mV increment. A variety of factory-trimmed undervoltage/overvoltage thresholds from  $\pm 4\%$  to  $\pm 11\%$  are available to accommodate different supply voltages and tolerances.

The MAX16137 features a unique Built-In-Self-Test (BIST) diagnostic capability that monitors the health of the internal reset circuit during power-up. If the built-in-self-test fails, the MAX16137 asserts  $\overline{\text{BIST}}$  low. During normal operation, the MAX16137 performs an on-demand BIST when the  $\overline{\text{CLR/BIST}}$  is pulled low for more than 150 $\mu\text{s}$ . See the Built-In-Self-Test section for more details.

The MAX16137 is available in a small, 2mm x 2mm, 8-pin TDFN side-wettable package with exposed pad and operates over the automotive temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Applications

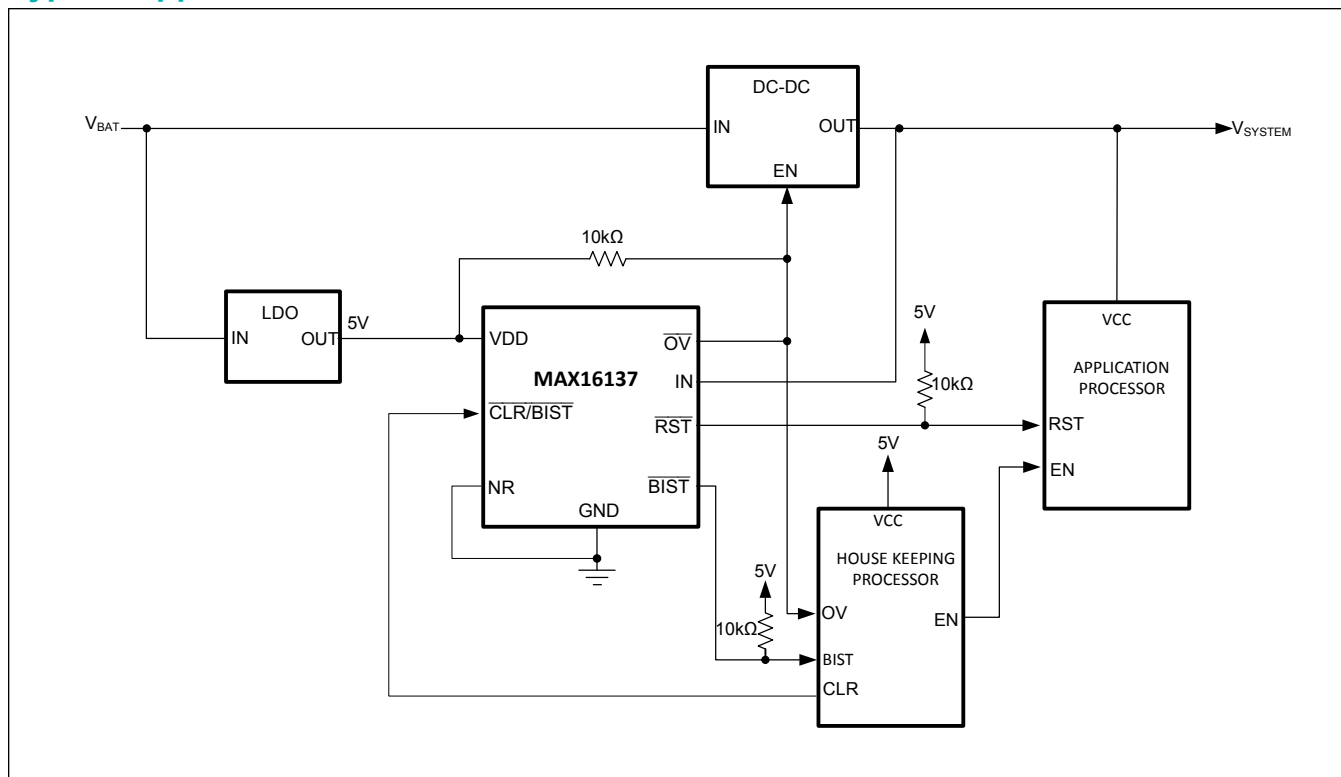
- Advanced Driver-Assistance Systems (ADAS)
- Multivoltage ASICs
- Servers
- Storage Equipment

### Benefits and Features

- $\pm 1\%$  Allow Precision Supply Monitoring
- BIST Enhances System Safety
- Enables ASIL Compliance at System Level
- Factory-Set Threshold 0.5V to 5V with 20mV Increment
- Factory-Set Input Tolerance  $\pm 4\%$  to  $\pm 11\%$  UV/OV Threshold Window
- Factory-Set Reset Timeout
- Latched Overvoltage Fault Output
- 5 $\mu\text{s}$  Overvoltage Fault Response
- Open-Drain/Push-Pull Reset Output
- 2mm x 2mm TDFN-8 Side-Wettable Package
- $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Temperature Range
- AEC-Q100 Qualified

[Ordering Information](#) appears at end of data sheet.

Typical Application Circuit



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## Absolute Maximum Ratings

VDD to GND	-0.3V to +6V	Junction Temperature	+150°C
IN, RST(Open-Drain Output), CLR/BIST, OV, BIST, NR to GND	-0.3V to +6V	Soldering Temperature (Reflow)	+260°C
RST(Push-Pull Output) to GND	-0.3V to (VDD+0.3V)V	Storage Temperature Range	-65°C to +150°C
Input/Output Continuous Current, RST, CLR/BIST, OV, BIST, NR	±20mA	Lead Temperature ((Soldering, 10s))	+300°C
Operating Temperature Range	-40°C to +125°C	Continuous Power Dissipation (TA = +70°C, TDFN-8, derate 6.2mW/°C above +70°C)	496mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Information

### TDFN-8

Package Code	T822CY+2C
Outline Number	<a href="#">21-100341</a>
Land Pattern Number	<a href="#">90-100117</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient ( $\theta_{JA}$ )	162
Junction to Case ( $\theta_{JC}$ )	20

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

(VDD = 1.71V to 5.5V. TA = TJ = -40°C to +125°C, unless otherwise noted. Typical values are at TA = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Operating Voltage Range	VDD	Comparators functional	1.71		5.5	V
Minimum Supply Voltage		RST is guaranteed to be at a known logic	1.1			V
Supply Current	IDD	RST, OV, BIST not asserted		12	23	µA
Undervoltage Lockout Threshold	VUVLO	VDD rising	1.30	1.50	1.68	V
UVLO Hysteresis	VUVLO_HYS	VDD falling		47		mV
<b>INPUT VOLTAGE(IN)</b>						
Nominal Input Voltage Programming Range	VIN_NOM		0.5		5	V
Nominal Input Voltage Programming Step				20		mV

**Electrical Characteristics (continued)**

( $V_{DD} = 1.71V$  to  $5.5V$ .  $T_A = T_J = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$  under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage/ Overvoltage Window Threshold Programming Range	TOL	Reset occurs when $V_{IN\_NOM}$ falls outside of $V_{IN\_NOM} \times (1 \pm TOL)$	$\pm 4$		$\pm 11$	%
Window Threshold Programming Resolution	TOL <sub>RES</sub>			1		%
<b>INPUT THRESHOLD ACCURACY</b>						
Undervoltage Threshold Accuracy	$V_{UVTH\_A}$	All $V_{IN\_TH}$ setting, $V_{IN\_NOM}$ falling, $V_{UVTH} = V_{IN\_NOM} \times (1 - TOL\%)$	-1		1	%
Overvoltage Threshold Accuracy	$V_{OVTH\_A}$	All $V_{IN\_TH}$ setting, $V_{IN\_NOM}$ rising, $V_{OVTH} = V_{IN\_NOM} \times (1 + TOL\%)$	-1		1	%
Undervoltage/ Overvoltage Threshold Hysteresis	$V_{HYS}$			0.5		%V <sub>TH</sub>
Input Current	$I_{IN}$			1.3	5	$\mu A$
Overvoltage Fault-to- $\overline{OV}$ Assert Delay	$t_{OV\ DLY}$	( $V_{OVTH} - 1\%$ ) to ( $V_{OVTH} + 1\%$ )		5		$\mu s$
<b>CLEAR/BUILT-IN-SELF-TEST INPUT (<math>\overline{CLR/BIST}</math>)</b>						
$\overline{CLR/BIST}$ Input Glitch Immunity			50			ns
$\overline{CLR/BIST}$ Input Pulse Width to Clear OV Latch	$t_{CLR}$	From falling edge of $\overline{CLR/BIST}$ to $\overline{OV}$ rising edge	0.4			$\mu s$
$\overline{CLR/BIST}$ Pulse Width to Initiate BIST	$t_{BIST}$	From falling edge of $\overline{CLR/BIST}$ to start of BIST (Note2)	150			$\mu s$
$\overline{CLR/BIST}$ Internal Pull Up Resistance				50		k $\Omega$
On-Demand $\overline{CLR/BIST}$ to BIST Assert Delay		From the falling edge of the $\overline{CLR/BIST}$ to BIST asserting			380	$\mu s$
<b>RESET OUTPUT (<math>\overline{RST}</math>)</b>						
Reset Timeout Period Accuracy	$t_{RP}$	From time $V_{IN}$ enters overvoltage/ undervoltage threshold-window to time $\overline{RST}$ goes high, $V_{DD} = 3.3V$	-20		+20	%
IN-to- $\overline{RST}$ Propagation Delay	$t_{DOV}$	( $V_{OVTH} - 1\%$ ) to $V_{OVTH} + 1\%$ )		5		$\mu s$
	$t_{DUV}$	( $V_{UVTH} + 1\%$ ) to ( $V_{UVTH} - 1\%$ )		12		
$\overline{RST}$ Leakage Current		$V_{\overline{RST}} = V_{OV} = 5.5V$		0.01	1	$\mu A$
<b>INPUT VOLTAGE (<math>\overline{CLR/BIST}</math>, NR)</b>						
$\overline{CLR/BIST}$ , NR Input Voltage Low	$V_{IL}$				$0.3 \times V_{DD}$	V
$\overline{CLR/BIST}$ , NR Input Voltage High	$V_{IH}$		$0.7 \times V_{DD}$			V
$\overline{CLR/BIST}$ , NR Leakage Current		$V_{\overline{CLR/BIST}} = V_{DD}$ , $V_{NR} = V_{DD}$	-0.1		+0.1	$\mu A$

**Electrical Characteristics (continued)**

( $V_{DD}$  = 1.71V to 5.5V.  $T_A = T_J$  = -40°C to +125°C, unless otherwise noted. Typical values are at  $T_A$  = +25°C under normal conditions, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OUTPUT VOLTAGE ( <math>\overline{RST}</math>, <math>\overline{OV}</math>, BIST )</b>						
Output Voltage Low	$V_{OL}$	$\overline{RST}$ , $\overline{OV}$ , $\overline{BIST}$ , $V_{DD} = 5V$ , $I_{SINK} = 3mA$		0.1	0.3	V
		$\overline{RST}$ , $\overline{OV}$ , $\overline{BIST}$ , $V_{DD} = 1.71V$ , $I_{SINK} = 8\mu A$		0.1	0.3	
		$\overline{RST}$ $V_{DD} = 1.1V$ , $I_{SINK} = 8\mu A$		0.1	0.3	

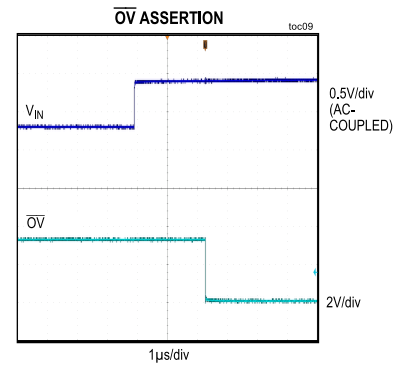
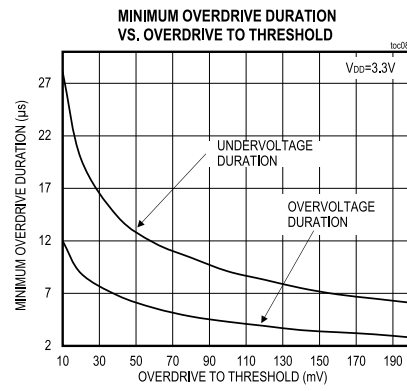
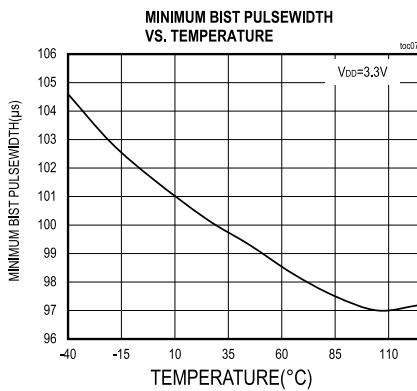
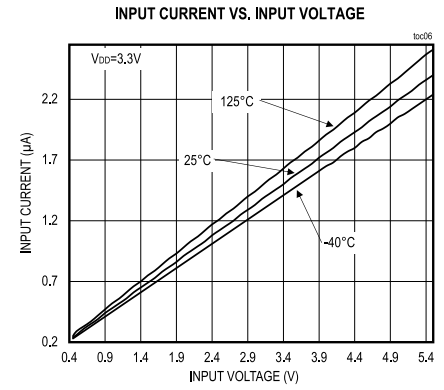
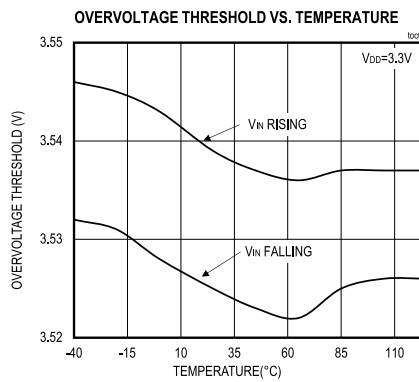
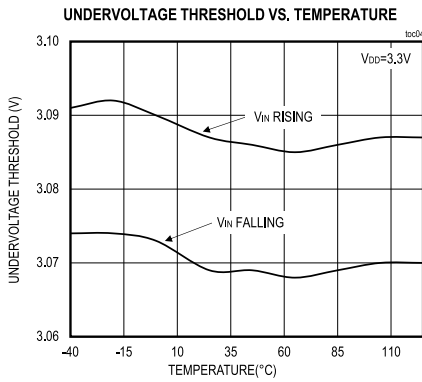
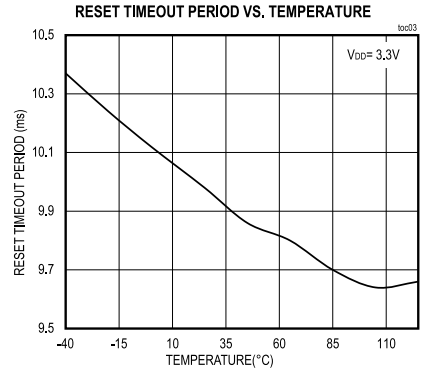
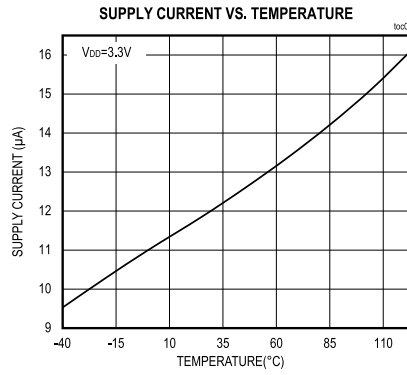
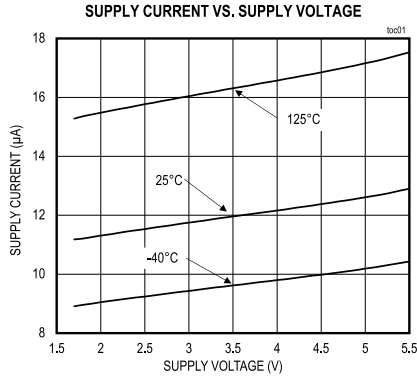
**Note 1:** Outputs are guaranteed to be in correct state down to  $V_{DD} = 1.1V$ .

**Note 2:** Minimum pulse required to clear  $\overline{OV}$  latched state. No overvoltage fault present and  $\overline{RST}$  = high.



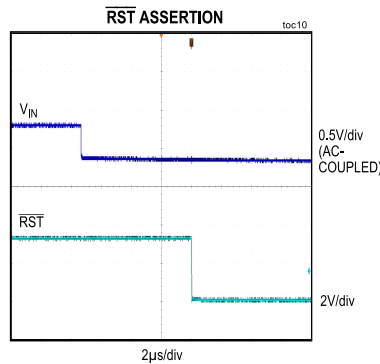
Typical Operating Characteristics

( $V_{DD} = 1.71V$  to  $5.5V$ ,  $T_A = -40^{\circ}C$  to  $125^{\circ}C$ , Typical values are at  $V_{DD} = 3.3V$ , unless otherwise specified.)



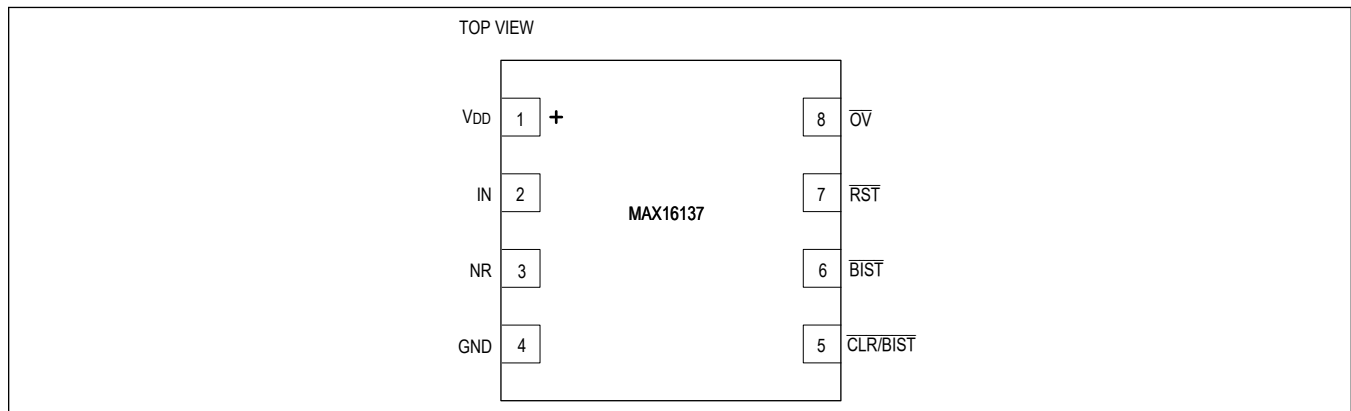
## Typical Operating Characteristics (continued)

( $V_{DD}$  = 1.71V to 5.5V,  $T_A$  = -40°C to 125°C, Typical values are at  $V_{DD}$  = 3.3V, unless otherwise specified.)



## Pin Configuration

### 8 TDFN



## Pin Description

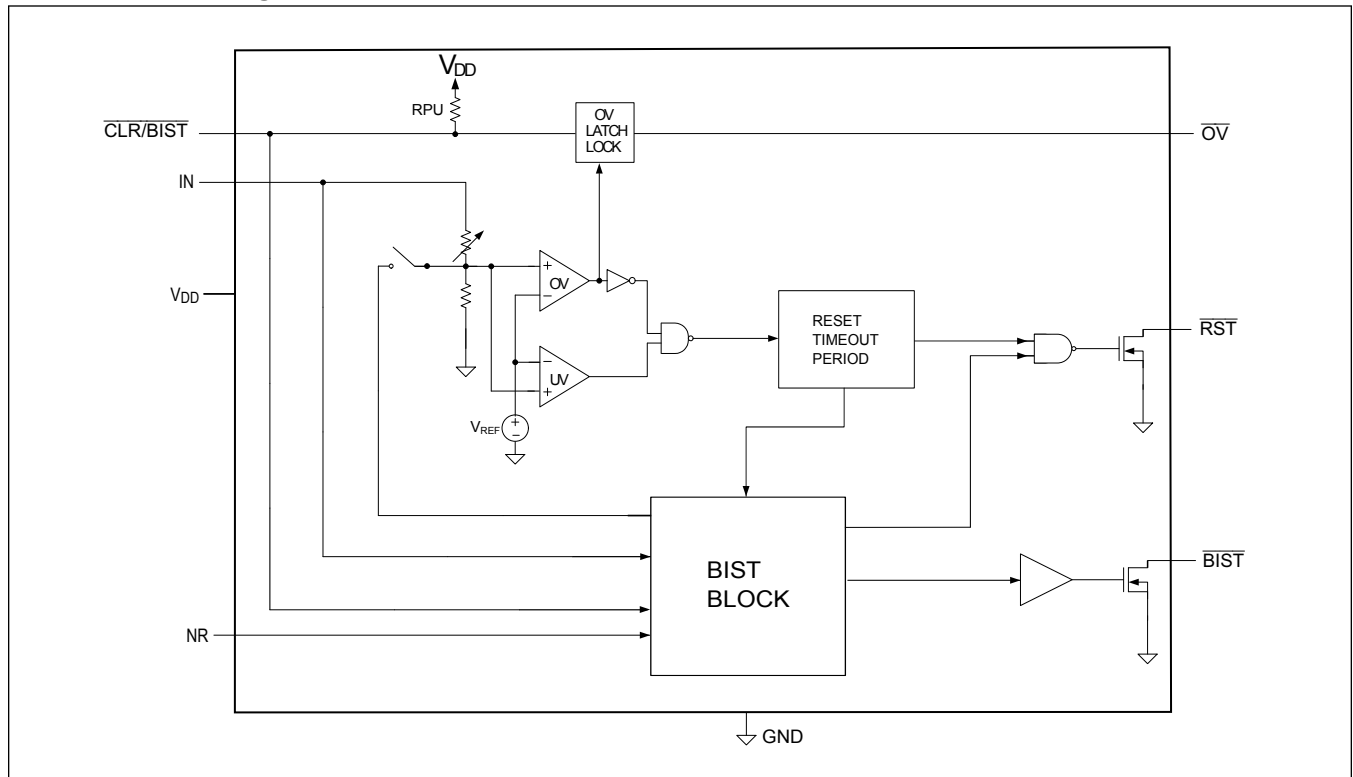
PIN	NAME	FUNCTION
1	VDD	Supply Input. Bypass $V_{DD}$ to ground with a 0.1 $\mu$ F capacitor.
2	IN	Monitoring Input IN is a factory-set threshold monitoring input. When $V_{IN}$ falls outside the factory selected undervoltage/overvoltage threshold window, $\overline{RST}$ asserts and stays asserted for a selected reset timeout period after $V_{IN}$ falls within the undervoltage/overvoltage threshold window. When $V_{IN}$ exceeds the overvoltage threshold, $\overline{OV}$ asserts and indicates an overvoltage fault.
3	NR	No Reset BIST Logic Input. Setting NR to a logic low and driving $\overline{CLR/BIST}$ low for more than 150 $\mu$ s initiates BIST and asserts the reset output and BIST if BIST fails. Setting NR to a logic high and driving $\overline{CLR/BIST}$ low for more than 150 $\mu$ s initiates BIST and asserts BIST only if BIST fails.
4	GND	Ground.
5	$\overline{CLR/BIST}$	Overvoltage Clear/Built-In-Self-Test Input. $\overline{CLR/BIST}$ is a multiplexed function input. A falling edge on $\overline{CLR/BIST}$ clears $\overline{OV}$ latch. Driving $\overline{CLR/BIST}$ for more than 150 $\mu$ s initiates BIST.

Pin Description (continued)

PIN	NAME	FUNCTION
6	$\overline{\text{BIST}}$	Active-Low, Open-Drain Output. $\overline{\text{BIST}}$ asserts low if BIST fails. Pull $\overline{\text{BIST}}$ to VDD with a pullup resistor.
7	$\overline{\text{RST}}$	Open-Drain Reset Output. $\overline{\text{RST}}$ asserts low when $V_{\text{IN}}$ falls outside of the undervoltage/overvoltage threshold window. The reset output deasserts after the reset timeout period when $V_{\text{IN}}$ enters the undervoltage/overvoltage threshold window.
8	$\overline{\text{OV}}$	Open-Drain, Active-Low Overvoltage Latched Fault Output. $\overline{\text{OV}}$ latches low when the voltage at IN exceeds the overvoltage threshold setting. $\overline{\text{OV}}$ latch is cleared on the falling edge of CLR/BIST.

Functional Diagrams

Internal Block Diagram



## Detailed Description

The MAX16137 is a high-accuracy single-channel supervisory reset circuit that monitors the system supply for undervoltage and overvoltage faults within factory-programmable window thresholds. The MAX16137's Built-In-Self-Test (BIST) diagnostic capability and overvoltage fault output optimizes system safety in ADAS applications. A reset output (RST) asserts when the input voltage falls outside of the threshold-window. The reset output deasserts after the reset timeout period when the supply voltage returns back to its nominal voltage level.

### Normal Input Threshold Range

The MAX16137 offers a wide range of nominal input voltages from 0.5V to 5V in approximately 20mV increment. Each selected nominal input voltage is factory-trimmed halfway between the undervoltage and overvoltage threshold window. See the [Undervoltage/Overvoltage Thresholds](#) section for more details. Contact Maxim sales for options not listed in the [Ordering Information](#) table.

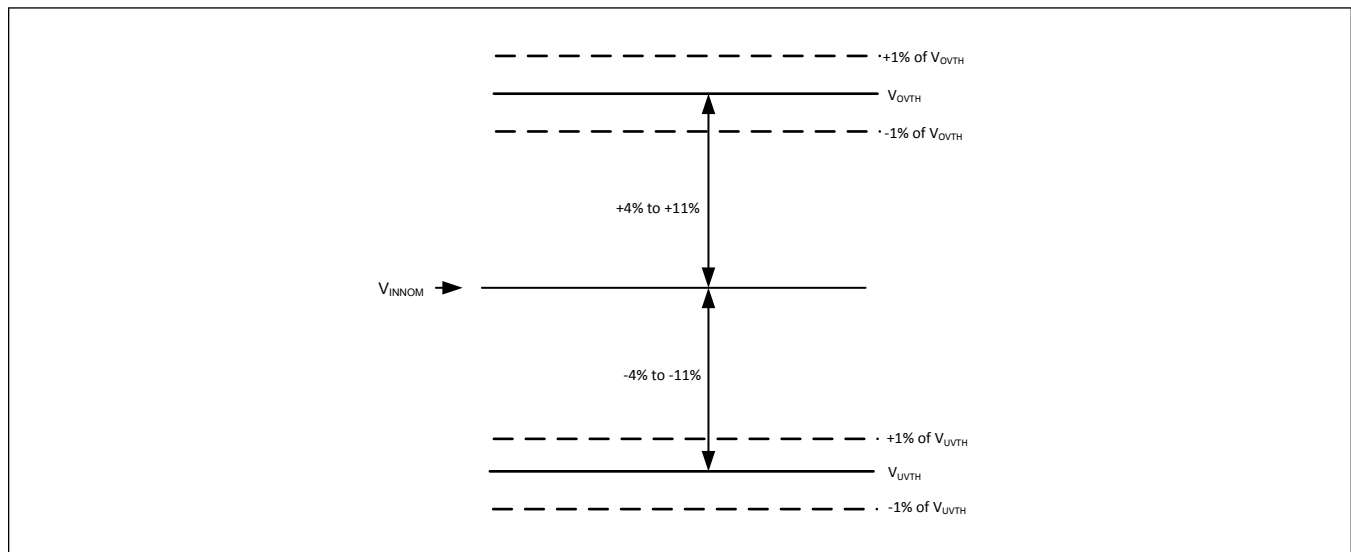


Figure 1. Undervoltage/Overvoltage Threshold Tolerance and Accuracy

### Undervoltage/Overvoltage Thresholds

The MAX16137 monitors supply voltage for undervoltage/overvoltage faults with respect to nominal input voltage within  $\pm 1\%$  accuracy over the operating temperature and supply ranges. The undervoltage and overvoltage thresholds are factory-trimmed from  $\pm 4\%$  to  $\pm 11\%$  in  $\pm 1\%$  increments. Contact Maxim for threshold not listed in the [Ordering Information](#) table.

### Undervoltage/Overvoltage Threshold Hysteresis

The monitoring input (IN) features undervoltage/overvoltage threshold hysteresis that provides immunity to short input transients. The input hysteresis is factory-set to either 0.25% or 0.5% and is applicable to both the undervoltage and overvoltage thresholds. Contact Maxim for hysteresis option not listed in the [Ordering Information](#) table.

### Overvoltage Fault Output

$\overline{OV}$  is an open-drain, active-low latched output that latches low  $5\mu\text{s}$  after  $V_{IN}$  exceeds the overvoltage threshold level.  $\overline{OV}$  latch is cleared on the falling edge of  $\overline{CLR/BIST}$  after the overvoltage fault is removed. See the Electrical Characteristics table and following [Figure 2](#) for more details.

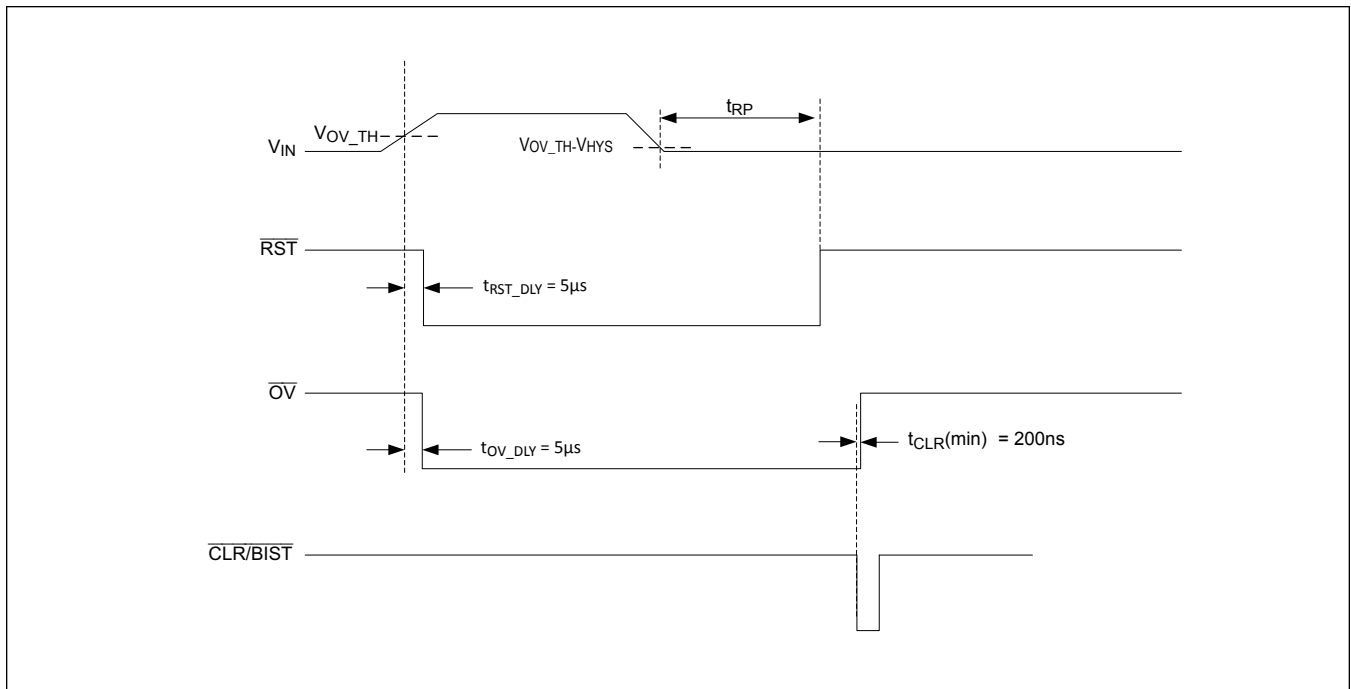


Figure 2. Clear Input Timing Diagram

### Built-In-Self-Test (BIST)

BIST is a diagnostic feature that monitors the health of the MAX16137. BIST is initiated during power-up and completes after the expiration of the reset timeout period. During power-up, the MAX16137 monitors the state of the reset output. A high-logic reset output status during power-up indicates a fault either inside or outside the MAX16137, and  $\overline{\text{BIST}}$  is pulled low. See the following [Figure 3](#) at T1. After the expiration of the reset timeout period, the MAX16137 generates internally fictitious undervoltage and overvoltage fault scenarios, and  $\overline{\text{RST}}$  deasserts. If the MAX16137 internal circuit does not respond properly to the internally generated undervoltage and overvoltage faults,  $\overline{\text{BIST}}$  and  $\overline{\text{RST}}$  are pulled low. See the following [Figure 3](#) at T2 and T3. Then the MAX16137 monitors the state of the reset output again. A low-logic reset output status indicates a fault either inside or outside the MAX16137 and  $\overline{\text{BIST}}$  is pulled low. See the following [Figure 3](#) at T4.

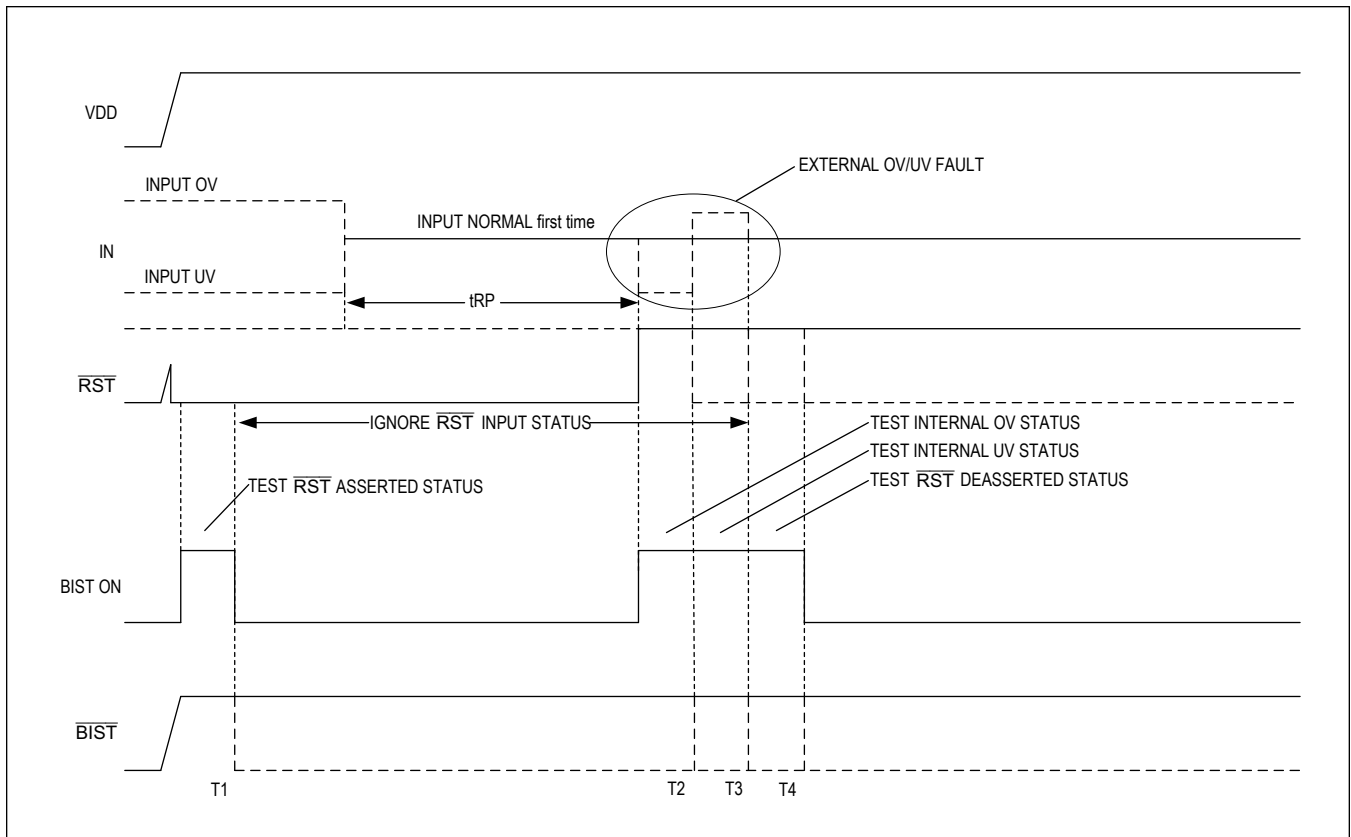


Figure 3. MAX16137 BIST Timing Relationship

**On-Demand BIST**

On-demand BIST allows the MAX16137 to initiate BIST during normal operation. On-demand BIST is initiated when  $\overline{\text{CLR/BIST}}$  is pulled low for more than  $t_{\text{BIST}}$ . See the Electrical Characteristic table for more details. If  $\overline{\text{CLR/BIST}}$  is pulled low for less than  $t_{\text{BIST}}$ , or if the input is overvoltage or undervoltage before the expiration of  $t_{\text{BIST}}$ , on-demand BIST is ignored.

With NR at logic low and  $\overline{\text{CLR/BIST}}$  is pulled low for more than  $t_{\text{BIST}}$ , on-demand BIST operation is similar to that of power-up: The MAX16137 pulls the reset output low during the internal OV and UV testing while keeping the system in reset, Figure 4. When NR is at logic high and  $\overline{\text{CLR/BIST}}$  is pulled low for more than  $t_{\text{BIST}}$ , on-demand BIST operation is carried out without pulling the reset output low. See the following Figure 5 for more details.

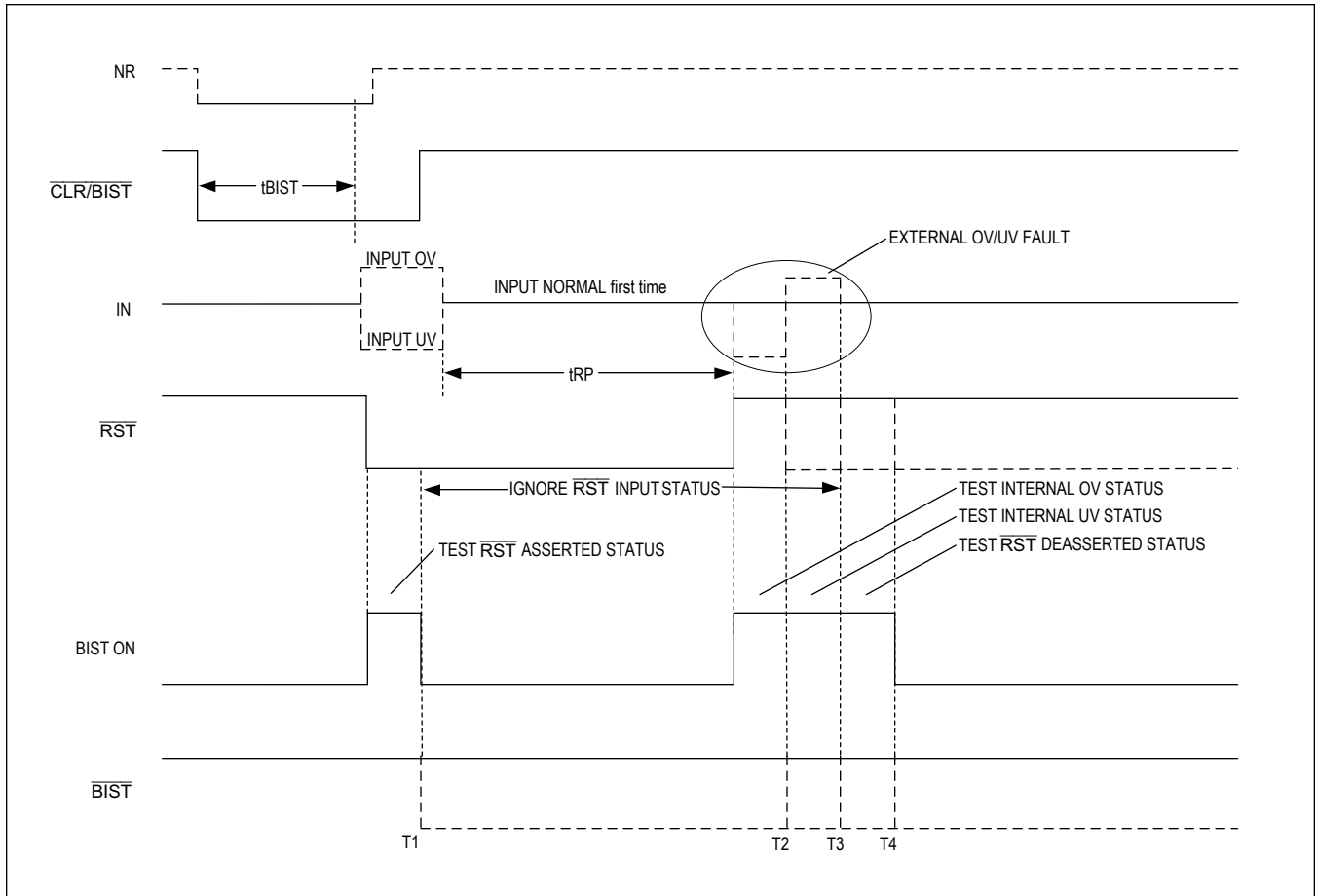


Figure 4. MAX16137 On-Demand BIST Timing with NR = LOW

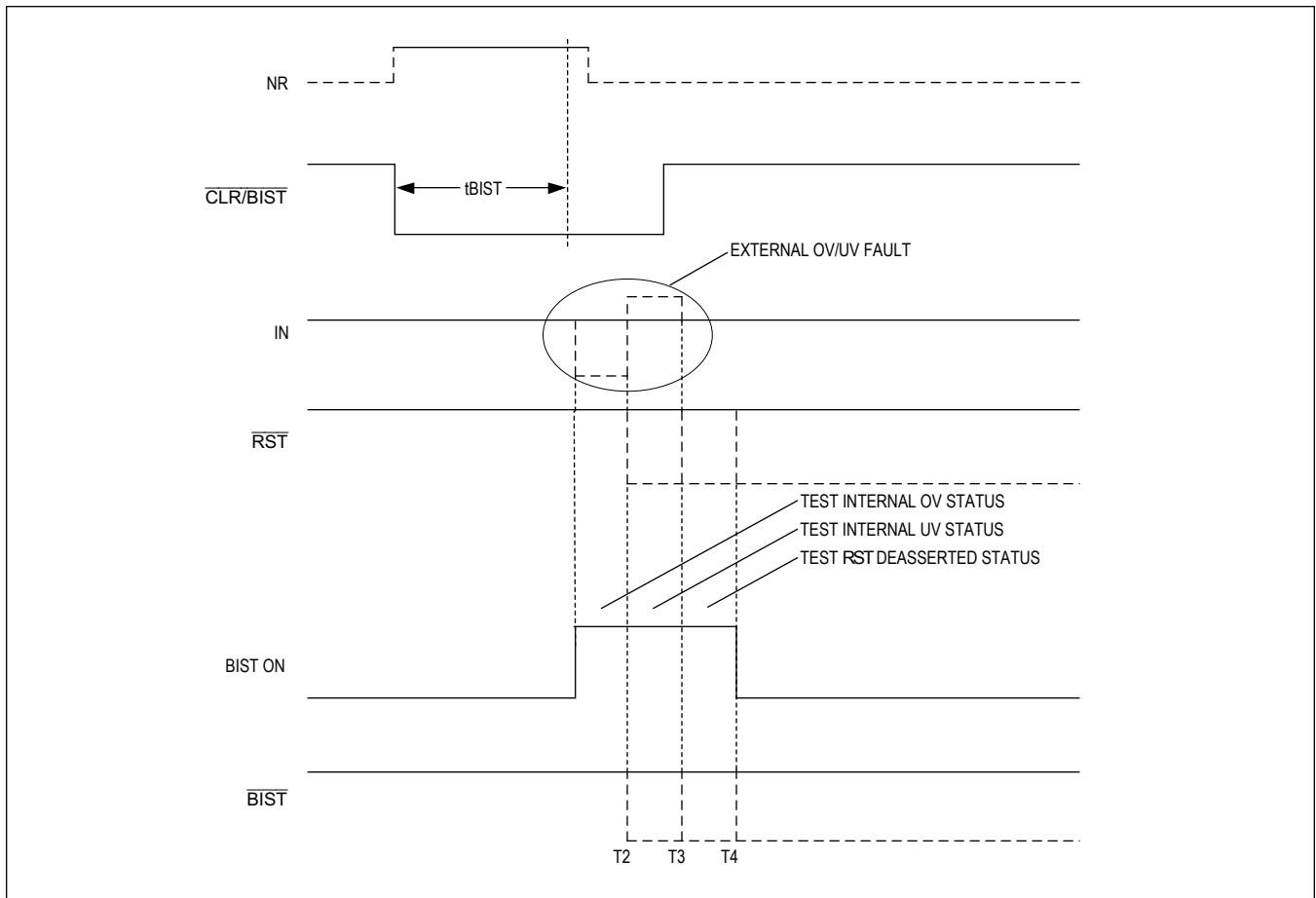


Figure 5. MAX16137 On-Demand BIST Timing with NR = HIGH

### Reset Timeout Period

The active-low, open-drain reset output ( $\overline{RST}$ ) asserts low when the input voltage falls outside the set undervoltage and overvoltage window threshold. The reset output deasserts after the reset timeout period when the input voltage falls within the set window threshold. At power-up, the resets stay asserted for the reset timeout period once  $V_{DD}$  is above the UVLO. The reset output requires a pullup resistor to  $V_{DD}$ . The MAX16137 offers 16 factory-set reset timeout periods. The MAX16137 offers both open-drain and push-pull reset output options. See [Table 1](#) for available options and [Figure 6](#) for more details.

### Table 1. Reset Timeout Options

MIN RESET TIMEOUT PERIOD
1ms
5ms
10ms
15ms
20ms
50ms
100ms
150ms



**Table 1. Reset Timeout Options (continued)**

200ms
250ms
300ms
500ms
750ms
1000ms
15000ms

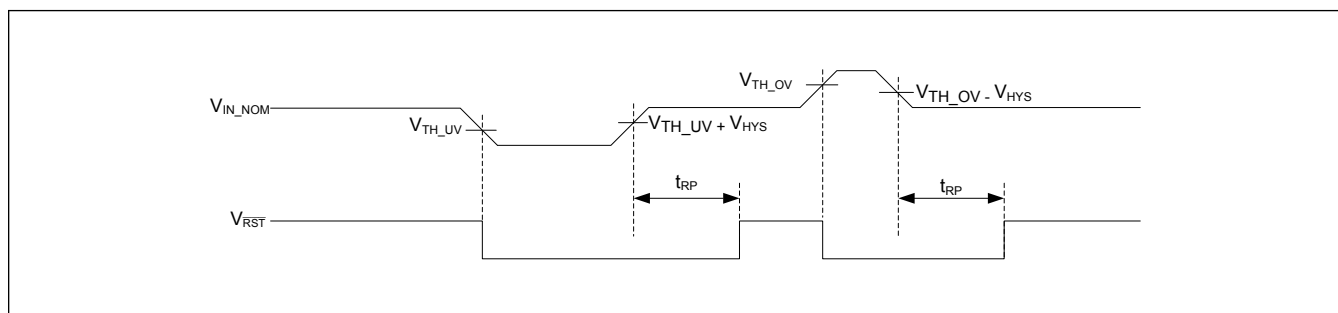


Figure 6. Reset Output Timing Diagram

## Applications Information

### Setting Input Thresholds and Hysteresis

The MAX16137 monitors a system supply voltage for undervoltage/overvoltage window threshold. Depending on the system supply tolerance requirement, the undervoltage/overvoltage thresholds can be factory-trimmed from  $\pm 4\%$  to  $\pm 11\%$ . The tolerance setting is symmetrical with respect to the selected nominal input threshold voltage ( $V_{IN\_NOM}$ ). A detailed calculation of how to determine the undervoltage/overvoltage threshold levels with  $\pm 1\%$  threshold accuracy for 3.3V  $\pm 5\%$  supply voltage is presented here:

$$V_{IN\_NOM} = 3.3V$$

$$TOL = \pm 5\%$$

$$V_{UVTH} = V_{IN\_NOM} (1 - 5\%) = 3.3V (1 - 0.05) = 3.135V$$

$$V_{OVTH} = V_{IN\_NOM} (1 + 5\%) = 3.3V (1 + 0.05) = 3.465V$$

where  $V_{IN\_NOM}$  is the selected nominal input threshold voltage, TOL is the input tolerance,  $V_{UVTH}$  is undervoltage threshold voltage, and  $V_{OVTH}$  is the overvoltage threshold voltage.

The MAX16137 monitors the supply voltage with  $\pm 1\%$  accuracy over the operating temperature and supply range. The accuracy range for the 3.3V  $\pm 5\%$  is as following:

$$V_{UVTH\_A} = V_{UVTH} (1 \pm 1\%) = 3.135V (1 \pm 0.01) = 3.135V \pm 0.03135V$$

$$V_{OVTH\_A} = V_{OVTH} (1 \pm 1\%) = 3.465V (1 \pm 0.01) = 3.465V \pm 0.03465V$$

where  $V_{UVTH\_A}$  is the undervoltage threshold accuracy range and  $V_{OVTH\_A}$  is the overvoltage threshold accuracy range. See [Figure 7](#) for details.

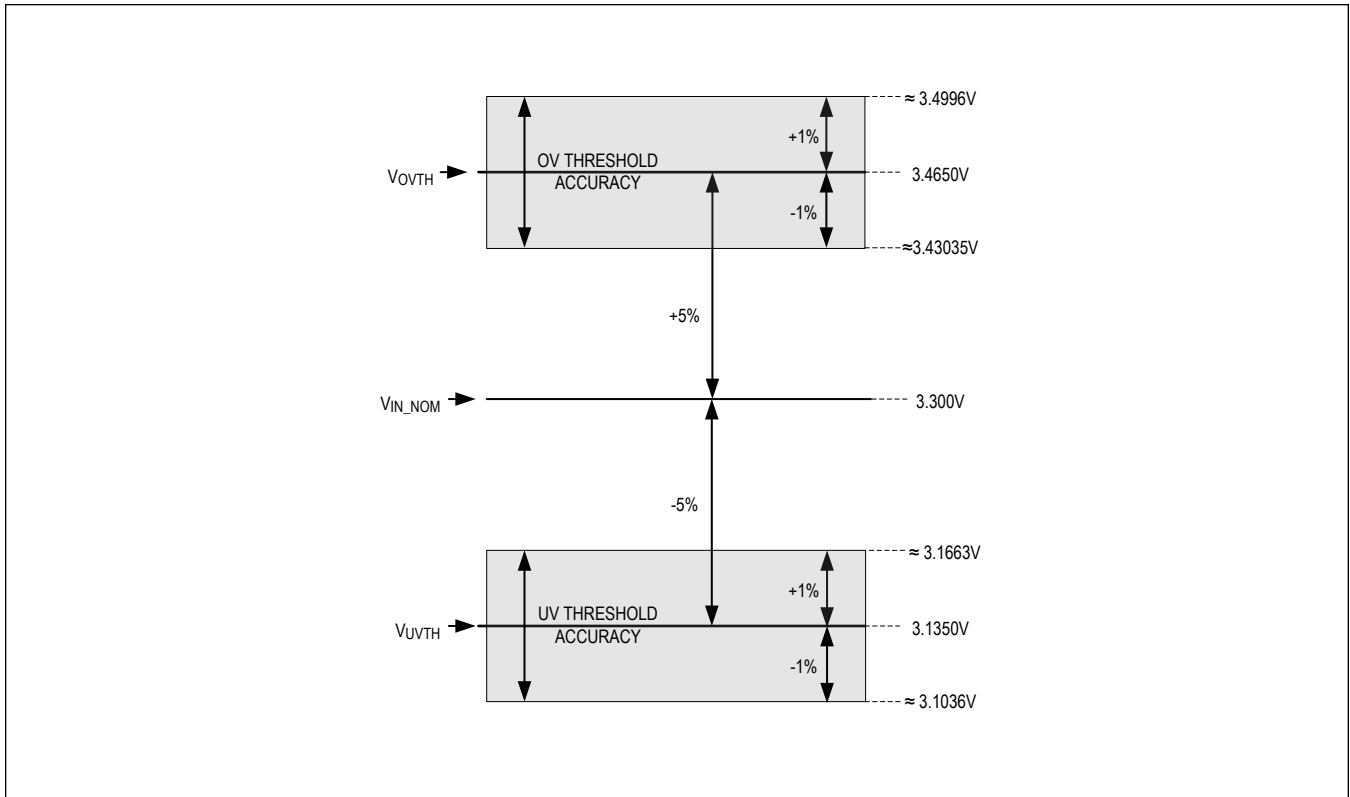


Figure 7. Undervoltage/Overvoltage Threshold Accuracy

Hysteresis adds noise immunity to the voltage monitors and prevents oscillation due to repeated triggering when the monitored voltage is near the threshold trip voltage.

A detailed calculation to get the threshold hysteresis is presented here.

$$V_{IN\_NOM} = 3.3V$$

$$\text{Hysteresis} = 0.5\%$$

$$V_{HYST} = 3.3V * 0.5\% = 0.0165V$$

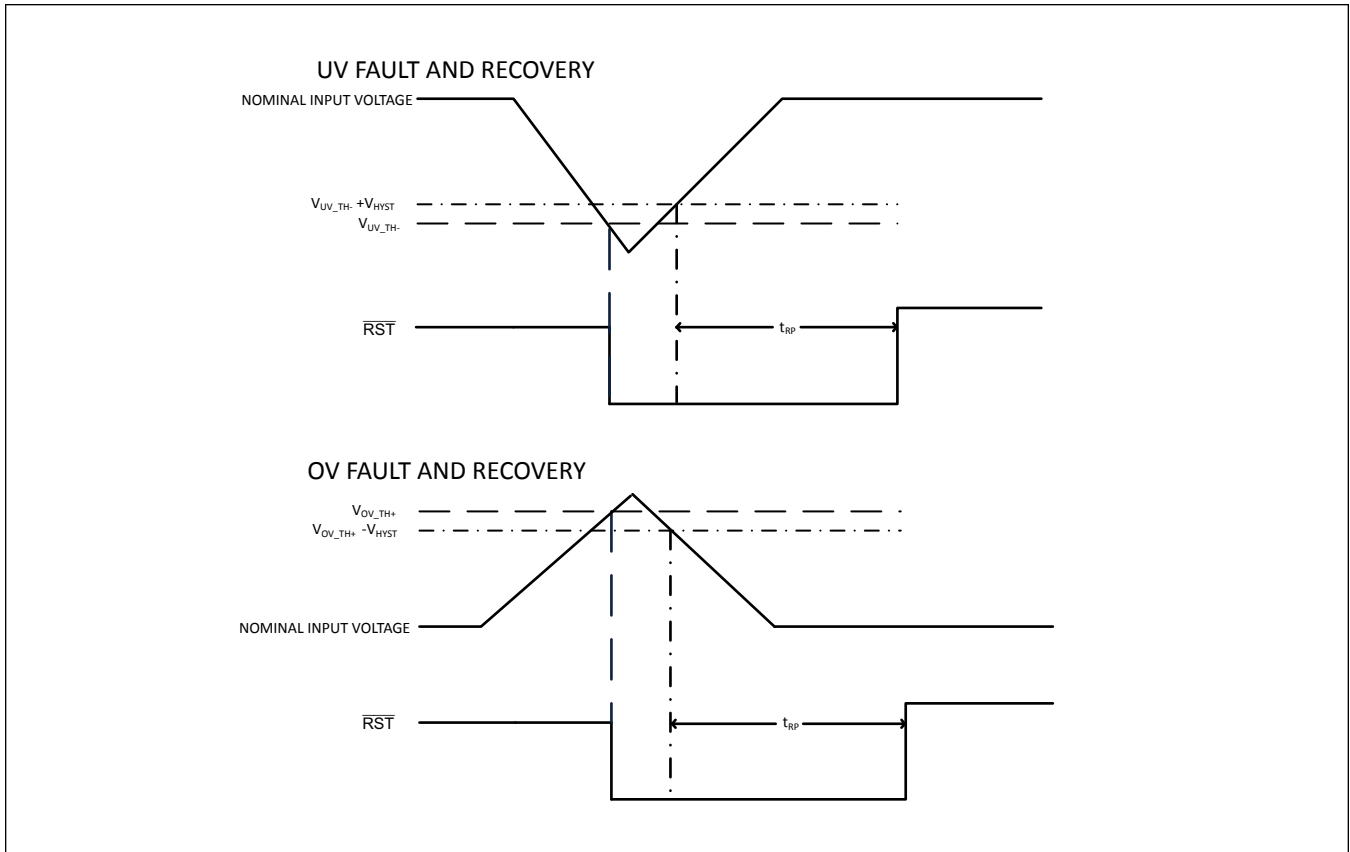


Figure 8. Undervoltage/Overvoltage Threshold Hysteresis

**Power-Supply Bypassing/Noise Immunity**

The MAX16137 operates from a 1.71V to 5.5V supply. Bypass  $V_{DD}$  to ground with a 0.1 $\mu$ F capacitor as close to the device as possible. An additional capacitor improves transient immunity.

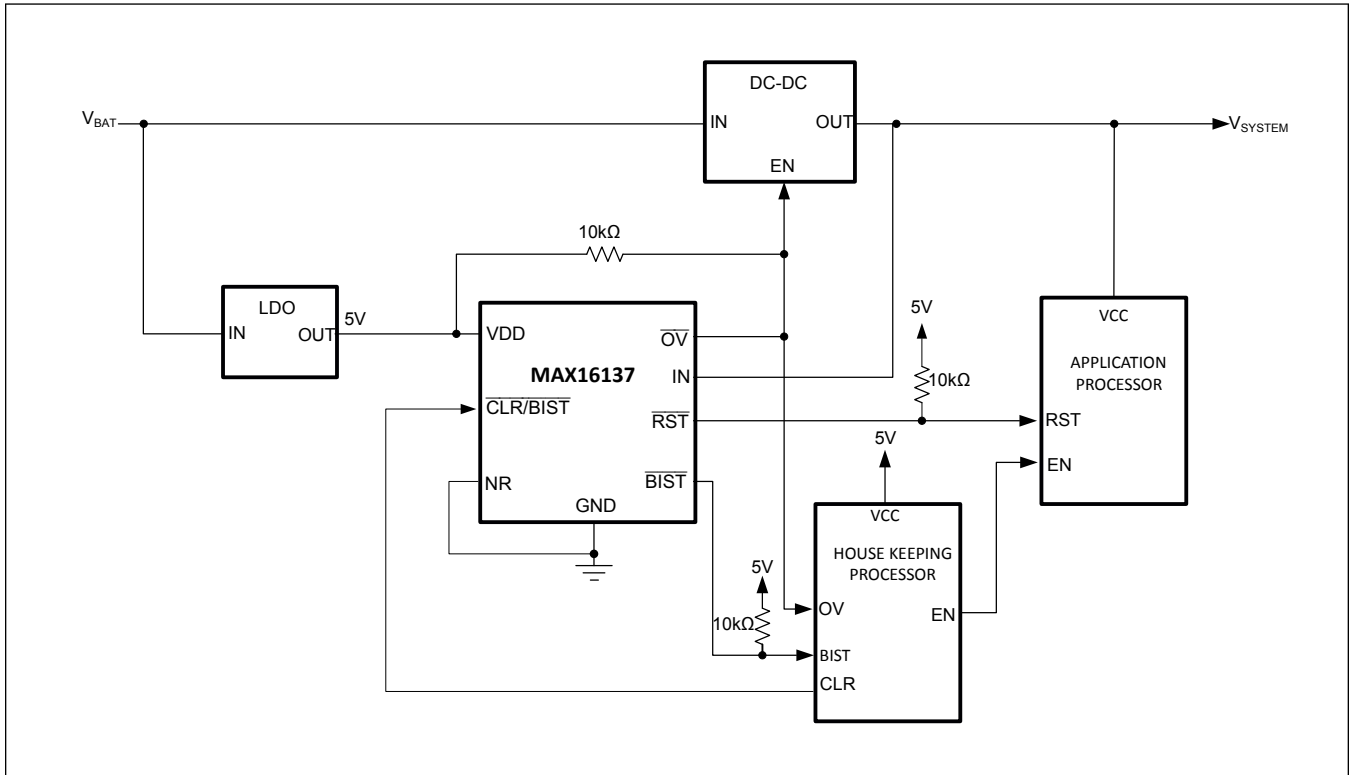
**Selector Guide Table**

**Table 2. Selector Guide Table**

PART NUMBER	THRESHOLD VOLTAGE	TOLERANCE	HYSTERESIS	RESET TIMEOUT
MAX1613700/VY+T	3.3V	7%	0.5%	10ms

Typical Application Circuits

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX1613700/VY+T	-40°C to +125°C	8-TDFN
MAX16137P01/VY+T*	-40°C to +125°C	8-TDFN

*V* denotes automotive grade.

*Y* denotes side-wettable package.

*+* denotes a lead(Pb)-free/RoHS-compliant package.

*T* = Tape and reel.

\* Future product—contact factory for availability.

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/21	Initial release	—

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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