MAX17577, MAX17578 — 4.5V to 60V, 1A High-Efficiency, Synchronous, Inverting Output DC-DC Converters

General Description

The Himalaya series of voltage regulator ICs, power modules, and chargers enable cooler, smaller, and simpler power-supply solutions. The MAX17577 and MAX17578 are high-efficiency, high-voltage, inverting, Himalaya synchronous DC-DC converters with integrated MOSFETs and internal compensation. The devices generate output voltages (V_{OUT}) from -0.9V to -36V and can deliver up to 1A of load current from a wide 4.5V to (60V - $|V_{OUT}|$) input-voltage range.

The devices feature peak current-mode control architecture. The MAX17577 operates in continuous conduction mode (CCM) at all loads; thus, providing a constant frequency operation. The MAX17578 operates in discontinuous conduction mode (DCM) for superior efficiency at light loads. Low minimum on-time allows higher switching frequencies and small solution sizes.

The devices allow the EN/UVLO, $\overline{RESET}$, and RT/SYNC pins to be driven by signals that are referenced to system ground, eliminating the need for external-level shifter circuits. The feedback-voltage regulation accuracy is ±1.3% over a wide -40°C to +125°C temperature range. The devices are available in a compact 12-pin (3mm x 3mm) TDFN package. Simulation models are available.

Applications

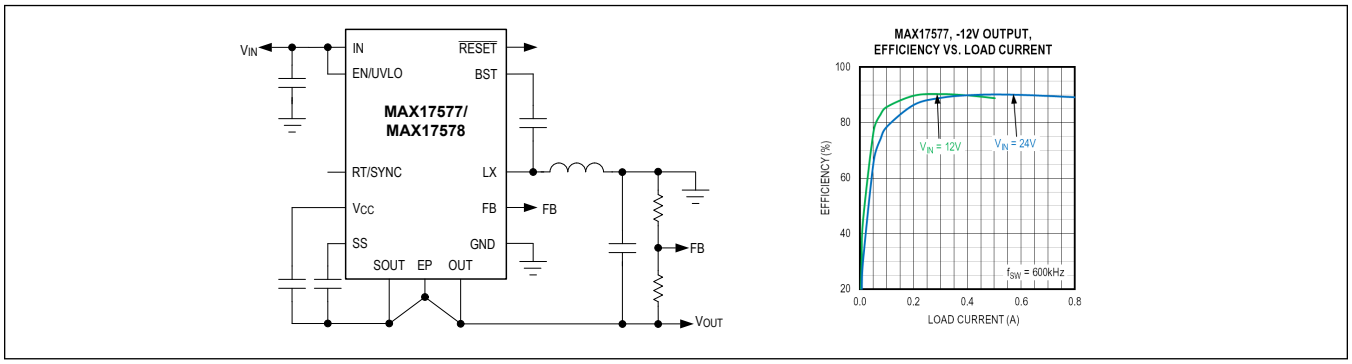
- Industrial Control Power Supply
- General-Purpose Point-of-Load
- Gate-Drive Circuits
- Motion Control
- Wall-Transformer Regulation
- High-Voltage, Single-Board System

Benefits and Features

- Reduces External Components and Total Cost
  - Synchronous Operation
  - All-Ceramic Capacitors, Compact Layout
  - Internal Loop Compensation
  - System Ground Referenced I/O Pins (EN/UVLO, $\overline{RESET}$)
- Flexibility to Support Multiple Rails in a System
  - Adjustable Output Voltage Range from -0.9V to -36V
  - Wide 4.5V to (60V - $|V_{OUT}|$) Input-Voltage Range
  - Up to 1A Output Current
  - 400kHz to 2.2MHz Adjustable Frequency with External Clock Synchronization
- Reduces Power Dissipation
  - 90.6% Peak Efficiency
  - DCM for Superior Light-Load Efficiency
  - 6.2µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Overload Protection
  - Adjustable Soft-Start
  - Monotonic Startup with Prebiased Output Voltage
  - Built-In Output-Voltage Monitoring with $\overline{RESET}$
  - Programmable EN/UVLO Threshold
  - Overtemperature Protection
  - Wide -40°C to +125°C Ambient Operating Temperature Range/ -40°C to +150°C Junction Temperature Range

***Ordering Information* appears at end of data sheet.**

Simplified Application Circuit



19-100840; Rev 0; 10/20

maxim integrated™

Absolute Maximum Ratings

IN, GND, EN/UVLO to OUT ..... -0.3V to +65V
IN to GND ..... -0.3V to +65V
EN/UVLO to GND ..... -0.3V to V_{IN} + 0.3V
RESET to GND ..... -0.3V to +6.5V
LX to OUT ..... -0.3V to (V_{IN} + 0.3V)
RESET, BST to OUT ..... -0.3V to +70V
BST to LX ..... -0.3V to +6.5V
BST to V_{CC} ..... -0.3V to +65V
FB, SS, V_{CC} to SOUT ..... -0.3V to +6.5V
RT/SYNC to SOUT ..... -2V to +6.5V
OUT to SOUT ..... -0.3V to +0.3V
LX Total RMS Current 1.6A
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 24.4mW/°C above +70°C) 1951.2mW
Operating Temperature Range (Note 1) ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN

Package Code	TD1233+1C
Outline Number	21-0664
Land Pattern Number	90-0397
THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2)	
Junction-to-Ambient (θ_{JA})	33ºC/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.5ºC/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 2: Package thermal resistance was obtained using the MAX17578 evaluation kit with no airflow

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, C_{VCC} = 2.2µF, V_{FB} = 1V, RT/SYNC = LX = SS = RESET = Open, V_{BST} to V_{LX} = 5V, V_{GND} = V_{SOUT} = V_{OUT} = 0V, T_A = -40°C to +125°C. Typical values are at T_A = +25°C. All voltages are referenced to SOUT, unless otherwise noted.) (*Note 3*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)						
Input-Voltage Range	V_{IN_GND}	(Referred to GND)	4.5		60 - $\lvert V_{OUT} \rvert$	V
Input-Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (referred to GND), shutdown mode		6.2	10	µA
No-Load Input Current	I_{NO_LOAD}	MAX17577, Normal Switching Mode		6.3		mA
		MAX17578		1.5	2	
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising (referred to GND)	1.165	1.229	1.275	V
	V_{ENF}	$V_{EN/UVLO}$ falling (referred to GND)	1.04	1.09	1.14	
EN/UVLO Input-Leakage Current	I_{ENLKG}	$V_{EN/UVLO}$ = GND, T_A = +25°C	-50	0	+50	nA

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, C_{VCC} = 2.2µF, V_{FB} = 1V, RT/SYNC = LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 5V, V_{GND} = V_{SOUT} = V_{OUT} = 0V, T_A = -40°C to +125°C. Typical values are at T_A = +25°C. All voltages are referenced to SOUT, unless otherwise noted.) (*Note 3*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO (V_{CC})						
V_{CC} Output Voltage	V_{CC}	1mA < I_{VCC} < 15mA	4.75	5	5.25	V
		6V ≤ V_{IN} ≤ 60V; I_{VCC} = 1mA	4.75	5	5.25	
V_{CC} Current Limit	I_{VCC_MAX}	V_{CC} = 4.3V, V_{IN} = 6.5V	25	60	100	mA
V_{CC} Dropout	V_{CC_DO}	V_{IN} = 4.5V, I_{VCC}=15mA			0.35	V
V_{CC} UVLO	V_{CC_UVR}	V_{CC} rising	4.05	4.2	4.3	V
	V_{CC_UVF}	V_{CC} falling	3.65	3.8	3.9	
HIGH-SIDE AND LOW-SIDE MOSFETS						
High-Side nMOSFET On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A, Sourcing		330	660	mΩ
Low-Side nMOSFET On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A,Sinking		163	325	mΩ
LX Leakage Current	I_{LXLKG}	V_{LX} = (V_{OUT} + 1V) to (V_{IN} - 1V), T_A = +25°C	-2		+2	µA
SOFT-START (SS)						
Charging Current	I_{SS}	V_{SS} = 0.5V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB-REG}		0.888	0.9	0.912	V
FB Input-Bias Current	I_{FB}	0 ≤ V_{FB} ≤ 1V, T_A = +25°C	-50		+50	nA
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		2.15	2.4	2.65	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$		2.3	2.65	3	A
Sink Current-Limit Threshold	$I_{SINK-LIMIT}$	MAX17577		-0.9		A
		MAX17578		0		
SWITCHING FREQUENCY AND EXTERNAL CLOCK SYNCHRONIZATION (RT/SYNC)						
Switching Frequency	f_{SW}	$R_{RT/SYNC}$ = Open	525	600	675	kHz
		$R_{RT/SYNC}$ = 6.81kΩ	365	400	425	
		$R_{RT/SYNC}$ = 10.5kΩ	565	600	635	
		$R_{RT/SYNC}$ = 43.2kΩ	1980	2200	2420	
Minimum On-Time	t_{ON_MIN}			60	80	ns
Minimum Off-Time	t_{OFF_MIN}		140	150	160	ns
LX Dead Time	t_{LX-DT}			5		ns
V_{FB} Hiccup Threshold	$V_{FB-HICF}$	V_{FB} Falling	0.55	0.58	0.61	V
Hiccup Timeout		(*Note 4*)		32768		cycles
Bias Current	I_{RT_BIAS}			60		µA
SYNC Frequency-Capture Range		f_{SW} set by $R_{RT/SYNC}$	1.1 x f_{SW}		1.4 x f_{SW}	kHz

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, C_{VCC} = 2.2µF, V_{FB} = 1V, RT/SYNC = LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 5V, V_{GND} = V_{SOUT} = V_{OUT} = 0V, T_A = -40°C to +125°C. Typical values are at T_A = +25°C. All voltages are referenced to SOUT, unless otherwise noted.) (*Note 3*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Pulse-Width	t_{SYNC}		100			ns
SYNC Threshold	V_{IH}	At RT/SYNC Pin (*Note 5*)	$V_{RT/SYNC}$ + 0.2			V
	V_{IL}	At RT/SYNC Pin (*Note 5*)			$V_{RT/SYNC}$ - 0.2	
SYNC Duty-Cycle Range	D_{SYNC}		10		90	%
SYSTEM GROUND (GND)						
GND Current	I_{GND}	Sourcing		10		µA
$\overline{RESET}$ (REFERRED TO GND)						
$\overline{RESET}$ Output Level Low	V_{RESETL}	$I_{\overline{RESET}}$ = 10mA (Referred to GND)			0.4	V
$\overline{RESET}$ Output-Leakage Current	$I_{RESETLKG}$	T_A = T_J = +25°C, $V_{\overline{RESET}}$ = 5.5V	-0.1		+0.1	µA
FB Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} Rising	93.8	95	97.8	%
FB Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} Falling	90.5	92	94.6	%
$\overline{RESET}$ Delay after FB reaches 95% regulation				1024		Cycles
THERMAL SHUTDOWN						
Thermal Shutdown Rising Threshold	T_{SHDNR}			165		°C
Thermal Shutdown Hysteresis	T_{SHDNHY}			10		°C

Note 3: Electrical specifications are production tested at T_A = +25ºC. Specifications over the entire operating temperature range are guaranteed by design and characterization.

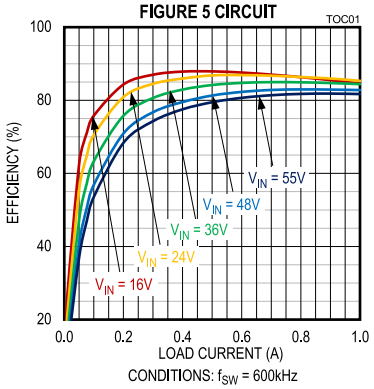
Note 4: See the *Overcurrent Protection (OCP)/Hiccup Mode* section for more details

Note 5: $V_{RT/SYNC}$ = I_{RT_BIAS} × $R_{RT/SYNC}$. See the *Switching Frequency and External Clock Synchronization (RT/SYNC)* section for more details.

Typical Operating Characteristics

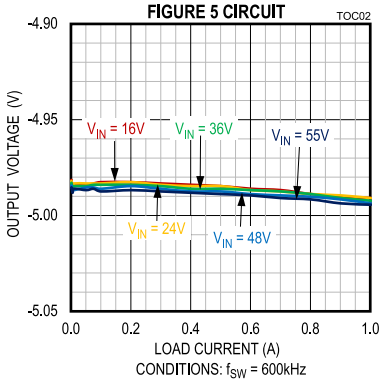
(V_{GND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17577, -5V OUTPUT, EFFICIENCY vs. LOAD CURRENT, FIGURE 5 CIRCUIT



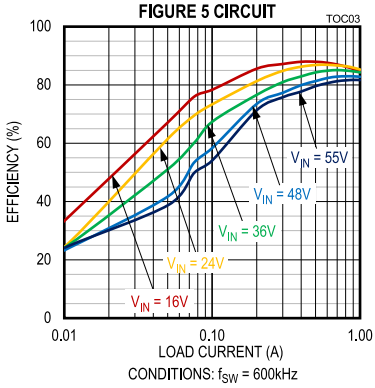
CONDITIONS: f_{SW} = 600kHz

MAX17577, -5V OUTPUT, LOAD AND LINE REGULATION, FIGURE 5 CIRCUIT



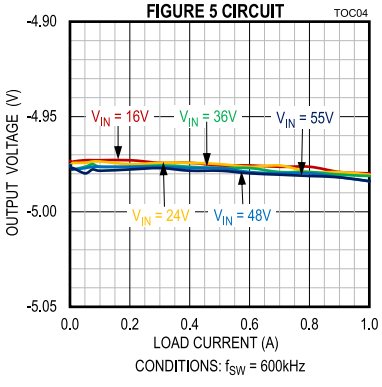
CONDITIONS: f_{SW} = 600kHz

MAX17578, -5V OUTPUT, EFFICIENCY vs. LOAD CURRENT, FIGURE 5 CIRCUIT



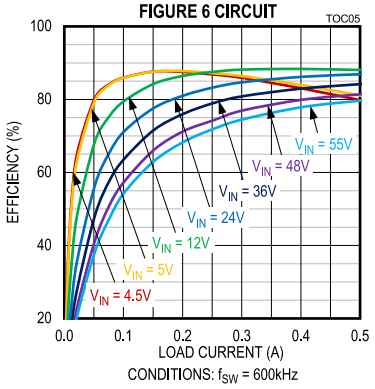
CONDITIONS: f_{SW} = 600kHz

MAX17578, -5V OUTPUT, LOAD AND LINE REGULATION, FIGURE 5 CIRCUIT



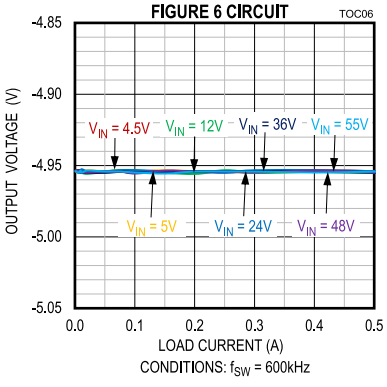
CONDITIONS: f_{SW} = 600kHz

MAX17577, -5V OUTPUT, EFFICIENCY vs. LOAD CURRENT, FIGURE 6 CIRCUIT



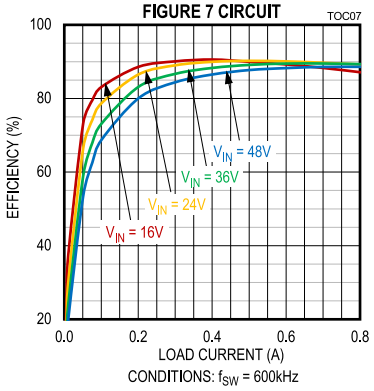
CONDITIONS: f_{SW} = 600kHz

MAX17577, -5V OUTPUT, LOAD AND LINE REGULATION, FIGURE 6 CIRCUIT



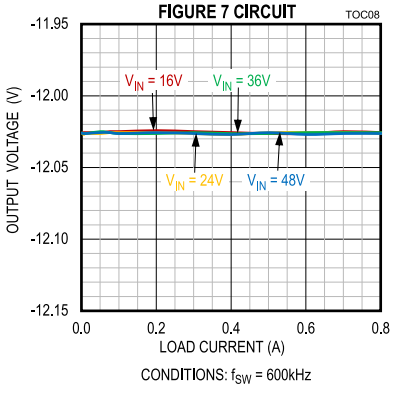
CONDITIONS: f_{SW} = 600kHz

MAX17577, -12V OUTPUT, EFFICIENCY vs. LOAD CURRENT, FIGURE 7 CIRCUIT



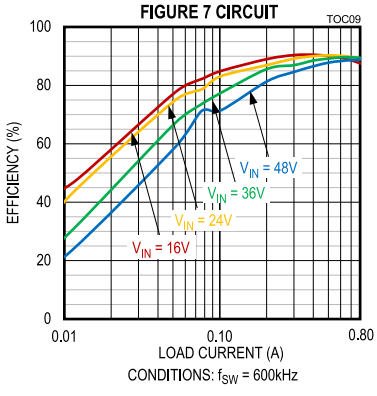
CONDITIONS: f_{SW} = 600kHz

MAX17577, -12V OUTPUT, LOAD AND LINE REGULATION, FIGURE 7 CIRCUIT



CONDITIONS: f_{SW} = 600kHz

MAX17578, -12V OUTPUT, EFFICIENCY vs. LOAD CURRENT, FIGURE 7 CIRCUIT

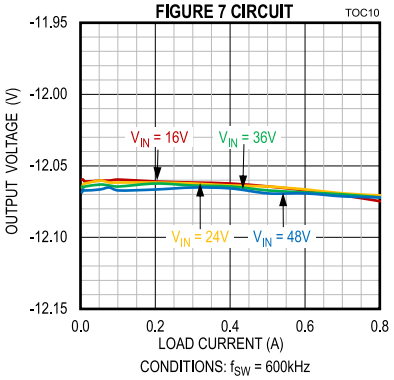


CONDITIONS: f_{SW} = 600kHz

Typical Operating Characteristics (continued)

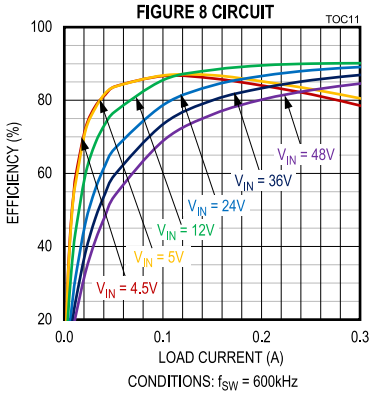
(V_{GND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17578, -12V OUTPUT, LOAD AND LINE REGULATION, FIGURE 7 CIRCUIT



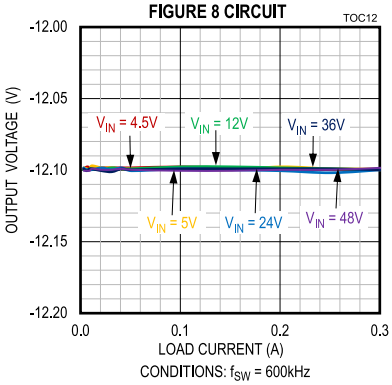
CONDITIONS: f_{SW} = 600kHz

MAX17577, -12V OUTPUT, EFFICIENCY vs. LOAD CURRENT, FIGURE 8 CIRCUIT



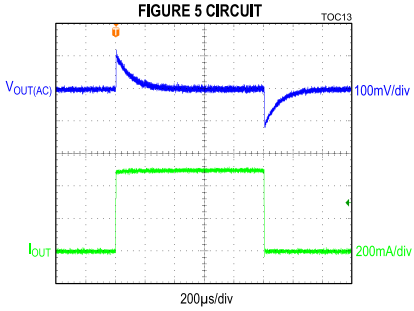
CONDITIONS: f_{SW} = 600kHz

MAX17577, -12V OUTPUT, LOAD AND LINE REGULATION, FIGURE 8 CIRCUIT



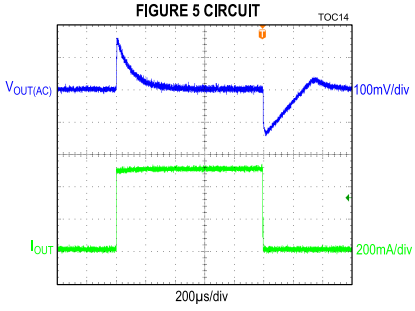
CONDITIONS: f_{SW} = 600kHz

MAX17577, -5V OUTPUT, LOAD TRANSIENT BETWEEN 0A AND 0.5A, FIGURE 5 CIRCUIT



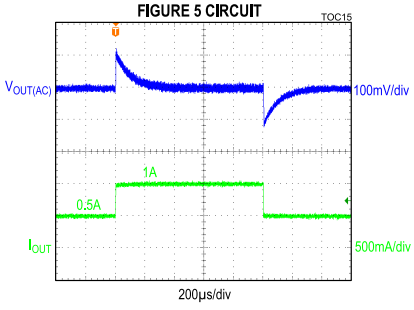
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V

MAX17578, -5V OUTPUT, LOAD TRANSIENT BETWEEN 10mA AND 0.5A, FIGURE 5 CIRCUIT



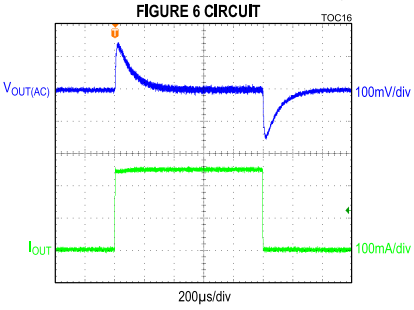
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V

MAX17577/MAX17578, -5V OUTPUT, LOAD TRANSIENT BETWEEN 0.5A AND 1A, FIGURE 5 CIRCUIT



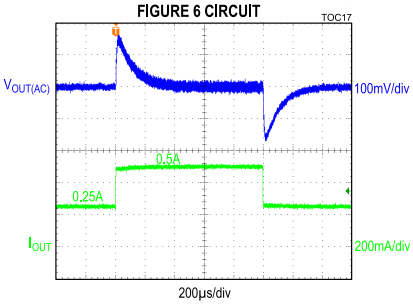
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V

MAX17577, -5V OUTPUT, LOAD TRANSIENT BETWEEN 0A AND 0.25A, FIGURE 6 CIRCUIT



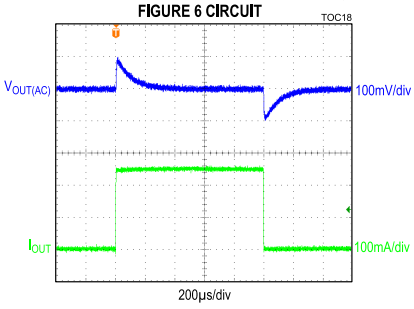
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 5V

MAX17577, -5V OUTPUT, LOAD TRANSIENT BETWEEN 0.25A AND 0.5A, FIGURE 6 CIRCUIT



CONDITIONS: f_{SW} = 600kHz, V_{IN} = 5V

MAX17577, -5V OUTPUT, LOAD TRANSIENT BETWEEN 0A AND 0.25A, FIGURE 6 CIRCUIT

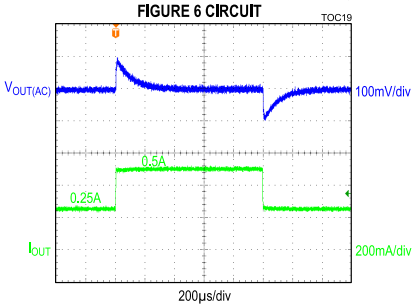


CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V

Typical Operating Characteristics (continued)

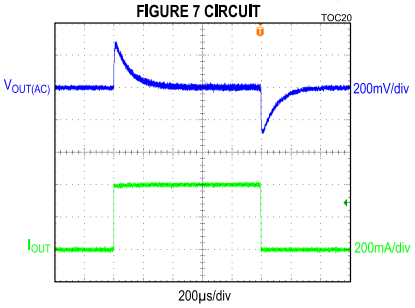
(V_{GND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17577, -5V OUTPUT, LOAD TRANSIENT BETWEEN 0.25A AND 0.5A, FIGURE 6 CIRCUIT



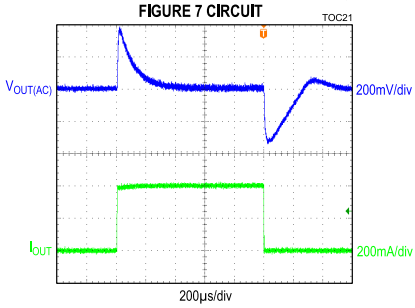
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V

MAX17577, -12V OUTPUT, LOAD TRANSIENT BETWEEN 0A AND 0.4A, FIGURE 7 CIRCUIT



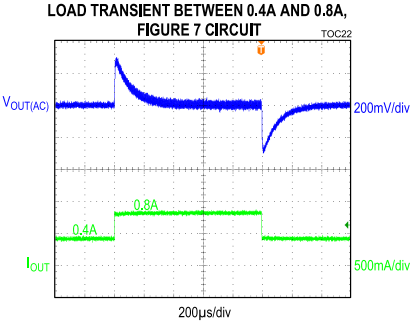
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V

MAX17578, -12V OUTPUT, LOAD TRANSIENT BETWEEN 8mA AND 0.4A, FIGURE 7 CIRCUIT



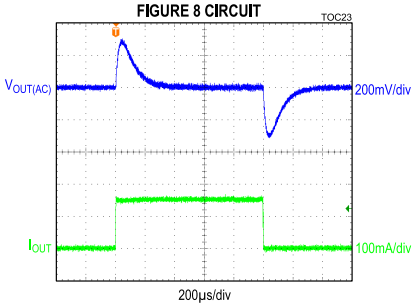
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V

MAX17577/MAX17578, -12V OUTPUT, LOAD TRANSIENT BETWEEN 0.4A AND 0.8A, FIGURE 7 CIRCUIT



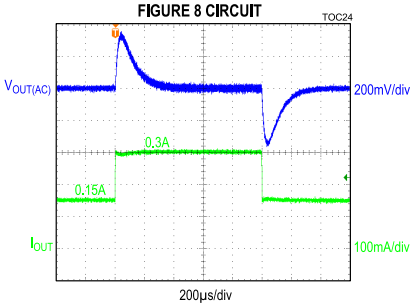
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V

MAX17577, -12V OUTPUT, LOAD TRANSIENT BETWEEN 0A AND 0.15A, FIGURE 8 CIRCUIT



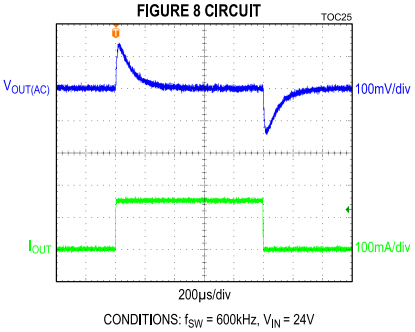
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 5V

MAX17577, -12V OUTPUT, LOAD TRANSIENT BETWEEN 0.15A AND 0.3A, FIGURE 8 CIRCUIT



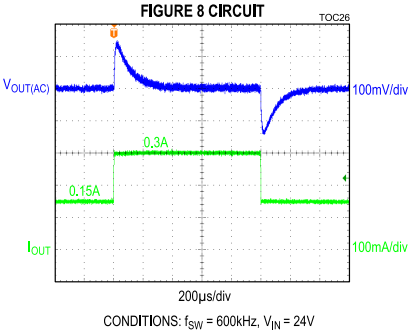
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 5V

MAX17577, -12V OUTPUT, LOAD TRANSIENT BETWEEN 0A AND 0.15A, FIGURE 8 CIRCUIT



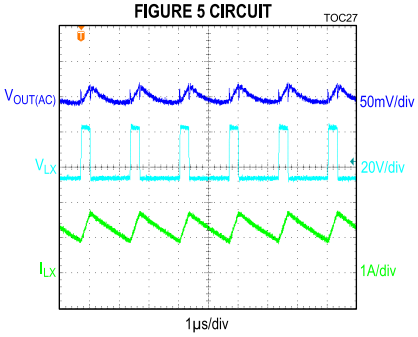
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V

MAX17577, -12V OUTPUT, LOAD TRANSIENT BETWEEN 0.15A AND 0.3A, FIGURE 8 CIRCUIT



CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V

MAX17577/MAX17578, -5V OUTPUT, STEADY-STATE, FIGURE 5 CIRCUIT

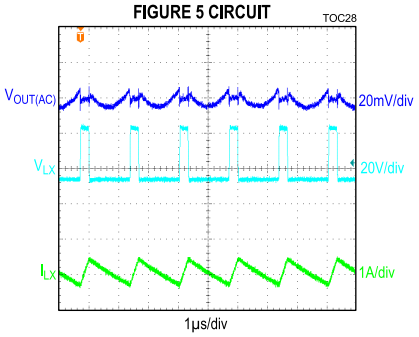


CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 1A LOAD

Typical Operating Characteristics (continued)

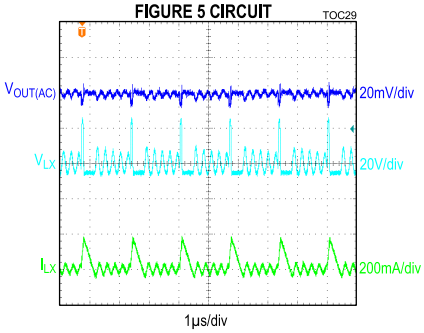
(V_{GND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17577, -5V OUTPUT, STEADY-STATE, FIGURE 5 CIRCUIT



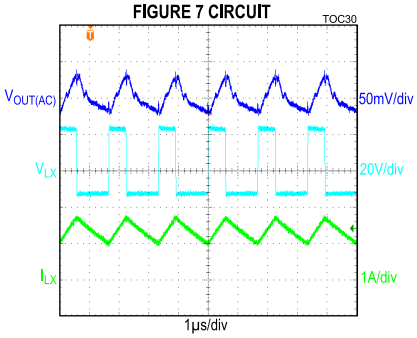
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, NO LOAD

MAX17578, -5V OUTPUT, STEADY-STATE, FIGURE 5 CIRCUIT



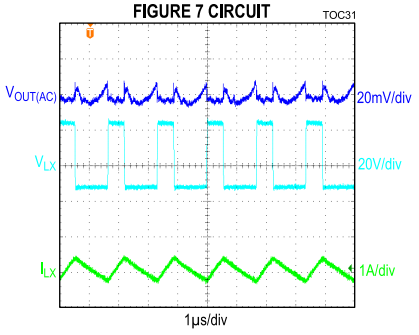
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 10mA LOAD

MAX17577/MAX17578, -12V OUTPUT, STEADY-STATE, FIGURE 7 CIRCUIT



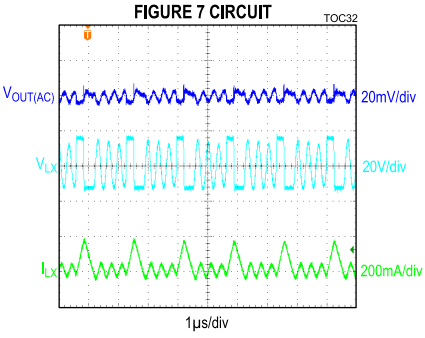
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 0.8A LOAD

MAX17577, -12V OUTPUT, STEADY-STATE, FIGURE 7 CIRCUIT



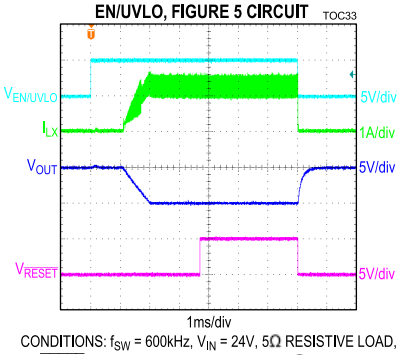
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, NO LOAD

MAX17578, -12V OUTPUT, STEADY-STATE, FIGURE 7 CIRCUIT



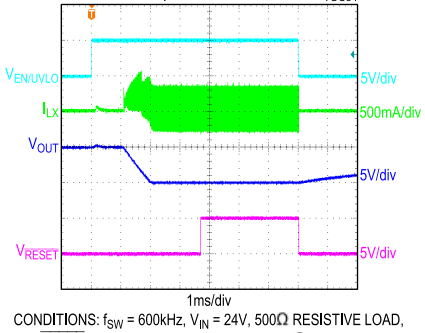
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 8mA LOAD

MAX17577/MAX17578, -5V OUTPUT, SOFT-START AND SHUTDOWN THROUGH EN/UVLO, FIGURE 5 CIRCUIT



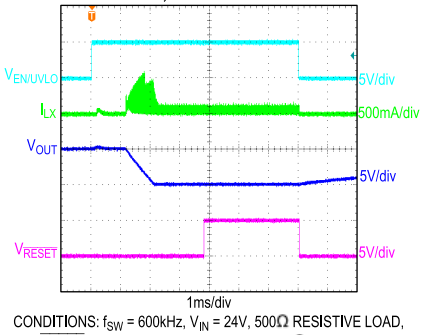
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 5Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

MAX17577, -5V OUTPUT, SOFT-START AND SHUTDOWN THROUGH EN/UVLO, FIGURE 5 CIRCUIT



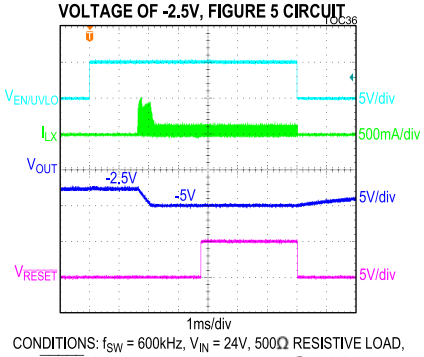
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 500Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

MAX17578, -5V OUTPUT, SOFT-START AND SHUTDOWN THROUGH EN/UVLO, FIGURE 5 CIRCUIT



CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 500Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

MAX17578, -5V OUTPUT, SOFT-START AND SHUTDOWN WITH PREBIAS VOLTAGE OF -2.5V, FIGURE 5 CIRCUIT

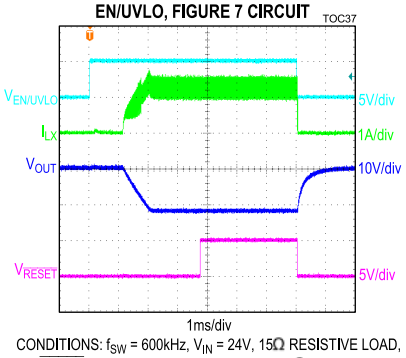


CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 500Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

Typical Operating Characteristics (continued)

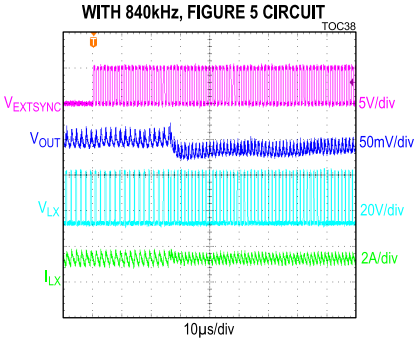
(V_{GND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

MAX17577/MAX17578, -12V OUTPUT, SOFT-START AND SHUTDOWN THROUGH EN/UVLO, FIGURE 7 CIRCUIT



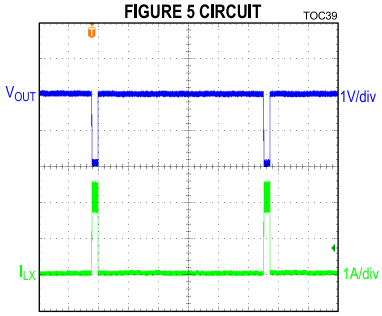
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 15Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO 5V WITH A 10kΩ RESISTOR

MAX17577/MAX17578, -5V OUTPUT, EXTERNAL CLOCK SYNCHRONIZATION WITH 840kHz, FIGURE 5 CIRCUIT



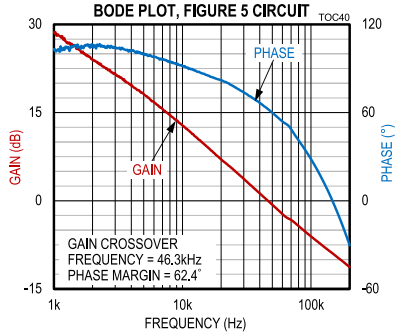
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 1A LOAD, FIGURE 1 CIRCUIT, $R_{RT/SYNC}$ = 10.5kΩ

MAX17577/MAX17578, -5V OUTPUT, OVERLOAD PROTECTION FIGURE 5 CIRCUIT



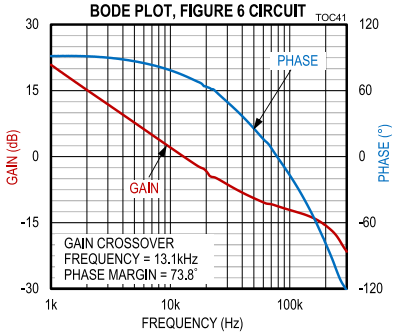
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 1Ω RESISTIVE LOAD

MAX17577/MAX17578, -5V OUTPUT, BODE PLOT, FIGURE 5 CIRCUIT



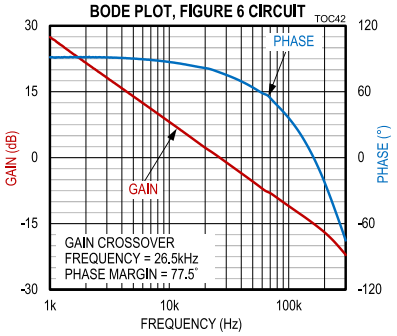
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 5Ω RESISTIVE LOAD

MAX17577, -5V OUTPUT, BODE PLOT, FIGURE 6 CIRCUIT



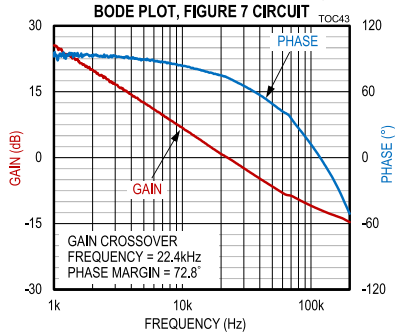
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 5V, 10Ω RESISTIVE LOAD

MAX17577, -5V OUTPUT, BODE PLOT, FIGURE 6 CIRCUIT



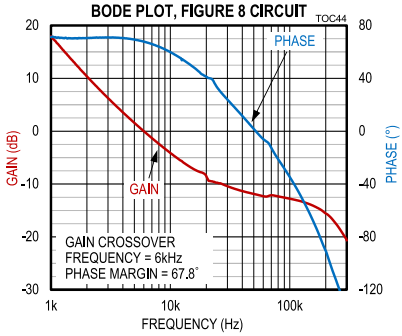
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 10Ω RESISTIVE LOAD

MAX17577/MAX17578, -12V OUTPUT, BODE PLOT, FIGURE 7 CIRCUIT



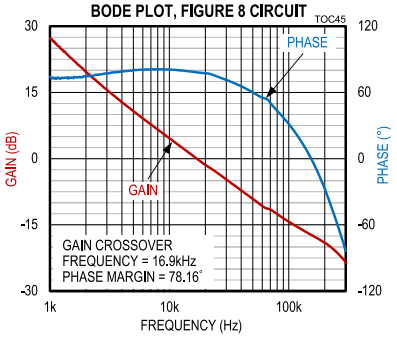
CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 15Ω RESISTIVE LOAD

MAX17577, -12V OUTPUT, BODE PLOT, FIGURE 8 CIRCUIT



CONDITIONS: f_{SW} = 600kHz, V_{IN} = 5V, 40Ω RESISTIVE LOAD

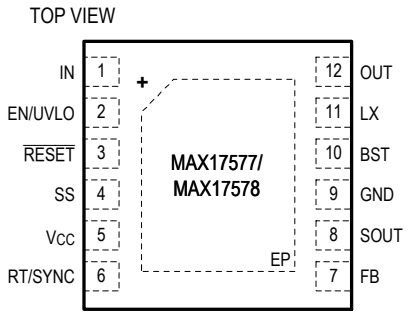
MAX17577, -12V OUTPUT, BODE PLOT, FIGURE 8 CIRCUIT



CONDITIONS: f_{SW} = 600kHz, V_{IN} = 24V, 40Ω RESISTIVE LOAD

Pin Configuration

MAX17577, MAX17578



TDFN-EP
3mm x 3mm

Pin Description

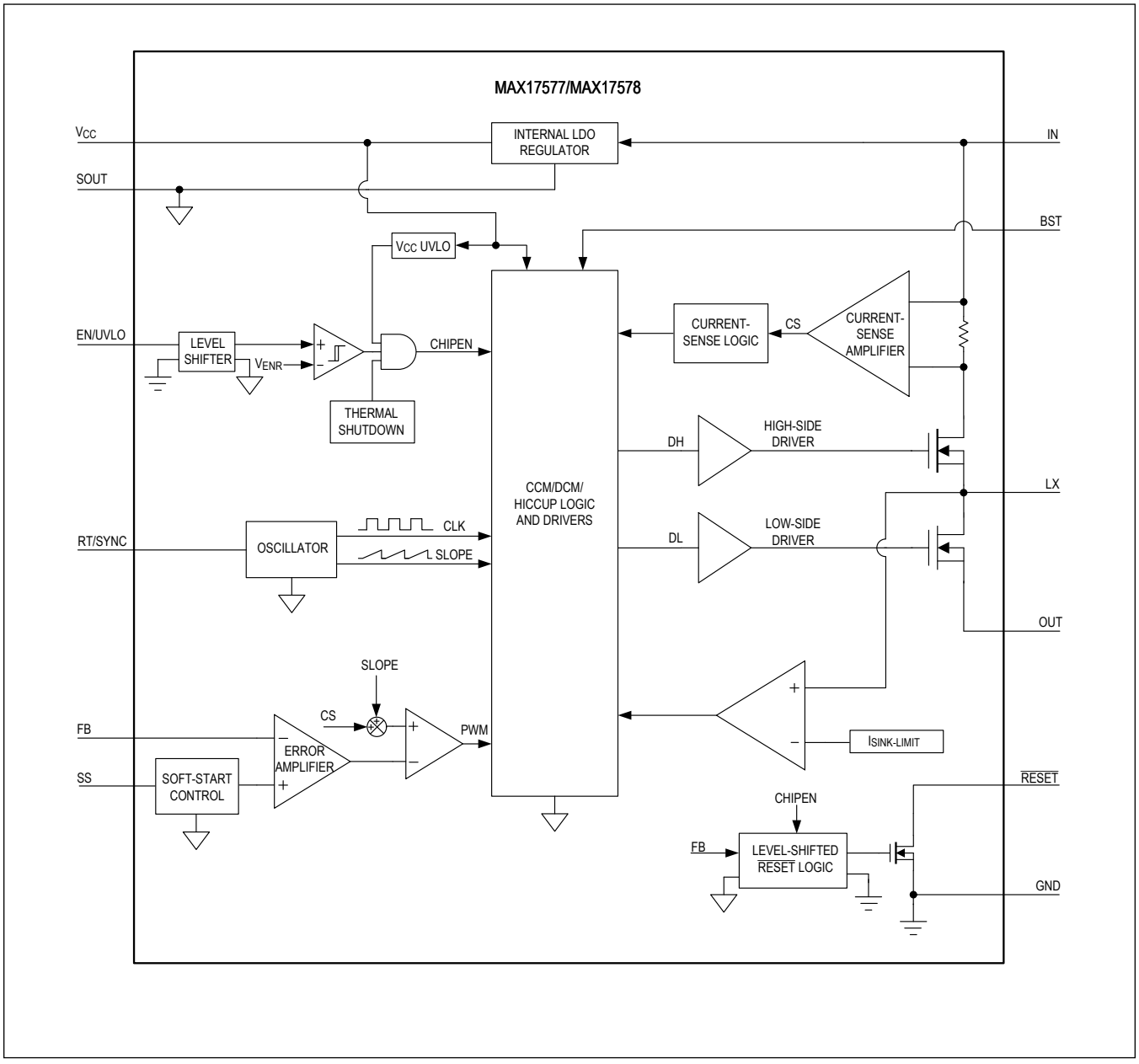
PIN	NAME	FUNCTION
1	IN	Power Supply Input Pin. Decouple the IN pin to GND with a minimum of 2.2µF X7R ceramic capacitor. Place the capacitor close to the IN and GND pins.
2	EN/UVLO	Enable/Undervoltage-Lockout Input Pin. Drive EN/UVLO high to enable the converter. Connect to the midpoint of a resistor divider connected between the IN and GND pins to set the input voltage above which the device turns on. Connect to the IN pin for always on operation. Pull low to GND to disable the device.
3	$\overline{\text{RESET}}$	Active-Low Open-Drain Status Output Pin. The $\overline{\text{RESET}}$ output is driven low to GND if the output voltage drops below 92% of its set value. $\overline{\text{RESET}}$ goes high 1024 cycles after the output voltage rises above 95% of its set value. Connect a pullup resistor of 10kΩ from the $\overline{\text{RESET}}$ pin to an external power supply for monitoring the output voltage status.
4	SS	Soft-Start Input Pin. Connect a capacitor from the SS pin to SOUT pin to set the soft-start time.
5	V_{CC}	5V Internal LDO Output Pin. Bypass V_{CC} with a 2.2µF ceramic capacitor to SOUT. LDO does not support the external loading on V_{CC}.
6	RT/SYNC	Switching Frequency Programming Input/External Clock Synchronization Input Pin. Connect a resistor from RT/SYNC to SOUT to set the internal clock frequency between 400kHz and 2.2MHz. Leave RT/SYNC open for the default 600kHz switching frequency. The RT/SYNC pin can also be used to synchronize the converter to an external clock. See the *Switching Frequency and External Clock Synchronization* section for more details.
7	FB	Feedback Input Pin. Connect FB to the center node of a resistor divider between the GND node and output-voltage node. See the *Adjusting Output Voltage* section for details.
8	SOUT	Reference Node for Internal Control Circuitry. Connect SOUT to an output capacitor with a Kelvin connection. Refer to the MAX17577 or MAX17578 evaluation kit data sheets for a layout example.
9	GND	System Ground Pin. Connect GND to the power ground plane. Connect all the circuit ground connections together at a single point. Refer to the MAX17577 or MAX17578 evaluation kit data sheets for a layout example.
10	BST	Bootstrap Capacitor Pin. Connect a minimum of 0.1µF ceramic capacitor between the BST and LX pins.
11	LX	Switching Node. Connect the LX pin to the switching side of the inductor. LX is high-impedance when the device is shut down.

Pin Description (continued)

PIN	NAME	FUNCTION
12	OUT	Negative Output Node. Switching current path for low-side nMOSFET. Connect the output capacitor from the OUT pin to system ground. Refer to the MAX17577 or MAX17578 evaluation kit data sheets for a layout example.
—	EP	Exposed Pad. Connect to the SOUT pin. Connect EP to a large copper plane with several thermal vias below the device to improve the heat dissipation capability. Refer to the MAX17577 or MAX17578 evaluation kit data sheets for an example of the correct method for EP connection and thermal vias.

Functional Diagrams

MAX17577/MAX17578 Block Diagram



Detailed Description

The MAX17577 and MAX17578 are high-efficiency, high-voltage, inverting, Himalaya synchronous inverting DC-DC converters with integrated MOSFETs operating over a wide 4.5V to (60V - $|V_{OUT}|$) input-voltage range. The devices can deliver up to 1A current and generate output voltages ranging from -0.9V to -36V. The feedback-voltage regulation accuracy is ±1.3% over a wide -40°C to +125°C temperature range.

The devices feature a peak current-mode control architecture with internal loop compensation. At the rising edge of each clock, the high-side MOSFET turns on and the inductor current ramps up. An internal error amplifier compares a fraction of the output voltage at the FB pin to an internal reference. To program the duty cycle of the converter, the output of the error amplifier sets the peak current in the inductor at which the high-side MOSFET turns off, and the low-side MOSFET turns on. During the rest of the switching cycle, stored energy in the inductor is released to the output as its current ramps down. An adjustable input enable/undervoltage-lockout (EN/UVLO) pin programs the desired input voltage at which the converter turns on/off. The soft-start (SS) pin can be used to reduce inrush currents during startup. An open-drain status output ($\overline{RESET}$) pin monitors the output voltage and pulls high to indicate that the output voltage is in regulation. The devices feature a RT/SYNC pin that can be used to program the switching frequency or to synchronize the device to an external clock. Low minimum on-time allows high switching frequencies and small solution sizes.

The MAX17577 operate in continuous conduction mode (CCM) at all loads; thus, providing a constant frequency operation. The MAX17578 operates in discontinuous conduction mode (DCM) for superior efficiency at light loads. In CCM mode, the inductor current is allowed to go negative. CCM operation provides constant frequency operation at all loads and is useful in applications sensitive to switching frequency. DCM mode of operation offers superior efficiency at light loads by disabling any negative inductor current.

Switching Frequency and External Clock Synchronization

The switching frequency of the MAX17577 and MAX17578 can be programmed from 400kHz to 2.2MHz with a resistor connected from the RT/SYNC pin to the SOUT pin. Calculate the value of the resistor at the RT/SYNC pin ($R_{RT/SYNC}$) for a desired switching frequency (f_{SW}) using the following equation.

$$R_{RT/SYNC} = \frac{340}{\left(\frac{20000}{f_{SW}}\right) - 1}$$

Where $R_{RT/SYNC}$ is in kΩ and f_{SW} is in kHz. Leave the RT/SYNC pin open for a default f_{SW} of 600kHz. See Table 1 for $R_{RT/SYNC}$ resistor values for a few common switching frequencies.

Table 1. Switching Frequency vs. $R_{RT/SYNC}$ Resistor

SWITCHING FREQUENCY (kHz)	$R_{RT/SYNC}$ RESISTOR (kΩ)
600	Open
600	10.5
400	6.81
2200	43.2

The RT/SYNC pin can be used to synchronize the internal oscillator of the device to an external clock as shown in Figure 1. When the external clock synchronization feature is used, always connect the $R_{RT/SYNC}$ resistor. The external clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the switching frequency programmed by the resistor connected at the RT/SYNC pin. When an external clock is applied to the RT/SYNC pin, the internal oscillator frequency changes to an external clock frequency after 16 internal oscillator cycles if at least 8 external clock cycles are applied. The external clock source can either be referenced to the GND or SOUT node. The external clock pulse-width should be more than 100ns (t_{SYNC}) and the allowable duty cycle (D_{SYNC}) range is 10% to 90%.

The external clock signal is AC-coupled onto the RT/SYNC pin. The amplitude of the external clock (V_{SYNCPK_PK}) should be chosen based on the following equation.

$V_{SYNCPK\_PK} > 1.3V$ for $20\% \le D_{SYNC} \le 80\%$

$V_{SYNCPK\_PK} > \frac{0.26}{D_{SYNC}}$ for $10\% \le D_{SYNC} < 20\%$

$V_{SYNCPK\_PK} > \frac{0.26}{1 - D_{SYNC}}$ for $80\% < D_{SYNC} \le 90\%$

The value of C_{SYNC} can be calculated using the following equation.

$$C_{SYNC} = \frac{45}{\left(V_{SYNCPK\_PK}\right) - 1}$$

where C_{SYNC} is in pF.

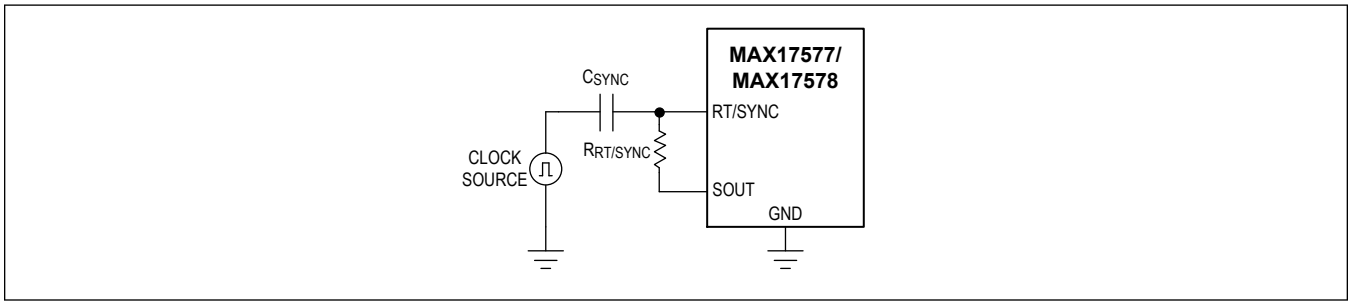


Figure 1. Synchronization to an External Clock

Linear Regulator (V_{CC})

The MAX17577 and MAX17578 have an internal low dropout (LDO) regulator that is referenced to SOUT and powers V_{CC}. This LDO is enabled during power-up or when EN/UVLO is above 0.8V (typ) with respect to GND. V_{CC} powers internal control circuitry. Bypass V_{CC} to SOUT with a 2.2µF low-ESR ceramic capacitor. The MAX17577 and MAX17578 commence operation when $V_{CC} > V_{CC-UVR}$ (4.2V) and turns OFF when $V_{CC} < V_{CC-UVF}$ (3.8V).

Operating Input-Voltage Range

The minimum operating-input voltage ($V_{IN(MIN)}$) for a given output-voltage setting is calculated using the following equation.

$$V_{IN(MIN)} = \frac{\left|V_{OUT}\right| \times \left(1 - D_{MAX}\right)}{D_{MAX}} + \frac{1.5A}{D_{MAX}}\left(R_{DCR(MAX)} + \left(1 - D_{MAX}\right) \times R_{DS-ONL(MAX)} + D_{MAX} \times R_{DS-ONH(MAX)}\right)$$

$V_{IN(MIN)}$ cannot be less than 4.5V.

To comply with internal device ratings, the maximum operating-input voltage ($V_{IN(MAX)}$) for a given output-voltage setting is limited to 60V - $|V_{OUT}|$. For example, the maximum permissible input voltage for a -12V output specification would be 48V. Thus, the value of the $V_{IN(MAX)}$ is given by the following equation.

$$V_{IN(MAX)} = \text{Lower of } (60V - |V_{OUT}|) \text{ or } \frac{\left|V_{OUT}\right| \times (1 - t_{ON\_MIN(MAX)} \times f_{SW})}{t_{ON\_MIN(MAX)} \times f_{SW}}$$

where:

V_{OUT} = Steady-state output voltage

$R_{DCR(MAX)}$ = Worst-case DC-resistance of the inductor

$R_{DS-ONH(MAX)}$ = Worst-case on-state resistance of the high-side internal MOSFET

$R_{DS-ONL(MAX)}$ = Worst-case on-state resistance of the low-side internal MOSFET

D_{MAX} = Maximum duty cycle of the converter

$D_{MAX} = 1 - t_{OFF\_MIN(MAX)} \times f_{SW}$

$t_{OFF\_MIN(MAX)}$ = Worst-case minimum switch off-time (160ns)

$t_{ON\_MIN(MAX)}$ = Worst-case minimum switch on-time (80ns)

f_{SW} = Operating switching frequency.

Overcurrent Protection (OCP)/Hiccup Mode

The MAX17577 and MAX17578 are provided with a robust overcurrent protection (OCP) scheme that protects the converter under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET when the high-side switch current exceeds an internal limit of $I_{PEAK-LIMIT}$ (2.4A). A runaway current limit on the high-side switch current at $I_{RUNAWAY-LIMIT}$ (2.65A) protects the device under output short-circuit conditions at high input voltages when there is insufficient output voltage available to restore the inductor current built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. Additionally, if the feedback voltage drops below $V_{FB-HICF}$ any time after soft-start is complete, hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles at half the programmed switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under an overload condition, if feedback voltage does not exceed $V_{FB-HICF}$, the device switches at half the programmed switching frequency for the time duration of the programmed soft-start time and the subsequent 1024 clock cycles. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

$\overline{\text{RESET}}$ Output

The MAX17577 and MAX17578 include a $\overline{\text{RESET}}$ comparator to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the regulator output increases above 95% of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below 92% of the nominal regulated voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown or when the EN/UVLO pin goes below V_{ENF}.

Prebiased Output

When the MAX17577 and MAX17578 start into a prebiased output, both the high-side and low-side nMOSFETs are turned off so that the converter does not sink current from the output. The switching of the nMOSFETs commence only after the voltage at the SS pin (V_{SS}) crosses the voltage at the feedback pin (V_{FB}). V_{FB} then smoothly ramps up to V_{FB-REG} in alignment with the V_{SS} and the output voltage reaches its target value.

Thermal-Shutdown Protection

The MAX17577 and MAX17578 offer thermal shutdown protection to limit the junction temperature.When the junction temperature of the device exceeds +165ºC, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10ºC. Soft-start is deasserted during thermal shutdown and initiates the start-up operation when the device recovers from thermal shutdown. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid undesired triggering of the thermal shutdown during normal operation.

Applications Information

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). Calculate the inductor value for a given output voltage and switching frequency using the following equation.

$$L = \frac{|V_{OUT}| \times 1.1}{f_{SW}}$$

where V_{OUT} and f_{SW} are nominal values and f_{SW} is in Hz. Select an inductor whose value is nearest to the value calculated by the above formula. Select a low-loss inductor with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation occurs only above the peak current limit threshold ($I_{PEAK-LIMIT}$).

Load Current Capability ($I_{OUT(MAX)}$)

The deliverable load current ($I_{OUT(MAX)}$) depends on converter operating parameters and maximum operating duty cycle (D_{MAX_OP}), which in turn depends on the designed minimum operating-input voltage ($V_{IN(MIN)\_OP}$). $I_{OUT(MAX)}$ in A is given by the following equation:

$$I_{OUT(MAX)} = 1.5A \times (1 - D_{MAX\_OP})$$

where,

$$D_{MAX\_OP} = \frac{|V_{OUT}| + 1.5A \times (R_{DCR(MAX)} + R_{DS\text{-}ONL(MAX)})}{V_{IN(MIN)\_OP} + |V_{OUT}| - 1.5A \times (R_{DS\text{-}ONH(MAX)} - R_{DS\text{-}ONL(MAX)})}$$

$V_{IN(MIN)\_OP}$ = Designed minimum operating-input voltage, which is ≥ $V_{IN(MIN)}$ (calculated in the *Operating Input-Voltage Range* section).

Input Capacitor Selection

The input filter capacitor connected between the IN and GND pins reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the converter switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \sqrt{\frac{D_{MAX\_OP}}{1 - D_{MAX\_OP}}}$$

I_{RMS} has a maximum value at maximum duty cycle.

Choose an input capacitor that exhibits less than +10°C temperature rise at the maximum RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability.

Calculate the input capacitance using the following equation.

$$C_{IN} = \frac{I_{OUT(MAX)} \times D_{MAX\_OP}}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

f_{SW} = Switching frequency

ΔV_{IN} = Allowable input-voltage ripple

η = Efficiency

In applications where the source is located distant from the device input, an appropriate electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the

inductance of the longer input cables and the input ceramic capacitor. Actual derating of ceramic capacitors with DC-bias voltage must be considered while selecting the input capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Output-Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output-voltage deviation is contained to 3% of the output voltage.

The procedure to calculate output capacitance (C_{OUT}) in F starts by calculating the right-half plane zero f_{RHPZ}.

$$f_{RHPZ} = \frac{\left|V_{OUT}\right| \times (1 - D_{MAX\_OP})^2}{2 \times \pi \times L \times D_{MAX\_OP} \times I_{OUT}}$$

where I_{OUT} is the load current which is ≤ $I_{OUT(MAX)}$.

For a given step-load current (I_{STEP}) and required output voltage deviation during the step load (ΔV_{OUT}) and target loop crossover frequency (f_C), the required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

where $t_{RESPONSE}$, is the response time of the controller. $t_{RESPONSE}$ can be approximated by the following equation:

$$t_{RESPONSE} \cong \frac{0.35}{f_C}$$

Select the target crossover frequency (f_C) to be the lower of f_{RHPZ} / 4 or f_{SW} / 14 and 50kHz. Actual derating of ceramic capacitors with DC-voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor vendors.

The output capacitor RMS current requirement (I_{RMS}) is defined by the following equation.

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{D_{MAX\_OP}}{1 - D_{MAX\_OP}}}$$

Choose an output capacitor that exhibits less than +10°C temperature rise at the maximum RMS output current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the output.

Soft-Start Capacitor Selection

The MAX17577 and MAX17578 implement adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to the SOUT pin programs the soft-start time. The selected output capacitance (C_{OUT_SEL}) in F and the output voltage (V_{OUT}) determine the minimum required soft-start capacitance in F as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{OUT\_SEL} \times |V_{OUT}|$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to the SOUT pin. Note that during startup, the device operates at half the programmed switching frequency until the feedback (FB) voltage reaches $V_{FB\text{-}HICF}$ (0.58V).

Adjusting Output Voltage

Set the output voltage using a resistive voltage-divider connected from the GND node to the output-voltage node (V_{OUT}) as shown in Figure 2. Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values.

Calculate the resistor R_{FB_TOP} from the GND node to the FB pin as follows:

$$R_{FB\_TOP} = \frac{111 \times \left(1 - D_{MAX\_OP}\right)}{\left(f_C \times C_{OUT\_SEL}\right)}$$

where:

R_{FB_TOP} is in kΩ

f_C = Crossover frequency in Hz

C_{OUT_SEL} = Actual capacitance of output capacitor at DC-bias voltage in F.

The minimum allowable value of R_{FB_TOP} is (5.6 x $|V_{OUT}|$), where R_{FB_TOP} is in kΩ. If the value of R_{FB_TOP} calculated using the above equation is less than (5.6 x $|V_{OUT}|$), increase the value of R_{FB_TOP} to at least (5.6 x $|V_{OUT}|$).

Calculate the resistor R_{FB_BOT} from the FB pin to the V_{OUT} node as follows:

$$R_{FB\_BOT} = \frac{R_{FB\_TOP} \times 0.9}{\left(|V_{OUT}| - 0.9\right)}$$

where R_{FB_BOT} is in kΩ.

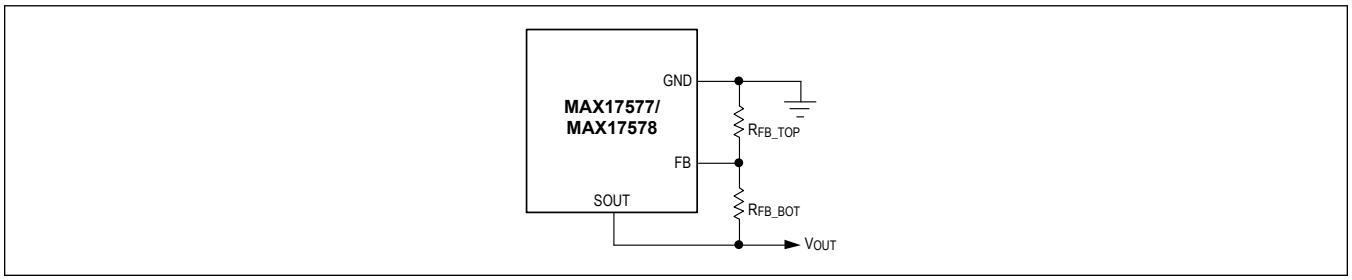


Figure 2. Setting the Output Voltage

Setting the Input Undervoltage-Lockout Level

The MAX17577 and MAX17578 offer an adjustable input undervoltage-lockout level. Set the voltage above which the device turns on with a resistive voltage-divider connected from IN to GND as shown in Figure 3. Connect the center node of the divider to the EN/UVLO pin. Choose R_{UVL_TOP} to be 3.32MΩ and then calculate R_{UVL_BOT} as follows:

$$R_{UVL\_BOT} = \frac{R_{UVL\_TOP} \times 1.229}{\left(V_{INU} - 1.229\right)}$$

where V_{INU} is the input-voltage level at which the device is required to turn on. Choose a minimum of 4.45V for V_{INU}. If the EN/UVLO pin is driven from an external signal source, a series resistance of 1kΩ (min) is recommended to be placed between the output pin of the signal source and the EN/UVLO pin to reduce voltage ringing on the line.

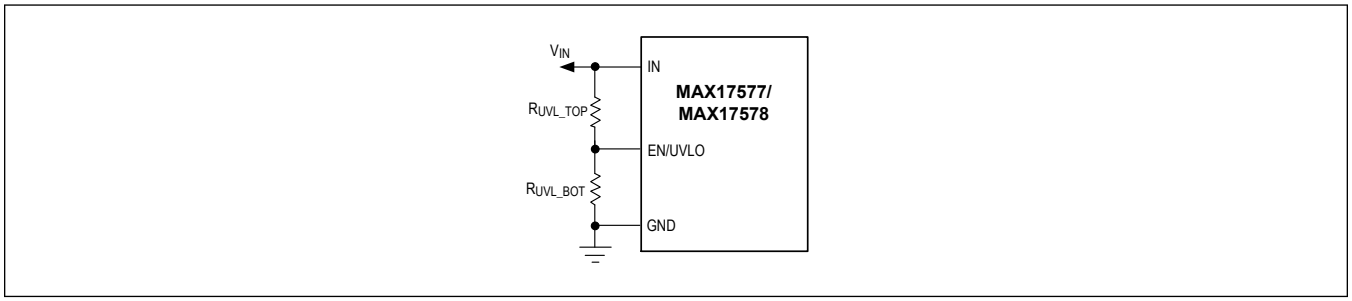


Figure 3. Setting the Input Undervoltage-Lockout

Inductive Output Short-Circuit Protection

In applications where an inductive short-circuit at the output terminals is expected, it is recommended to use a resistor (R_{GND}) and a Schottky diode (D_{GND}) as shown in Figure 4. In a typical application, the high inductance (L_{SH}) and low resistance (R_{SH}) in the short-circuit path can cause the V_{OUT} to swing positive above the system ground. This could forward bias the internal protection diode (D_{INT}) and likely damage the device. To prevent the damage, connect R_{GND} = 50Ω between the GND pin and the system ground, and D_{GND} across SOUT and GND pins. It is recommended to keep the parasitic board or wiring inductance to a minimum value.

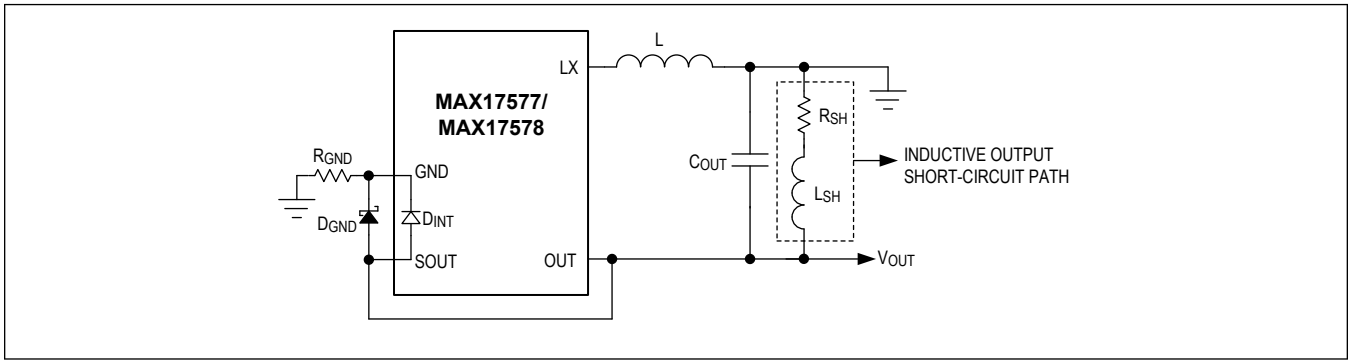


Figure 4. Inductive Output Short-Circuit Protection

Power Dissipation

At a given operating condition, the power losses that lead to a temperature rise of the part are estimated as follows:

$$P_{LOSS} = \left(P_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right) - \left(\frac{I_{OUT}}{1 - D}\right)^2 \times R_{DCR}$$

$$P_{OUT} = |V_{OUT}| \times I_{OUT}$$

where:

P_{OUT} = Output power

η = Efficiency of the converter

D = Operating duty cycle

R_{DCR} = DC resistance of the inductor

See the *Typical Operating Characteristics* section for more information on efficiency at typical operating conditions.

The junction temperature of the device can be estimated at any given maximum ambient temperature (T_A) from the following equation:

$$T_J = T_A + (\theta_{JA} \times P_{LOSS})$$

PCB Layout Guidelines

Use the following guidelines for a good PCB layout:

- Place the input capacitor as close as possible to the IN pin.
- Place the output capacitor as close as possible to the OUT pin.
- Minimize the length and area of the trace connection from the LX pin to the inductor.
- Place the GND terminals of the input capacitor, output capacitor, and the inductor as close as possible and connect them to the GND plane.
- Place the BST capacitor close to the BST and LX pins.
- Connect the V_{CC} bypass capacitor close to the V_{CC} pin and connect the other terminal to the SOUT plane.
- Place the RT/SYNC resistor and feedback resistor divider as close as possible to their respective pins. Connect their other terminals to the SOUT plane.
- Keep all the power connections and load connections short.
- Connect the SOUT and OUT nodes at a point where the switching activity is at its minimum.

Refer to the MAX17577/MAX17578 EV kit data sheet for recommended PCB layout and routing.

Typical Application Circuits

-5V Typical Application Circuits

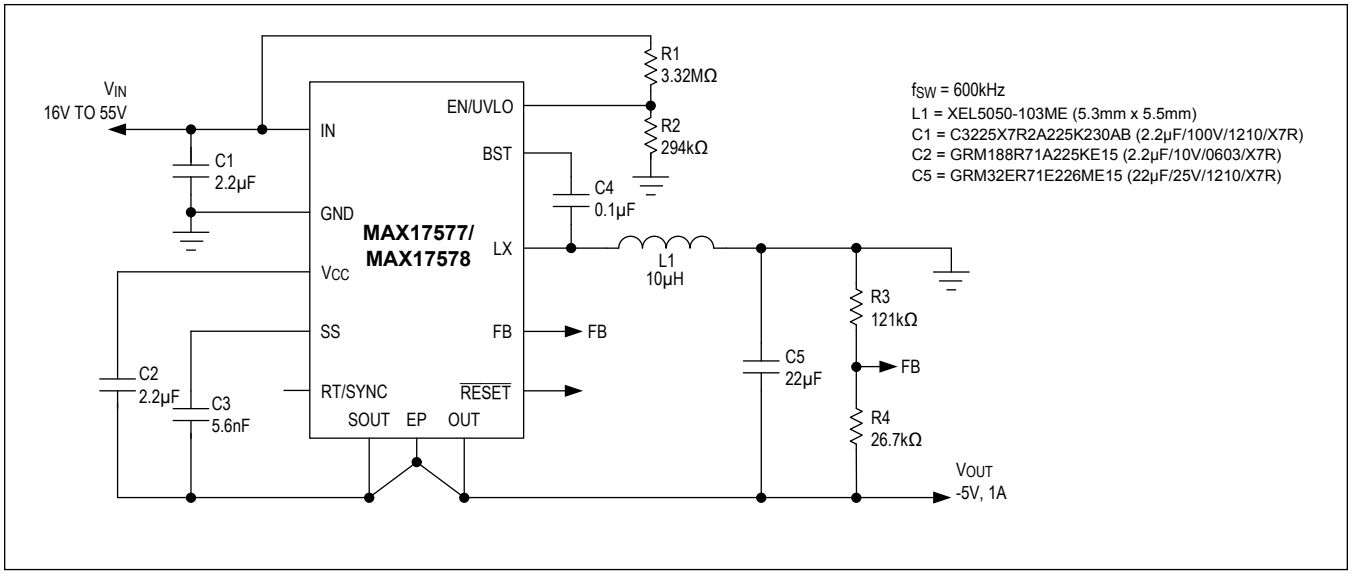


Figure 5. MAX17577 and MAX17578 -5V Output Application Circuit Compatible with 24V Input Bus Voltage

Typical Application Circuits (continued)

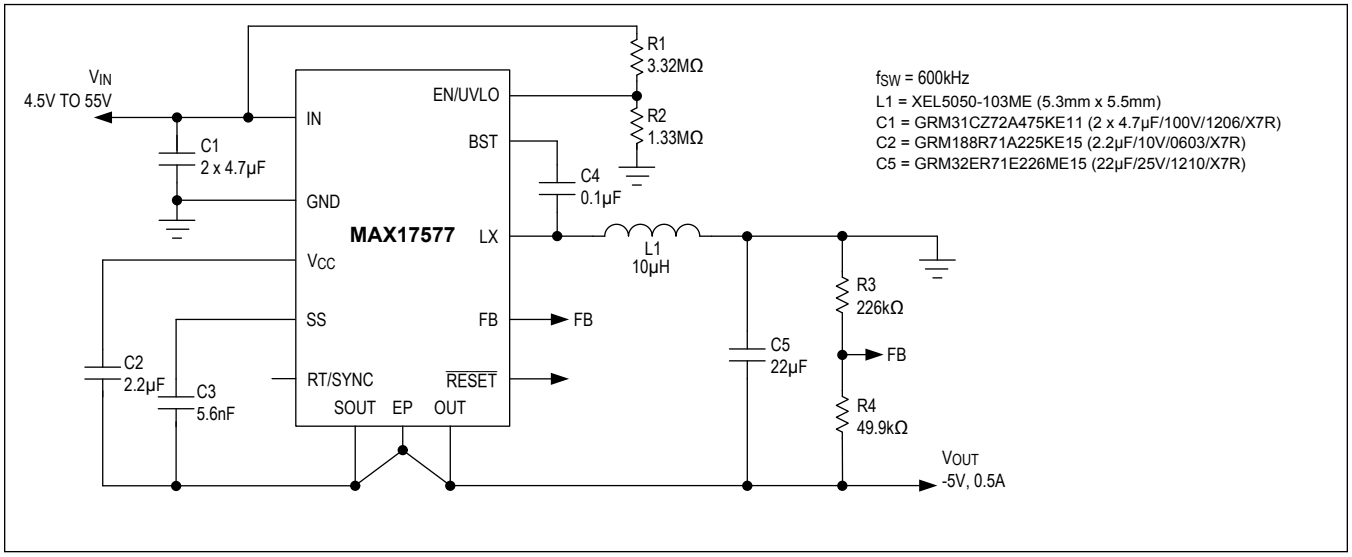


Figure 6. MAX17577 -5V Output Application Circuit Compatible with 5V Input Bus Voltage

-12V Typical Application Circuit

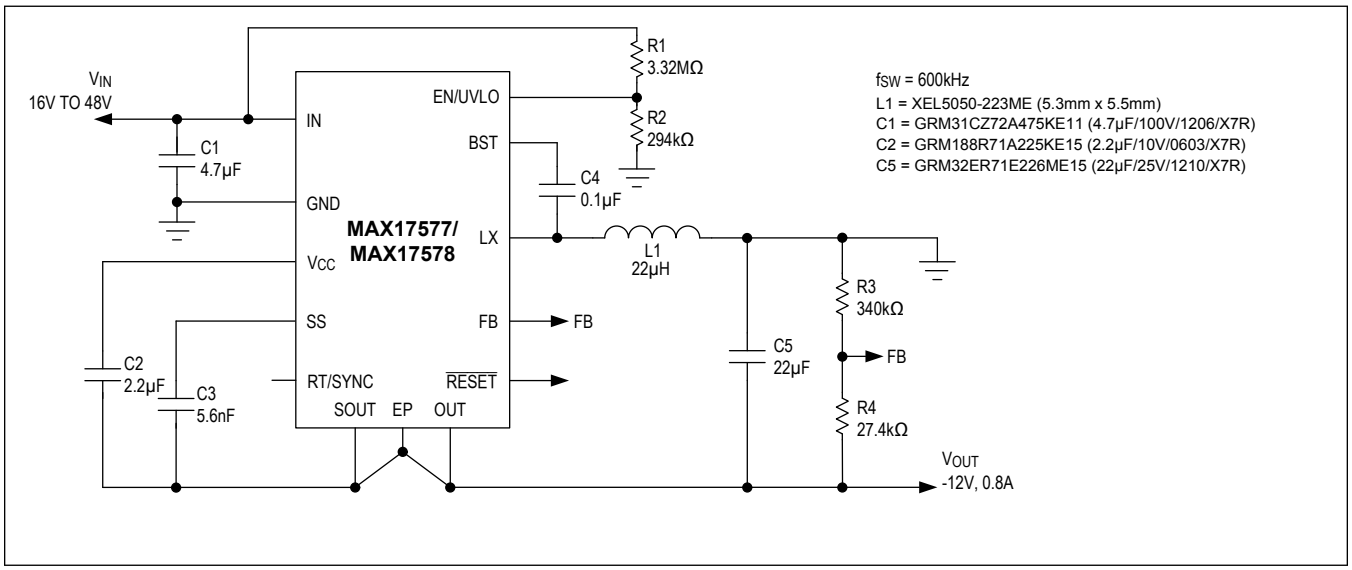


Figure 7. MAX17577 and MAX17578 -12V Output Application Circuit Compatible with 24V Input Bus Voltage

Typical Application Circuits (continued)

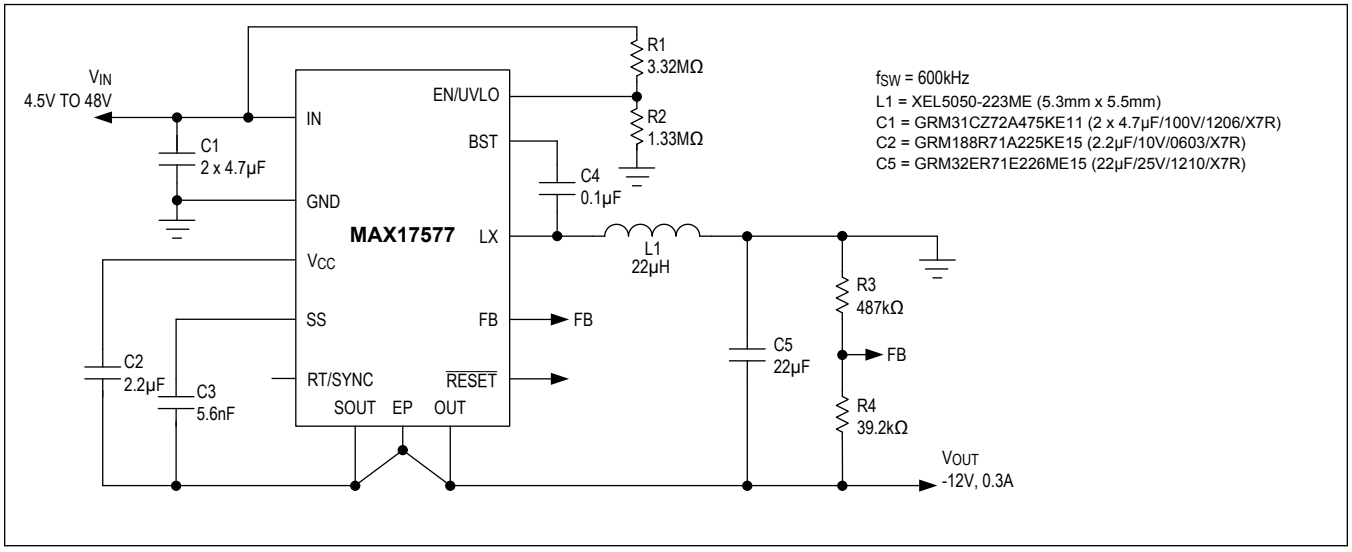


Figure 8. MAX17577 -12V Output Application Circuit Compatible with 5V Input Bus Voltage

Ordering Information

PART NUMBER	MODE OF OPERATION	PIN-PACKAGE
MAX17577ATC+	CCM	12 TDFN 3mm x 3mm
MAX17577ATC+T	CCM	12 TDFN 3mm x 3mm
MAX17578ATC+	DCM	12 TDFN 3mm x 3mm
MAX17578ATC+T	DCM	12 TDFN 3mm x 3mm

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/20	Release for Market Intro	—