Datasheet

DS000571

CSG14K_CSG8K

13.8Mp_8.3Mp High Speed Global Shutter CMOS Image Sensor

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Content Guide

1 General Description

The CSG14K_CSG8K is a high speed CMOS image sensor family developed for machine vision and video applications. The image array consists of 3.2 µm pipelined global shutter pixels, which allow exposure during read out, while performing true CDS (Correlated Double Sampling) operation. The image sensor has 16 sub-LVDS data output channels. Each output channel runs at up to 1.25 Gbit/s, resulting in a frame rate of 140 fps (CSG14K) or 231 fps (CSG8K) in full resolution. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read out timings are generated by a programmable on-chip sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by a dual exposure HDR (High Dynamic Range) mode. The image sensor also integrates black level clamping.

1.1 Key Benefits & Features

The benefits and features of CSG14K_CSG8K, 13.8Mp_8.3Mp High Speed Global Shutter CMOS Image Sensor, are listed below:

Figure 1:
Added Value of Using CSG14K_CSG8K

Benefits	Features
High performance applications	13.8 Mp resolution at 140/93.6 fps (CSG14K, 10/12-bit)
	8.3 Mp resolution at 231/154 fps (CSG8K, 10/12-bit)
Capture fast moving objects	Global shutter pixel with true Correlated Double Sampling (true-CDS)
Use in low light conditions	Low noise and high sensitivity with on-chip noise reduction.
Small camera size	1” optical format in a 20 mm × 22 mm LGA package (CSG14K)
	3/4” optical format in a 20 mm × 22 mm LGA package (CSG8K)
Operation modes tailored to application needs	Programmable sensor timing & readout configuration

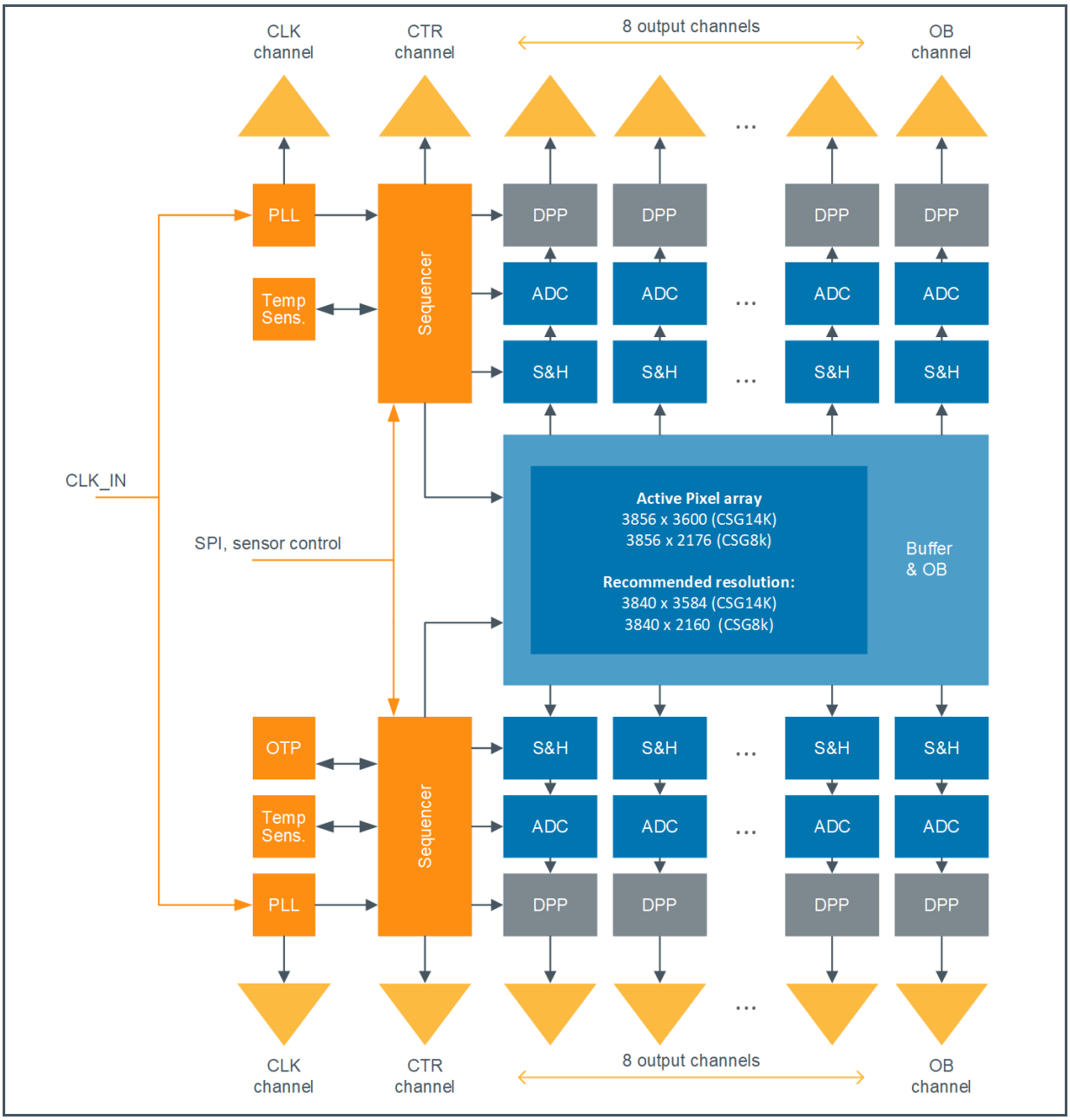
1.2 Applications

- Machine Vision
- High-End Inspection
- Video / Broadcast
- Security

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2 :
Functional Blocks of CSG14K_CSG8K



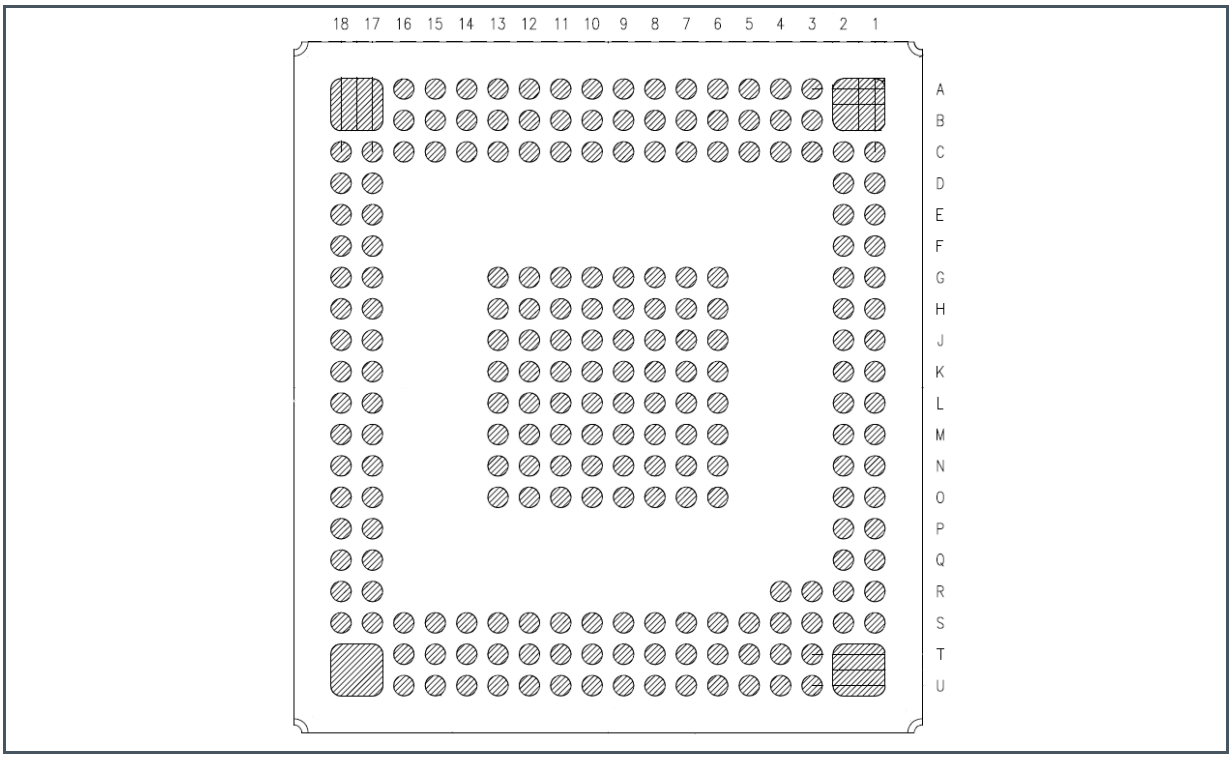
2 Ordering Information

Marking	Mono/Color	Glass Type	Package	Delivery Form	Delivery Qty
CSG14K-1E5MLA	Mono	AR coated	LGA	Tray	40 pcs/tray
CSG8K-1E5MLA	Mono	AR coated	LGA	Tray	40 pcs/tray

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
Pin Diagram



The center 8×8 pads have no functional use (internally not connected (NC)) and should be used for improved thermal conductance from the sensor to the camera.

The four large corner pads are internally NC and needed for solderability.

3.2 Pin Description

Figure 4:
Pin Description of CSG14K_CSG8K

Pin Number	Pin Name	Pin Type[1]	Description
C7, M2, S2, S7	VDD33	S	Analog supply

Pin Number	Pin Name	Pin Type[1]	Description
K1, K17, K18, K2, L1, L17, L18, L2, N17, O17	VSS33	G	Analog ground
C1, C2, S1	VDD33D	S	IO supply
J1, J2, M1	VDDPIX	S	Pixel supply
A7, B14, B4, C11, C12, S11, S12, T14, T4, U7	VDD12	S	Digital supply
A12, B3, B9, C16, C6, S16, S6, T3, T9, U12	VSS12	G	Digital ground
C14, C8, C9, S10, S14, S8, S9	VDD12C	S	ADC supply
C13, F1, F2, N1, N2, S13, S5	VSS12C	G	ADC ground
C10, P1	VDD12_PLL	S	PLL supply
C5, P2	VSS12_PLL	G	PLL ground
S15	-	G	Connect to VSS33
C15	VDD45	S	Regulator supply
S17	VSSNEG	S	Negative regulator supply
J18	VPIX1_H_IN	S	Analog supply
E18	VPIX1_L_IN	S	Analog supply
H18	VPIX2_H_IN	S	Analog supply
D18	VPIX2_L_IN	S	Analog supply
F18	VPIX3_H_IN	S	Analog supply
M17	VPIX3_L_IN	S	Analog supply
G18	VPIX4_H_IN	S	Analog supply
C18	VPIX4_L_IN	S	Analog supply
E1	SPI_CSN	DI	SPI chip select
E2	SPI_MISO	DO	SPI master in/slave out data
D2	SPI_MOSI	DI	SPI master out/slave in data
D1	SPI_CLK	DI	SPI clock
G2	REQ_FRAME	DI	Request frame (stop exposure)
G1	REQ_EXP	DI	Request exposure (start exposure)
H1	RST_N	DI	Asynchronous hard reset
H2	CLK_IN	DI	Sensor input clock
O1	JTAG_MODE	DI	JTAG Mode select. Connect to VSS33 if JTAG is not used.
O2	SCAN_MODE	DI	Reserved for test. Connect to VSS33.
Q2, Q1, R1, R2	TDIG1..4	DO	Digital test monitor
U4, U3 U6, U5 T8, T7 U9, U8 U11, U10 T11, T10 U14, U13 T13, T12	DOUT<i>_B_N/P	HSO	Output data channel (i=1..8) at bottom

Pin Number	Pin Name	Pin Type(1)	Description
A4, A3 A6, A5 B8, B7 A9, A8 A11, A10 B11, B10 A14, A13 B13, B12	DOUT<i>_T_N/P	HSO	Output data channel (i=1..8) at top
U16, U15	DOUT_OB_B_N/P	HSO	Optical black data channel at bottom
A16, A15	DOUT_OB_T_N/P	HSO	Optical black data channel at top
T6, T5	DOUT_CTR_B_N/P	HSO	Control channel at bottom
B6, B5	DOUT_CTR_T_N/P	HSO	Control channel at top
T16, T15	DOUT_CLK_B_N/P	HSO	Clock channel at bottom
B16, B15	DOUT_CLK_T_N/P	HSO	Clock channel at top
S4, S3	-	G	connect to VSS33
C4, C3	-	G	connect to VSS33
P17, Q17, R17	-	G	connect to VSS33
O18, P18, Q18, M18, N18	REFA0..4	A	Analog reference
R18	VBGAP	A	Analog reference
S18	BIAS_IDAC_RES	A	Analog reference, connect to bias resistor
E17	VPIX1_L_OUT	A	Analog reference
J17	VPIX1_H_OUT	A	Analog reference
D17	VPIX2_L_OUT	A	Analog reference
H17	VPIX2_H_OUT	A	Analog reference
C17	VPIX4_L_OUT	A	Analog reference
G17	VPIX4_H_OUT	A	Analog reference
F17	VPIX3_H_OUT	A	Analog reference
R3, R4	-	NC	Do not connect

(1) Explanation of abbreviations:

DI	Digital Input
DO	Digital Output
HSO	High Speed Output
A	Analog reference
G	Ground
S	Supply
NC	Not Connected

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5
Absolute Maximum Ratings of CSG14K_CSG8K

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
VDD12	Logic Supply Voltage of digital core	- 0.3	1.7	V	
VDD12_PLL	Logic Supply Voltage of PLL analog	- 0.3	1.7	V	
VDD12C	Logic Supply Voltage of ADC	- 0.3	1.7	V	
VDD33D	I/O Supply Voltage for CMOS I/O’s	- 0.3	3.6	V	
VDD33	Main Analog Supply Voltage	- 0.3	3.6	V	
VDDPIX	Pixel Array Supply Voltage	- 0.3	3.6	V	
VDD45	Positive Regulators	- 0.3	4.7	V	
VSSNEG	Negative Regulators	- 1.5	0.3	V	
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JEDEC JESD78D Nov 2011
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 2		kV	JS-001-2014
ESD_{CDM}	Electrostatic Discharge CDM	± 250		V	JEDEC JESD22-C101F Oct 2013
Temperature Ranges and Storage Conditions					
T_J	Operating Junction Temperature	-30	85	°C	
T_{STRG}	Storage Temperature Range	-30	40	°C	
RH_{NC}	Relative Humidity (non-condensing)	30	60	%	Storage condition
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h
Bump Temperature (soldering)					
T_{PEAK}	Peak Temperature	245		°C	Solder Profile in chapter 10

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics of CSG14K_CSG8K

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supplies						
VDD12	Logic supply voltage of digital core		1.25	1.28	1.32	V
VDD12_PLL	Logic supply voltage of PLL analog		1.25	1.28	1.32	V
VDD12C	Logic supply voltage of ADC		1.25	1.28	1.32	V
VDD33D	I/O supply voltage for CMOS I/O's		3.25	3.30	3.35	V
VDD33	Main analog supply voltage		3.25	3.30	3.35	V
VDDPIX	Pixel array supply voltage		3.25	3.30	3.35	V
VDD45	Positive regulators		4.4	4.5	4.6	V
VSSNEG	Negative regulators		-1.4	-1.3	-1.2	V
IDD12	Supply current(1)	Idle Running		306 321		mA
IDD12_PLL	Supply current(1)	Idle Running		13 13		mA
IDD12C	Supply current(1)	Idle Running		105 151		mA
IDD33D	Supply current(1)	Idle Running		116 116		mA
IDD33	Supply current(1)	Idle Running		246 251		mA
IDDPIX	Supply current(1)	Idle Running		106 106		mA
IDD45	Supply current(1)	Idle Running		25 25		mA
ISSNEG	Supply current(1)	Idle Running		125 126		mA
Ptot	Total power consumption(1)	Idle Running		2.0		W
Tpu1	Settling time after VDD45 power-up		100	-	-	µs
Tpd1	Settling time after VSSNEG power-down		100	-	-	µs
Digital I/O						
V_{IH}	High level input voltage		0.7*VDD33		VDD33	V
V_{IL}	Low level input voltage		0		0.3*VDD33	V
V_{OH}	High level output voltage	I_{OH}=12 mA	VDD33-0.6			V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Low level output voltage	I_{OL}=12 mA			0.4	V
C_I	Input load				3	pF
C_O	Output load				20	pF
f_{CLK_IN}	CLK_IN frequency		12		20	MHz
DC_{CLK_IN}	CLK_IN duty cycle		30	50	70	%
f_{SPI_CLK}	SPI input clock frequency				15	MHz
t_{setup}	SPI setup time		10			ns
t_{hold}	SPI hold time				0	ns
t_{REQ}	REQ_FRAME/EXP pulse width		2 × t_{CLK_PIX}		-	ns
Sub-LVDS Interface						
DR_{HS}	Output data rate		0.25	1.25	1.25	Gbit/s
V_{FCM}	Fixed common mode voltage		0.8	0.9	1	V
V_{OD}	Differential voltage swing		100	150	200	mV
R_O	Output impedance		40	100	140	Ohm
D_{R0}	Impedance mismatch				10	%
I_{OD}	Drive current		0.83		2	mA
ΔIOD	IOD variation				15	%
t_R	V_{OD} rise time (20 %-80 %)		300		400	ps
t_F	V_{OD} fall time (80 %-20 %)		300		400	ps

(1) Current and Power numbers measured in IMG.4 mode (12b default)

6 Typical Operating Characteristics

6.1 Electro-Optical Characteristics

Below are the typical electro-optical specifications of CSG14K_CSG8K, when operated in the 12-bit default mode. These are typical values with typical supplies at room temperature.

Figure 7:
Electro-Optical Characteristics

Parameter	Value	Remark
Active pixels	3856 (H) × 3600 (V)	CSG14K
	3856 (H) × 2176 (V)	CSG8K
Pixel pitch	3.2 × 3.2 µm^2	
Optical format	1”	
Pixel type	Global shutter with true CDS	Allows fixed pattern noise correction and reset (kTC) noise canceling by true correlated double sampling (true-CDS).
Shutter type	Pipelined global shutter	Exposure of next image during readout of the previous image.
Full well charge$_{sat}$	10500 e$^-$	Normal mode, 8 lux conditions
Conversion gain	0.386 DN/e$^-$	Normal mode, unity gain
Responsivity	0.254 DN/photon 0.276 A/W	@510 nm (with micro-lenses)
Temporal noise	3.7 e$^-$	Normal mode
Dynamic range	69.1 dB	Normal mode
SNR$_{MAX}$	40.0 dB	Normal mode
Shutter efficiency 1/PLS	1/11130	At 520 nm, f/8.
Dark current (DC)	32.9 e$^-$/s	@ 60 °C sensor junction temperature
DC doubling	6.59 °C	The DC doubles every 6.59 °C increase
DCNU	16.2 e-/s	Dark current non uniformity @60 °C sensor temperature
DSNU$_{1288}$	1.9 e$^-$	Dark signal non uniformity
PRNU$_{1288}$	0.89 %	Photo response non-uniformity RMS of signal
Quantum efficiency	64 / 66 / 51 / 10 %	@ 450 / 510 / 600 / 850 nm (mono) Quantum Efficiency (with micro-lenses)
Data interface standard	Sub-LVDS	Similar to CMV sensor family
Sub-LVDS outputs	16 Data 1 Control 1 Clock 2 OB	Less outputs selectable at reduced frame rate

Parameter	Value	Remark
Output interface bit rate	1.25 Gbit/s	Per data channel (maximum)
Frame rate (1)	140 fps	CSG14K, 10-bit
	93 fps	CSG14K, 12-bit
	231 fps	CSG8K, 10-bit
	154 fps	CSG8K, 12-bit
Timing generation	On-chip	Possibility to control exposure time through external pin.
Programmable registers	Sensor parameters	Window coordinates, timing parameters, exposure time, offset …
HDR mode	Interleaved	2 exposure times for odd/even rows
ADC	10-bit 12-bit	Column ADC
Cover glass	D263Teco	
RoHS/REACH		
MSL	3	Represents a maximum floor life time of 168 hours
Mass	3.223 g	

(1) Higher frame rate possible in row windowing mode or when operating in 10-bit mode. Based on recommended pixel area.

The following table details the expected typical performance in the various readout configuration modes.

Figure 8:
Typical Performance Values for the Various Readout Configurations

Parameter	10 b Default (IMG.1)	10 b Short Exp. Mode (IMG.2)	10 b Small Window Mode (IMG.3)	12 b Default (IMG.4)	12 b Short Exp. Mode (IMG.5)	12 b Binning Mode (IMG.7)
ADC resolution	10 b			12 b		
Output image resolution (recommended pixels) for CSG14K	3840 (h) 3584 (v)		3840 (h) 400 (v)	3840 (h) 3584 (v)		1920 (h) 1792 (v)
Output image resolution (recommended pixels) for CSG8K	3840 (h) 2160 (v)		3840 (h) 400 (v)	3840 (h) 2160 (v)		1920 (h) 1080 (v)
Full well charge	10000 e-		9800 e-	10500 e-		40600 e-
Conversion gain	0.10 DN/e-			0.38 DN/e-		0.10 DN/e-
Temp. noise	5.6 e-			3.7 e-		12.4 e-
Dynamic range	65.1 dB	65.1 dB	64.9 dB	69.1 dB	69.1 dB	70.3 dB
SNRmax	39.8 dB	39.8 dB	39.7 dB	40.0 dB	40.0 dB	45.9 dB
DSNU (1288)	1.9 e-	1.8 e-	20.7 e-	1.9 e-	1.7 e-	3.4 e-
Maximum FR at recommended resolution (CSG14K)	140 fps	140 fps	NA	93 fps	93 fps	129.7 fps
Maximum FR at recommended resolution (CSG8K)	231 fps	228 fps	NA	153 fps	153 fps	214 fps
Maximum FR (100 lines ROI, 100 µs exposure time)	3829 fps	3017 fps	4793 fps	2625 fps	2255 fps	3361 fps
Minimum exposure time ($t_{exp,min}$)	36.7 µs	7.9 µs	11.2 µs	46.2 µs	10.0 µs	36.9 µs
Maximum exposure time ($t_{exp,max}$)	NA	100 µs	NA	NA	100 µs	NA
I/F DR (at maximum FR)	1250 Mbit/s	1250 Mbit/s	1250 Mbit/s	1000 Mbit/s	1000 Mbit/s	1000 Mbit/s
Power consumption	2.02 W	2.23 W	2.19 W	1.93 W	2.13 W	1.86 W

6.2 Spectral Characteristics

Figure 9:
Quantum Efficiency Mono

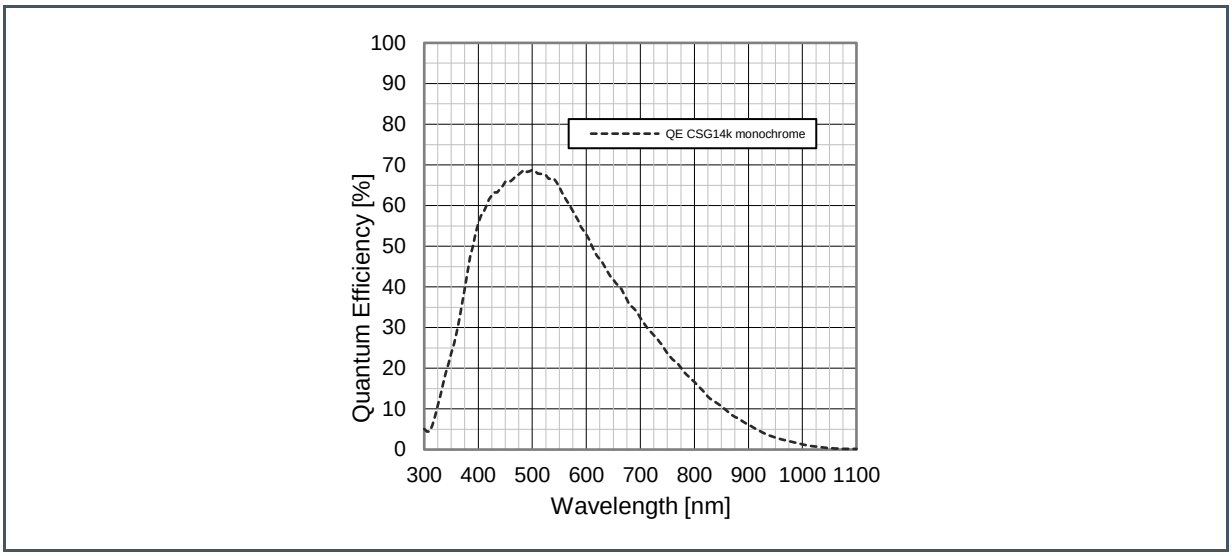
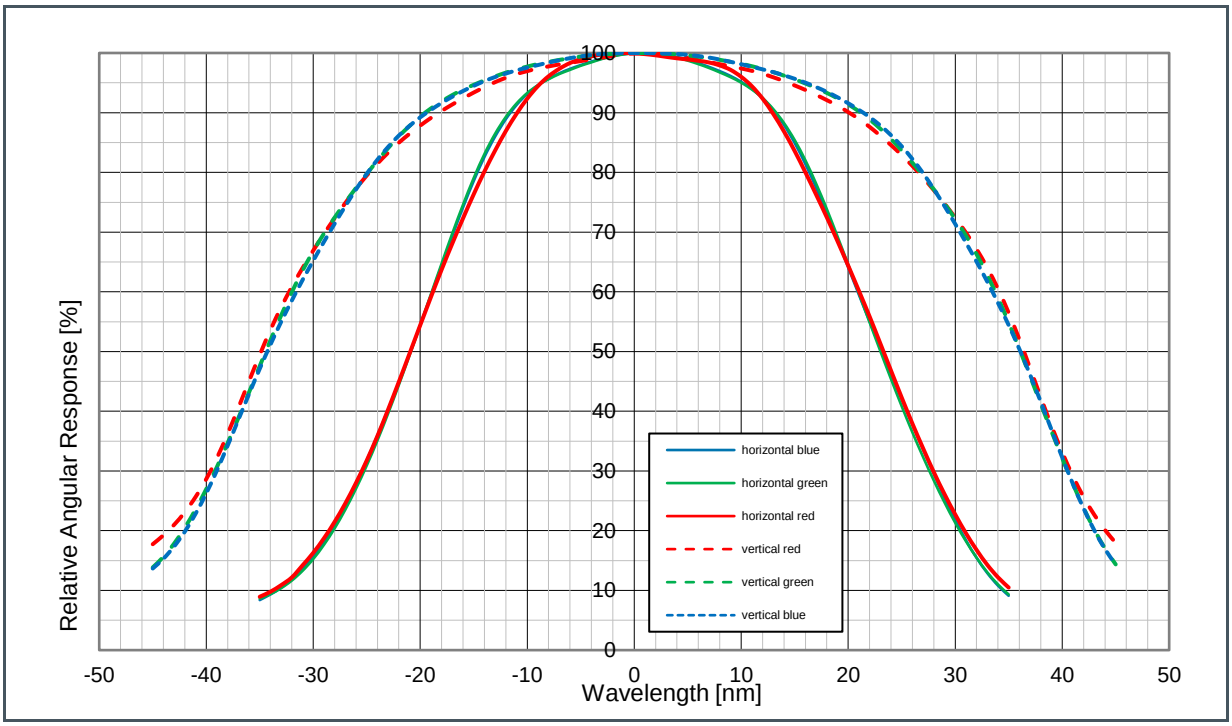


Figure 10:
Angular Response Color



7 Functional Description

7.1 Sensor Architecture

Figure 2 shows a high-level representation of the chip architecture for the CSG14K_CSG8K sensor. The drawing shows the pixel array and the periphery around it that enables the control and readout of the pixels.

The core of the image sensor is made up from the pixel array, which is driven from two sides through row logic and drivers. The pixel data is read out, row by row, using a data path consisting of an sample and hold stage (S&H), analog-to-digital converter (ADC) and a digital data post-processing (DPP) block. The top part of the pixel array is read out via the top outputs, while the bottom part is read via the bottom outputs.

The converted data is sent, pixel by pixel, to a configurable number of data output channels. An additional control (CTR) channel provides synchronization information about the data on the data channels, while a specific CLK channel can be used to sample the data channels.

An optional output channel allows reading out OB pixel columns on the right side of the pixel array.

The on-chip PLL transforms a low-frequency CMOS input clock into all the high frequency clocks needed to operate the sensor.

An on-chip sequencer controls the sensor operation and contains SPI programmable registers.

Two on-chip temperature sensors and an OTP memory are available.

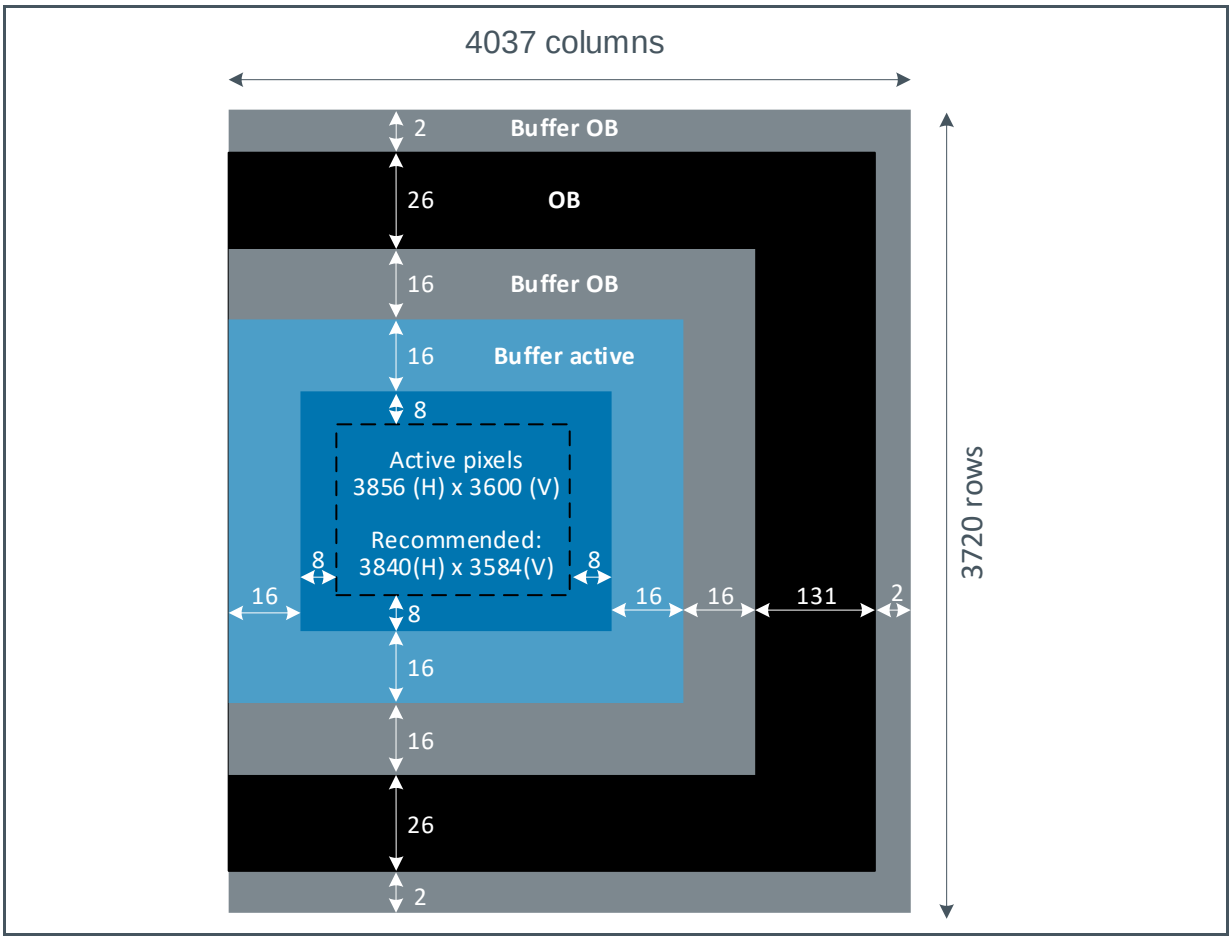
7.1.1 Pixel Array

This section is split-up between CSG14K and CSG8K. The pixel array of the CSG8K is very similar to the pixel array of the CSG14K, except that some rows cannot be read out to limit vertical resolution in CSG8K. Refer to chapter 7.5.3 for more details on which rows can be addressed.

Pixel Array of the CSG14K

Figure 11 shows the complete pixel array.

Figure 11:
CSG14K Pixel Array



The physical resolution of the complete pixel array is 4037 (H) × 3720 (V) pixels.

The pixel array can be split up in three parts: active pixels, optical black pixels (OB), and buffer pixels (around both the active array and OB perimeter). The OB pixels are used for internal row clamping, which improves row noise and allows setting a pre-defined black level. The buffer pixels form a guard ring around the active pixels. The buffer pixels are optically active, but are not guaranteed to meet the optical specifications. The OB and buffer pixel columns can be read out via the OB output channel.

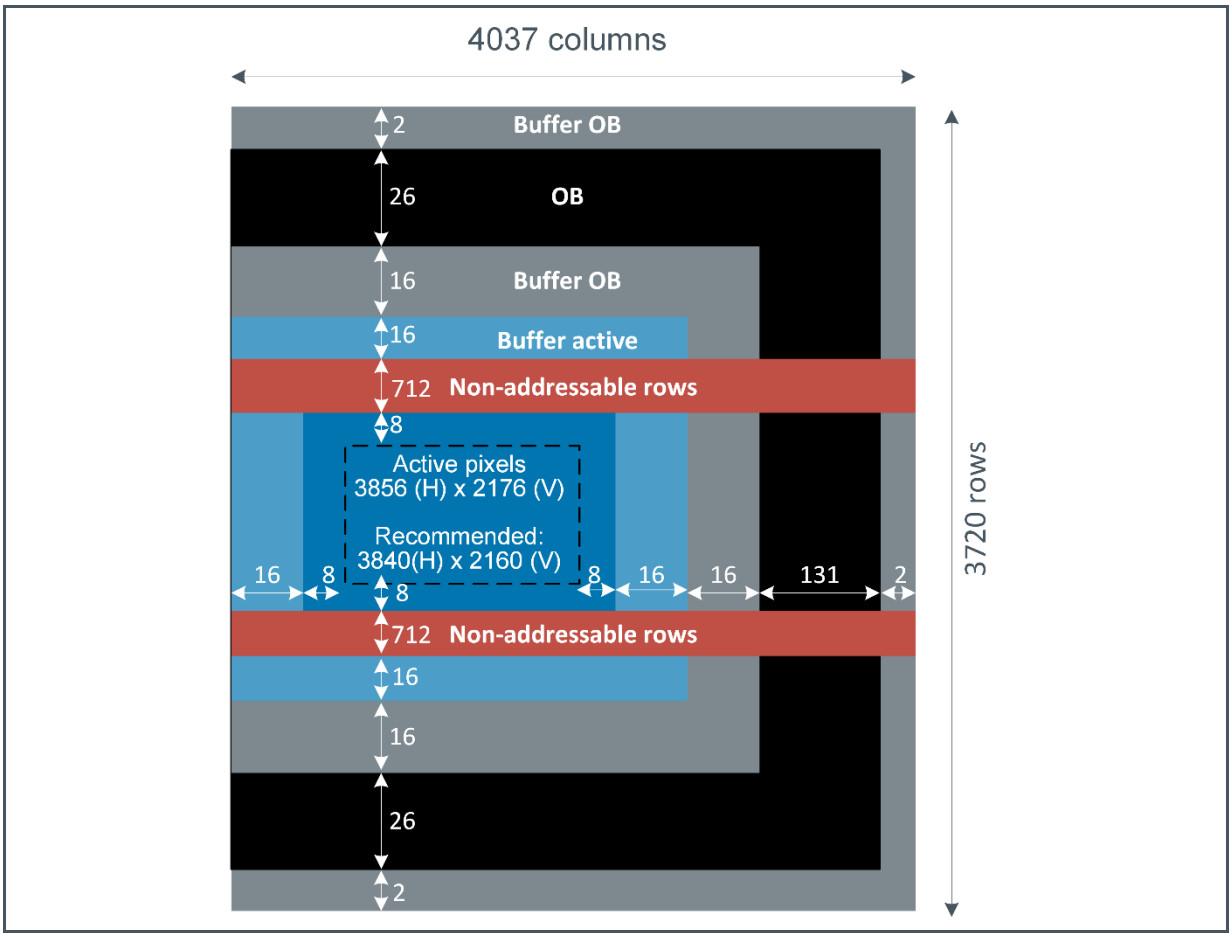
The resolution of the active pixel array is 3856 (H) × 3600 (V) pixels. This is further split into a ring of 8 pixels on every side for color reconstruction and an optically centered recommended pixel array with a resolution of 3840 (H) × 3584 (V) pixels. The recommended array is 12.29 mm × 11.47 mm, which is a 1” optical format.

Micro-lenses are placed on the pixels for improved quantum efficiency and fill factor.

Pixel Array of the CSG8K

Figure 12 shows the complete pixel array.

Figure 12:
CSG8K Pixel Array



The physical resolution of the complete pixel array is 4037 (H) × 3720 (V) pixels.

The resolution of the active pixel array is 3856 (H) × 2176 (V) pixels. This is further split into a ring of 8 pixels on every side for color reconstruction and an optically centered recommended pixel array with a resolution of 3840 (H) × 2160 (V) pixels. The recommended array is 12.29 mm × 6.91 mm, which is a 3/4” optical format.

Micro-lenses are placed on the pixels for improved quantum efficiency and fill factor.

7.1.2 Analog Front End

The analog front end consists of circuitry to prepare the signal for ADC conversion also called the sample & hold stage (S&H).

7.1.3 ADC

The column ADC converts the analog pixel value to a 10/12-bit value.

7.1.4 DPP

The DPP blocks perform digital operations on the visible pixel data: digital offset, digital gain, row noise correction.

7.1.5 Sub-LVDS Outputs

The sensor has 16 data channels to output the processed data. Every channel outputs the data of 480 columns when reading the recommended pixel array. Multiplexing the data on fewer outputs is supported as well.

7.1.6 Sequencer

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control signals. This sequencer can be activated and programmed through the SPI interface.

The sequencer includes the following features:

- SPI protocol and register banks management.
- Exposure and frame timing generation based on external inputs or internal settings.
- Dual exposure HDR mode.
- Y-windowing, Y-subsampling and binning.
- Statistics data gathering.

7.1.7 SPI Interface

The SPI interface is used to load the on-chip registers with settings to configure the image sensor. Features like exposure time, windowing, and subsampling are programmed using this interface. The settings in the on-chip registers can also be read back for test and debug of the surrounding system.

7.1.8 Temperature Sensor

Two on-chip thermal sensors are included (one on the top right side and one on the bottom right side of the pixel array). The temperature data is read out through the SPI interface.

7.1.9 PLL

Various clock frequencies are required internally to operate the sensor. These are derived from a single input frequency using an on-chip PLL. Through configuration over SPI, a range of input clock frequencies is supported.

The main internal clocks are:

- CLK_ADC is the PLL output clock and is used to operate the ADC.
- CLK_SER is the sub-LVDS output clock (625 MHz for 1.25 Gbit/s).
- CLK_PIX is the pixel clock and has a ratio of:
  - 1:5 of CLK_SER in 10-bit ADC mode
  - 1:6 of CLK_SER in 12-bit ADC mode

7.1.10 OTP Memory

A non-volatile, one time programmable memory is included on-chip. This is programmed with unique identifier and temperature sensor calibration data.

7.2 Operating the Sensor

This section explains how to connect and power the sensor, as well as basic recipes of how to configure the sensor in a certain operation mode.

7.2.1 Power Supplies

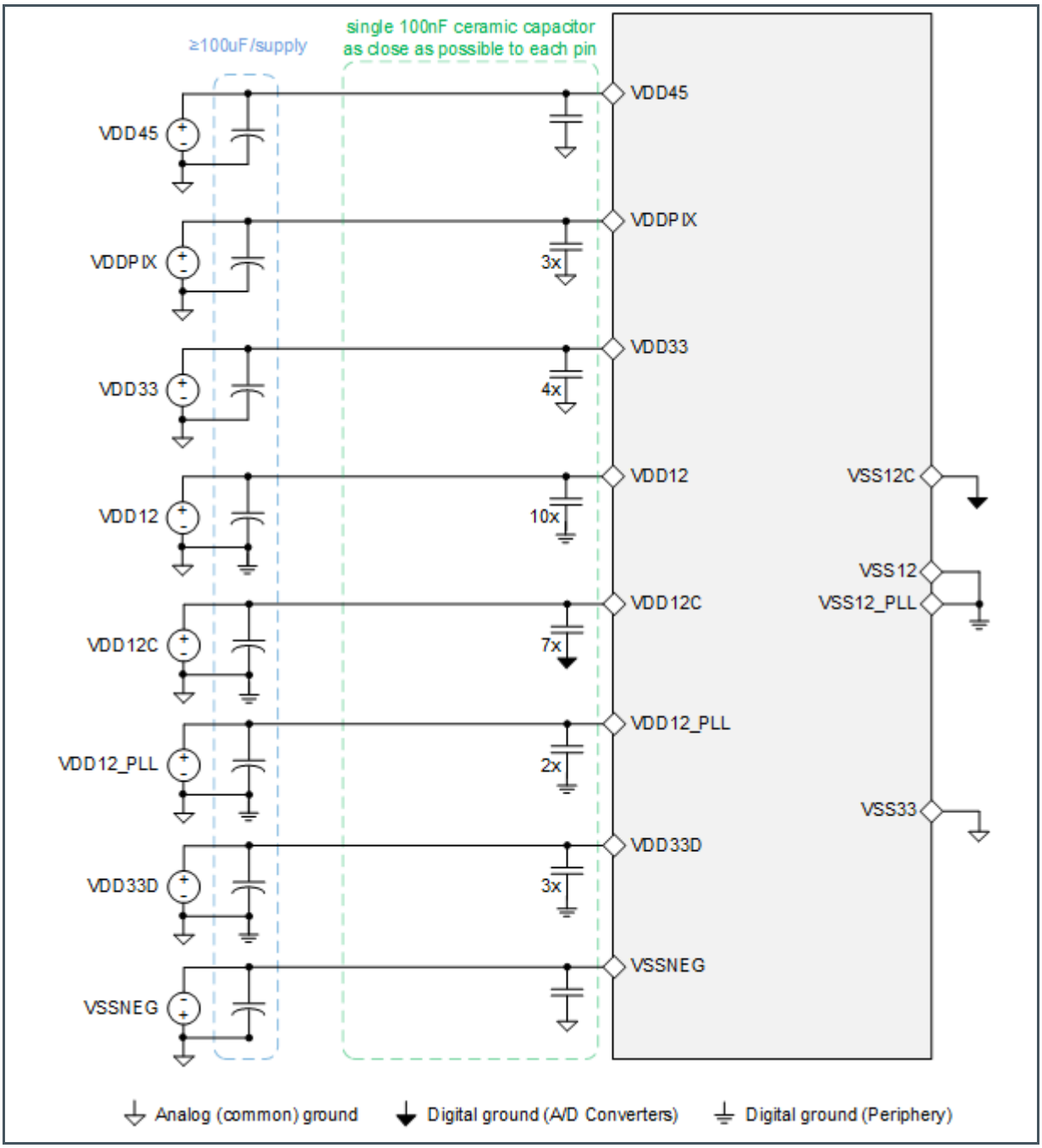
External Power Supplies

To power the sensor, eight externally generated supplies are required as listed in Figure 6. A Figure 6 distinction is made between digital supplies (VDD12, VDD12C, VDD33D, VDD12_PLL) and analog supplies (VDD33, VDDPIX, VDD45, VSSNEG). Avoid using switching power supplies when possible, especially for the analog supplies.

Sufficient bulk (at the regulators) and local (at the sensor pins) decoupling is needed, see Figure 13. In case of multiple pins for the same supply, local decoupling must be foreseen for each pin (e.g. 3 capacitors for the 3 VDDPIX pins). Separate ground planes must be provided to minimize coupling.

For optimal noise performance, it is advised to keep the analog and digital ground nets separated and connect them together as close as possible to the external supply regulators.

Figure 13 :
Power Supply Decoupling and Grounding Diagram



Biasing (on-chip regulators)

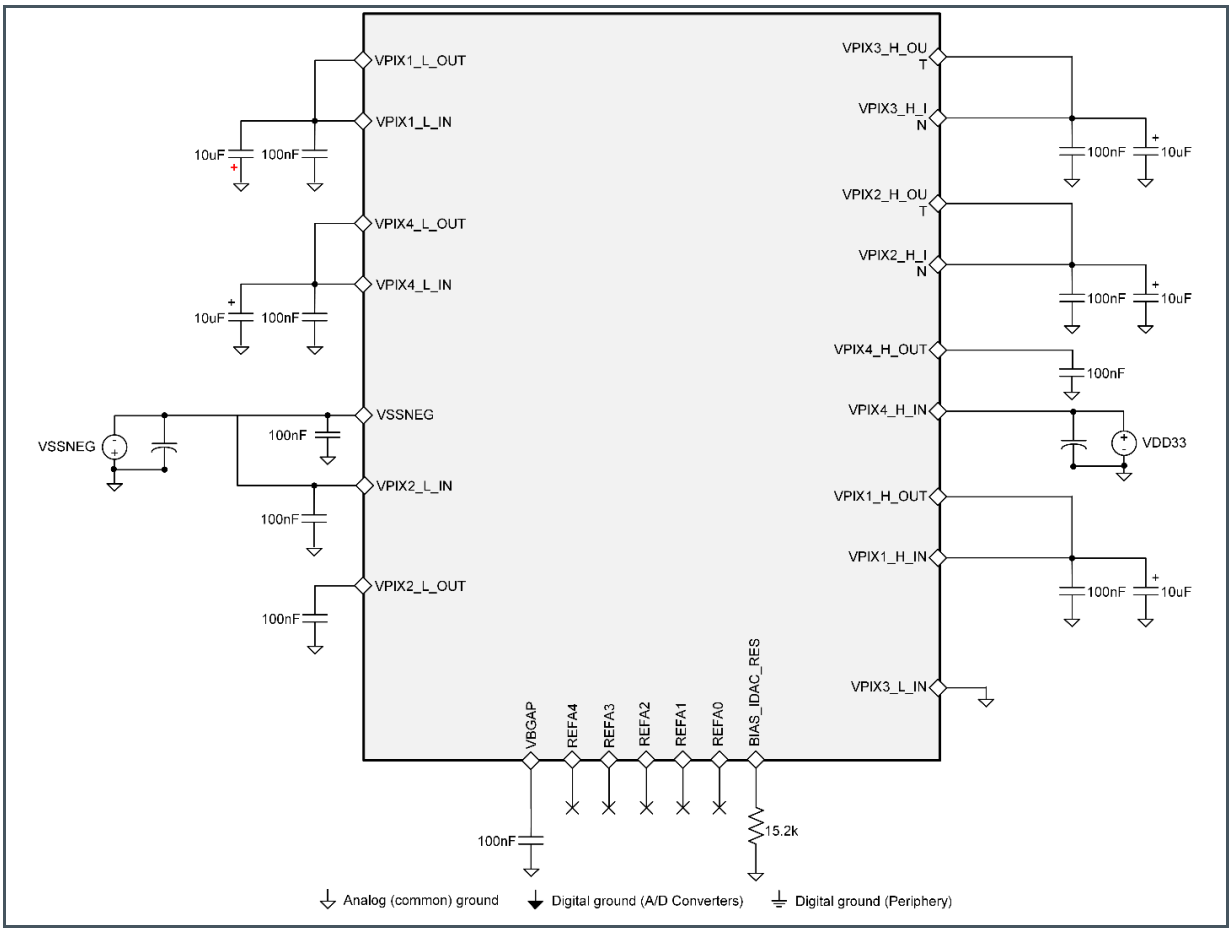
Operating the pixel array requires multiple different biasing supply levels. These supply levels can be generated using on-chip regulators. The chip contains 2 types of regulators, for positive supply levels and negative supply levels. The regulator output voltages are controlled using the SPI interface.

Internally, the supply regulators are not connected to the actual image sensor. Connections have to be made on PCB level (from a Vxx_H/L_OUT pin to a Vxx_H/L_IN pin). In addition, each supply regulator requires to be decoupled by a 10 µF and 100 nF capacitor. **ams** recommends to use at least X7R-rated ceramic capacitors.

To obtain an accurate bias reference in the sensor, an external bias resistor of 15.2 kΩ must be placed between BIAS_IDAC_RES and ground. It is advised to use a low tolerance (± 1%) and low temperature coefficient (50 ppm/°C or better).

Next figure shows the positive and negative voltage regulator as well as the bias connections.

Figure 14:
On-Chip Regulators Connection Diagram



After power-up of the sensor, the recommended register settings will set the correct supply levels for these regulators. Figure 14 gives an overview of the available supply regulators, the connection to the bias pin and the required voltage on that pin.

Figure 15:
Bias Voltages

Regulator Pin	Type	Bias Pin	Voltage [V]
-	Analog ref	VBGAP	1.24
-	Analog ref	BIAS_IDAC_RES	1.24
VPIX1_L_OUT	Pixel control	VPIX1_L_IN	-0.70
VDD33 (ext)	Pixel control	VPIX4_H_IN	3.30
VPIX1_H_OUT	Pixel control	VPIX1_H_IN	4.13
VPIX3_H_OUT	Pixel control	VPIX3_H_IN	3.83
VPIX2_H_OUT	Pixel control	VPIX2_H_IN	3.53
VPIX4_L_OUT	Pixel control	VPIX4_L_IN	0.73
VSSNEG	Pixel control	VPIX2_L_IN	-1.30

7.2.2 Startup Sequence

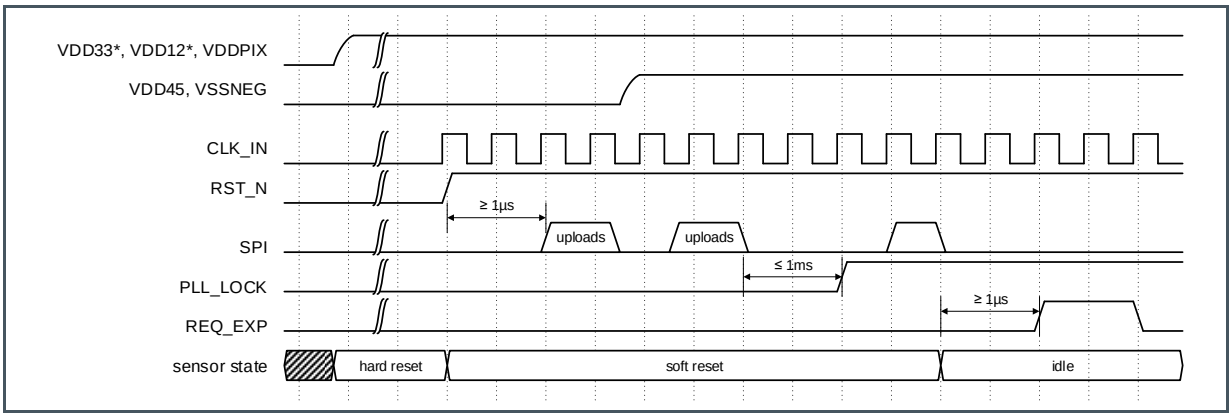
After the supply power-up sequence, the general sequence below (also shown in Figure 16) must be followed to configure and start operating the sensor. Deviating from the order or timing can lead to the sensor being in an unknown or unstable state.

The sensor hard reset pin, RST_N, must be asserted (‘0’) during the supply ramp-up to initialize the sensor in the hard reset state. By releasing RST_N (‘1’), the sensor moves to soft reset state. CLK_IN can be started during either the hard reset or during soft reset state (there is no relation to the releasing of RST_N). During the soft reset state, the recommended SPI uploads must be executed (see section 7.4.3). This includes ramping up VDD45 and VSSNEG, and enabling the PLL, which locks after maximally 1 ms. After the PLL has locked, the sensor can be moved from soft reset state to idle state through a short SPI upload.

In idle state, the sensor waits for an exposure request to begin grabbing, for example with the REQ_EXP pin (depending on the configured sensor control mode).

As indicated in the figure, a non-overlap of 1 µs must be respected between each sensor state change and the next action.

Figure 16:
Power-Up Sequence (not to scale)



7.2.3 Clocking

The sensor has two CMOS clock inputs: SPI_CLK and CLK_IN. SPI_CLK is part of the SPI interface used to configure the sensor. All other internal sensor clocks are derived from the PLL running on CLK_IN.

Refer to section 5 for the electrical specifications of the input clocks and to section 7.4.3 for the configuration procedure of the PLL.

7.2.4 SPI and Register Access

The sensor operation must be configured by uploading register settings. These static register values control the behavior of the sequencer on the chip, but also of all the analog and mixed-signal blocks. To write and read register settings the SPI interface is used.

The SPI (Serial Peripheral Interface) consists of four wires, as shown in Figure 17.

The CSG14K_CSG8K image sensor always operates as the SPI slave. A single SPI access always consists of:

- Transfer of a control bit from master to slave to specify the transfer direction (read or write).
- Transfer of 7-bit register address from master to slave.
- Transfer of 8-bit data from master to slave (write operation) or from slave to master (read operation).

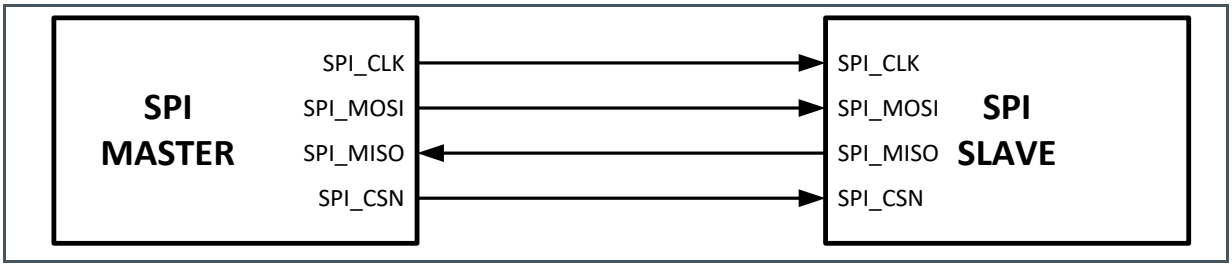
Figure 17:
SPI Signal Overview

Pin Name	Direction	Purpose
SPI_CSN	Sensor Input	Active-low chip select

Pin Name	Direction	Purpose
SPI_CLK	Sensor Input	Rising-edge triggered clock for SPI protocol
SPI_MOSI	Sensor Input	Data moving from master to slave
SPI_MISO	Sensor Output	Data moving from slave to master

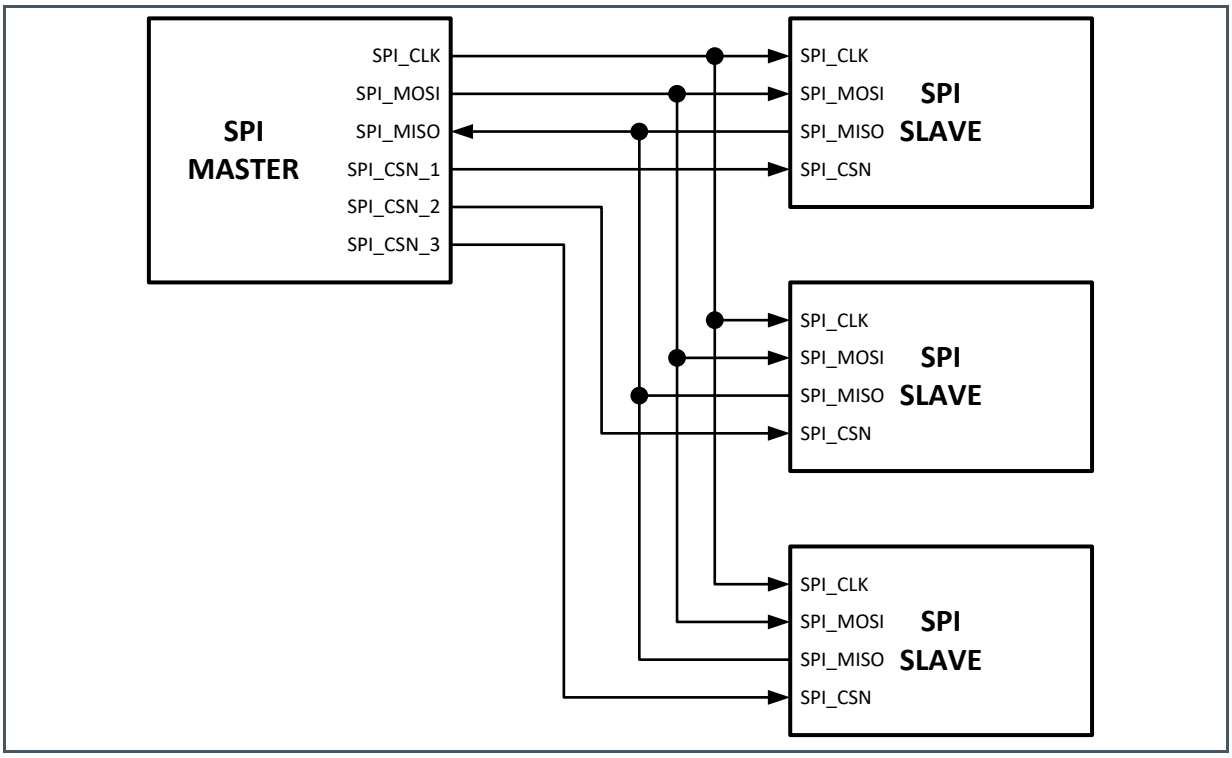
Data is written to the registers of the SPI slave over the SPI_MOSI wire. The data written to the programming registers can also be read out over this same SPI interface, using the SPI_MISO wire. SPI_CSN is an active-low chip select that enables the SPI slave. The details of the timing and data format are described below.

Figure 18:
SPI Connection Diagram



When using multiple image sensors, the SPI_CLK and SPI_MOSI can be shared among them. The SPI_CSN operates as a chip select for each of the slaves. The SPI_MISO can also be shared on a bus because it is tri-stated when it is not used. This configuration of one master and multiple slaves is shown in Figure 18.

Figure 19:
SPI with 1 Master and 3 Slaves



An SPI access always consists of the transfer of the following bits (in this order), as given in Figure 19

Figure 20:
SPI Bits Transfer Sequence

Phase	# Bits	Via	Purpose
CTRL	1	SPI_MOSI	Control bit indicating SPI access direction (1 for write, 0 for read)
ADDR	7	SPI_MOSI	Address (0-127) of register to be accessed
DATA	N*8	SPI_MOSI	Data written to N consecutive register addresses, starting at ADDR
		SPI_MISO	Data read from N consecutive register addresses, starting at ADDR

Via a burst mode, it is possible to write/read multiple consecutive register addresses with a single address upload.

The state of SPI_CLK whenever SPI_CSN is high is ignored, though it is advised to stop the clock to save unnecessary power consumption.

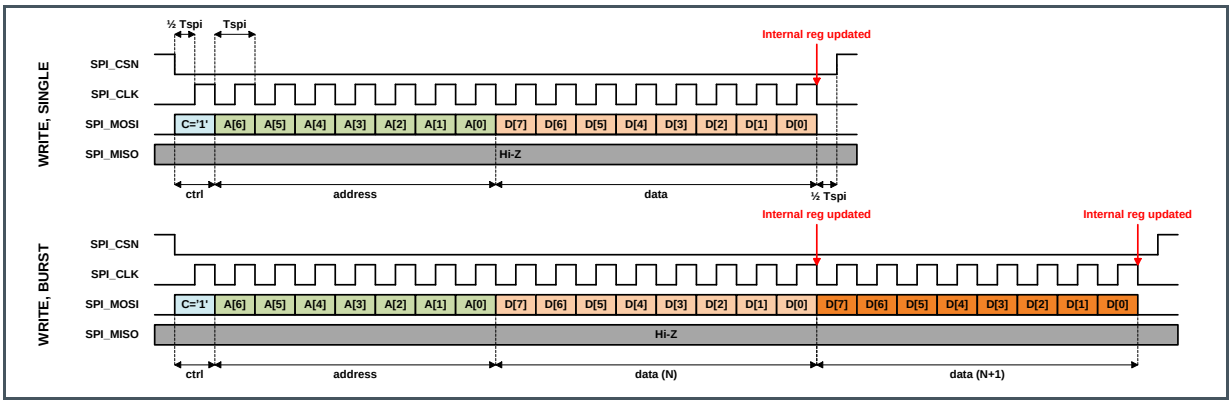
SPI Write

All data bits on SPI_MOSI are sampled by the sensor on the rising edge of SPI_CLK. The chip-select signal, SPI_CSN, shall be low at least ½ of an SPI_CLK period before the first data bit is sampled. SPI_CSN shall remain low for at least ½ of an SPI_CLK period after the last falling edge of SPI_CLK. The first bit transferred is a control bit indicating a write operation (‘1’). Both the subsequent address (A<6:0>) and data (D<7:0>) are sent MSB-first.

When writing multiple sequential registers (e.g. 100, 101, 102 ...), the write burst mode can be used. The address is that of the first register to be written to and the sequencer will automatically shift to the next register after 8 data bits. SPI_CSN shall stay low the entire time.

The actual register value is updated with the new value on the falling edge of SPI_CLK on every D[0] bit. I.e. SPI_CLK shall go low at the end of D[0] for the write sequence to be completed. The timing of both write modes is illustrated below.

Figure 21:
SPI Write Timing

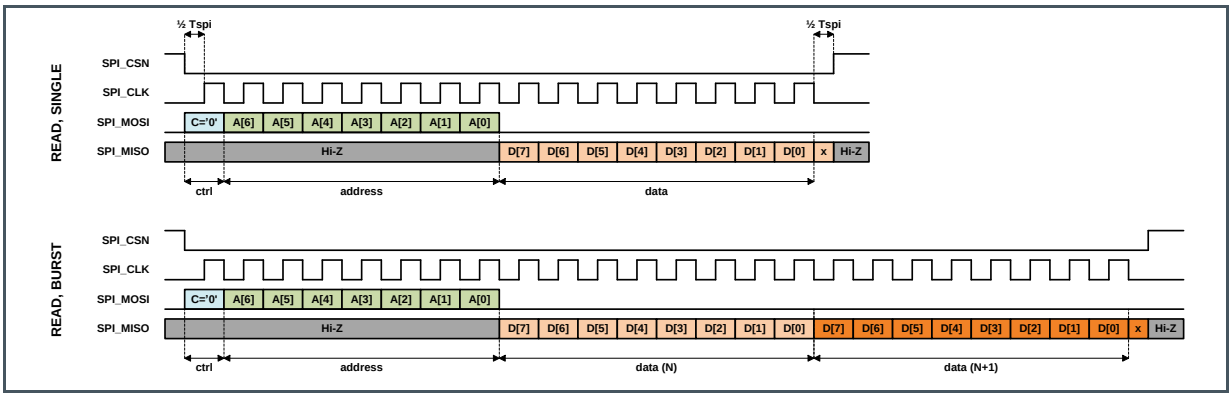


SPI Read

The timing of the SPI read sequence is similar to the SPI write sequence. The main differences are the control bit and the use of SPI_MISO. An SPI read is indicated by setting the control bit to ‘0’. After the control bit, the address of the register to read shall be transmitted MSB first. At the end of the LSB of the address, the data is launched on the SPI_MISO pin on the falling edge of the SPI_CLK. This means that the data can be sampled by the SPI master on the rising edge of the SPI_CLK. The data D<7:0> is transmitted MSB first on SPI_MISO. When not transmitting data, the SPI_MISO output is in high-Z state.

Sequential SPI register addresses can also be read out in burst mode by keeping SPI_CSN low and clocking out additional bytes. The timing of both read modes is illustrated below.

Figure 22:
SPI Read Timing



Register Banks

The sensor's configuration registers are organized in five banks. Each bank contains 124, 8-bit registers.

To select a certain register bank, the register at address 0 is used. Address 0 is always accessible, regardless of the currently selected register bank.

Figure 23:
Bank Selection Register

Register Name	Bit Name	Bank	Addr	Pos	Description
BANK_SEL	BANK_SEL	N/A	0	[2:0]	0: Bank 0 1: Bank 1 2: Bank 2 3: Bank 3 4: Bank 4

The value of BANK_SEL selects which register bank the current SPI access will have an effect on.

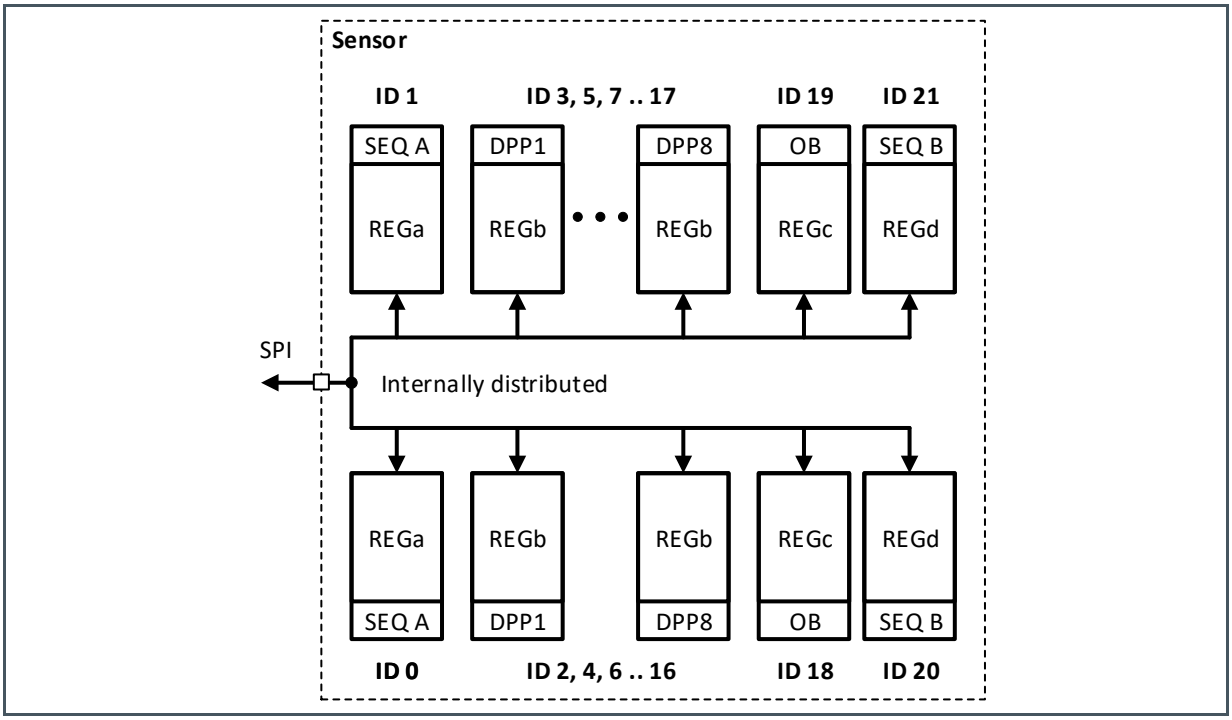
The Block ID

Inside the sensor, there are different blocks that each hold a unique copy of the register banks. The different blocks are the sequencers (A and B) and the DPPs for the output channels (VIS + OB). All of these blocks are connected to the SPI interface and are addressed with a unique identifier called the BLOCK_ID.

Figure 26 shows the organization of all blocks in the sensor along with their BLOCK IDs. The sensor's SPI interface is distributed internally towards all blocks.

The BLOCK_SEL register, located at address 1, determines which block is accessed by future SPI transactions. For example, when the BLOCK_SEL register is set to 0, all SPI read and write operations act on the bottom sequencer A (which has BLOCK_ID 0). The BLOCK_SEL register is always accessible, regardless of the currently selected bank.

Figure 24:
The BLOCK ID



The different blocks contain a certain subset of the total register bank, meaning that not every register is present in every block. This is denoted with REGa, REGb, REGc, and REGd in the figure above. Section 8 gives an overview of all registers that are included in every block.
A register (on a specific address) is always present in at least one block. If the register is present in multiple blocks, then each block hold a unique copy of that register, allowing it to be programmed differently in each of these blocks.

The sensor supports a broadcast mode where all blocks are written at once. This is done by setting the BLOCK_SEL register to 255. This allows faster configuration as not every block has to be programmed individually. Blocks that do not contain the currently addressed register ignore the write operation, i.e. broadcasting does not overwrite anything in blocks that do not have the currently addressed register.

Registers are unique per address. This means that a register (with a certain name) is present on the same address in all blocks that contain this register. For blocks that do not contain this register, the address points to nothing. In this case, write operations are ignored and read operations return all zeros.

Information

SPI read operations in broadcast mode are not supported. The sensor will always return 0 whenever a register is read with BLOCK_SEL set to 255.
SPI read operations can only be performed on single blocks.

Figure 25:
Block Selection Register

Register Name	Bit Name	Bank	Addr	Pos	Description
BLOCK_SEL	BLOCK_SEL	N/A	1	[7:0]	255: Broadcast (write access only) 0: Bottom sequencer A 1: Top sequencer A 2: Bottom data channel 1 3: Top data channel 1 4: Bottom data channel 2 5: Top data channel 2 6: Bottom data channel 3 7: Top data channel 3 8: Bottom data channel 4 9: Top data channel 4 10: Bottom data channel 5 11: Top data channel 5 12: Bottom data channel 6 13: Top data channel 6 14: Bottom data channel 7 15: Top data channel 7 16: Bottom data channel 8 17: Top data channel 8 18: Bottom OB channel 19: Top OB channel 20: Bottom sequencer B 21: Top sequencer B

Active Context Switching

Selected registers related to exposure and readout can be set to define two different modes of operation or contexts. The register RW_CONTEXT selects which context is accessed by the SPI interface for reading or writing.

Contexts can be switched quickly by a single access to the register ACTIVE_CONTEXT. The sensor allows “on-the-fly” context switching, i.e. during any phase of the image acquisition, and will produce consistent images in terms of exposure and readout settings combinations.

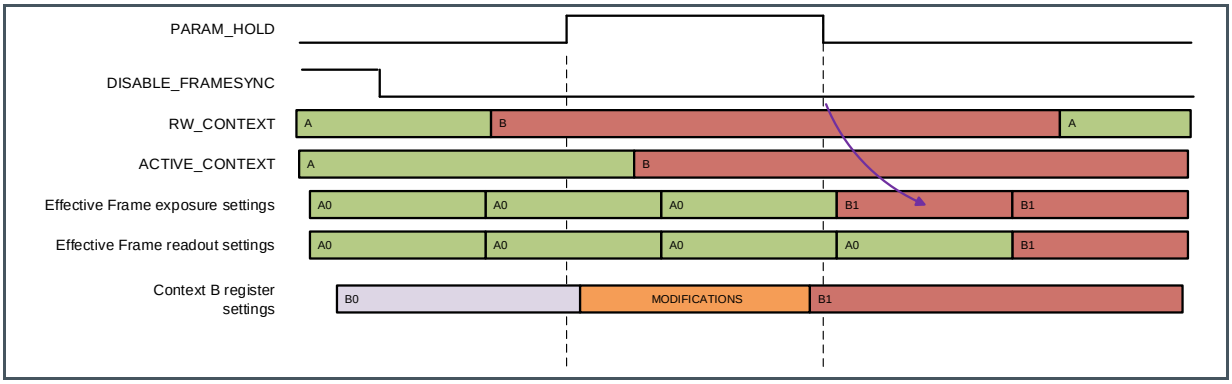
Both RW_CONTEXT and ACTIVE_CONTEXT registers are always accessible, regardless of the currently selected bank.

Figure 26:
Context Switching Registers

Register Name	Bank	Addr	Pos	Description
ACTIVE_CONTEXT	N/A	2	[7:0]	0: Use context A 1: Use context B
RW_CONTEXT	N/A	3	[7:0]	0: Access context A 1: Access context B
PARAM_HOLD	0	4	[0:0]	Must be set to '1' during the new context upload. See detailed procedure below
DISABLE_FRAMESYNC	0	5	[0:0]	Must be set to '0' for on-the-fly context switching.

The figure below shows how to upload a new context B and achieve a seamless context switch from context A to context B while acquiring frames (for example in streaming mode).

Figure 27 :
Context Switch Procedure



(1) DISABLE_FRAMESYNC must be set to '0' first to guarantee uninterrupted frame acquisition
(2) Then set RW_CONTEXT to the inactive context (B in this example)
(3) Set PARAM_HOLD to '1', followed by all modifications to context B registers.
(4) The setting of the new ACTIVE_CONTEXT can be done at any time, while PARAM_HOLD is '1'
(5) When all uploads to context B are done, setting PARAM_HOLD back to '0' will initiate a new frame using the exposure settings of context B, at the first frame time possible, while finishing the readout of the last frame with context A settings in parallel.

Register Categories

The registers are grouped into various categories, based on when they may or may not be updated. The category for every individual register can be found in section 8. The table below explains the details of the various categories.

Figure 28:
Register Categories

Category	Description
-	Registers without category can be changed at any time, but might directly influence the sensor execution.
SYNC	Registers are internally synchronized to start of frame (at the start of the GLOB state), so an entire frame is always read with the same SYNC configuration. This means that the registers may be updated at any time.
CONTEXT	Registers can only be changed in the non-active context (i.e. RW_CONTEXT differs from ACTIVE_CONTEXT). These register can also be changed under the same conditions as DC, if ACTIVE_CONTEXT is the same as RW_CONTEXT.
DC	Can only be changed when sensor is in IDLE state, or in soft reset state.
RST	Only to be changed when sensor is in soft reset state.
RO	Read-only register. All write operations are ignored.

Reading from a register is always allowed. When reading registers of category ‘SYNC’, the last value that was written to the register is read. The value read may differ from the value that the sensor’s logic is currently using, as SYNC registers are frame-synchronized.

Figure 29:
Frame Sync

Reg. Name	Bank	Addr	Bits	Def.	Description
DISABLE_FRAMESYNC	0	5	[0]	0	0: Enable 1: Disable
PARAM_HOLD	0	4	[0]	0	0: Registers are frame synchronized 1: Registers are not frame synchronized

The upload of 'SYNC' type registers can be constrained with the following registers:

If **DISABLE_FRAMESYNC** is set to '1', frame synchronization is disabled. Any uploads will take effect immediately.

Frame synchronization only happens if **PARAM_HOLD** is '0'. When uploading a bunch of SYNC-type registers together (for example, change a number of different YWIN settings), it is advised to set **PARAM_HOLD** to '1' during the entire upload. This prevents a frame from being started with only half of the required updates in case the frame start happened when the entire upload had not completed.

7.2.5 Soft Reset

Figure 30:
Soft Reset Register

Reg.Name	B	Addr	Bits	Description
CMD_REGS.CMD_RST_SOFT_N	0	6	[0]	0: Soft-reset active (brings the sensor in soft-reset state) 1: Soft-reset inactive

The sensor has an asynchronous reset input pin (**RST_N**) and an asynchronous reset register (**CMD_RST_SOFT_N**). Both are active-low.

When combined, they have the following function:

- **RST_N**: Reset the entire sensor when low. This is considered a hard reset.
- **CMD_RST_SOFT_N:** Reset the entire sensor, except the SPI interface and register bank when low. This is considered a soft reset.

As long as RST_N is high, all registers retain their value when CMD_RST_SOFT_N is low.

The procedures to assert and release soft reset are described in detail in section **7.4.3**.

7.2.6 Controlling Exposure and Readout

This section explains the different ways the exposure of a frame can be started and ended. First some important concepts of the frame timing model are explained.

Basic Frame Timing

During operation, the sensor can be in any of the following states:

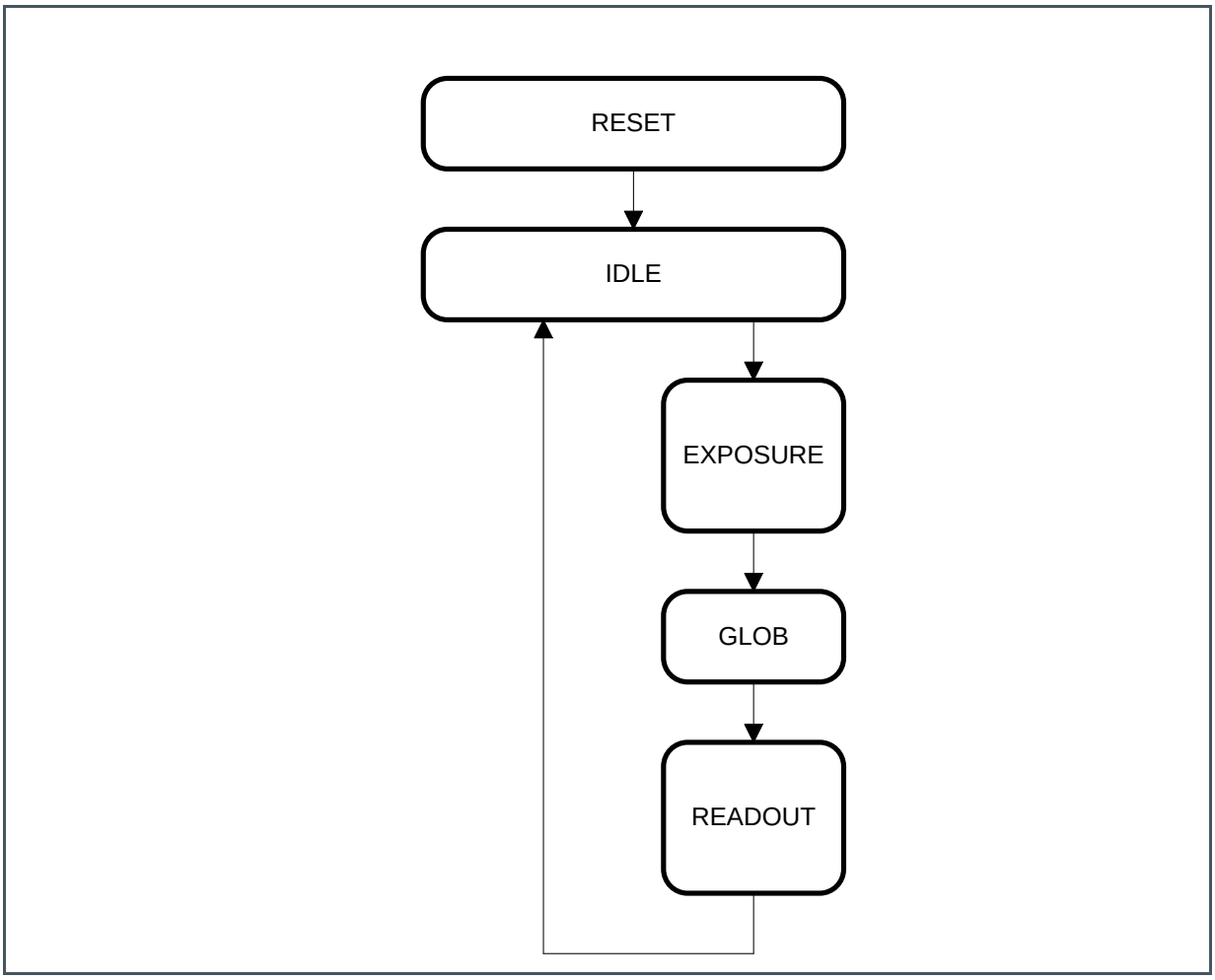
- **RESET:** Asynchronous sensor reset is low, disabling the sensor entirely
- **IDLE:** Sensor is not doing anything while waiting for external requests
- **EXPOSURE:** Light is being integrated in the pixels
- **GLOB:** Closing global shutter by sampling all integrated pixel values
- **READOUT:** Reading out the acquired frame plus meta data and mandatory overhead

A distinction can be made between two basic frame timing operations (sequential and pipelined operation), as detailed in the following two sections.

Sequential Operation

In sequential operation, the sensor goes through a sequential succession of EXPOSURE - GLOB - READOUT to grab a single image, as indicated in the figure below. When a cycle like this has been completed, the sensor is again in an IDLE state, waiting for new commands.

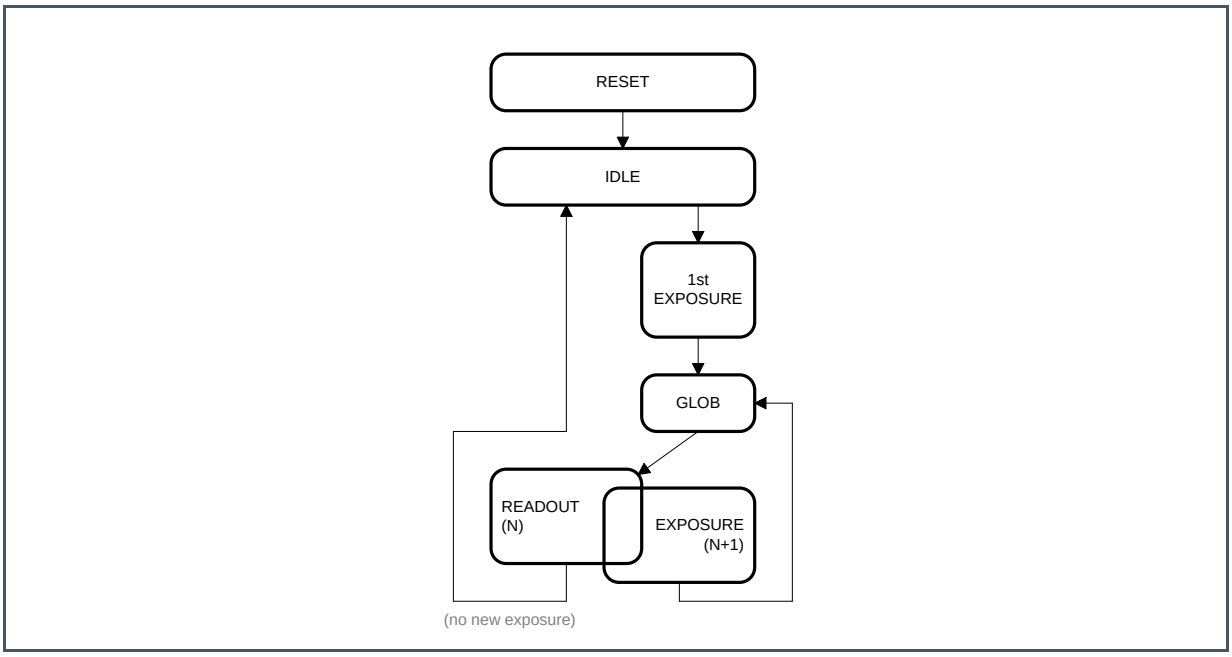
Figure 31:
State Chart: Sequential Operation



Pipelined Operation

The main property of pipelined operation is that the sensor can be in the EXPOSURE state and READOUT state at the same time. This basically means that the readout of frame N can be busy while the EXPOSURE state of frame N+1 has already started. The EXPOSURE can fully or partially overlap with a READOUT state.

Figure 32:
State Chart: Pipelined Operation



When exiting IDLE state, the first EXPOSURE period starts. Just like in the sequential operation, this flows into a GLOB state, which in its turn starts the READOUT of a frame. Depending on the sensor control or configuration (see 7.2.7 for details and options), a new EXPOSURE may start when the READOUT is still busy.

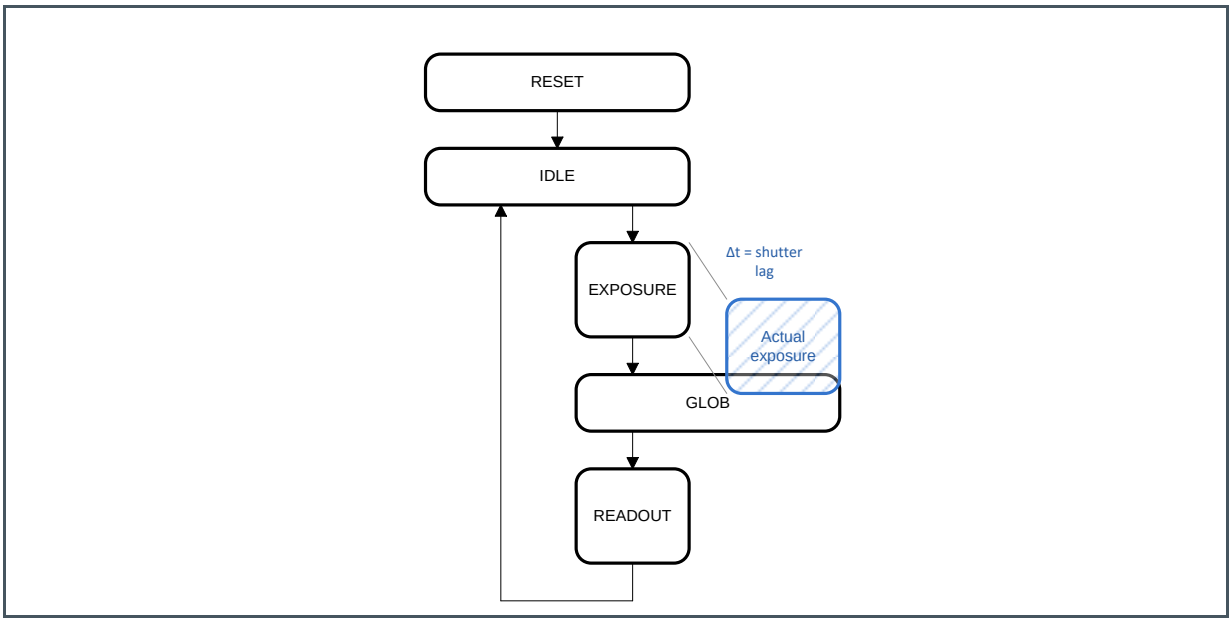
At the end of the READOUT period, there are two options:

- **No new EXPOSURE got started**. The sensor will return to IDLE.
- **A new EXPOSURE did get started**. The sensor will wait until this new EXPOSURE finishes, before moving back to GLOB, which will always trigger a new READOUT.

Shutter Lag

The shutter lag is the delay between the start and end of the **EXPOSURE state** and the start and end of the **actual exposure**. The actual exposure is the time where the sensor is actually capturing and integrating light. Figure 33 illustrates the shutter lag.

Figure 33:
State Diagram: Sequential Operation with Shutter Lag



The distinction is important because the EXPOSURE state is the direct response of external control (through sensor I/O requests or register settings), but it is the actual exposure that really matters to the user.

In the remainder of the document, when the concept of exposure or exposure time is mentioned, it will always be about the **EXPOSURE state**, unless stated otherwise. The reader should always bear in mind that the **actual exposure** is delayed in time with respect to this EXPOSURE state due to the shutter lag mechanism.

In Figure 33, the shutter lag is shown under sequential operating conditions only, but note that the shutter lag is present in all operation modes.

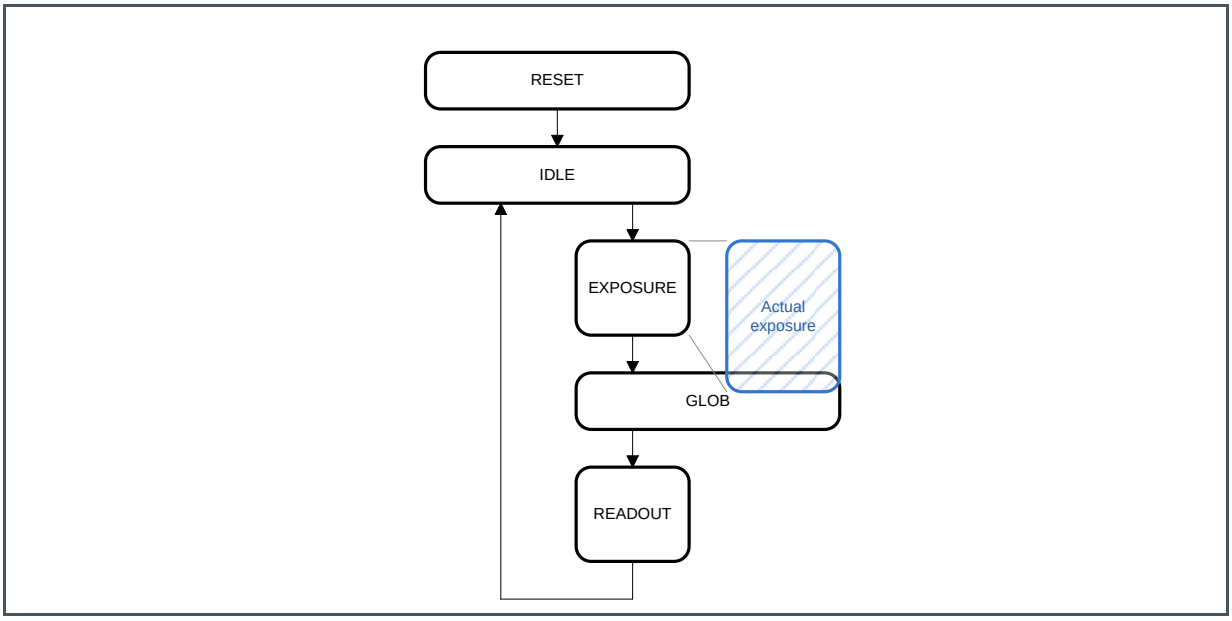
The shutter lag is always present at the end of the EXPOSURE period, since part of the actual exposure time will always extend into the GLOB state. This is sometimes called "exposure overlap". The shutter lag at the beginning of the EXPOSURE periods is introduced artificially to compensate for this exposure overlap.

The shutter lag matching can also be disabled to operate in “no shutter lag”-mode. In that case, the sensor will move to the exposure state after a maximum internal latency of 33 * t_{CLK_PIX} when it receives an exposure request. The start of the actual exposure happens together with the start of the exposure state. As a result, the length of the actual exposure time is larger than the length of the EXPOSURE state (the exposure overlap is added). Figure 34 shows the state diagram with the no shutter lag.

Information

Disabling shutter lag matching causes an image artefact when operating the sensor in pipelined mode. This artefact shows up as one bright row in the output image. The location of that row depends on when the pipelined exposure started.

Figure 34:
State Diagram: Sequential Operation, No Shutter Lag at Start



7.2.7 Sensor Control Modes

Figure 35:
Control Mode Register

Reg.Name	Bank	Addr	Bits	Def.	Description
CTRL_MODE	0	11	[2:0]	0	0: Full external 1: Programmed external 2: Triggered internal 3: Streaming 4: In-line streaming

The travel through the state diagrams of Figure 33 and Figure 34 can be externally controlled with the sensor inputs REQ_EXP and REQ_FRAME and a bunch of register settings (which will be detailed in further sections). This can be done in a number of different modes (each varying slightly in behavior and level of dependency on I/O control versus register configuration).

The control mode is set with the **CTRL_MODE** register, as listed in Figure 36.

Figure 36:
Control Modes

CTRL MODE	Name	External Control	Internal Control
0	Full external	Start of exposure. End of exposure (starting readout).	Readout details.
1	Programmed external	Start of exposure.	Length of exposure. Readout details.
2	Triggered internal	A finite sequence of 1 or more consecutive frames.	Length of exposure. Frame rate. Sequence length. Readout details.
3	Streaming	An infinite sequence of consecutive frames.	Length of exposure. Frame rate. Readout details.
4	In-line streaming(1)		

(1) The in-line streaming mode is a special case, dedicated to readout with very small window sizes for “line scan”-like applications. As it differs quite a lot from the other control modes, it is only mentioned here for completeness' sake and will be further detailed in section 7.8.2.

Each of these control modes is introduced in one of the following sections.

Control Mode 0: Full External

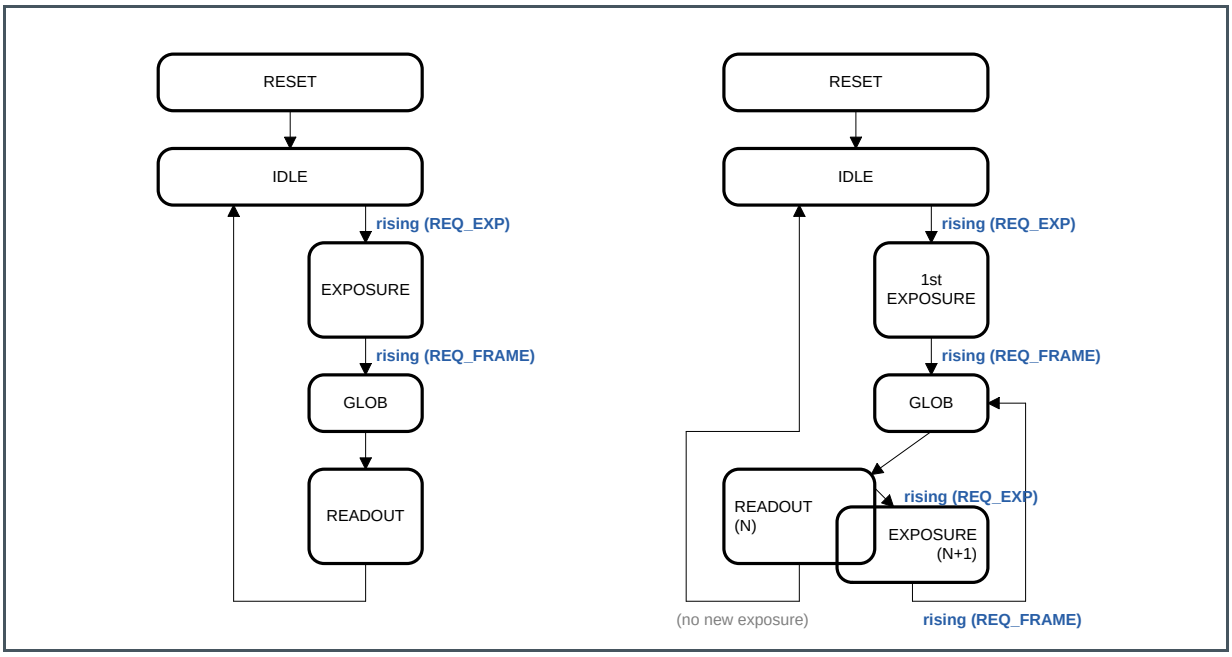
In the *Full External* control mode, the exposure timing is fully controlled with the sensor input pins:

- A rising edge on **REQ_EXP** moves the sensor to the EXPOSURE state
- A rising edge on **REQ_FRAME** moves the sensor to the GLOB state, which will be automatically followed by READOUT.

The length of the EXPOSURE state will exactly match the time between the rising edges of both triggers.

In the figure below, the state diagrams of sequential and pipelined operation are annotated with the external control events.

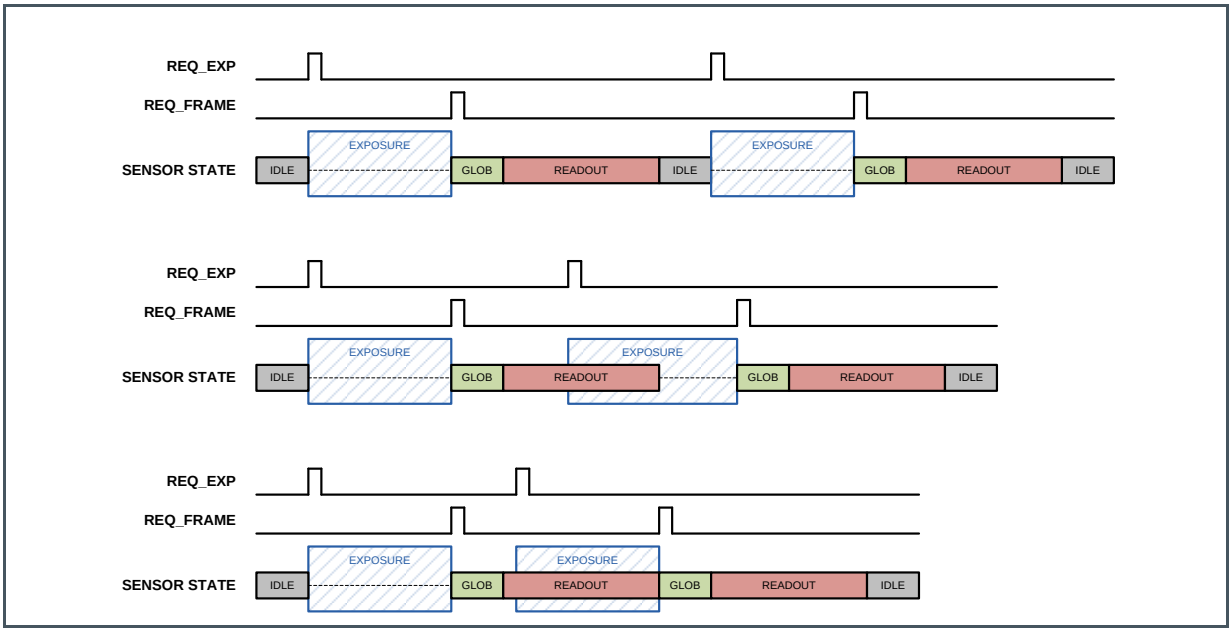
Figure 37:
State Diagram: Full External Mode



The length of the GLOB state, as well as the length of the READOUT period depends on a number of register settings.

The state diagram is expanded into a timing diagram for a few situations in the figure below.

Figure 38:
Timing Diagram: Full External Mode



The figure shows how the *Full External* control mode can be used to (from top to bottom):

- Operate the sensor in *Sequential Operation* mode.
- Operate the sensor in *Pipelined Operation* mode, with the parallel exposure extending beyond the readout phase.
- Operate the sensor in *Pipelined Operation* mode, with the parallel exposure ending together with the readout phase (gives maximum frame rate).

Except for the invalid timings listed in Figure 39 the requests on REQ_EXP and REQ_FRAME can be freely placed anywhere by the external controller. This will result in the most flexible external control possible with this sensor (start and end exposure at any possible time, freely vary exposure time from frame to frame, interrupt frames being read to start a new readout).

Figure 39:
Full External Mode: Invalid Control Timing

#	Invalid Control Timing	Sensor Response
FE_i0	REQ_EXP during GLOB	Will disrupt the GLOB execution, causing the READOUT that naturally follows the GLOB phase to contain corrupted data.
FE_i1	REQ_FRAME during GLOB	Will initiate a new GLOB, followed by READOUT. Image data in this READOUT will be corrupt.
FE_i2	2 consecutive REQ_FRAME, without REQ_EXP in between	Second REQ_FRAME will initiate GLOB followed by READOUT. Since there has not been EXPOSURE, the image data in the second frame will be corrupt.
FE_i3	REQ_FRAME when sensor is IDLE	Same as above: READOUT without EXPOSURE results in corrupted image.

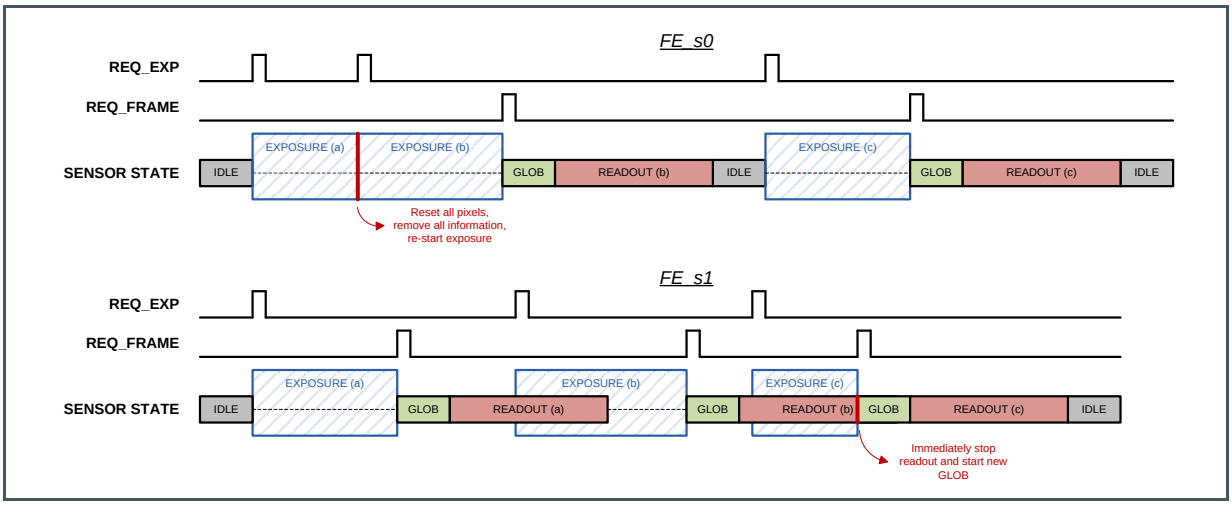
The table below lists some special cases that are not part of the table above and are therefore not illegal (though they each do have some consequences)

Figure 40:
Full External Mode: Special Control Timing

#	Special Control Timing	Sensor Response
FE_s0	REQ_EXP during EXPOSURE	Will initiate a new EXPOSURE, erasing all previously integrated information. The next REQ_FRAME will initiate a GLOB+READOUT that will contain image data of only the second EXPOSURE.
FE_s1	REQ_FRAME during READOUT	Will immediately interrupt the active READOUT to start a new GLOB, followed by a new READOUT. The image information of the first READOUT which had not been read will be forever lost. The new READOUT will be complete and correct (if not violating FE_i2, Figure 39).

The figure below shows an example of the cases listed in Figure 40.

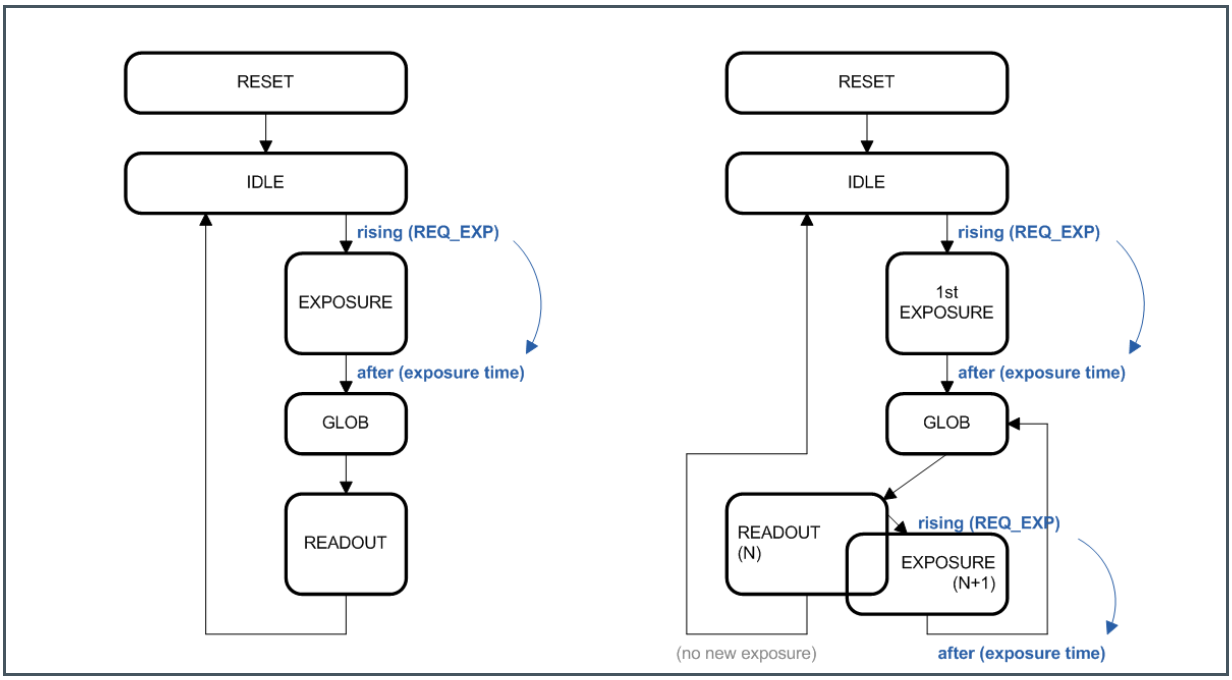
Figure 41:
Timing Diagram: Special Control Timing in Full External Mode



Control Mode 1: Programmed External

This control mode is quite similar to the *Full External* mode, with the exception that the transition from EXPOSURE to GLOB state is not triggered by a pulse on REQ_FRAME sensor input. Instead the sensor ends the EXPOSURE period and moves to GLOB after a programmable time, set by register upload. This behavior is illustrated in the figure below.

Figure 42:
State Diagram: Programmed External Mode



Expanding this to a timing diagram gives similar timings to the ones shown in Figure 38 with REQ_FRAME continuously low.

Since this mode is so similar to the *Full External* mode, also the lists of invalid and special control timing are quite similar.

Figure 43:
Programmed External Mode: Invalid and Special Control Timing

#	Invalid Control Timing	Sensor Response
PE_i0	REQ_EXP during GLOB	Same response as FE_i0
PE_i1	EXPOSURE time expires during GLOB	Same response as FE_i1

#	Special Control Timing	**Sensor** Response
PE_s0	REQ_EXP during EXPOSURE	Same response as FE_s0
PE_s1	EXPOSURE time expires during READOUT	Same response as FE_s1
PE_s2	Any pulse on REQ_FRAME	Will be ignored

Control Mode 2: Triggered Internal

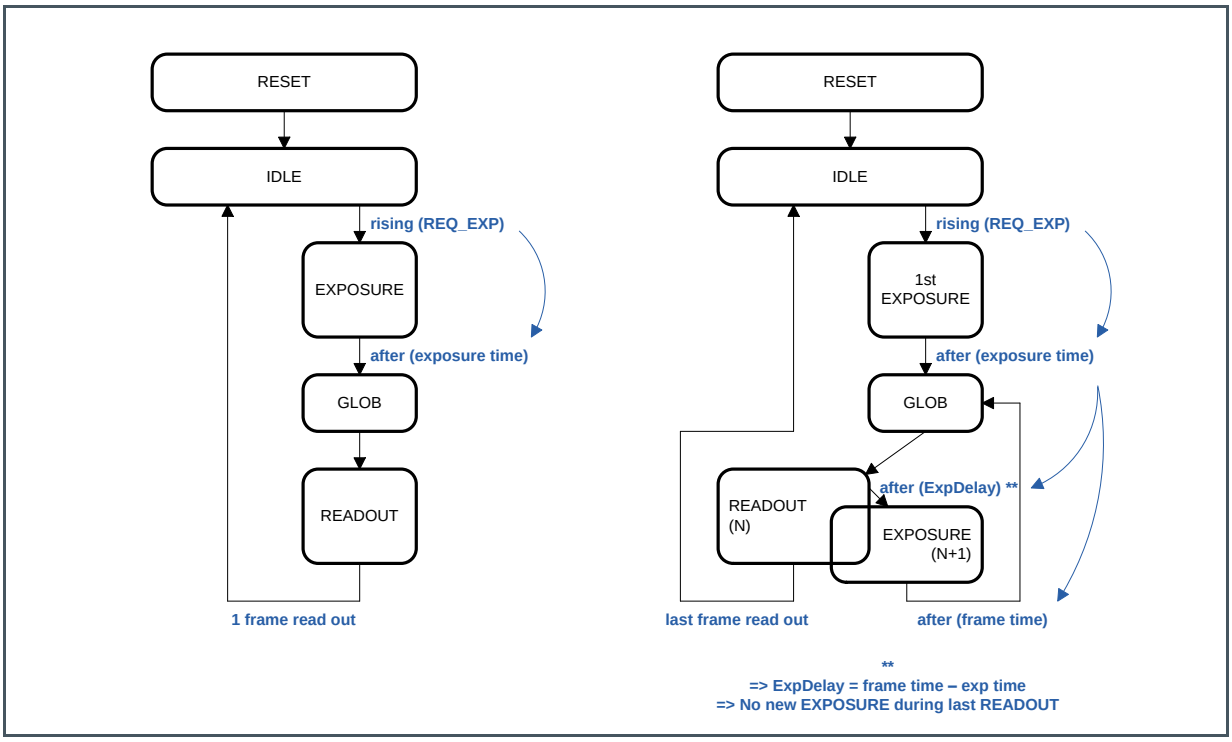
Both external control modes have in common that every external request results in exactly one sensor response:

- In Full External mode:
  - Each REQ_EXP initiates 1 EXPOSURE period
  - Each REQ_FRAME initiates 1 GLOB period, followed by READOUT
- In Programmed External mode:
  - Each REQ_EXP initiates the complete readout of 1 frame (EXPOSURE, GLOB and READOUT).

This means that in those two modes, the frame rate is fully controlled externally by timing the requests.

In the *Triggered Internal* mode, a single request is followed by a programmable number of frames, at a frame rate also set by register upload.

Figure 44:
State Diagram: Triggered Internal Mode



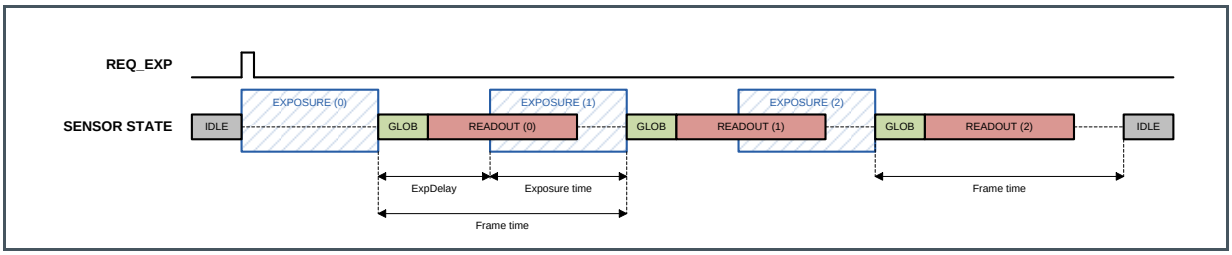
When exiting IDLE mode, the behavior is identical to Programmed External mode: a rising edge on REQ_EXP will initiate the EXPOSURE state, which ends after a register defined exposure time. When the exposure time expires, a GLOB state is started, followed by READOUT.

The behavior during the READOUT phase depends on the number of frames that were requested (also set by register) and the amount of frames that have already been read during the active sequence:

- Last READOUT of requested sequence:
  - Finish active READOUT and move back to IDLE state
- All other READOUT:
  - Restart EXPOSURE for the next frame. EXPOSURE is started at the correct moment to make it finish exactly 'frame time' later than the GLOB period was started.
  - The end of this EXPOSURE will initiate a new GLOB phase.
  - Because a GLOB period immediately follows the EXPOSURE period, there will be exactly 'frame time' delay between two consecutive frames.

An example (with 3 frames requested) is shown in the figure below.

Figure 45:
Timing Diagram: Triggered Internal Mode



In the example, the programmed 'frame time' is longer than the sum of GLOB length and READOUT length. This situation is allowed and provides an easy mechanism to fine-tune frame rate.

In the most extreme case, the programmed frame time exactly matches the minimum length of the GLOB and READOUT phases together. This will start a new GLOB period as soon as the previous READOUT is finished, which results in the maximum frame rate for given GLOB and READOUT settings.

Because this mode is internally controlled based on register settings, there are no invalid control timing conditions. Invalid register settings do exist (for example: frame time shorter than GLOB+READOUT length), but these are specified in the relevant sections describing those registers later in this document.

The table below lists the special timing conditions of this mode.

Figure 46:
Triggered Internal Mode: Special Control Timing

#	Special Control Timing	Sensor Response
TI_s0	REQ_EXP ***before*** last READOUT of sequence has started	Will do nothing else than increase the sequence length (add the number of frames of the new request to the total length of this sequence, with a maximum total of 255 frames).
TI_s1	REQ_EXP ***after*** last READOUT of sequence has started	Will initiate a new 'first' EXPOSURE, followed by a complete new sequence. Depending on the timing of the new request, the frame rate may be temporally change. See below.
TI_s2	Any pulse on REQ_FRAME	Will be ignored

The behavior in case of TI_s1 depends on the relation between (1) the programmed exposure time of the new request and (2) the time remaining to complete the active frame (see last 'Frame time' in Figure 45).

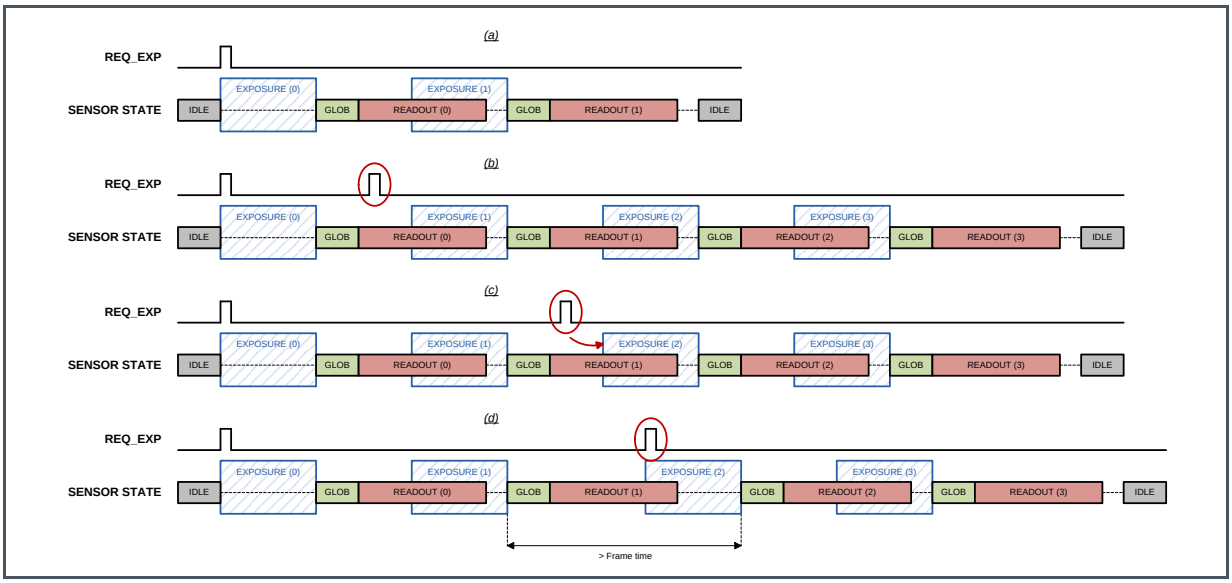
- If (1) < (2):
  - The start of the new EXPOSURE will be delayed.
  - It will be started at the correct moment so its end will coincide with the end of the active frame.

- The frame rate will not change: the first GLOB of the new sequence will be exactly 'frame time' after the last GLOB of the active sequence.

- If (1) > (2)
  - The new EXPOSURE will start immediately.
  - Because (1) is larger than (2), this EXPOSURE will end after the last frame would have finished.
  - This causes a temporary drop in frame rate.

The figure below shows the following cases (in all cases, the requested sequence is 2 frames long):

Figure 47:
Timing Diagram: Special Control Timing in Triggered Internal Mode



(a) Normal timing → Capture 2 frames and go back to idle when done
(b) TI_s0 → New request before last frame is active; extend sequence length to 4
(c) TI_s1, (1) < (2) → New EXPOSURE delayed to guarantee programmed frame rate
(d) TI_s1, (1) > (2) → Temporary frame rate decrease to guarantee complete exposure time

Programmed External vs Triggered Internal

The attentive reader may have noticed that the *Triggered Internal* mode with a sequence length of 1 is quite similar to the *Programmed External* mode. This is mainly true, yet both differ in the way they handle new REQ_EXP requests if the sensor is **not IDLE**.

Figure 48:
Special Control Timing: PE and TI Comparison

#	Special Timing	Programmed External Response	Triggered Internal Response
PE_i0	REQ_EXP during GLOB	Will corrupt next frame	= TI_s0 Sequence length extended by 1 frame with every new request
PE_s0	REQ_EXP during EXPOSURE	Will stop EXPOSURE and start new one	Impossible situation: EXPOSURE by construction never finishes during READOUT or GLOB
PE_i1	EXPOSURE time expires during GLOB	Will corrupt next frame	
PE_s1	EXPOSURE time expires during READOUT	Will stop READOUT and start new GLOB	
TI_s0	REQ_EXP ***before*** last READOUT of sequence has started	= PE_i0 or PE_s0	Extend sequence length
TI_s1	REQ_EXP ***after*** last READOUT of sequence has started	Will start new exposure immediately, resulting in default behavior or PE_s1	Will start new exposure (directly or after delay, see Figure 47)

In summary:

- *Triggered Internal* is the more forgiving mode. It adjusts the actual timing and scheduling of events as needed to always yield complete and correct images.
- *Programmed External* mode (and by extend also *Full External* mode) however directly responds to external requests at the cost of possibly corrupting or interrupting images but no missing higher priority exposures.

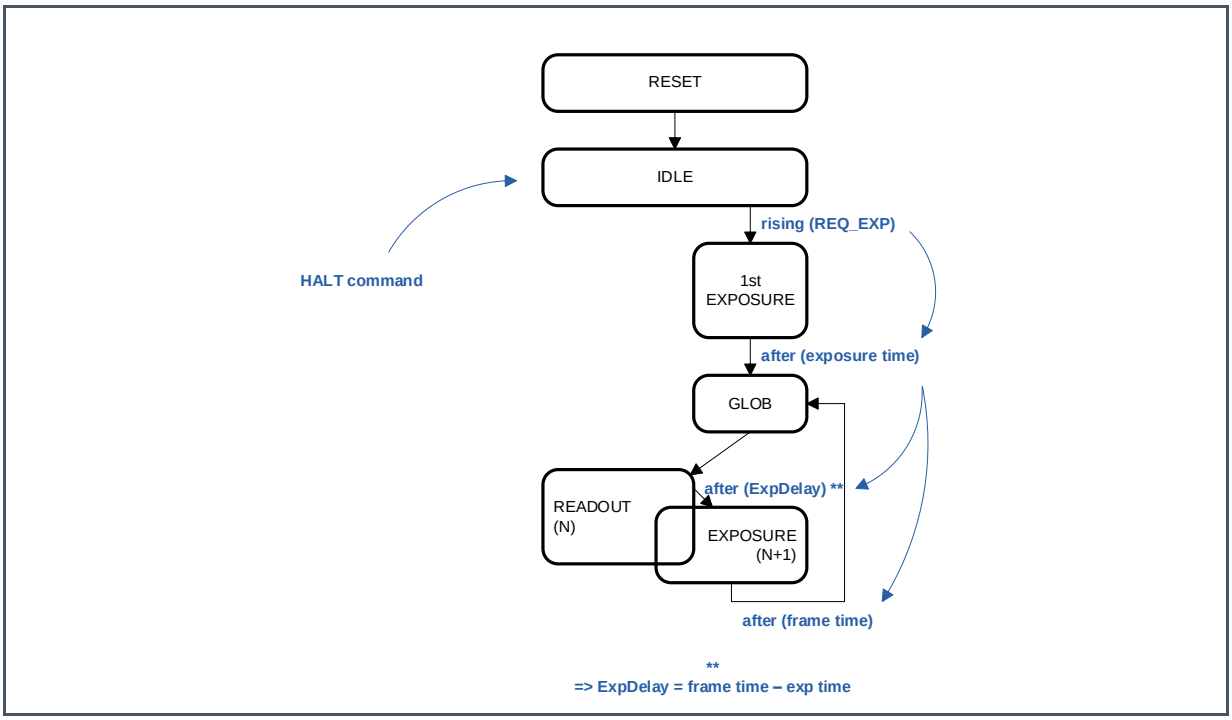
Control Mode 3: Streaming

Streaming mode is nothing else than *Triggered Internal* mode with an infinite sequence length.

After starting the *Streaming* mode with a rising edge on REQ_EXP, it will keep on generating a continuous stream of frames forever until stopped explicitly (via sensor reset or HALT command; see section 7.2.8). As in Triggered Internal mode, the entire frame configuration is done by register upload.

Next figure shows the state diagram of the *Streaming* mode.

Figure 49:
State Diagram: Streaming Mode



Because of the nature of the streaming mode, there is no such thing as invalid or special control timing. Once started, it will be forever looping and all further REQ_EXP and REQ_FRAME pulses are ignored.

7.2.8 Software Commands

Figure 50:
Software Command Registers

Reg.Name	Bank	Addr	Bits
CMD_REGS.CMD_RST_SOFT_N	0	6	[0]
CMD_REGS.CMD_REQ_EXP	0	6	[1]
CMD_REGS.CMD_REQ_FRAME	0	6	[2]
CMD_REGS.CMD_HALT_BLOCK	0	6	[3]
CMD_REGS.CMD_HALT_NBLOCK	0	6	[4]

The register bits **CMD_REQ_EXP** and **CMD_REQ_FRAME** are equivalent to their sensor input counterparts REQ_EXP and REQ_FRAME. The sensor REQ_EXP and REQ_FRAME inputs can therefore be tied low to use the register uploads for frame timing control. By setting the CMD register bit, the respective command is sent to the internal control logic. The CMD bits are not automatically

cleared after a request is progressed, this should be done by the user. Note that the sensor's internal registers are updated at the end of the SPI data transfer, as detailed in section 7.2.4.

By using the three registers defined above, the sensor can in theory be controlled with just the SPI interface plus 2 timing inputs (RST_N and CLK_IN) at the cost of a slightly reduced timing accuracy (because the registers are loaded via the SPI interface).

The two HALT commands can be used to stop any active sensor operation and return the sensor to the IDLE state, waiting for new requests. The difference between the two is:

- **CMD_HALT_BLOCK**: When asserted, the active READOUT is finished before moving to IDLE state.
- **CMD_HALT_NBLOCK**: When asserted, all the operations are stopped immediately and the sensor directly moves to IDLE state.

The HALT commands are a good way to get the sensor out of the *Streaming* control mode without asserting any reset.

7.3 Sensor Readout Format

The sensor puts out image data in a format similar to the CMV sensor family. Sub-LVDS channels are used for data transfer, with separate clock and control channels running in parallel, to be used for data sampling and sync codes.

The CSG14K_CSG8K has sub-LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Data is read out simultaneously from both sides (top and bottom) of the pixel array. The sensor has the following channels on each side:

- 8 Data channels
- 1 OB data channel (optional)
- 1 Control channel
- 1 Clock channel

In total, the sensor has 22 sub-LVDS output pairs (2 pins for each sub-LVDS channel). This means that a total of 44 pins of the CSG14K_CSG8K are used for the sub-LVDS outputs. See the pin list for the exact pin numbers of the sub-LVDS outputs.

The data channels are used to transfer the pixel data from the sensor to the receiver in the surrounding system.

The output clock channel transports a clock, synchronous to the data on the other sub-LVDS channels. This clock should be used at the receiving end to sample the data. This clock is a DDR clock, which means that the frequency will be half of the output data rate. When 1250 Mbit/s output data rate is used, the sub-LVDS output clock will be 625 MHz.

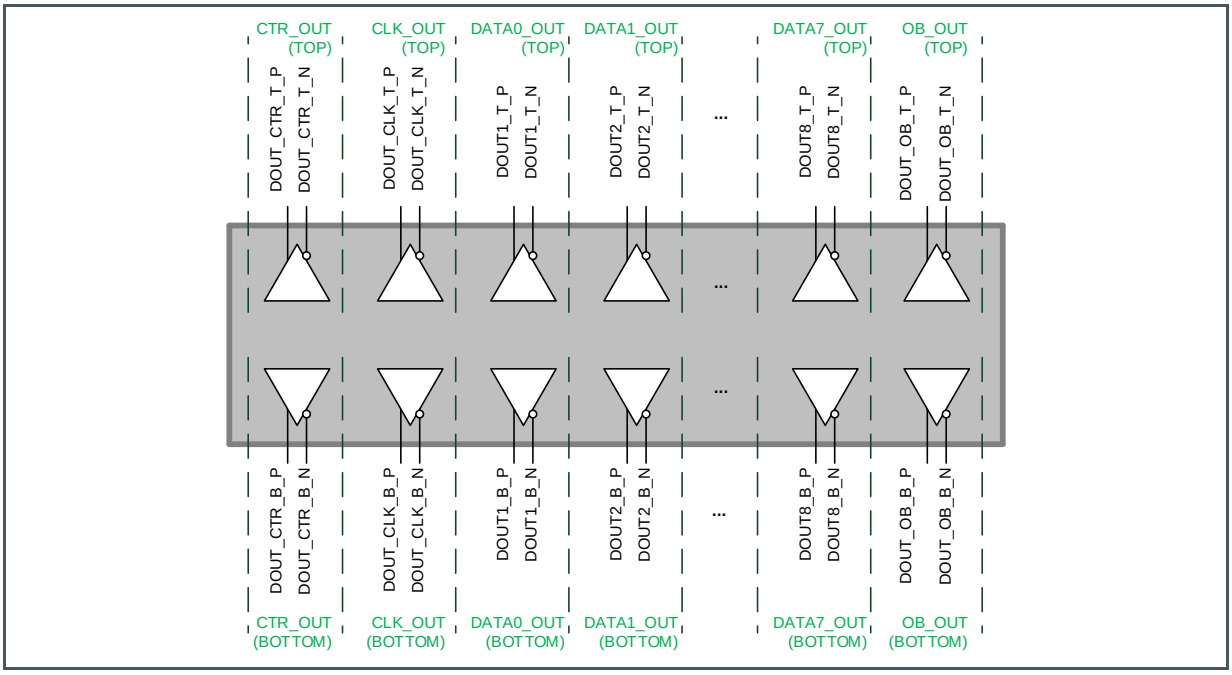
Information

The top and bottom output channels are not aligned. The user should use the top side clock and control channels to evaluate the top data channels, and the bottom side clock and control channels to evaluate the bottom data channels.

The data on the control channel contains status information on the validity of the data on the data channels, along with status information on the sensor state. Information on the control channel is grouped into 12-bit words that are transferred synchronous to the data channels.

The figure below shows the data output interface.

Figure 51:
Sub-LVDS Data Output Interface



Each pair of differential output pins transports data on one sub-LVDS channel.

For easier reading and writing, the channels will be called CTR_OUT, DATAx_OUT, OB_OUT and CLK_OUT in the remainder of the document. The output channels have the following functionality:

Figure 52:
Sub-LVDS Output Channels Functionality

Name	Function
CLK_OUT	Should be used as sampling clock.
CTR_OUT	Serially transmit status word. Captures sensor status and data validity in various status bits.

Name	Function
DATAx_OUT	Serially transmit pixel data. Every channel transmits the data of 1 pixel, so up to 16 pixels are transmitted at the same time from the sensor.
OB_OUT	Serially transmit pixel data of pixels in OB columns.

Information

At the sensor output, all channels are bit and word aligned with minimal skew (per readout side). Yet, it is advised to perform bit-alignment on the receiver to optimize the sample point of every data channel.

Reading out a frame is done row-by-row. The pixels of a row are evenly distributed along all enabled outputs. Any number between 1 and 8 DATAx_OUT channels (per side) can be used, depending on the horizontal multiplexing settings (see section 7.6.2). DATA0_OUT is always active. If more than 1 channel is used, additional channels are enabled from left to right.

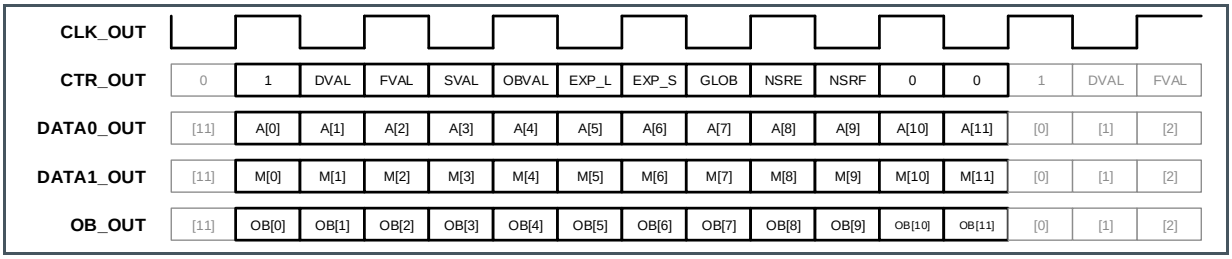
Using the OB_OUT channel is optional, because by default the row OB corrections (using the OB columns) are done on-chip.

Low-Level Pixel Timing

- Data is transferred serially over each channel, one complete word at a time.
- Data is transferred either LSBit or MSBit first through configuration.
- All channels are word aligned (first bit of all channels sent during same CLK_OUT cycle).

This results in the timing diagram in the figure below (shown for 12-bit data, LSBit first).

Figure 53:
Low-Level Pixel Timing (per side)



Control Channel

Like all other data channels, the CTR_OUT channel transmits its data word-based. A word being transmitted on the CTR channel consists of a number of bits, each reflecting the status of a certain aspect of the sensor behavior. The table below lists the function of each bit.

Figure 54:
Control Word

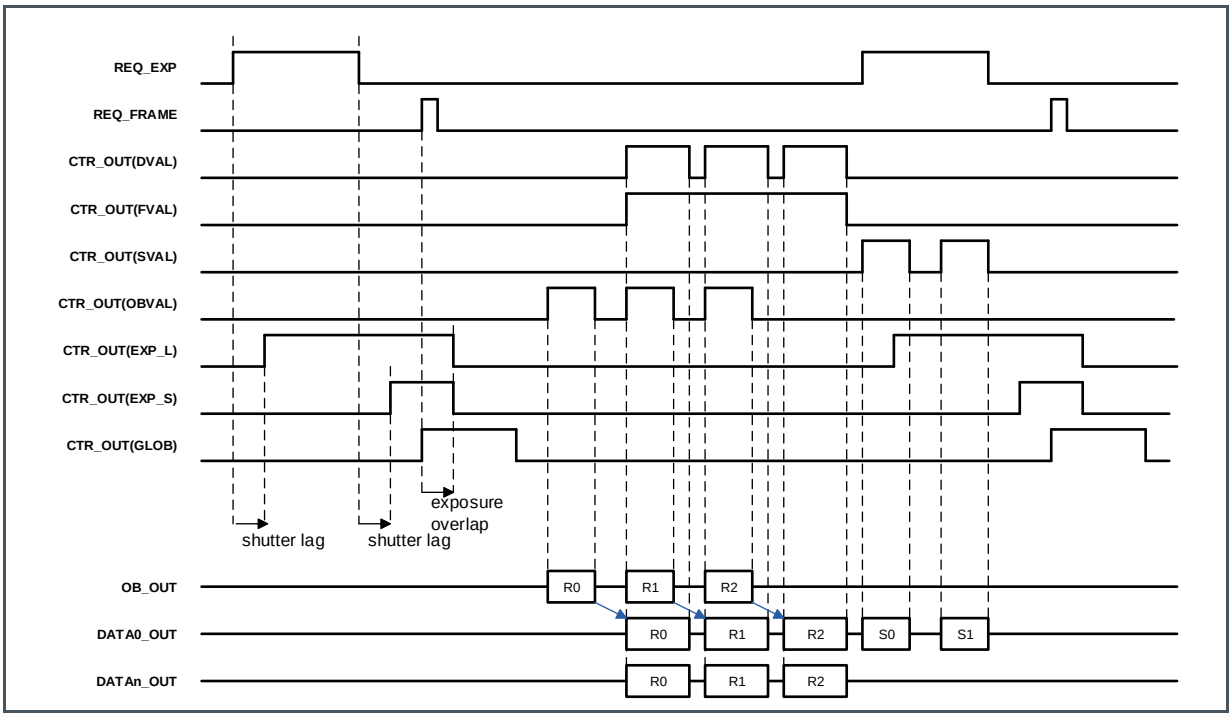
#	Name	Function
[0]	SYNC	Always '1'
[1]	DVAL	High when there is valid pixel data on DATAx_OUT. (Stays high for entire row of valid data)
[2]	FVAL	Goes high together with first DVAL of frame. Goes low together with last DVAL of frame. (Frames valid frame)
[3]	SVAL	High when there is valid statistics data on DATA0_OUT
[4]	OBVAL	High when there is valid OB pixel data on OB_OUT
[5]	EXP_L	High when exposure group 'L' is integrating light
[6]	EXP_S	High when exposure group 'S' is integrating light
[7]	GLOB	High when sensor is in GLOB state
[8]	NSRE	(optional) High when it is Not Safe to Request a new Exposure
[9]	NSRF	(optional) High when it is Not Safe to Request a new Frame
[10:11]	N/A	Always ‘0’

Figure 53 illustrates how the control word is transferred in line with pixel data. At the controller side, the data on CTR_OUT should be de-serialized like any other data channel. In the parallel domain, the various bits of the word can be used to extract status information on the sensor.

The figure below shows the timing of the various bits of the control word in an example frame. The timing of the bits is shown in the parallel domain. Some remarks concerning the figure:

- Sensor is in full external control mode
- Dual exposure time is active (EXP_L is different from EXP_S)
- Only 2 histograms of image statistics are requested (typically there will be 0, 1 or 5)
- The frame size (y-window settings) is 3 rows.
- The optional NSRE and NSRF bits are disabled and not shown. These bits are discussed in more detail in 7.8.3.

Figure 55:
CTR_OUT Channel Bits Timing



Some notes concerning the figure:

- EXP_L and EXP_S indicate the actual exposure time (so taking shutter lag and exposure overlap into account)
- The READOUT phase of the sensor (as used in section 7.2.6) is more than only FVAL. There is some overhead time between the end of GLOB and the start of FVAL.
- Two DVAL periods are separated by an overhead time (OT). The length of this overhead time depends on the channel multiplexing and row time settings, but will be at least 1 word.
- The OB data of a row of pixels appears on OB_OUT about one row time before the valid pixel data of the same row appears on DATAx_OUT. The exact timing is evident on the control channel. This allows external grabbing and evaluation of the OB data before the pixels of the same row are being read. This way, corrections can be done without the need for an additional row buffer.
- Image statistics data is always sent via DATA0_OUT and is framed with the SVAL bit.

Information

The sensor can be operated without using the control channel. The presence of the inverted training word on each of the LVDS output channels allows to recognize the start of data transmission. The advantage is reduced complexity and possible power savings by disabling the CTRL channel LVDS output, also see section 7.6.1. For more details, an application note is available.

7.4 Configuring the Sensor

This section provides detailed recipes for configuring the sensor in a certain operation mode. Refer to sections 7.5.1 and 7.6 for details on sensor exposure control and reading out images.

7.4.1 Image Modes

The sensor supports a number of images modes, listed in the table below, targeted for different use-cases. Each image mode corresponds to an optimized sensor configuration, resulting in an optimal sensor performance for each use-case (e.g. maximum framerate, output resolution, power consumption, dynamic range …, see also Figure 8). Depending on the selected image mode, specific sensor settings (as defined in the following sections) will be applicable.

Figure 56:
Image Modes

Image Modes	Description
IMG.1	10-bit default mode
IMG.2	10-bit short exposure mode
IMG.3	10-bit small window mode
IMG.4	12-bit default mode
IMG.5	12-bit short exposure mode
IMG.7	12-bit binning mode

Information

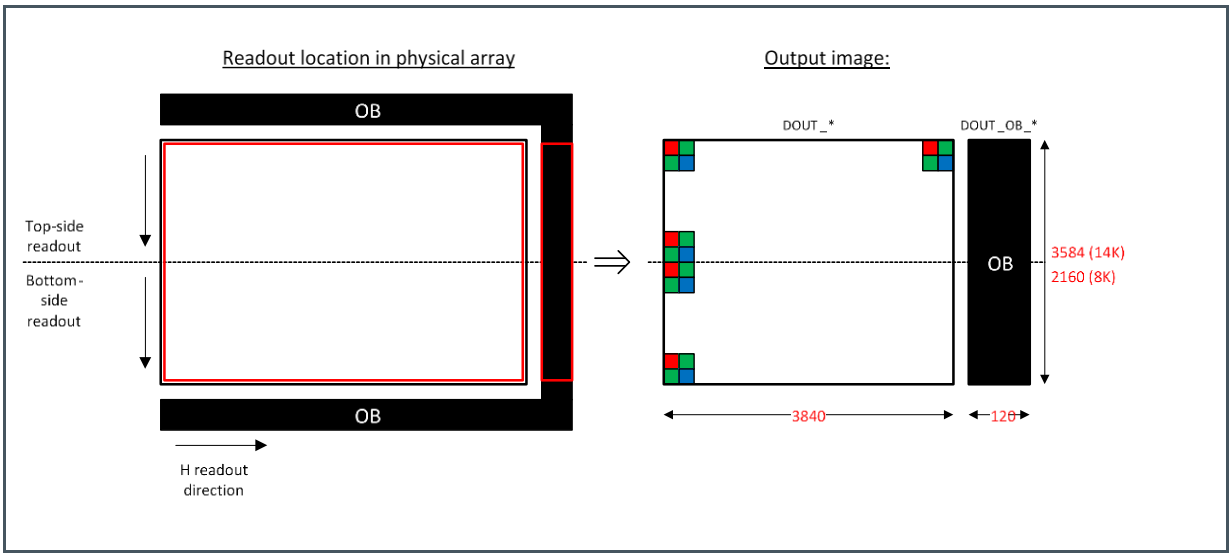
Depending on the image mode chosen, additional limitations may apply to the maximum internal clock rate of the sensor (PLL configuration), and resulting maximum output data rate. See section 7.4.3, subsection “Set PLL” for details.

10-Bit and 12-Bit Default Modes (IMG.1 and IMG.4)

The 10-bit and 12-bit default modes implement the most generic readout mode, targeting a full sensor readout at maximum resolution.

Figure 57 shows the pixel readout area and corresponding output image properties in case the horizontal and vertical ROI are set to the recommended values and OB channel readout is enabled.

Figure 57:
Recommended ROI Selection and Resulting Output Image Format in IMG.1 and IMG.4



10-Bit and 12-Bit Short Exposure Modes (IMG.2 and IMG.5)

The 10-bit and 12-bit short exposure modes target the usage of a minimal exposure time. These modes should only be used when very short exposure times are required. The short exposure modes have the following limitations:

- Pipelined exposure is not possible. This means a new exposure cannot be started when the readout of the previous frame is still ongoing.
- Shutter lag matching cannot be disabled. This means it is not possible to start exposure immediately after the exposure request.

The maximum recommended exposure time in the short exposure modes is limited to 100 µs. For longer exposure times, it is recommended to use the default modes (IMG.1 or IMG.4).

The image readout area and output image format is identical to the default modes (IMG.1 and IMG.4), as shown in Figure 57.

10-Bit Small Window Mode (IMG.3)

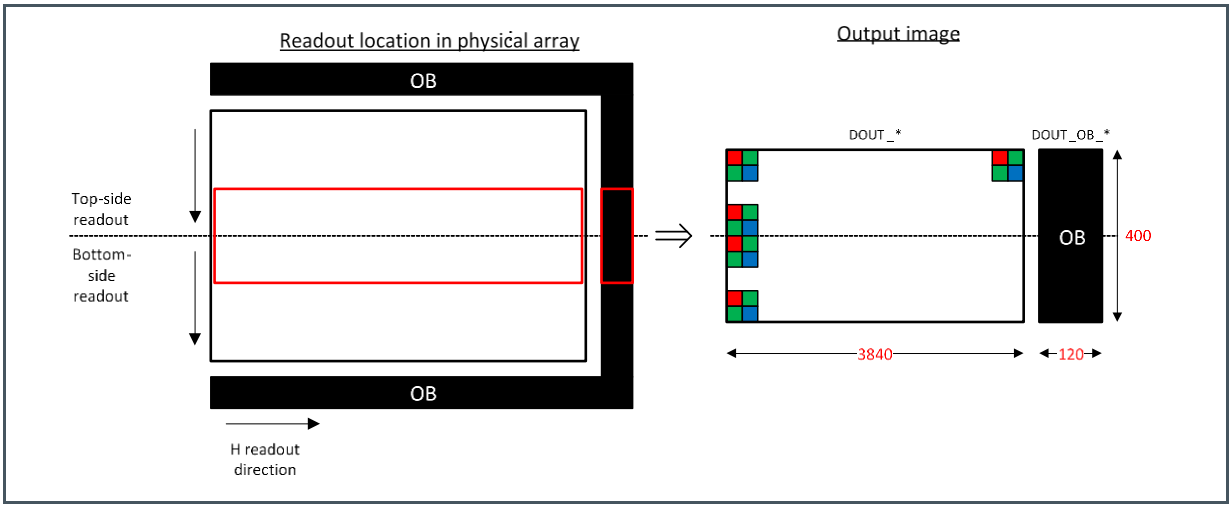
The 10-bit small window mode result in an increased maximum frame rate when the vertical ROI is limited. The frame rate increase is achieved by disabling the pixel control signal drivers in the unused part of the image array, which reduces the required time of the global sample period.

The small window modes have the following limitations:

- The vertical ROI is limited to a centered window of maximum 2x200 rows. Rows outside this centered region cannot be read out.

Figure 58 shows the active pixel readout area and corresponding output image properties. This example assumes the maximum allowed vertical ROI (2x200 rows) and that OB channel readout is enabled.

Figure 58:
Recommended ROI Selection and Resulting Output Image Format in IMG.3



Information

- The recommended sensor control mode for the small window modes is Inline Streaming. This control mode maximizes the frame rate as it reduces the amount of overhead rows in a frame. See section 7.8.2 for more information on the Inline Streaming mode.
- The small window modes can also be operated in any of the other sensor control modes.

12-Bit Binning Mode (IMG.7)

The 12-bit binning mode implements a sensor readout in which the value of 4 pixels are averaged, prior to ADC conversion. This reduces the readout resolution by 4x, but increases the full well charge, dynamic range and SNR.

Figure 59 shows the binning schemes for color and monochrome modes. In color mode, the binning scheme is adapted to preserve the Bayer pattern. The averaged value of 4 binned pixels is readout on the bottom-left position of the binned square.

Figure 59:
Color and Monochrome Binning Modes

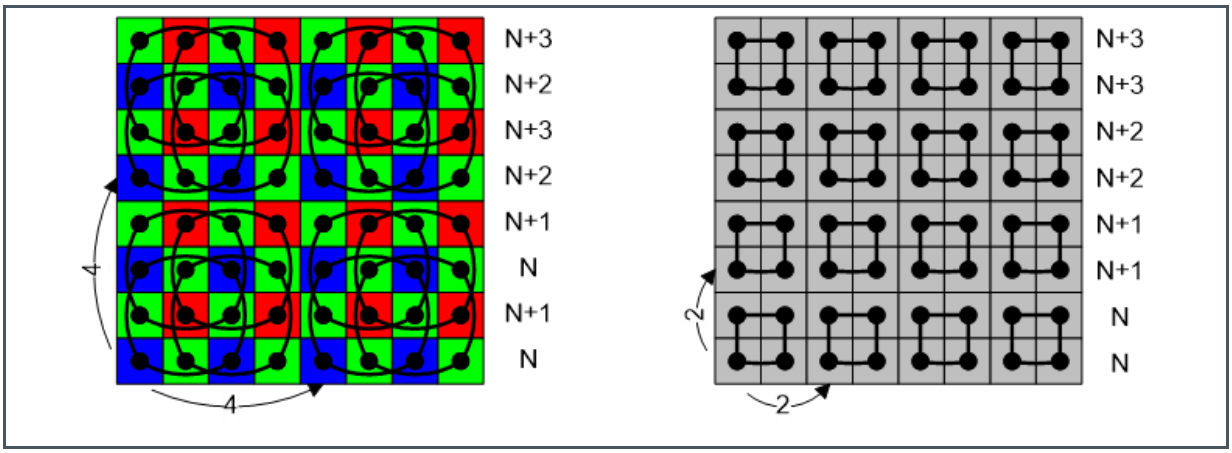
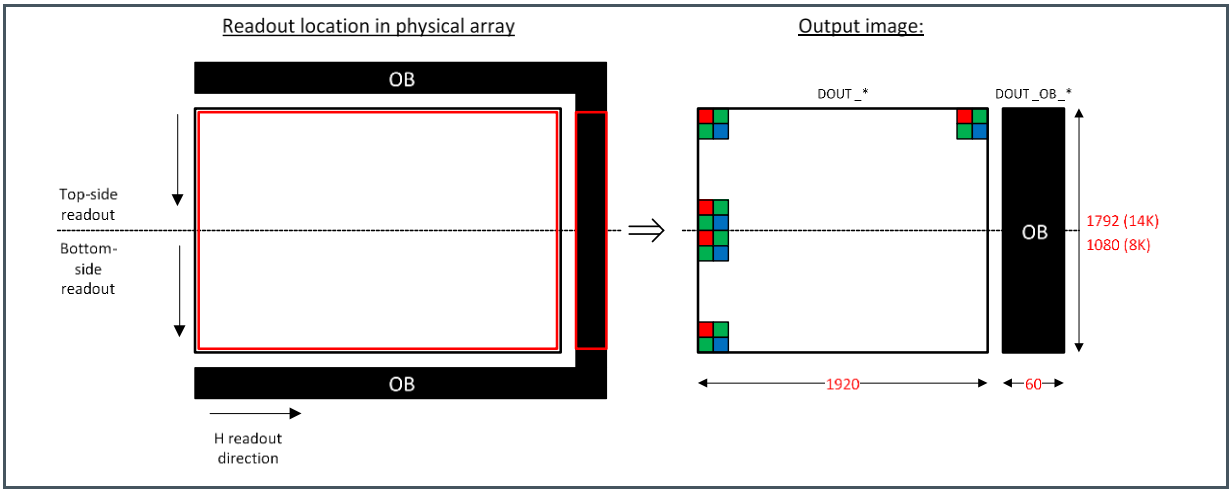


Figure 60 shows the active pixel readout area and corresponding output image properties in case of default ROI settings. Although the physical ROI on the pixel array is identical to the default 12-bit mode (IMG.4), the output image dimension is reduced by 50% in each dimension due to the binning operation.

Figure 60:
Recommended ROI Selection and Resulting Output Image Format in IMG.7



The binning mode still supports all ROI configurations, although some things have to be taken into account:

- YWINi.SIZE refers to the number of physical rows in the array that are accessed. The number of binned rows at the output is half of this number.
- The XSUBS setting should be increased by 1 compared to the default 12-bit mode. This is not needed for YWINi.SUBS settings.

Information

The maximum data rate of the sensor is limited in low-noise mode. Refer to section 7.4.3, subsection “Set PLL” for more details.

Image Mode Dependent Parameters

A number of timing related parameters are dependent on the selected image mode. The table below details these parameters, for each image mode. Additional information on maximum framerate, minimum and maximum exposure time per image mode is listed in Figure 8.

Figure 61:
Image Mode Dependent Parameters

Image Mode	ROW_LENGTHmin	GLOB_BASE	GLOB_LENGTH	PTR_EXP_0 (no shutter lag)
IMG.1	492	496	90	97
IMG.2	492	496	30	NA
IMG.3	492	96	120	96
IMG.4	492	500	90	97
IMG.5	492	500	30	NA
IMG.7	884	500	86	105

7.4.2 Functional Operation Modes

In addition to the previously defined image mode, implementing an optimized sensor readout performance, the functional behavior of the sensor can be further modified in different operation modes, listed per category in the table below, allowing for a large number of possible combinations.

Figure 62:
Operation Modes

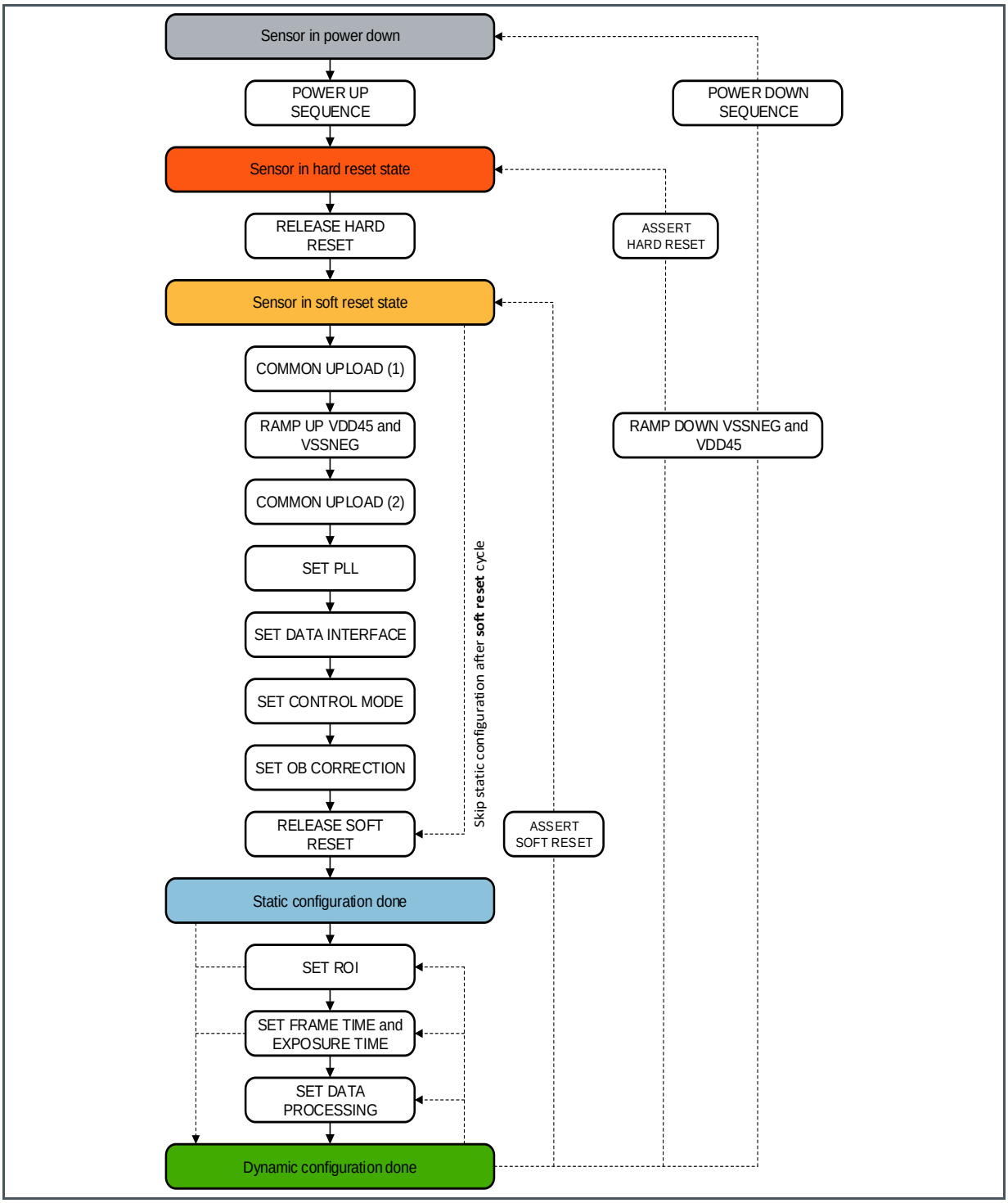
Modes	Description
Data Multiplexing Modes	
MUX.1	Use all 16 output channels (8 per side)
MUX.2	Multiplex image data to 14 output channels (7 per side)
MUX.3	Multiplex image data to 12 output channels (6 per side)
MUX.4	Multiplex image data to 10 output channels (5 per side)
MUX.5	Multiplex image data to 8 output channels (4 per side)
MUX.6	Multiplex image data to 6 output channels (3 per side)
MUX.7	Multiplex image data to 4 output channels (2 per side)

Modes	Description
MUX.8	Multiplex image data to 2 output channels (1 per side)
Sensor Control Modes	
SEN.1	Full External
SEN.2	Programmed External
SEN.3	Triggered Internal
SEN.4	Streaming
OB Clamping Modes	
OBC.1	Optical black clamping ON
OBC.2	Optical black clamping OFF

7.4.3 Flow Chart

Using the flow chart below, all steps necessary to configure or reconfigure the sensor can be determined, as well as their correct and recommended order of execution.

Figure 63 :
Flow Chart



Each step is elaborated in the next sections as a small recipe or procedure to follow. Where applicable, a reference to additional background information will be provided.

The configuration is split in a static and a dynamic part. The static part must be executed once after every power-up or upon a static mode change. The dynamic part must be executed at least once after every power-up and is grouped in a context to allow changing the operation mode on the fly, as detailed in section 7.2.5. Subsequent steps cannot be skipped, e.g. GAIN mode can be changed without changing IMG mode, but not the other way around.

Information

Useful are the optional paths to return to either the soft or hard reset state, which can be taken to temporarily put the sensor in a lower consumption state without having to do a full power cycle.

Attention

Not following these recommendations can lead to the sensor being in an unknown state with unpredictable behavior.

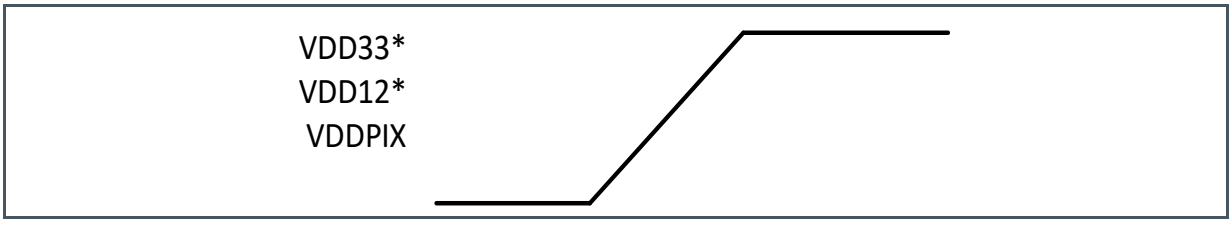
Attention

A specific order and timing must be applied to the sensor supplies to guarantee a proper power-up sequence and to avoid peak currents.

The overall power-up and reset release sequence is described in section 7.2.2. The sections below describe in more detail the exact parts of that sequence.

Power-Up Sequence

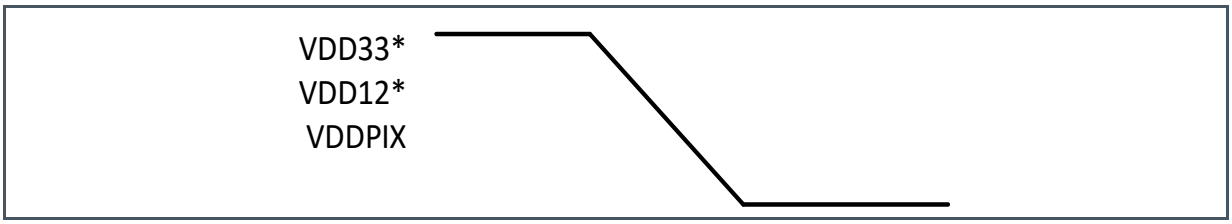
Figure 64:
Power-Up Sequence



All external supplies start at 0 V and must ramp to their respective values as specified in chapter 5 and section 7.2.1, respecting the order and the timing as shown in the figure. Supplies that are shown to be ramping at the same time may also be ramped up one by one.

Power-Down Sequence

Figure 65:
Power-Down Sequence



All external supplies ramp back down to 0 V. Supplies that are shown to be ramping at the same time may also be ramped down one by one.

Release Hard Reset

This is achieved by changing the RST_N input from ‘0’ to ‘1’.

Assert Hard Reset

This is achieved by changing the RST_N input from ‘1’ to ‘0’.

Common Upload (1)

Independent of the sensor operation mode, a group of settings referred to as the Common Upload (1) must be uploaded in the specified order. These settings are provided in a separate file called *CSG14K_common_upload_1.txt*, where every line of that file corresponds to a single 8-bit SPI transaction or a wait statement. The syntax for these commands is detailed below.

```
Write DATA to ADDRESS
```

Lines starting with the **write** keyword indicate SPI write transactions where DATA specifies the value to be written to ADDRESS.

```
Read EXPECTED from ADDRESS
```

Lines starting with the **read** keyword indicate SPI read transactions where EXPECTED is the value that should be read from ADDRESS.

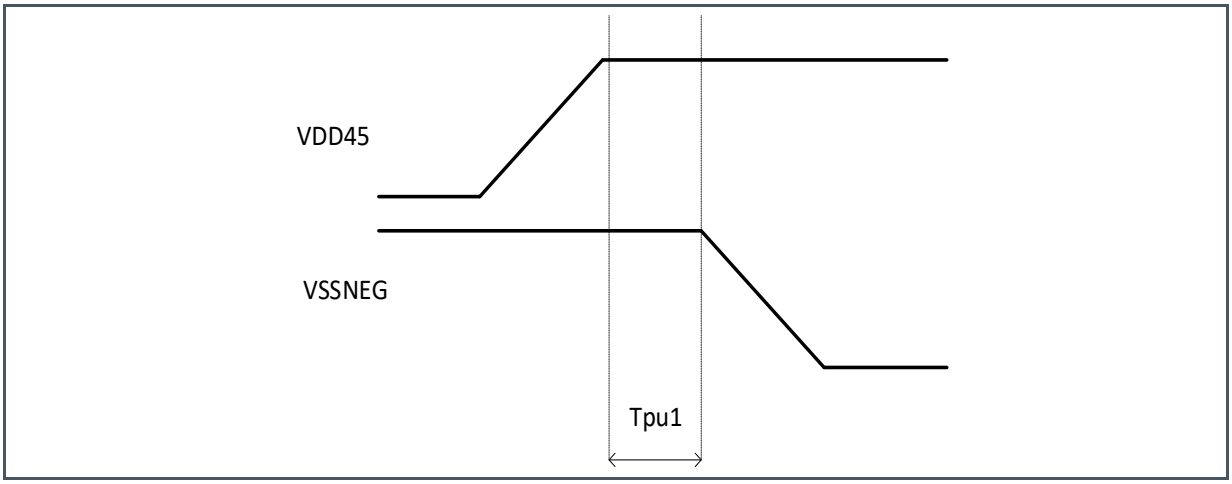
```
Wait TIME
```

Lines starting with the **wait** keyword indicate that a minimum time as specified by TIME has to be respected before moving on to the next instruction. These wait times are necessary for proper settling in the sensor.

Ramp-Up VDD45 and VSSNEG

Both VDD45 and VSSNEG must start at 0 V and ramp to their values as specified in chapter 5 and section 7.2.1, respecting the order and the timing described in the figure below.

Figure 66:
Ramp-Up VDD45 and VSSNEG



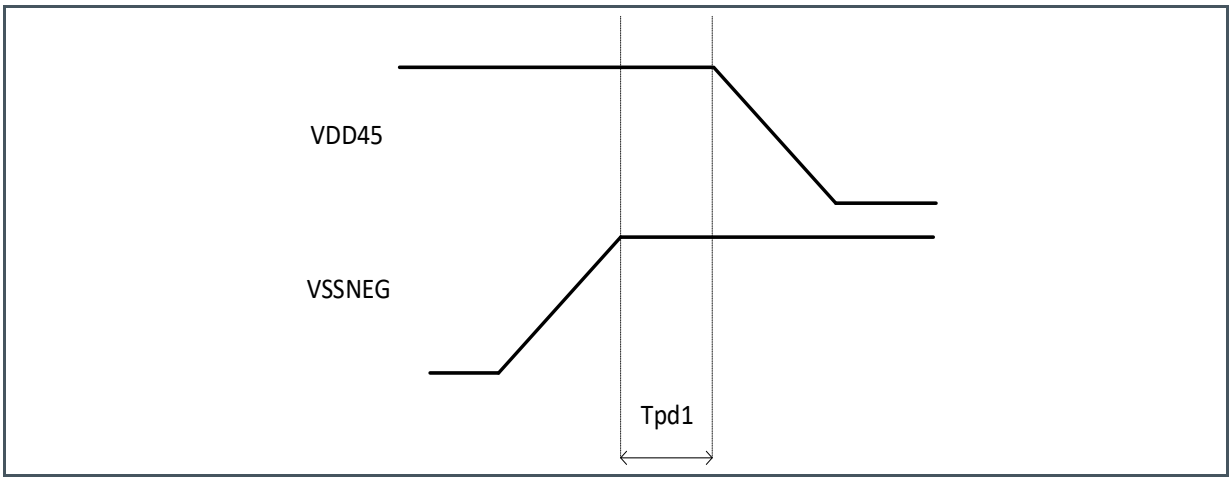
Ramp-Down VSSNEG and VDD45

Attention

A specific order and timing must be applied to these sensor supplies also when ramping down.

To put the sensor back into hard reset state, VDD45 and VSSNEG must be ramped back to 0 V, respecting the order and the timing described in the figure below.

Figure 67:
Power-Down and Ramp-Down Sequences



Common Upload (2)

Dependent on the static sensor operation mode, a certain group of settings referred to as the Common Upload (2) must be uploaded in the specified order. In contrast to Common Upload (1), these settings depend on the user's choice of static sensor operation mode. Switching between static operation modes requires a complete new Common Upload (2). The commands found in Common Upload (2) are similar to Common Upload (1) and follow the same rules.

Figure 68 gives an overview of which file to use as Common Upload (2) for all sensor operating modes.

Figure 68:
Common Upload (2) for Sensor Operating Modes

Operating Mode	Common Upload (2)
IMG.1: 10-bit	CSG14K_common_upload_2_10bit.txt
IMG.2: 10-bit Short Exposure	CSG14K_common_upload_2_10bit_short_exp.txt
IMG.3: 10-bit Small Window	CSG14K_common_upload_2_10bit_small_win.txt
IMG.4: 12-bit	CSG14K_common_upload_2_12bit.txt
IMG.5: 12-bit Short Exposure	CSG14K_common_upload_2_12bit_short_exp.txt
IMG.7: 12-bit Binning	CSG14K_common_upload_2_12bit_binning.txt

In addition to the Common Upload sequence, an additional SPI write is required to indicate if the sensor has a monochrome pixel array, or includes the Bayer RGB color pattern. Configure the sensor according to Figure 69. Besides the COLOR_MODE, also 2 additional registers need to be set when using a color sensor in binning mode. Make sure not to overwrite other bits of register 118.

Figure 69:
Color Mode

Register Name	Bank	Address	Bits	Description
COLOR_MODE	4	4	[0]	0: Mono 1: Color
-	1	118	[10:7]	5: Mono (default) 3: Color
-	1	118	[19:16]	5: Mono (default) 3: Color

Set PLL

Starting from the input clock frequency and the targeted output data rate, 4 parameters must be calculated to correctly configure the PLL. Then the PLL must be configured using the upload sequence below.

Figure 70:
PLL Configuration Sequence

#	Register	Bank	Address	Value
1	PLL_DIV	0	78	See calculation below
2	PLL_WRAP_ADC_DIV	0	86	See calculation below
3	PLL_WRAP_MAIN_DIV	0	87	See calculation below
4	PLL_RST_N	0	80	1
5	Wait at least 10 µs			
6	PLL_PD_N	0	77	1
7	Wait for PLL lock status (see procedure below)			
8	RG_CTRL	1	115	See calculation below
9	PLL_WRAP_RST_N	0	88	1

The parameter PLL_DIV depends on the targeted output data rate and the input clock frequency (between 12 MHz and 20 MHz) as shown in the equation below.

Equation 1:

$$PLL\_DIV = floor\left(\frac{data\_rate\ [Mbps] \cdot 2^{PLL\_WRAP\_MAIN\_DIV}}{f_{clk\_in}[MHz]}\right)$$

Where PLL_WRAP_MAIN_DIV is derived from the targeted output data rate as shown in the tables below.

Figure 71:
PLL_MULT, PLL_WRAP_MAIN_DIV, PLL_WRAP_ADC_DIV and RG_CTRL Calculation

Target Output Data Rate	PLL_WRAP_MAIN_DIV	PLL_WRAP_ADC_DIV	RG_CTRL
250 – 375 Mbit/s	IMG.1-5,7: 3	IMG.1-3: 3 IMG.4-5: 2 IMG.7: 3	IMG.1-3: 1 IMG.4-5: 11 IMG.7: 1
375 – 475 Mbit/s	IMG.1-5,7: 2	IMG.1-3: 2 IMG.4-5: 1 IMG.7: 2	IMG.1-3: 11 IMG.4-5: 21 IMG.7: 11
475 – 750 Mbit/s	IMG.1-5,7: 2	IMG.1-3: 2 IMG.4-5: 1 IMG.7: 2	IMG.1-3: 11 IMG.4-5: 21 IMG.7: 11
750 – 1000 Mbit/s	IMG.1-5,7: 1	IMG.1-3: 1 IMG.4-5: 0 IMG.7: 1	IMG.1-3: 21 IMG.4-5: 31 IMG.7: 21
1000 – 1250 Mbit/s	IMG.1-3,7: 1 IMG.4-5,	IMG.1-3: 1 IMG.4-5: NA IMG.7: 1	IMG.1-3: 21 IMG.4-5: NA IMG.7: 21

The parameters PLL_WRAP_ADC_DIV and RG_CTRL depend on the targeted output data rate as shown in the table above.

The effective data rate is calculated with the following formula:

Equation 2:

$$effective\_data\_rate\ [Mbps] = \frac{f_{clk\_in}[MHz] \cdot PLL\_DIV}{2^{PLL\_WRAP\_MAIN\_DIV}}$$

Note that due to the flooring operation in calculating the parameters, the targeted data cannot be reached exactly for every possible input clock frequency (see example 1 below).

Figure 72:
Calculation Examples

Parameter	Example 1	Example 2
Image mode	IMG.4	IMG.4
f_{clk_in}	12 MHz	12.5 MHz
Targeted data rate	700 Mbit/s	1000 Mbit/s
PLL_WRAP_ADC_DIV	2	1
PLL_WRAP_MAIN_DIV	2	1
PLL_DIV	233	160

Parameter	Example 1	Example 2
RG_CTRL	21	31
Effective data rate(1)	699 Mbit/s	1000 Mbit/s

(1) The effective data rate is equal to the available bandwidth and does not take into account any overhead data.

As described in section 7.2.2, a PLL lock time of maximum 1 ms needs to be respected. The lock status of a PLL can be checked by polling the read-only **PLL_LOCK** register.

The PLL_LOCK registers are only present in the two sequencers. The bottom-side sequencer (with BLOCK_ID 0) holds the lock information of the bottom-side PLL. The top-side sequencer (with BLOCK_ID 1) holds the lock information of the top-side PLL.

Figure 73:
PLL Lock Register

Register Name	Bank	Addr	Read Value
PLL_LOCK	0	85	0: PLL out of lock 1: PLL locked

Set Data Interface

The sensor's pixel data is transmitted over its sub-LVDS output channels. More information on the output interface and low-level timing can be found in section 7.3.Figure 44 shows the required register uploads to set the output format.

Figure 74:
Output Format Registers

Register	Bank	Address	Value
OUTP_FORMAT	0	8	0
PLL_WRAP_MAIN_DIV	0	87	1
CLKGEN_BYTE_H	1	8	2
CLKGEN_BYTE_L	1	9	1

A distinction should be made between the amount of *used* output channels and the amount of *active* output channels. The amount of *used* output channels refers to the amount of channels that is used for full horizontal ROI readout. The amount of *active* output channels refers to the amount of channels that are actively outputting pixel data. Depending on the horizontal ROI settings, the amount of *active* channels is either equal to or less than the amount of *used* output channels. More information on configuring the horizontal ROI can be found in section 7.5.4.

Typically, all of the sensor's output channels are used. The amount of *used* channels may be reduced for the following reasons:

- Power saving. By limiting the number of used output channels, all unused output channels are automatically powered down.
- The receiving system is IO-limited and cannot capture all output channels at once.

The amount of *used* output channels is set with the MAX_NR_OUTP register as shown in Figure 75.

Figure 75:
MAX_NR_OUTP register

MAX_NR_OUTP (bank 0, address 14)	Amount of Used Data Channels
1	1 (per side)
2	2 (per side)
3	3 (per side)
4	4 (per side)
5	5 (per side)
6	6 (per side)
7	7 (per side)
8	8 (per side)

The required power-up sequence of the output drivers is shown in Figure 76.

Figure 76:
Power-Up Sequence of Output Drivers

#	Register	Bank	Address	Value
1	DATA_CH_CTRL	3	74	1026
2	CLK_CH_CTRL	3	78	1026
3	Wait at least 1 ms			
4	DATA_CH_ENA	3	77	1
5	CLK_CH_ENA	3	81	1
6	CLK_CH_EN_DRIVE	3	82	1
7	DATA_CH_EN_DRIVE(1)	4	35	1

(1) This register should be written in both sensor context banks.

Set Row Length

The ROW_LENGTH register sets the line rate of the sensor. The required setting of this parameter is dependent on different sensor operation modes – which are known at this stage of the configuration procedure.

The maximum frame time is achieved when the ROW_LENGTH register is set to its minimal allowed value as per below equation.

Equation 3 – ROW_LENGTH register limitation:

$$\text{ROW\_LENGTH} \geq \max(ROW\_LENGTHmin, KSIZE + 12)$$

Where KSIZE refers to the register value and ROW_LENGTHmin is image mode dependent (see Figure 61).

Refer to section 7.5.2 for further details on this register.

Set Control Mode

Depending on the selected sensor control mode (see 7.4.2), the following SPI register settings must be written. Refer to section 7.2.7 for a detailed description of the control modes.

Figure 77:
Control Mode Register

Register	Bank	Address	SEN.1	SEN.2	SEN.3	SEN.4
CTRL_MODE	0	11	0	1	2	3

SEN.1 (Full External) provides maximal freedom to the user as all exposure and frame control is external to the sensor. It is also the most complex mode, as the user is responsible for generating correct timing of the request pulses (REQ_EXP and REQ_FRAME). The other control modes each add a little intelligence to the sensor, making it easier for the user to control the frame acquisition.

When choosing the sensor control mode, it is important to consider the latency between the external REQ_EXP request and the start of the first exposure on the image array. The SEN.2, SEN.3 and SEN.4 control modes all have an additional latency of 1 Time Unit. The SEN.1 control mode does not have this additional latency.

Release Soft Reset

Once the PLLs are locked, the sensor can be released from soft reset and the main clock can be enabled, by applying the following register write sequence.

Figure 78:
Release Soft Reset Sequence

#	Register	Bank	Address	Value
1	CMD_REGS	0	6	1
2	EN_CLK_MAIN	0	90	1
3	-	-	1	1

#	Register	Bank	Address	Value
4	-	3	96	241
5	-	-	1	0
6	-	3	96	243
7	EN_ADC_RST_N	1	101	1
8	EN_CLK_ADC	1	100	1

Assert Soft Reset

To return the sensor to the soft reset state, the following register uploads need to be applied.

Figure 79:
Assert Soft Reset Sequence

#	Register	Bank	Address	Value
1	CMD_REGS	0	6	0
2	EN_CLK_MAIN	0	90	0
3	-	-	1	1
4	-	3	96	240
5	-	-	1	0
6	-	3	96	240
7	EN_ADC_RST_N	1	101	0
8	EN_CLK_ADC	1	100	0

Asserting the soft reset does not affect the PLL. However, internal clock generation and distribution are disabled when the soft reset is asserted. The soft reset has to be released again before any frames can be grabbed.

Attention

Asserting the soft reset stops the output drivers. Any phase alignment done by the external system is lost and should be redone when the soft reset is released.

Set ROI

Refer to section 7.5.3 for details on configuring the vertical ROI. Refer to section 7.5.4 for details on configuring the horizontal ROI.

In case of operation in IMG.3 (10-bit small window mode), the following sequence of SPI writes is required for correct sensor configuration.

Figure 80:
Additional Configuration Sequence in Case of IMG.3

#	Register	Bank	Address	Value
1	BLOCK_ID	-	1	255
2	-	3	65	1
3	-	0	98	2
4	-	0	96	111
5	-	0	97	6
6	-	0	98	3
7	-	0	98	7
8	-	0	98	3
9	-	0	96	15
10	-	0	97	8
11	-	0	98	2
12	-	0	98	6
13	-	0	98	2
14	-	3	65	0

Set Frame Time and Exposure Time

Refer to section 7.5.1.

Set Data Processing

Next table lists the required uploads per available OB clamping mode. Refer to section 7.7.1 for details.

Figure 81:
OB Bypass Registers

Register	Bank	Address	OBC.1	OBC.2
EOB_BYPASS	0	93	0	1
EOB_BYPASS_VALUE	0	94	N/A	Value from Section 7.7.1

Refer to section 7.7.

7.5 Configuring Readout and Exposure

7.5.1 Frame Time and Exposure Time

Figure 82:
Frame and Exposure Time Registers

Reg. Name	Bank	Addr	Bits	Description
CTRL_MODE	0	11	[2:0]	Sets the sensor control mode
TIME_UNIT	4	5-6	[13:0]	Unit for frame, glob and exposure time
MIN_FRAME_TIME	4	8-9	[15:0]	Sets the minimal frame time in TIME_UNITs
EXP_TIME_L	4	14-15	[15:0]	Sets the exposure time in TIME_UNITs
GLOB_TIME	4	10	[15:0]	See Equation 5 below
GRAN_TG	3	7	[7:0]	Scale factor dependent on the CLK_PIX period

The table below briefly recaps the exposure and frame time configurability in the various sensor control modes (see section 7.2.7).

Figure 83:
Sensor Control Modes

CTRL_MODE	Mode	Frame Time	Exposure Time
0	Full External	Via external timing	Via external timing
1	Programmed External	Via external timing	Via registers
2	Triggered Internal	Via registers	Via registers
3	Streaming Internal	Via registers	Via registers

Both Frame time and Exposure time are specified via registers in number of Time Units (TU). The length of a Time Unit (TU) is itself register-programmable in 'number of CLK_PIX cycles'.

The period of CLK_PIX (t_{CLK_PIX}) depends on the output data width as shown in the table below. The effective data rate (EDR) is set by configuring the PLL (see section 7.4.3).

Figure 84:
CLK_PIX Period [ns] for Different Data Width Modes

Parameter	IMG.1-3 10-bit	IMG.4,5,7 12-bit
t_{CLK_PIX} [ns]	10/EDR [Gbit/s]	12/EDR [Gbit/s]

Register GRAN_TG needs to be scaled with the CLK_PIX period that is used, according to Equation 4. Parameter GLOB_BASE is image mode dependent (see Figure 61).

Equation 4:

$$GRAN\_TG = floor\left(\frac{GLOB\_BASE}{T_{CLK\_PIX}[ns]}\right)$$

Setting register **TIME_UNIT** to f_{CLK_PIX} [MHz] results in usage of an internal time unit of approximately 1 µs. The (minimal) frame time and exposure time, as set with the **MIN_FRAME_TIME** and **EXP_TIME_*** registers now represent multiples of ~1 µs.

In case of image mode IMG.4 at nominal data rate, the CLK_PIX frequency is 83.33 MHz (=1000 MHz / 12). In case register TIME_UNIT is set to 83, this results in a time unit (TU) of 0.996 µs (=83 / 83.33 MHz). Reducing the nominal data rate in this mode slightly to 996 Mbit/s yields a time unit of exactly 1 µs. Similarly (also valid in image mode IMG.4 at nominal data rate), the table below shows the resulting frame and exposure time in case of a time unit of ~2.5 µs.

Figure 85:
Example: Relationship Between Exposure and Frame Time to Time Unit in IMG.4.

Register	Default Setting	Equation	Effective
TIME_UNIT	208	208 / f_{CLK_PIX} [MHz]	2.496 µs
MIN_FRAME_TIME	5000	5000 TU	12.84 ms (~100 fps)
EXP_TIME_L	1000	1000 TU	2.496 ms

Frame and exposure time registers are both 16-bit wide, which means that the exposure time can be specified with a resolution of up to 1/65536 with respect to the frame time.

MIN_FRAME_TIME defines the minimal frame time, in case the minimal frame period is constrained by the readout, rather than the exposure. The actual frame time is adjusted automatically by the sensor for longer exposure times, as soon as the exposure time becomes dominant over the readout time. For the sensor to detect this condition, it needs to be aware of the duration of the global sampling state (GLOB, refer to Basic Frame Timing in 7.2.6). This is done using the register GLOB_TIME, expressed in TU. Register GLOB_TIME needs to be set according to the equation below, which depends on the previously set register GRAN_TG and image mode dependent parameter GLOB_LENGTH (see Figure 61).

Equation 5:

$$\mathrm{GLOB\_TIME} = \mathrm{ceil}\left(\mathrm{GLOB\_LENGTH} * \frac{GRAN\_TG}{TIME\_UNIT}\right)$$

Attention

Because the constant global sampling time is expressed in relative time units (TU), whenever TIME_UNIT is changed, GLOB_TIME must be adapted accordingly (inverse proportional).

Dual Exposure HDR

Figure 86:
HDR Registers

Reg. Name	Bank	Addr	Bits	Description
DUAL_EXPOSURE	4	12	[0]	0: Dual Exposure off 1: Dual exposure on
DUAL_EXP_GROUPING	4	13	[0]	0: Default grouping (mono) 1: Paired grouping (color mode)
EXP_TIME_L	4	14-15	[15:0]	Exposure Time of group L
EXP_TIME_S	4	16-17	[15:0]	Exposure Time of group S

In dual exposure mode, one image can have 2 different exposure times, divided in 2 row groups. In the camera system, this image can be translated into an HDR image containing both details in dark and bright areas.

In the effective pixel array, the pixels are split into two exposure groups. When **DUAL_EXP_GROUPING** is set low:

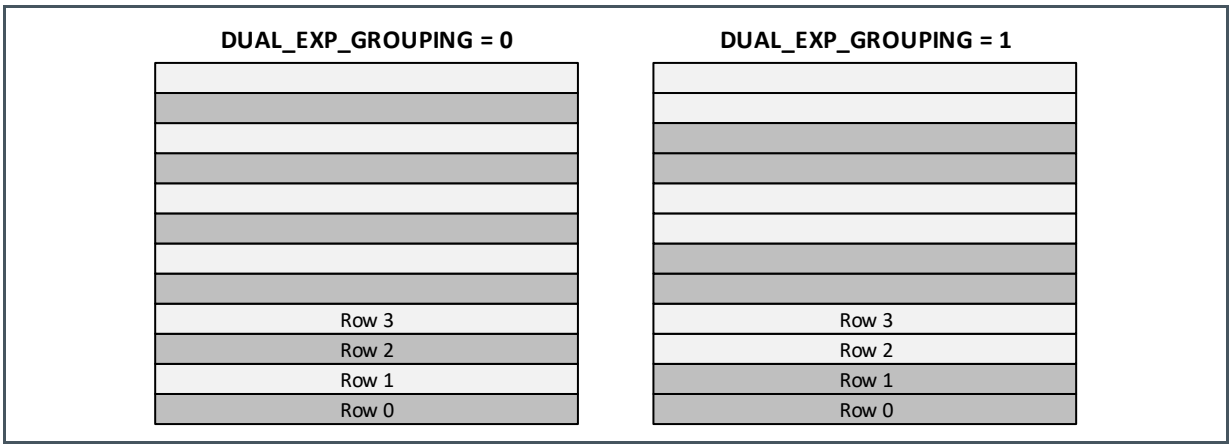
- **Exposure group S**: all pixels of rows 0+4i and 2+4i
- **Exposure group L**: all pixels of rows 1+4i and 3+4i

When **DUAL_EXP_GROUPING** is set high, the exposure groups use adjacent row pairs:

- **Exposure group S**: all pixels of rows 0+4i and 1+4i
- **Exposure group L**: all pixels of rows 2+4i and 3+4i

The latter should be used in color mode, keeping the Bayer pattern complete. Figure 87 shows how the rows of the pixel array are divided into two exposure groups.

Figure 87:
Dual Exposure Grouping



When **DUAL_EXPOSURE** is set low, the exposure time of all pixels is set with **EXP_TIME_L**. When the register is set high, the exposure time of the two groups can be set independently with **EXP_TIME_S** and **EXP_TIME_L**.

Despite the naming of the L(ong) and S(hort) groups, it is allowed to have a shorter exposure time for the L group than for the S group.

Dual exposure mode is also supported in *Full External* control mode. In this control mode, the rising edge of REQ_EXP starts the exposure of the L group and the falling edge of REQ_EXP starts the exposure of S. This behavior is illustrated in Figure 55. If **DUAL_EXPOSURE** is low, both groups are started with the rising edge of REQ_EXP.

Minimal Frame Time Constraint

The frame time has a minimum value requirement to guarantee the entire frame readout and exposure is completed successfully before a new frame starts. This minimum requirement is captured in the equation:

Equation 6:

$$t_{frame} > t_{\text{glob}} + t_{read} \qquad with: t_{read} = t_{row} \cdot (N_{fval} + N_{dummy} + N_{stats})$$

The components of this equation are:

Figure 88:
Minimal Frame Time Dependencies

Component	Description	Equation
t_{frame}	Target Frame time (= 1 / max frame rate)	**FRAME_TIME** · TU
t_{glob}	Length GLOB state	**GLOB_TIME** · TU

Component	Description	Equation
t_{row}	Row length	**ROW_LENGTH** · t_{CLK_PIX}
N_{fval}	Number of valid rows in frame	sum(**YWIN**$_{enabled}$.**SIZE**)
N_{dummy}	Number of dummy rows in frame	IMG.3: 3 Others: 7
N_{stats}	Number of image statistics rows in frame	**STAT_NROF_HIST**

TU is time unit expressed in seconds, not to be confused with contents of register TIME_UNIT. The t_{read} component corresponds to the length of the READOUT state used in section 7.2.6.

In the external control modes, the same frame time equation should be respected to not interrupt the readout of active frames.

The N_{dummy} component represents a number of dummy rows read out between the GLOB and READOUT phase. Depending on the configuration used, this number varies between 3 and 7.

Attention

If the above equation is not respected, the sensor behavior is undefined and no warning or error message is generated. It is the responsibility of the external controller to apply compliant register settings.

The equation above specifies a minimum frame time. The maximum frame time is only constrained by the limits of the relevant registers.

Attention

The sensor has an absolute minimal exposure time, which is image mode dependent (see parameter $t_{exp,min}$ in Figure 8 for applicable value).

Maximum Frame Rate Calculation

The maximum frame rate in any user configuration can be calculated with the formula below. Refer to the previous section for the registers and formulas for the constituting times. The maximum frame rate per image mode provided in Figure 8.

Equation 7:

$$Frame\ rate = \frac{1}{Frame\ Time} = \frac{1}{t_{glob} + t_{read}}$$

Sequence Length

Figure 89:
Number of Frames Register

Register Name	Bank	Addr	Bits	Description
NROF_FRAMES	4	7	[7:0]	See below

In triggered internal mode (**CTRL_MODE** = 2), every rising edge on REQ_EXP (through external pin or register) will initiate the capture of a sequence of frames. The value in the **NROF_FRAMES** register at the moment of the rising edge on REQ_EXP will determine the sequence length.

NROF_FRAMES may be set to any value between 1 and 255. In all other control modes, the register is ignored.

When a sequence is still active, a new rising edge on REQ_EXP will increment the remaining number of frames by the value set in **NROF_FRAMES**. The total number of remaining frames may not be higher than 255.

Shutter Lag

Figure 90:
Shutter Lag Register

Register Name	Bank	Addr	Bits	Description
SHUTTER_LAG	1	32	[15:0]	See description below
PTR_EXP_0	1	112	[6:0]	Set differently depending on whether the matching of the shutter lag is enabled or disabled

Following the default configuration (see Figure 61); the shutter lag functionality is enabled, resulting in a shutter lag delay equal to the equation below.

Equation 8:

$$T_{shutter\_lag} = T_{exp,min} + 32 * T_{CLK\_PIX}$$

The shutter lag matching can also be disabled:

1. Set the PTR_EXP_0 register to the image mode dependent value (see Figure 61)
2. Set the SHUTTER_LAG register to 0.

In this case, the shutter lag time becomes:

Equation 9:

$$t_{shutter\_lag} = 32 * T_{CLK\_PIX}$$

Disabling shutter lag is not possible in the 10-bit short exposure more (IMG.2) and the 12-bit short exposure mode (IMG.5).

7.5.2 Row Length

Figure 91:
Row Length Register

Register Name	Bank	Addr	Bits	Description
ROW_LENGTH	4	18-19	[13:0]	See below

The row length t_{row} defines the DVAL frequency during readout; it can be programmed in number of CLK_PIX cycles with the **ROW_LENGTH** register.

The row length has a minimum value because a number of parallel processes in the sensor need to be completed within one row time. The minimal row length depends on the number of outputs used (see equations in section 7.4.3).

The maximal row length value is only constrained by the 14 bits size of register.

Fine frame rate adjustments are done through external timing or with the **FRAME_TIME** register. Changing the row length only influences the DVAL frequency within a readout sequence. This can be useful when smaller or slower row buffers are used in the external system.

An exception to this rule is the in-line streaming mode, where the **ROW_LENGTH** register does directly alter the frame rate.

7.5.3 Vertical Windowing

The sensor supports multiple windows in the vertical direction to create regions of interest (ROI).

Row Addressing

As introduced in section 7.1.1, the sensor has buffer pixels rows above and below the effective pixels.

Every row in the array is paired with a physical row address. This row address is used to specify vertical ROI positions as described in next section.

Row addresses are assigned in ascending order starting from 0 for the row closest to the package pin row 1.

Figure 92:
Valid Row Addresses

Region	Row Address Range (14 K)	Row Address Range (8 K)
Active pixels	60 … 3659	772 … 2947
Recommended pixels	68 … 3651	780 … 2939
Bottom buffer pixels	0 … 59	0 … 59
Top buffer pixels	3660 … 3719	3660 … 3719

ROI Settings

The sensor allows up to 10 vertical windows to be concatenated in one single frame readout.

Each of these windows is enabled by setting their bit in **YWIN_ENA** to '1' (bit [0] = **YWIN0**, [1] = **YWIN1** …).

Each of these windows is configured with an **YWINi** register that defines the position, size and sub-sampling of the window. The 31 bits of each YWINi register span 4 physical SPI addresses. In the table below, only the start address is given (the upper address being 21+4×i).

The readout direction of all windows can be changed from the default incrementing addresses (bottom to top) to decrementing addresses (top to bottom) with the **YWIN_DIR** register. Using a different setting for this register on both sides of the readout allows for reading out from center to edge or vice versa.

Figure 93:
Vertical Windows Registers

Register Name	Bank	Addr	Bits	Description
YWIN_ENA	4	28-29	[9:0]	One bit per window 0: Disable 1: Enable
YWIN_BLACK	0	15	[9:0]	One bit per window to control the 'Electrical Black' mode 0: Disable 1: Enable
YWIN_DIR	0	17	[0:0]	Direction of readout addresses 0: Count upwards 1: Count downwards
YWINi.SIZE	0	18+4×i	[13:0]	Number of read out rows in window i
YWINi.START	0	18+4×i	[27:14]	Physical address of first row in window i
YWINi.SUBS	0	18+4×i	[30:28]	Row subsampling in window i Ratio = $1/(2^{SUBS})$

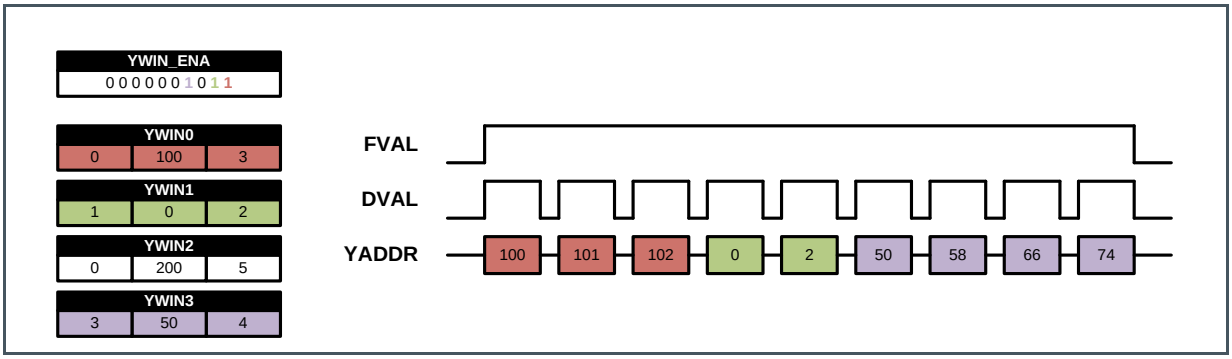
The **START** address of a window should comply with the values in Figure 92.

Only windows for which the respective bit in **YWIN_ENA** is set high are actually read out. This way multiple relevant Y-window specifications can be stored in the register map at the same time, enabling only the relevant ones.

All enabled windows are concatenated together (the first row of a new window is read immediately after the last row of the previous). The number of rows actually read in one frame (= # of DVAL within one FVAL) is the sum of the SIZE fields of all windows enabled by **YWIN_ENA**.

The figure below shows an example of using multiple windows.

Figure 94:
Vertical ROI Example (monochrome)



Attention

Because the readout is dual-sided (top/bottom), the sensor top sequencer must be programmed to only access rows in the upper half of the array (1860 to 3719) and the bottom sequencer to only access rows in the lower half of the array (0 to 1859).

Small Window Mode

When reading out small windows, the unused rows are disabled to decrease the global sampling time and finally increase the frame rate. For more details, refer to section 7.4.1.

Electrical Black Windows

With the **YWIN_BLACK** register, windows can be made 'electrical black' (setting a fixed voltage at the read out path instead of the pixel voltage). If the respective bit of the YWIN_BLACK register is set high (same mapping as YWIN_ENA), then all signal information in the window is suppressed. This results in a black window containing only readout FPN information. This feature could be used for column FPN correction.

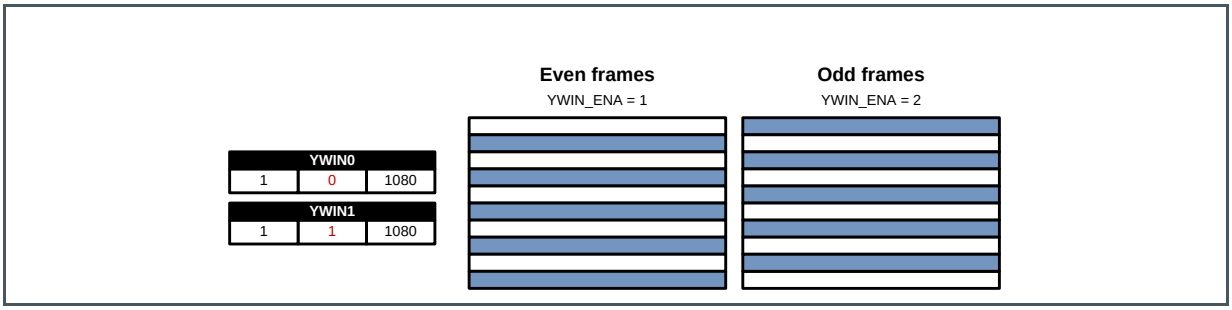
Window Overlap

Several vertical windows may overlap, although this is only useful in subsampling mode. If the same row is read multiple times within one frame, it will only contain valid data the first time (destructive read out).

One possibility is to create an interleaved readout scheme by:

1. Defining two vertical windows with identical size and SUBS set to 1
2. Giving START of the second window an offset so it starts at a row skipped by the sub sampling scheme of the first window
3. Alternating the respective YWIN_ENA bits between every frame.

Figure 95:
Interleaved Readout



7.5.4 Horizontal Windowing

Figure 96:
Horizontal ROI Registers

Register Name	Bank	Addr	Bits	Description
XSTART	4	20-21	[13:0]	Start column of horizontal ROI
KSIZE	4	23-24	[13:0]	Number of columns read per DATAx_OUT channel.
NR_OUTP	4	27	[3:0]	Number of DATAx_OUT channels to be used (per side)
XSUBS	4	22	[1:0]	Horizontal subsampling setting

The sensor supports reading out any horizontal region of interest starting at column **XSTART** and a width of **KSIZE**×**NR_OUTP**×$2^{\mathbf{XSUBS}}$, as long as the following constraints are honored.

Equation 10:

$$1 \leq NR\_OUTP \leq MAX\_NR\_OUTP$$

Equation 11:

$$XSTART + (NR\_OUTP \times KSIZE \times 2^{XSUBS}) < 3870$$

Equation 12:

$$KSIZE \times 2^{XSUBS} \geq 480$$

Attention

In binning modes, the XSTART address must be even (mono mode) or a multiple of 4 (color mode).

The horizontal ROI configuration supports output channel multiplexing. This allows a user to read out the same horizontal ROI with a reduced number of output channels. Figure 97 shows the horizontal ROI settings for all multiplexing options using the recommended ROI.

Figure 97:
Output Channel Multiplexing for Recommended ROI

Mode	XSTART	KSIZE	NR_OUTP	XSUBS(2)
MUX.1	8	IMG.1 - 5: 480 IMG.7: 240	8	IMG.1 - 5 : 0 IMG.7: 1
MUX.2(1)	10	IMG.1 - 5 : 548 IMG.7: 274	7	IMG.1 - 5 : 0 IMG.7: 1
MUX.3	8	IMG.1 - 5 : 640 IMG.7: 320	6	IMG.1 - 5 : 0 IMG.7: 1
MUX.4	8	IMG.1 - 5 : 768 IMG.7: 384	5	IMG.1 - 5 : 0 IMG.7: 1
MUX.5	8	IMG.1 - 5 : 960 IMG.7: 480	4	IMG.1 - 5 : 0 IMG.7: 1
MUX.6	8	IMG.1 - 5 : 1280 IMG.7: 640	3	IMG.1 - 5 : 0 IMG.7: 1
MUX.7	8	IMG.1 - 5 : 1920 IMG.7: 960	2	IMG.1 - 5 : 0 IMG.7: 1
MUX.8	8	IMG.1 - 5 : 3840 IMG.7: 1920	1	IMG.1 - 5 : 0 IMG.7: 1

(1) In MUX.2 mode, the full horizontal ROI (3840 columns) is slightly reduced (to 3836 columns) to keep an equal amount of pixels on each data channel. The start column is shifted by two columns to keep the ROI centered (this is optional).

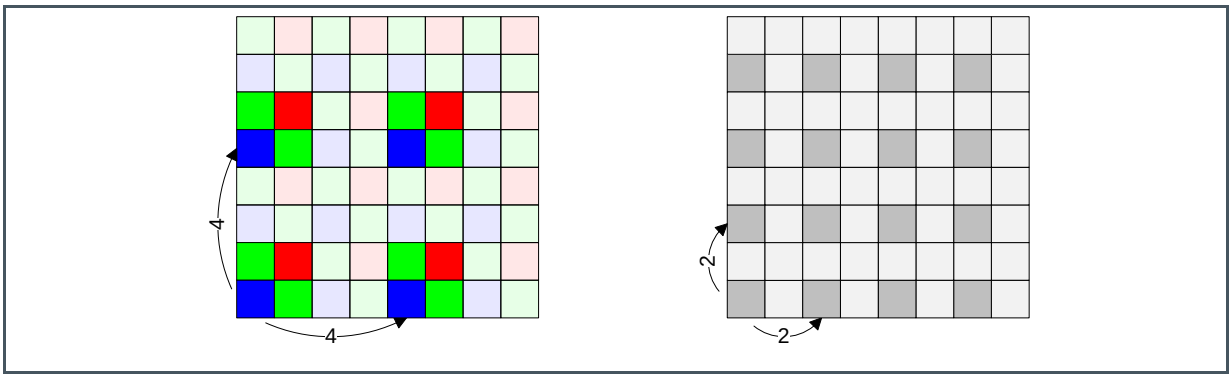
(2) XSUBS is set to 0 in normal operation. When using IMG.7 (binning) mode, add 1 to this value. When using this mode together with subsampling, contact our application engineer.

7.5.5 Subsampling

Mode

Combining both horizontal and vertical subsampling will divide the resolution of the image by 2 in both dimensions as illustrated in Figure 98.

Figure 98:
XY-Subsampling for Color and Mono Sensors



In color mode, only 4 out of 4x4 neighboring pixels are read out. The output data is still Bayer patterned.

In monochrome mode, only 1 out of 2x2 neighboring pixels is read out.

The amount of pixels per channel mentioned in section 7.6.2, scales accordingly when combining horizontal subsampling with the readout over a reduced number of data channels.

Vertical Subsampling

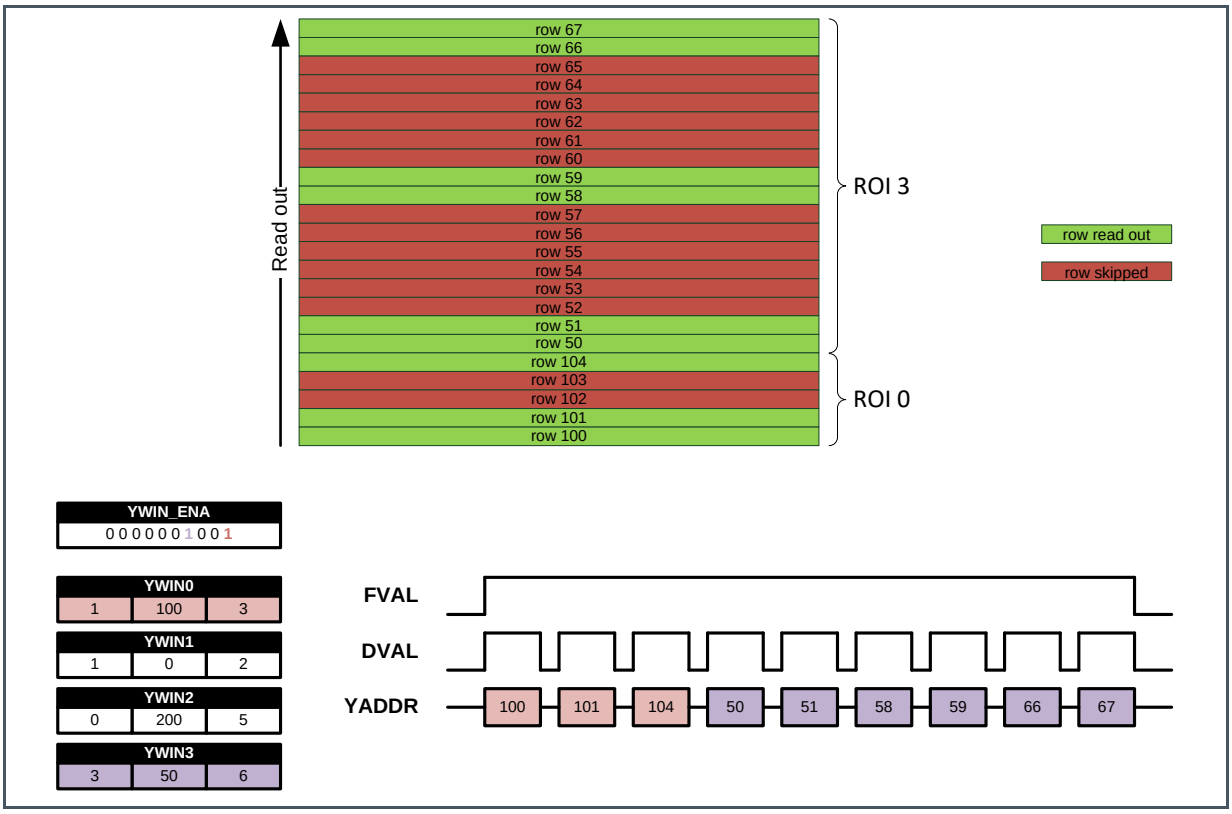
Figure 99:
Vertical Subsampling Registers

Register Name	Bank	Addr	Bits	Description
YWINi.SUBS	0	18+4×i	[30:28]	Row subsampling in window i
COLOR_MODE	4	4	[0]	0: Monochrome 1: Color

The sensor supports vertical subsampling (skipping rows), which can be set per window. The register **YWINi.SUBS** defines the ratio of the accessed rows in window *i* as 1 out of every 2^{SUBS} rows.

When COLOR_MODE register is set to 1, the rows are grouped per 2 to follow the Bayer pattern, as illustrated in Figure 100. It is recommended to only use even window sizes in color mode to keep the Bayer filter pattern intact. ROI0 in the example below demonstrates the effect of an odd window size.

Figure 100:
Vertical ROI Example (color mode)



Horizontal Subsampling

Figure 101:
Horizontal Subsampling Registers

Register Name	Bank	Addr	Bits	Description
XSUBS	4	22	[1:0]	Horizontal subsampling setting Ratio = $1/(2^{XSUBS})$
COLOR_MODE	4	4	[0]	0: Mono 1: Color

The sensor supports horizontal subsampling, reducing the amount of pixels per line to $1:2^{XSUBS}$. This horizontal subsampling is applied to the whole array and not per ROI like vertical subsampling. Depending on COLOR_MODE, pixel grouping is done to preserve the Bayer pattern.

Note: KSIZE should be set according to the formulas in section 7.5.4.

7.6 Configuring the Output Data Format

7.6.1 Word Alignment

Figure 102:
Training Word Register

Reg. Name	Bank	Addr	Bits	Description
TRAINING_WORD	0	73-74	[13:0]	See below. Default value is 85

Whenever a data channel is not sending valid data (*), a training word is being transmitted continuously. The content of the training word can be set with the **TRAINING_WORD** register. When the sensor operates in 12-bit mode, only the lowest 12 bits of the register are sent as training word.

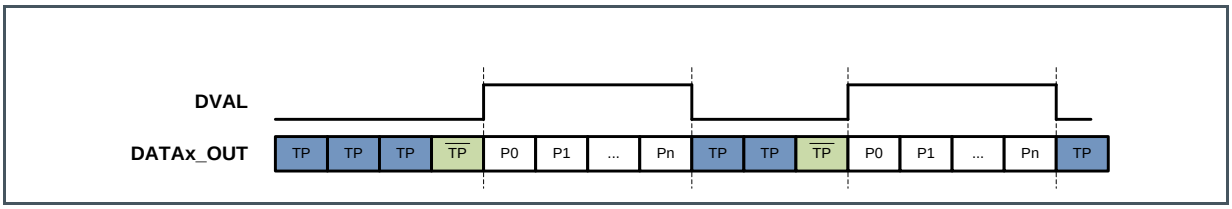
On all DATAx_OUT channels, the last word cycle before DVAL, the training word is inverted. If the overhead time between two DVAL cycles is only 1 word wide, only the inverted training word is sent.

(*) Valid data is:

- **DATAx_OUT:** Valid pixel data (DVAL = '1')
- **OB_OUT:** Valid OB pixel data (OBVAL = '1')

The figure below shows illustrates this timing (drawn in the parallel domain).

Figure 103:
Training Pattern



When the sensor is not transmitting valid data, the training word can be used by the external controller to do word alignment (in other words: finding the position of bit [0]). Detecting the inverted training word will alert the presence of valid pixel data 1 pixel cycle in advance.

When the sensor is IDLE, all control word bits except the LSB (SYNC) are '0'. Detecting the SYNC bit allows for easy word alignment at the receiver side.

7.6.2 Outputs

As illustrated in Figure 51 the sensor has 8 output channels on each side to transfer valid image data. This means that in the fastest configuration, the sensor can output 16 pixels at the same time. As the

maximal valid image width is 3856 columns, a complete row is transferred in 482 word cycles when utilizing all outputs.

Reduced Number of Data Channels

In many applications, it is not mandatory to use all data channels (for example when reading a limited horizontal ROI or when operating the sensor below its nominal frame rate). In these cases, it could be interesting to use less data channels to save power consumption.

The number of DATAx_OUT channels used per side is programmable with the **NR_OUTP** register.

Figure 104:
Number of Outputs Registers

Reg. Name	Bank	Addr	Bits	Description
NR_OUTP	4	27	[3:0]	Number of DATAx_OUT channels to be used (per side)
MAX_NR_OUTP	0	14	[3:0]	Upper limit to number of channels to be used, in case of context switching (per side)
DATA_CH_EN_DRIVE	4	35	[0:0]	'0': Disable channel driver '1': Enable channel driver

The first N channels starting at DATA0_OUT are used (per side).

For example, when setting **NR_OUTP** to 4, DATA0_OUT to DATA3_OUT channels are used on both top and bottom side, totaling 8 outputs. DATA4_OUT to DATA7_OUT are disabled on both sides.

All unused DATAx_OUT channels are automatically disabled, but not necessarily powered-down. To allow on-the-fly context switching to a context with a different setting of NR_OUTP, the register **MAX_NR_OUTP** must be set to the maximum setting of NR_OUTP over the different contexts. MAX_NR_OUTP defines the number of output channels that will be powered-on. Channels above MAX_NR_OUTP are automatically powered-down. Channels between NR_OUTP and MAX_NR_OUTP must be individually powered-down using DATA_CH_EN_DRIVE.

The number of columns read on every output or kernel size is defined by these registers.

Figure 105:
Kernel Size Registers

Reg. Name	Bank	Addr	Bits	Description
KSIZE	4	23-24	[13:0]	Number of columns read per output

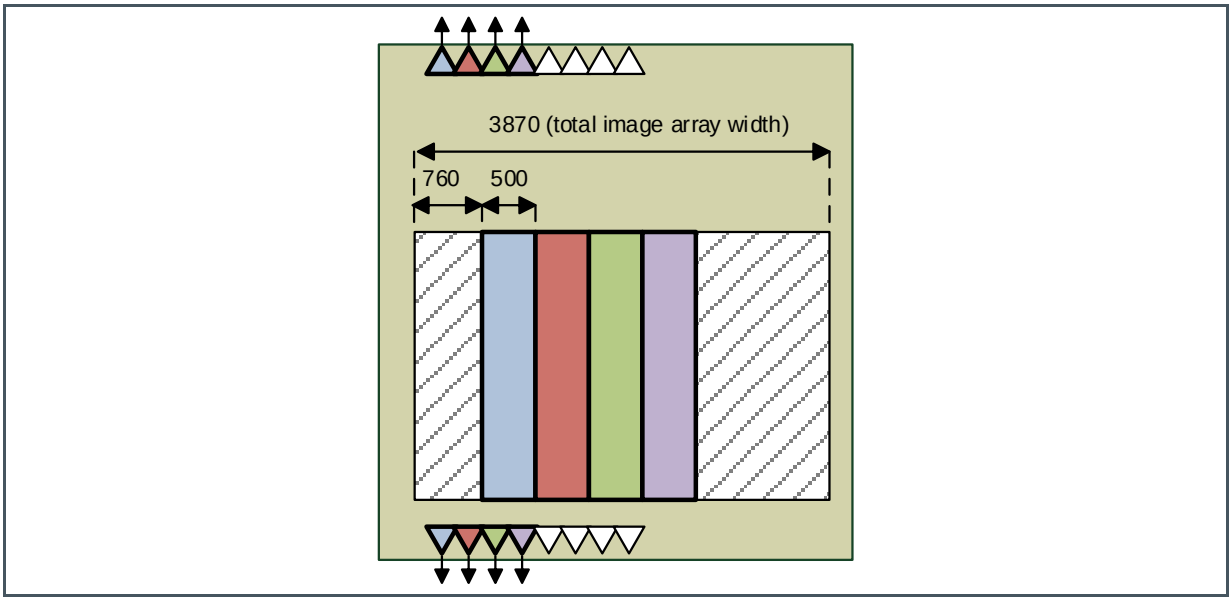
Every channel sends an equal amount of pixels per row defined by **KSIZE**. The last (or rightmost) channel of the used DATAx_OUT channels pads dummy pixels after the valid pixels when needed.

Attention

The equations introduced in 7.5.4 must be respected.

The figure below shows an example for an ROI of 2000 columns, starting at column 760, read out over 4 outputs per side (XSTART=760, KSIZE=500, NR_OUTP=4).

Figure 106:
Readout of a Horizontal ROI Over 4 Outputs Per Side

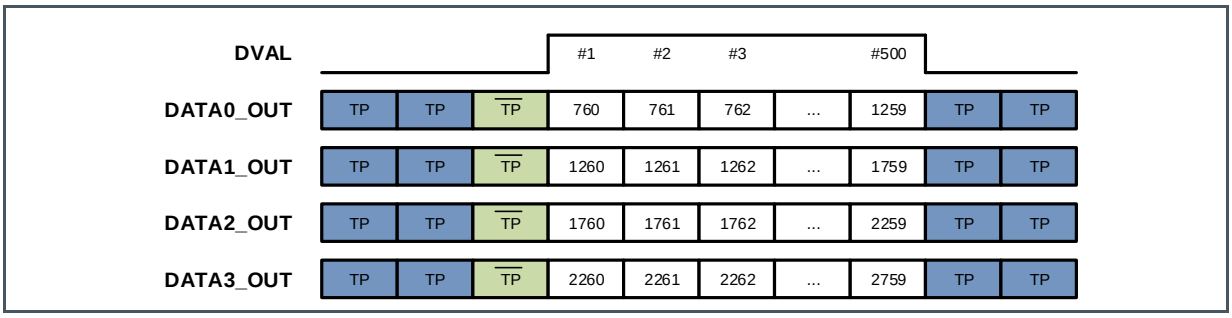


Pixel Order

The selected ROI (or full image width) is divided over 1 or more output channels. On each output, pixels are presented in-order.

The figure below shows the timing of the readout the scenario of Figure 106 (each box represents the physical column address of the pixel).

Figure 107:
Multiplexed Sub-LVDS Timing Example



7.6.3 Pixel Bit Order

Figure 108:
Output Bit Order Register

Reg. Name	Bank	Addr	Bits	Description
OUTP_BITORDER	0	10	[0]	0: Serial data is sent LSB first 1: Serial data is sent MSB first

To accommodate different receiver systems, least or most significant bit of pixel data can be sent first (within the pixel word). This is independent from the chosen output format as it acts on the level of the pixel data.

7.7 Configuring the On-Chip Data Processing

7.7.1 Optical Black Clamping

Figure 109:
Optical Black Registers

Reg. Name	Bank	Addr	Bits	Description
EOB_TARGET	0	58-59	[12:0]	Sets the target black level value in DN
EOB_BYPASS	0	93	[0]	0: OBC on (recommended) 1: OBC off
EOB_BYPASS_VALUE	0	94-95	[12:0]	Sets the ideal black level at the ADC (when OBC off).

This section explains how to set and correct the black levels.

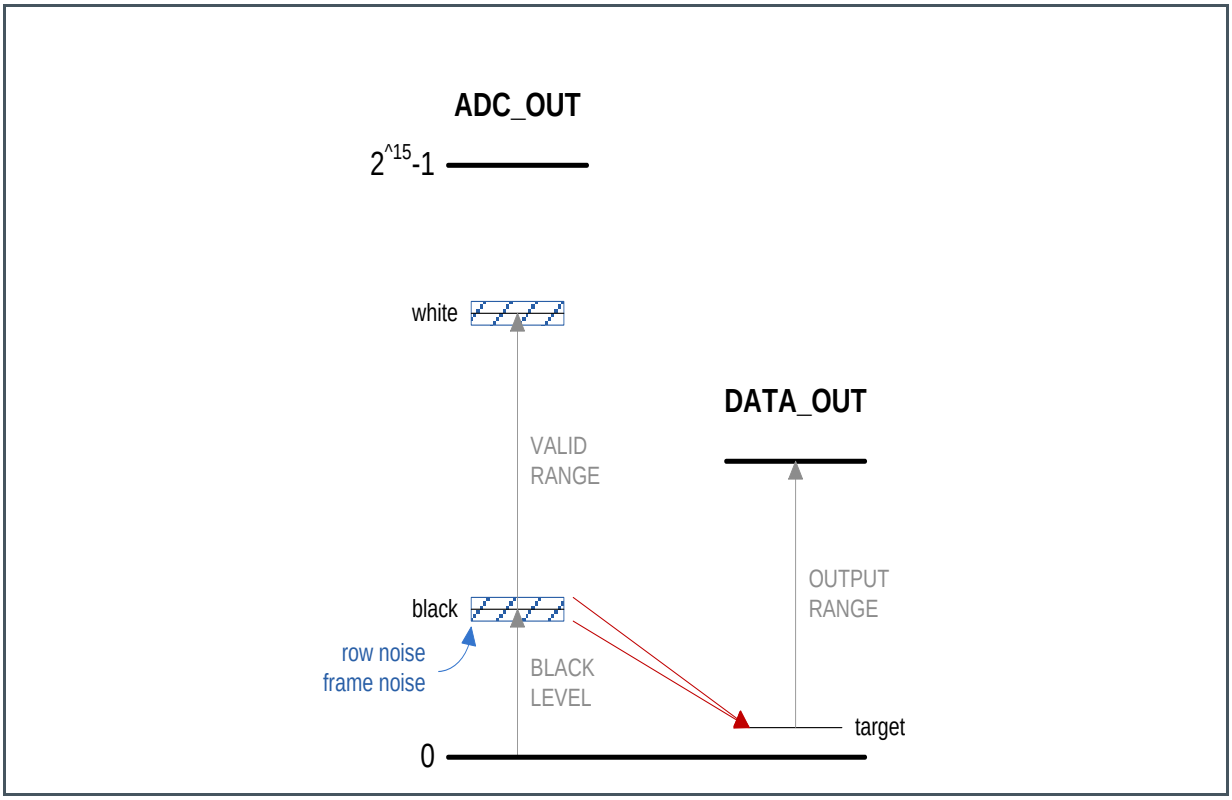
Black Level Mapping

The black level at a certain point in the pixel data path on the sensor is the analog level or digital word that corresponds to the level of an ideal dark pixel (zero illumination). In practice, it is the average of all real dark pixels (optically shielded) at that point in the data path.

The black level at the output of the ADC does not equal the desired black level in the output images for several reasons including the ADC architecture, fixed pattern and temporal noise (row noise, frame noise), dark current and so on.

As illustrated in the figure below, the black level at the ADC output needs to be mapped on the target black level at the sensor output.

Figure 110:
Black Level Mapping



The mapping is done using the equation:

Equation 13:

$$PIX_{DATA\_OUT} = clip[PIX_{ADC\_OUT} - BLACK\_LEVEL_{ADC\_OUT} + BLACK\_LEVEL_{DATA\_OUT}]$$

$BLACK\_LEVEL_{DATA\_OUT}$ is the target black level at the output of the sensor. It is specified with the register **EOB_TARGET**. The recommended minimal setting is 30 (lower settings may decrease the

quality of the resulting image), which means the level at the output for black pixels will be around 30 DN.

$BLACK\_LEVEL_{ADC\_OUT}$ is the black level at the output of the ADC. Its value is set differently depending on how the black level correction is done. This is detailed in the next two sections.

On-Chip OBC

Setting **EOB_BYPASS** to 0 enables the automatic on-chip black level correction (clamping). In this mode, $BLACK\_LEVEL_{ADC\_OUT}$ is calculated on-chip, based on OB pixels, for every row allowing to correct for row and frame noise in the image.

This is the recommended mode of operation.

Off-Chip OBC

Setting **EOB_BYPASS** to 1 disables the automatic OBC. $BLACK\_LEVEL_{ADC\_OUT}$ is now specified with register **EOB_BYPASS_VALUE**. This value is constant and cannot correct for row noise in the image.

Equation 14:

$$PIX_{DATA\_OUT} = clip[PIX_{ADC\_OUT} - EOB\_BYPASS\_VALUE + EOB\_TARGET]$$

The theoretical value for register **EOB_BYPASS_VALUE** is shown in the table below. The parameter t_{CLK_PIX} can be derived from Figure 84.

Figure 111:
Theoretical Values for Register EOB_BYPASS_VALUE

EOB_BYPASS_VALUE
$12.5*t_{CLK\_PIX}$

Further external or off-chip OBC can be achieved by reading out the OB pixel data (refer to section 7.8.7).

7.7.2 Digital Gain

Digital gain can be specified for the 4 color channels individually (even/odd columns, even/odd rows). E.g. GDIG_RE_CO relates to **R**ows **E**ven and **C**olumns **O**dd.

The digital gain for each channel is defined by a similar equation:

Equation 15:

$$Digital\ gain\ (Rx\_Cy) = (GDIG\_Rx\_Cy + 1)/16$$

Base (default) digital gain is set by uploading a value of 15 to **GDIG_Rx_Cy**. The maximum digital gain is 16x with **GDIG_Rx_Cy** at 255. The lowest digital gain is 1/16x with **GDIG_Rx_Cy** at 0.

Figure 112:
Digital Gain Registers

Reg. Name	Bank	Addr	Bits	Description
GDIG_RE_CE	4	30	[7:0]	Even Rows & Even Columns See Equation 15
GDIG_RE_CO	4	31	[7:0]	Even Rows & Odd Columns See Equation 15
GDIG_RO_CE	4	32	[7:0]	Odd Rows & Even Columns See Equation 15
GDIG_RO_CO	4	33	[7:0]	Odd Rows & Odd Columns See Equation 15

The digital gain is applied after the black level correction. This means that changing the digital gain setting does not require any of the offset correction settings to be updated.

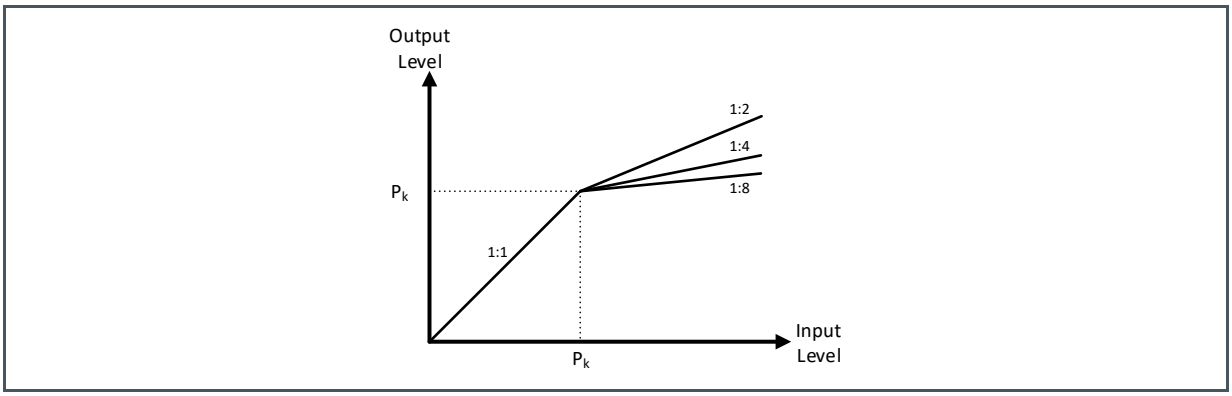
7.7.3 Compression

Figure 113:
Compression Registers

Register Name	Bank	Addr	Bits	Description
COMPRESS_EN	0	65	[0:0]	0: Disable digital compression 1: Enable digital compression
COMPRESS_KNEEPOINT	0	66	[12:0]	Threshold above which data is compressed
COMPRESS_RATIO	0	68	[1:0]	Compression number 0: Ratio 2 1: Ratio 4 2: Ratio 8 3: Ratio 16
OUTP_BITMODE	0	7	[1:0]	Pixel data width of the output channels 0: Unused 1: 10-bit data 2: 12-bit data

The sensor can digitally compress the output pixel data as shown in the figure below.

Figure 114 :
Digital Data Compression



Pixel values below the knee point (P_k) are not compressed (1:1 mapping); pixel values above the knee point are compressed with a ratio of 1 over COMPRESS_RATIO. At the receiver side, the original pixel levels can be reconstructed (except for the LSB bits for pixels above Pk).

After limiting the output level to a lower number of bits that the input level, the framerate can be increased by trimming the width of the output data channels, with OUTP_BITMODE.

Attention

In different scenarios, depending OUTP_BITMODE, other static register uploads are required. Refer to section Set Output Data Width in section 7.4.3 for detailed uploads.

7.8 Additional Features

7.8.1 Image Statistics

Figure 115:
Stat Registers

Register Name	Bank	Addr	Bits	Description
STAT_NROF_HIST	0	70	[2:0]	0: No image statistics are output 1: Send out 1 histogram: all color channels only 2: Send out 2 histograms: all colors + ReCe 3: Send out 3 histograms: all colors + ReCe + ReCo 4: Send out 4 histograms: all colors + ReCe + ReCo + RoCe 5: Send out 5 histograms: all colors + ReCe + ReCo + RoCe + RoCo
STAT_FREQ	0	71	[7:0]	Inverse proportional to the number of pixels used in the statistics gathering. Minimal value is the number of physical output channels per side on the sensor, i.e. 8

To support AWB and/or AEC/AGC algorithms in the camera, the sensor produces a 32-bin histogram for each color channel of the frame that has been sent out. A total histogram (4 color channels combined) is also sent out. The histogram data is gathered from pixels in dual exposure group 'L'.

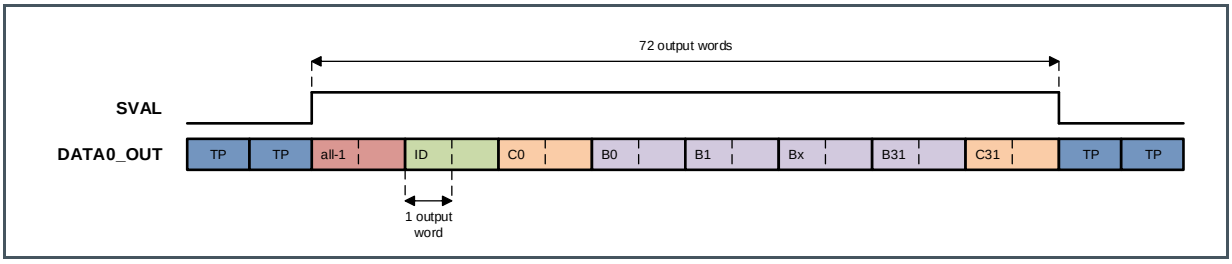
Next to the 32 equally distributed bins, also the number of clipped black and clipped white pixels is sent out.

Note that due to the dual sided readout, 2 image statistics blocks are sent off-chip: one for the top part and one for the bottom part of the sensor. All statistical data need to be combined to get the histograms of the total pixel array.

Image statistics are always transferred over the DATA0_OUT channels, one histogram per row time. Valid image statistics data are indicated by the SVAL bit on the CTR_OUT channel.

The figure below shows the output sequence of a single histogram on a single channel.

Figure 116:
Timing Histogram Data



Every element of the histogram data is split into two consecutive output words (length set by **OUTP_BITMODE**). The LSBs are always placed in the first of these two words of the element. The various elements are listed in the table below.

Figure 117:
Histogram Elements

Element #	Name	Description
0	All-1	Start of sequence marker
1	ID	Histogram ID: 0 = All color channels 1 = Pixels of even rows, even columns 2 = Pixels of even rows, odd columns 3 = Pixels of odd rows, even columns 4 = Pixels of odd rows, odd columns
2	C0	Bin containing the pixels that are 0
3-34	B0-B31	32 equally sized histogram bins spread over the entire output range
35	C31	Bin containing the pixels that have the maximum value in the active bit mode (defined by DPATH_BITMODE)

All pixels in bin C0 are also part of bin B0. In the same way, all pixels in bin C31 are part of bin B31.

Not all pixels are included in the statistics gathering, although the selected pixels are evenly distributed over the image. The spatial distribution is configured by setting **STAT_FREQ**. The best distribution is achieved when it is set to 8.

The total amount of pixels included in the histogram depends on a number of readout settings, therefore the histogram bins must be compared in a relative way.

ERRATUM: The last word of bin C31 is not transmitted off-chip. The amount of data words per histogram is 71, instead of 72 as indicated in Figure 14. As a result, bin C31 is not usable and should be discarded by the user.

7.8.2 In-Line Streaming Mode

Figure 118:
In-Line Streaming Mode Registers

Register Name	Bank	Addr	Bits	Description
CTRL_MODE	0	11	[2:0]	4: In-line streaming mode
EXP_TIME_INL	0	12-13	[13:0]	Exposure time in in-line streaming mode. Expressed as multiples of ROW_LENGTH
ROW_LENGTH	4	18-19	[13:0]	See section 7.5.2
YWIN_ENA	4	28-29	[9:0]	See section 7.5.3
YWIN*i*	0	18+4×i	[30:0]	See section 7.5.3

The default frame sequence contains a number of overhead rows (see t_{read} in section 7.5.1, subsection “Minimal Frame Time Constraint”). Some of the overhead rows, like t_{stats} can be skipped, others not. Under nominal conditions, these overhead rows do not have a significant impact on the total throughput because their amount is small compared to the number of valid rows being read (t_{fval}).

If the number of valid rows being read is small ("line scan mode"), however, these overhead rows do have a significant impact on the maximum achievable frame rate. The in-line streaming mode removes these overhead rows to achieve a higher frame rate.

Equation 16:

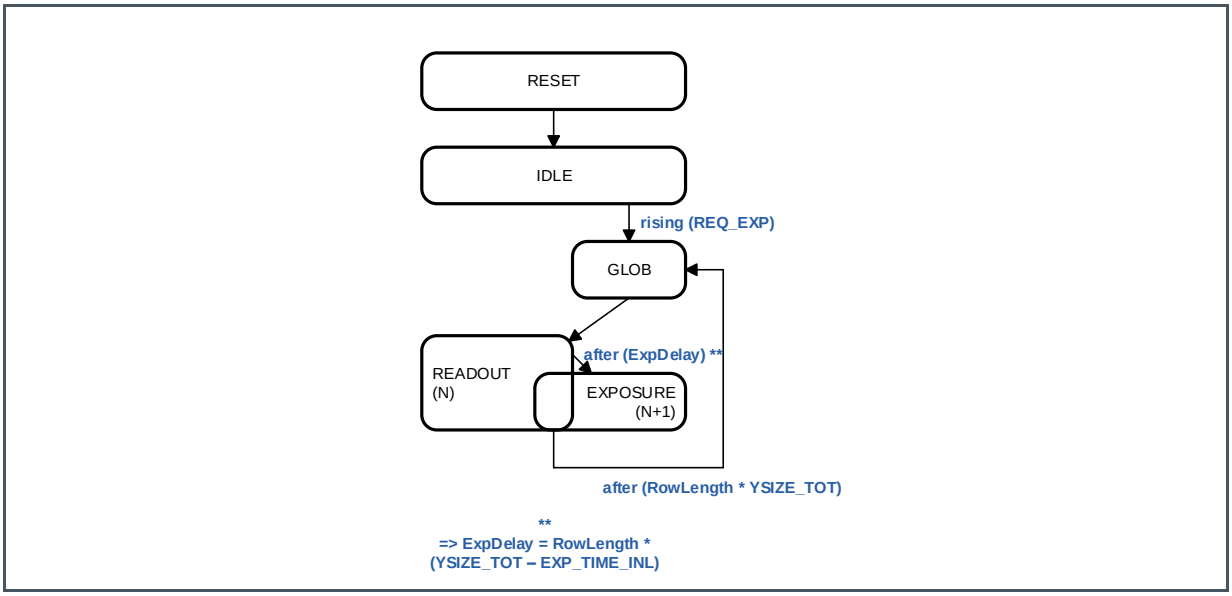
$$t_{frame} = t_{\mathrm{glob}} + t_{row} \times t_{fval}$$

In-line streaming mode is typically used with small Y-windows. In this case, the GLOB length can be reduced to further increase the frame rate.

The in-line streaming mode is enabled by setting the **CTRL_MODE** register to 4. Just like in normal streaming mode, the stream is started with a rising edge on REQ_EXP. The stream stays active forever until externally stopped (with a software non-blocking HALT command or (soft) reset).

The figure below shows the state diagram of the in-line streaming mode.

Figure 119:
State Diagram: In-Line Streaming Mode



In the figure, YSIZE_TOT is the total number of rows that are read in a frame (set with YWINi and YWIN_ENA as described in section 7.5.3). Just like in normal streaming mode, the exposure is pipelined (expose frame N+1 while frame N is being read). The start of exposure is controlled with EXP_TIME_INL (and its relation to YSIZE_TOT). Like in other modes, the shutter lag applies to both start and end of exposure by default. The resulting actual exposure time is always a multiple of the row length.

In case shutter lag is not disabled, the actual exposure time is exactly EXP_TIME_INL * t_{row}. The valid range for the register is 1 ≤ EXP_TIME_INL ≤ YSIZE_TOT.

Attention

After a rising edge on REQ_EXP, the sensor goes directly to a GLOB state without first exposing. This means that the first frame read out after the trigger will contain corrupted data.

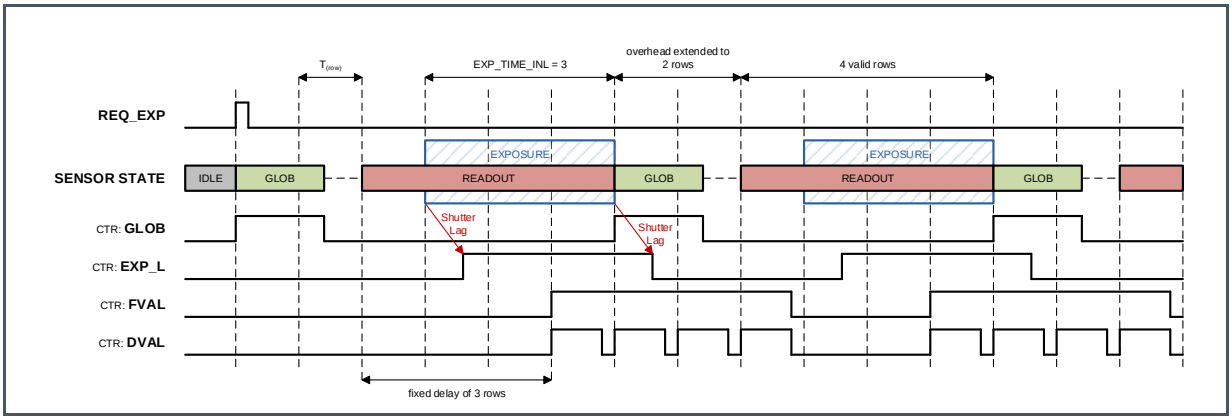
Attention

After a rising edge on REQ_EXP, the sensor goes directly to a GLOB state without first exposing. This means that the first frame read out after the trigger will contain corrupted data.

The entire operation in this mode runs at the rate of the row timing, with a frequency set by ROW_LENGTH (see 7.5.2 for more details). The length of the GLOB state is extended to an exact multiple of the row length by appending some idle time after the word generator program has finished.

The figure below expands the state diagram into a timing diagram. The figure shows an example with the readout of 4 valid rows, a GLOB length of 1.5*t_{row} and EXP_TIME_INL set to 3. The figure also shows a number of bits of the CTR_OUT channel to illustrate what is going on.

Figure 120:
Timing Diagram: In-Line Streaming Mode



Information

In-line streaming mode is incompatible with these functionalities:

- Dual exposure
- Synchronized register updates and context switching
- Image statistics
- Dummy rows

7.8.3 Not-Safe-to-Request Status

Figure 121:
EN_NSF Register

Reg. Name	Bank	Addr	Bits	Description
EN_NSF	0	76	[0:0]	'0': Bits 8 and 9 in the CTR word are '0' '1': Enable NSFE and NSFR status bits on the control channel

The sensor can indicate through status bits when it is not safe to request a new frame/exposure or when it will be ignored. This coincides with these invalid and special cases described in 7.2.7 :

- FE_i0, FE_i1, FE_i2, FE_i3
- PE_i0, PE_s2
- TI_s2
- In steaming mode, the status bits indicate that the request will be ignored.

The status bits can be enabled on the CTRL channel or observed on one of the digital test output pins.

Attention

Enabling the not-safe-to-request status bits on the CTRL channel might influence the control word in idle state. It is therefore recommended to perform control channel training with EN_NSF set to '0'.

7.8.4 Digital Test Output

Figure 122:
Digital Test Output Register

Reg. Name	Bank	Addr	Bits	Description
DMUX1_SEL	3	50-51	[9:5]	Sets pin TDIG1 function
DMUX2_SEL	3	50-51	[14:10]	Sets pin TDIG2 function

A number of digital signals of the chip can be monitored in real-time during normal sensor operation via the sensor output pins TDIG1 to TDIG4. This can be useful for testing and debugging the system without having to rely on the sub-LVDS implementation of the control channel, so a test pad or connection to the FPGA is recommended.

Selecting which signal to be monitored is done with **DMUX1_SEL** registers for TDIG1 (bottom) and TDIG3 (top) and with **DMUX2_SEL** registers for TDIG2 (bottom) and TDIG4 (top).

Figure 123:
TDIG Mapping

DMUX*_SEL	Description
0	PLL lock status
8	Global sampling phase(1)
9	Exposure status (group S)
10	Exposure status (group L)
11	EOBVAL
12	SVAL
13	FVAL

DMUX*_SEL	Description
14	DVAL
24	NSRF (Not-Safe-to request frame status bit)
25	NSRE (Not-Safe-to request exposure status bit)

(1) GLOB time seen on TDIG pin is only a fraction of the real GLOB time. GLOB program still extends after falling edge of this signal.

7.8.5 OTP Memory

A non-volatile, one time programmable memory is provided on-chip. This is programmed with unique device ID and temperature sensor calibration data from both temperature sensors. During manufacturing, both temperature sensors are read out from the SPI registers in a controlled environment temperature. The data is then written to the OTP memory.

The OTP memory is organized in 64 addresses of 8 bits each. Only the following registers are useful for end users.

Figure 124:
OTP Memory Map

OTP Cell Name	Address	Bits	Description
Version	0	[7:0]	Highest bit denotes the version
TSENS1_CONV_MSB	22	[7:0]	Temperature sensor SPI value read when wafer testing at 60 ºC. These values can be used for calibrating the temperature sensor. Data from top temperature sensor.
TSENS1_CONV_LSB	23	[7:0]	
TSENS1_REF_MSB	24	[7:0]	
TSENS1_REF_LSB	25	[7:0]	
TSENS2_CONV_MSB	26	[7:0]	Data for bottom temperature sensor.
TSENS2_CONV_LSB	27	[7:0]	
TSENS2_REF_MSB	28	[7:0]	
TSENS2_REF_LSB	29	[7:0]	
Chuck Temperature	30	[7:0]	Temperature of wafer during production testing. Should be used for temperature calibration.
Resolution	31	[7:0]	Denotes 8 k or 14 k resolution. 0b 0000 0000 = Virgin state 0b 0000 0001 = 14 K full resolution 0b 0000 0011 = 8 K resolution 0b 0000 01xx = 14 K full resolution 0b 0000 11xx = 8 K resolution 0b 0001 xxxx = 14 K full resolution 0b 0011 xxxx = 8 K resolution 0b 01xx xxxx = 14 K full resolution 0b 11xx xxxx = 8 K resolution

Readout of the OTP registers requires interfacing with following SPI registers.

Figure 125:
OTP SPI Registers

Reg. Name	Bank	Addr	Bits	Description
OTP_CONTROL	3	24	[11:0]	OTP control register
OTP_A	3	26	[8:0]	OTP address
OTP_DOUT	3	28	[7:0]	OTP data out

The procedure to readout an OTP register goes as follows:

1. Set BANK_SEL to 3
2. Set BLOCK_SEL to 20
3. Set OTP_CONTROL to 3
4. Set OTP_CONTROL to 7
5. Set OTP_CONTROL to 21
6. Set OTP_A to the desired OTP address
7. Set OTP_CONTROL to 29
8. Set OTP_CONTROL to 21
9. Read data from OTP_DOUT
10. Set OTP_CONTROL to 7

7.8.6 Temperature Sensor

Figure 126:
Temperature Sensor Register

Reg. Name	Bank	Addr	Bits	Description
TSENS_CONTROL.EN	3	30	[0:0]	Temperature sensor power up
TSENS_CONTROL.MEAS	3	30	[5:1]	Temperature sensor measurement control
TSENS_REF	3	31-32	[15:0]	Pulse width of output reference voltage
TSENS_CONV	3	33-34	[15:0]	Pulse width of converted temperature voltage

Uncalibrated Temperature Measurement

To perform an uncalibrated temperature measurement, with an accuracy of ±5°C, follow this procedure:

1. Set TSENS_CONTROL to 1 (power-up temperature sensor)
2. Wait for 100 µs
3. Set TSENS_CONTROL to 31
4. Wait for 10 µs
5. Set TSENS_CONTROL to 27
6. Wait for 1 µs
7. Set TSENS_CONTROL to 11
8. Wait for 1 µs
9. Set TSENS_CONTROL to 9
10. Wait for 1 µs
11. Set TSENS_CONTROL to 33
12. Wait for 200 µs
13. Read TSENS_REF and TSENS_CONV
14. Calculate the uncalibrated temperature with the equation

Equation 17:

$$T\,[°C] = \frac{425 \times TSENS\_CONV}{TSENS\_REF} - 273.15$$

15. To start a new measurement, go back to step 3
16. To power down the temperature sensor, set TSENS_CONTROL to 0

Information

The temperature measurement uses the internal clock. This means that the sensor must have followed the flow chart in section 7.4.3 until at least the soft reset release step before a temperature measurement can be started.

Calibrated Temperature Measurement

The accuracy of temperature measurements can be improved to ±1°C after performing a single-point calibration.

During wafer test, temperature is measured in a controlled environment. Calibration data is written to the OTP memory of the sensor.

In section 7.8.5 we described how to read out data from OTP fuses.

Calibration of the temperature sensor readout value involves two steps:

1. Calculate the calibration gain coefficient using following equation:

Equation 18:

$$A_{cal} = \frac{T_{wafer,expected}[°C] + 273.15}{T_{wafer,measured}[°C] + 273.15}$$

Which uses following parameters:

- $T_{wafer,expected}$ is the expected temperature at wafer test, which is close to 60 ºC. The exact value is stored in OTP register “Chuck Temperature” (see Figure 124)
- $T_{wafer,measured}$ is the measured (uncalibrated) temperature sensor value at wafer test. The values can be calculated based on the temperature sensor readout values TSENS_REF and TSENS_CONV, as stored in OTP registers “TSENSx_CONV” and “TSENSx_REF” (see Figure 124). Using both values, the corresponding temperature value can be calculated using Equation 19.

This calibration gain coefficient is fixed and only needs to be calculated once.

Note that a separate calibration gain coefficient needs to be calculated for both temperature sensors.

2. Calculate the calibrated temperature measurement value using following equation:

Equation 19:

$$T_{cal}\,[°C] = A_{cal} \times (T_{uncal,x}[°C] + 273.15) - 273.15$$

7.8.7 Enable Optical Black Outputs

The OB pixels on the right side of the pixel array that are used for on-chip OB correction can be read out through the DOUT_OB_* output channels. By default, these channels are disabled.

To enable the DOUT_OB_* channels, use the SPI sequence listed in Figure 127. Note that the registers should only be written to the specified BLOCK_IDs.

Figure 127:
Enable OB Outputs Sequence

#	Register	Bank	Address	BLOCK_ID	Value
1	DATA_CH_CTRL	3	74	18	1027
2	DATA_CH_CTRL	3	74	19	1027

Using the DOUT_OB_* channels is optional. Using the channels requires routing additional output channels to the receiving system.

Enabling the DOUT_OB_* channels has no impact on the regular DOUT* channels transporting the visible pixel data.

7.8.8 Test Images

The data stream can be replaced with a number of test patterns. Selection of test mode is made with the **TEST_LVDS** register as indicated in the table below.

Figure 128:
Test Images Registers

Reg. Name	Bank	Addr	Bits	Description
TEST_LVDS	0	75	[1:0]	See table below
TRAINING_WORD	0	73-74	[12:0]	Choose a value
TX_TEST_EN	3	74-75	[9:7]	See table below. Applies to DATAx_OUT, OB_OUT and CTR_OUT
CLK_OUT.TX_TEST_EN	3	78-79	[9:7]	See table below. Applies only to CLK_OUT

Figure 129:
Test Modes

#	TX_TEST_EN	TEST_LVDS	DATAx_OUT	OB_OUT	CTR_OUT	CLK_OUT
0	0	0	Normal	Normal	Normal	Normal
1	0	1	Force training word continuously	Force training word continuously	Force training word continuously	Normal
2	0	2	Test image: gradient	Drive constant 0	Normal	Normal
3	0	3	Test image: LFSR	Drive constant 0	Normal	Normal
4	1	-	Force clock output	Force clock output	Force clock output	Normal
5	3	-	PRBS-7	PRBS-7	PRBS-7	PRBS-7
6	4	-	PRBS-15	PRBS-15	PRBS-15	PRBS-15

Mode 0 is the functional mode. Modes 1 to 3 are test modes that replace the image data with known data. In test mode 1, the data and OB output channels are forced to output register **TRAINING_WORD** and the control channel outputs its own training word.

In test modes 2 and 3, a fixed test image is created. The CLK_OUT and CTR_OUT channels drive their normal values, so only the actual pixel data is replaced. This is useful to debug the camera system before grabbing real images.

In test mode 2, the data of pixel N is replaced by the value:

Equation 20:

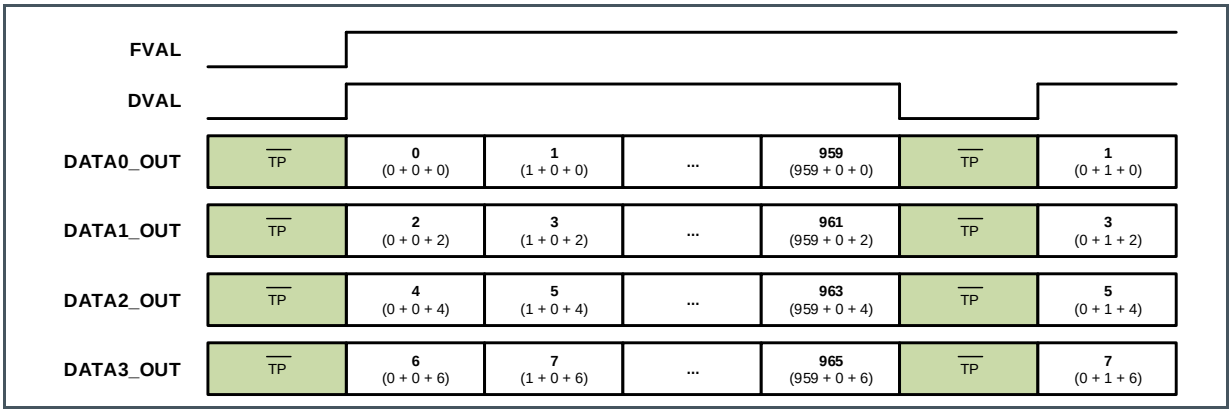
$$D_{TEST} = N_{COL} + N_{ROW} + N_{KERNEL} + 1$$

With:

- N_{COL} is the running number of pixel N in the DVAL pulse (0 for first valid pixel on each output)
- N_{ROW} is the running number of the DVAL pulse within FVAL (0 for first valid row in each FVAL)
- N_{KERNEL} is the number of the originating DPP block that generates pixel N (per side ranging from 0 to 7)

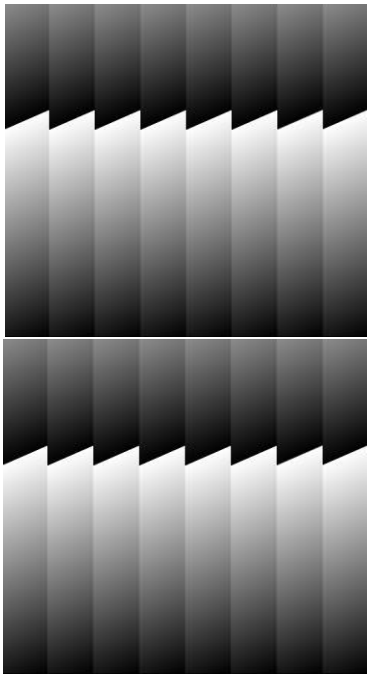
The result is a 2D gradient (per channel), with a starting offset depending on the kernel number. The figure below shows an example using NR_OUTP = 4, XSTART = 0, KSIZE=960 (N_{KERNEL} is resp. 0, 2, 4, 6).

Figure 130:
Gradient Test Image Pixel Data



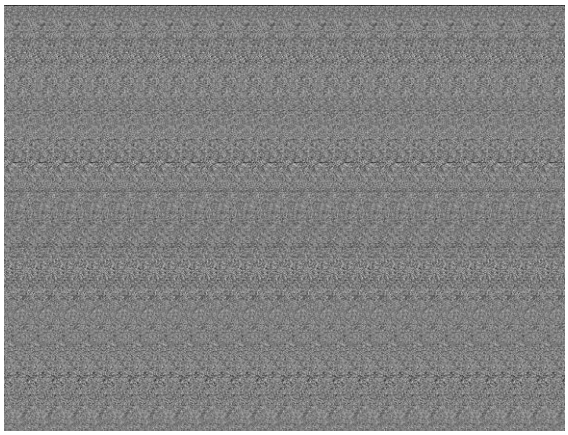
The resulting image for YWIN_DIR = 0 is shown in the figure below. Note that the gradient test image has no relation to the physical pixel array and can contain more rows than the pixel array. Depending on the setting of OUTP_BITMODE and YWIN_SIZE, the gradient will wrap around.

Figure 131:
Gradient Test Image Example



In test mode 3, the actual data of every pixel is replaced by the output of a pseudo-random generator. The value of the first valid pixel of a frame is 4095. All outputs drive the same output value (unlike test mode 2, where the N_{KERNEL} generates an offset between outputs).

Figure 132:
LSFR Test Image Example



8 Register Overview

For easier reading, logical -instead of physical- register names are used to identify registers in this document.

The table below shows how each logical register (reg name) or logical register field (bit name) maps to a physical register's B(ank), A(ddress) and used bit P(ositions). The CAT(egory) are the Register Categories as described in 7.2.4. ID shows the value of BLOCK_ID to be set before reading a certain register.

More details for each register can be found in the referred section.

Attention

All non-described address locations are reserved. Only values specified in section 7.4.3 are allowed to be uploaded to these reserved/internal registers.

Figure 133:
Register Overview

B	A	P	Reg Name	Bit Name	CAT	ID	Section
-	0	[7:0]	BANK_SEL	-	-	-	7.2.4
-	1	[7:0]	BLOCK_ID	-	-	-	7.2.4
-	2	[7:0]	ACTIVE_CONTEXT	-	SYNC	-	7.2.4
-	3	[7:0]	RW_CONTEXT	-	-	-	7.2.4
0	4	[0:0]	PARAM_HOLD	-	-	0-1	7.2.4
0	5	[0:0]	DISABLE_FRAMESYNC	-	-	0-21	7.2.4
0	6	[0:0]	CMD_REGS	CMD_RST_SOFT_N	-	0-19	7.2.5
0	6	[1:1]	CMD_REGS	CMD_REQ_EXP	-	0-1	7.2.8
0	6	[2:2]	CMD_REGS	CMD_REQ_FRAME	-	0-1	7.2.8
0	6	[3:3]	CMD_REGS	CMD_HALT_BLOCK	-	0-1	7.2.8
0	6	[4:4]	CMD_REGS	CMD_HALT_NBLOCK	-	0-1	7.2.8
0	7	[1:0]	OUTP_BITMODE	-	RSTN	0-19	7.7.3
0	8	[0:0]	OUTP_FORMAT	-	RSTN	0-19	7.4.3
0	9	[1:0]	COMMA_SEL	FVAL0	DC	2-19	7.6.1
0	9	[3:2]	COMMA_SEL	FVAL1	DC	2-19	7.6.1
0	10	[0:0]	OUTP_BITORDER	-	DC	0-19	7.6.3
0	11	[2:0]	CTRL_MODE	-	DC	0-1	7.2.7
0	12	[13:0]	EXP_TIME_INL	-	SYNC	0-1	7.8.2
0	14	[3:0]	MAX_NR_OUTP	-	RSTN	2-17	7.6.2

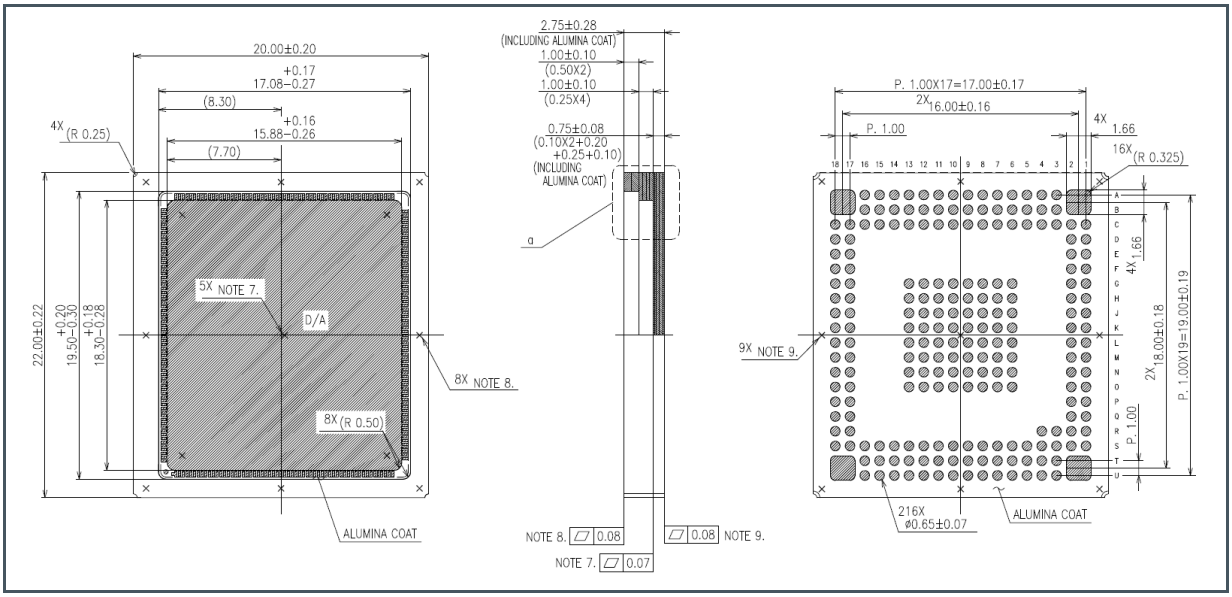
B	A	P	Reg Name	Bit Name	CAT	ID	Section
0	15	[9:0]	YWIN_BLACK	-	SYNC	0-1	7.5.3
0	17	[0:0]	YWIN_DIR	-	SYNC	0-1	7.5.3
0	18	[13:0]	YWIN0	SIZE	SYNC	0-1	7.5.3
0	18	[27:14]	YWIN0	START	SYNC	0-1	7.5.3
0	18	[30:28]	YWIN0	SUBS	SYNC	0-1	7.5.4
0	22	[13:0]	YWIN1	SIZE	SYNC	0-1	7.5.3
0	22	[27:14]	YWIN1	START	SYNC	0-1	7.5.3
0	22	[30:28]	YWIN1	SUBS	SYNC	0-1	7.5.4
0	26	[13:0]	YWIN2	SIZE	SYNC	0-1	7.5.3
0	26	[27:14]	YWIN2	START	SYNC	0-1	7.5.3
0	26	[30:28]	YWIN2	SUBS	SYNC	0-1	7.5.4
0	30	[13:0]	YWIN3	SIZE	SYNC	0-1	7.5.3
0	30	[27:14]	YWIN3	START	SYNC	0-1	7.5.3
0	30	[30:28]	YWIN3	SUBS	SYNC	0-1	7.5.4
0	34	[13:0]	YWIN4	SIZE	SYNC	0-1	7.5.3
0	34	[27:14]	YWIN4	START	SYNC	0-1	7.5.3
0	34	[30:28]	YWIN4	SUBS	SYNC	0-1	7.5.4
0	38	[13:0]	YWIN5	SIZE	SYNC	0-1	7.5.3
0	38	[27:14]	YWIN5	START	SYNC	0-1	7.5.3
0	38	[30:28]	YWIN5	SUBS	SYNC	0-1	7.5.4
0	42	[13:0]	YWIN6	SIZE	SYNC	0-1	7.5.3
0	42	[27:14]	YWIN6	START	SYNC	0-1	7.5.3
0	42	[30:28]	YWIN6	SUBS	SYNC	0-1	7.5.4
0	46	[13:0]	YWIN7	SIZE	SYNC	0-1	7.5.3
0	46	[27:14]	YWIN7	START	SYNC	0-1	7.5.3
0	46	[30:28]	YWIN7	SUBS	SYNC	0-1	7.5.4
0	50	[13:0]	YWIN8	SIZE	SYNC	0-1	7.5.3
0	50	[27:14]	YWIN8	START	SYNC	0-1	7.5.3
0	50	[30:28]	YWIN8	SUBS	SYNC	0-1	7.5.4
0	54	[13:0]	YWIN9	SIZE	SYNC	0-1	7.5.3
0	54	[27:14]	YWIN9	START	SYNC	0-1	7.5.3
0	54	[30:28]	YWIN9	SUBS	SYNC	0-1	7.5.4
0	58	[12:0]	EOB_TARGET	-	SYNC	2-17	7.7.1
0	65	[0:0]	COMPRESS_EN	-	SYNC	2-17	7.7.3
0	66	[12:0]	COMPRESS_KNEEPOINT	-	SYNC	2-17	7.7.3
0	68	[1:0]	COMPRESS_RATIO	-	SYNC	2-17	7.7.3
0	69	[1:0]	DPATH_BITMODE	-	DC	0-19	7.8.1
0	70	[2:0]	STAT_NROF_HIST	-	SYNC	0-1	7.8.1
0	71	[7:0]	STAT_FREQ	-	SYNC	0-1	7.8.1
0	73	[12:0]	TRAINING_WORD	-	DC	0-19	7.6.1

B	A	P	Reg Name	Bit Name	CAT	ID	Section
0	75	[1:0]	TEST_LVDS	-	DC	0-19	7.8.8
0	76	[0:0]	EN_NSF	-	-	0-1	7.8.3
0	85	[0:0]	PLL_LOCK	-	RO	0-1	7.4.3
0	93	[0:0]	EOB_BYPASS	-	DC	18-19	7.7.1
0	94	[12:0]	EOB_BYPASS_VALUE	-	DC	18-19	7.7.1
1	32	[15:0]	SHUTTER_LAG	-	DC	0-1	7.5.1
3	24	[0:11]	OTP_CONTROL	-	-	20-21	7.8.5
3	26	[8:0]	OTP_A	-	-	20-21	7.8.5
3	28	[7:0]	OTP_DOUT	-	RO	20-21	7.8.5
3	30	[2:2]	TSENS_CONTROL	TSENS_AMP_PC	-	20-21	7.8.6
3	30	[3:3]	TSENS_CONTROL	TSENS_RAMP_PC	-	20-21	7.8.6
3	30	[4:4]	TSENS_CONTROL	TSENS_COMP_PC	-	20-21	7.8.6
3	30	[5:5]	TSENS_CONTROL	TSENS_EN_MEASUREMENT	-	20-21	7.8.6
3	31	[7:0]	TSENS_REF_LSB	-	RO	20-21	7.8.6
3	32	[7:0]	TSENS_REF_MSB	-	RO	20-21	7.8.6
3	33	[7:0]	TSENS_CONV_LSB	-	RO	20-21	7.8.6
3	34	[7:0]	TSENS_CONV_MSB	-	RO	20-21	7.8.6
3	50	[9:5]	TDIG	DMUX1_SEL	-	0-1	7.8.4
3	50	[14:10]	TDIG	DMUX2_SEL	-	0-1	7.8.4
3	74	[9:7]	DATA_CH_CTRL	TX_TEST_EN	RSTN	0-19	7.8.8
3	78	[9:7]	CLK_CH_CTRL	TX_TEST_EN	RSTN	18-19	7.8.8
3	100	[12:0]	EOB_CLIP	-	SYNC	18-19	7.7.1
4	4	[0:0]	COLOR_MODE	-	SYNC	0-19	7.5.5
4	5	[13:0]	TIME_UNIT	-	DC	0-1	7.5.1
4	7	[7:0]	NROF_FRAMES	-	CONTEXT	0-1	7.5.1
4	8	[15:0]	MIN_FRAME_TIME	-	SYNC	0-1	7.5.1
4	10	[15:0]	GLOB_TIME	-	DC	0-1	7.5.1
4	12	[0:0]	DUAL_EXPOSURE	-	CONTEXT	0-1	7.5.1
4	13	[0:0]	DUAL_EXP_GROUPING	-	CONTEXT	0-1,20-21	7.5.1
4	14	[15:0]	EXP_TIME_L	-	CONTEXT	0-1	7.5.1
4	16	[15:0]	EXP_TIME_S	-	CONTEXT	0-1	7.5.1
4	18	[13:0]	ROW_LENGTH	-	SYNC	0-1	7.5.2
4	20	[13:0]	XSTART	-	SYNC	0-1	7.5.4
4	22	[1:0]	XSUBS	-	SYNC	2-19	7.4.1
4	23	[13:0]	KSIZE	-	SYNC	0-17	7.5.4
4	27	[3:0]	NR_OUTP	-	SYNC	2-17	7.6.2
4	28	[9:0]	YWIN_ENA	-	SYNC	0-1	7.5.3
4	30	[7:0]	GDIG_RE_CE	-	SYNC	2-19	7.7.2
4	31	[7:0]	GDIG_RE_CO	-	SYNC	2-19	7.7.2
4	32	[7:0]	GDIG_RO_CE	-	SYNC	2-19	7.7.2

B	A	P	Reg Name	Bit Name	CAT	ID	Section
4	33	[7:0]	GDIG_RO_CO	-	SYNC	2-19	7.7.2
4	35	[0:0]	DATA_CH_EN_DRIVE	-	SYNC	0-19	7.6.2

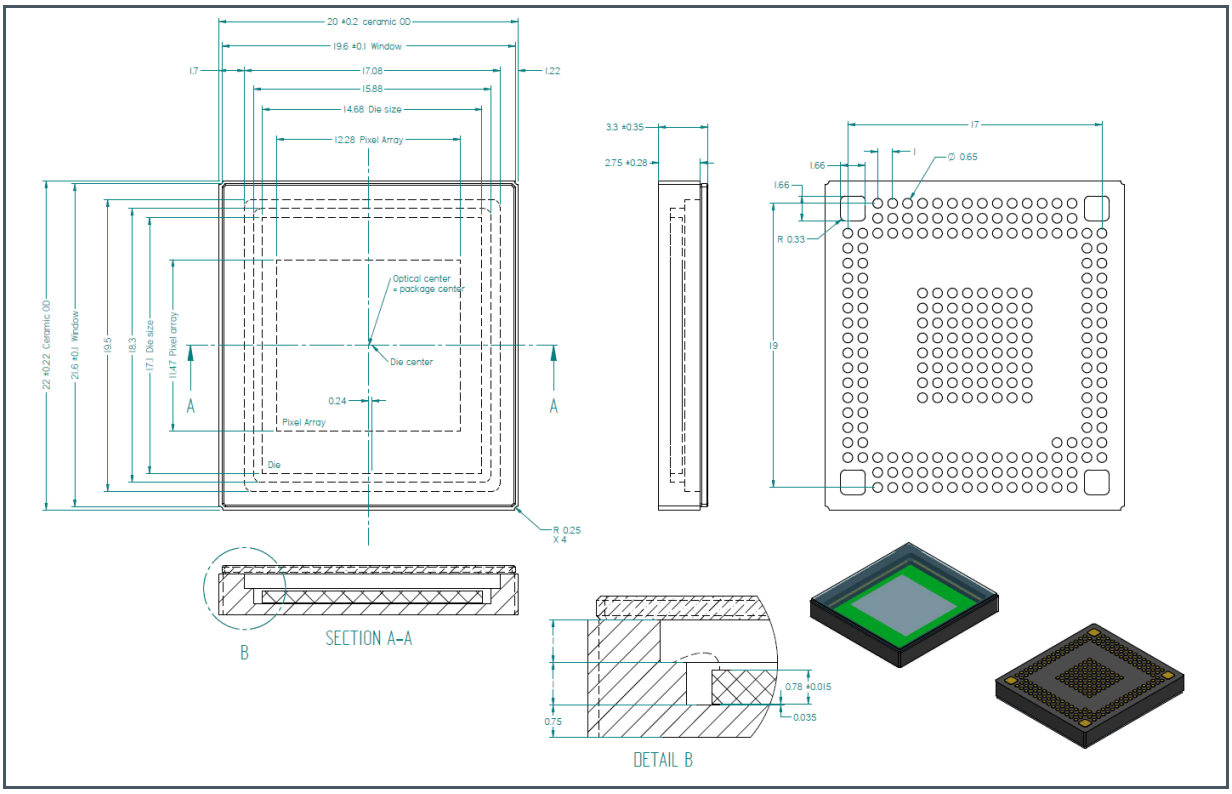
9 Package Drawings & Markings

Figure 134:
216p LGA Package Outline Drawing



(1) All dimensions are in millimeters. Angles in degrees.

Figure 135:
216 p LGA Assembly Outline Drawing



(1) All dimensions are in millimeters. Angles in degrees.

Figure 136:
Package Marking/Code

AWWYYCCNNNN

A = Assembly subcontractor sensor ID
WW = Manufacturing Week
YY = Manufacturing Year
CC = CMOSIS number
NNNN = Running serial number within an ARF, starting with 0001

10 Soldering & Storage Information

Figure 137:
Solder Reflow Profile Graph

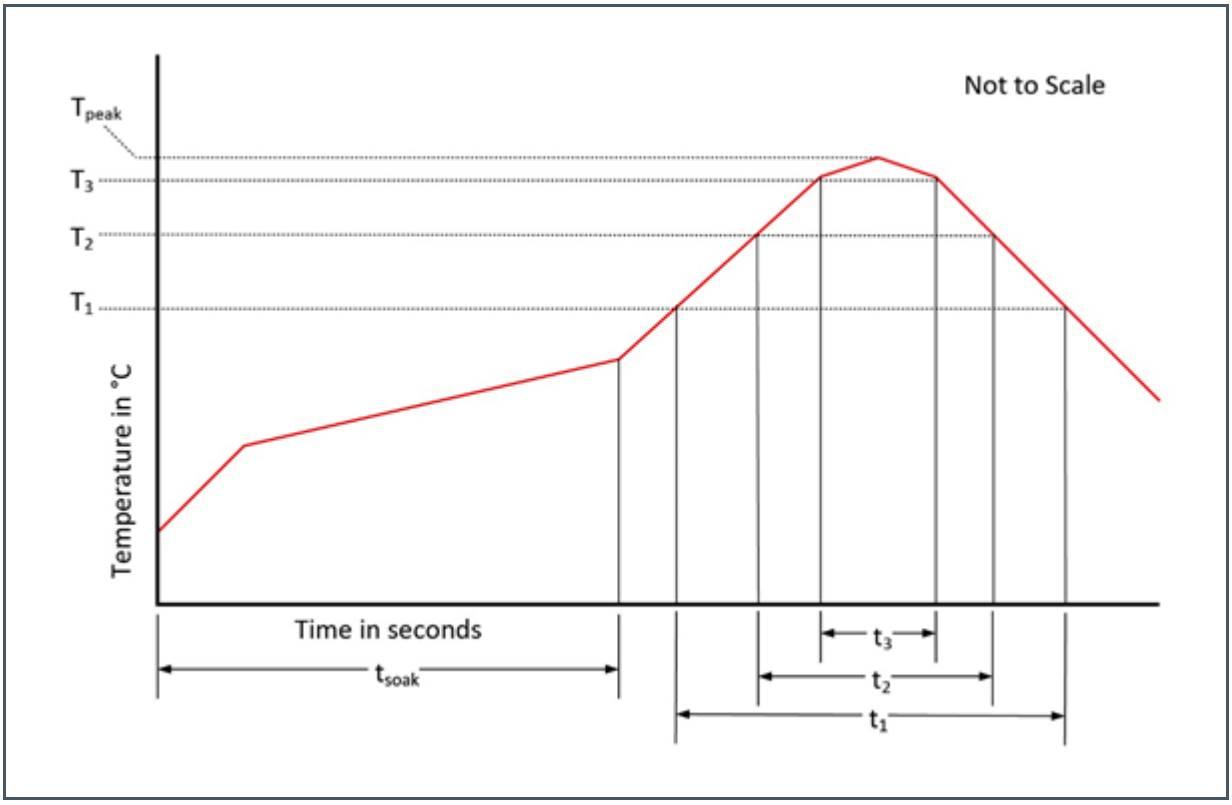


Figure 138:
Solder Reflow Profile (1)

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60 s
Time above 230 °C (T2)	t_2	Max 50 s
Time above T_{peak} – 10 °C (T3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	245 °C
Temperature gradient in cooling		Max −5 °C/s

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn)

11 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v1-00	Page
Added connection info for DIN_* pins	8
Change 3.3V tolerance to ±50mV	11
Updated Figure 7 (Responsivity, PRNU)	12
Corrected QE graphs	13
Corrected connection diagram to be in line with the description	21
Mistake in table, replaced with VDD33	25
Added row to Figure 72 (1000 – 1250 Mbit/s)	66
Binning mode corrected with 2 extra registers.. + KSIZE table	
Removed IMG.6 and IMG.8 modes	
Removed color parts	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

12 Legal Information

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