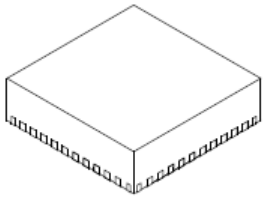
Bi-CMOS Linear Integrated Circuit, Silicon Monolithic

TB9053FTG,TB9054FTG

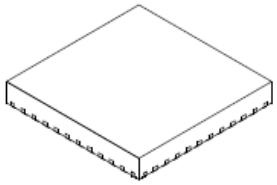
PWM type 2-channel H-Bridge DC brushed motor driver for automotive application

TB9053FTG



P-QFN40-0606-0.5

TB9054FTG



P-VQFN40-0606-0.5

1. Outline

TB9053FTG and TB9054FTG incorporates in each two channels of output driver for the direct drive of a DC brushed motor for automotive application.

The PWM control with low on-resistance enables highly efficient motor drive output.
Forward, reverse, or brake mode can be selected for motor 1 using the PWM1 and PWM2 pins, and for motor 2 using the PWM3 and PWM4 pins. The ENABLE pins (EN1/ENB1 and EN2/ENB2) can select motor drive or stop mode.
The devices can control the motor 1 speed by PWM signal duty to PWM1/PWM2 pins or through SPI registers, that is selectable with ISEL1 input signal.
The devices can control the motor 2 speed by PWM signal duty to PWM3/PWM4 pins or through SPI registers, that is selectable with ISEL2 input signal.
The output current capacity is 6.5 A (typ.), which is suitable for a wide range of automotive applications such as a throttle valve control, various engine valves, retractable door mirrors, and a seat positioning.

2. Application

Automotive applications such as a throttle valve control, various engine valves, retractable door mirrors, and a body system including an electric door latch, etc.

3. Features

- Motor driver block: 2-channel H-bridge driver
  (Ron(Nch+Nch)) = 142 mΩ (Typ. @Tj = 25°C, VBAT = 8 V)
  2-channel mode and combined 2-channel mode selectable
- Detection features: Over-current detection, over-temperature detection, VBAT under-voltage detection, and VCC under-voltage detection
- Initial diagnosis: Power supply fault detection circuit (VBAT under-voltage and VCC under-voltage)
- PWM control output
- Forward/reverse/brake modes
- Current limit control: Chopper-type current limiter
- Hi-side output current monitoring function (CM1 and CM2 pins)
- Open-load detection: During operation/non-operation
- Diagnosis output (DIAG1 and DIAG2 pins)
- H-bridge mode/Half-bridge mode selectable with OSEL1 and OSEL2
- Low-power sleep mode
- Through-current prevention circuit

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- SPI communication: fault reporting, device settings and motor control through the SPI registers
- Operating voltage range: VBAT = 4.5 to 28 V (Maximum rating of power supply voltage 40 V (max.) (0.5 s))
  VCC = 4.5 to 5.5 V
  VDDIO = 3.0 to 5.5 V
- Operating ambient temperature range: Ta = -40°C to 125°C
- Small flat package: QFN40-0606-0.5(TB9053FTG), VQFN40-0606-0.5(TB9054FTG)

- If the label of shipping box indicates "[[G]]/RoHS COMPATIBLE", "[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)", "RoHS COMPATIBLE", or "RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV", this product is compatible with the EU RoHS Directive (2011/65/EU) in the sense that the indication states.

4. Block diagram

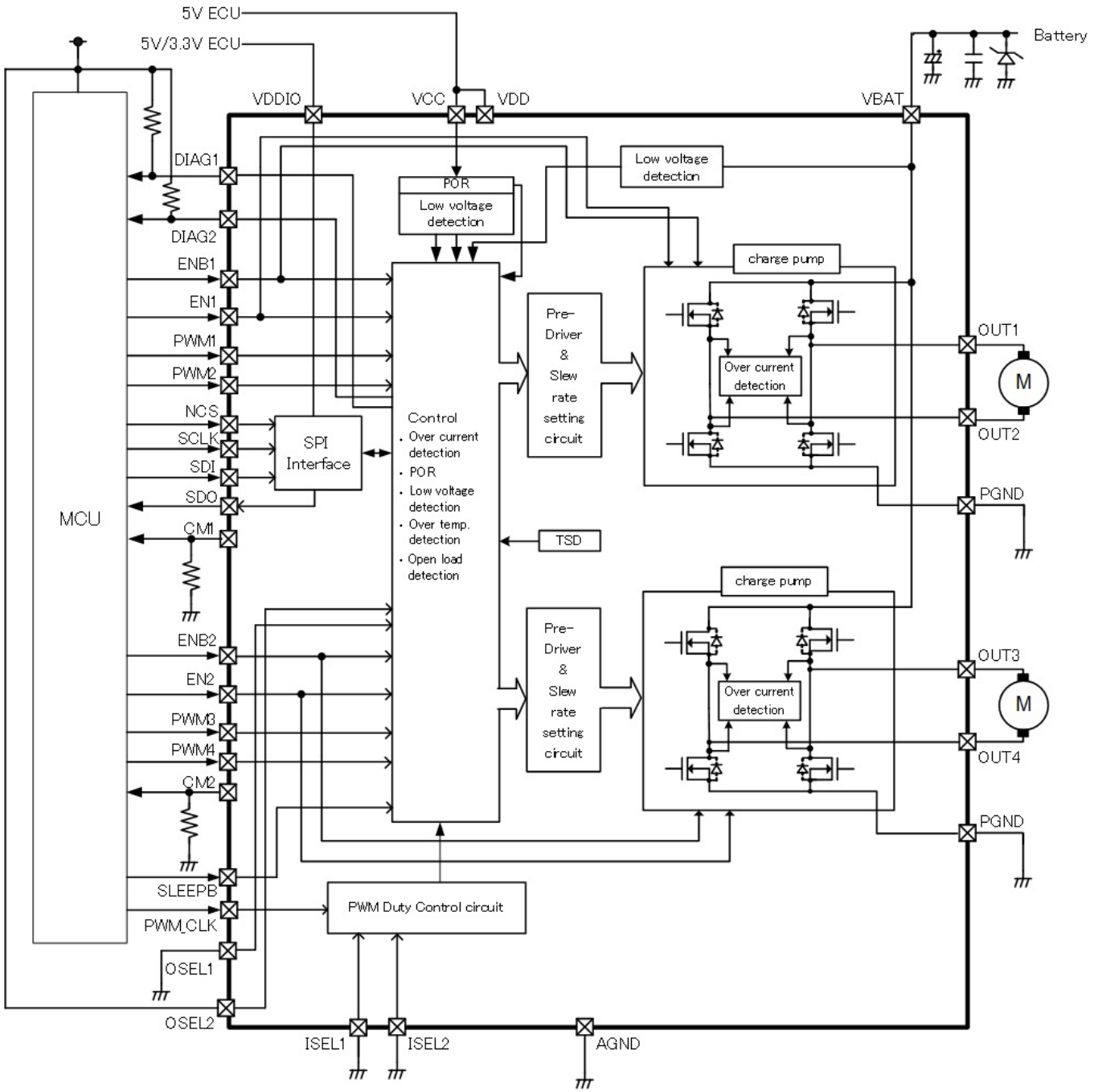


Figure 4.1 Block diagram

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.
The signal supplied to each driver output circuit is not a signal generated by logical operation between the EN and ENB pin inputs, the independent EN and ENB signals are directly supplied to each driver output circuit instead.

5. Function description

In the specifications below, DT denotes a dead time and SB denotes a short brake at motor drive operations.

5.1. Motor drive output circuit

The output circuit operates in the following functions (Table 5.1).

In Table 5.1 to Table 5.3, the following notation are used. X: Don't Care, H: High, L: Low, Z: High Impedance.

	OSEL1	OSEL2
LARGE mode (combined 2 channels; 1 motor)	L	L
Half mode	H	L
SMALL mode (separate 2 channels; 2 motors)	L	H
Prohibited mode (Motor output OFF)	H	H

Note: The OSEL1 and OSEL2 pin inputs are latched when the initial diagnosis starts. If prohibited mode is entered, reset the VCC power supply (by lowering it below the VCC under-voltage POR detection voltage) to restart the IC.

5.1.1. 2-channel mode (SMALL mode) (OSEL1 = L and OSEL2 = H)

Table 5.1 H-bridge motor function 1

	PWM1	PWM2	EN1	ENB1	SLEEPB	OUT1	OUT2
Forward	H	L	H	L	H	**H**	**L**
Short brake	L	L	H	L	H	**L**	**L**
Reverse	L	H	H	L	H	**L**	**H**
Short brake	H	H	H	L	H	**H**	**H**
EN1 Disable	X	X	L	L	H	**Z**	**Z**
ENB1 Disable	X	X	H	H	H	**Z**	**Z**
Sleep mode	X	X	X	L/H	L	**Z**	**Z**
EN1 Disconnected	X	X	Z	X	X	**Z**	**Z**
ENB1 Disconnected	X	X	X	Z	X	**Z**	**Z**
PWM1 Disconnected	Z	L/H	H	L	H	**L**	**L/H**
PMM2 Disconnected	L/H	Z	H	L	H	**L/H**	**L**

	PWM3	PWM4	EN2	ENB2	SLEEPB	OUT3	OUT4
Forward	H	L	H	L	H	**H**	**L**
Short brake	L	L	H	L	H	**L**	**L**
Reverse	L	H	H	L	H	**L**	**H**
Short brake	H	H	H	L	H	**H**	**H**
EN2 Disable	X	X	L	L	H	**Z**	**Z**
ENB2 Disable	X	X	H	H	H	**Z**	**Z**
Sleep mode	X	X	X	L/H	L	**Z**	**Z**
EN2 Disconnected	X	X	Z	X	X	**Z**	**Z**
ENB2 Disconnected	X	X	X	Z	X	**Z**	**Z**
PWM3 Disconnected	Z	L/H	H	L	H	**L**	**L/H**
PMM4 Disconnected	L/H	Z	H	L	H	**L/H**	**L**

Note: When changing the motor rotation from Forward to Reverse or vice versa, always insert a brake, which involves regeneration. Otherwise, the IC may be broken down.

Note: When the current limit control is applied, the operation is different from the motor function table above. For details, refer to the current limit control (5.3).

Note: The SLEEPB pin sets a low-power sleep mode. When SLEEPB = L, the system enters a sleep mode. When SLEEPB = H, the system cancels a sleep mode.

Note: When SLEEPB = L, the ENB1/2 pins does not use OPEN, set the ENB1/2 pins to L or H.

5.1.2. Combined 2-channel mode (LARGE mode) (OSEL1 = L and OSEL2 = L)

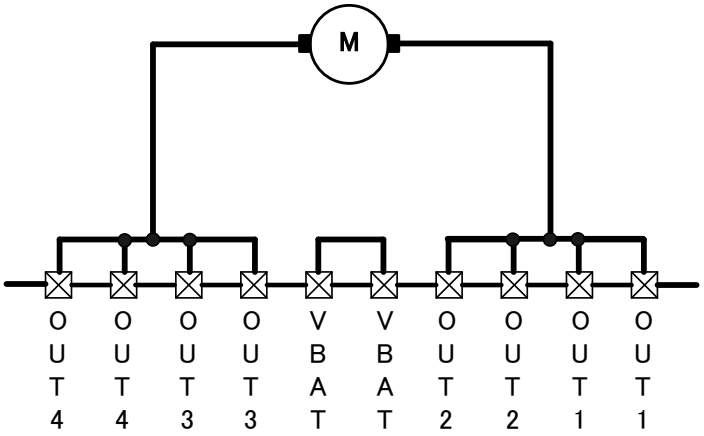
PWM3 and PWM4 are ineffective.
Externally short-circuit ISEL1/2, EN1/2, ENB1/2, OUT1/2, and OUT3/4.

Table 5.2 H-bridge motor function 2

	PWM1	PWM2	EN	ENB	SLEEPB	**OUT1/2**	**OUT3/4**
Forward	H	L	H	L	H	**H**	**L**
Short brake	L	L	H	L	H	**L**	**L**
Reverse	L	H	H	L	H	**L**	**H**
Short brake	H	H	H	L	H	**H**	**H**
EN Disable	X	X	L	L	H	**Z**	**Z**
ENB Disable	X	X	H	H	H	**Z**	**Z**
Sleep mode	X	X	X	L/H	L	**Z**	**Z**
EN Disconnected	X	X	Z	X	X	**Z**	**Z**
ENB Disconnected	X	X	X	Z	X	**Z**	**Z**
PWM1 Disconnected	Z	L/H	H	L	H	**L**	**L/H**
PMM2 Disconnected	L/H	Z	H	L	H	**L/H**	**L**

Note: When SLEEPB = L, the ENB1/2 pins does not use OPEN, set the ENB1/2 pins to L or H.

- Combined 2-channel mode (LARGE mode) uses the IC as a 1-channel device by short-circuiting the outputs as follows:



5.1.3. Half mode (OSEL1 = H and OSEL2 = L)

Table 5.3 Half-bridge motor function

	PWM1	PWM2	EN1	ENB1	SLEEPB	OUT1	OUT2
OUT1 H	H	X	H	L	H	**H**	**X**
OUT1 L	L	X	H	L	H	**L**	**X**
OUT2 H	X	H	H	L	H	**X**	**H**
OUT2 L	X	L	H	L	H	**X**	**L**
EN1 Disable	X	X	L	L	H	**Z**	**Z**
ENB1 Disable	X	X	H	H	H	**Z**	**Z**
Sleep mode	X	X	X	L/H	L	**Z**	**Z**
EN1 Disconnected	X	X	Z	X	X	**Z**	**Z**
ENB1 Disconnected	X	X	X	Z	X	**Z**	**Z**
PWM1 Disconnected	Z	L/H	H	L	H	**L**	**L/H**
PMM2 Disconnected	L/H	Z	H	L	H	**L/H**	**L**

Note: In the Half-bridge mode, only the motor drive with the PWM1 and PWM2 pins is usable.
Note: In the Half-bridge mode, set the ISEL1 pin to L.
Note: In the Half-bridge mode, if ISEL1 = H, the system enters a prohibited mode (output OFF). During a prohibited mode, a prohibited mode (output OFF) is canceled when ISEL1 is set to L again.
Note: When SLEEPB=L, the ENB1/2 pins does not use OPEN, set the ENB1/2 pins to L or H.

	PWM3	PWM4	EN2	ENB2	SLEEPB	OUT3	OUT4
OUT3 H	H	X	H	L	H	**H**	**X**
OUT3 L	L	X	H	L	H	**L**	**X**
OUT4 H	X	H	H	L	H	**X**	**H**
OUT4 L	X	L	H	L	H	**X**	**L**
EN2 Disable	X	X	L	L	H	**Z**	**Z**
ENB2 Disable	X	X	H	H	H	**Z**	**Z**
Sleep mode	X	X	X	L/H	L	**Z**	**Z**
EN2 Disconnected	X	X	Z	X	X	**Z**	**Z**
ENB2 Disconnected	X	X	X	Z	X	**Z**	**Z**
PWM3 Disconnected	Z	L/H	H	L	H	**L**	**L/H**
PMM4 Disconnected	L/H	Z	H	L	H	**L/H**	**L**

Note: In the Half-bridge mode, only the motor drive with the PWM3 and PWM4 pins is usable.
Note: In the Half-bridge mode, set the ISEL2 pin to L.
Note: In the Half-bridge mode, if ISEL2 = H, the system enters a prohibited mode (output OFF). During a prohibited mode, a prohibited mode (output OFF) is canceled when ISEL2 is set to L again.
Note: When SLEEPB=L, the ENB1/2 pins does not use OPEN, set the ENB1/2 pins to L or H.

5.2. DIAG output

DIAG1 and DIAG2 are open-drain-type output pins. Insert pull-up resistors between these pins and VDDIO (MCU power supply). If no SPI communication is used, connect the VDDIO pin and the external pull-up resistors, that is connected at DIAG1 and DIAG2, to the VCC power supply.
When the following faults are detected, these pins outputs L.
In the following table, X: Don't Care, H: High, L: Low, and Hiz: High Impedance.

Table 5.4 DIAG function (2-channel mode)

								Motor drive output			
Function	EN1	ENB1	EN2	ENB2	Is EN/ENB pulse input needed when DIAG is cleared?	DIAG1 pin	DIAG2 pin	OUT1	OUT2	OUT3	OUT4
Forward (Normal operation)	H	L	H	L	-	H	H	H	L	H	L
Reverse (Normal operation)	H	L	H	L	-	H	H	L	H	L	H
Short brake (Normal operation)	H	L	H	L	-	H	H	L/H	L/H	L/H	L/H
EN1 Disable	L	X	X	X	No	L	H/L	Hiz	Hiz	H/L/Hiz	H/L/Hiz
EN2 Disable	X	X	L	X	No	H/L	L	H/L/Hiz	H/L/Hiz	Hiz	Hiz
ENB1 Disable	X	H	X	X	No	L	H/L	Hiz	Hiz	H/L/Hiz	H/L/Hiz
ENB2 Disable	X	X	X	H	No	H/L	L	H/L/Hiz	H/L/Hiz	Hiz	Hiz
Sleep mode	X	L/H	X	L/H	-	H	H	Hiz	Hiz	Hiz	Hiz
When over-temperature is detected (TSD)	X	X	X	X	No	L	L	Hiz	Hiz	Hiz	Hiz
When Ch1 over-current is detected (ISD)	X	X	X	X	Yes	L	H/L	Hiz	Hiz	H/L/Hiz	H/L/Hiz
When Ch2 over-current is detected (ISD)	X	X	X	X	Yes	H/L	L	H/L/Hiz	H/L/Hiz	Hiz	Hiz
When VBAT under-voltage is detected	X	X	X	X	No	L	L	Hiz	Hiz	Hiz	Hiz
When VCC under-voltage is detected	X	X	X	X	No	L	L	Hiz	Hiz	Hiz	Hiz
When VCC under-voltage is detected (POR)	X	X	X	X	No	L	L	Hiz	Hiz	Hiz	Hiz
When Ch1 open load during operation is detected	X	X	X	X	No	L	H/L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz
When Ch2 open load during operation is detected	X	X	X	X	No	H/L	L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz
When Ch1 open load during non-operation is detected	H	L	X	X	No	L	H/L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz
When Ch2 open load during non-operation is detected	X	X	H	L	No	H/L	L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz
When initial/restarted diagnosis detects an error (Detection of VBAT/VCC under-voltage or over-temperature)	X	X	X	X	No	L	L	*1	*1	*1	*1
When Initial/restarted diagnosis detects an error (Detection of Ch1 over-current or open load during operation/non-operation)	X	X	X	X	No	L	H/L	*1	*1	*1	*1
When Initial/restarted diagnosis detects an error (Detection of Ch2 over-current or open load during operation/non-operation)	X	X	X	X	No	H/L	L	*1	*1	*1	*1
When initial/restarted diagnosis is attempted but it does not start (Detection of VBAT/VCC under-voltage or over-temperature)	X	X	X	X	No	L	L	Hiz	Hiz	Hiz	Hiz

Function	EN1	ENB1	EN2	ENB2	Is EN/ENB pulse input needed when DIAG is cleared?	DIAG1 pin	DIAG2 pin	Motor drive output			
								OUT1	OUT2	OUT3	OUT4
When initial/restarted diagnosis is attempted but it does not start (Detection of Ch1 over-current or open load during operation/non-operation)	X	X	X	X	No	L	H/L	Hiz	Hiz	*1	*1
When initial/restarted diagnosis is attempted but it does not start (Detection of Ch2 over-current or open load during operation/non-operation)	X	X	X	X	No	H/L	L	*1	*1	Hiz	Hiz
When SPI communication disruption is detected	X	X	X	X	No	L	L	*2	*2	*2	*2
When an SPI communication CRC error is detected	X	X	X	X	No	L	L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz
When a fault SPI communication SCLK clock count is detected	X	X	X	X	No	L	L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz
When a fault SPI communication address is detected	X	X	X	X	No	L	L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz

*1: Operation similar to Table 5.1 H-bridge motor function 1
*2: Operation specified in CONFIG1 DATA[8]

Table 5.5 DIAG function (Combined 2-channel mode)

Function	EN1	ENB1	EN2	ENB2	Is EN/ENB pulse input needed when DIAG is cleared?	DIAG1 pin	DIAG2 pin	Motor drive output			
								OUT1	OUT2	OUT3	OUT4
Forward (Normal operation)	H	L	H	L	-	H	H	H	H	L	L
Reverse (Normal operation)	H	L	H	L	-	H	H	L	L	H	H
Short brake (Normal operation)	H	L	H	L	-	H	H	L/H	L/H	L/H	L/H
EN1 and EN2 Disable	L	X	L	X	No	L	L	Hiz	Hiz	Hiz	Hiz
ENB1 and ENB2 Disable	X	H	X	H	No	L	L	Hiz	Hiz	Hiz	Hiz
Sleep mode	X	L/H	X	L/H	-	H	H	Hiz	Hiz	Hiz	Hiz
When over-temperature is detected (TSD)	X	X	X	X	No	L	L	Hiz	Hiz	Hiz	Hiz
When Ch1 over-current is detected (ISD)	X	X	X	X	Yes	L	H	Hiz	Hiz	Hiz	Hiz
When Ch2 over-current is detected (ISD)	X	X	X	X	Yes	H	L	Hiz	Hiz	Hiz	Hiz
When VBAT under-voltage is detected	X	X	X	X	No	L	L	Hiz	Hiz	Hiz	Hiz
When VCC under-voltage is detected	X	X	X	X	No	L	L	Hiz	Hiz	Hiz	Hiz
When VCC under-voltage is detected (POR)	X	X	X	X	No	L	L	Hiz	Hiz	Hiz	Hiz
When Ch1-Ch2 open load during operation is detected	X	X	X	X	No	L	L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz
When Ch1-Ch2 open load during non-operation is detected	H	L	H	L	No	L	L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz

Function	EN1	ENB1	EN2	ENB2	Is EN/ENB pulse input needed when DIAG is cleared?	DIAG1 pin	DIAG2 pin	Motor drive output			
								OUT1	OUT2	OUT3	OUT4
When initial/restarted diagnosis detects an error (Detection of VBAT/VCC under-voltage or over-temperature)	X	X	X	X	No	L	L	*1	*1	*1	*1
When Initial/restarted diagnosis detects an error (Detection of Ch1-Ch2 over-current or open load during operation/non-operation)	X	X	X	X	No	L	L	*1	*1	*1	*1
When initial/restarted diagnosis is attempted but it does not start (Detection of VBAT/VCC under-voltage or over-temperature)	X	X	X	X	No	L	L	Hiz	Hiz	Hiz	Hiz
When initial/restarted diagnosis is attempted but it does not start (Detection of Ch1-Ch2 over-current or open load during operation/non-operation)	X	X	X	X	No	L	L	Hiz	Hiz	Hiz	Hiz
When SPI communication disruption is detected	X	X	X	X	No	L	L	*2	*2	*2	*2
When an SPI communication CRC error is detected	X	X	X	X	No	L	L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz
When a fault SPI communication SCLK clock count is detected	X	X	X	X	No	L	L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz
When a fault SPI communication address is detected	X	X	X	X	No	L	L	H/L/Hiz	H/L/Hiz	H/L/Hiz	H/L/Hiz

*1: Operation similar to Table 5.2 H-bridge motor function 2

*2: Operation specified in CONFIG1 DATA[8]

Note: In combined 2-channel mode, externally short-circuit ISEL1/2, EN1/2, ENB1/2, OUT1/2, and OUT3/4.
However, EN2/ENB2 are effective as analog signals to control the output DMOS gates but ineffective as signals supplied to the logic circuit.

5.3. Current-limit control

This IC adopts a chopper-type current-limit control. When an event such as transient pulses due to high-speed throttle operation or a locked motor due to an immovable motor shaft causes a large current, the IC activates the current-limit control to protect the actuator and reduce the power dissipation. (An additional over-current protection circuit prepared in another block deals with a short-circuit to power supply or ground.)

The current-limit comparator is located on the low side. Higher threshold is defined as Ilim-H, and lower as Ilim-L. The Lo-side performs regeneration (Slow Decay).

A blanking time is set internally after which a current-limit control is activated. Ilim-H = 6.5 A (typ.) and Ilim-L = Ilim-H - 0.25 A (typ.)

Two current-limit thresholds are selectable for 16 combinations by SPI registers as following table.

<table>
<tr><td></td><td colspan="2">Ch1 (OUT1/OUT2)</td><td colspan="2">Ch2 (OUT3/OUT4)</td></tr>
<tr><td rowspan="10">2-channel mode
(to drive two motors)</td><td>Ilim-H</td><td>Ilim-L</td><td>Ilim-H</td><td>Ilim-L</td></tr>
<tr><td rowspan="2">6.5 A
(Initial value)</td><td>6.5 A - 0.25 A
(Initial value)</td><td rowspan="2">6.5 A
(Initial value)</td><td>6.5 A - 0.25 A
(Initial value)</td></tr>
<tr><td>6.5 A - 0.5 A</td><td>6.5 A - 0.5 A</td></tr>
<tr><td rowspan="2">4.6 A</td><td>4.6 A - 0.25 A
(Initial value)</td><td rowspan="2">6.5 A
(Initial value)</td><td>6.5 A - 0.25 A
(Initial value)</td></tr>
<tr><td>4.6 A - 0.5 A</td><td>6.5 A - 0.5 A</td></tr>
<tr><td rowspan="2">6.5 A
(Initial value)</td><td>6.5 A - 0.25 A
(Initial value)</td><td rowspan="2">4.6 A</td><td>4.6 A - 0.25 A
(Initial value)</td></tr>
<tr><td>6.5 A - 0.5 A</td><td>4.6 A - 0.5 A</td></tr>
<tr><td rowspan="2">4.6 A</td><td>4.6 A - 0.25 A
(Initial value)</td><td rowspan="2">4.6 A</td><td>4.6 A - 0.25 A
(Initial value)</td></tr>
<tr><td>4.6 A - 0.5 A</td><td>4.6 A - 0.5 A</td></tr>
</table>

In combined 2-channel mode, the following 4 combinations are selectable.

<table>
<tr><td></td><td colspan="2">Ch1 (OUT1/OUT2), Ch2 (OUT3/OUT4)</td><td colspan="2">Total</td></tr>
<tr><td rowspan="6">Combined 2-channel mode
(to drive one motor)</td><td>Ilim-H</td><td>Ilim-L</td><td>Ilim-H</td><td>Ilim-L</td></tr>
<tr><td rowspan="2">6.5 A
(Initial value)</td><td>6.5 A - 0.25 A
(Initial value)</td><td rowspan="2">13 A
(Initial value)</td><td>6.5 A - 0.5 A
(Initial value)</td></tr>
<tr><td>6.5 A - 0.5 A</td><td>6.5 A - 1.0 A</td></tr>
<tr><td rowspan="2">4.6 A</td><td>4.6 A - 0.25 A
(Initial value)</td><td rowspan="2">9.2 A</td><td>4.6 A - 0.5 A
(Initial value)</td></tr>
<tr><td>4.6 A - 0.5 A</td><td>4.6 A - 1.0 A</td></tr>
</table>

5.3.1. Current-limit control adjusted to temperature

When junction temperature Tj increases to Twar temperature (150°C to 174°C), the current-limit control circuit decreases the current-limit threshold to 2.5 A.
Ilim-L also decreases as with Ilim-H.

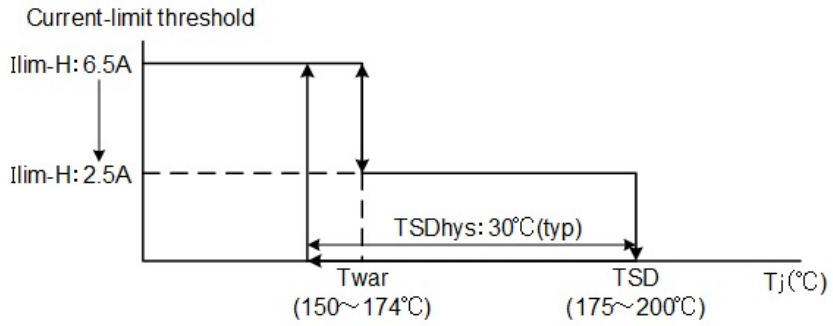


Figure 5.1 Current-limit control adjusted to temperature

Note: Part of the timing charts shown in this specification document may be omitted or simplified for explanatory purposes.

5.4. Hi-side current monitoring: CM pin

This IC monitors the current value (0 to 6A) flowing through the high side Nch of the H-bridge circuit anytime in active mode. 0.24% of the current is output from CM1(CM2) pin to be converted to voltage with an external resistor(220Ω) connected between CM1(CM2) and GND. The MCU can recognize the motor condition such as the motor rocked or the motor disconnected in active mode with the voltage generated at CM1(CM2) pin.

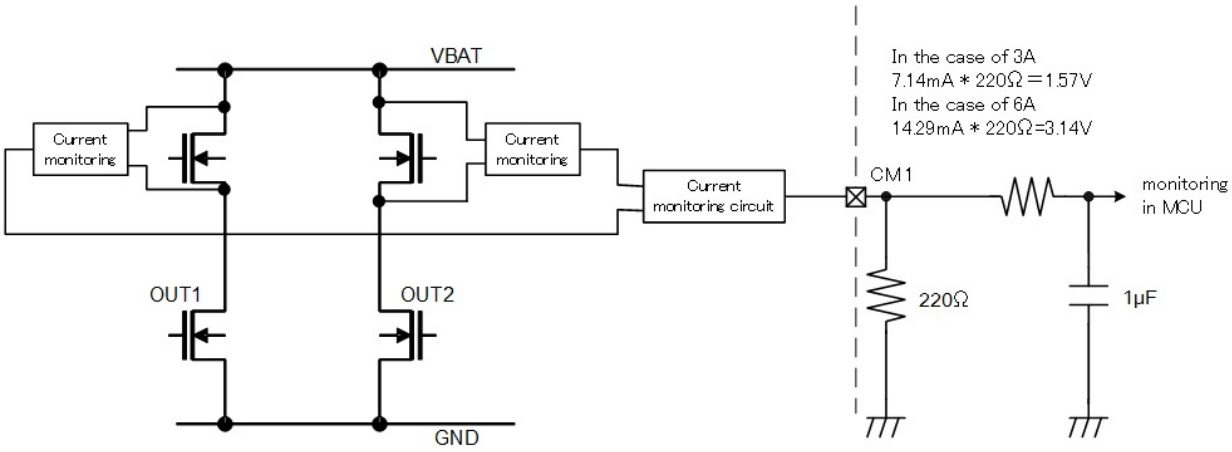


Figure 5.2 Hi-side current monitoring configuration

For open-load detection, connects an external resistor.
The current monitoring is enabled even when EN/ENB are disabled and the output is OFF. However, the monitoring is disabled in a sleep state (SLEEPB = L).

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

Note: The above resistor (220 Ω) is under the assumption that the MCU (ADC) power supply is 5 V.
If the MCU power supply is less than 5 V, adjust the resistor.
Be careful for the external resistor (220 Ω). Sufficient evaluation to the resistor is required, because the variation of resistance value causes the variation of output voltage.
Note: It is important to judge whether the external capacitor (1μF) should be connected by the purpose of system use.

5.5. Open load detection

This IC detects an open load when the motor connected between OUT1 and OUT2 is open. When detecting it, the IC changes the DIAG pin to L and performs a function operation to notify an SPI register that the load is open. As shown below, an open load can be detected under two environments (operation/non-operation).

5.5.1. Open load detection circuit during operation (output ON)

An open load is identified using the CM (current monitoring) function. So insert a resistor between the CM pin and GND.
When the motor is operating and the load current goes below the threshold, the open load detection circuit outputs an open detection signal.

5.5.2. Open load detection circuit during non-operation (output OFF)

After the initial diagnosis is completed, start the function of open load detection during non-operation using an SPI signal at any timing whenever the user considers it necessary.
Open load detection during non-operation detects an open load when the motor is stopped (braked or output OFF (Hiz) due to SPI control).
When the IC is enabled and the motor is stopped (braked or output OFF (Hiz) due to SPI control), execute detection operation by SPI communication.

5.5.3. Detection of short-circuit to power supply or ground during non-operation

The open load detection circuit shown above is also used to detect short-circuit to power supply or ground.
For detection, when a single Hi-side/Lo-side DMOS is turned ON, check the output voltage while monitoring the voltage of the other side.
Note that if the detection takes too much time, short-circuit to power supply or ground may cause over-current through the DMOS.

5.6. Sleep function

This IC has a sleep function. When the SLEEPB pin is L, the IC enters a sleep state, which reduces the power consumption.

5.7. SPI communication circuit

This IC incorporates an SPI communication circuit for bidirectional communication between this IC and an external MCU. This IC is the Slave and the external MCU is the Master in the communication.
Via SPI communication, this IC and the external MCU can transmit and receive various motor control settings, monitored various fault detection, and motor drive control (drive mode and PWM duty ratio).
Both parallel and daisy-chain connections can be used to connect this IC and the external MCU.

5.7.1. SPI communication operation

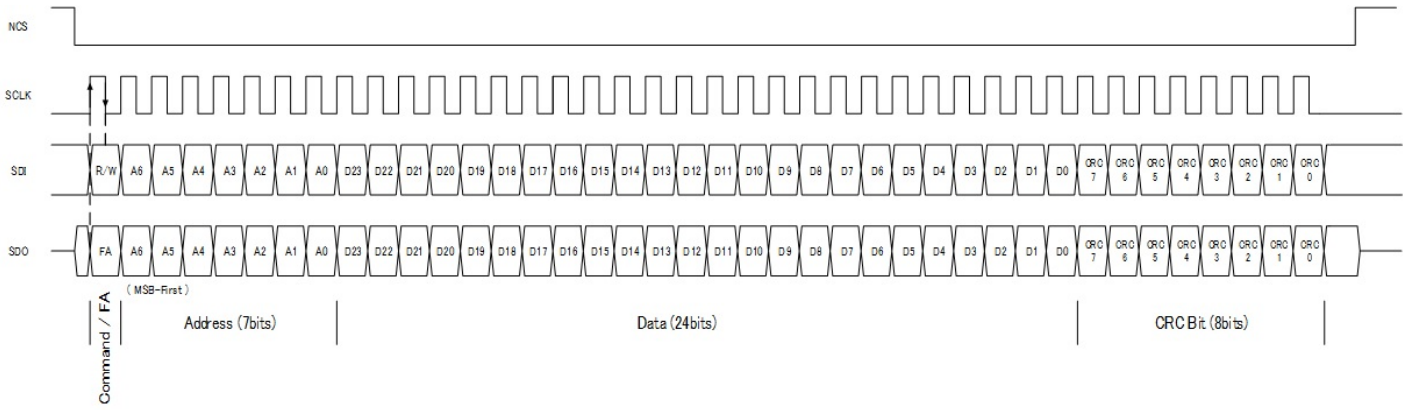


Figure 5.3 SPI communication format

NCS is a chip-select input. When NCS is Lo, communication with an external MCU is enabled (Lo active). The IC determines the received command at the rise edge of NCS. When NCS is Lo, serial data are transmitted and received, synchronized with SCLK. When NCS is Hi, SDO is in a high-impedance (Hi-Z) state.

SCLK is a clock input to synchronize the communication between this IC and an external MCU. The external MCU, synchronizing with the rise edge of SCLK, outputs transmitted data to SDI of this IC. This IC, synchronizing with the fall edge of SCLK, reads the received data. On the other hand, this IC, synchronizing with the rise edge of SCLK, outputs transmission data from SDO to the external MCU or the next IC in the daisy chain. The external MCU or the next IC in the daisy chain, synchronizing with the fall edge of SCLK, reads the received data.

SDI is serial data received by this IC. SDI receives serial data in the order from MSB to LSB. SDI reads data, synchronizing with the fall edge of SCLK. The external MCU outputs transmitted data, synchronizing with the rise edge of SCLK.

SDO is serial data transmitted by this IC. SDO transmits serial data in the order from MSB to LSB. SDO outputs data, synchronizing with the rise edge of SCLK. When NCS is Hi, SDO is in a high-impedance (Hi-Z) state.

As shown in Figure 5.3, the length of serial data is 40 bits, which are defined as 1 frame. There are two communication operations: READ and WRITE. The external MCU selects READ/WRITE using the command bit (R/W bit) of serial data.

For parallel connection between the external MCU and this IC, NCS needs to be turned to Lo for each frame. For daisy-chain connection, the MCU can consecutively communicate with multiple ICs (up to 8) after turning NCS to Lo. For example, if 8 ICs are connected in a daisy chain, 8 frames (40 bits * 8 = 320 bits) can be consecutively communicated while NCS is Lo.

5.7.2. SPI connection method

5.7.2.1. SPI parallel connection

SPI parallel connection

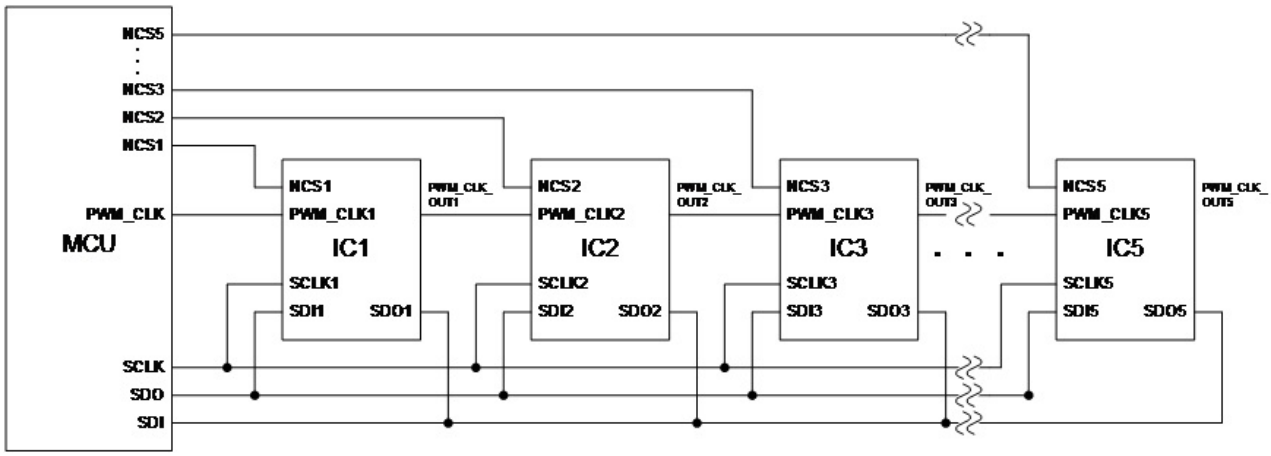


Figure 5.4 Example SPI parallel connection (5 ICs are connected.)

In the example SPI parallel connection (Figure 5.4), a communication clock (SCLK), a data output (SDO), and a data input (SDI) are connected in parallel. The external MCU (Master) assigns an independent chip-select signal to each IC (Slave: IC1 to IC5) to enable individual access. Since all ICs (Slave: IC1 to IC5) share one communication clock (SCLK) and two data lines (SDO and SDI), only the IC (Slave) whose chip-select signal (NCS) is Lo receives the communication clock and the data, and replies.

5.7.2.2. SPI daisy-chain connection

SPI daisy-chain connection

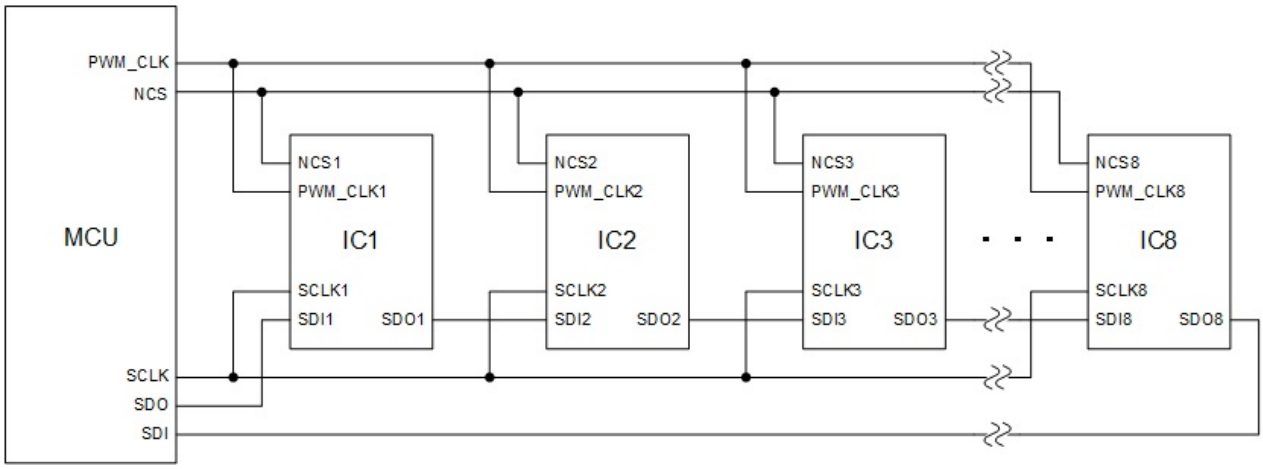


Figure 5.5 Example SPI daisy-chain connection (8 ICs are connected.)

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

A single chip-select signal (NCS) from the external MCU (Master) controls the NCS inputs of all ICs (Slave). All ICs (Slave) operate with the same clock signal. Only the first IC (Slave: IC1) connected to the daisy chain directly receives data from the external MCU (Master). Another IC (Slave: IC2 to IC8) receives its input data into SDI from a IC's SDO output of connecting at the daisy chain immediately before the IC.

In the example SPI daisy-chain connection (Figure 5.5), IC1 receives data directly from the external MCU while the chip-select signal (NCS) is Lo, and captures the data into an internal shift register in IC1. While the external MCU keeps NCS Lo, the data is propagated to the SDO1 output of IC1 as it is. Since SDO1 of IC1 is connected to SDI2 of IC2, the output data from SDO1 of IC1 is sent to an internal shift register in IC2. While IC2 is receiving data from IC1, the external MCU can simultaneously transmit another command to IC1. The new command overwrites the previous data in the shift register of IC1. While NCS is Lo, until each of IC1 to IC8 receives a command directed to it, sets of data propagate throughout the daisy-chain connection. A command stored in the shift register of each IC is executed at the rise edge of NCS.
If 8 ICs are connected in a daisy chain, the Lo period of NCS is a duration of 8 frames.

5.7.3. Motor control function by SPI communication

When the ISEL1/ISEL2 pin is set to H (connected to VCC) to set SPI motor drive mode, motor control with SPI communication is enabled.
The settings of the ISEL1 and ISEl2 pins (H or L) can be read from the STATUS1 register, whose address is ADR[38:32] = 0x01.

5.7.3.1. Operation when ISEL1/ISEL2 = H

- Motor control with SPI communication: Enabled
  The data written in the CONFIG3/4/5/6 registers, whose addresses are ADR[38:32] = 0x06, 0x07, 0x08, and 0x09, drive the motor.
  See Table 5.6.
- PWM1/2/3/4 pin input: Disabled
  No input signals are accepted.
- Clock for output Dr circuit (IC internal circuit):
  Select the externally input clock (input to the PWM_CLK pin). Use an internal clock for various fault detection circuits to avoid a filtering time variation, which an external clock may cause.
- PWM_CLK pin input clock fault detection: Enabled
  When the PWM_CLK pin input clock is stopped, the IC alternatively uses an internal clock. SPI notifies the MCU when the PWM_CLK pin input clock is fault. When using an internal clock instead of an external clock, the IC drives the outputs (OUT1/2 and OUT3/4) with a 2 MHz clock, which is generated by dividing the original oscillation 16 MHz by 8, as retaining the CONFIG3/4/5/6 register settings.

5.7.3.2. Operation when ISEL1/ISEL2 = L

- Motor control with SPI communication: Disabled
  The data written in the CONFIG3/4/5/6 registers, whose addresses are ADR[38:32] = 0x06, 0x07, 0x08, and 0x09, are ineffective.
  Data from a WRITE attempt is discarded to prevent overwrite.
  The initial value (all "0") is retained.
- PWM1/2/3/4 pin input: Enabled
  The IC drives the outputs (OUT1/2 and OUT3/4) according to the input signals.
- Clock for output Dr circuit (IC internal circuit): Disabled
  The externally input clock (input to the PWM_CLK pin) is not used.
- PWM_CLK pin input clock fault detection: Enabled
  PWM_CLK pin input clock suspension is monitored. However, the PWM_CLK pin input clock fault is ignored.
  When ISEL1/ISEL2 = L, connect the PWM_CLK pin to GND.

5.7.3.3. External clock supply by PWM_CLK pin

An external MCU supplies a reference clock of the PWM frequency to the PWM_CLK pin.
Each IC connected with SPI communication (parallel or daisy chain) generates its PWM control clock frequency from the reference clock of the PWM frequency externally supplied to the PWM_CLK pin.
The PWM control clock frequency of each IC (for Ch1 and Ch2) can be selected with the CONFIG register setting using SPI communication.

5.7.3.4. Motor operation setting with SPI communication

Write the settings of motor operation (Forward/Reverse/Brake/output OFF (Hiz)), drive frequency (drive cycle period), and Duty-ON period (PWM Duty-ON interval) in address ADR[38:32] = 0x08 and 0x09.
Setting CONFIG5/6 data: DATA[31:30] selects a motor operation.
Setting CONFIG5/6 data: DATA[29:19] specifies a PWM drive cycle period.
Setting CONFIG5/6 data: DATA[18:8] specifies a Duty-ON period within the PWM drive cycle period set by data DATA[29:19]. The period is defined as a PWM Duty-ON interval.

Write a setting whether low- or high-side regeneration is applied during PWM Duty-OFF interval in address ADR[6:0] = 0x04/0x05.
Setting CONFIG1/2 data: DATA[20] selects either low- or high-side regeneration during PWM Duty-OFF interval.

- PWM drive frequency (drive cycle period) fpwm is calculated as follows:

fpwm = fdiv / Drive frequency (drive cycle period) setting (register value) (5.1)

fdiv: Base frequency
= External input clock frequency * Base frequency register setting (frequency division ratio)
Base frequency register: CONFIG3/4 DATA[31:30]
Drive frequency (drive cycle period) setting register: CONFIG5/6 DATA[29:19]

- PWM Duty-ON interval is calculated as follows:

PWM Duty-ON interval
= Duty-ON period setting (register value) / Drive frequency setting (register value + 1) (5.2)

Set the registers so that:
Duty-ON period setting register value ≤ Drive frequency setting register value.
1) If Duty-ON period setting register value = Drive frequency setting register value, PWM Duty-ON interval is 100%.
2) If Duty-ON period setting register value > Drive frequency setting register value, PWM Duty-ON interval is still 100%.
3) If Duty-ON period setting register value = 0, PWM Duty-ON interval is 0%.

5.7.4. SPI register map

Table 5.6 SPI register map

NAME	R/W	Address	Data bit																						CRC bit
	[39]	[38:32]	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7:0]
STATUS1	R (1WC)	0x01	ISEL1 pin state detection (Automatic recovery)	ISEL2 pin state detection (Automatic recovery)	OSEL1/OSEL2 pin state detection (Automatic recovery)		Initial/restarted diagnosis error (VBAT under-voltage)	Initial/restarted diagnosis start fault (VBAT under-voltage)	Initial/restarted diagnosis error (VCC under-voltage)	Initial/restarted diagnosis start fault (VCC under-voltage)	Initial/restarted diagnosis error (over-temperature detection)	Initial/restarted diagnosis start fault (over-temperature detection)	Initial/restarted diagnosis Ch1 diagnosis result	Initial/restarted diagnosis Ch2 diagnosis result	Over-temperature detection (Automatic recovery)	Ch1 open load detection during non-operation	Ch2 open load detection during non-operation	SPI communication disruption detection (1WC_Flag)	SPI communication CRC error detection (1WC_Flag)	SPI communication SCLK clock count fault detection (1WC_Flag)	SPI communication Fault address detection (1WC_Flag)	External clock fault detection (PWM_CLK_I input) (1WC_Flag)	VBAT under-voltage detection (Automatic recovery)	VCC under-voltage detection (1WC_Flag)	Ch1 state *1 (Automatic recovery)	Ch2 state *1 (Automatic recovery)	CRC calculation result of bit[39:8]
STATUS2	R (1WC)	0x02	-	-	-	-	Initial/restarted diagnosis error (Ch1 Over-current detection)	Initial/restarted diagnosis start fault (Ch1 over-current detection)	-	-	Initial/restarted diagnosis error (Ch1 open load detection during operation)	Initial/restarted diagnosis start fault (Ch1 open load detection during operation)	Initial/restarted diagnosis error (Ch1 open load detection during non-operation)	Initial/restarted diagnosis start fault (Ch1 open load detection during non-operation)	OUT1 Hi-side over-current detection (short-circuit to ground) (Automatic recovery)	OUT2 Hi-side over-current detection (short-circuit to ground) (Automatic recovery)	OUT1 Lo-side over-current detection (short-circuit to power supply) (Automatic recovery)	OUT2 Lo-side over-current detection (short-circuit to power supply) (Automatic recovery)	Ch1 open load detection during operation (Automatic recovery)	-	-	-	-	-	-	-	CRC calculation result of bit[39:8]
STATUS3	R (1WC)	0x03	-	-	-	-	Initial/restarted diagnosis error (Ch2 Over-current detection)	Initial/restarted diagnosis start fault (Ch2 over-current detection)	-	-	Initial/restarted diagnosis error (Ch2 open load detection during operation)	Initial/restarted diagnosis start fault (Ch2 open load detection during operation)	Initial/restarted diagnosis error (Ch2 open load detection during non-operation)	Initial/restarted diagnosis start fault (Ch2 open load detection during non-operation)	OUT3 Hi-side over-current detection (short-circuit to ground) (Automatic recovery)	OUT4 Hi-side over-current detection (short-circuit to ground) (Automatic recovery)	OUT3 Lo-side over-current detection (short-circuit to power supply) (Automatic recovery)	OUT4 Lo-side over-current detection (short-circuit to power supply) (Automatic recovery)	Ch2 open load detection during operation (Automatic recovery)	-	-	-	-	-	-	-	CRC calculation result of bit[39:8]

R: Read, R (1WC): Flag clear with "1" write, W: Write

*1: Even in combined 2-channel mode (LARGE mode), a fault flag is set in the channel that detects the fault.

NAME	R/W [39]	Address [38:32]	Data bit [31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	CRC bit [7:0]
CONFIG1	R/W	0x04	-	-	-	-	-	-	-	-	-	Ch1: Open load during non-operation Detection time setting		Ch1: PWM Duty-OFF interval Low- or high-side regeneration setting	VBAT under-voltage cancellation delay time (Common to Ch1 and Ch2) (Digital filter)	Ch1: Current limit Threshold: Upper limit setting	Ch1 (OUT1/2) Current limit Threshold: Lower limit setting	Ch1: Open load detection during operation Threshold setting		Ch1 SR mode SR2, SR1, SR0			Ch1: Over-current detection mode (latched or automatic recovery)	SPI communication disruption determination threshold setting (Common to Ch1 and Ch2)		Operation mode setting when SPI communication is disrupted (Common to Ch1 and Ch2)	CRC calculation result of bit[39:8]
CONFIG2	R/W	0x05	-	-	-	-	-	-	-	-	-	Ch2: Open load during non-operation Detection time setting		Ch2: PWM Duty-OFF interval Low- or high-side regeneration setting	-	Ch2: Current limit Threshold: Upper limit setting	Ch2 (OUT3/4) Current limit Threshold: Lower limit setting	Ch2: Open load detection during operation Threshold setting		Ch2 SR mode SR2, SR1, SR0			Ch2: Over-current detection mode (latched or automatic recovery)	-	-	-	CRC calculation result of bit[39:8]
CONFIG3	R/W	0x06	Ch1: Base frequency setting		-	-	-	-	-	-	-	-	-	-	-	Ch1: ON delay time setting (Counter value: 0 to 2047)											CRC calculation result of bit[39:8]
CONFIG4	R/W	0x07	Ch2: Base frequency setting		-	-	-	-	-	-	-	-	-	-	-	Ch2: ON delay time setting (Counter value: 0 to 2047)											CRC calculation result of bit[39:8]

R: Read, R (1WC): Flag clear with "1" write, W: Write

NAME	R/W [39]	Address [38:32]	Data bit [31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	CRC bit [7:0]
CONFIG5	R/W	0x08	Ch1: Motor operation setting (Forward/Reverse/Brake/output OFF (Hiz))		Ch1: Drive frequency setting (Counter value: 0 to 2047)											Ch1: Duty-ON period setting (PWM Duty) (Counter value: 0 to 2047)										CRC calculation result of bit[39:8]
CONFIG6	R/W	0x09	Ch2: Motor operation setting (Forward/Reverse/Brake/output OFF (Hiz))		Ch2: Drive frequency setting (Counter value: 0 to 2047)											Ch2: Duty-ON period setting (PWM Duty) (Counter value: 0 to 2047)										CRC calculation result of bit[39:8]
CONFIG7	W	0x0A	Ch1: Over-current detection Output OFF cancellation in short-circuit to power supply or ground	Ch1: Open load diagnosis execution during non-operation	Ch1: CONFIG3/CONFIG5 setting update	Ch2: Over-current detection Output OFF cancellation in short-circuit to power supply or ground	Ch2: Open load diagnosis execution during non-operation	Ch2: CONFIG4/CONFIG6 setting update	OUT1: Over-current detection Output OFF cancellation in short-circuit to power supply or ground (Effective only in Half mode)	OUT2: Over-current detection Output OFF cancellation in short-circuit to power supply or ground (Effective only in Half mode)	OUT3: Over-current detection Output OFF cancellation in short-circuit to power supply or ground (Effective only in Half mode)	OUT4: Over-current detection Output OFF cancellation in short-circuit to power supply or ground (Effective only in Half mode)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CRC calculation result of bit[39:8]

R: Read, R (1WC): Flag clear with "1" write, W: Write

5.8. Power supply monitoring function

This IC has a power supply monitoring function.

5.8.1. VBAT under-voltage detection circuit

・When VBAT voltage decreases below the under-voltage detection threshold, OUT1/2 and OUT3/4 goes OFF (Hiz state).
The IC has a filter (TVBAT_uv: approximately 2.0 µs (typ.)) to avoid chattering.
Even while an H-bridge circuit is OFF (Hiz) due to VBAT under-voltage detection, if VCC voltage is above the VCC under-voltage POR voltage, logic circuits can operate.

5.8.2. VCC under-voltage detection circuit

When VCC voltage decreases below the under-voltage detection threshold, OUT1/2 and OUT3/4 goes OFF (Hiz state). The IC has a filter (2.5 ms (typ.)) to avoid chattering.
The fault bit of SPI latches a flag that VCC under-voltage is detected.
The logic circuit is reset if VCC voltage is below VCCRHL (3.07 V (typ.)).
Moreover, in order to prevent chattering, a filter (13.0µs(typ.)) is built in.

5.9. Over-temperature detection circuit

This IC has an over-temperature detection circuit. At a temperature above TSD, the IC turns the motor drive output OUT1/2 and OUT3/4 to Hiz to protect the IC. Simultaneously, the DIAG pin outputs L.
When the temperature decreases below to the TSD – TSDhys by operation of over-temperature detection circuit, normal operation automatically resumes.
(The output automatically resumes from Hiz when the temperature is below TSD - TSDhys.)
The DIAG pin output automatically resumes from L output when the temperature is below TSD - TSDhys.

Note: According to the absolute maximum ratings of this product, the guaranteed range of storage temperature is 150°C (max). If the IC is stored or used under a condition exceeding this temperature, subsequent normal operations are not guaranteed. Moreover, it may cause smoke and/or ignition. Under any circumstances, do not store or use this IC under a condition exceeding this temperature. Although this IC incorporates an over-temperature detection function as shown above, the function is not intended to suppress the temperature of the IC below the over-temperature detection shutdown temperature (TSD), nor work within the guaranteed operation range. This function should be considered as an auxiliary function. (This function is not individually tested under a real temperature at the shipment. A test function simulates the detection circuit operation.)

5.10. Circuit to detect over-current caused by short-circuit to power supply or ground, or short-circuited load

This IC incorporates over-current detection circuits for Hi- and Lo-side drivers of the motor drive outputs.
When a motor drive output pin is short-circuited to power supply or ground, or a load is short circuited, if the current exceeds the over-current threshold (11 A (typ.)), the over-current detection circuit operates to turn the motor drive output OFF. All Hi- and Lo-side drivers of OUT1/2 and OUT3/4 pins turn OFF.
Simultaneously, the DIAG pin outputs L.
The over-current detection function has two modes: after over-current is detected, a mode turns the output OFF and the other mode recovers automatically. Use an SPI setting to select the modes. However, in Half-bridge, the automatic recovery mode is disabled. Only the Half-bridge output where the over-current arises is latched to OFF.

5.11. Initial diagnosis

The IC has an initial diagnosis function to check the operation of comparators for power-supply monitoring, over-temperature detection, over-current detection, and open load detection during operation/non-operation in advance.

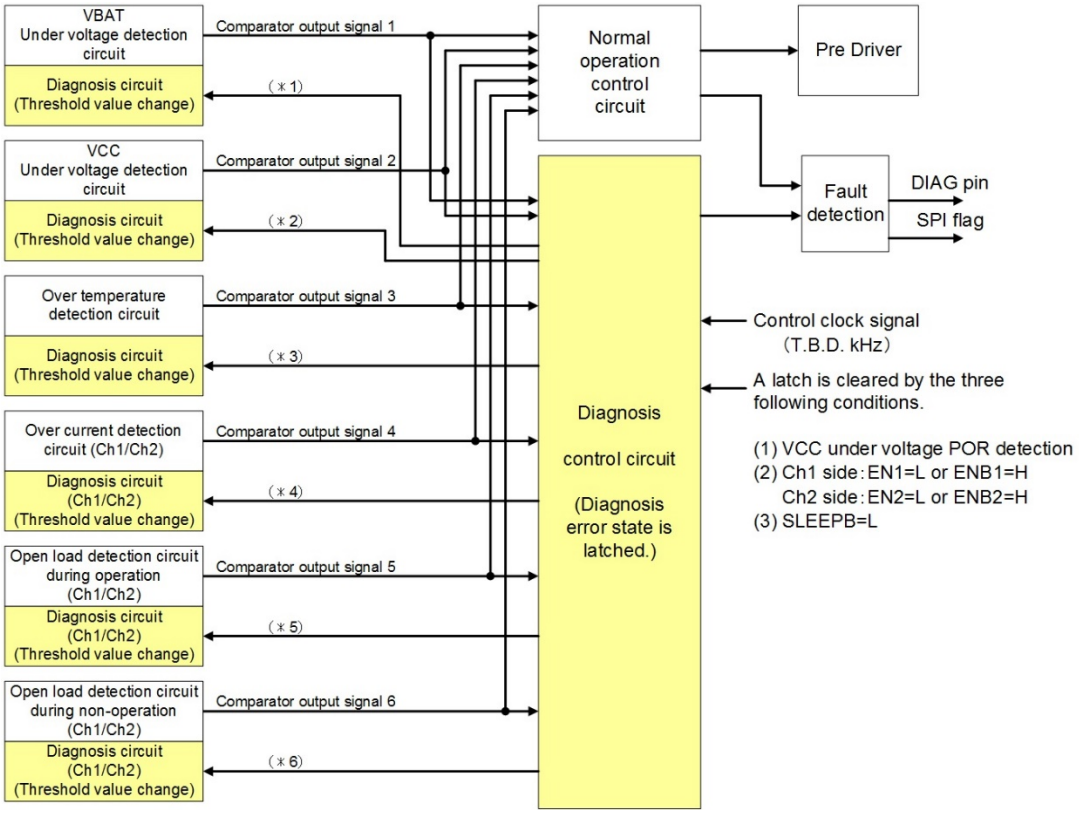


Figure 5.6 Initial diagnosis block diagram

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

*1 to 6: Initial diagnosis/ normal operation threshold value switching signal
H: Threshold value for initial diagnosis: With normal voltage and current, VBAT, VCC, over-temperature, over-current, and open load during operation/non-operation are "detected".
L: Threshold value for normal operation: With normal voltage and current, VBAT, VCC, over-temperature, over-current, and open load during operation/non-operation are "undetected".

◆Table 5.7 Operation summary of initial diagnosis

Condition	Each detector	Start-after POR formation conditions	The state where it does not detect Test 1 (Normal threshold)	The state where it does not detect Test 2 (A threshold is changed)	The state where it does not detect Test 3 (Normal threshold)	Diagnostic result	Under diagnostic operation		After termination of initial diagnosis		memo
							DIAG1, DIAG2 PIN	OUT1/2, OUT3/4 PIN	DIAG1, DIAG2 PIN	OUT1/2, OUT3/4 PIN	
1	CP voltage starting	○	–	–	–	Normal	L	Hiz	H	Output Function	
	VBAT under voltage	○	○	○	○						
	VCC under voltage	○	○	○	○						
	Over temperature	○	○	○	○						
	Over current	○	○	○	○						
	Open load during operation	○	○	○	○						
	Open load during non-operation	○	○	○	○						
2	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	In the case of NG, it is also at any 1 condition	○	○						
	VCC under voltage	○		○	○						
	Over temperature	○		○	○						
	Over current	○		○	○						
	Open load during operation	○		○	○						
	Open load during non-operation	○		○	○						
3	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	○	In the case of NG, it is also at any 1 condition	○						
	VCC under voltage	○	○		○						
	Over temperature	○	○		○						
	Over current	○	○		○						
	Open load during operation	○	○		○						
	Open load during non-operation	○	○		○						
4	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	○	○	In the case of NG, it is also at any 1 condition						
	VCC under voltage	○	○	○							
	Over temperature	○	○	○							
	Over current	○	○	○							
	Open load during operation	○	○	○							
	Open load during non-operation	○	○	○							
5	CP voltage starting	When at least one condition continues the state where it detects	–	–	–	Fault	L	Hiz	L	Hiz	Initial diagnosis does not start.
	VBAT under voltage		–	–	–						
	VCC under voltage		–	–	–						
	Over temperature		–	–	–						
	Over current		–	–	–						
	Open load during operation		–	–	–						
	Open load during non-operation		–	–	–						

Note: The CP voltage rise detection circuit is used as a condition for startup but not diagnosed.

Note: In case 5, the IC keeps waiting until six detection circuits output normal values (undetected state). At the timing when they output normal values, initial diagnosis starts and lasts for 57 µs (if 32 µs have elapsed after POR is canceled).

Note: In Half mode, open load detection circuits during operation/non-operation are not diagnosed.

Note: When VBAT voltage is in the range of VBAT under-voltage detecting voltage - VBAT under-voltage cancellation voltage, initial diagnosis is NG. Since DAIG output = L and initial-diagnosis NG (fault flag: "1") of STATUS1 register of SPI is output, set the VBAT voltage as the voltage more than VBAT under-voltage cancellation voltage.

Note: "-" indicates that no test (diagnosis) is applied.

◆Table 5.8 Operation summary of restarted diagnosis

Condition	Each detector	Initial diagnositic restart formation conditions	The state where it does not detect Test 1 (Normal threshold)	The state where it does not detect Test 2 (A threshold is changed)	The state where it does not detect Test 3 (Normal threshold)	Diagnostic result	Under diagnostic operation		After termination of a restart		memo
							DIAG1, DIAG2 PIN	OUT1/2, OUT3/4 PIN	DIAG1, DIAG2 PIN	OUT1/2, OUT3/4 PIN	
1	CP voltage starting	○	–	–	–	Normal	L	Hiz	H	Output Function	
	VBAT under voltage	○	○	○	○						
	VCC under voltage	○	○	○	○						
	Over temperature	○	○	○	○						
	Over current	○	○	○	○						
	Open load during operation	○	○	○	○						
	Open load during non-operation	○	○	○	○						
2	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	–	–	–						
	VCC under voltage	○	–	–	–						
	Over temperature	○	–	–	–						
	Over current	○	In the case of NG, it is also at any 1 condition	○	○						
	Open load during operation	○		○	○						
	Open load during non-operation	○		○	○						
3	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	–	–	–						
	VCC under voltage	○	–	–	–						
	Over temperature	○	–	–	–						
	Over current	○	○	In the case of NG, it is also at any 1 condition	○						
	Open load during operation	○	○		○						
	Open load during non-operation	○	○		○						
4	CP voltage starting	○	–	–	–	Fault	L	Hiz	L	Output Function	
	VBAT under voltage	○	–	–	–						
	VCC under voltage	○	–	–	–						
	Over temperature	○	–	–	–						
	Over current	○	○	○	In the case of NG, it is also at any 1 condition						
	Open load during operation	○	○	○							
	Open load during non-operation	○	○	○							
5	CP voltage starting	When at least one condition continues the state where it detects	–	–	–	Fault	L	Hiz	L	Hiz	Diagnosis does not restart.
	VBAT under voltage		–	–	–						
	VCC under voltage		–	–	–						
	Over temperature		–	–	–						
	Over current		–	–	–						
	Open load during operation		–	–	–						
	Open load during non-operation		–	–	–						

Note: The CP voltage rise detection circuit is used as a condition for restart but not diagnosed.
Note: In case 5, the IC keeps waiting until six detection circuits output normal values (undetected state). At the timing when they output normal values, restarted diagnosis starts and lasts for 57 µs (if 32 µs have elapsed after EN/ENB are disabled).
Note: "-" indicates that no test (diagnosis) is applied.
Note: The diagnosis does not work if VCC is below the under-voltage POR detection voltage.
Note: In Half mode, open load detection circuits during operation/non-operation are not diagnosed.

When the EN or ENB signal sets a Disable state, diagnosis restarts.

6. Absolute maximum ratings

Table 6.1 Absolute maximum ratings

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applicable pin	Condition	Rating	Unit
Power supply voltage 1	VBAT	VBAT	DC	-0.3 to +28.0	V
Power supply voltage 2	VBAT	VBAT	Transient: 0.5 s	-0.3 to +40.0 (*5)	V
Power supply voltage 3	VCC VDD VDDIO	VCC VDD VDDIO	DC (*3)	-0.3 to +6.0 (*6)	V
Input voltage 1	VIN	PWM1, PWM2, PWM3, PWM4, EN1, ENB1, EN2, ENB2, ISEL1, ISEL2, SDI, NCS, SCLK, SCLK, PWM_CLK, SLEEPB	DC	-0.3 to VCC, VDD, VDDIO+VF and VCC, VDD, VDDIO+VF ≤ +6.0 (*6)	V
Input voltage 2	VIN	OSEL1, OSEL2	DC	-0.3 to VCC, VDD, VDDIO+VF and VCC, VDD, VDDIO+VF ≤ +6.0 (*6)	V
Output voltage 1	VOUT	DIAG1, DIAG2	DC	-0.3 to +6.0 (*6)	V
Output voltage 2	VOUT	CM1, CM2	DC	-0.3 to VCC	V
Output voltage 3	VOUT	SDO	DC	-0.3 to VCC, VDD, VDDIO+VF and VCC, VDD, VDDIO+VF ≤ +6.0 (*6)	V
Output voltage 4	VOUT	OUT1, OUT2, OUT3, OUT4	DC (*4)	-VF to VBAT+VF and VBAT+VF ≤ +40.0 (*5)	V
Output voltage 5	VOUT	OUT1, OUT2, OUT3, OUT4	DC, VBAT-OUT1/2, (*4)	-VF to +40.0	V
Output current 1	IOUT	OUT1, OUT2, OUT3, OUT4	(*2)	Over-current detection value	A
Output current 2	IOUT	DIAG1, DIAG2	DC	+2.5	mA
Output current 3	IOUT	CM1, CM2	DC	-25.0	mA
Output current 4	IOUT	SDO	DC	3.0	mA
Storage temperature	Tstg	-	-	-55 to +150	°C
Lead temperature and time	Tsol	-	Manual soldering	260 (10 s)	
Permissible power dissipation	PD	-	-	TBD	W

Note: Current flowing into this IC is indicated as "+" and that flowing out as "-".

(*1) Including voltage caused by counter electromotive force, do not exceed the maximum ratings.
Absolute maximum ratings
The absolute maximum ratings are a set of ratings that must not be exceeded, even for a moment. Exceeding the rating(s) may cause the IC breakdown, deterioration, or damage, and may damage other devices. Regardless of the operating conditions, design your system so that the maximum ratings are never exceeded. Use the IC within the specified operation range.
(*2) When using the IC with continuous output current, to ensure that the junction temperature is within 150°C, carefully review and evaluate your board thermal design.
(*3) Use the ECU to generate the 5 V power supply for VCC. To apply the voltage to VCC, avoid various surges applied to the ECU connector.
(*4) The assumed VF value is voltage generated by regeneration current flowing through the body diode of DMOS output after the load is short-circuited and the output goes OFF.
(*5) Voltage difference between PGND and VBAT must be within 40 V.
(*6) Voltage difference between AGND and VCC must be within 6 V.

7. Operation range

7.1. Power supply

Three power supplies (VBAT, VCC, and VDDIO) are externally supplied to this IC
(1) VBAT power supply
Connect a battery power supply to VBAT, which is used for motor drive output.
The IC has a function to detect VBAT under-voltage.
(2) VCC power supply
Externally supply 5 V to VCC, which is used as a power supply for digital I/O in the IC.
VCC is also used as a power supply for internal analog circuits, which is used for various monitoring.
The IC has a monitoring function to detect VCC under-voltage.
(3) VDDIO power supply
Externally supply the same power supply as the I/O power supply of the MCU to VDDIO, which is used as a power supply for the digital I/O of the SPI communication circuit in the IC.
The IC has no function to monitor VDDIO power supply.

Table 7.1 Operation range

Item	Symbol	Rating	Unit	Remarks
Power supply voltage 1	VBAT	4.5 to 28.0	V	**However, until VBAT or VCC goes below each under-voltage detection voltage,** the motor functions.
Power supply voltage 2	VCC	4.5 to 5.5	V	**However, until VBAT or VCC goes below each under-voltage detection voltage,** the motor functions.
Power supply voltage 3	VDDIO	3.0 to 5.5	V	-
Operation temperature	Tj	-40 to 150	°C	-

Table 7.2 Power supply slew rate

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 V to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Power supply slew rate	VBSLEW	VBAT, VCC, VDD, VDDIO		-2	-	2	V/μs

8. Electrical characteristics

8.1. Input circuit

Table 8.1 Input circuit electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 V to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Input voltage	VIH1	PWM1/PWM2/ PWM3/PWM4, EN1/ENB1/EN 2/ENB2, ISEL1/ISEL2, PWM_CLK, SLEEPB, OSEL1/OSEL2		2.0	-	VCC	V
	VIL1			-0.3	-	0.8	V
	Vhys1			-	0.35	-	V
Input current	IIH1	PWM1/PWM2/ PWM3/PWM4, EN1/EN2/ ISEL1/ISEL2, PWM_CLK, SLEEPB, OSEL1/OSEL2	VIN = VCC = 5 V	-	50	-	µA
	IIH2	ENB1/ENB2		-5	-	5	µA
	IIL1	ENB1/ENB2	VIN = GND	-	-14	-	µA
	IIL2	PWM1/PWM2/ PWM3/PWM4, EN1/EN2/ ISEL1/ISEL2, PWM_CLK, SLEEPB, OSEL1/OSEL2		-5	-	5	µA
Sleep start time	tsleep (on)	SLEEPB		-	2.3	-	ms
Sleep cancellation time	tsleep (off)	SLEEPB		10	-	50	µs
PWM input maximum frequency	PWMMAX	PWM1/PWM2 PWM3/PWM4		-	-	20	kHz
EN/ENB logic determination time	TEN_ENB	EN1, ENB1 EN2, ENB2	Logic determination time when the logic formed by the EN1/2 and ENB1/2 pins is changed.	-	-	5.0	µs
Input pin noise filter	VI (noise)	EN1, ENB1, EN2, ENB2,		-	(0.5)	-	µs
Current consumption	ICC	VCC	VCC = 5 V	-	2.9	-	mA
	ICC (sleep)	VCC	VCC = 5 V, Iout=0A, Sleep mode	-	-	10	µA
	IDDIO	VDDIO	VDDIO = 5 V	-	-	1	mA
	IBAT	VBAT	VBAT = 14 V	-	1.0	-	mA
	IBAT (sleep)	VBAT	VBAT = 14V, Iout=0A, Sleep mode	-	-	30	µA

Note: PWM1/2/3/4 have internal pull-down resistors.

Note: EN1/2 have internal pull-down resistors and ENB1/2 pull-up resistors.

8.2. Power supply monitoring function

Table 8.2 Power supply monitoring function electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 V to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
VBAT under-voltage detection voltage	VBATRSTL	VBAT		-	3.75	-	V
VBAT under-voltage cancellation voltage	VBATRSTH	VBAT		-	4.25	-	V
VCC under-voltage detection voltage	VCCHL	VCC		-	3.5	-	V
VCC under-voltage POR detection voltage	VCCRHL	VCC		-	3.07	-	V

8.3. Motor drive output circuit

Table 8.3 Motor drive output circuit electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 V to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
H-bridge output ON-resistance (Hi Side + Lo Side)	Ron (H + L)	OUT1, OUT2, OUT3, OUT4	Tj = +25°C Iout = 3 A, VBAT = 8 V	-	142	-	mΩ
Output leak current	I outleak	OUT1, OUT2, OUT3, OUT4	OUT1/2 OFF (Hiz) Vout = VBAT = 28 V	-	-	100	μA
	I outleak	OUT1, OUT2, OUT3, OUT4	OUT1/2: OFF (Hiz) Vout = GND	-100	-	-	μA
Output SR	trD/tfD	OUT1, OUT2, OUT3, OUT4	RL = 3 Ω, VBAT = 14 V.	-	1.09	-	V/μs
	trD/tfD			-	2.19	-	V/μs
	trD/tfD			-	4.38	-	V/μs
	trD/tfD			-	8.75	-	V/μs
	trD/tfD			-	17.50	-	V/μs
	trD/tfD			-	21.88	-	V/μs
	trD/tfD			-	26.25	-	V/μs
Driver output delay time	tD(on)	PWM1/2, PWM3/4 OUT1/2, OUT3/4	VBAT = 14 V Output SR=17.50 V/μs	-	8.0	-	μs
	tD(off)			-	8.0	-	μs
	ΔtD		tD(on) - tD(off)	-	-	5	μs
Enable/Disable delay time	tDEN	EN1/2, ENB1/2 OUT1/2, OUT3/4	Output SR=17.50 V/μs	-	8	-	μs

8.4. Current limit control

Table 8.4 Current limit control electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 V to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Current limit H-side threshold	Ilim-H	OUT1/2, OUT3/4	CONFIG1/2 DATA[18] = 0	-	6.5	-	A
	Ilim-H	OUT1/2, OUT3/4	CONFIG1/2 DATA[18] = 1	-	4.6	-	A
Current limit time	Toff_min	OUT1/2, OUT3/4		-	20.5	-	μs
Current limit L-side threshold	Ilim-L	OUT1/2, OUT3/4	CONFIG1/2 DATA[17] = 0	-	Ilim-H -0.25	-	A
	Ilim-L	OUT1/2, OUT3/4	CONFIG1/2 DATA[17] = 1	-	Ilim-H -0.5	-	A

* This IC has an internal filter.

Table 8.5 Current limit control electrical characteristics (when temperature requiring current limitation is detected)

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 V to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Current limit H-side threshold	Ilim-H	OUT1/2, OUT3/4		-	2.5	-	A
Current limit temperature	Twar	-	*	-	160	-	°C

Note: * is a design value to which no mass-production test is applicable.

8.5. Over-temperature detection circuit

Table 8.6 Over-temperature detection circuit electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 V to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Over-temperature detection Shutdown temperature	TSD	-	*	175	-	-	°C
Over-temperature detection recovery temperature	TSDL		*	150	-	-	°C

Note: * is a design value to which no mass-production test is applicable.

8.6. Circuit to detect over-current caused by short-circuit to power supply or ground, or short-circuited load

Table 8.7 Circuit to detect over-current caused by short-circuit to power supply or ground, or short-circuited load - electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 V to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Over-current circuit threshold	Iovc	OUT1/2, OUT3/4		-	11.0	-	A
OFF time	TOFF	OUT1/2, OUT3/4	Automatic recovery mode	-	300	-	ms

8.7. DIAG output

Table 8.8 DIAG output electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 V to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
DIAG output leak current	Idiag (leak)	DIAG1/2	Vdiag = 5 V	-	-	5.0	μA
L level output voltage	Vdiag	DIAG1/2	RL = 5.1 kΩ, VCC = 1.5 to 5.5 V (L-retention circuit)	-	-	0.4	V

8.8. Hi-side current monitoring

Table 8.9 Output (Hi-side) current monitoring electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 V to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
CM1/2 output current 1	VCM	CM1, CM2	R = 220 Ω, Iout = 0 mA	-	-	50	μA
CM1/2 output current 2			R = 220 Ω, Iout = 300 mA	-	270	-	μA
CM1/2 output current 3			R = 220 Ω, Iout = 1 A	-	2.2	-	mA
CM1/2 output current 4			R = 220 Ω, Iout = 1.5 A	-	3.57	-	mA
CM1/2 output current 5			R = 220 Ω, Iout = 3.0 A	-	7.14	-	mA
CM1/2 output current 6			R = 220 Ω, Iout = 6.0 A	-	14.3	-	mA

Note: Since the VCC voltage (min.) is 4.5 V, even with external resistor larger than 220 Ω, the voltage is limited.

8.9. SPI communication

Table 8.10 SPI communication electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
Input voltage	VIH3	SDI, SCLK, NCS	VDDIO = 4.5 to 5.5 V	3.6	-	VDDIO	V
	VIL3		VDDIO = 4.5 to 5.5 V	-0.3	-	0.8	V
	Vhys3		VDDIO = 4.5 to 5.5 V	0.1	-	1	V
Input voltage	VIH4	SDI, SCLK, NCS	VDDIO = 3.0 to 3.6 V	2.4	-	VDDIO	V
	VIL4		VDDIO = 3.0 to 3.6 V	-0.3	-	0.8	V
	Vhys4		VDDIO = 3.0 to 3.6 V	0.1	-	1	V
Input current	IIH3	NCS	VIN = VDDIO = 5 V	-5	-	5	μA
	IIH4	SDI, SCLK		-	50	-	μA
	IIL3	SDI, SCLK	VDDIO = 5 V, VIN = GND	-5	-	5	μA
	IIL4	NCS		-	-14	-	μA
Output voltage	VOH (SDO)	SDO	IOH = -2 mA	0.9 * VDDIO	-	-	V
	VOL (SDO)	SDO	IOL = 2 mA	-	-	0.1 * VDDIO	V
AC characteristics	Td (SDO1)	NCS → SDO		-	-	100	ns
	Td (SCLK)	NCS → SCLK		100	-	-	ns
	Td (NCS)	SCLK → NCS		100	-	-	ns
	Tsu (SDI)	SCLK → SDI		50	-	-	ns
	Th (SDI)	SCLK → SDI		50	-	-	ns
	Tvalid	SCLK → SDO	CL = 100 pF	-	-	50	ns
	Ttrans	NCS↑ → NCS↓		1000	-	-	ns
	Td (SDO2)	NCS → SDO (OFF)	CL = 100 pF	-	-	300	ns
	fSPI	SCLK		-	-	5	MHz

Table 8.11 SPI communication disruption detection electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
SPI communication disruption duration	Tstop (NCS)	NCS	CONFIG1 DATA[10:9] = 00	-	10	-	ms
			CONFIG1 DATA[10:9] = 01	-	100	-	ms
			CONFIG1 DATA[10:9] = 10	-	1000	-	ms
			CONFIG1 DATA[10:9] = 11	-	Not applicable	-	ms

Table 8.12 PWM_CLK pin input clock fault detection electrical characteristics

Test conditions unless otherwise specified: VBAT = 4.5 to 28 V, VCC = 4.5 to 5.5 V, VDDIO = 3.0 to 5.5 V, Tj = -40 to 150°C

Item	Symbol	Applicable pin	Test condition	Min.	Typ.	Max.	Unit
PWM_CLK suspension determination time	Tstop (PWM_CLK)	PWM_CLK		-	8	-	μs

9. Example application circuit

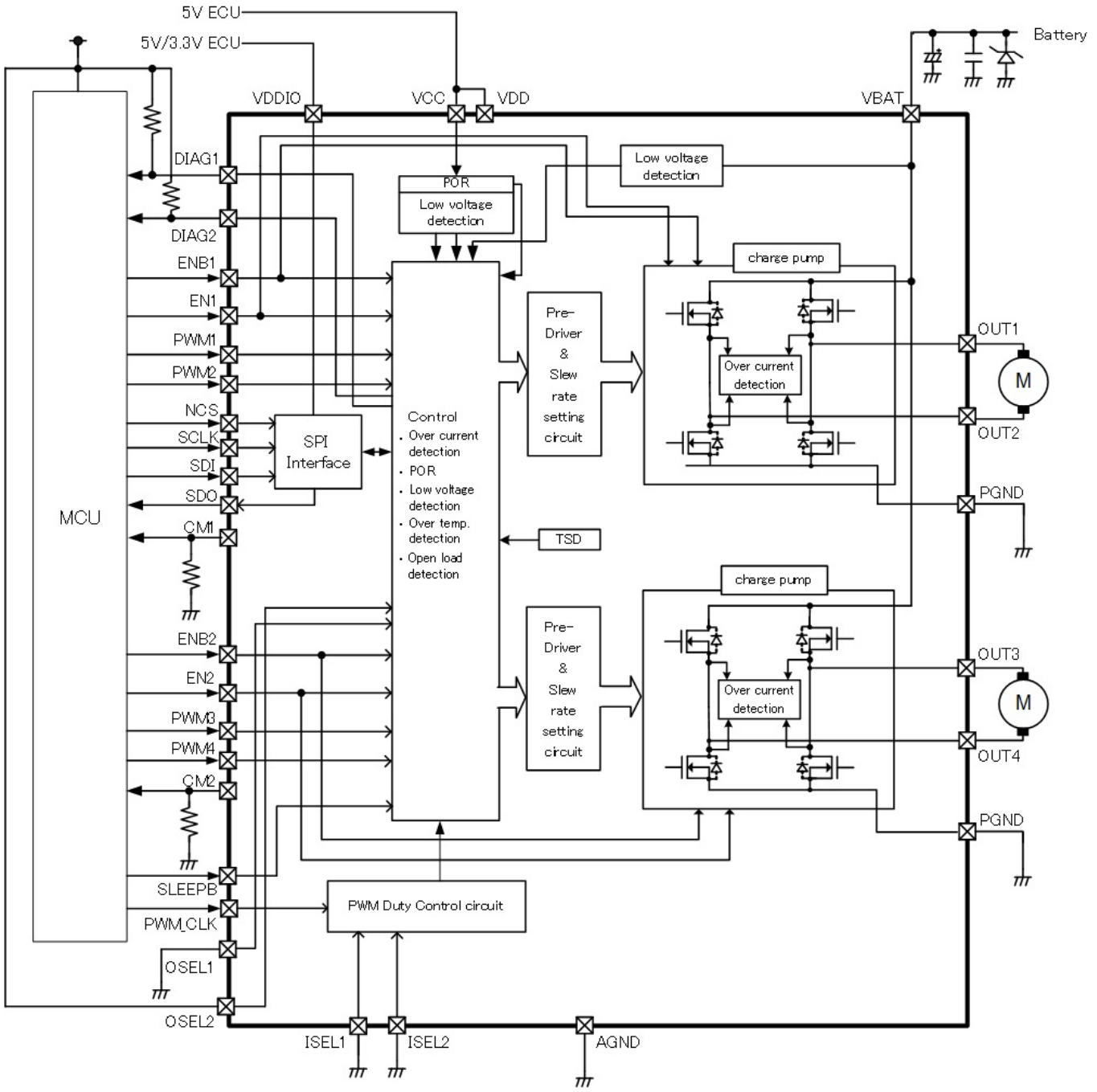


Figure 9.1 Example application circuit

Note: Some of the functional blocks and circuits in the block diagram may be omitted or simplified for explanatory purposes.

Note: Do not insert devices in the wrong orientation or incorrectly. Otherwise, it may cause device breakdown, damage and/or deterioration.

Note: The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

Note: When an output pin is short-circuited to another output pin, power supply, or ground, the IC may be broken down. Carefully design the output, VBAT, VCC, and GND lines.

Note: For the board design, use solid patterns for AGND and PGND.

Counter electromotive force

At the power-regeneration timing during motor rotation, the motor current is fed back to the power supply due to motor counter electromotive force.

If the power supply does not have enough sink capability, the power supply and output pins of the IC might rise above the rated voltages.

The magnitude of the motor counter electromotive force varies with use conditions and motor characteristics. Thoroughly verify that the counter electromotive force does not cause malfunction or breakdown of the IC or other part of the system such as a peripheral circuit.

10. Package drawings

10.1. Package dimensions TB9053FTG (P-QFN40-0606-0.50)

Weight: 0.19g (Typ.)

" Unit : mm "

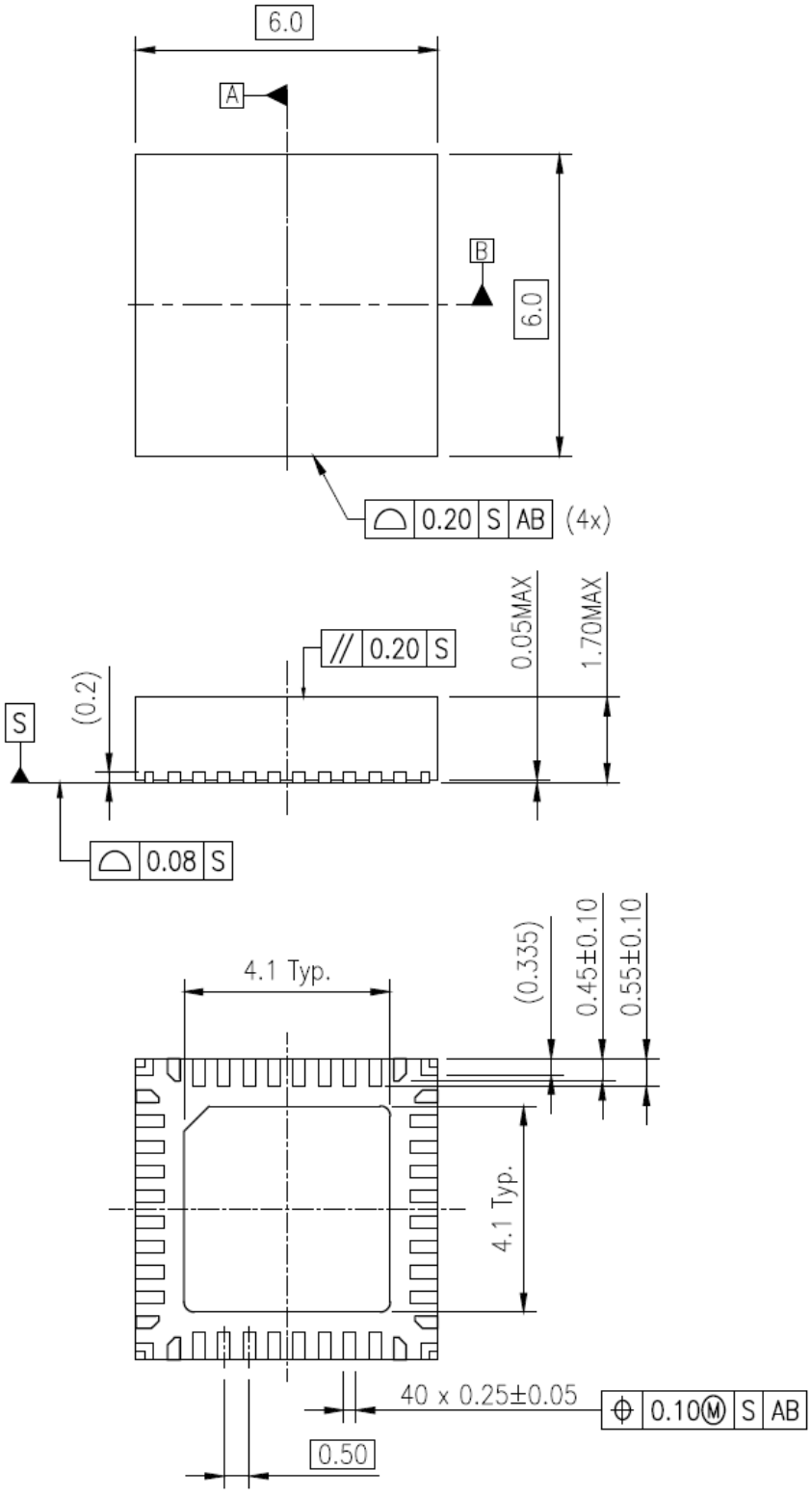


Figure 10.1 Package dimensions TB9053FTG

10.2. Package dimensions TB9054FTG (P-VQFN40-0606-0.50)

Weight: 0.10g (Typ.)

" Unit : mm "

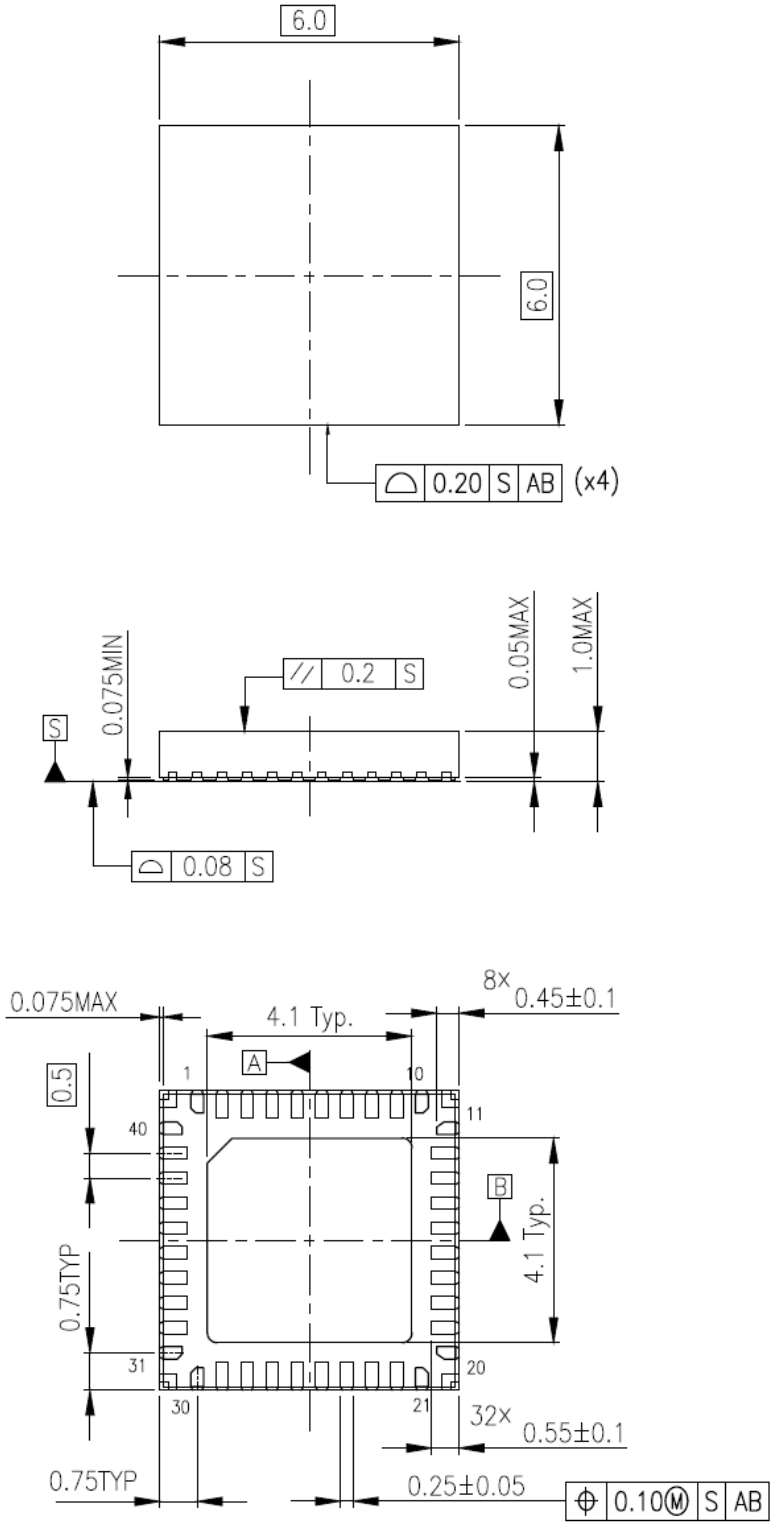


Figure 10.2 Package dimensions TB9054FTG

11. IC Usage Considerations

11.1. Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment.
Do not exceed any of these ratings.
Exceeding the ratings may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

11.2. Points to remember on handling of ICs

(1) Over-current protection circuit
An over-current limiting circuit does not necessarily protect an IC under all circumstances. When it is activated, promptly eliminate the over-current state. Depending on the method of use and/or usage conditions such as exceeding absolute maximum ratings, an over-current detection circuit may not operate properly or the IC is broken down before the circuit is activated. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal shutdown circuit
A thermal shutdown circuit does not necessarily protect an IC under all circumstances. When it is activated, promptly eliminate the over-temperature state. Depending on the method of use and/or usage conditions such as exceeding absolute maximum ratings, a thermal shutdown circuit may not operate properly or the IC is broken down before the circuit is activated.

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