RICOH

RN5C750

4ch RGB Laser Diode Driver for Display System, for Automotive Applications

NO.EC-544-191115

OVERVIEW

The RN5C750 is a laser-diode driver designed to support four-channel RGB/RGGB displays for driving laser scanning systems. By connecting photo diodes (PD), this device is capable of automatically detecting a threshold current and a light emitting current of each channel of the laser-diode drivers (LD).

KEY BENEFITS

- 200Mdot/sec High Speed Sink Type 10-Bit Current DAC RGGB 4-Channel Configuration.
- Equipped with TIA/PGA for PD Light Receiving System and Automatic Setting Functions of Increase/ /Decrease Rate for LD Light Emitting Current and LD Threshold Current.
- QFN 56-Pins Wettable Frank Compatible.
- Provided Safe Pin Arrangement with Consideration for Shorting between Adjacent Pins.

KEY SPECIFICATIONS

- RGGB 4 Channel Current Output (Sink)
- LD1 (R) Maximum Operating Current...... IOP = 800 mA (ICOLOR = up to 500 mA, ITH = up to 300 mA)
- LD2 to 4 (GGB) Maximum Operating Current IoP = 400 mA (ICOLOR = up to 250 mA, ITH = up to 150 mA)
- Maximum Output Rate Per 1 Channel 200Mdot/sec
- High Gradation Output by Using 10-Bit Color DAC
- High Speed Output of Typically 1.0-ns Rising/Falling
- 20-bit Parallel Input Video I/F, Maximum Clock Frequency: 200 MHz, LVCMOS I/F
- 10-bit Parallel Input Video I/F, Maximum Clock Frequency: 225 MHz, LVCMOS I/F
- 10-V LD Pin Corresponding to High Forward Voltage (VF) LD
- Power Saving and Heat Generation Suppression of Package by Using LD Power Source Control
- Protections: LD Overcurrent, LD Pin Short Circuit, PDI Input, Thermal Shutdown
- Pulse-Off Function, Dimming Function
- 12-bit SAR-ADC
- Serial Port Control by Using SPI Communication, SPI Maximum: 25 MHz
- Operating Temperature Range: -40°C to 105°C



NO.EC-544-191115

BLOCK DIAGRAM



RN5C750 Block Diagram

RICOH

NO.EC-544-191115

PIN DESCRIPTIONS



RN5C750 (QFN0808-56) Pin Configuration

NO.EC-544-191115

RN5C750 Pin Description

1 PC2 0 A Laser 2 Driving Power Source Control Signal 2 PC3 0 A Laser 4 Driving Power Source Control Signal 3 PC4 0 A Laser 4 Driving Power Source Control Signal 4 BST 0 A Laser 4 Driving Power Source Control Signal 5 GNDLD1 I G LD1 Driving Block GND Signal 6 LD1 0 A Laser 2 Driving Current Signal 7 GNDLD2 I G LD2 Driving Block GND Signal 8 LD2 0 A Laser 2 Driving Current Signal 10 LD3 0 A Laser 3 Driving Current Signal 10 LD3 0 A Laser 3 Driving Current Signal 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 0 A Laser 4 Driving Current Signal 13 GNDLD4 I G Digital Block GND Signal 14 RST I D Reset Signal 15 XIRQ O D Interruption	Pin No.	Pin Name	I/O ⁽¹⁾	Pin Type ⁽²⁾	Description
2 PC3 0 A Laser 3 Driving Power Source Control Signal 3 PC4 0 A Laser 4 Driving Power Source Control Signal 4 BST 0 A BST Signal for a boosting capacitor 5 GNDLD1 I G LD1 Driving Block GND Signal 6 LD1 0 A Laser1 Driving Current Signal 7 GNDLD2 I G LD2 Driving Block GND Signal 8 LD2 0 A Laser2 Driving Current Signal 10 LD3 I G LD3 Driving Block GND Signal 10 LD3 O A Laser3 Driving Current Signal 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 O A Laser4 Driving Current Signal 13 GNDED5 I G Digital Block GND Signal 14 RST I D Reset Signal 14 RST I D Reset Signal 15 XIRQ O D Interruption Signal 16<	1	PC2	0	А	Laser 2 Driving Power Source Control Signal
3 PC4 0 A Laser 4 Driving Power Source Control Signal 4 BST 0 A BST Signal for a boosting capacitor 5 GNDLD1 I G LD1 Driving Block GND Signal 6 LD1 0 A Laser1 Driving Current Signal 7 GNDLD2 I G LD2 Driving Block GND Signal 8 LD2 0 A Laser2 Driving Current Signal 10 LD3 0 A Laser3 Driving Current Signal 10 LD3 0 A Laser4 Driving Current Signal 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 0 A Laser4 Driving Current Signal 13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal 15 XIRQ O <td>2</td> <td>PC3</td> <td>0</td> <td>А</td> <td>Laser 3 Driving Power Source Control Signal</td>	2	PC3	0	А	Laser 3 Driving Power Source Control Signal
4 BST O A BST Signal for a boosting capacitor 5 GNDLD1 I G LD1 Driving Block GND Signal 6 LD1 O A Laser1 Driving Current Signal 7 GNDLD2 I G LD2 Driving Block GND Signal 8 LD2 O A Laser2 Driving Current Signal 10 LD3 I G LD3 Driving Block GND Signal 10 LD3 O A Laser3 Driving Current Signal 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 O A Laser4 Driving Current Signal 13 GNDB4 I G Digital Block GND Signal 14 RST I D Reset Signal 15 XIRQ O D Interruption Signal 16 XDIM I D	3	PC4	0	А	Laser 4 Driving Power Source Control Signal
5 GNDLD1 I G LD1 Driving Block GND Signal 6 LD1 O A Laser1 Driving Current Signal 7 GNDLD2 I G LD2 Driving Block GND Signal 8 LD2 O A Laser2 Driving Current Signal 9 GNDLD3 I G LD3 Driving Block GND Signal 10 LD3 O A Laser3 Driving Current Signal 10 LD3 O A Laser3 Driving Current Signal 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 O A Laser4 Driving Current Signal 13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal This pin connects to the cathode of Laser 4. Digital Block GND Signal This pin sactive at "High". This has a 3.3V tolerant I/O buffer with a pull-up resistor. 15 XIRQ O D Interruption Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer with a pull-up resistor. 17 VCC3LD I	4	BST	0	А	BST Signal for a boosting capacitor
6 LD1 0 A Laser1 Driving Current Signal This pin connects to the cathode of Laser 1. 7 GNDLD2 I G LD2 Driving Block GND Signal 8 LD2 0 A Laser2 Driving Current Signal This pin connects to the cathode of Laser 2. 9 GNDLD3 I G LD3 Driving Block GND Signal 10 LD3 0 A Laser3 Driving Current Signal This pin connects to the cathode of Laser 3. 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 0 A Laser3 Driving Current Signal This pin connects to the cathode of Laser 4. 13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal This pin becomes "Low" when detected interruption and "Hiz" when not detected it or when reset. This has a 3.3V tolerant I/O buffer. 15 XIRQ O D Interruption Signal This pin becomes "Low" when detected interruption and "Hiz" when not detected it or when reset. This has a 3.3V tolerant I/O buffer. 16 XDIM I D Power Dimming Valid Range Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer with a pull-up resistor.	5	GNDLD1	I	G	LD1 Driving Block GND Signal
This pin connects to the cathode of Laser 1. 7 GNDLD2 I G LD2 Driving Block GND Signal 8 LD2 O A Laser2 Driving Current Signal 9 GNDLD3 I G LD3 Driving Block GND Signal 10 LD3 O A Laser3 Driving Current Signal 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 O A Laser3 Driving Current Signal 13 GNDB I G D4 Driving Block GND Signal 14 RST I D Reset Signal This pin connects to the cathode of Laser 4. 13 GNDB I G Digital Block GND Signal This pin sontents of the cathode of Laser 4. 14 RST I D Reset Signal This pin sontexts of the cathode of Laser 4. 15 XIRQ O D Interruption Signal This pin sontext of the cathode of Laser 4. 16 XDIM I D Power Dimming Valid Range Signal This pin sontext of the cathode of Laser 4. 17 VCC3LD I P<	6	LD1	0	A	Laser1 Driving Current Signal
7 GNDLD2 1 G LD2 Driving Block GND Signal 8 LD2 O A Laser2 Driving Current Signal 9 GNDLD3 I G LD3 Driving Block GND Signal 10 LD3 O A Laser3 Driving Current Signal 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 O A Laser4 Driving Current Signal 13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal This pin connects to the cathode of Laser 4. Digital Block GND Signal This pin is active at "High". This has a 3.3V tolerant I/O buffer with a pull-up resistor. 15 XIRQ O D Interruption Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer. Power Dimming Valid Range Signal 16 XDIM I D Power Dimming Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization Enabled Signal 18 XAPC I D Initialization starts at the falling edge of XAPC ("High" to					This pin connects to the cathode of Laser 1.
8 LD2 O A Laser2 Driving Current Signal 9 GNDLD3 I G LD3 Driving Block GND Signal 10 LD3 O A Laser3 Driving Current Signal 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 O A Laser4 Driving Current Signal 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 O A Laser4 Driving Current Signal 13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal This pin is active at "High". This has a 3.3V tolerant I/O buffer with a pull-up resistor. 15 XIRQ O D Interruption Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer. 16 XDIM I D Power Dimming Valid Range Signal 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization starts at the falling edge of XAPC ("High" to "Low").	7	GNDLD2		G	LD2 Driving Block GND Signal
9 GNDLD3 I G LD3 Driving Block GND Signal 10 LD3 0 A Laser3 Driving Current Signal This pin connects to the cathode of Laser 3. 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 0 A Laser4 Driving Current Signal This pin connects to the cathode of Laser 4. 13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal This pin is active at "High". This has a 3.3V tolerant I/O buffer with a pull-up resistor. 15 XIRQ O D Interruption Signal This pin is active at "High". This has a 3.3 V tolerant I/O buffer. 16 XDIM I D Power Dimming Valid Range Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer with a pull-up resistor. 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset. 20 SCL I D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer. 20 SCL I D SPI Serial	8	LD2	0	A	Laser2 Driving Current Signal
3 O(NDEDS) 1 0 A Laser3 Driving Current Signal 10 LD3 O A Laser3 Driving Current Signal 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 O A Laser4 Driving Current Signal 13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal 14 RST I D Reset Signal 15 XIRQ O D Interruption Signal 16 XDIM I D Power Dimming Valid Range Signal 17 VCC3LD I P Power Dimming Valid Range Signal 18 XAPC I D Power Dimming Valid Range Signal 18 XAPC I D Initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Clock Line Signal 17 D D SPI Serial Clock Line Signal	9		1	G	Ins pin connects to the carlode of Laser 2.
Instruction Construction Construction Construction 11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 O A Laser4 Driving Current Signal 13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal 14 RST I D Reset Signal 15 XIRQ O D Interruption Signal 15 XIRQ O D Interruption Signal 16 XDIM I D Power Dimming Valid Range Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer. Power Dimming Valid Range Signal 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization Enabled Signal 18 XAPC I D SPI Serial Data Line Signal 19 SDA I/O D SPI Serial Clock Line Signal 17 D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer	10		0	Δ	Laser3 Driving Current Signal
11 GNDLD4 I G LD4 Driving Block GND Signal 12 LD4 O A Laser4 Driving Current Signal This pin connects to the cathode of Laser 4. 13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal This pin is active at "High". This has a 3.3V tolerant I/O buffer with a pull-up resistor. 15 XIRQ O D Interruption Signal This pin becomes "Low" when detected interruption and "Hiz" when not detected it or when reset. This has a 3.3 V tolerant I/O buffer. 16 XDIM I D Power Dimming Valid Range Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer with a pull-up resistor. 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer. 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN </td <td>10</td> <td>LDJ</td> <td></td> <td>~</td> <td>This pin connects to the cathode of Laser 3.</td>	10	LDJ		~	This pin connects to the cathode of Laser 3.
12 LD4 O A Laser4 Driving Current Signal This pin connects to the cathode of Laser 4. 13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal This pin is active at "High". This has a 3.3V tolerant I/O buffer with a pull-up resistor. 15 XIRQ O D Interruption Signal This pin becomes "Low" when detected interruption and "Hiz" when not detected it or when reset. This has a 3.3 V tolerant I/O buffer. 16 XDIM I D Power Dimming Valid Range Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer with a pull-up resistor. 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. <	11	GNDLD4	I	G	LD4 Driving Block GND Signal
Image: Second system This pin connects to the cathode of Laser 4. 13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal This pin is active at "High". This has a 3.3V tolerant I/O buffer with a pull-up resistor. 15 XIRQ O D Interruption Signal 16 XDIM I D Power Dimming Valid Range Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer. Power Dimming Valid Range Signal 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset. 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I	12	LD4	0	А	Laser4 Driving Current Signal
13 GNDB I G Digital Block GND Signal 14 RST I D Reset Signal 14 RST I D Reset Signal 15 XIRQ O D Interruption Signal 15 XIRQ O D Interruption Signal 16 XDIM I D Power Dimming Valid Range Signal 16 XDIM I D Power Dimming Valid Range Signal 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization Enabled Signal The initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset. 20 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. PO Enabled Signal This has a 3.3 V tolerant I/O buffer.		_			This pin connects to the cathode of Laser 4.
14 RST I D Reset Signal This pin is active at "High". This has a 3.3V tolerant I/O buffer with a pull-up resistor. 15 XIRQ O D Interruption Signal This pin becomes "Low" when detected interruption and "Hiz" when not detected it or when reset. This has a 3.3 V tolerant I/O buffer. 16 XDIM I D Power Dimming Valid Range Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer with a pull-up resistor. 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization Enabled Signal The initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset. 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D SPI Enabled Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High".	13	GNDB	I	G	Digital Block GND Signal
15 XIRQ O D Interruption Signal This pin becomes "Low" when detected interruption and "Hiz" when not detected it or when reset. This has a 3.3 V tolerant I/O buffer. 16 XDIM I D Power Dimming Valid Range Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer with a pull-up resistor. 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization Enabled Signal The initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset. 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 23 VCLK I D Video Clock Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High".	14	RST	I	D	Reset Signal
15 XIRQ O D Interruption Signal This pin becomes "Low" when detected interruption and "Hiz" when not detected it or when reset. This has a 3.3 V tolerant I/O buffer. 16 XDIM I D Power Dimming Valid Range Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer with a pull-up resistor. 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization Enabled Signal The initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset. 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 23 VCLK I D Video Clock Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High".					I his pin is active at "High". This has a 3.3V tolerant I/O buffer with a pull-up resistor
Image: Construct of the systemThis pin becomes "Low" when detected interruption and "Hiz" when not detected it or when reset. This has a 3.3 V tolerant I/O buffer.16XDIMIDPower Dimming Valid Range Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer with a pull-up resistor.17VCC3LDIPLDn Driving Block 3.3 V Power Source Signal (n: 1 to4)18XAPCIDInitialization Enabled Signal The initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor.19SDAI/ODSPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset.20SCLIDSPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer.21SENIDSPI Enabled Signal This has a 3.3 V tolerant I/O buffer.22POENIDSPI Enabled Signal This has a 3.3 V tolerant I/O buffer.23VCLKIDVideo Clock Signal Maximum frequency: 225MHz	15	XIRQ	0	D	Interruption Signal
Image: Second state is a second state second state is a second state is a second state is a second stat	-				This pin becomes "Low" when detected interruption and "Hiz" when
16 XDIM I D Power Dimming Valid Range Signal This pin indicates a valid range for power dimming. This has a 3.3V tolerant I/O buffer with a pull-up resistor. 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization Enabled Signal The initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer with a pull-up resistor. 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D PO Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D PO Enabled Signal This has a 3.3 V tolerant I/O buffer. 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz					not detected it or when reset. This has a 3.3 V tolerant I/O buffer.
Initial printing and the printing and the printing of the power dimining. This has a 3.3 violerant I/O buffer with a pull-up resistor. 17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization Enabled Signal The initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset. 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D Video Clock Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High". 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz	16	XDIM		D	Power Dimming Valid Range Signal
17 VCC3LD I P LDn Driving Block 3.3 V Power Source Signal (n: 1 to4) 18 XAPC I D Initialization Enabled Signal The initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset. 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 VCLK I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz					tolerant I/O buffer with a pull-up resistor.
18 XAPC I D Initialization Enabled Signal The initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor. 19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset. 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D SPI Enabled Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High". 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz	17	VCC3LD	I	Р	LDn Driving Block 3.3 V Power Source Signal (n: 1 to4)
The initialization starts at the falling edge of XAPC ("High" to "Low"). From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor.19SDAI/ODSPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset.20SCLIDSPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer.21SENIDSPI Enabled Signal This has a 3.3 V tolerant I/O buffer.22POENIDSPI Enabled Signal This has a 3.3 V tolerant I/O buffer.23VCLKIDVideo Clock Signal Maximum frequency: 225MHz	18	XAPC	I	D	Initialization Enabled Signal
From that time forward, the initialization runs during the XAPC of "Low". This pin has a 3.3 V tolerant I/O buffer with a pull-up resistor.19SDAI/ODSPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset.20SCLIDSPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer.21SENIDSPI Enabled Signal This has a 3.3 V tolerant I/O buffer.22POENIDSPI Enabled Signal This has a 3.3 V tolerant I/O buffer.23VCLKIDVideo Clock Signal Maximum frequency: 225MHz					The initialization starts at the falling edge of XAPC ("High" to "Low").
19 SDA I/O D SPI Serial Data Line Signal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset. 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D PO Enabled Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High". 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz					From that time forward, the initialization runs during the XAPC of
10 10 10 10 For Formal Para Line orginal This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This pin is an input signal at reset. 20 SCL I D SPI Serial Clock Line Signal 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D PO Enabled Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High". 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz Maximum frequency: 225MHz D	19	SDA	1/0	D	SPI Serial Data Line Signal
pin is an input signal at reset. 20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D PO Enabled Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High". 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz	10	ODA	",	U	This has a 3.3 V tolerant I/O buffer and outputs a 1.8 V signal. This
20 SCL I D SPI Serial Clock Line Signal This has a 3.3 V tolerant I/O buffer. 21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D PO Enabled Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High". 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz					pin is an input signal at reset.
21 SEN I D SPI Enabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D PO Enabled Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High". 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz	20	SCL	I	D	SPI Serial Clock Line Signal
21 3EIN 1 D 3FT Litabled Signal This has a 3.3 V tolerant I/O buffer. 22 POEN I D PO Enabled Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High". 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz	21	SEN		П	This has a 3.3 V tolerant I/O buffer.
22 POEN I D PO Enabled Signal To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High". 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz	21	SLIN		U	This has a 3.3 V tolerant I/O buffer.
To reduce a speckle noise, a light-off pulse set in the register occurs to a video data during the POEN of "High". 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz	22	POEN	I	D	PO Enabled Signal
to a video data during the POEN of "High". 23 VCLK I D Video Clock Signal Maximum frequency: 225MHz					To reduce a speckle noise, a light-off pulse set in the register occurs
	- 22		1		to a video data during the POEN of "High".
	23	VULN			Maximum frequency: 225MHz

⁽¹⁾ I: Input Pin, O: Output Pin, I/O: Input/Output Pin
⁽²⁾ A: Analog Signal, D: Digital Signal, P: Power, G: Ground

NO.EC-544-191115

Pin No.	Pin Name	I/O ⁽¹⁾	Pin Type ⁽²⁾	Description
24	D19/PCLK	I	D	VCLK Synchronized Video Data Signal
				Dx is enabled at "High".
				Pixel Clock Signal
				PCLK is valid when selected the mode 2/3 in the video data input
				mode. The pixel clock is the same frequency as a dot rate (dot/sec)
				for output current LDn (n:1 to 4).
				Maximum frequency: 150MHz
25	D18		D	VCLK Synchronized Video Data Signal
26	D17		D	Dx is enabled at "High".
27	D16		D	
28	VCC18		P	Digital Block 1.8 V Power Source Signal
29	D15		D	VCLK Synchronized Video Data Signal
30	D14		D	Dx is enabled at "High".
31	D13		D	
32	D12		D	
33	D11		D	
34	D10	I	D	
35	D9		D	
36	D8		D	
37	D7		D	
38	D6		D	
39	D5		D	
40	D4		D	
41	D3		D	
42	D2		D	
43	GNDB		G	Digital Block GND Signal
44	D1		D	VCLK Synchronized Video Data Signal
45	DO	I	D	Dx is enabled at "High".
46	VCC18		P	Digital Block 1.8 V Power Source Signal
47	PDO	IO	A	TIA-PGA Output Monitoring and ADC Input
48	VCC3		Р	Analog Block 3.3 V Power Source Signal
49	VREF	0	A	Internal Reference Voltage Capacitance Signal
50	GNDA	<u> </u>	G	Analog Block GND Signal
51	PDI4	I	A	Photo Diode (PD) 4 Monitor Current Signal (Im4)
	DDIO			This pin connects to the anode of PD4.
52	PDI3	I	A	Photo Diode (PD) 3 Monitor Current Signal (Im3)
	DDIO		^	This pin connects to the anode of PD3.
53	PDI2	I	A	Photo Diode (PD) 2 Monitor Current Signal (Im2)
E A			Δ	This pin connects to the anode of PD2.
54	רוטיי		A	This pip compare to the anode of DD1
FE		1		This pill connects to the anode of PDT.
25				Leser 4 Driving Block 3.3 v Power Source Signal (n: 1 to4)
56	PUT	0	A	Laser 1 Driving Power Source Control Signal

QEN0808-56 Pin Description (Continued)

TAB

⁽¹⁾ I: Input Pin, O: Output Pin, I/O: Input/Output Pin
⁽²⁾ A: Analog Signal, D: Digital Signal, P: Power, G: Ground

Recommended to connect TAB to ground.

NO.EC-544-191115

Recommended Processing for Unused Pins

It is recommended that unused pins apply the following processing.

Pin Name	Unused Pin Processing
LDn	Shorted to GND
PDI n	Open
PDO	Open
PC n	Pulled up to VCC3
D[19:0]	Pulled down to GND

(n: 1 to 4)

RICOH

NO.EC-544-191115

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit	
V _{CC3}	3.3 V Power Source Voltage ⁽¹⁾	Voltage on VCC3 and VCC3LD	-0.3 to +5	V	
V _{CC18}	1.8 V Power Source Voltage ⁽¹⁾	VCC18 Pin Voltage	-0.3 to +2.5	V	
	1.9.) / Digital Dig Valtage (1)	Voltage on D[19:0], PCLK(D19),	-0.3 to V _{CC18} +0.3	M	
VD18	1.8 V Digital Pin Voltage ()	VCLK, and POEN Pins	Max: +2.5	V	
	1.8 V Digital 3.3 V Tolerant Pin	Voltage on XAPC, XDIM, SDA,	-0.2 to 15	V	
VD18TL	Voltage ⁽¹⁾	SCL, SEN, RST, and XIRQ Pins	-0.3 10 +5	v	
Ma	2 2 V Analog Bin Voltago ⁽¹⁾	Voltage on PCn, PDIn, PDO,	-0.3 to V _{CC3} +0.3	V	
V A3	5.5 V Analog Fill Voltage	VREF, and BST Pins	Max: +5	v	
VLD	LD Pin Voltage ⁽¹⁾	Voltage on LDn Pins	−0.3 to +11	V	
PD	Power Dissipation	Refer to Appendix "Pov	ver Dissipation".		
Tj	Junction Temperature Range	_	-40 ~ 150	°C	
Tstg	Storage Temperature Range	_	-55 ~ 150	°C	

(n: 1 to 4)

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc3	3.3 V Power Source Voltage	3.135	3.3	3.465	V
V _{CC18}	1.8 V Power Source Voltage	1.7	1.8	1.9	V
VLD	LD Pin Voltage			10	V
Та	Operating Temperature Range	-40	25	105	°C

RECOMMENDED OPERATING CONDITONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ With reference to the GND pin voltage

NO.EC-544-191115

ELECTRICAL CHARACTERISTICS

All parameters are tested under the recommended operating conditions, unless otherwise noted.

RN5C750 Electrical Characteristics

Symbol	Parameter	Pin	Conditions	Min.	Тур.	Max.	Unit
Idd3ld	3.3 V Power Source Current at Operation	VCC3LD	SLP = L		15		mA
I _{DD3}	3.3 V Power Source Current at Operation	VCC3	SLP = L		0.5		mA
I _{DD18}	1.8 V Power Source Current at Operation	VCC18	SLP = L		75		mA
I _{SS3LD}	3.3 V Power Source Current at Sleep	VCC3LD	SLP = H, D[19:0] = 0		0		mA
I _{SS3}	3.3 V Power Source Current at Sleep	VCC3	SLP = H, D[19:0] = 0		0.5		mA
I _{SS18}	1.8 V Power Source Current at Sleep	VCC18	SLP = H, D[19:0] = 0		60		mA

Operating Conditions: VCLK = 200MHz, Initialization's off, Each DAC code ⁽¹⁾ = "001h"

RN5C750 Electrical Characteristics: Input / Output Pin

Symbol	Parameter	Pin	Conditions	Min.	Тур.	Max.	Unit
		XAPC, XDIM, RST		V _{CC18} ×0.8			V
Vih	Input Voltage, High	D[19:0], PCLK(D19), VCLK, POEN		V _{CC18} /2 +0.25			V
		SCL, SEN, SDA		V _{CC18} ×0.7			V
		XAPC, XDIM, RST				V _{CC18} ×0.2	V
VIL	Input Voltage, Low	D[19:0], PCLK(D19), VCLK, POEN				V _{CC18} /2 -0.25	V
		SCL, SEN, SDA				V _{CC18} ×0.3	V
Vон	Output Voltage, High	SDA	$I_{LOAD} = 4 \text{ mA}$	V _{CC18} -0.4			V
Vol	Output Voltage, Low	XIRQ, SDA	$I_{LOAD} = 4 \text{ mA}$			0.4	V
loz	Output Off Leakage Current	SDA, XIRQ		-3		3	μA
lız	Input Off Leakage Current	XAPC, XDIM, RST, D[19:0], PCLK(D19),, VCLK, POEN, SCL SEN,				0.1	μA

⁽¹⁾ Thresh_MIN_DAC, Thresh_Scale_DAC, Thresh_DAC, and Color_Scale_DAC

NO.EC-544-191115

Symbol	Parameter	Pin	Conditions	Min.	Тур.	Max.	Unit
VIDON	Output Voltage at Light-on	LDn	IOP_MAX	1.5			V
	Maximum Threaded Current	LD1		240	300		
ITH	Maximum Infeshold Current	LD2/3/4		120	150		mA
	Maximum Light Emitting	LD1		400	500		
ICOLOR	Current	LD2/3/4		200	250		mA
1	Maximum Operating Current	LD1	Icolor + Ith		800		~ ^
IOP	Maximum Operating Current	LD2/3/4	Icolor + Ith		400		mA
CLDNL	Color DAC DNL	LDn	V _{LD} = 1.5 V	-5		5	LSB
CLINL	Color DAC INL	LDn	V _{LD} = 1.5 V	-10		30	LSB
	Color Scale DAC DNL	LDn	V _{LD} = 1.5 V	-5		5	LSB
CSINL	Color Scale DAC INL	LDn	V _{LD} = 1.5 V	-10		35	LSB
T _{HDNL}	Threshold DAC DNL	LDn	V _{LD} = 1.5 V	-2		2	LSB
T _{HINL}	Threshold DAC INL	LDn	V _{LD} = 1.5 V	-5		25	LSB
THSDNL	Threshold Scale DAC DNL	LDn	V _{LD} = 1.5 V	-1		2	LSB
THSINL	Threshold Scale DAC INL	LDn	V _{LD} = 1.5 V	-1		2	LSB
THMDNL	Thresh MIN DAC DNL	LDn	V _{LD} = 1.5 V	-1		1	LSB
THMINL	Thresh MIN DAC INL	LDn	V _{LD} = 1.5 V	-5		5	LSB
li poss	Output Current at Paset	LD1	$PST = high V_{12} = 7 V_{2}$			6	
ILDOFF	Output Current at Neset	LD2/3/4				3	μΑ
lu povo	I D Pin Overcurrent Detection	LD1				880	m۸
ILDOVC		LD2/3/4				440	ША
Vlduvd	LD Pin short-circuit Detection	LD2/3/4			0.5	0.6	V
V _{BST}	Pin Output	BST			5		V
A _{OCDET}	LD Pin Overcurrent Detection	LDn	LD1: up to 880mA LD2/3/4: up to 440mA	-20		35	%

RN5C750 Electrical Characteristics: LD Output DC

(n: 1 to 4)

RN5C750 Electrical Characteristics: LD Output AC

Symbol	Parameter	Pin	Conditions	Min.	Тур.	Max.	Unit
t _{RLD}	ICOLOR Rising Time	LDn			1		ns
t _{FLD}	ICOLOR Falling Time	LDn			1		ns

(n: 1 to 4)

NO.EC-544-191115

Symbol	Parameter	Pin	Conditions	Min.	Тур.	Max.	Unit
VREF	Reference Voltage	VREF	at start up		2.5		V
Vc	Vcont Reference Voltage		at initialization	0.05		2.45	V
V _{PC}	LD Voltage after PC Processing	LDn	PCREF = 4h (1.5 V), LD Power Source: 5 V or more	1.4	1.5	1.6	V
l	Monitor Input Current	DDIn	GAIN = Fh	2.5			uA
IPDI	Monitor input Current	FDIII	GAIN = 0h			6	mA
Vpdo	Monitor Output Voltage	PDO		0.05		2.45	V
Gmax	Maximum IV Amplification Factor		GAIN = Fh		20250		V/A
Gmin	Minimum IV Amplification Factor		GAIN = 0h		300		V/A
Vapca	Input conversion APC accuracy		GAIN = 0h			33	uA
V_{ADIN}	ADC Input Voltage	PDO		0.05		2.45	V
V _{ADA}	ADC accuracy		TIA-PGA GAIN = 0h to Fh APCCLK = 2MHz	-25		25	mV
I _{NITH}	Threshold Detection Error	LDn	LD-PD Liner Model			5	%
INICS	Color Scale Detection Error	LDn	LD-PD Liner Model			5	%
			GAD = 3h		0.33		mA
I	PDI Input Fault Detection		GAD = 2h		1		mA
IPDOVC	(Maximum setting)	PDIN	GAD = 1h		3		mA
			GAD = 0h		9		mA
t APC	Initialization Processing Time		APCCLK = 2MHz, 1ch, Standard Flow			128	μs
t _{PC1}	PC Processing Time1		PCCLK = 0.5 MHz, 1ch, Standard Flow, At startup			130	μs
t _{PC2}	PC Processing Time 2		PCCLK = 0.5MHz, 1ch, Standard Flow, For the 2 nd and subsequent times			6	μs

RN5C750 Electrical Characteristics: Initialization Operation

(n: 1 to 4)

RN5C750 Electrical Characteristics: PLL, Reference Clock

Symbol	Parameter	Pin	Conditions	Min.	Тур.	Max.	Unit
fclkq	PLL Frequency (CLKQ)			100		200	MHz
f _R	Comparison Frequency			10		20	MHz

NO.EC-544-191115

RN5C750 Electrical Characteristics: Overtemperature Protection

Symbol	Parameter	Pin	Conditions	Min.	Тур.	Max.	Unit
	Detection Temperature		TSHUT_DET = 0h		150		°C
Τ			TSHUT_DET = 1h		155		°C
I DET			TSHUT_DET = 2h		160		°C
			TSHUT_DET = 3h		165		°C
			TSHUT_REL = 0h		135		°C
Τ	Pologog Tomporatura		TSHUT_REL = 1h		140		°C
I REL	Release temperature		TSHUT_REL = 2h		145		°C
			TSHUT_REL = 3h		150		°C

RN5C750 Electrical Characteristics: Input Video I/F AC

Symbol	Parameter	Pin	Conditions	Min.	Тур.	Max.	Unit
fvcк	VCLK Frequency	VCLK		10		225	MHz
t _{VCL}	VCLK Low Period	VCLK		2			ns
tvcн	VCLK High Period	VCLK		2			ns
t _{VDS}	Data Setup Time	D[19:0], PCLK(D19), POEN	V _{CC18} x 0.5, ±0.25V	0			ns
t _{VDH}	Data Hold Time	D[19:0], PCLK(D19), POEN	V _{CC18} x 0.5, ±0.25V	1.5			ns
tdrr	Data Input Slew Rate	D[19:0], PCLK(D19), POEN	V _{CC18} x 0.5, ±0.25V	1			V/ns



Video Data I/F Timing Chart

NO.EC-544-191115

	_				_		
Symbol	Parameter	Pin	Test Conditions/Comments	Min.	Тур.	Max.	Unit
fск	SCLK Frequency	SCL				25	MHz
tскн	SCLK High Period	SCL		10			ns
t _{CKL}	SCLK Low Period	SCL		10			ns
t _{ENL}	SEN Low Period	SEN		20			ns
tens	Enable Setup Time	SEN		10			ns
t _{ENH}	Enable Hold Time	SEN		10			ns
tois	Data Setup Time	SDA		5			ns
t _{DIH}	Data Hold Time	SDA		5			ns
too	Data Output Delay Time	SDA				25	ns

RN5C750 Electrical Characteristics: SPI I/F AC







SPI I/F Timing Chart

⁽¹⁾ Address is automatically incremented when during continuous access, without upper limit.

POWER DISSIPATION

QFN0808-56

PD-QFN0808-56(105150)-JE-A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51.

Measurement Conditions

ltem	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 1.6 mm
Copper Ratio	Outer Layer (First Layer): Less than 10% Inner Layers (Second and Third Layers): Approx. 100% of 74.2 mm Square Outer Layer (Fourth Layer): Less than 10%
Through-holes	φ 0.3 mm × 25 pcs

Measurement Result

(Ta = 25°C, Tjmax = 150°C)

Item	Measurement Result
Power Dissipation	5680 mW
Thermal Resistance (θja)	θja = 22°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 4°C/W

θja: Junction-to-Ambient Thermal Resistance

wjt: Junction-to-Top Thermal Characterization Parameter





Power Dissipation vs. Ambient Temperature

Measurement Board Pattern

PACKAGE DIMENSIONS

QFN0808-56

Ver. A



QFN0808-56 Package Dimensions

- 1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to Ricoh sales representatives for the latest information thereon.
- 2. The materials in this document may not be copied or otherwise reproduced in whole or in part without prior written consent of Ricoh.
- 3. Please be sure to take any necessary formalities under relevant laws or regulations before exporting or otherwise taking out of your country the products or the technical information described herein.
- 4. The technical information described in this document shows typical characteristics of and example application circuits for the products. The release of such information is not to be construed as a warranty of or a grant of license under Ricoh's or any third party's intellectual property rights or any other rights.
- 5. The products in this document are designed for automotive applications. However, when using the products for automotive applications, please make sure to contact Ricoh sales representative in advance due to confirming the quality level.
- 6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
- 7. Anti-radiation design is not implemented in the products described in this document.
- 8. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
- 9. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
- There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact Ricoh sales or our distributor before attempting to use AOI.
- 11. Please contact Ricoh sales representatives should you have any questions or comments concerning the products or the technical information.



Ricoh is committed to reducing the environmental loading materials in electrical devices with a view to contributing to the protection of human health and the environment. Ricoh has been providing RoHS compliant products since April 1, 2006 and Halogen-free products since April 1, 2012.

RICOH RICOH ELECTRONIC DEVICES CO., LTD.

Official website https://www.e-devices.ricoh.co.jp/en/ Contact us https://www.e-devices.ricoh.co.jp/en/support/