

PRODUCT BRIEF - Preliminary

1 MAIN FEATURES

- Quad channel 12-bit 1.6 GSps ADC.
- 1 Vpp 100Ω differential DC/AC coupled input voltage
- 100Ω Differential input AC coupled clock
- Cross-point switch enabling 1, 2 or 4 channel mode at 6.4 GSps/3.2 GSps/1.6 GSps
- 4.5/ >6GHz selectable analog input bandwidth (-3dB)
- Low Latency ESStream serial link at 12.8 Gbps
- Power supply: 3.3V (analog), 2.5V (I/O), 1.2V (digital), optional 1.8V (SPI)
- Power consumption 6.6W (Typical)
- SPI digital interface (gain, offset, sampling delay adjust, test modes)
- 2 manufacturing calibration sets for interleaving (through IN0 input)
- ADC Gain, Offset, Sampling delay adjustment for user's interleaving calibration
- Clock and SYNC chaining
- Package: CBGA323 (HiTCE) 16x16mm pitch 0.80mm : RoHS
- Temperature range: Tc -40°C / Tj +110°C

2 PERFORMANCE

Typical performance (Ambient temperature, nominal power supply)

Performance @1.6GSps (4 channel-mode)	Performance @6.4GSps (1 channel-mode)
SFDR (Spurious Free Dynamic Range) <ul style="list-style-type: none"> - Fin = 100MHz : 71.0 dBFS - Fin = 740MHz : 64.7 dBFS - Fin = 1480MHz : 60.1 dBFS - Fin = 2980MHz : 56.4 dBFS - Fin = 5980MHz : 37.1 dBFS 	SFDR (Spurious Free Dynamic Range) <ul style="list-style-type: none"> - Fin = 100MHz : 54.8 dBFS - Fin = 1480MHz : 58.6 dBFS - Fin = 2230MHz : 61.9 dBFS - Fin = 2980MHz : 55.0 dBFS - Fin = 5980MHz : 37.1 dBFS
SNR (Signal to Noise Ratio) <ul style="list-style-type: none"> - Fin = 100MHz : 54.2 dBFS - Fin = 740MHz : 53.8 dBFS - Fin = 1480MHz : 52.9 dBFS - Fin = 2980MHz : 49.6 dBFS - Fin = 5980MHz : 45.5 dBFS 	SNR (Signal to Noise Ratio) <ul style="list-style-type: none"> - Fin = 100MHz : 54.1 dBFS - Fin = 1480MHz : 52.8 dBFS - Fin = 2230MHz : 50.6 dBFS - Fin = 2980MHz : 49.5 dBFS - Fin = 5980MHz : 45.5 dBFS

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<p>ENOB (Effective Number Of Bits)</p> <ul style="list-style-type: none"> - Fin = 100MHz : 8.7 bitFS - Fin = 740MHz : 8.6 bitFS - Fin = 1480MHz : 8.3 bitFS - Fin = 2980MHz : 7.8 bitFS - Fin = 5980MHz : 5.6 bitFS <p>NPR (Noise Power Ratio) at -12dB Loading Factor (80% Nyquist = 600MHz)</p> <p>1st Nyquist : NPR = 44.9dB 2nd Nyquist : NPR = 40.6dB 3rd Nyquist : NPR = 39.9dB</p>	<p>ENOB (Effective Number Of Bits)</p> <ul style="list-style-type: none"> - Fin = 100MHz : 7.9 bitFS - Fin = 1480MHz : 8.1 bitFS - Fin = 2230MHz : 7.9 bitFS - Fin = 2980MHz : 7.5 bitFS - Fin = 5980MHz : 5.1 bitFS
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3 APPLICATIONS

- Automatic Test Equipment
- High-speed Data Acquisition
- Oscilloscopes
- Phased-Array RADAR Receivers
- Wideband Satellite Receivers
- Point-to-Point Microwave Receivers
- LIDAR (LIght Detection And Ranging)
- Direct RF data conversion
- High Energy Physics

4 DESCRIPTION

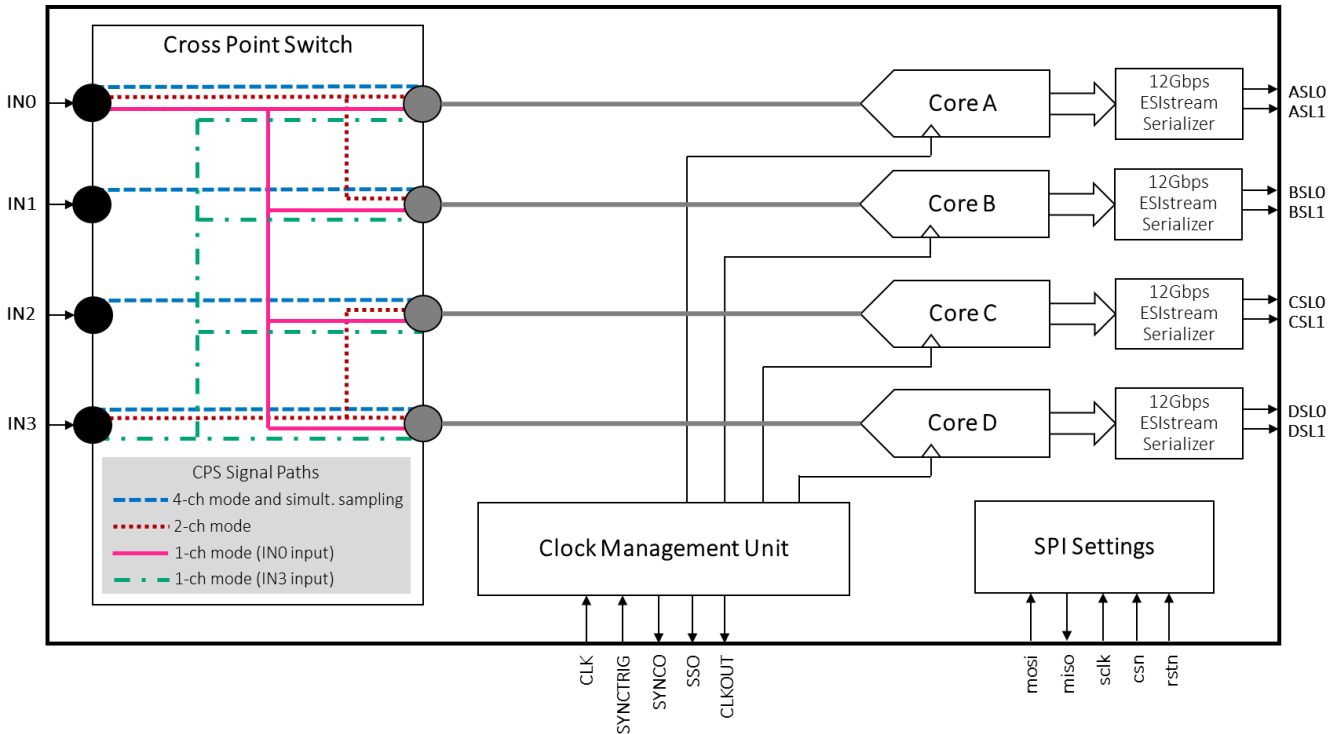


Figure 1 – Simplified block diagram

EV12AQ605 is a quad 12 bit 1.6GSps ADC featuring a built in cross-point switch (controlled thru the SPI) allowing 1, 2 or 4 channel digitizing at respectively 6.4 GSps, 3.2 GSps or 1.6 GSps sampling rate.

The four ADC cores can operate in phase or interleaved (option controlled thru the SPI). External clock must be provided at four times the individual sampling rate.

The architecture uses four high sampling rate single cores (up to 1.6GSps) without interleaving thus providing high level of spectral purity.

Data is output on a short latency serial link at up to 12.8 Gbps, using ESStream protocol.

ADC synchronization is achieved through SYNC input pin. Multiple ADC synchronization is simplified thanks to ability of SYNC chaining through SYNCO output.

Digital CMOS inputs levels can be configured in 1.8V, 2.5V or 3.3V logic compatibility.

Functionalities controlled thru the SPI include:

- Clocking modes: 4 ADC cores sampling simultaneously, 2 ADC cores sampling simultaneously in opposition with 2 others, 4 ADC cores interleaved.
- Clocking features: enable/disable CLKOUT, SSO and SYNCO outputs (in order to save power if these features are not needed).
- Inputs selection: 4 ADC cores interleaved and driven by the same input IN0 (or IN3), 2 ADC cores driven simultaneously by IN0 and IN3, 4 ADCs core driven simultaneously by IN0, IN1, IN2 and IN3.
- Analog input bandwidth: 4.5GHz (nominal) or >6GHz (extended)
- 2 manufacturing calibration sets selection for interleaved mode (IN0). Custom interleaved mode calibration through Offset/Gain/Phase adjustment
- Swing Adjust: Output swing of both serial links and timer CML or LVDS buffers is reduced by 30% for power dissipation reduction purpose.
- Output buffer impedance adjust (trim by a range of 20%) to improve transmission
- 12.8 Gbps Serial link polarity can be inverted

5 PIN DESCRIPTION

5.1 Type / Outline

HiTCE Ceramic Ball Grid Array CBGA323

- High TCE Glass-Ceramic substrate
- Body size: 16.0x16.0 mm
- Lands Pitch: 0.80mm
- Number of balls: 323
- Conductor: cofired copper

Package interconnection

- 18x18 BGA matrix (323 balls, A1 removed)
- 0.80 mm ball pitch
- Ball type : SAC305
- MSL3 (non-hermetic)

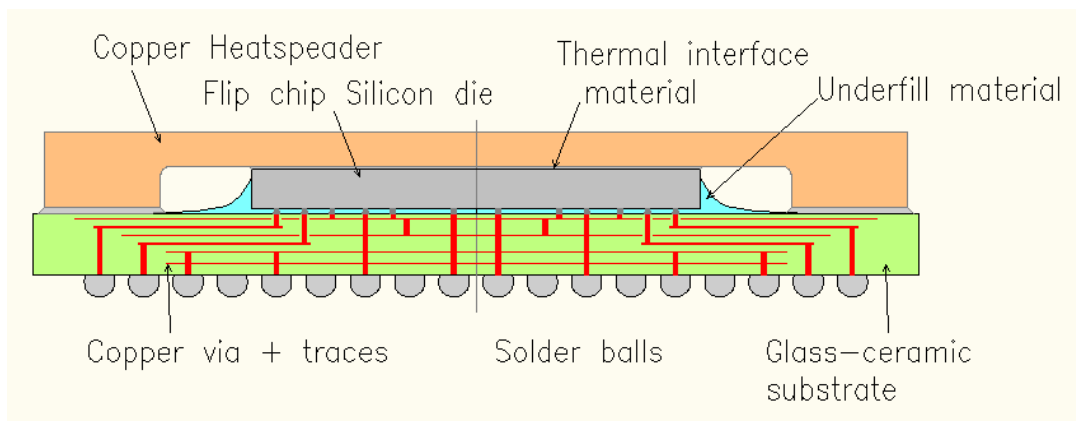


Figure 2 – Package cross-section

5.2 Pinout top-view

Package axis

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A		AGND	AGND	SYNCON	SYNCOF	AGND	CLKOUTN	CLKOUTP	AGND	AGND	CLKP	CLKN	AGND	SYNCTRIGP	SYNCTRIGN	AGND	AGND	DGND	A
B	DGND	DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DGND	B
C	miso	mosi	rstn	DGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	SSON	SSOP	AGND	DGND	DGND	VSP1_SEL	C
D	GND0	GND0	DNC	csn	zclk	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	DNC	GND0	GND0	D
E	GND0	GND0	GND0	DNC	DNC	DGND	AGND	AGND	VCCA	VCCA	AGND	AGND	DGND	DNC	DNC	GND0	GND0	GND0	E
F	ASLIP	ASLIN	GND0	GND0	VCC_SPI	DGND	AGND	AGND	AGND	AGND	AGND	AGND	DGND	VCCD	GND0	GND0	DSLIN	DSLIP	F
G	GND0	GND0	GND0	GND0	DNC	VCCD	AGND	VCCA	VCCA	VCCA	VCCA	AGND	VCCD	DNC	GND0	GND0	GND0	GND0	G
H	ASLOP	ASLON	GND0	VCCD	VCCD	VCCD	AGND	AGND	VCCA	VCCA	AGND	AGND	VCCD	VCCD	VCCD	GND0	DSLON	DSLIP	H
J	GND0	GND0	GND0	GND0	GND0	DGND	AGND	VCCA	AGND	AGND	VCCA	AGND	DGND	GND0	GND0	GND0	GND0	GND0	J
K	BSLOP	BSLON	GND0	VCCD	VCCD	VCCD	AGND	VCCA	VCCA	VCCA	VCCA	AGND	VCCD	VCCD	VCCD	GND0	CSLON	CSLIP	K
L	GND0	GND0	GND0	GND0	GND0	DGND	AGND	VCCA	AGND	AGND	VCCA	AGND	DGND	GND0	GND0	GND0	GND0	GND0	L
M	BSLIP	BSLIN	GND0	VCCD	VCCD	VCCD	AGND	AGND	VCCA	VCCA	AGND	AGND	VCCD	VCCD	VCCD	GND0	CSLIN	CSLIP	M
N	GND0	GND0	GND0	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GND0	GND0	GND0	N
P	GND0	GND0	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	GND0	GND0	P
R	DIODE_C	DIODE_A	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	DNC	CMIREF	R
T	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	T
U	AGND	AGND	AGND	INOP	INON	AGND	ININ	INIP	AGND	AGND	IN2P	IN2N	AGND	IN3N	IN3P	AGND	AGND	AGND	U
V	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Figure 3 - Pinout

5.3 Package drawing

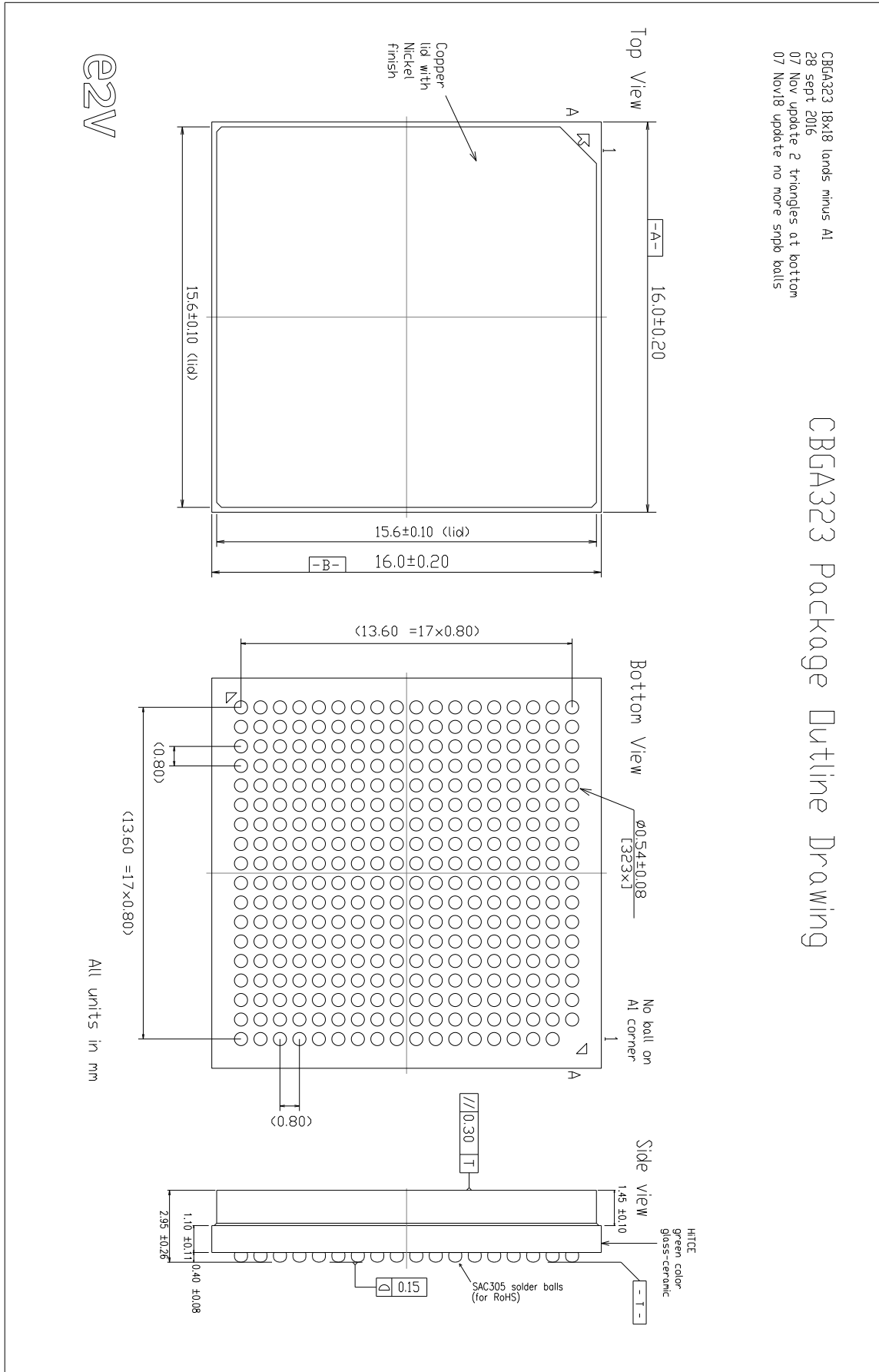


Figure 4 – Package outline for SAC305 balls

6 ORDERING INFORMATION

Part Number	Temperature Range	Screening Level	RoHS compliance	Comments
EVP12AQ605SH	Ambient	Prototype	RoHS	Beta sampling

7 REVISION HISTORY

Issue	Date	Comments
A	19/11/2018	Creation

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