

## TPS62840 1.8-V to 6.5-V, 750-mA, 60-nA $I_Q$ Step-Down Converter

### 1 Features

- 60-nA operating quiescent current
- 100% duty-cycle mode with 150-nA  $I_Q$
- Input voltage range  $V_{IN}$  from 1.8 V to 6.5 V
- Output current up to 750 mA
- RF friendly DCS-Control™
- 80% efficiency at 1  $\mu$ A  $I_{OUT}$  (3.6  $V_{IN}$  to 1.8  $V_{OUT}$ )
- 16 selectable output voltages via VSET pin
- Auto transition PFM/PWM or forced-PWM mode
- Selectable forced PWM and STOP modes
- Output discharge function
- 20-nA shutdown current
- SON-8, WCSP-6 and HVSSOP-8 packages

### 2 Applications

- Smart meters, smart thermostats
- Tracking devices
- Wearable electronics
- Medical sensor patches and patient monitors
- Industrial IoT (smart sensors)
- Test and measurement

### 3 Description

The TPS62840 is a high efficiency step-down converter with ultra-low operating quiescent current of typically 60 nA. The device contains special circuitry to achieve just 150 nA  $I_Q$  in 100% mode to further extend battery life near the end of discharge.

The device uses DCS-Control to cleanly power radios and operates with a typical switching frequency of 1.8 MHz. In Power-Save Mode the device extends the light load efficiency down to a load current range of 1- $\mu$ A and below.

16 predefined output voltages can be selected by connecting a resistor to pin VSET, making the device flexible for various applications with a minimum amount of external components.

The device's STOP pin immediately eliminates any switching noise in order to take a noise-free measurement in test & measurement systems.

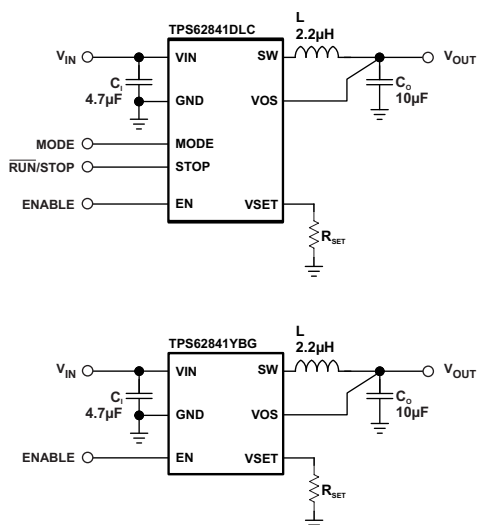
The TPS6284x provides an output current of up to 750 mA. With an input voltage of 1.8 V to 6.5 V, the device supports multiple power sources such as 2S to 4S Alkaline, 1S to 2S Li-MnO<sub>2</sub> or 1S Li-Ion/Li-SoCl<sub>2</sub>.

#### Device Information<sup>(1)</sup>

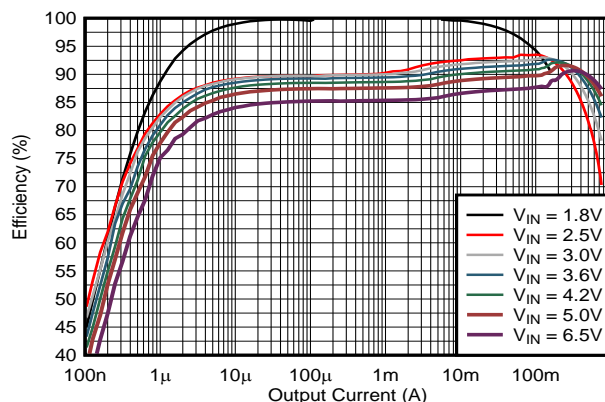
| PART NUMBER | PACKAGE            | BODY SIZE (NOM)   |
|-------------|--------------------|-------------------|
| TPS6284x    | 8 pin DLC (SON)    | 1.5 mm x 2 mm     |
|             | 6 pin YBG (WCSP)   | 0.97 mm x 1.47 mm |
|             | 8 pin DGR (HVSSOP) | 3 mm x 5 mm       |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Typical Application



#### Efficiency vs. Load Current ( $V_{OUT} = 1.8V$ )



D002



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

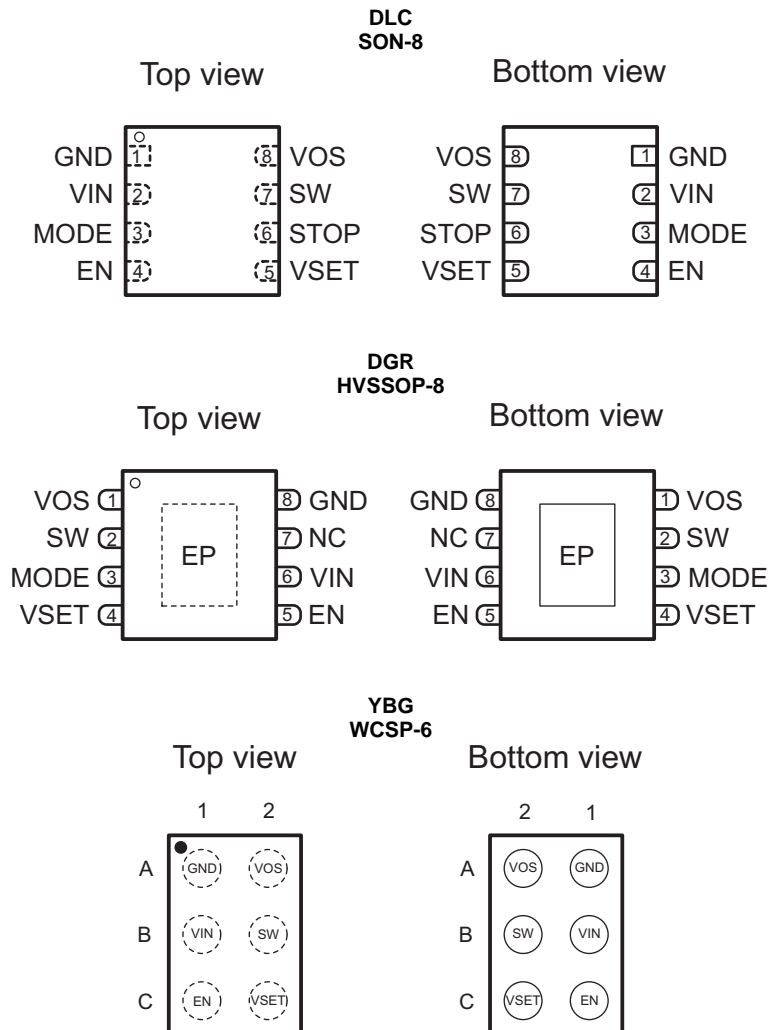
| <b>Changes from Revision A (July 2019) to Revision B</b>                | <b>Page</b> |
|---|-------------|
| • Changed Advance Information marketing status to Production Data ..... | <b>1</b>    |

## 5 Device Comparison Table

| ORDERABLE PART NUMBER      | OUTPUT VOLTAGE   | OUTPUT CURRENT | OUTPUT DISCHARGE | MODE PIN | STOP PIN | PACKAGE        | PACKAGE MARKING |
|----------------------------|--|----------------|------------------|----------|----------|----------------|-----------------|
| TPS62841DLC                | 0.8 V to 1.55 V<br>in 50mV steps                       | 750 mA         | yes              | yes      | yes      | SON-8 (DLC)    | E9              |
| TPS62841YBG                |  |                | yes              | no       | no       | WCSP-6 (YBG)   | 62841           |
| TPS62840DLC                | 1.8 V to 3.3 V<br>in 100-mV steps                      | 750 mA         | yes              | yes      | yes      | SON-8 (DLC)    | E5              |
| TPS62840YBG                |  |                | yes              | no       | no       | WCSP-6 (YBG)   | 62840           |
| TPS62842DGR <sup>(1)</sup> | 1.8 V, 2.0 V, 2.2 V,<br>2.4 V to 3.6 V in 100-mV steps | 750 mA         | yes              | yes      | no       | HVSSOP-8 (DGR) | 62842           |
| TPS62849DLC                | 3.4-V fixed output voltage                             |                |                  |          | yes      | SON-8 (DLC)    | FF              |

(1) Future device options

## 6 Pin Configuration and Functions



### Pin Functions

| NAME | PIN            |                   |                 | I/O | DESCRIPTION  |
|------|----------------|-------------------|-----------------|-----|--|
|      | DLC<br>(SON-8) | DGR<br>(HVSSOP-8) | YBG<br>(WCSP-6) |     |  |
| VIN  | 2              | 6                 | B1              | PWR | V <sub>IN</sub> power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A 4.7-μF ceramic capacitor is required.  |
| SW   | 7              | 2                 | B2              | PWR | The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.  |
| GND  | 1              | 8                 | A1              | PWR | GND supply pin. Connect this pin close to the GND terminal of the input and output capacitors.   |
| VSET | 5              | 4                 | C2              | IN  | Connecting a resistor to GND sets the output voltage when the converter is enabled. For TPS62849, connect this pin to GND.   |
| VOS  | 8              | 1                 | A2              | IN  | Output voltage sense pin for the internal feedback divider network and regulation loop. When the converter is disabled this pin discharges V <sub>OUT</sub> by an internal MOSFET. Connect this pin directly to the output capacitor with a short trace.   |
| EN   | 4              | 5                 | C1              | IN  | Enable pin. A high level enables the device and a low level turns the device off. The pin features an internal pull-down resistor, which is disabled once the device has started up and the output voltage is regulated. The pull-down resistor is activated again, once a low level has been detected.  |
| STOP | 6              | n/a               | n/a             | IN  | STOP Switching pin. When this pin is logic high, the converter stops switching in order to provide a quiet supply rail. The output is powered from the charge available in the output capacitor. When this pin is logic low, the device immediately resumes operation. The pin features an internal pull-down resistor, which is disabled once a high level is detected at the input. The pull-down resistor is activated again, once a low level has been detected. |
| MODE | 3              | 3                 | n/a             | IN  | MODE pin. A low level enables Power-Save Mode operation with an automatic transition between PFM and PWM modes. A high level forces the converter to operated in PWM mode. This pin can be toggled during operation. It must be terminated on not be left open.  |
| NC   | n/a            | 7                 | n/a             |     | This pin is not connected internally. Do not connect this pin.   |
| EP   | n/a            | 9                 | n/a             | PWR | Exposed thermal pad. The PowerPAD must be connected to GND.  |

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

|  |                         | MIN  | MAX                         | UNIT |
|--|-------------------------|------|-----------------------------|------|
| Pin voltage <sup>(2)</sup>                     | VIN                     | -0.3 | 7                           | V    |
|  | SW (DC)                 | -0.3 | V <sub>IN</sub> + 0.3       | V    |
|  | SW (AC), less than 10ns | -2.0 | 8.5                         | V    |
|  | EN, MODE, STOP          | -0.3 | 6.5                         | V    |
|  | VSET                    | -0.3 | V <sub>IN</sub> + 0.3 < 3.6 | V    |
|  | VOS                     | -0.3 | 3.7                         | V    |
| Operating junction temperature, T <sub>J</sub> |                         | -40  | 150                         | °C   |
| Storage temperature, T <sub>stg</sub>          |                         | -65  | 150                         | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal GND.

## 7.2 ESD Ratings

|                    |                         |  | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2000 | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

|                   |  | MIN   | NOM | MAX  | UNIT   |
|-------------------|--|-------|-----|------|--------|
| V <sub>IN</sub>   | Supply voltage V <sub>IN</sub>   | 1.8   |     | 6.5  | V      |
| L                 | Effective inductance   | 1.51  | 2.2 | 2.9  | μH     |
| C <sub>OUT</sub>  | Effective output capacitance   | 3     | 10  | 40   | μF     |
| C <sub>IN</sub>   | Effective input capacitance  | 1     | 4.7 |      | μF     |
| C <sub>VSET</sub> | External parasitic capacitance at VSET pin   |       |     | 100  | pF     |
| R <sub>SET</sub>  | Nominal resistance range for external voltage selection resistor (E96 resistor series) | 0.909 |     | 267  | kΩ     |
|                   | External voltage selection resistor tolerance  |       |     | 1%   |        |
|                   | External voltage selection resistor temperature coefficient                            |       |     | ±200 | ppm/°C |
| T <sub>J</sub>    | Operating junction temperature range   | -40   |     | 125  | °C     |

## 7.4 Thermal Information

| THERMAL METRIC        |  | DLC Package    | YBG Package | DGR Package    | UNIT |
|-----------------------|--|----------------|-------------|----------------|------|
|                       |  | JEDEC PCB 51-7 |             | JEDEC PCB 51-5 |      |
| R <sub>θJA</sub>      | Junction-to-ambient thermal resistance       | 106.2          | 133.4       | 63.4           | °C/W |
| R <sub>θJC(top)</sub> | Junction-to-case (top) thermal resistance    | n/a            | 0.4         | 53.0           | °C/W |
| R <sub>θJB</sub>      | Junction-to-board thermal resistance         | n/a            | 39.4        | 37.4           | °C/W |
| Ψ <sub>JT</sub>       | Junction-to-top characterization parameter   | 2.5            | 0.1         | 3.7            | °C/W |
| Ψ <sub>JB</sub>       | Junction-to-board characterization parameter | 32.1           | 39.4        | 37.1           | °C/W |
| R <sub>θJC(bot)</sub> | Junction-to-case (bottom) thermal resistance | n/a            | n/a         | 13.5           | °C/W |

## 7.5 Electrical Characteristics

 $V_{IN} = 3.6\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , STOP = GND, MODE = GND, typical values are at  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                    |  | TEST CONDITIONS  | MIN | TYP  | MAX  | UNIT       |
|------------------------------|--|--|-----|------|------|------------|
| <b>SUPPLY</b>                |  |  |     |      |      |            |
| $I_{Q\_NO\_LOAD}$            | No load operating input current            | EN = $V_{IN}$ , $I_{OUT} = 0\mu\text{A}$ , $V_{OUT} = 1.8\text{V}$<br>MODE = GND, device switching   |     | 60   |      | nA         |
| $I_{Q\_NO\_LOAD}$            | No load operating input current            | EN = $V_{IN}$ , $I_{OUT} = 0\mu\text{A}$ , $V_{OUT} = 1.2\text{V}$ , MODE = GND<br>device switching  |     | 80   |      | nA         |
| $I_{Q\_NO\_LOAD}$            | No load operating input current (PWM Mode) | EN = $V_{IN}$ , $I_{OUT} = 0\mu\text{A}$ , $V_{OUT} = 1.8\text{V}$ , MODE = $V_{IN}$<br>device switching   |     | 3    |      | mA         |
| $I_{Q\_VIN}$                 | Operating quiescent current into pin VIN   | EN = $V_{IN}$ , $I_{OUT} = 0\mu\text{A}$ , $V_{OUT} = 1.55\text{V}$ or $V_{OUT} = 1.8\text{V}$<br>MODE = GND, device not switching, $T_J = 25^\circ\text{C}$<br>(DLC package option) |     | 36   | 100  | nA         |
| $I_{Q\_VOS}$                 | Operating quiescent current into pin VOS   | EN = $V_{IN}$ , $I_{OUT} = 0\mu\text{A}$ , $V_{OUT} = 1.55\text{V}$ or $V_{OUT} = 1.8\text{V}$<br>MODE = GND, device not switching, $T_J = 25^\circ\text{C}$<br>(DLC package option) |     | 56   | 120  | nA         |
| $I_{Q\_VIN}$                 | Operating quiescent current into pin VIN   | EN = $V_{IN}$ , $I_{OUT} = 0\mu\text{A}$ , $V_{OUT} = 1.55\text{V}$ or $V_{OUT} = 1.8\text{V}$<br>MODE = GND, device not switching, $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$  |     | 36   | 360  | nA         |
| $I_{Q\_VOS}$                 | Operating quiescent current into pin VOS   | EN = $V_{IN}$ , $I_{OUT} = 0\mu\text{A}$ , $V_{OUT} = 1.55\text{V}$ or $V_{OUT} = 1.8\text{V}$<br>MODE = GND, device not switching, $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$  |     | 56   | 170  | nA         |
| $I_{Q\_VOS}$                 | Operating quiescent current into VOS pin   | EN = $V_{IN}$ , $V_{OUT} = 3.3\text{V}$ , MODE = GND<br>device not switching   |     | 70   |      | nA         |
|                              |  | EN = $V_{IN}$ , $V_{OUT} < 1.5\text{V}$ , MODE = GND<br>device not switching   |     | 5    |      | nA         |
|                              |  | EN, STOP = $V_{IN}$ , $3\text{V} < V_{OUT} < 3.3\text{V}$ , MODE = GND<br>$T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$  |     | 5    | 100  | nA         |
| $I_{Q\_100\%\_MODE}$         | Operating quiescent current 100% Mode      | $V_{IN} = V_{OUT} = 3.3\text{V}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$   |     | 120  |      | nA         |
| $I_{Q\_VIN\_STOP}$           | Operating quiescent current into pin VIN   | STOP = High, $V_{OUT} = 1.8\text{V}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$   |     | 70   | 175  | uA         |
| $I_{SD}$                     | Shutdown current                           | EN = GND, shutdown current into $V_{IN}$<br>VSET = GND, MODE = GND, $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$  |     | 25   | 300  | nA         |
| $V_{TH\_UVLO+}$              | Undervoltage lockout threshold             | Rising $V_{IN}$  |     | 1.72 | 1.8  | V          |
| $V_{TH\_UVLO-}$              |  | Falling $V_{IN}$   |     | 1.45 | 1.75 | V          |
| <b>EN, MODE, STOP INPUTS</b> |  |  |     |      |      |            |
| $V_{IH\_TH}$                 | High level input voltage                   |  | 1.1 |      |      | V          |
| $V_{IL\_TH}$                 | Low level input voltage                    |  |     |      | 0.4  | V          |
| $I_{IN}$                     | Input bias current                         | $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$  |     | 1    | 25   | nA         |
| $R_{PD}$                     | Internal pull-down resistance              | EN, STOP inputs  | 200 | 450  |      | k $\Omega$ |

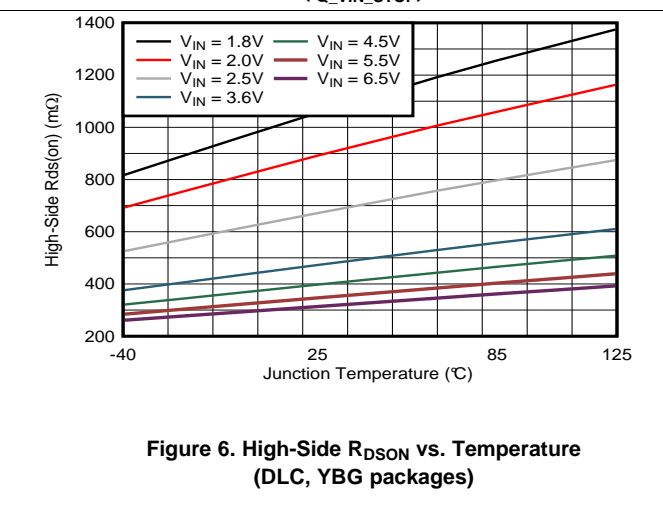
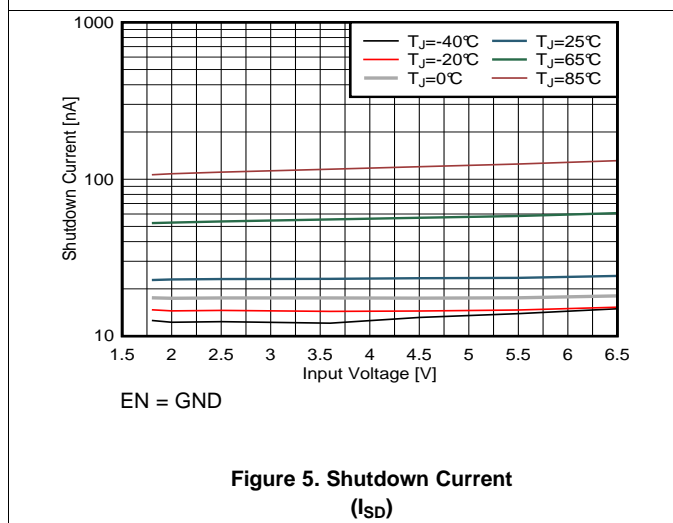
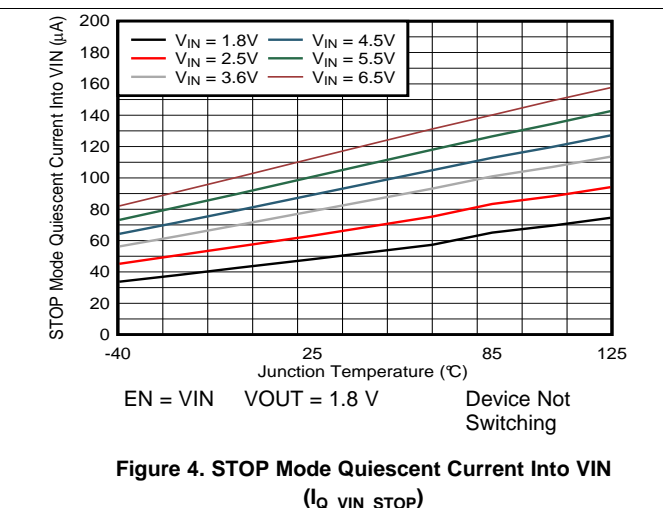
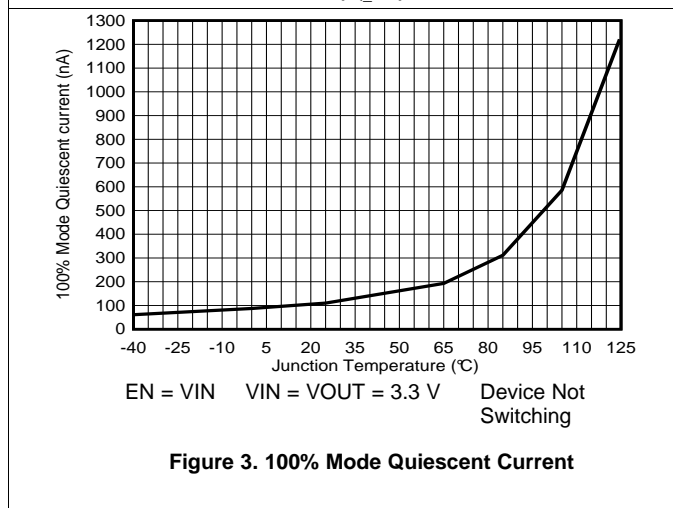
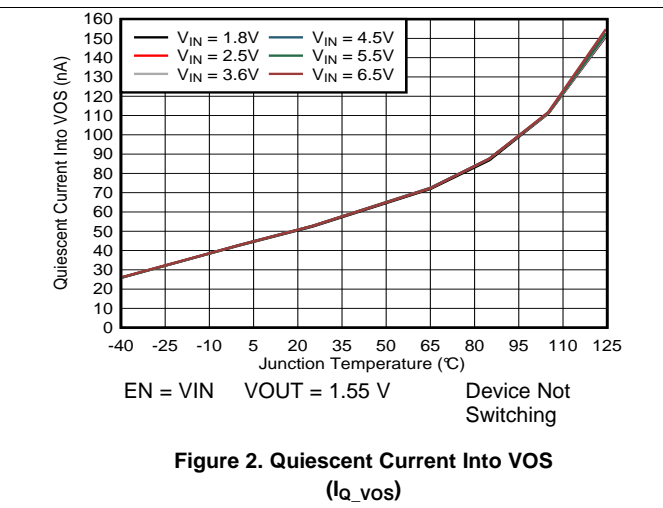
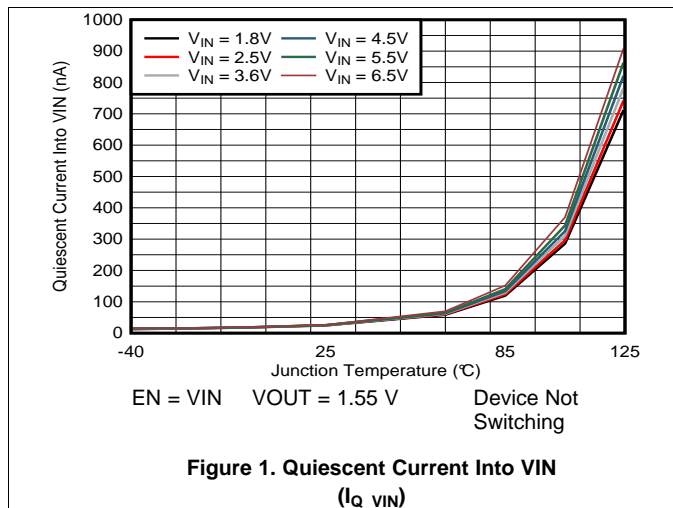
## Electrical Characteristics (continued)

 $V_{IN} = 3.6\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , STOP = GND, MODE = GND, typical values are at  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER                                      |   | TEST CONDITIONS  | MIN  | TYP   | MAX        | UNIT             |
|--|---|--|------|-------|------------|------------------|
| <b>POWER SWITCHES</b>                          |   |  |      |       |            |                  |
| $R_{DS(ON)}$                                   | High-side MOSFET on-resistance (SON, WCSP package)  | $V_{IN} = 3.6\text{V}$ , $I = 200\text{mA}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$                                    |      | 430   | 600        | m $\Omega$       |
|  |   | $V_{IN} = 5\text{V}$ , $I = 200\text{mA}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$                                      |      | 340   | 465        |                  |
|  | Low-side MOSFET on-resistance (SON, WCSP package)   | $V_{IN} = 3.6\text{V}$ , $I = 200\text{mA}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$                                    |      | 170   | 240        | m $\Omega$       |
|  |   | $V_{IN} = 5\text{V}$ , $I = 200\text{mA}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$                                      |      | 135   | 180        |                  |
|  | High-side MOSFET on-resistance (HVSSOP package)   | $V_{IN} = 3.6\text{V}$ , $I = 200\text{mA}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$                                    |      | 460   | 630        | m $\Omega$       |
|  |   | $V_{IN} = 5\text{V}$ , $I = 200\text{mA}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$                                      |      | 370   | 495        |                  |
| Low-side MOSFET on-resistance (HVSSOP package) | $V_{IN} = 3.6\text{V}$ , $I = 200\text{mA}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$ |  | 200  | 270   | m $\Omega$ |                  |
|  | $V_{IN} = 5\text{V}$ , $I = 200\text{mA}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$   |  | 165  | 210   |            |                  |
| $I_{LIM\_SS}$                                  | Soft-start switch current limit   | open-loop  | 0.15 | 0.225 | 0.3        | A                |
| $I_{LIMF}$                                     | High-side MOSFET switch current limit   | open-loop  | 1.0  | 1.2   | 1.4        | A                |
|  | Low-side MOSFET switch current limit  | open-loop  |      | 1.0   |            | A                |
| $I_{LIM\_DELAY}$                               | Current limit propagation delay   |  |      | 50    |            | ns               |
| $I_{LKG\_SW}$                                  | Leakage current into SW pin   | $V_{SW} = 1.8\text{V}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$   |      | 10    |            | nA               |
| <b>OUTPUT VOLTAGE DISCHARGE</b>                |   |  |      |       |            |                  |
| $I_{DISCHARGE\_VOS}$                           | Output discharge current  | EN = GND, sink current into VOS pin, over VIN range<br>$V_{OUT} = 1.8\text{V}$ , $T_J = -40^\circ\text{C}$ to $85^\circ\text{C}$ | 16   | 35    | 44         | mA               |
| <b>THERMAL PROTECTION</b>                      |   |  |      |       |            |                  |
| $T_{SD}$                                       | Thermal shutdown temperature  | Rising junction temperature  |      | 160   |            | $^\circ\text{C}$ |
|  | Thermal shutdown hysteresis   |  |      | 5     |            | $^\circ\text{C}$ |
| <b>OUTPUT</b>                                  |   |  |      |       |            |                  |
| $V_{OUT}$                                      | Output voltage accuracy   | PWM Mode. $I_{OUT} = 0\text{ mA}$ , $V_{OUT} > 1.8\text{ V}$   | -1.5 | 0     | 1.5        | %                |
|  |   | PWM Mode. $I_{OUT} = 0\text{ mA}$ , $V_{OUT} \leq 1.55\text{ V}$   | -2   | 0     | 2          | %                |
| $V_{OUT}$                                      | DC output voltage load regulation   | PWM Mode   |      | 0     |            | %/mA             |
|  | DC output voltage line regulation   | PWM Mode<br>$V_{OUT} = 1.8\text{V}$ , $I_{OUT} = 200\text{ mA}$ , over VIN range   |      | 0     |            | %/V              |
| $f_{SW}$                                       | Switching frequency   | $V_{IN} = 3.6\text{V}$ , $V_{OUT} = 1.8\text{V}$ , MODE = $V_{IN}$<br>$I_{OUT} = 0\text{mA}$                                     |      | 1.8   |            | MHz              |
| $t_{STARTUP\_DELAY}$                           | Regulator start up delay time   | $V_{IN} = 3.6\text{V}$ , from EN = low to high until device starts switching   |      |       | 200        | $\mu\text{s}$    |
| $t_{SS}$                                       | Soft-start time   | $I_{OUT} = 0\text{mA}$   |      | 120   |            | $\mu\text{s}$    |
| $t_{SS\_ILIMF}$                                | Reduced current limit soft-start timeout  |  |      | 700   | 1200       | $\mu\text{s}$    |



## 7.6 Typical Characteristics



Typical Characteristics (continued)

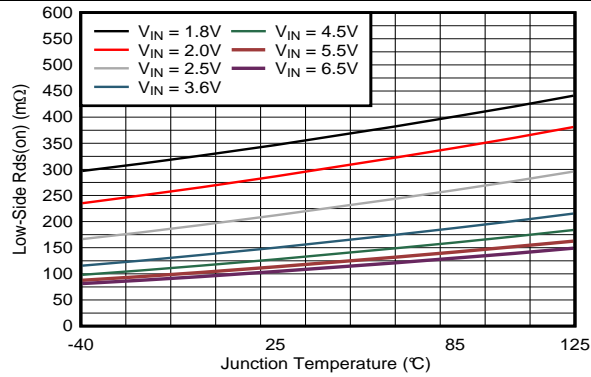


Figure 7. Low-Side  $R_{DS(on)}$  vs. Temperature (DLC, YBG packages)

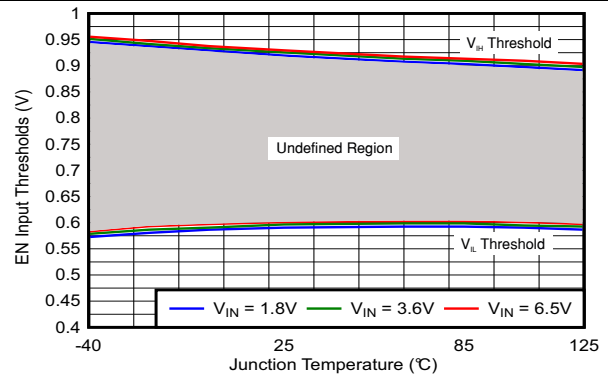


Figure 8. EN Input Thresholds vs. Temperature

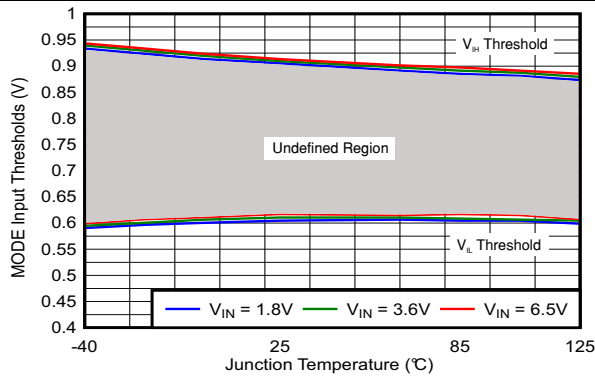


Figure 9. MODE Input Thresholds vs. Temperature

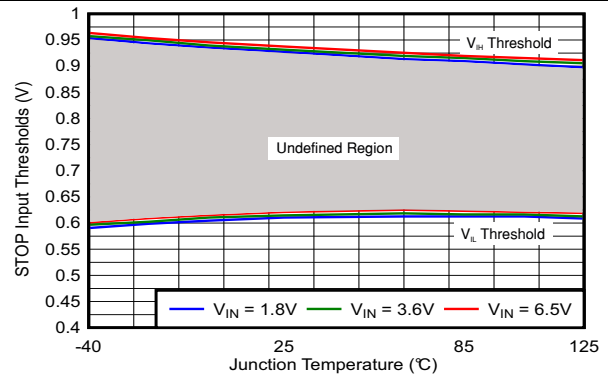


Figure 10. STOP Input Thresholds vs. Temperature

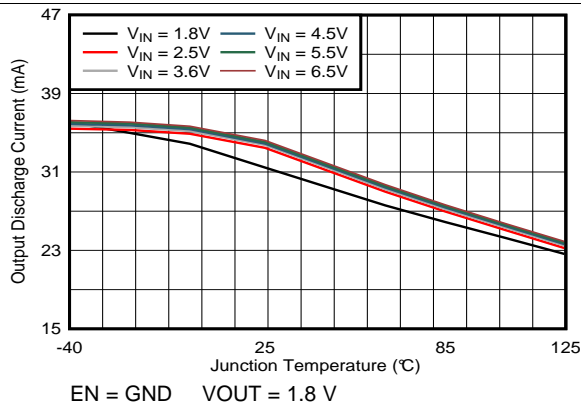


Figure 11. Output Discharge Current vs. Temperature

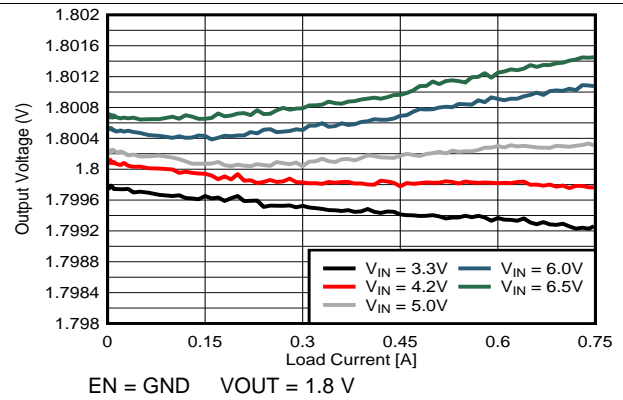
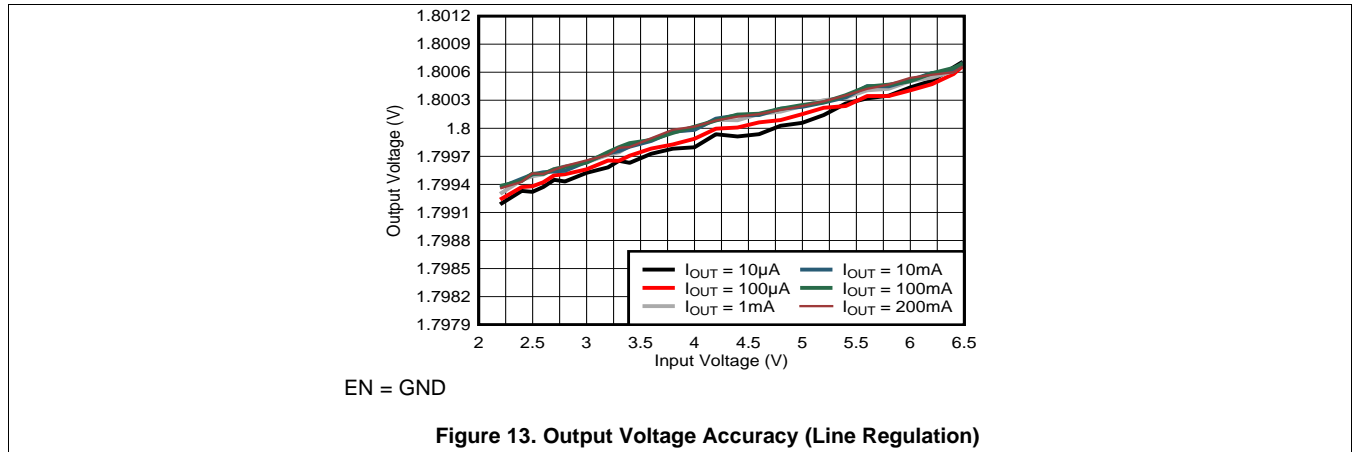


Figure 12. Output Voltage Accuracy (Load Regulation)

Typical Characteristics (continued)



## 8 Detailed Description

### 8.1 Overview

The TPS6284x is a synchronous step-down converter with ultra-low quiescent current consumption. Using TI's DCS-Control™ topology the device extends the high efficiency operation area down to micro amperes of load current during Power-Save Mode Operation.

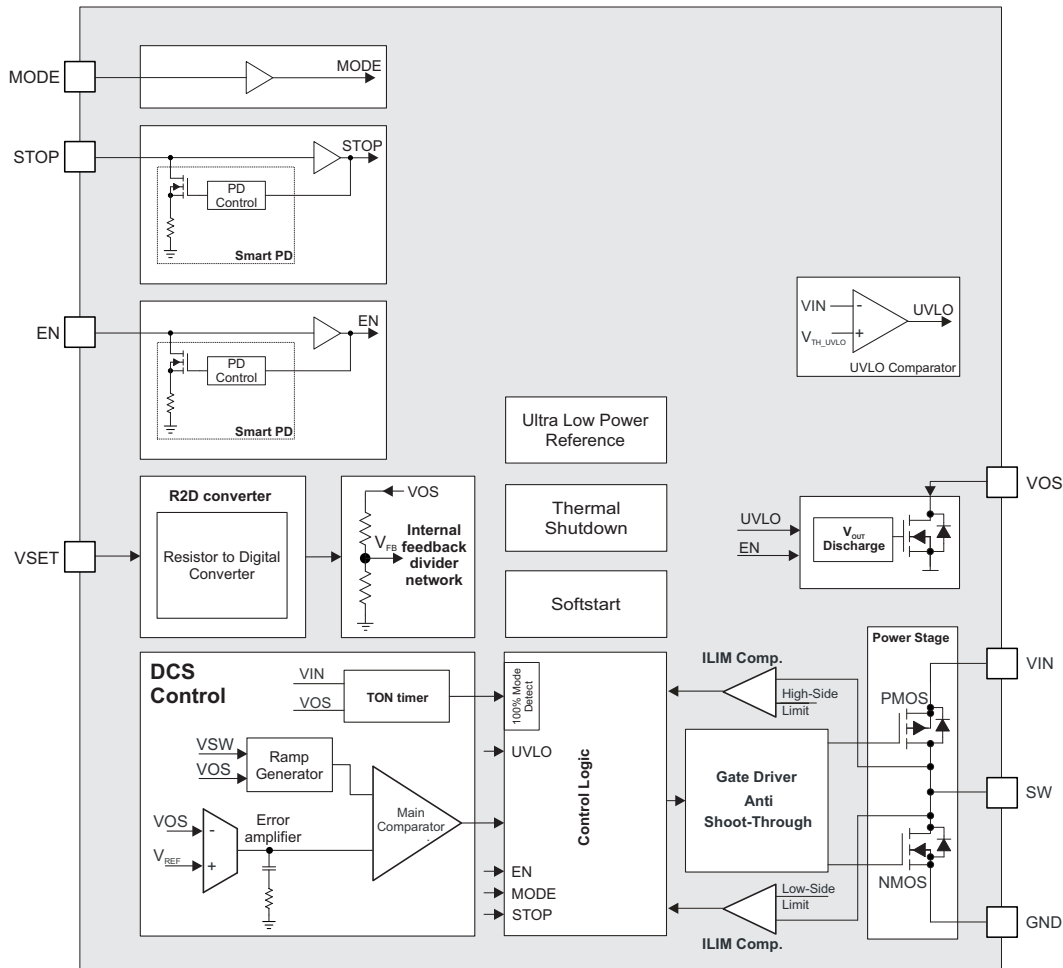
DCS-Control™ (Direct Control with Seamless Transition into Power-Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode controls. Characteristics of DCS-Control™ are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between PFM and PWM modes. It includes a AC loop which senses the output voltage (VOS pin) and directly feeds this information into a fast comparator stage.

The device operates with a nominal switching frequency of 1.8MHz. An additional voltage feedback loop is used to achieve accurate DC load regulation. To save extra quiescent current under light load condition (i.e.  $I_{OUT}$  in the mA range), the internal error amplifier is powered down with a minimum influence on the DC line and load regulation characteristic. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

In Power-Save Mode, the switching frequency varies linearly with the load current. Since DCS-Control™ supports both operating modes, the transition from PWM to PFM is seamless with minimum output voltage ripple. The TPS6284x offers both, excellent DC voltage and superior load transient regulation, combined with low output voltage ripple thereby minimizing interferences with Radio Frequency circuits.

Depending on the output voltage, the device consumes quiescent current from both the input and output to reduce the overall input current consumption to 60 nA typical.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Smart Enable and Shutdown

To avoid a floating input an internal 450kΩ resistor pulls the EN pin to GND. This prevents an uncontrolled start-up of the device in case the EN pin can not be driven low safely. The device is in shutdown mode when the EN input is logic low.

The device turns on with a logic high EN signal. An internal control circuit disconnects the EN pin pull-down resistor once the device has finished soft-start and the output voltage is in regulation. With the EN pin set low, the device enters shutdown mode and the pull-down resistor is activated again.

### 8.3.2 Soft-start

In order to protect the battery and system from excessive inrush current, the device features a soft-start of the output voltage.

Once the device has been enabled, it initializes and powers up its internal circuits. This occurs during the regulator start-up delay time ( $t_{STARTUP\_DELAY}$ ). Once this delay expires, the device enters soft-start, starts switching and ramps up the output voltage.

The device operates with a reduced switch current limit ( $I_{LIMF\_SS}$ ) throughout the entire soft-start phase ( $t_{SS}$ ). The switch current limit is increased to its nominal value ( $I_{LIMF}$ ) once the output voltage has reached its nominal value or the reduced current limit soft-start time ( $t_{SS\_ILIMF}$ ) has expired, whichever occurs first. The soft-start phase ( $t_{SS}$ ) can last up to approx. 700μs. Figure 14 shows the startup procedure.

Feature Description (continued)

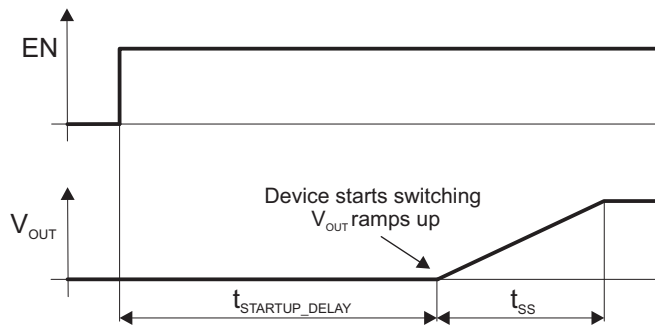


Figure 14. Device Startup

8.3.3 Mode Selection: Power-Save Mode (PFM/PWM) or Forced PWM Operation (FPWM)

Connecting the MODE input to GND enables the automatic PWM and power-save mode operation. The converter operates in PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in PWM mode even at light load currents. That allows lower ripple compared to PFM mode switching. In this mode, the efficiency is lower compared to the power-save mode during light loads. For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

This Pin is not available in YBG package option where the device automatically transits between power-save and PWM modes.

8.3.4 Output Voltage Selection (VSET)

The output voltage is set with a single external resistor connected between the VSET pin and GND. Once the device has been enabled and the control logic as well as the reference system are powered-up, an R2D (resistor to digital) conversion is started to detect the value of the external R<sub>SET</sub> resistor. A pre-defined fixed output voltage is set based on the R<sub>SET</sub> value. The output voltage is preset once during the device startup delay phase.

Once the output voltage is preset, the R2D converter is turned-off to avoid current flowing through the R<sub>SET</sub>. Care must be taken that no parasitic current and/or capacitance greater than 100pF is present between the VSET and GND pins. This could cause false R<sub>SET</sub> readings and a faulty output voltage to be set. The R2D converter is designed to operate with resistor values out of E96 series. Table 1 shows the allowed R<sub>SET</sub> values.

**Feature Description (continued)**
**Table 1. Output Voltage Setting, R<sub>SET</sub> Resistor**

| Output voltage setting V <sub>OUT</sub> [V] |             |             | VSET resistance to GND - E96 values[Ω] |        |         |
|---|-------------|-------------|--|--------|---------|
| TPS62841YBG                                 | TPS62840YBG | TPS62842DGR | MIN                                    | NOM    | MAX     |
| TPS62841DLC                                 | TPS62840DLC |             |  |        |         |
| 0.8   | 1.8         | 1.8         | 0                                      | GND    | 0.01k   |
| 0.85  | 1.9         | 2.0         | 0.87k                                  | 0.909k | 0.95k   |
| 0.9   | 2.0         | 2.2         | 1.67k                                  | 1.74k  | 1.81k   |
| 0.95  | 2.1         | 2.4         | 2.76k                                  | 2.87k  | 2.98k   |
| 1.0   | 2.2         | 2.5         | 4.15k                                  | 4.32k  | 4.49k   |
| 1.05  | 2.3         | 2.6         | 5.80k                                  | 6.04k  | 6.28k   |
| 1.1   | 2.4         | 2.7         | 8.11k                                  | 8.45k  | 8.79k   |
| 1.15  | 2.5         | 2.8         | 11.04k                                 | 11.5k  | 11.96k  |
| 1.2   | 2.6         | 2.9         | 15.17k                                 | 15.8k  | 16.43k  |
| 1.25  | 2.7         | 3.0         | 20.64k                                 | 21.5k  | 22.36k  |
| 1.3   | 2.8         | 3.1         | 27.55k                                 | 28.7k  | 29.85k  |
| 1.35  | 2.9         | 3.2         | 36.77k                                 | 38.3k  | 39.83k  |
| 1.4   | 3.0         | 3.3         | 50.21k                                 | 52.3k  | 54.39k  |
| 1.45  | 3.1         | 3.4         | 68.64k                                 | 71.5k  | 74.36k  |
| 1.5   | 3.2         | 3.49        | 97.92k                                 | 102k   | 106.08k |
| 1.55  | 3.3         | 3.59        | 256.32k                                | 267k   | 277.68k |

**8.3.5 Undervoltage Lockout UVLO**

To avoid mis-operation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input below the threshold V<sub>TH\_UVLO-</sub> with falling V<sub>IN</sub>. The device starts at an input voltage higher than the threshold V<sub>TH\_UVLO+</sub> with rising V<sub>IN</sub>.

When the device resumes operation from an under voltage lockout condition, it behaves like being enabled. This means the internal control logic is powered up, the external R<sub>SET</sub> resistor is read out and a soft-start sequence is initiated.

**8.3.6 Switch Current Limit / Short Circuit Protection**

The TPS6284x integrates a current limit on the high-side as well as on the low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle-by-cycle. If the high-side MOSFET current limit (I<sub>LIMF</sub>) trips, the high-side element is turned off and the low-side MOSFET is turned on to ramp the inductor current down. Once the inductor current decreases below the low-side current limit (I<sub>LIMF</sub>), the low-side device is turned off and the high-side MOSFET turns on again.

During soft-start, the current limit is reduced to I<sub>LIMF\_SS</sub>. After soft-start has finished, the current limit value increases to the normal value I<sub>LIMF</sub>.

Due to internal propagation delay, the actual inductor current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD} \quad (1)$$

where

- I<sub>LIMF</sub> is the static current limit, specified in the ,
- L is the inductance,
- V<sub>L</sub> is the voltage across the inductor (V<sub>IN</sub> - V<sub>OUT</sub>) and
- t<sub>PD</sub> is the internal propagation delay.

### 8.3.7 Output Voltage Discharge of the Buck Converter

The purpose of the output discharge function is to ensure a defined ramp-down of the output voltage when the device is disabled.

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. It is not active during Thermal Shutdown. The minimum supply voltage required to ensure the discharge function is always active is  $V_{IN} > V_{TH\_UVLO}$ .

### 8.3.8 Thermal Shutdown

The junction temperature ( $T_J$ ) of the device is monitored by an internal temperature sensor. The device enters thermal shutdown when the junction temperature exceeds the thermal shutdown threshold ( $T_{SD}$ ) of 160°C (typ.). Both the high-side and low-side power FETs are turned-off. The device continues its operation when the junction temperature falls below typically 155°C again. The converter resumes operation by beginning with a soft-start cycle without reading  $R_{SET}$  again. In Power-Save Mode, the thermal shutdown feature is not active during skip pause.



### 8.3.9 STOP Mode

The TPS6284x includes the STOP input pin, allowing the user to temporarily stop the regulator switching regardless of the mode of operation.

When a logic high level is applied to the STOP pin, the regulator is forced to stop switching after the current switching cycle. The application is powered by the charge available in the output capacitor. No switching noise is generated which could be beneficial in noise sensitive sampled applications.

An MCU controlling this pin needs to take care to turn the device back on before the output voltage reaches a system critical level. Should this not happen, the output voltage will be clamped to about 0.5V below the set output voltage. In STOP mode, the device consumes typically 90µA operating quiescent current from the input supply.

When a logic low level is applied to the STOP pin, the regulator immediately resumes switching operation without a startup delay or soft start. To avoid a floating input an internal 450kΩ resistor pulls the STOP pin to GND. A control circuit disconnects the pull-down resistor at the STOP pin once a high level has been detected (similarly to the EN pin).

## 8.4 Device Functional Modes

### 8.4.1 Power-Save Mode Operation

The DCS-Control™ topology supports Power-Save Mode operation. The device operates at light loads in PFM (Pulse Frequency Modulation) mode that generates a single switching pulse to ramp-up the inductor current and recharges the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typically 60nA. This low quiescent current consumption is achieved by an ultra-low power reference, an integrated high impedance feedback divider network and an optimized Power-Save Mode operation. To achieve a stable switching frequency in a steady state condition, the on-time is calculated as in [Equation 2](#).

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 556\text{ns} \quad (2)$$

In PFM Mode, the switching frequency varies linearly with the load current. At medium and high load conditions, the device enters automatically PWM (Pulse Width Modulation) mode and operates in continuous conduction mode with a nominal switch frequency ( $f_{sw}$ ). The switching frequency in PWM mode is controlled and depends on  $V_{IN}$  and  $V_{OUT}$ . The boundary between PWM and PFM mode is when the inductor current becomes discontinuous. In PFM, the device operates with a fixed on-time and the switching frequency further decreases proportional to the load current. It can be calculated as in [Equation 3](#)

$$f_{PSM} = \frac{2 \cdot I_{OUT}}{T_{ON}^2 \cdot \frac{V_{IN}}{V_{OUT}} \left[ \frac{V_{IN} - V_{OUT}}{L} \right]} \quad (3)$$

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to ultra-light loads. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to PFM modes is seamless with minimum output voltage ripple.

### 8.4.2 Forced PWM Mode Operation

With a high level on the MODE input, the device enters forced PWM Mode and operates with a quasi-constant switching frequency over the entire load range, even at very light loads. This reduces or eliminates interference with RF and noise sensitive circuits, but reduces efficiency at light loads.

## Device Functional Modes (continued)

### 8.4.3 100% Mode Operation

In PWM mode, the duty-cycle of a buck converter is given as  $D = V_{OUT}/V_{IN}$ . The duty-cycle increases as the input voltage comes closer to the output voltage. As the input voltage decreases to the point the on-time reaches  $1.6\mu\text{s}$ , the nominal output set point is offset by  $+30\text{mV}$ . Once the input voltage decreases to near 100% duty cycle, the output voltage set point is increased by  $+30\text{mV}$ . As the input voltage decreases further, the device enters 100% duty-cycle mode and keeps the high-side switch on continuously. The output ( $V_{OUT}$ ) is connected to the input ( $V_{IN}$ ) via the inductor and the internal high-side MOSFET switch. The minimum input voltage to maintain a given output voltage depends on the load current and is calculated as:

$$V_{INmin} = V_{OUTmax} + I_{OUTmax} \times (R_{DS(on)max} + R_L)$$

where

- $I_{OUTmax}$  = Maximum output current plus inductor ripple current
- $R_{DS(on)max}$  = Maximum P-channel switch  $R_{DS(on)}$
- $R_L$  = DC resistance of the inductor
- $V_{OUTmax}$  = Nominal output voltage plus maximum output voltage tolerance

The TPS6284x contains special circuitry to keep an ultra-low  $I_Q$  of  $150\text{nA}$  during 100% mode operation.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

### 9.2 Typical Application

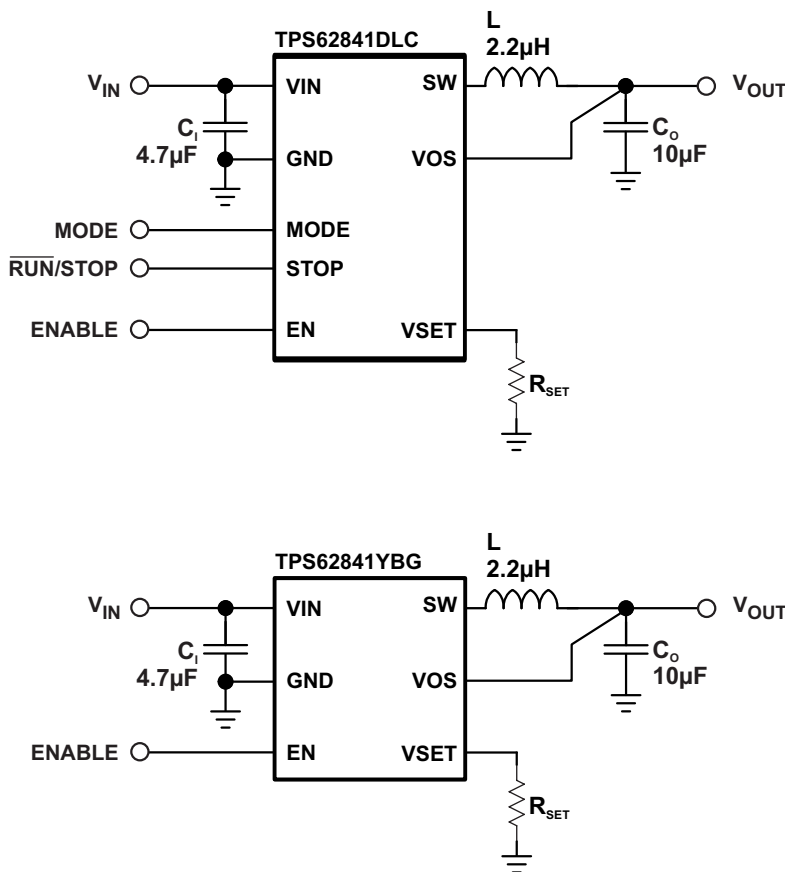


Figure 15. TPS6284x Adjustable  $V_{OUT}$  Application Circuit

Additional circuits are shown in the [System Examples](#) section.

#### 9.2.1 Design Requirements

Table 2 shows the list of components for the application circuit and the characteristic application curves

Table 2. Components for Application Characteristic Curves

| Reference | Description                  | Value | Size [L x W x T] | Manufacturer <sup>(1)</sup> |
|-----------|------------------------------|-------|------------------|-----------------------------|
| IC        | TPS6284x step-down converter |       |                  | TI                          |

(1) See [Third-party Products Disclaimer](#)

Typical Application (continued)

Table 2. Components for Application Characteristic Curves (continued)

| Reference        | Description                          | Value              | Size [L x W x T]                    | Manufacturer <sup>(1)</sup> |
|------------------|--------------------------------------|--------------------|-------------------------------------|-----------------------------|
| C <sub>I</sub>   | GRM155R61A475MEAAD ceramic capacitor | 4.7 μF / 10V / X5R | (0402) [1mm x 0.5mm x 0.65mm max.]  | muRata                      |
| C <sub>O</sub>   | GRM155R60G106ME44D ceramic capacitor | 10 μF / 4V / X5R   | (0402) [1mm x 0.5mm x 0.65mm max.]  | muRata                      |
| L                | DFE201612E-2R2M=P2 inductor          | 2.2 μH / 116mΩ DCR | (2016) [2.0mm x 1.6mm x 1.2mm max.] | muRata                      |
| R <sub>SET</sub> | Resistor E96 series 1%, TC ±200ppm   | see Table 1        |                                     |                             |

9.2.2 Detailed Design Procedure

The inductor and output capacitor together provide a low-pass filter. To simplify this process, Table 3 outlines possible inductor and capacitor value combinations.

Table 3. Recommended LC Output Filter Combinations

| Inductor Value [μH] <sup>(1)</sup> | Output Capacitor Value [μF] <sup>(2)</sup> |      |
|------------------------------------|--|------|
|                                    | 10μF                                       | 22μF |
| 2.2                                | √ <sup>(3)</sup>                           | √    |

- (1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -20%.
- (2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance varies by +20% and -50%.
- (3) Typical application configuration. Other check marks indicate alternative filter combinations.

9.2.2.1 Inductor Selection

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI<sub>L</sub>) decreases with higher inductance and increases with higher V<sub>IN</sub> or V<sub>OUT</sub> and can be estimated according to Equation 4.

Equation 5 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, as calculated with Equation 5. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high-side MOSFET switch current limit, I<sub>LIMF</sub>.

$$\Delta I_L = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \tag{4}$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

where

- f = Switching Frequency
  - L = Inductance
  - ΔI<sub>L</sub> = Peak to Peak inductor ripple current
  - I<sub>Lmax</sub> = Maximum Inductor current
- (5)

The table below shows a list of possible inductors.

Table 4. List of Possible Inductors<sup>(1)</sup>

| INDUCTANCE [μH] | INDUCTOR TYPE | SIZE [L x W x T]             | SUPPLIER |
|-----------------|---------------|------------------------------|----------|
| 2.2             | DFE201612     | [2.0mm x 1.6mm x 1.2mm max.] | muRata   |

(1) See [Third-party Products Disclaimer](#)

### 9.2.2.2 Output Capacitor Selection

The DCS-Control™ scheme of the TPS62840 allows the use of tiny ceramic capacitors. Ceramic capacitors with low-ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric.

At light load currents, the converter operates in Power-Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple. The leakage current of the output capacitor adds to the overall quiescent current.

**Table 5. List of Possible Capacitors<sup>(1)</sup>**

| CAPACITOR VALUE [μF] | CAPACITOR TYPE     | SIZE IMPERIAL (METRIC) | SIZE [L x W x T]            | SUPPLIER |
|----------------------|--------------------|------------------------|-----------------------------|----------|
| 10                   | GRM155R60G106ME44D | 0402 (1005)            | [1mm x 0.5mm x 0.65mm max.] | muRata   |

(1) See [Third-party Products Disclaimer](#)

### 9.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications a 4.7-μF input capacitor is sufficient.

When operating from a high impedance source, a larger input buffer capacitor is recommended avoiding voltage drops during start-up and load transients.

The input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall quiescent current. [Table 6](#) shows a selection of input and output capacitors.

**Table 6. List of Possible Capacitors<sup>(1)</sup>**

| CAPACITOR [μF] | CAPACITOR TYPE      | SIZE IMPERIAL (METRIC) | SIZE [L x W x T]             | SUPPLIER |
|----------------|---------------------|------------------------|------------------------------|----------|
| 4.7            | GRM155R61A475MEAAD  | 0402 (1005)            | [1mm x 0.5mm x 0.65mm max.]  | muRata   |
| 4.7            | GRM31CR71H475MA12L  | 1206 (3216)            | [3.2mm x 1.6mm x 1.8mm max.] | muRata   |
| 4.7            | C1608X7S1A475M080AC | 0603 (1608)            | [1.6mm x 0.8mm x 1.0mm max.] | TDK      |
| 10             | GRM155R60J106ME15D  | 0402 (1005)            | [1mm x 0.5mm x 0.65mm max.]  | muRata   |

(1) See [Third-party Products Disclaimer](#)

### 9.2.3 Application Curves

The condition for below application curves are  $V_{IN} = 3.6V$ ,  $V_{OUT} = 1.8V$ , MODE = GND, STOP = GND and the used components listed in Table 2, unless otherwise noted.

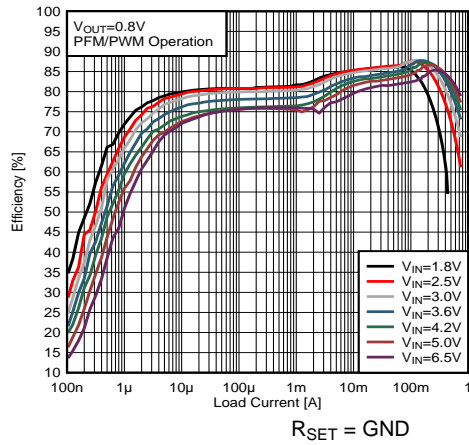


Figure 16. Efficiency Power Save Mode  
 $V_{OUT} = 0.8V$

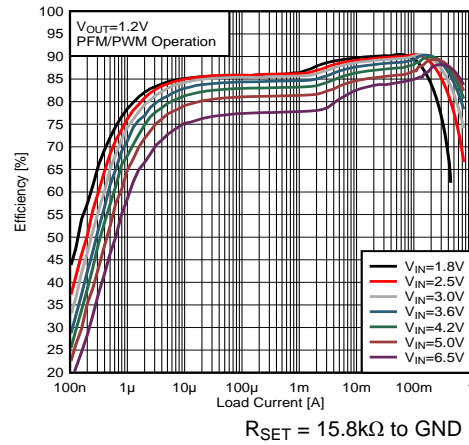


Figure 17. Efficiency Power Save Mode  
 $V_{OUT} = 1.2V$

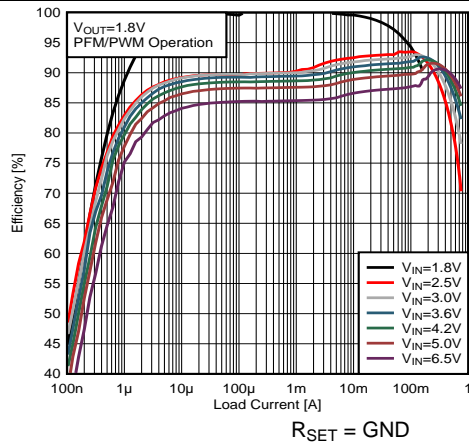


Figure 18. Efficiency Power Save Mode  
 $V_{OUT} = 1.8V$

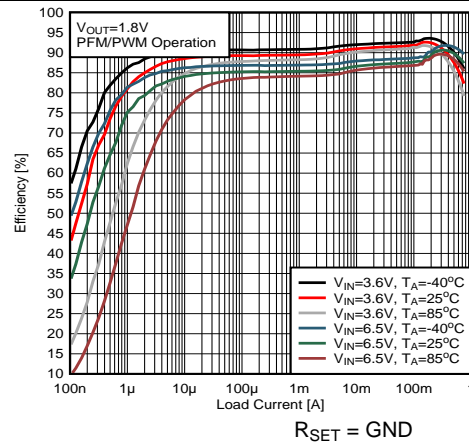


Figure 19. Efficiency Power Save Mode  
 $V_{OUT} = 1.8V$

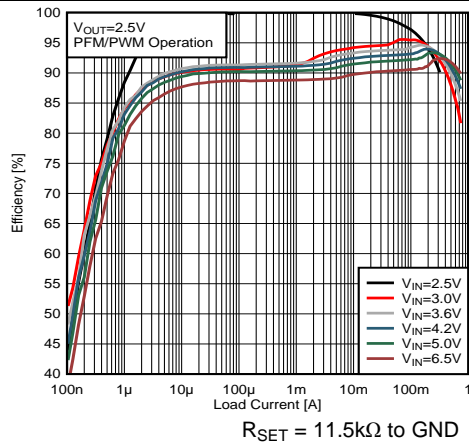


Figure 20. Efficiency Power Save Mode  
 $V_{OUT} = 2.5V$

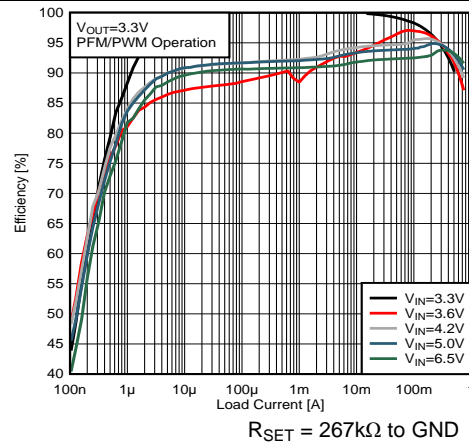


Figure 21. Efficiency Power Save Mode  
 $V_{OUT} = 3.3V$

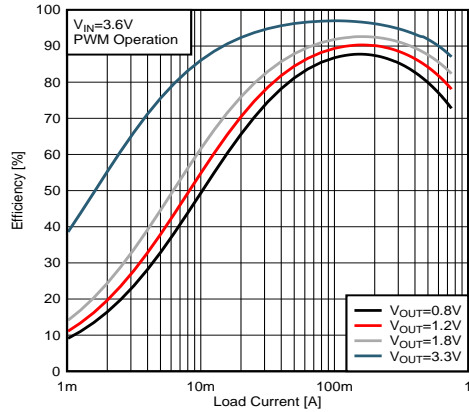


Figure 22. Efficiency Forced PWM Mode  
V<sub>OUT</sub> = 0.8V / 1.2V / 1.8V / 3.3V

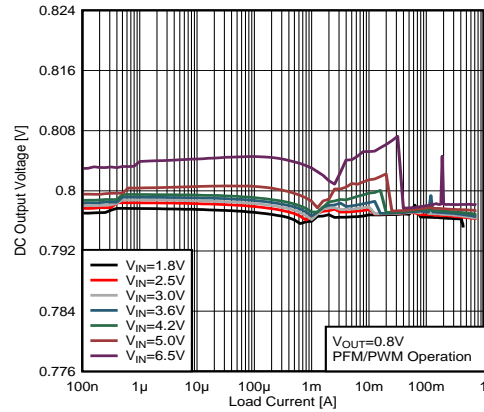


Figure 23. Output Voltage vs. Load Current  
V<sub>OUT</sub> = 0.8V

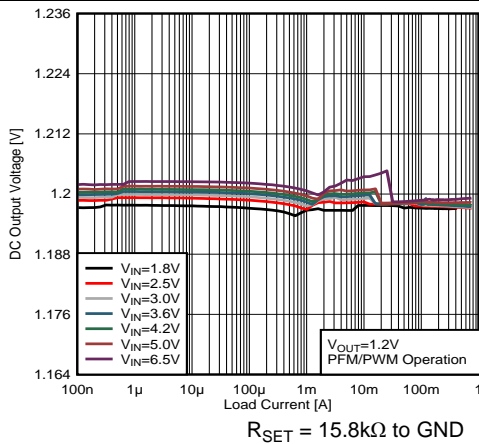


Figure 24. Output Voltage vs. Load Current  
V<sub>OUT</sub> = 1.2V

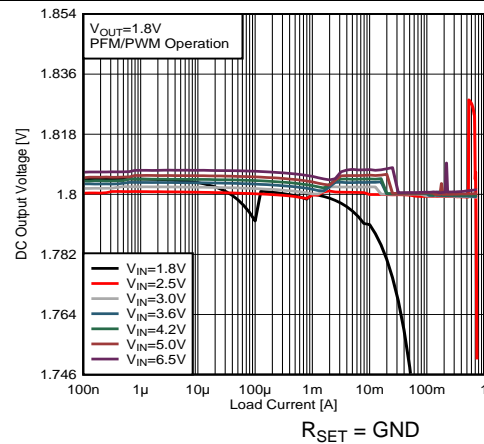


Figure 25. Output Voltage vs. Load Current  
V<sub>OUT</sub> = 1.8V

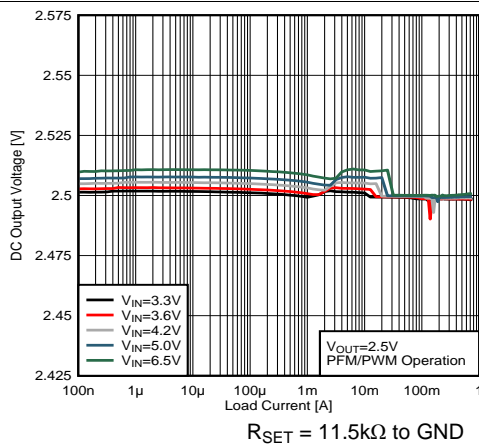


Figure 26. Output Voltage vs. Load Current  
V<sub>OUT</sub> = 2.5V

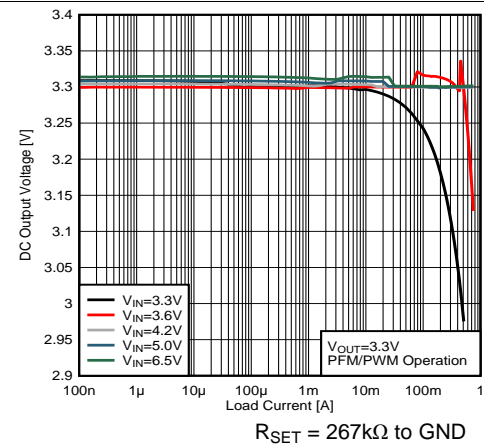


Figure 27. Output Voltage vs. Load Current  
V<sub>OUT</sub> = 3.3V

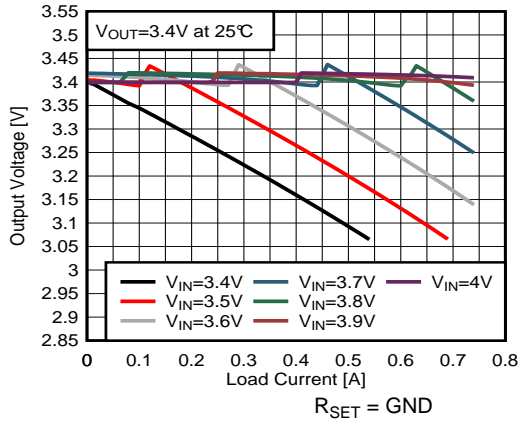


Figure 28. Output Voltage vs. Load Current  
V<sub>OUT</sub> = 3.4V

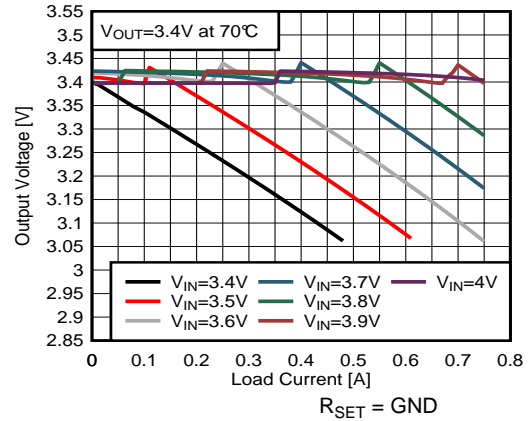


Figure 29. Output Voltage vs. Load Current  
V<sub>OUT</sub> = 3.4V

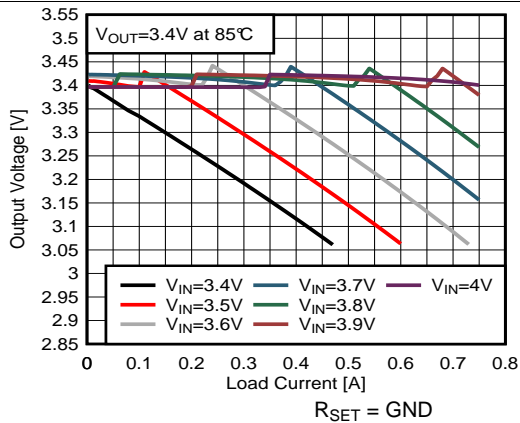


Figure 30. Output Voltage vs. Load Current  
V<sub>OUT</sub> = 3.4V

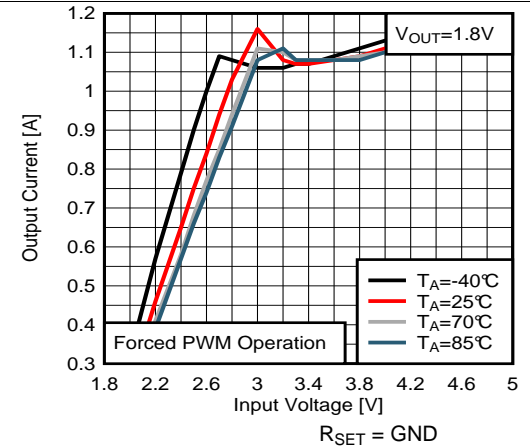


Figure 31. Maximum Output Current vs. Input Voltage  
V<sub>OUT</sub> = 1.8V

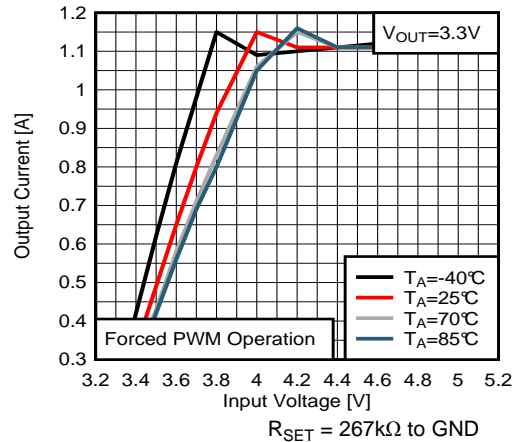


Figure 32. Maximum Output Current vs. Input Voltage  
V<sub>OUT</sub> = 3.3V

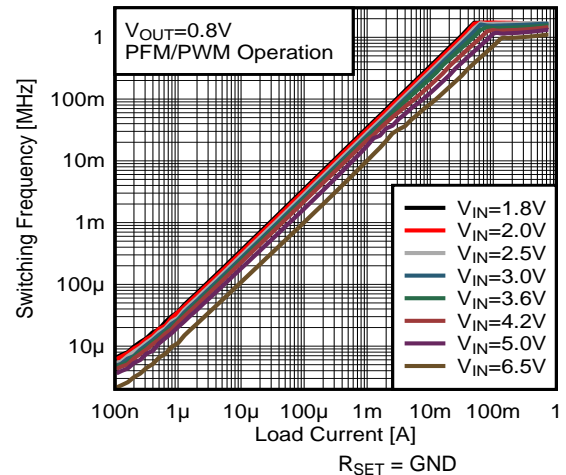


Figure 33. Switching Frequency vs. Load Current  
V<sub>OUT</sub> = 0.8V



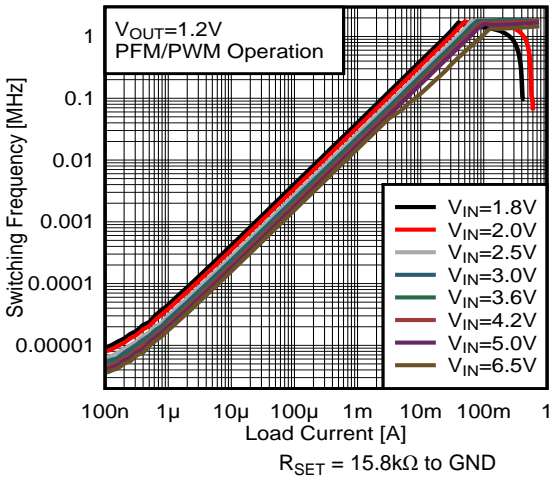


Figure 34. Switching Frequency vs. Load Current  
V<sub>OUT</sub> = 1.2V

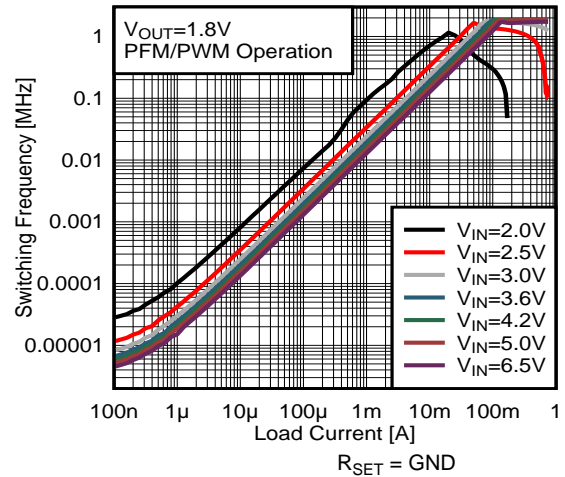


Figure 35. Switching Frequency vs. Load Current  
V<sub>OUT</sub> = 1.8V

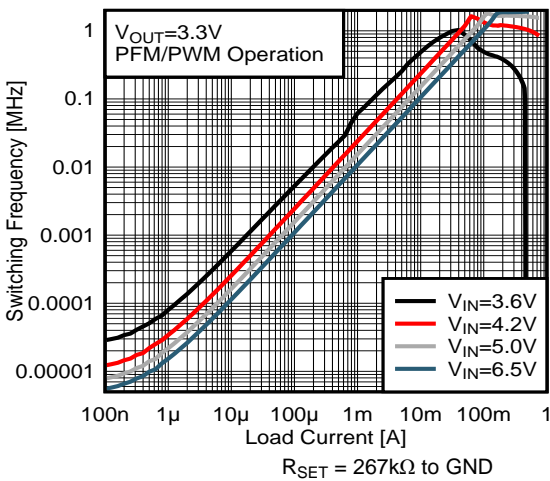


Figure 36. Switching Frequency vs. Load Current  
V<sub>OUT</sub> = 3.3V

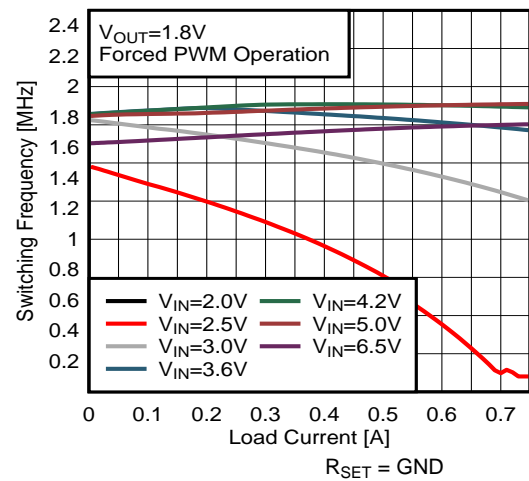


Figure 37. Switching Frequency vs. Load Current  
V<sub>OUT</sub> = 1.8V

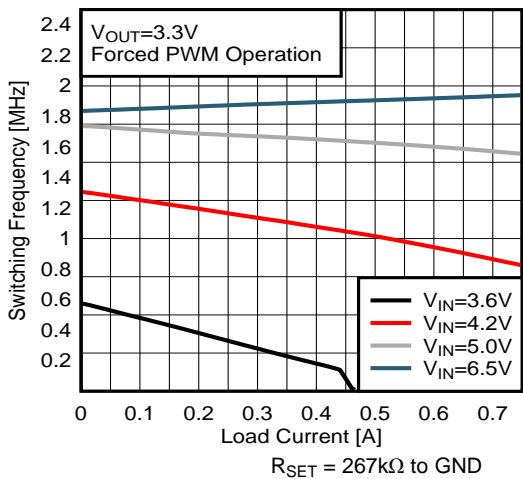


Figure 38. Switching Frequency vs. Load Current  
V<sub>OUT</sub> = 3.3V

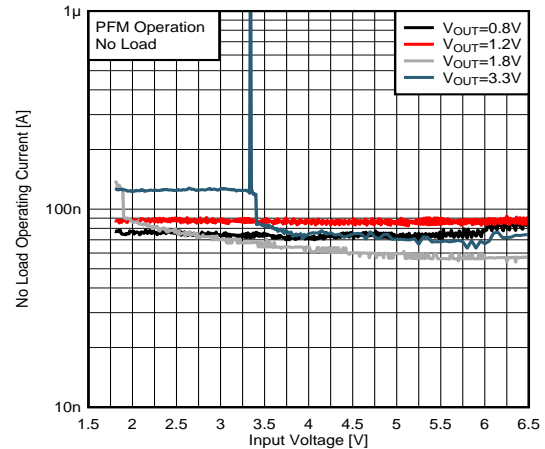


Figure 39. No Load Operating Current vs. Input Voltage

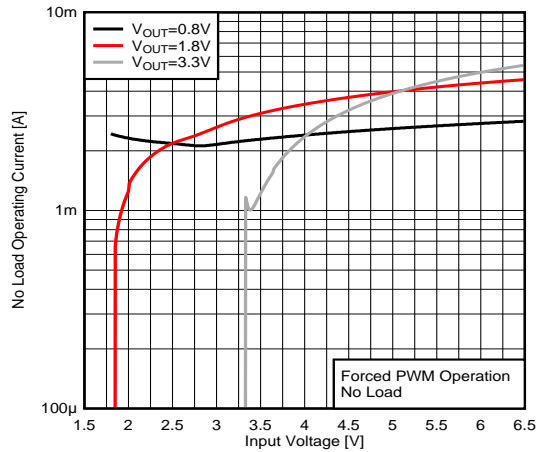
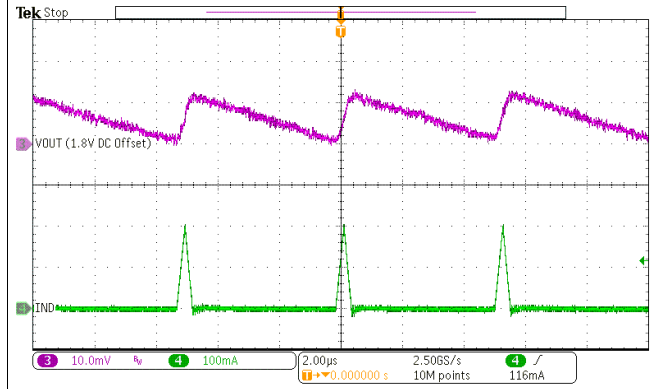
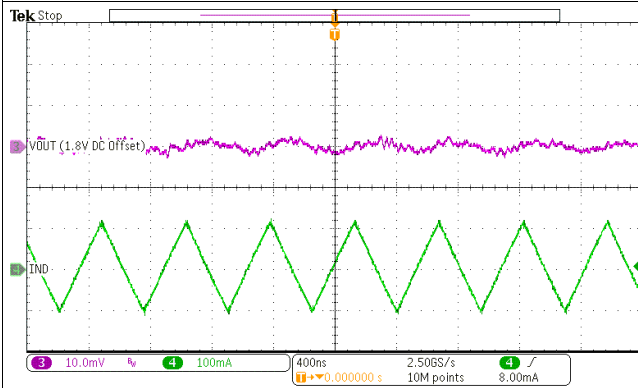


Figure 40. No Load Operating Current vs. Input Voltage



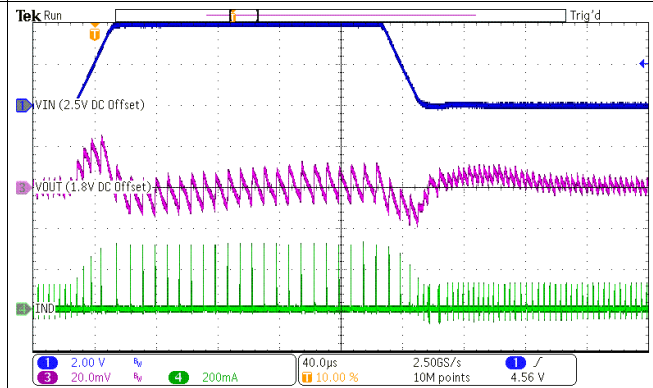
$V_{OUT} = 1.8V$   $I_{OUT} = 10mA$

Figure 41. PFM Operation



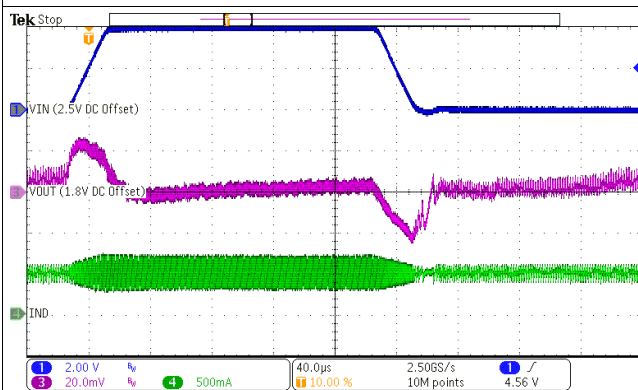
$V_{OUT} = 1.8V$   
MODE = HIGH  $I_{OUT} = 10mA$

Figure 42. PWM Operation



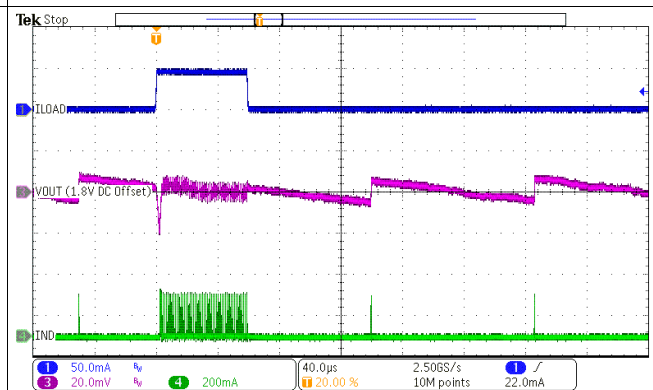
$V_{OUT} = 1.8V$   
rise/fall time = 20µs  $V_{IN} = 2.5V$  to 6.5V  
 $I_{OUT} = 10mA$

Figure 43. Line Transient PFM Mode



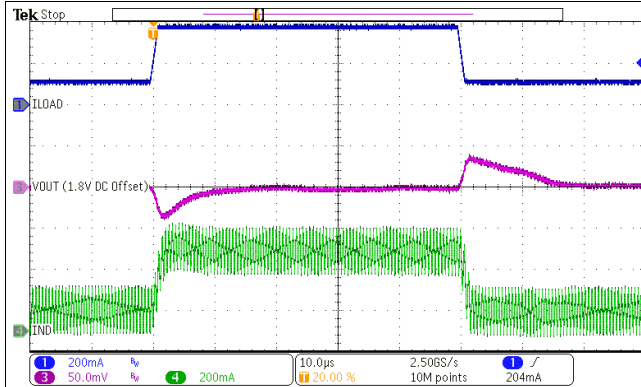
$V_{OUT} = 1.8V$   
rise/fall time = 20µs  $V_{IN} = 2.5V$  to 6.5V  
 $I_{OUT} = 500mA$

Figure 44. Line Transient PWM Mode



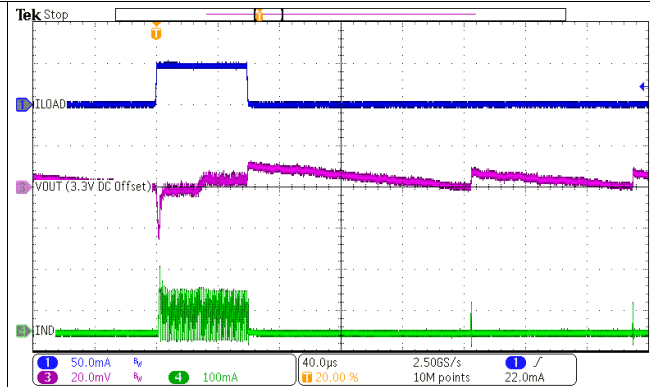
$V_{OUT} = 1.8V$   
rise/fall time < 1µs  $V_{IN} = 3.6V$   
 $I_{OUT} = 125µA$  to 50mA

Figure 45. Load Transient PFM Mode



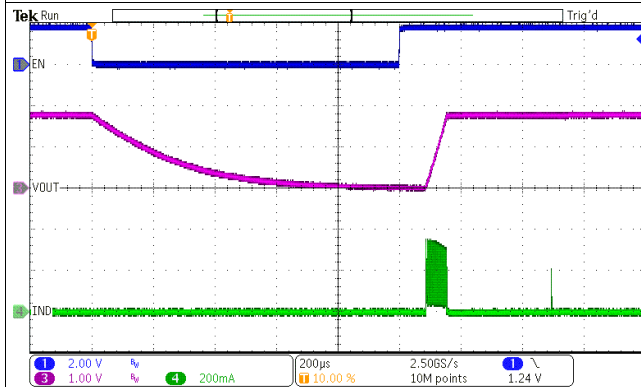
$V_{OUT} = 1.8V$   $V_{IN} = 3.6V$   
 rise/fall time <  $1\mu s$   $I_{OUT} = 125mA$  to  $375mA$

Figure 46. Load Transient PFM/PWM Mode



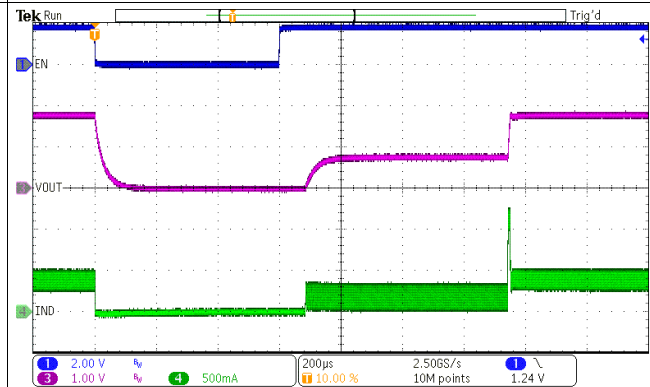
$V_{OUT} = 3.3V$   $V_{IN} = 3.6V$   
 rise/fall time <  $1\mu s$   $I_{OUT} = 75\mu A$  to  $50mA$

Figure 47. Load Transient PFM Mode



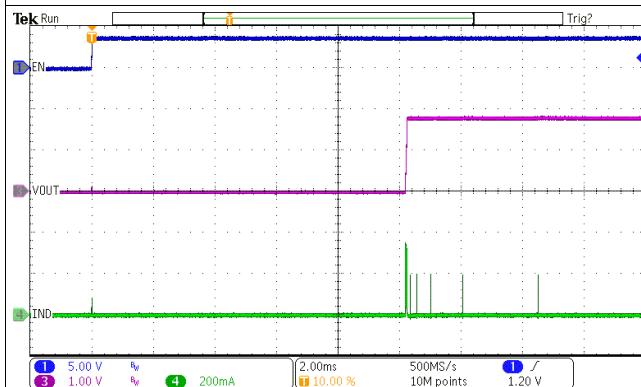
$V_{OUT} = 1.8V$   $V_{IN} = 3.6V$   
 Turned-on via EN input  $I_{OUT} = 0mA$

Figure 48. Startup/Shutdown Into No Load



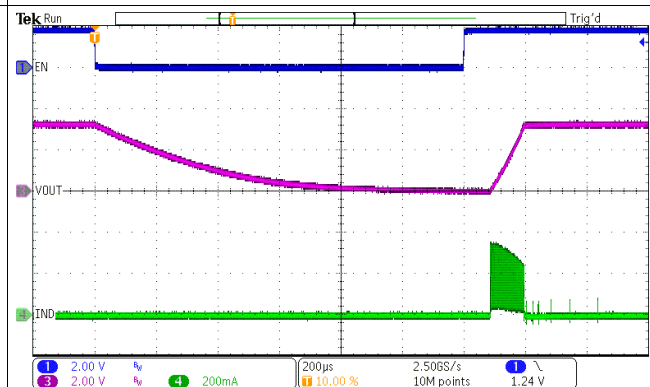
$V_{OUT} = 1.8V$   $V_{IN} = 3.6V$   
 Turned-on via EN input  $I_{OUT} = 400mA$   
 $R_{LOAD} = 4.5\Omega$

Figure 49. Startup/Shutdown Into Load



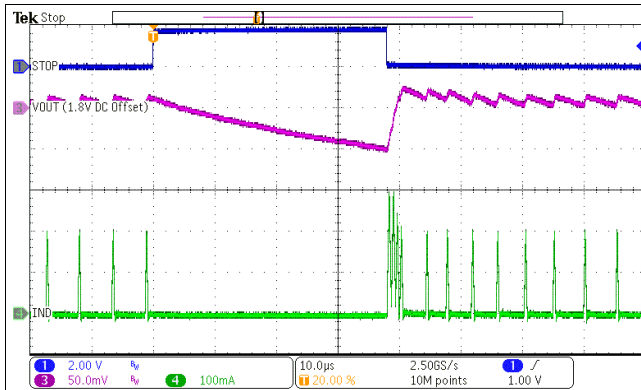
$V_{OUT} = 1.8V$   $EN = V_{IN}$   
 $V_{IN}$  rising from  $0V$  to  $3.6V$   $I_{OUT} = 0mA$

Figure 50. Startup/Shutdown Into No Load



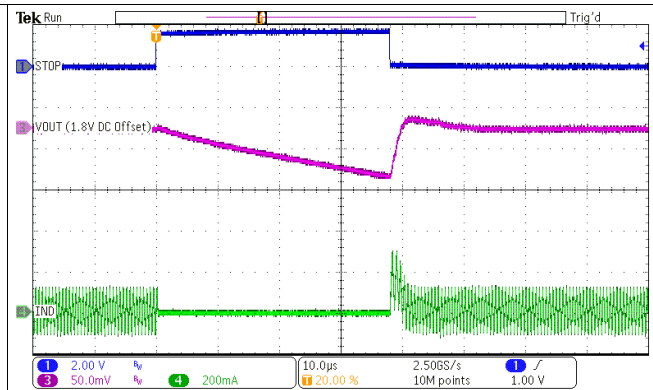
$V_{OUT} = 3.3V$   $V_{IN} = 3.6V$   
 Turned-on via EN input  $I_{OUT} = 0mA$

Figure 51. Startup/Shutdown Into No Load



$V_{OUT} = 1.8V$   $V_{IN} = 3.6V$   
 PFM Operation  $I_{OUT} = 10mA$

Figure 52. STOP Mode Operation



$V_{OUT} = 1.8V$   $V_{IN} = 3.6V$   
 PWM Operation  $I_{OUT} = 10mA$

Figure 53. STOP Mode Operation

### 9.3 System Example

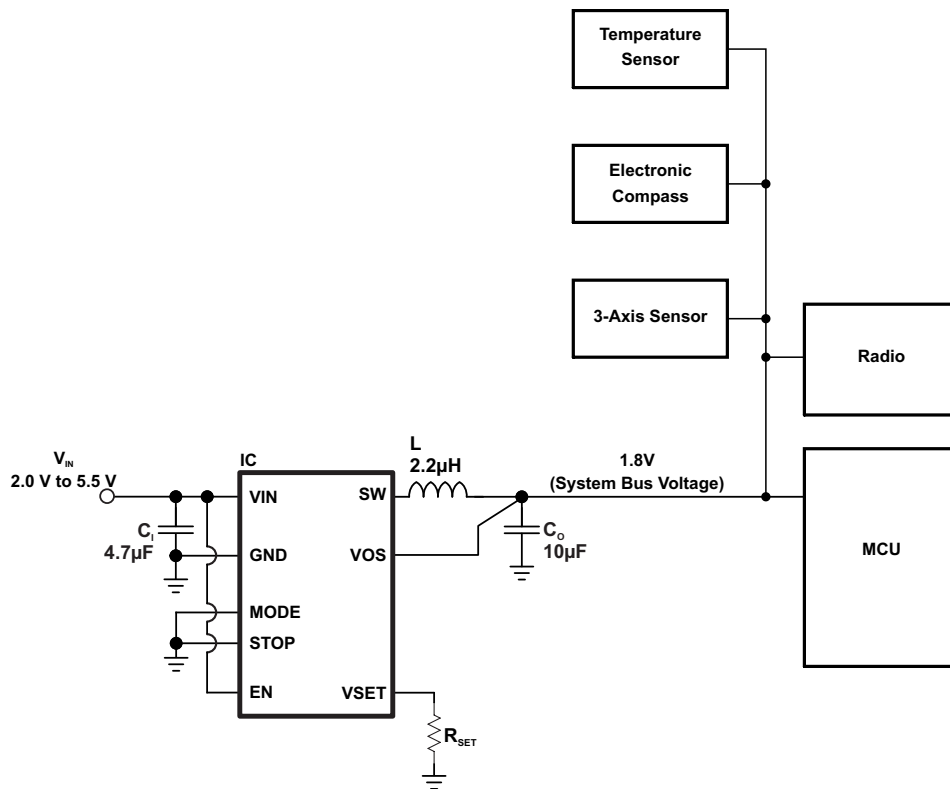


Figure 54. Example Of Implementation In A Master MCU Based System

System Example (continued)

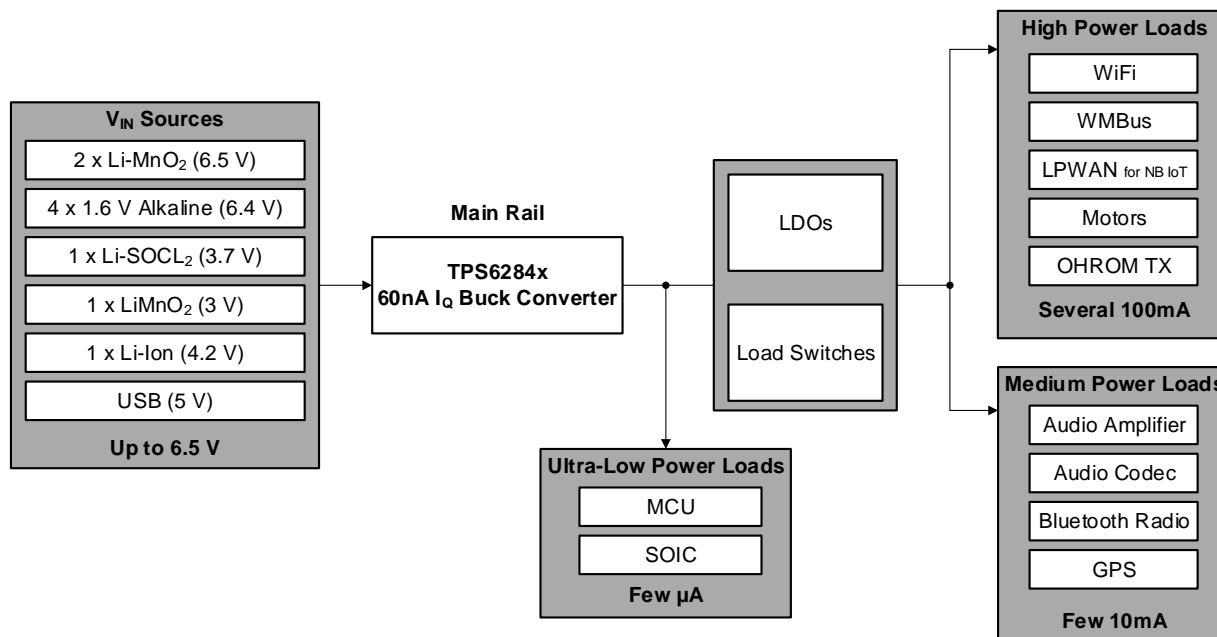


Figure 55. The Broad Range of Input Voltage Sources and Various Power Loads that TPS6284x Can Support

## 10 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage and output current of the TPS62840.

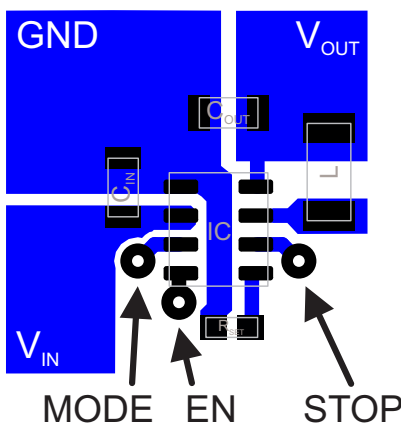
## 11 Layout

### 11.1 Layout Guidelines

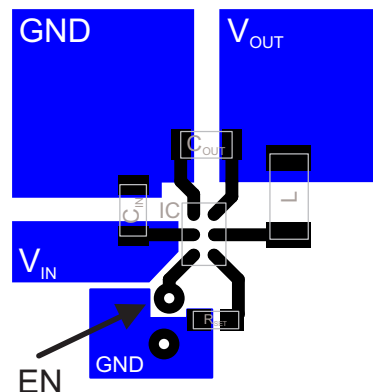
The TPS62840 pinout has been optimized to enable a single layer PCB routing of the device and its critical passive components such as  $C_{IN}$ ,  $C_{OUT}$  and L.

- As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance.
- It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths.
- The input capacitor should be placed as close as possible to the device's  $V_{IN}$  and GND pins. This is the most critical component placement.
- The VOS line is a sensitive, high impedance line and should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line) or other noise sources.

### 11.2 Layout Example



**Figure 56. Recommended PCB Layout  
DLC Package**



**Figure 57. Recommended PCB Layout  
YBG Package**

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

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### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

DCS-Control, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS62840DLCR     | ACTIVE        | VSON-HR      | DLC             | 8    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | E5                      | <a href="#">Samples</a> |
| TPS62840YBGR     | ACTIVE        | DSBGA        | YBG             | 6    | 3000        | Green (RoHS & no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 62840                   | <a href="#">Samples</a> |
| TPS62841DLCR     | ACTIVE        | VSON-HR      | DLC             | 8    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | E9                      | <a href="#">Samples</a> |
| TPS62841YBGR     | ACTIVE        | DSBGA        | YBG             | 6    | 3000        | Green (RoHS & no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 125   | 62841                   | <a href="#">Samples</a> |
| TPS62849DLCR     | ACTIVE        | VSON-HR      | DLC             | 8    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | FF                      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS62840DLCR | VSON-HR      | DLC             | 8    | 3000 | 180.0              | 8.4                | 1.8     | 2.25    | 1.15    | 4.0     | 8.0    | Q1            |
| TPS62841DLCR | VSON-HR      | DLC             | 8    | 3000 | 180.0              | 8.4                | 1.8     | 2.25    | 1.15    | 4.0     | 8.0    | Q1            |
| TPS62849DLCR | VSON-HR      | DLC             | 8    | 3000 | 180.0              | 8.4                | 1.8     | 2.25    | 1.15    | 4.0     | 8.0    | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS62840DLCR | VSON-HR      | DLC             | 8    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS62841DLCR | VSON-HR      | DLC             | 8    | 3000 | 182.0       | 182.0      | 20.0        |
| TPS62849DLCR | VSON-HR      | DLC             | 8    | 3000 | 182.0       | 182.0      | 20.0        |

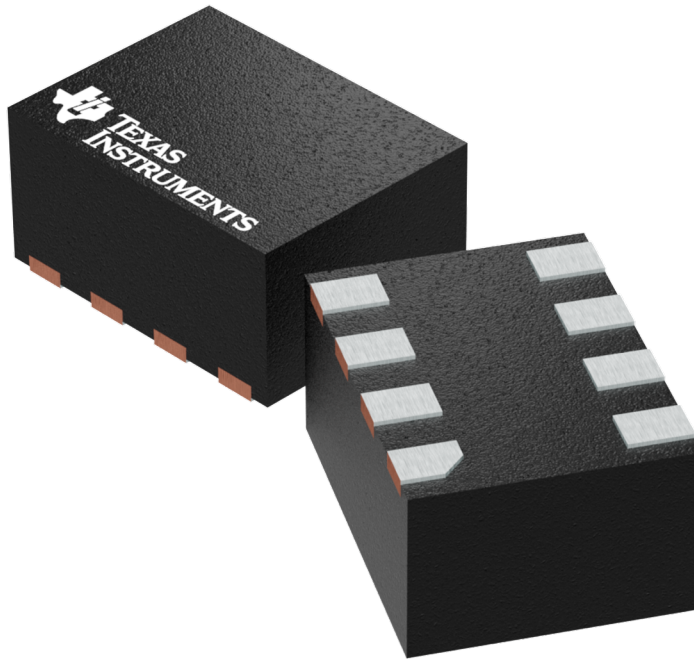
## GENERIC PACKAGE VIEW

**DLC 8**

**VSON-HR - 1 mm max height**

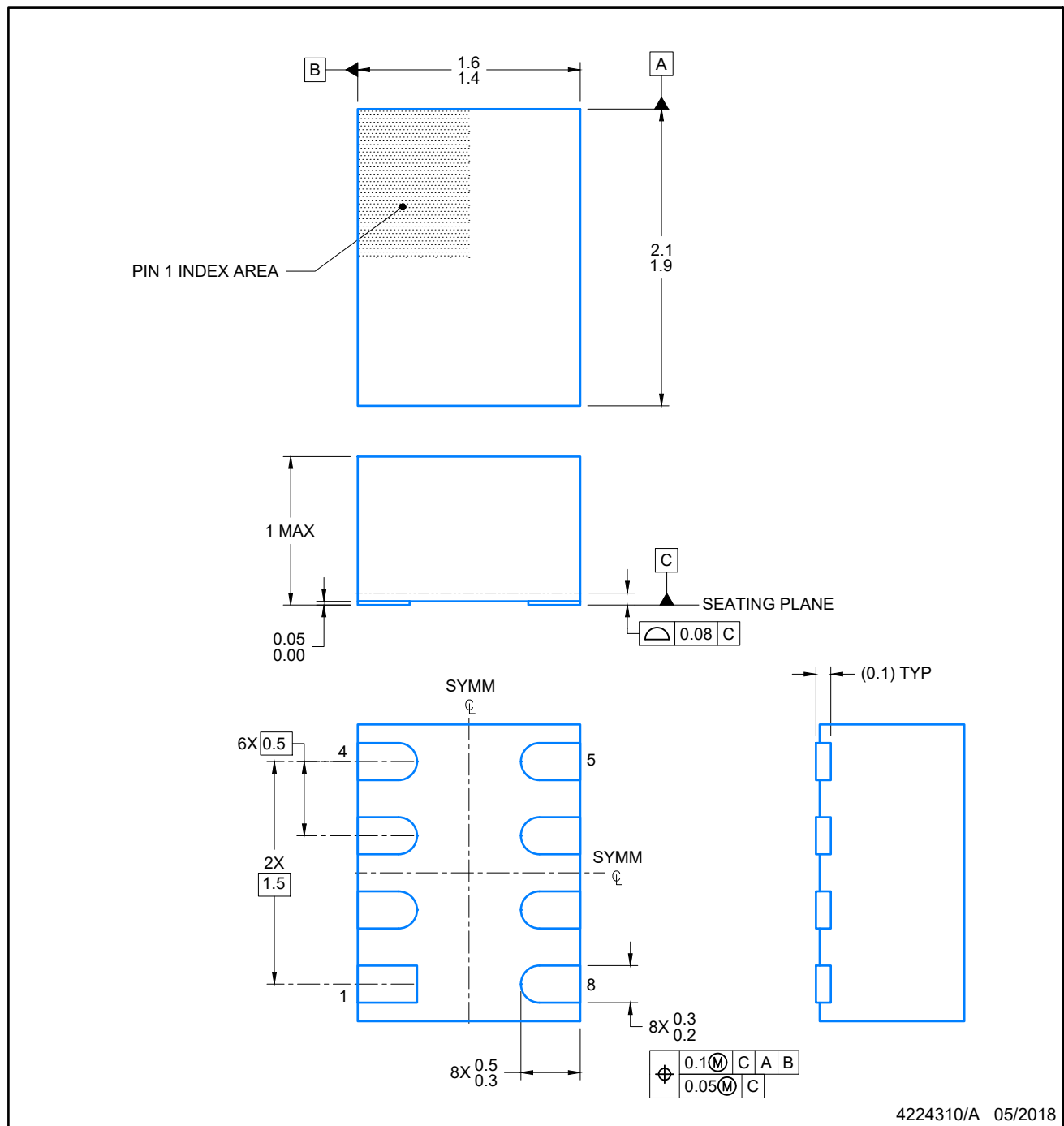
2.0 x 1.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



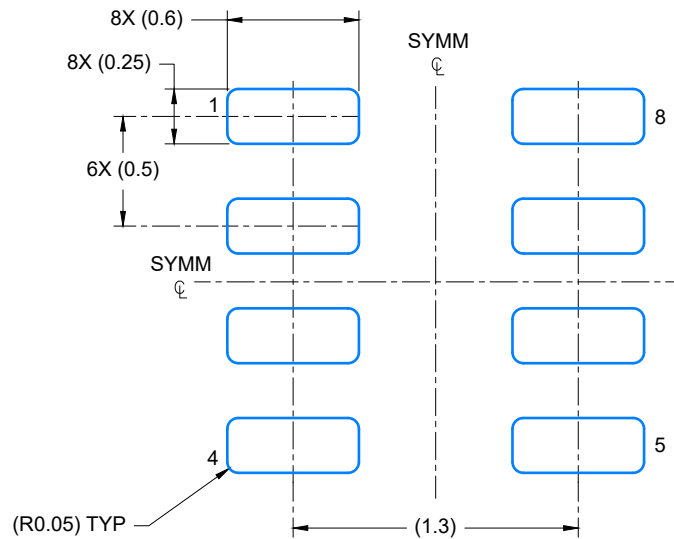
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224379/A

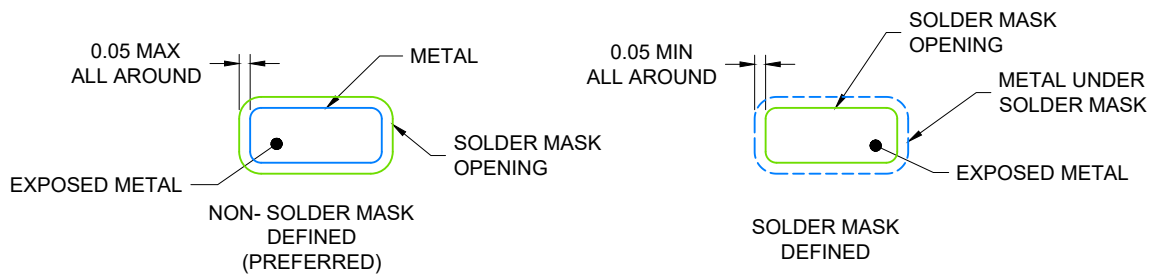


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 30X

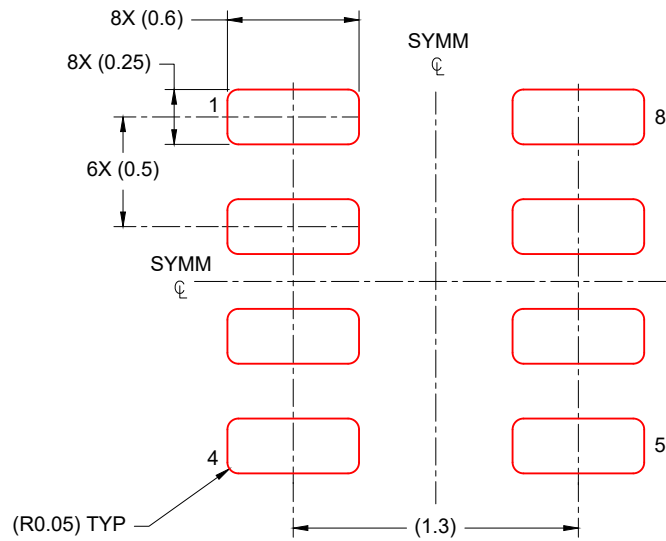


SOLDER MASK DETAILS

4224310/A 05/2018

NOTES: (continued)

- For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 30X

4224310/A 05/2018

NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



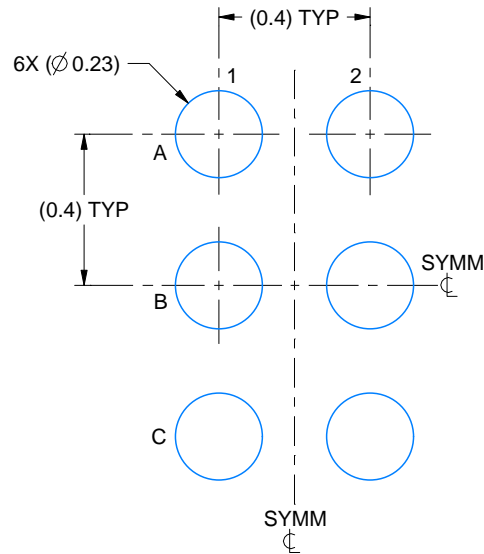


# EXAMPLE BOARD LAYOUT

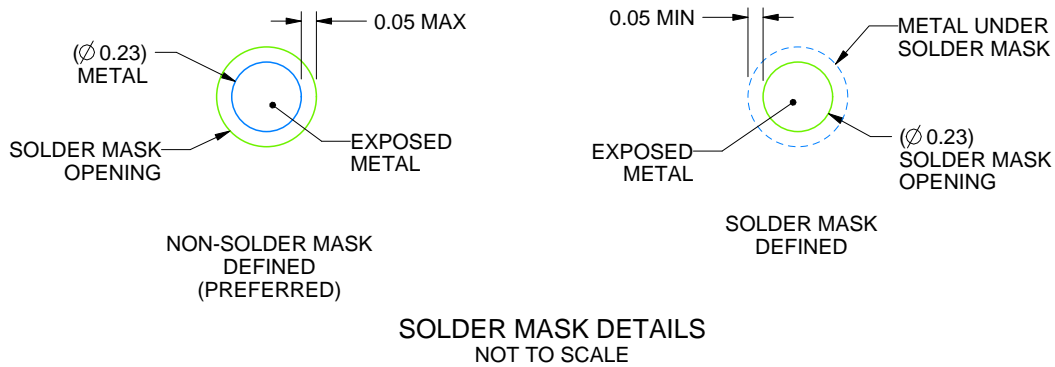
YBG0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 50X



SOLDER MASK DETAILS  
NOT TO SCALE

4224328/A 05/2018

NOTES: (continued)

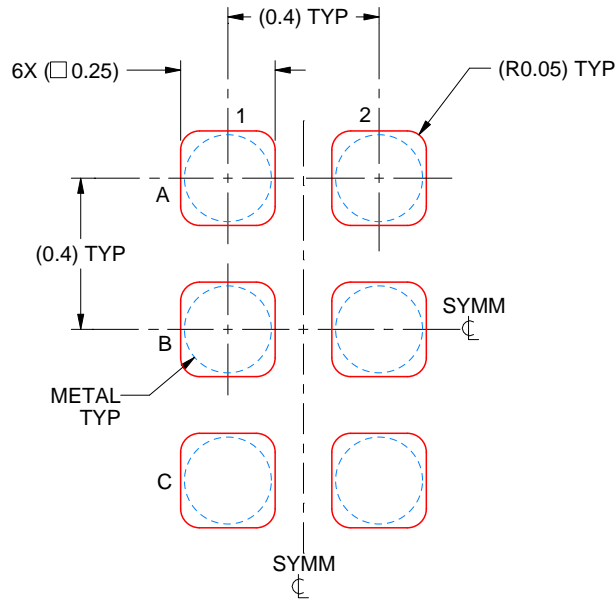
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YBG0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 50X

4224328/A 05/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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